Liquid-Si Technology for High-Speed Circuits on Flexible Substrates

Jin Zhang

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To my family

Contents

Chapter 1

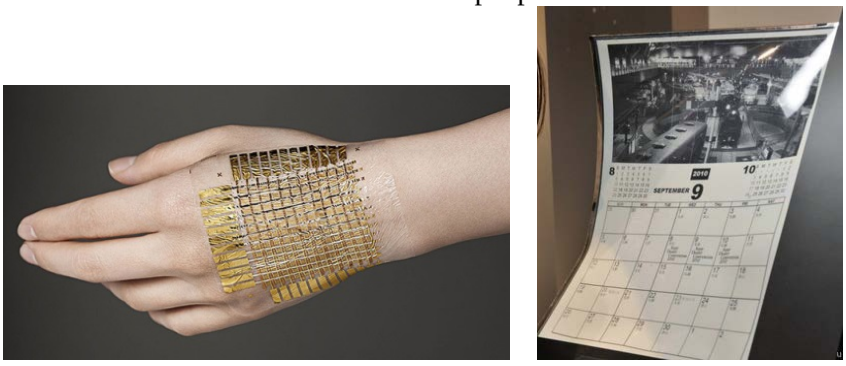
Introduction

This thesis focuses on high-performance single-grain silicon thin-film transistors (Si TFTs), fabricated from a printed liquid-Si solution at a low process temperature, on a flexible substrate. In this chapter, the need for flexible circuits is explained in Section 1.1, together with the fabrication approaches for them. In Section 1.2, the printing method, as a low-cost method for manufacturing the flexible circuits, is discussed in detail. The current research status and the challenges for printed electronics are presented to highlight the urgent need of the single-grain Si TFTs. The ‘super e-paper’, as the final goal, or the final application of this research, is described in Section 1.3, where the structure of the chapters in this thesis is outlined as well.

1.1 Flexible Electronics: Technology and Applications

Compared to electronics on a rigid substrate, flexible circuits are light in weight, transparent, bendable, foldable and rollable, and last but not least, robust, in the sense that they are not so easy to break just by dropping them on the floor or accidently sitting on them. They benefit from large-area fabrication, and thus low-cost manufacturing. They show potential in biomedical applications, life science research and aerospace equipment for special requirements in space. In commercial electronics, there is more and more need for flexible electronics, since the compact form factor, and lighter and more flexible electronics are becoming the trend.

Nowadays, flexible circuits exist not only in theory and in research reports, but also as prototypes for applications in our daily lives. Radio-frequency identification (RFID) tags, as an example of flexible circuits, are emerging for material handling and transport. [1] Flexible smart cards, another example of flexible circuits, which store information and provide registration and access to our work, public transport, etc., would make our lives more convenient. There are more prototypes still under investigation, for example, the electronic skin (e-skin) [2] and electronic paper (e-paper) [3]. There are prototypes in the medical field as well, such as electronic capsules and flexible visual prosthesis. They offer possibilities to help diagnose diseases, release medicine to accurate locations and build artificial vision for blind people.



(a) (b)

Figure 1.1 Photo of (a) e-skin demonstrated by the University of Tokyo and (b) e-paper demonstrated by Sony.

The substrates for the flexible circuits have to be, of course, flexible. Actually, when any solid layer is made thin enough, it becomes flexible. Commonly, glass, organic (plastic), stainless steel and paper are used as flexible substrates. [4][5] Table 1.1 summarizes the important properties of these

materials. The most important property is the maximum process temperature the substrate can handle, without severe physical or chemical deformation. The stainless steel and the glass substrates can be processed with relatively high temperatures. The plastic substrate, which refers to a group of possible polymer substrates, can be processed only up to 350 °C, which is the case for polyimide (PI), due to the limitation of the glass transition temperature. If the process temperature exceeds the glass transition temperature, severe physical deformation would show up, breaking the device layer. Nevertheless, the outgassing from the substrate would happen at a high temperature. Paper is the cheapest among these substrates, but it can undergo the processes only at a low temperature. Besides the process temperature, the transparency, the weight density, the coefficient of temperature expansion (CTE) and the cost, etc., are also important.

Table 1.1 Table of properties of commonly-used flexible substrates

	Glass	Organic		Stainless Steel	Paper
		PEN	PI		
Maximum Process Temperature (°C)	600	200	350	1000	150
Transparent	Yes	Yes	Yellow	No	Yes
Weight (g/m^2)	250	120	120	800	-
CTE (ppm/°C)	4	13	16	10	-
Roll-to-Roll Compatible?	Yes	Yes	Yes	Yes	Yes

The fabrication approaches for the flexible circuits could be generally divided into three types, as indicated in the following three subsections.

Thinning the wafer after fabrication

One way to manufacture flexible circuits is to first fabricate the devices on the c-Si wafer or the SOI wafer in the same way as the traditional IC industry, then thin the wafer to make it flexible, and at last transfer the circuits onto a

flexible substrate. Historically, the first flexible electronics were the flexible solar cells made for satellites in the 1960s.They were manufactured by thinning the Si wafer down to 100 μm and transferring it onto a plastic substrate. [4] This method benefits from the high device performance of the IC fabrication and the advantages of flexible circuits, but the cost of fabrication and material is high.

Fabrication on Chemical Vapor Deposited Semiconductors

Another way to fabricate flexible electronics is to deposit the semiconductor material or the precursor of the semiconductor using chemical vapor deposition (CVD), directly on top of the flexible substrate, or on the flexible substrate with a supporting wafer, and then to fabricate the devices at a relatively low temperature to meet the requirements for the substrate. It is reported that a-Si:H TFTs could be fabricated by plasma enhanced CVD (PECVD) on top of a flexible PI substrate, and released by the Electronics on Plastic by Laser Release (EPLaR) technique. [6][7] With the help of an excimer laser, the deposited a-Si film could be crystallized, and the low-temperature polysilicon (LTPS) TFTs could be manufactured on top of the flexible substrates. [7] This method adapts the fully developed deposition methods of the semiconductor industry, but the need of a vacuum and photo lithography makes the processing costs high.

Fabrication on Printed Semiconductors

The last method is printing the circuits, which implies the deposition of the semiconductor, or the precursor of the semiconductor, by the printing of the ‘ink’ in the liquid phase. Ideally, it does not require any vacuum or photo lithography process, and it is adaptable for all kinds of substrates. Instead of a subtractive process, printing needs an additive manufacturing process, which benefits from simplicity and high throughput. Because of the cost reduction, the printing method is investigated intensively in the research field in recent years.

1.2 Materials for Printed Electronics

The printing method to process the semiconductor devices is attractive due to its low fabrication costs and the possibility it brings to manufacture on large area substrates. TFTs can be fabricated from the printed semiconductors.

The printing methods include screen printing, ink-jet printing, stamping, nanoimprinting and gravure printing, all of which are reviewed and compared in [8]. The screen printing is the method where the solution patterns are pressed

through a patterned mask onto a certain substrate. [8] It is fast and simple, but the printable solutions are limited to the ones with high viscosity, since the pattern has to 'stand' on the substrate after printing. In ink-jet printing, the ink is propelled drop-by-drop onto the substrate, forming the patterns. [8] The process is precise and allows low-viscosity inks, but it takes time to go through the entire substrate unless parallel ink-jet heads are used. Another issue is the high topography of the printed structure, in the sense that the film thickness varies from the edge to the centre of one droplet, which is described as the 'coffee-ring effect'.[9] The stamping method means that a patterned master board is 'inked' and pressed onto the substrate, leaving the pattern. The nanoimprinting method is similar to stamping, but the substrate is 'inked' and the master board is pressed onto it. Nanoimprinting fabricates features as small as 25 nm [10], but both methods need to solve some issues, like the adhesion of the ink to the substrate, to improve the manufacturability. The gravure printing uses a master board as well. The master board is put in the ink, and the extra liquid outside the structures is cleaned with a doctor blade. Using the roll-to-roll technique with the master board as one of the 'rolls', the patterns are printed on the substrate. [8] Thus,the 'doctor-blade coating' method, which is mentioned frequently in this thesis, is one part of the 'roll-to-roll' process for gravure printing. Figure 1.2(a) shows the illustration of the roll-to-roll process.[8]Another process that we have to introduce is the 'slot-die coating' technique, [11] which is shown schematically in Figure 1.2 (b).Similar to the doctor-blade coating, a blade is used for spreading the liquid onto film. However, a slot in the die distributes the ink. The advantage of the gravure printing is the high throughput and the resulting smooth films, but like screen printing, the viscosity needs to be high.

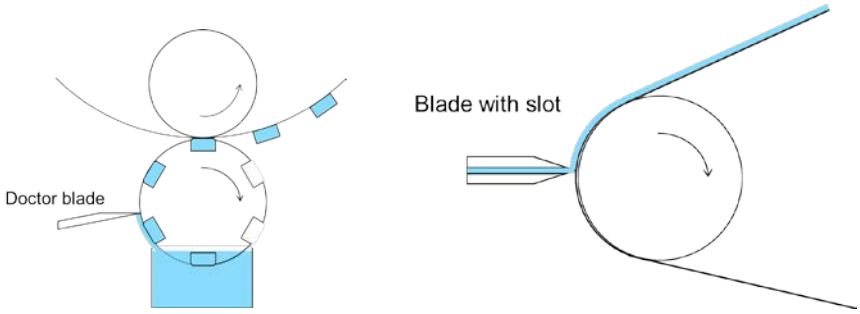


Figure 1.2 Illustration of (a) roll-to-roll process and (b) slot-coating technique.

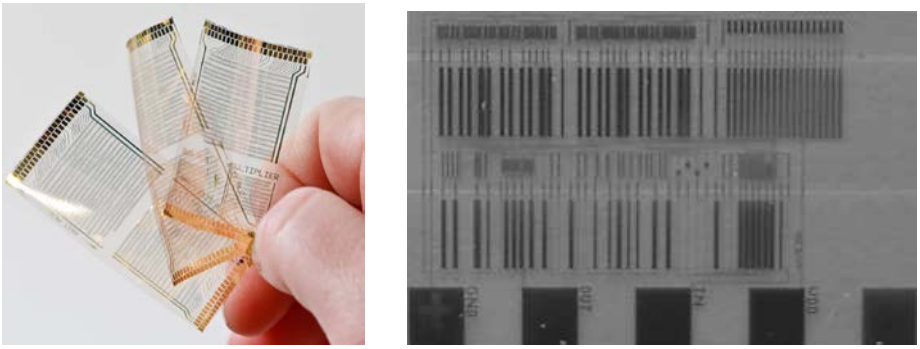
Commonly, all printing methods are done at low temperature and an atmospheric-pressure environment, with the 'ink' in the liquid phase. The 'ink' could first, be the semiconductor itself, which is the case for a lot of organic semiconductors and metal oxide semiconductors. Second, it could be the precursor of the semiconductor, which needs further annealing or crystallization to become a semiconductor, and third,the solution of nanoparticle powders in a solvent, which is usually used for the conducting leads and pads. [4] We would like to further our discussion on the printed TFTs using different semiconductors, including organic TFTs, metal oxide TFTs, and printed Si TFTs. A summary of the above TFTs is listed in Table 1.2.

Table 1.2 List of characteristics of printed TFTs using different materials

	Organic TFTs	Metal Oxide TFTs	Printed a-Si TFTs	Printed poly-Si TFTs
Mobility (cm^2/Vs)	<1	~10	~1	~100
Process Temp.(°C)	20	+	430	430
Reliability	- -	-	+	+
High Transparency	++	++	-	-

Organic Semiconductors

Organic semiconductors are polymer compounds of carbon, hydrogen and oxygen. Originally, they were used as insulators for transistors. They are suitable for the printing process since they are either in the liquid phase, or highly soluble in organic solvents. Their application could be as display drivers, due to their transparency, low deposition temperature and low material cost. Organic TFTs are also highly flexible. Figure 1.3 shows pictures of flexible arithmetic and logic unit (ALU) foils [12] and a flexible organic radio-frequency identification (RFID) chip [13].



(a) (b)

Figure 1.3 Photo of flexible organic circuits with examples of (a) an organic processer, with operation speed of 40 instructions per second, by IMEC [12] and (b) the organic logic circuit as a part of a 13.56-MHz RFID, by the Technische Universität Darmstadt and PolyIC [13].

The carrier mobility of the organic TFTs is low, and it has been recently improved to that of a:Si-H (1 cm^2/Vs). [11][14] Both the PMOS- and the NMOS- TFTs could be fabricated using organic semiconductors, although the NMOS TFTs show an even lower mobility than PMOS TFTs. The organic channel materials are sensitive to water and oxygen, and the resulting reliability issues limit a lot of applications. Despite the disadvantages, organic TFTs show an application potential for low-cost or disposable circuits, which are not critical for carrier mobility and circuit speed.

Metal Oxide Semiconductors

Metal oxide semiconductors, such as zinc oxide, zinc tin oxide (ZTO), indium gallium zinc oxide (IGZO) and zinc indium oxide (ZIO), are good candidates for flexible TFTs. They are highly transparent, and the carrier mobility is relatively high, compared to the organic TFTs. The carrier mobility varies with the process temperature, and a typical value for the low-temperature-processed IGZO TFT is about 10 cm^2/Vs. Recently, the IGZO TFTs have been manufactured on a large scale by Sharp for the pixel and driver circuit of the high-resolution LCD displays. Figure 1.4 shows a photo of a flexible AMOLED display with a backplane carrying metal oxide TFTs.[15]

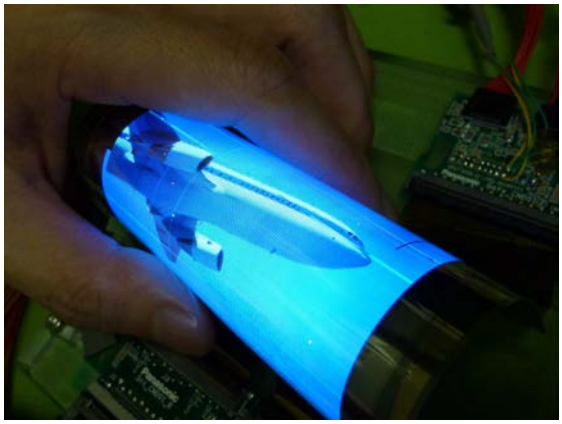


Figure 1.4 Photo of a flexible display, driven by the IGZO TFTs, prototyped by the Panasonic and Holst Centre[15].

Although the carrier mobility of the metal oxide TFTs is still lower than that of crystalline Si, some small-scaled high-speed analog and digital circuits could already been realized using them. Gelinck et al. presented a RFID circuit which works at a radio-frequency of 13.56 MHz, using IGZO for NMOS TFTs and organic semiconductors for PMOS TFTs. [16] At IEDM in 2013, Heremans et al. presented a-IGZO Schottky diodes with a cutoff frequency as high as 1.8 GHz. [17]

Despite all the advantages, metal oxide semiconductor can only be fabricated for either n-channel or p-channel MOSTFT, for example, IGZO for NMOS TFTs and SnO for PMOS TFTs.[18]Thus the complementary PMOS- and the NMOS- TFTs cannot be fabricated using the same metal oxide semiconductor. Multiple-channel materials must be applied for CMOS circuits, or a pseudo-CMOS logic circuit has to be employed. The metal oxide TFTs also suffer from reliability issues, and threshold voltage, V_{th}, shifts under negative bias and light exposure, [19][20] resulting in unstable logic circuits.

Printed Si

This thesis deals with printed Si.

Since neither the organic TFTs nor the metal oxide TFTs have a performance as high as the c-Si counterpart, it is relevant to study the printing of Si devices on flexible substrates. Silane and cyclosilane molecules, which are in the liquid phase when the length of the Si chain is proper, seem to be good candidates for the precursor of printed Si TFTs. Cyclopentasilane (Si_5H_{10}, or CPS)and cyclohexasilane (Si_6H_{12}) could be spin-coated on the substrate, converted to polysilane under UV light, and forma-Si after annealing.

[21][22]a-Si and poly-Si TFTs were made with the CPS precursor at a 430 °C process. The details of the process are discussed in Chapter 2. The carrier mobility of the poly-Si TFT is 108 cm^2/Vs, which is higher than the organic or metal oxide TFTs, but still relatively low due to the existence of the grain boundaries in the channel region. Nevertheless, the processing temperature is much higher than that for organic or metal oxide TFTs, and they could not be processed directly on the plastic substrates (temperature limit 350 °C). Figure 1.5 shows a microscopy image of a TFT with a-Si channel fabricated from the ink-jet printed CPS.

In this thesis, the mixture of the monomer Si_5H_{10}, the polysilane formed by its photon-induced polymerization and solvent, is referred to as the 'liquid-Si' solution.

Besides a-Si and poly-Si for the channel semiconductor, other important layers for IC manufacturing, such as doped Si for the source and drain regions, and SiO_2 for the gate dielectric and for insulation, are also reported to be fabricated from CPS. For n-type doped Si, phosphorus could be dissolved in the CPS monomer or the UV-polymerized CPS. The solution is then copolymerized, coated on the wafer and annealed on a hot plate, the same as the process for a-Si. With the help of post rapid temperature annealing (RTA) and excimer laser annealing (ELA), the resistivity of the doped Si film is in the range of 6.5-27 Ωcm, which is low enough for the source and drain regions. [23] The fabrication process of SiO_2 is similar to that of a-Si process as well, but the annealing process by the hot plate was only partly done before the sample was transferred to the furnace with air atmosphere and the oxidation was done at 450 °C. [24]

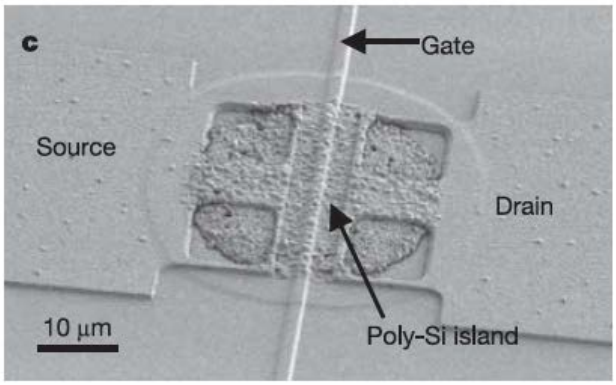


Figure 1.5 Photo of a-Si TFTs from the ink-jet printed liquid-Si solution, reported by Shimoda [22].

1.3 Single-Grain Si TFTs

The poly-Si TFTs face a low-carrier-mobility problem, since there are grain boundaries randomly located in the transistor channel region. If the grain boundaries could be controlled to avoid the channel region, in other words, if the Si grain size is large enough to place the channel of a transistor, in which case the carriers in the inversion layer would not scatter at any of the grain boundaries when drifting, the carrier mobility would be much improved, and the transistor speed would be faster. The transistors, with their channel region inside one single Si crystal grain, are referred to as the 'single-grain Si TFTs', which were first developed by our group. [25]

The 'grain-filters', which are narrow cavities in the SiO_2 substrate, were used to control the location of the single grains. The a-Si film was deposited on top of the grain filters by Low-Pressure Chemical Vapor Deposition (LPCVD) at 550 °C. By treatment with the XeCl excimer laser with a wavelength of 308 nm, silicon single grains would be formed with the grain filter as the center, at the predetermined location. The laser-assisted crystallization method to form Si single grains at the location of the grain filters is referred to as the 'μ-Czochralski process'. The size of the resulted grain could be as large as 7.5 μm, as shown in Figure 1.6. [26] The grain size ensures that the channel region (usually 1 μm in length) of the single-grain Si TFTs could be completely placed inside one single grain. The technical detail of the μ-Czochralski process is discussed in Chapter 2.

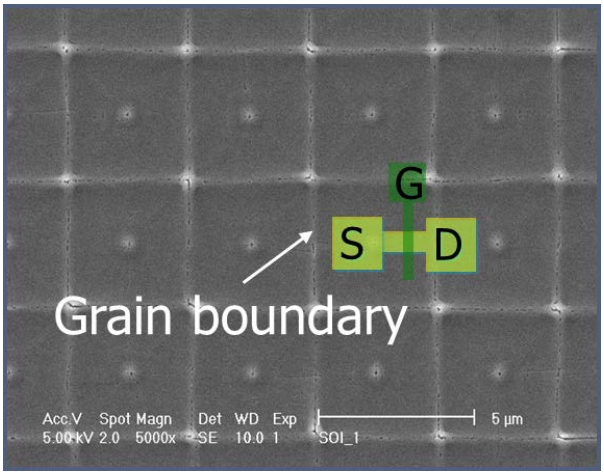


Figure 1.6 SEM image of the single grains crystallized by laser from LPCVD Si.

The single-grain Si TFTs, with their channel region inside one laser-crystallized singl egrain, show electron mobility of 600 cm^2/Vs, which is comparable to SOI MOSFETs. [27] The cutoff frequency of the single-grain Si TFTs is reported to be as high as 5.5 GHz. Our investigation on the single-grain Si TFTs extended to more topics. In Chen's work, not only the location of the grains, but also the orientation of them could be controlled by Metal-Induced Lateral Crystallization (MILC), using IGZO for (111) orientation and Ni for (100) and (110) orientation. The carrier mobility of the NMOS TFT is as high as 998 cm^2/Vs. [28][29] In the work of Arslan, thick a-Si film (1 μm) was crystallized for the application of medical image sensors. [30] Work of Vollebreght and Tajari Mofrad show the possibility of the 3-D circuit integration with single-grain Si TFTs. [31][32]

All the work discussed above are on rigid c-Si wafer substrates and based on LPCVD Si, and the deposition temperature (550 °C),makes it not processable on flexible plastic substrates. Thus the work we have been doing could not be transferred to flexible substrates. We found this problem intriguing, and this led to one of our investigations: Is it possible to process single-grain Si TFTs on plastic substrates at low temperature (<350 °C)?

1.4 Goal of the Research and Outline of the Thesis

The goal of this research is to realize flexible,single-grain Si TFTs from a printed liquid-Si solution. Based on the research already done for the poly-Si TFTs with liquid-Si solution, the focus of our research is on the crystallization to the Si single grains and the processing at low temperature (< 350 °C)of the single-grain Si TFTs on the flexible substrate, with the help of the μ-Czochralski process.

The initial topic of the research could be split and extended into several questions, or points of interest:

- What would be the performance if we combine the liquid-Si process, the μ-Czochralski process and the TFT fabrication process? (Chapter 3)
- How can the process temperature be lowered to meet the requirement of the flexible plastic substrate (< 350 °C)? (Chapter 4)
- What is the influence on the flexible Si TFT performance of the bending stress? How can we improve the flexibility? (Chapter 5)
- Is it possible to fabricate low-temperature (<350 °C) SiO_2 with the liquid-Si solution as well? (Chapter 6)

All these questions will be answered in this thesis. In Chapter 2, the general process flow of the Si TFTs will be introduced, together with a detailed discussion of the liquid-Si process and the μ-Czochralski process. In Chapter 3, the fabrication of the single-grain Si TFTs at a temperature of 650 °C will be presented, showing the promising results of combining the liquid-Si process and the μ-Czochralski process. Chapter 4 will demonstrate an improved approach for the single-grain Si TFT fabrication at a lower temperature of 350 °C on the polyimide substrate, with the result as good as that of the high-temperature processes. Chapter 5 will describe the substrate transfer process for making the devices flexible, and show the possibility of improving the flexibility. In Chapter 6, the fabrication of the low-temperature solution-processed SiO_2will be shown, and one possible application will be discussed. Lastly, Chapter 7 will provide a conclusion and recommendations for future research. Our attempt to make high-frequency transistors is shown in the Appendix.

The printed, flexible Si film with location-controlled single grains, could be used in many fields. It could be employed as the channel semiconductor, the gate oxide (solution-processed SiO2) and the conductive gate (doped Si); it could also be applied to memories, sensors, battery, RFID tags and solar cells, etc., as listed in Figure 1.7. In this thesis, we mainly investigated the application in TFTs, memories and RFIDs. Of course, as a semiconductor which shows a performance as high as single crystalline Si, there are more interesting application fields to be studied.

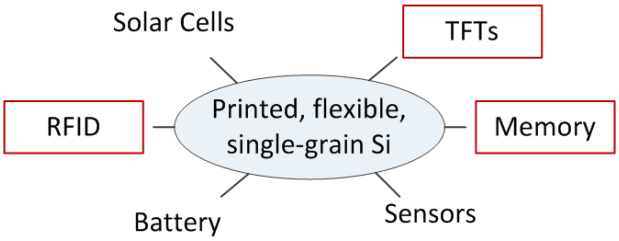


Figure 1.7 Illustration of possible application fields for printed, flexible, single-grain Si film.

Our final goal in this research, or our ambition, is to fabricate the ‘super e-paper’ system (Figure 1.8) with the single-grain Si TFTs from the liquid-Si solution with such a high performance to take the place of the c-Si, integrating the display, the display driver circuit, the RF module, the CPU, the RAM and the analog circuits, together on the same flexible substrate.

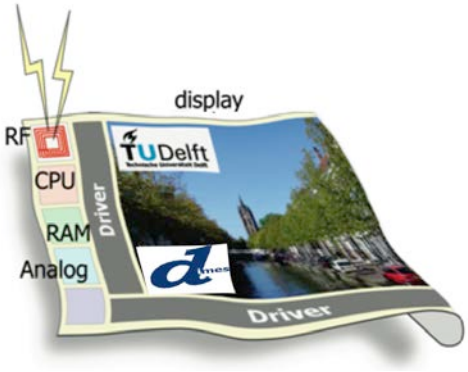


Figure 1.8 Schematic of super e-paper.

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Chapter 2

General Process Flow of Liquid-Si Technology and Single-Grain TFTs

In Chapter 1, we have introduced the background to this thesis and some technical aspects. In this chapter, a more detailed discussion about the fabrication processes will be presented. Top-gated, and standard IC process compatible TFT structures are used in our research. In Section 2.1, the a-Si film deposition from liquid-Si solution is shown, followed by Section 2.2, the dehydrogenation step of the deposited a-Si film with an excimer laser and a flash lamp system. The excimer laser crystallization (the μ-Czochralski process) and activation are discussed in Section 2.3. In Section 2.4, the flowchart of the single-grain Si TFTs is illustrated. The detaching methods to make the devices flexible are listed in Section 2.5. Section 2.6 deal with the characterization method of TFTs. Section 2.7 concludes the chapter.

2.1 Liquid-Si Solution and Formation of Amorphous Si and SiO_2 film

As was explained in Chapter 1, liquid-Si solution is a mixture of cyclopentasilane (CPS) monomer, photo-induced polysilane and solvent. CPS, Si_5H_{10}, is a cyclic compound, with a chemical structure shown in Figure 2.1. CPS is a colorless liquid with a boiling point of 194 °C, and it is highly reactive to oxygen and water.

Si-H compounds, including the open-ring compounds, Si_nH_{2n+2}, and cyclic compounds, Si_nH_{2n}, are liquid-phase at room temperature when $n \geq 3$, and a-Si could be formed if they are heated above 300 °C. [1] But when $n<10$, the boiling point of the compound is lower than 300 °C, which means that the evaporation happens earlier than the a-Si formation and it is difficult to make a-Si film.

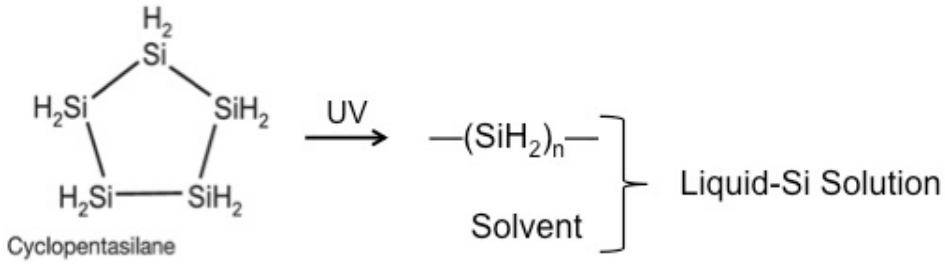


Figure 2.1 The chemical structure of a CPS monomer and the photo-induced polymerization reaction of CPS.

CPS shows high photo-reactivity under UV light. As the polymerization reaction shows in Figure 2.1, under UV light the ring of CPS is opened and it is polymerized to polysilane. According to the study of Shimoda[1], the resulting polysilane is composed of molecules with different molecular weights, and the molecules are soluble in CPS or a mixture of CPS and organic solvent, known as the liquid-Si solution. The liquid-Si solution is transparent and colorless, as shown in the photo in Figure 2.2. The distribution of the molecular weights in liquid-Si affects the wettability, the coating properties and the thickness of the resulting films. Due to the high oxygen reactivity of CPS, the whole liquid-Si process, including the polymerization, the coating, and the thermal decomposition, should be performed in a glove box with both the oxygen and water vapor level lower than 0.1 ppm. Figure 2.3 shows a photo of the oxygen-free glove box in the Dimes Laboratory in TU Delft.

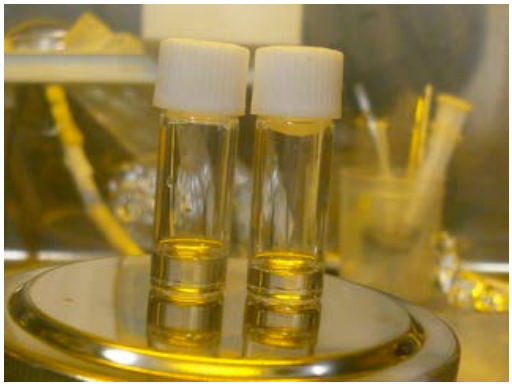


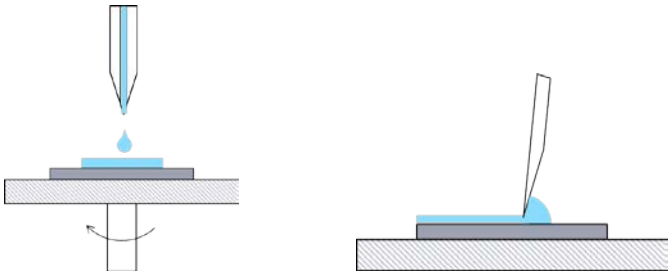
Figure 2.2 Photo of the liquid-Si solution.

Figure 2.3 Photo of the glove box, used for the processing of 100% CPS and the liquid-Si solution in an oxygen- and water-free environment.

The thermal decomposition procedure of the polysilane takes place in several stages. [2] At first, the organic solvent evaporates from the solution. Then at around 280 °C, part of the Si-Si bonds break as a result of the Si-Si bonding energy of 224 kJ/mol. Later at around 300 °C, the Si-H bonds (bonding energy 318 kJ/mol) break and the 3D Si network starts to form. The higher the heating temperature is, the less the hydrogen concentration is in the resulting Si film. A heating temperature that is too low would easily cause oxidation of the resulting Si film. [2]

For 100 nm thick a-Si film, a 21-wt% UV-irradiated CPS solution (liquid-Si) was used. The solution was spin coated on the SiO_2 surface at 2000 rpm and baked at 430 °C for 1 hour to remove the solvent and to form the a-Si film. Figure 2.4 (a) shows a diagram of the spin coating method. The devices made from the resulting a-Si film are discussed in Chapter 3.

Another method we applied to form a 100 nm thick a-Si film is the doctor-blade coating, which is actually one process step of the roll-to-roll process, and shares similarities with the slot-die coating, as we introduced in Section1.2. The doctor-blade coating method is illustrated in Figure 2.4 (b). The 100% CPS monomer liquid was used as the liquid-Si, and it was applied as a coating on the wafer with a Si_3N_4 or polyimide blade on the SiO_2 substrate. The wafer was then treated under a UV lamp for half an hour for the ring opening and polymerization of CPS. The polyimide substrate limited the decomposition temperature to no higher than 350 °C, causing a higher hydrogen concentration in the Si film than that of the 430 °C process. A dehydrogenation step, discussed in the next section, could remove the hydrogen. TFTs are also fabricated with the 350 °C-annealed a-Si film. The film characteristics and the device behavior will be shown in Chapter 4.



(a) (b)

Figure 2.4 Illustration of (a) spin-coating and (b) doctor-blade coating.

SiO_2 formation

SiO_2 film could also be fabricated from liquid-Si solution, as we have mentioned in Chapter 1. Similar to a-Si formation, the SiO_2 film fabrication also takes place in several steps, including the polymerization of CPS to form liquid-Si solution, the use of this solution to coat the substrate, the polymerization of the coated film, the baking of the sample on the hotplate to remove the solvent and oxidize the not completely oxidized Si film. The SiO_2 process includes terminating the a-Si film formation at some stage before the

complete 3D Si network builds up, followed by the oxidation of the incompletely annealed polysilane in air or in oxygen. [3]

A crystalline Si wafer was used as the substrate in our experiment. The wafer was dip etched in 0.55% hydrofluoric acid (HF) for 4 minutes to remove the native oxide and was then transferred into the glove box with an O_2 level of less than 0.1 ppm. The liquid-Si solution was prepared by diluting CPS in a solvent (toluene) to 50 vol%. It was placed under a UV lamp for 3 minutes to start the polymerization, forming a mixture of CPS, polysilane and toluene. It was then coated by the doctor-blade method on top of the c-Si substrate, and was treated under the UV lamp again for 30 minutes to continue the polymerization. The film was baked at 200 °C for 1 hour to form the 3D Si network, after that it was transferred to a furnace with air and baked at 400 °C for 1 hour for the oxidation. [4] At last, the sample was transferred back to the glove box for the post-anneal process to passivate the interface traps, which is performed at 350 °C for 30 minutes in the N_2 atmosphere. [4]

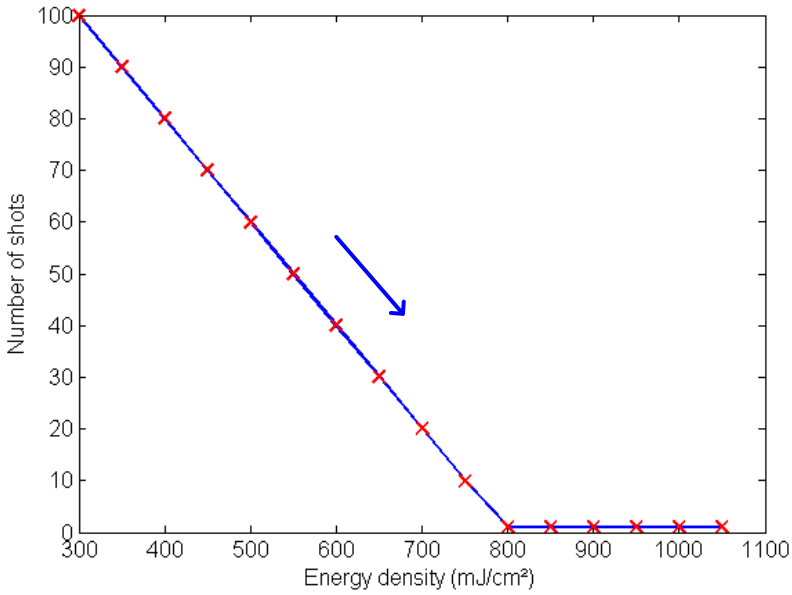
2.2 Dehydrogenation

The presence of hydrogen in the poly-Si TFTs and the a-Si TFTs is usually advantageous, since hydrogen terminates the Si dangling bonds, lowers the potential barriers and enhances the carrier mobility in the TFTs. [5][6] But for the laser-crystallized single-grain Si devices, a lower hydrogen concentration is preferred because a too high hydrogen concentration would cause a hydrogen explosion during the laser irradiation. There are several ways to dehydrogenate the a-Si film.

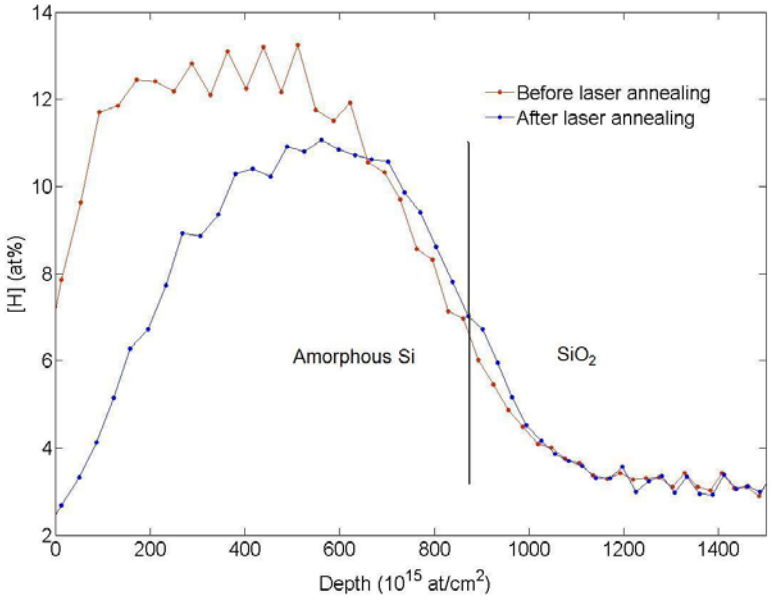
One way is to anneal the film at a high temperature. According to our discussion in the last section, the higher the temperature the polysilane is baked at, the lower the hydrogen concentration is in the a-Si film. Even after film formation, it could be annealed at a temperature higher than the film formation temperature to decrease the hydrogen concentration. We showed in Chapter 3 that in the fabrication of the single-grain Si TFTs the a-Si film was formed after being baked at 430 °C, and that the dehydrogenation step was performed in the furnace at 650 °C in a nitrogen flow (3 liter/min) for 2 hours. After the dehydrogenation, the hydrogen concentration dropped from 6.7e21 atoms/cm^3 to 5.0e19 atom/cm^3, as discussed in Chapter 3 and shown in Table 3.1. The furnace annealing method is effective, but the application is limited by the thermal budget.

Another way to dehydrogenate is by using the XeCl excimer laser with a wavelength of 308 nm. The laser system is illustrated and explained in Section 2.3. A gentle laser treatment with a low laser energy and many repeating shots would break the Si-H bonds, melt the Si film layer by layer, and force the

hydrogen to drift out of the film. [7] [8] Instead of the high-temperature annealing in the furnace, the laser dehydrogenation step can be done at room temperature, thus it is suitable for the polyimide substrate. In Chapter 4, the low-temperature (350 °C) fabrication of the single-grain Si TFTs is shown. The a-Si film was made at a baking temperature of 350 °C, and then dehydrogenated using the laser with a pulse duration of 250 ns and a gentle treatment. The starting energy density of the laser is 100 mJ/cm^2, and the number of shots is 100. Then the energy density increases, and the number of shots at each energy density decreases until 1 shot. The laser recipe is illustrated in Figure 2.5(a). The Elastic Recoil Detection Analysis (ERDA) measurement of the hydrogen concentration of the a-Si film after part of the laser dehydrogenation up to 500 mJ/cm^2 is shown in Figure 2.5(b). The hydrogen concentration at the surface of the film decreased.



(a)



(b)

Figure 2.5(a) Illustration of the excimer laser recipe to dehydrogenate and crystallize the a-Si film and (b) hydrogen concentration measured with ERDA for the a-Si film before and after laser annealing at 500 mJ/cm^2.

Another way to dehydrogenate the film is to use a flash lamp at room temperature and with a higher throughput than the laser. The 'flash lamp' equipment is introduced in Section 6.3. The principle of dehydrogenation by the flash lamp is similar to that of the laser. The Si film is melted slowly and the hydrogen drifts out of the film. An a-Si film made with a heating temperature of 350 °C was used for the test. The film was irradiated by the flash lamp, with the bank voltage increasing from 300 V till 600 V with a step of 50 V. Table 2.1 lists the radiant energy corresponding to the bank voltage. In Figure 2.6 the ERDA result shows that after the flash lamp treatment, the hydrogen concentration in the film dropped.

Table 2.1 List of the energy values corresponding to the bank voltages of the flash lamp

Bank Voltage (V)	Radiant Energy (mJ/cm^2)
300	987
350	1620
400	2377
450	3258
500	4279
550	5459
600	6829

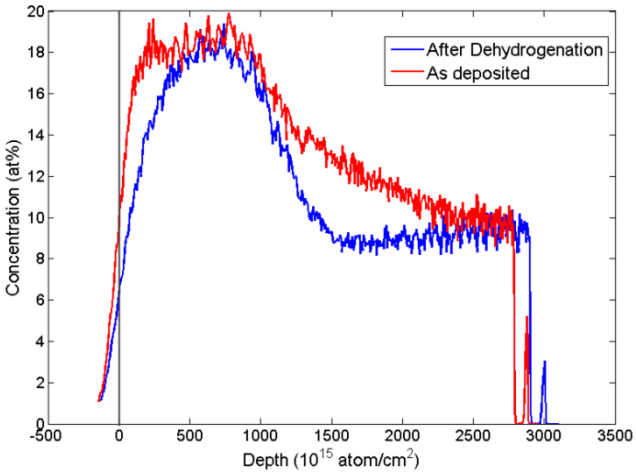


Figure 2.6 ERDA result of (blue curve) the hydrogen concentration of the a-Si film after the dehydrogenation by the flash lamp, compared to (red curve) that of the as-deposited film.

2.3 Laser Crystallization and Activation

The excimer laser crystallization and activation were investigated using a XeCl excimer laser with a wavelength of 308 nm. The laser system is conditioned with the Cleanroom 100 standards and provides fully automated wafer-to-wafer processing. The system is illustrated in Figure 2.7.

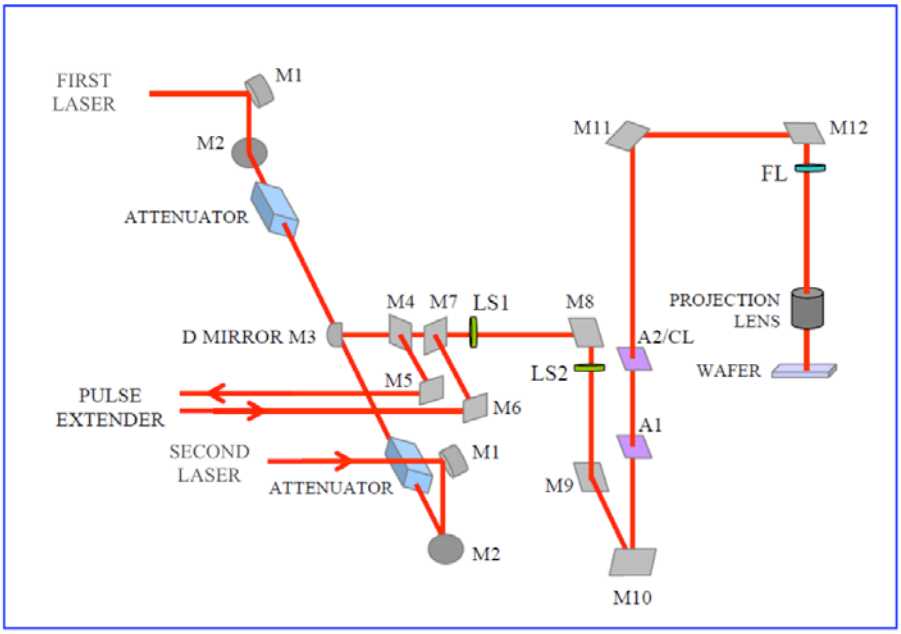


Figure 2.7 Illustration of the components of the laser system.

The laser system is composed of 2 Lamda Physik LPX 200 laser sources (medium: XeCl), with maximum output energy of 350 mJ each, and a pulse width of full width half maximum (FWHM) of 25 ns. The laser beam from the first laser and the one from the second laser are combined by a mirror into a double laser beam. The output pulse width could be tuned by delaying the second laser up to 25 ns with respect to the first laser. If the delay is 25 ns, the combined output beam has a FWHM pulse width of 50 ns. Since the pulse induced by the laser beam is stretched, the delay could be more than 25 ns to output a single pulse. The pulse width could also be tuned by the pulse extender, which extends the pulse up to 8 pulses, generating a FWHM pulse width of 250 ns. Combining the pulse extender and the delay of the second laser, the

maximum output pulse width could be 500 ns. The tuning of the FWHM pulse width is shown in the schematic in Figure 2.8.

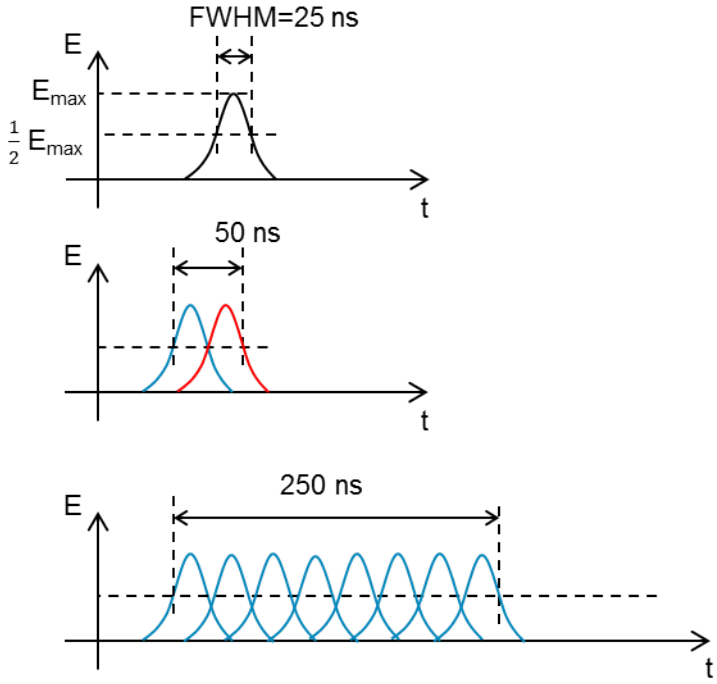


Figure 2.8 Schematic of the FWHM pulse width tuning.

The laser beam passes a homogenizer that changes the shape of the pulse from a Gaussian distribution to a 'top-hat' shape. The speed of the shooting could be accelerated by changing the repetition rate in the range of 1 to 100 Hz. The spot dimension of the laser is defined by a mask, which is 1 mm by 1 mm, or 2.5 mm by 1.75 mm. The wafer chuck could be heated up to 450 °C, and the laser process is done in a vacuum under a pressure of 10^{-7}mBar.

Laser Crystallization: μ-Czochralski Process

The laser crystallization of the a-Si film could be summarized in two steps, melting and solidification. The absorption coefficient of Si is high (10^6 S/cm) at a laser wavelength of 308 nm. The laser beam activates the electron states of the Si atoms, and the energy is converted into lattice vibrations with a time scale of

10^{-12} s. [9] Due to the high heat diffusion coefficient of Si, the laser-induced heat is diffused into the SiO_2 substrate, where SiO_2 acts as the heat sink. [10] When the film temperature exceeds the melting point of a-Si (1147 °C), the a-Si film is melted. After the laser beam is stopped, the solidification starts from nucleation in the film. If the laser energy is not high enough to melt the complete film , the solidification starts from heterogeneous nucleation in the unmelted film. Otherwise it starts from the homogenous nucleation, in both cases resulting in poly-Si film with random locations of the Si grains and the grain boundaries.

To precisely define the location of the single grains and the grain boundaries, the μ-Czochralski process was developed in previous studies of our group. [11] Figure 2.9 shows the schematic of the μ-Czochralski process. First, holes with the dimensions of 1μm by 1 μm were plasma etched in the 750 nm thick thermal oxide by wet oxidation, which is done with the same steps as the alignment markers. Then a second layer of SiO_2 was deposited using TEOS by PECVD with a thickness of 840 nm, resulting in smaller cavities with a diameter of 100 nm and a depth of 700 nm. The cavities are the grain filters, as we mentioned in Section 1.3. The oxide layer for the grain filters is about 1.6 μm in total. For the grain filters on top of polyimide substrate, the total SiO_2 thickness has to be more than 4 μm, in order to cap and passivate the polyimide substrate. Then a 250 nm LPCVD a-Si film was deposited on the oxide layer at 550 °C, filling the grain filters. Under laser irradiation, the Si film is melted until a certain depth in the grain filters is reached, and part of the Si remains solid at the bottom of the cavity. When the laser is terminated, the solidification starts from the bottom of the grain filter, with the solid crystalline Si as a seed, resulting in the single grain growth in the grain filter. Then the grain continues to grow laterally, forming a single Si grain. If the grain filter pitch is smaller than the diameter of the grain, the grains would collide with each other and show a square shape, as shown in the SEM image in Figure 2.10. If the grain diameter is large enough, single-grain transistors could be fabricated with the channel region inside one single grain. The largest grain size we have obtained is 7.5 μm. [12] From the single-grain transistors made inside the grain, the carrier mobility was extracted, which was 600 cm^2/Vs for electrons and 250 cm^2/Vs for holes. The carrier mobility is much higher than that of a-Si transistors (~1 cm^2/Vs [13]) and poly-Si TFTs (~100 cm^2/Vs [14]) due to the absence of the grain boundaries. The cutoff frequency for a TFT transistor is 5.5 GHz, and for Low Noise Amplifiers (LNA), the cutoff frequency was 430 MHz. [15] All the results listed above are based on LPCVD a-Si.

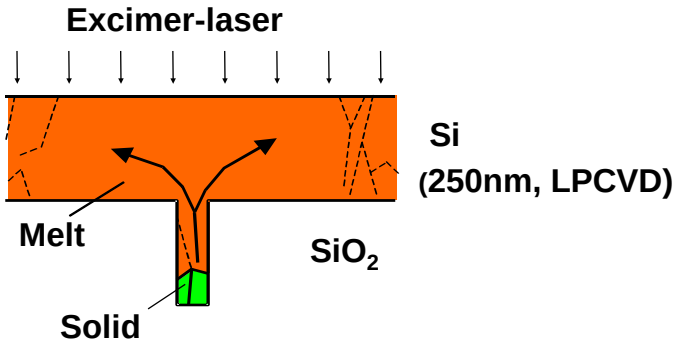


Figure 2.9 Schematic of the µ-Czochralski process.

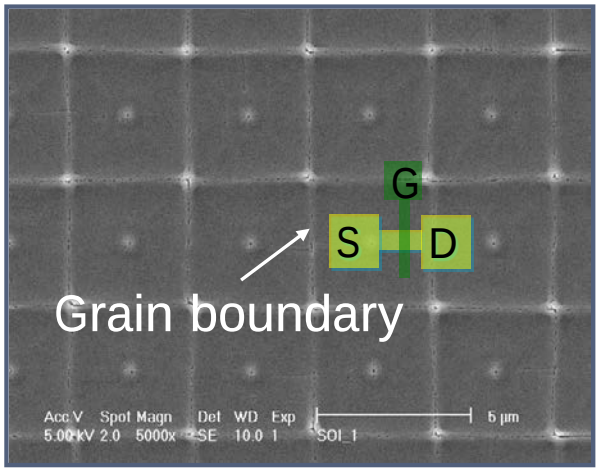


Figure 2.10 SEM image of single grains crystallized by laser from LPCVD Si.

Excimer Laser Activation

The dopants implanted by ion-implantation for the source and the drain region could be instantly activated using the XeCl excimer laser at room temperature. For that the thickness of the underlying SiO_2 layer (4 µm) has to be larger than the heat diffusion length in SiO_2 (about 1 µm); during the laser irradiation the polyimide is at a temperature below the glass transition temperature as long as it is not directly exposed to the laser beam. The Al gate electrode acts as a self-alignment hard-mask not only during the ion-

implantation, but also for the laser activation, under which the Si film remains solid, realizing an abrupt doping profile because no dopants diffuse beyond the liquid/solid interface. Laser activation could result in a high activation level of the dopants, sometimes even higher than the solid solubility. [16] For 100 nm thin Si film, which is discussed in this thesis, the laser activation energy is 300 mJ/cm^2 repeating 5 shots with the pulse duration of 25 ns.

Special Design for Protecting Polyimide

During laser crystallization or activation, direct laser beam irradiation would burn the polyimide substrate, both with and without the capping SiO_2. Because of manual blade coating, the a-Si film does not always cover the surface. The region without the Si film faces the risk of burning the polyimide, as shown in Figure 2.11 (a). It is necessary to design the devices in certain regions to make sure that the laser is only used in the regions covered with Si. One way is to distribute the devices into the squares with a size of 1 mm by 1 mm, the dimension of which matches the spot size of the laser. In 1 die area (1 cm by 1 cm), an 8 by 8 array of squares was defined. Due to the precise alignment of the laser system, only the Si-covered squares were irradiated with the laser.

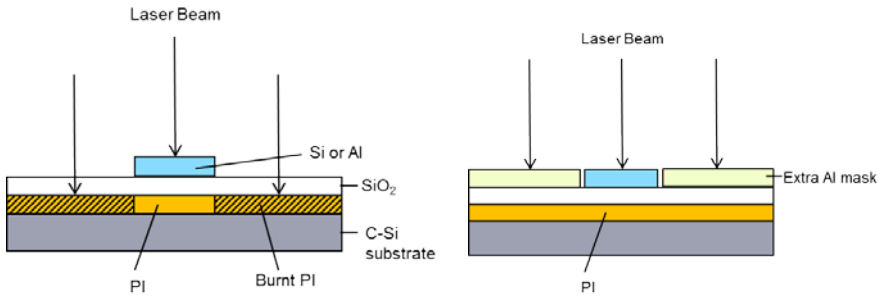


Figure 2.11 Schematic of (a) potential risk of the polyimide directly irradiated by the laser and (b) an extra Al layer for blocking the substrate against the laser during dopant activation.

Another risk of burning the polyimide is during the laser activation of the dopants. In the previous design of our group, the gate mask is designed as an ‘open’ mask, since only the channel region needs to be covered in the dopant ion implantation and in the laser activation, as shown in Figure 2.13(a). While for the design with the polyimide substrate, a more ‘closed’ gate mask is needed

to cover the exposed polyimide outside the gate, source and drain region, as shown in the schematic of Figure 2.11(b) and the layout in Figure 2.12. After the laser activation, an ALRE mask is added to remove the Al outside the gate. Since the maximum shift of the lithography stepper in the Cleanroom 100 is 0.5 µm, a 0.5 µm gap is left between the gate/source/drain of the device and the polyimide protection metal. Experimental results show that the laser going through the 0.5 µm gap does not damage the polyimide. From a processing point of view, to be easily removed afterwards, the gate metal, which is also the polyimide protection metal, should be pure Al instead of Al/Si (99% Al and 1 % Si). Wet etching with H_3PO_4 and CH_3COOH at 35 °C was used to remove the Al.

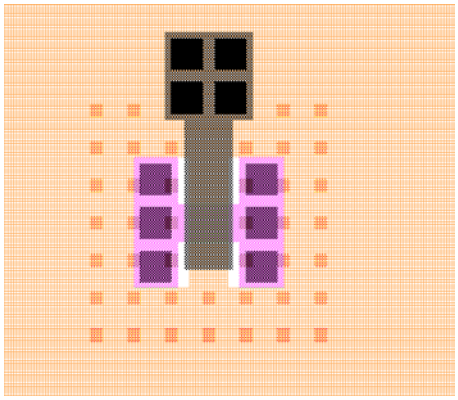
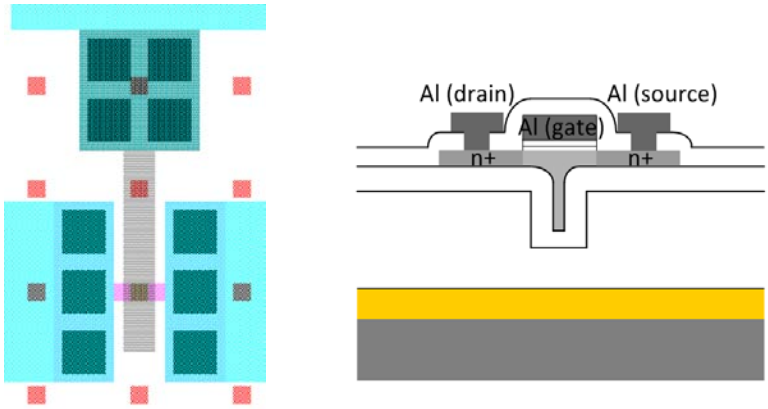


Figure 2.12 Mask design of a TFT with extra Al protection for polyimide. The light orange color is the gate/protection mask, and the grey color is the ALRE mask, which protects the gate electrode in wet etching.

2.4 Process Flow

The top-gated single-grain Si TFT on a flexible substrate is shown in Figure 2.13, in which both the top view and the cross-sectional view are shown. The process flow is shown in the illustration in Figure 2.14. The process flow is divided into steps, including the substrate preparation, the a-Si film formation, the laser dehydrogenation and crystallization, the Si-island etching and gate oxidation, the Al gate etching, the self-alignment source and drain doping and activation, and lastly the passivation and metallization.



(a) (b)

Figure 2.13 The (a) top view and the (b) cross-sectional view illustration of the top-gated single-grain Si TFTs.

Substrate preparation

As shown in Figure 2.14 (a), a 100-mm single crystalline p-type Si wafer was used as the starting material that mechanically supported the plastic substrate layer for ease of handling during the process. Then polyimide (PI115A), as the flexible substrate for the devices, was spin-coated onto the wafer with a thickness of 18 µm (as deposited) and 10 µm (after curing in vacuum at 400 °C for 2 hours). The glass transition temperature of polyimide 115A is 371 °C [17], consequently no process steps with a temperature higher than 371 °C could be used for the fabrication of devices on top of the polyimide substrate. The polyimide on the edge of the wafer was etched to become polyimide-free for the compatibility of processing in Cleanroom 100. Then 4 µm thick SiO_2 by Plasma Enhanced Chemical Vapor Deposition (PECVD) of Tetraethyl Orthosilicate (TEOS) was deposited on top of the polyimide layer at 350 °C to cap the polyimide to prevent contamination. Then the narrow holes, called ‘grain filters’, were created on top of the oxide for making single Si grains using the µ-Czochralski crystallization method (see Section 2.3).

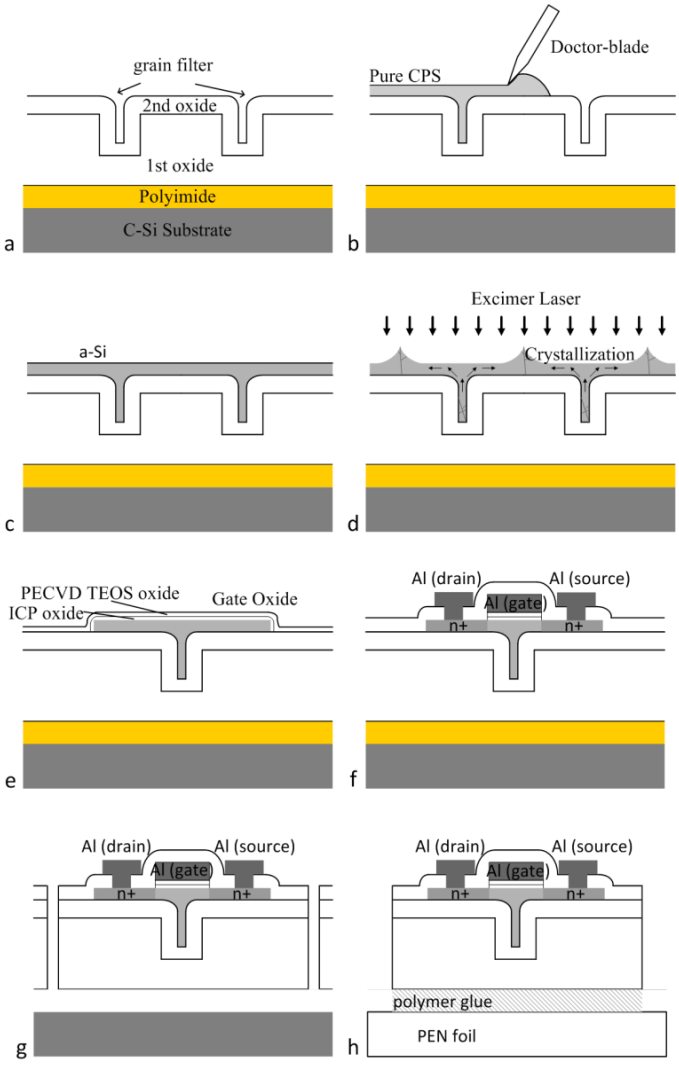


Figure 2.14 Schematic of the process flow of the single-grain Si TFTs on a flexible substrate using a liquid-Si solution.

Liquid-Si coating and a-Si film formation

After the preparation of the substrate, liquid-Si solution was coated on the grain filters by the spin-coating or doctor-blade coating method, shown in Figure 2.14 (b). Then the wafer was irradiated with an UV-lamp to polymerize

the monomers in the liquid-Si solution into polysilane. The sample was put on a hotplate for a thermal treatment to break the Si-H bond and form Si-Si bond, and a-Si was formed, as shown in Figure 2.14 (c). (See Section 2.1) The Si film had a thickness of around 100 nm. The coating and transition of liquid-Si solution to a-Si was performed in a glove box with both the oxygen and the water vapor level lower than 0.1 ppm and at ambient atmospheric pressure. The solution process and no need for a vacuum make it easy to transfer the process to the roll-to-roll printing method.

Laser dehydrogenation and crystallization

Due to the processing-temperature limit of the polyimide substrate, the dehydrogenation has to be done at a low temperature (< 350 °C), with the excimer laser (308 nm) at room temperature, using the recipe shown in Section 2.2. Then the a-Si film was crystallized using the same laser, right after the dehydrogenation. With the help of the grain filters, single grains were obtained on the Si film by the μ-Czochralski process, shown in Figure 2.14 (d). (See Section 2.3)

Si islands etching and gate oxidation

Then the top-gated single-grain Si TFTs were fabricated on the single grains. To restrain the leakage current, the Si film was etched to form Si islands, using the Trikon Ωmega 201 plasma etcher at 20 °C. Next the gate oxide was made using Inductively Coupled Plasma (ICP) oxidation at 250 °C, with a remote plasma source of 13.56 MHz and a power of 500 W. According to a previous study of Tajari Mofrad [18], the interface trap state density of the ICP oxide is in the same order as that of thermally grown oxide, and the standard deviation of the thickness of ICP oxide is only 8 percent. However, due to the low oxidation temperature, the oxidation rate is low, about 12-15 nm in the first hour, and the oxidation rate becomes much slower after the first hour. Thus, an extra gate oxide layer was usually added for the gate oxide by Novellus PECVD oxide using TEOS at 350 °C. A total thickness of the gate oxide layer of 30-50 nm is needed for the functioning of TFTs.

Al gate etching

Next, the gate metal, which was a mixture of 99% Al and 1% Si to prevent spiking, with a thickness of 675 nm, was sputtered by a Sigma Sputter at 50 °C. The metal was patterned by the Ωmega plasma etcher at 25 °C. The gate oxide does not need to be patterned, because of concern that when etching the oxide by plasma, the over etching may damage the thin Si layer. The gate metal was not only used as the gate electrode, but also as the hard mask for the channel

during the self-alignment source-drain dopant ion implantation and laser activation. Sometimes it was also used as the mask to protect the polyimide substrate from the excimer laser in the laser activation of the source and drain dopants, which is discussed in Section 2.3.

Self-alignment source and drain doping and activation

The source and the drain regions were doped using the self-alignment method with the gate electrode as a mask. For NMOS TFTs, phosphorus was implanted as the source and the drain dopant at an energy of 70 keV and a dose of 1.0e16 atoms/cm^2, resulting in a projected range of 85 nm from the gate oxide surface (35-33 nm from the silicon surface) and a peak concentration of 1.21e21 atoms/cm^3. For PMOS TFTs, boron was added as a dopant to the source and the drain region at 20 keV and with 1.0e16 atoms/cm^2, giving a projected range of 66 nm (16-36 nm from silicon surface) and a peak concentration of 1.47e21 atoms/cm^3. The dopants were activated by the excimer laser with an energy density of 300 mJ/cm^2 and 80% overlap at room temperature.

Passivation and metallization

After the laser activation, the passivation oxide was deposited with a thickness of 800 nm, using PECVD SiO_2 by TEOS. The contact holes to source, drain and gate electrodes were opened by plasma dry etching using the Drytek plasma etcher, and 1.4 μm Al/Si (99% Al and 1% Si) was sputtered and patterned by dry etching to make contact pads. Lastly, the alloying took place at a forming gas atmosphere at 400 °C to passivate the Si channel and to alloy the Al/Si interface. For the process on the polyimide substrate, the alloying step has to be skipped.

2.5 Debonding Method

The transistors and the circuits are fabricated on the polyimide substrate on top of a Si wafer, but the wafer serves only for supporting the polyimide substrate and the ease of handling in the processing. The devices need to be detached from the Si wafer to make them flexible. In this section 4 detaching methods are described.

Mechanical Peeling

About 10 μm thick polyimide was spin coated and cured on the wafer, then a 4 μm thick capping SiO_2 layer was deposited to avoid contamination of the clean room, on top of which the devices were fabricated. One straightforward detaching method is to mechanically peel the polyimide off, together with the devices, and transfer them to other substrates, as shown in Figure 2.15. [19] It is a simple method, but it causes stretching of the polyimide film, and stress in the capping SiO_2 layer and the devices.

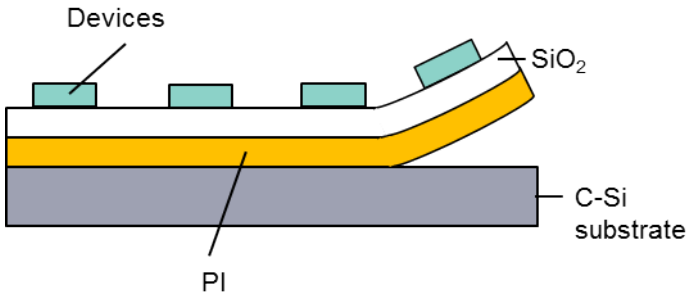


Figure 2.15 Illustration of mechanical peeling method.

Bulk Etch Method

A substitution could be bulk etching the Si wafer from the backside. The device was fabricated on the Si wafer substrate instead of the polyimide substrate. When the fabrication was completed, a 10 μm thick polyimide layer was spin coated on top of the wafer. After curing and opening of the contact holes, the wafer is etched from the backside through the bulk Si until the SiO_2 layer under the devices forms a flexible membrane. [20] The process is illustrated in Figure 2.16. Compared to the mechanical peeling-off method, it solved the mechanical stress problem, but it is not efficient enough since the bulk etching process costs much energy and material.

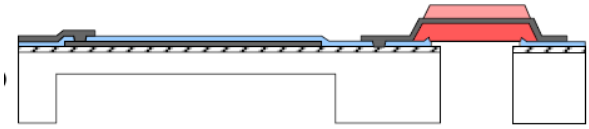


Figure 2.16 Illustration of the bulk etching method to detach the devices from the wafer.

EPLaR Process

Last but not least, we would like to introduce the Electronics on Plastic by Laser Release (EPLaR) process developed by Philips Lab. [21] A polyimide film is spin coated on top of a glass substrate, which is cured and passivated to withstand the TFT process. Low Temperature Polycrystalline Silicon (LTPS) TFTs were fabricated on top of the substrate. Lastly, a laser beam irradiates from the backside through the glass wafer to release the polyimide substrate (with the devices) from the glass wafer, as shown in Figure 2.17. Flexible displays with the polyimide substrate as thin as 5 μm were fabricated with a-Si TFTs.[21] The method offers fast processing and high yield, and consequently the LTPS process could be suitable for mass production in industry. There is no change in the electrical characteristics after the laser release process. [22] However, since a-Si TFTs (0.55 cm^2/Vs, [21]) and LTPS TFTs (~50 cm2/Vs, [22]) are used for the circuits of the EPLaR process, the transistor performance and the carrier mobility are low.

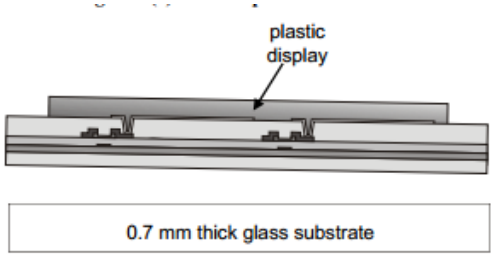


Figure 2.17 Illustration of the EPLaR detaching method.

Detaching Method Applied in This Thesis -'Single-Polyimide Process'

As was introduced in Section 2.4, the TFTs and circuits are on the polyimide substrate placed on a supporting Si wafer. The mechanical peeling method seems to be a good option to detach the devices because of the

similarities in the layer structures. To reduce the mechanical stress in the peeling process, we propose a more gentle way, as shown in Figure 2.18.

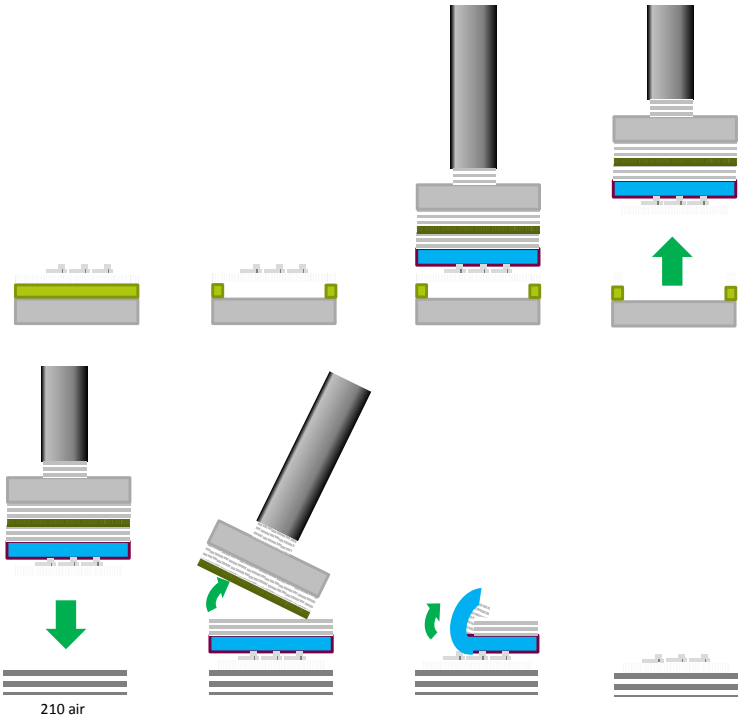


Figure 2.18 Illustration of the substrate transfer process, including the detaching method similar to the mechanical peeling-off method

A tool with the from-bottom-to-top stack of acrylic-based blue dicing tape, double-sided tape and one-die-sized wafer piece was used to detach the devices die by die from the Si wafer, as shown in Figure 2.18. First the SiO_2 layer underneath the devices was etched through with 10 μm by 10 μm holes, to expose the polyimide substrate. Then the polyimide substrate was etched off using an oxygen plasma, resulting in the devices and the underlying SiO_2 floating and only attached to the wafer by polyimide at the edge of the dies. Then the floating devices and the SiO_2 underlying layer were taped to the stacked tool by the blue dicing tape. Next they could be detached easily from the crystalline Si wafer.

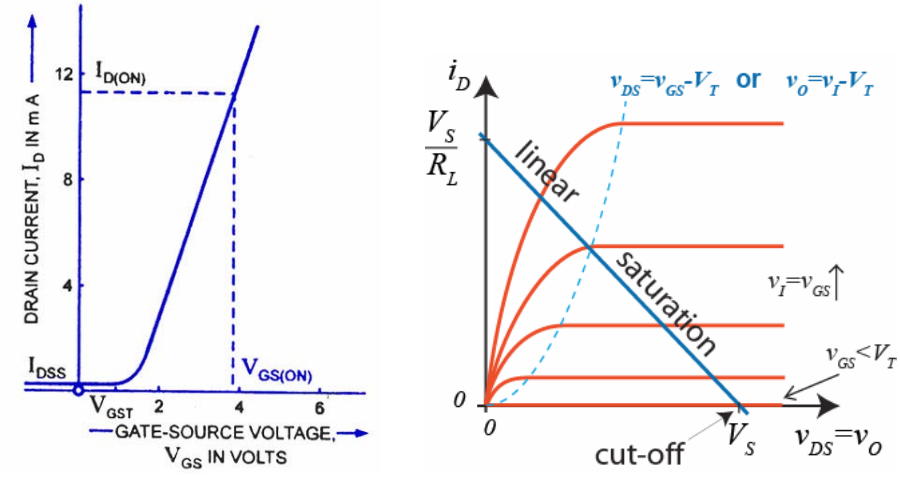
The devices were transferred to a 125 μm thick flexible polyethylene naphthalate (PEN) foil using a glue made of polymers. Then the tool with stacked layers was broken from the middle layers, and the soft blue tape could

be peeled off gently from the devices. Figure 4.8 shows a photo of a die of the single-grain Si TFTs, with the size of 1 cm by 1 cm, transferred to PEN foil. The devices and the circuits were transparent and flexible.

2.6 Electrical Characterizations of TFTs and MOS Capacitors

TFT Characterization

The electrical characteristics of the TFTs are measured on the probe station with the source measurement units (SMU) connected to the Agilent 4156C Precision Semiconductor Parameter Analyzer, driven by the Agilent ICCAP software. The drain current is measured at the preset source, drain and gate voltage points. The important current-voltage characteristics of the TFTs are the transfer characteristics and the output characteristics. Let's take the NMOS TFTs as an example. In Figure 2.19, the transfer characteristics and the output characteristics are shown. [23] From the two characteristics, several important parameters of the TFTs could be extracted, including the electron field-effect mobility (μ_{FE}), the threshold voltage (V_{th}), the subthreshold slope (S) and the on-off ratio (I_{on}/I_{off}). For the characterization of PMOS TFTs and the hole mobility, the case is similar.



(a) (b)

Figure 2.19 (a) Transfer characteristics and (b) output characteristics of NMOS TFTs.

The electron mobility describes how well the electrons would move due to the electrical field. It depends on the semiconductor material and on the quality of the crystalline. μ_{FE} could be calculated from the transfer characteristics in the linear region with a low drain-source voltage, for example, 0.02 V. In the linear region, the drain current I_D is given by the following function with the gate voltage V_{GS}.

$$I_D = \frac{W\mu_{FE}C_{ox}}{2L}[2(V_{GS} - V_{th})V_{DS} - V_{DS}^2]$$

in which, W and L are the width and the length of the transistor channel, and C_{ox} is the capacitance of the gate oxide. From the derivative, the field-effect mobility could be calculated.

$$\mu_{FE} = \frac{L}{W}\frac{1}{C_{ox}V_{DS}}\frac{dI_D}{dV_{GS}}$$
$$\mu_{FE} = \frac{Lt_{ox}}{WV_{DS}\epsilon_0\epsilon_r}\frac{dI_D}{dV_{GS}}$$

in which t_{ox} is the thickness of the gate oxide, ϵ_0 is the permittivity of free space, and ϵ_r is the relative permittivity of the gate oxide. When calculated from the transfer characteristics (Figure 2.19 (a)), the field-effect mobility is not constant for the whole curve. It starts with a low value at the low V_{GS} since the transistor is off, increases with V_{GS} when the transistor is switching on, stays at the value of μ_{FE}, and finally decreases because of velocity saturation.

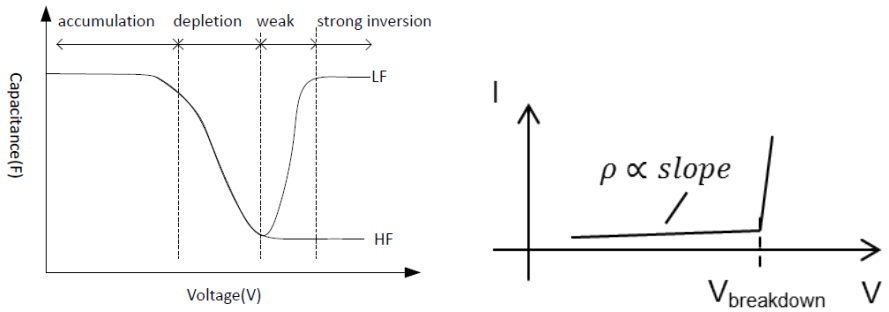
The threshold voltage V_{th} is the voltage that creates the inversion layer in the semiconductor. For Si TFTs, it is determined by the oxide charge, the oxide thickness and the dopant concentration in the channel region. A low threshold voltage is preferred in the TFTs for displays, since a low drive voltage to switch on the transistor could lower the power consumption. For TFTs, there are several ways to determine the threshold voltage. [24] One way is the constant current method, in which the threshold voltage is the voltage at which the drain current is at a given value in the sub-threshold region. Usually values of 10^{-9} A, 10^{-8} A or 10^{-7} A, etc., are used. This method is widely used due to its simplicity, but it is uncertain since the resulting threshold voltage depends on the chosen current. Another widely-used method to determine the threshold voltage is the extrapolation in the linear region, in which the threshold voltage is the intercept value of the extrapolation of the curve in the linear region and the $I_D = 0$ axis. This method is more accurate than the constant current method, but the calculated threshold voltage value varies if the curve in the linear region is not ideal due to the parasitic resistance in the source and drain regions and mobility degradation. In this thesis, both of the above two methods are used.

The sub-threshold slope shows how fast the transistor could be switched from the off-state to the on-state. It measures how much voltage change in V_{GS} is needed for a current change of one decade in I_D. Its value is influenced by the interface state density and the dopant concentration in the semiconductor, while these two cause additional charge in the channel and weaken the impact of the gate voltage V_{GS} on the surface potential. A smaller sub-threshold voltage would improve the on-off ratio.

Lastly, the on-off ratio of a TFT is the ratio of the on-current and the off-current. A high on-off ratio and a low leakage current are desired because of concern for the off-state power consumption.

MOS Capacitor Characterization

The electronic characteristics of the Metal-Oxide-Semiconductor (MOS) capacitors are also measured on the probe station, with the semiconductor parameter analyzer and the additional LCR meter, both of which are driven by ICCAP software. The MOS capacitor characteristics indicate the parameters of the quality of the oxide. For example, the fixed oxide charge Q_s, the mid-gap interface trap density D_{it}, the breakdown electric field strength $E_{breakdown}$, and the film resistivity ρ_{ox}. To extract the parameters, usually the high-frequency capacitance voltage (HF-CV), the low-frequency capacitance voltage (LF-CV), and the current voltage (IV) curves need to be measured.



(a) (b)

Figure 2.20 (a) HF-CV and LF-CV characteristics and (b) IV characteristics of a MOS capacitor.

Figure 2.20 shows the ideal HF-CV, LF-CV and IV characteristics of a MOS capacitor. [23] The CV curves show the MOS capacitance as a function of the bias voltage. Because of the charges in the silicon redistribute with the

applied voltage, the capacitance value is not a constant. Let's take the n-channel MOS capacitor as an example. The case for PMOS is similar.

For the LF-CV behavior, usually four regions could be recognized from the measured CV-curve, as shown in Figure 2.20 (a), which are the accumulation, the depletion, the weak inversion and the strong inversion.

In the accumulation region, the holes in the silicon body accumulate at the interface of Si/SiO_2. Due to the small differential change of the voltage, charges would also change in the accumulation layer and the metal gate, as the charges at the two electrodes of a parallel plate capacitor. Thus the capacitance of the MOS structure is the oxide capacitance.

$$C(acc) = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

in which $\in_{ox}$ is the permittivity and t_{ox} is the thickness of the oxide layer.
In the depletion region, holes in the silicon body near the Si/SiO_2 interface are depleted away from the surface, leaving a space charge region. The differential change in the applied voltage causes a change of the width of the depletion region. So the capacitance of the MOS capacitor is the oxide capacitance in series with the capacitance of the depletion region. It can be described as follows.

$$C(dep) = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_s}}$$

in which C_s is the capacitance of the space charge region in silicon.

As the biased voltage increases, the depletion region width increases, and the capacitance of the MOS capacitor decreases. It reaches its minimum value when the depletion width reaches its maximum value.

After that, the increase in the biased voltage attracts electrons to the Si/SiO_2 interface, forming the inversion layer, since the existence of the electrons reverses the surface Si layer to n-type. In the strong inversion region, the change in the applied voltage makes a change in only the electron charges in the inversion layer. As a result, the capacitance is the oxide capacitance.

$$C(LF\_inv) = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

The discussion above explains the constant-decreasing-increasing-constant trend in the LF-CV curve.

For the HF-CV curve, the case is the same until the inversion region. Since the electron charges in the inversion layer come from the p-substrate, or the electron-hole pairs generation in the space-charge region, both of which supply the electrons with some rate, they could not respond to the change of the high-frequency applied voltage. So the charges change at the far end of the depletion region, and the capacitance stays at the minimum value, but does not increase to C_{ox}.

$$C(HF\_inv) = C_{min} = \frac{\epsilon_{ox}}{t_{ox} + (\frac{\epsilon_{ox}}{\epsilon_s})x_{DT}}$$

in which ϵ_s is the permittivity of silicon and x_{DT} is the maximum width of the space charge region.

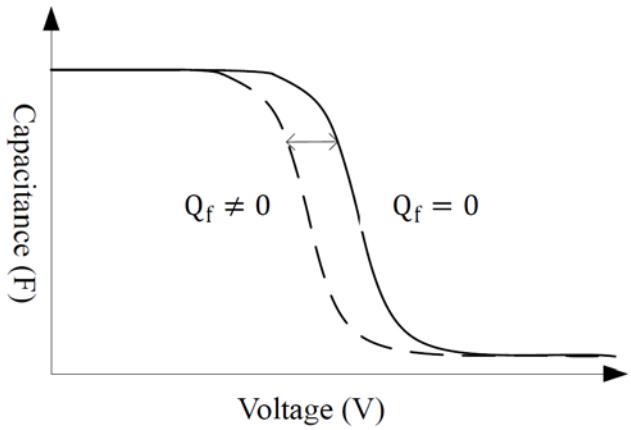


Figure 2.21 HF-CV curve shift due to oxide fixed charge.

As we know, capacitance is the ability of the capacitor to contain charges. It is sensitive to the charge and traps in the oxide. Thus the fixed oxide charge Q_s and the mid-gap interface trap density D_{it} could be derived when comparing the measured CV curve with the ideal curve.

The influence of the fixed oxide charge on the HF-CV curve is in the shift of the curve, as shown in Figure 2.21. When there is a positive fixed oxide charge in the SiO_2 near the Si/SiO_2 interface, extra negative charge is needed in the metal near the metal/SiO_2 interface, to balance the charge and keep electrical neutrality. The curve is shifted by the amount of

$$\Delta V = -\frac{Q_{ss}}{C_{ox}}$$

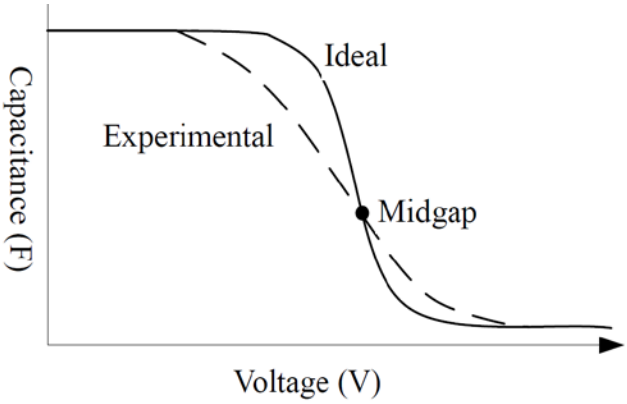


Figure 2.22 Slope change of HF-CV curve due to interface trap states

The influence of the interface trap states is similar but different. The interface trap states exist at the Si/SiO_2 interface and charges could flow between the interface states and the silicon body. They are not charged with a fixed value, but depend on the location of the Fermi level. Generally, the states above the mid-gap level are the 'acceptor states', and below are the 'donor states'. The acceptor states are negatively charged when they are below the Fermi level, and the donor states are positively charged when they are above the Fermi level. They are neutral in other cases. As a result, the HF-CV curve will show a more steady slope when the interface traps exist, as shown in Figure 2.22.

$$D_{it} = \frac{C_{ox}}{q}\frac{d(\Delta V_G)}{d\psi_s}$$

in which q is the electron charge, ΔV_G is the difference of the applied gate voltage and the ideal gate voltage for the same capacitance, and ψ_s is the surface potential, which is the difference between the mid-gap voltage measured in the bulk semiconductor and at the surface.

In practice, when we examine an oxide film using the MOS capacitance characteristics, usually the HF-CV curve is shifted and with a more steady slope due to the existence of both the fixed oxide charge and the interface state. In this case, we have to first shift the curve back to the intersection with the ideal curve to calculate Q_{ss}, then extract D_{it} according to the difference in the ideal slope and the measured slope. In the first step for Q_{ss}, the measured curve is shifted back at the value of the mid-gap capacitance, since at the mid-gap level

the interface is not charged and has no influence on the capacitance value. The capacitance at the mid-gap level could be calculated as follows.

$$C_{mid} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_{s,mid}}}$$

in which $C_{s,mid}$ is the capacitance of the space charge region at mid-gap voltage.

$$C_{s,mid} = \frac{\epsilon_s}{W_{mid}}$$

in which W_{mid} is the width of the space charge region.

$$W_{mid} = \left(\frac{2\epsilon_s \psi_s}{eN_a}\right)^{\frac{1}{2}} = \left(\frac{2\epsilon_s}{eN_a} \times kT \ln\left(\frac{N_a}{n_i}\right)\right)^{\frac{1}{2}}$$

in which N_a is the doping concentration of the semiconductor and n_i is the intrinsic carrier concentration.

In the IV characteristics, the resistivity of the oxide, which is the slope of the curve until the breakdown point, and the breakdown voltage could be read. With the data of the oxide thickness, the breakdown electrical field could be calculated.

2.7 Conclusion

The discussion about the general process flow of single-grain TFTs is shown in this chapter. The liquid-Si technology, the excimer laser characterization and activation, the detaching methods, and the characterization method of the transistor parameters were investigated in detail. All the techniques that were applied in the fabrication process were shown in this thesis of the single-grain Si TFTs from the liquid-Si solution. The changes in the process for specific applications will be discussed in Chapters 3 and 4.

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Chapter 3

Single-Grain Si TFT from liquid-Si with Furnace Dehydrogenation

In the last two chapters, we have introduced the importance of single-grain Si TFTs and the liquid-Si solution, and the process details of them. We have also raised the question of the manufacturability of combining the liquid-Si solution technique with the μ-Czochralski process. In this chapter, manufacturing Si TFTs from solution-processed Si, which offers the possibility of printing Si transistors and circuits, is discussed. In Section 3.1, we introduce more about the background of the printed Si transistors. In Section 3.2, the formation, the dehydrogenation and the crystallization of the Si film from liquid-Si solution with a process temperature as high as 650 °C, is shown. Section 3.3 deals with the fabrication and the characteristics of the Si TFTs on Si single grains with a standard Si TFT process. In Section 3.4, the chapter is summarized.

CHAPTER 3 SINGLE-GRAIN SI TFT FROM LIQUID-SI WITH FURNACE DEHYDROGENATION

3.1 Introduction

As we mentioned in Chapter 1, for flexible electronics printing is an attractive option as it does not require a vacuum and photolithography processes, resulting in low-cost manufacturing. Previous studies focused on printed organic semiconductor TFTs and metal oxide TFTs, but unfortunately the carrier mobility and the device reliability are inferior to those of Si devices, as discussed in detail in Chapter 1. Liquid-Si has a proven ability to be applied in the manufacture of Si devices, but its use has not been reported in the fabrication of single crystalline Si TFTs.

In this chapter we present the fabrication of single-grain (SG) Si TFTs, with a performance as high as the crystalline Si counterpart. This is the first time that single-grain Si TFTs are reported to have been fabricated with the solution process. By a-Si film formed on the precursor of spin-coated liquid-Si solution followed by the μ-Czochralski process, single-grains with a diameter as large as 3.5 μm were made at predetermined positions of the grain filters. The carrier mobilities of the TFTs made in Si single grains are 423 $cm^{2/}Vs$ and 118 cm^2/Vs, for electrons and holes, respectively.

The fabrication process is limited to a maximum production temperature of 650 ºC for the a-Si film dehydrogenation. This temperature is too high for the flexible plastic substrates. Despite that, the solution process, the absence of a need for a vacuum and the high device performance make this technology a strong candidate for replacing the LPCVD Si.

3.2 a-Si Film Formation, Dehydrogenation and Crystallization

We used the μ-Czochralski process [1] to control the position of Si grains. Figure 3.1 shows a schematic view illustrating the fabrication process. First, a grid of grain filters is formed on the SiO_2 substrate, on top of which liquid-Si solution was spin coated. After UV illumination and baking treatment, a-Si film is obtained. The process details are explained in Section 2.1 and Section 2.2. Raman spectroscopy (Figure 3.2) shows that after baking a-Si film was formed. The film thickness was 112 nm. Figure 3.3 shows the cross-section SEM image of the silicon film and the grain filters. It can be seen that the grain filters are completely filled by liquid silicon. Unlike LPCVD Si, which usually shows an indentation at the position of the grain filters, the surface roughness can be observed only when the sample was tilted. (Figure 3.4)

Next the film was pre-annealed in a furnace at 650°C for 2 hours to dehydrogenate the a-Si film, as indicated in Chapter 2. After annealing, the hydrogen concentration of the a-Si film, measured with Time-of-Flight Secondary Ion Mass Spectrometry (TOF-SIMS) decreased from $6.7x10^{21}$ cm^{-3}

to 2-5x10^{19} cm^{-3} (see Table 3.1), and the film density, measured by XRR (X-Ray Reflectivity), increased from 1.96 g/cm^3 to 2.328 g/cm^3, of which the latter is exactly the same as that of the crystalline Si substrate. [2] The thickness of the film decreased to 88 nm. The dehydrogenation step by furnace is reducing the H concentration by 2 orders of magnitude; however, the furnace temperature of 650 °C is the highest process temperature in the fabrication and it limits the selection of the substrates. In the future, to solve the application limitations due to the high temperature, a furnace step with a temperature of 450 °C can be used to replace the step with that of 650 °C. It is reported that this results in a sufficient dehydrogenation level for laser crystallization. [3]

Next the crystallization of a-Si film was investigated using a XeCl excimer laser (308 nm) with a pulse-duration of 25 ns or 250 ns at a substrate temperature of 450 ºC or 20 ºC, with the laser energy densities varying from 450 mJ/cm^2 to 1400 mJ/cm^2.

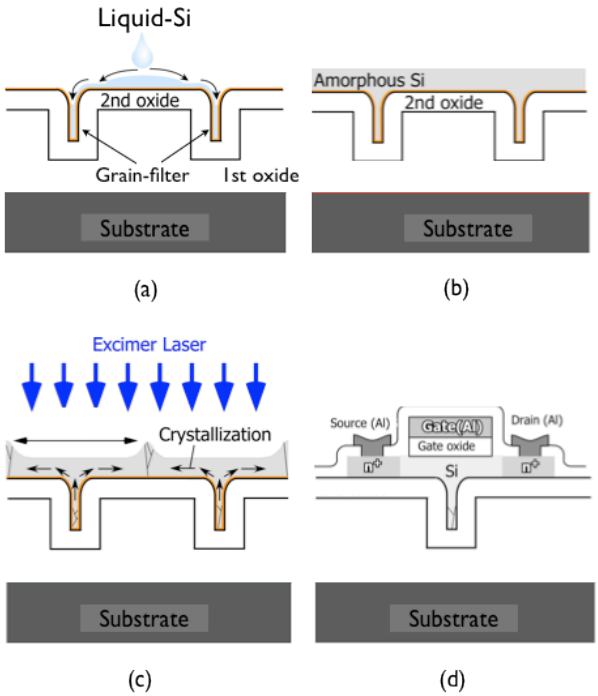


Figure 3.1 Schematic view of the fabrication process of the single-grain Si TFT using liquid-Si

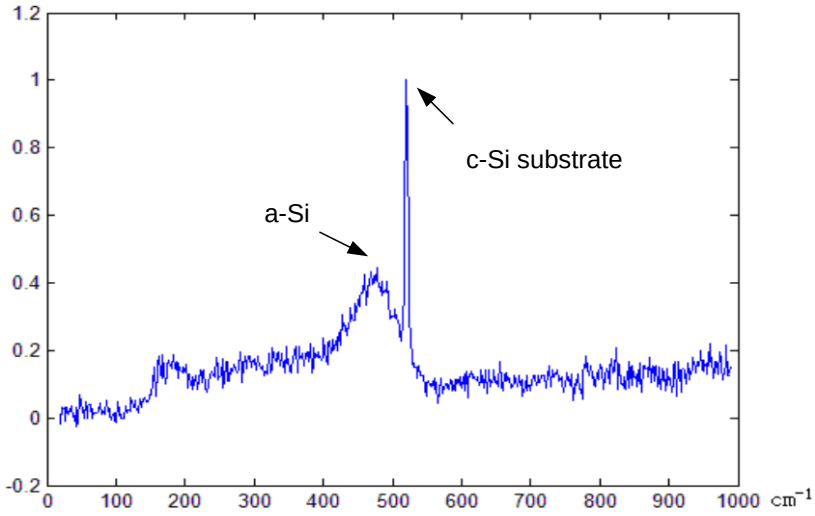


Figure 3.2 Raman spectroscopy of the a-Si film from spin-coated liquid-Si solution, after baking at 430 ℃ for 1 hour

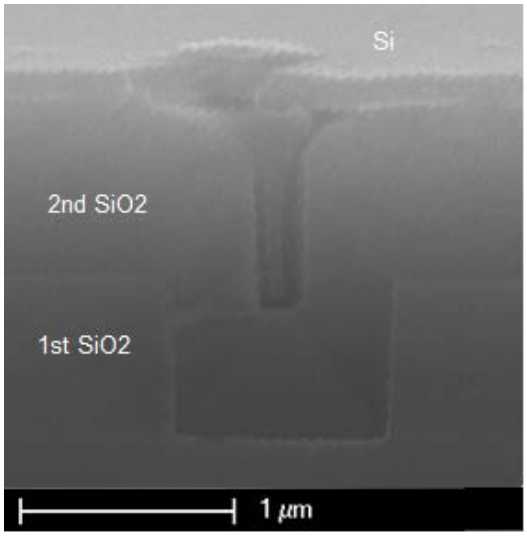


Figure 3.3 Cross-sectional SEM image of a-Si film, part of the film on the grain filter was damaged during sample cleaving

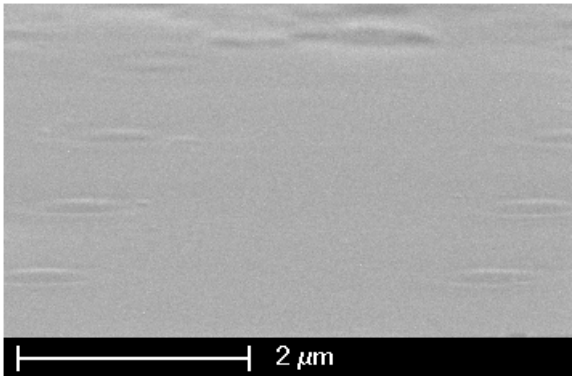


Figure 3.4 SEM image of a-Si film surface before crystallization.

Table 3.1 Hydrogen concentration and density of the film before and after annealing at 650 ºC, measured by TOF-SIMS. The value for 'LPCVD a-Si film' is measured on the a-Si film deposited by Low-Pressure Chemical Vapor Deposition (LPCVD) at 600 ºC

Sample	[H] (cm^{-3})	Density (g/cm^3)
a-Si with spin-coated liquid Si	6.7e21	1.96
a-Si with spin-coated liquid Si after pre-anneal	2-5e19	2.238
LPCVD a-Si film	4.1e19	2.29

Figure 3.5 shows the relationship of the crystalline grain size and the laser energy density under different conditions for various combinations of pulse duration and substrate temperature. In general, the grain size increased with the laser energy density, which is a trend commonly reported in the literature. [3] After obtaining the largest grains, we observed ablation at the center of the grain filters. If we continued to increase the energy density, the ablation area at the grain filter increased, and then the region outside the grain filter eventually started to be ablated.

Figure 3.5 shows that if the same pulse duration was used, a higher energy density was needed to obtain the same grain size when the substrate temperature was lower. The maximum grain size increased with the high substrate temperature, because a higher substrate temperature causes less heat loss of the melt-silicon to the substrate, thus increasing the solidification duration. Grains could grow until their boundaries impinge, instead of being terminated by 'super-cool' of the unsolidified Si layer. The effect is discussed in the publications [5] and [6].

Due to the same effect of the longer solidification duration, the maximum grain size was larger when a longer pulse was used. [7] The effect of the pulse duration on the maximum grain size is much more than that of the substrate temperature. The maximum grain size that could be obtained with the long laser pulse and the high substrate temperature was 3.5 μm, as shown in Figure 3.6 (a). The maximum grain size that we could obtain from the short-pulse (25 ns) laser and high substrate temperature is shown in Figure 3.6 (b).

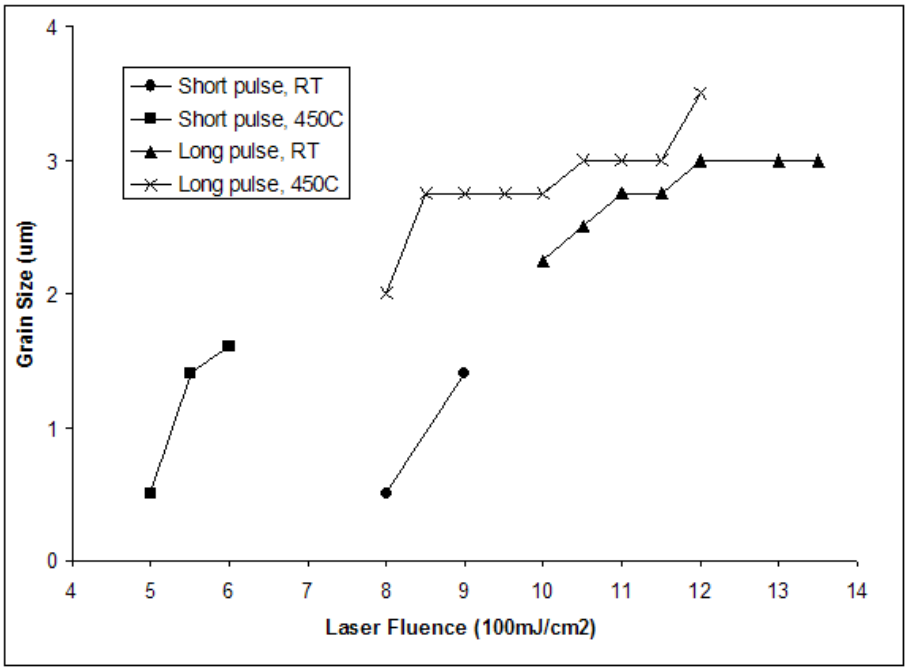
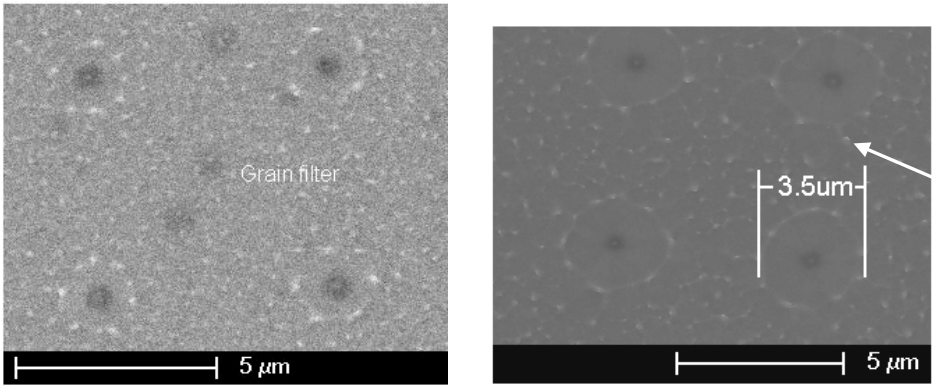


Figure 3.5 Grain size vs. laser energy density for various laser pulse width and substrate temperature.



(a) (b)

Figure 3.6 SEM image of silicon grains crystallized using the excimer laser at 450 °C, with pulse duration and maximum grain size of (a) 250 ns and 3.5 μm and (b) 25 ns and 1.6 μm. Dark spots correspond to the positions of the grain filters.

3.3 Single-Grain TFT

Single-grain Si TFTs were fabricated on top of the grains, which are crystallized withlong-duration pulses (250 ns) at the substrate temperature of 450 ºC, and having a grain size of 3.5 μm. The TFTs are manufactured using the standard TFT process that we have discussed in Chapter 2. In this particular fabrication flow, the gate oxide thickness is 41 nm, consisting of 13 nm thick SiO_2 by ICP oxidation and an additional 28 nm thick SiO_2 by PECVD TEOS. The rest of the process is the same as introduced in Chapter 2.

The maximum temperature in the process steps, 650 ºC, was for the dehydrogenation. Figure 3.7 is an optical microscopic image of the fabricated SG TFTs. The width and the length of the channel are both 1 μm.

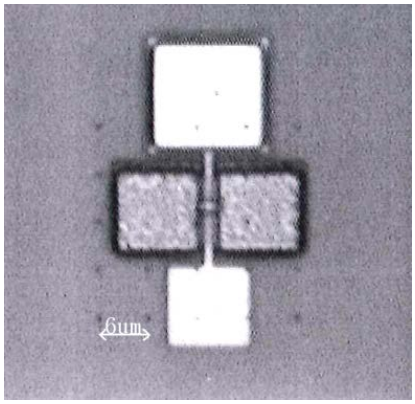
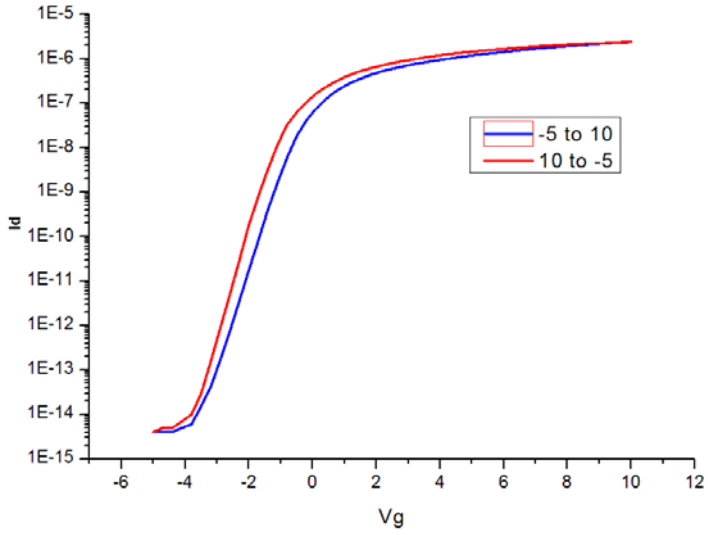
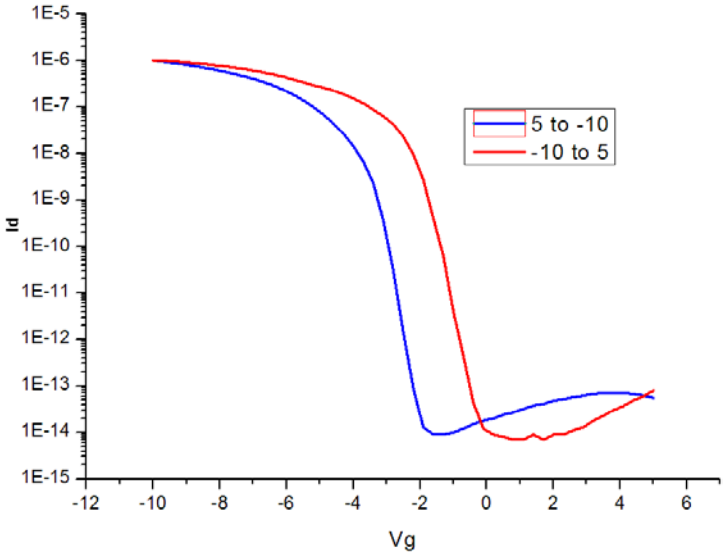


Figure 3.7 Optical microscopic image of fabricated SG-TFTs. The channel size is 1 μm by 1 μm.

Figure 3.8 shows the transfer characteristics of NMOS and PMOS SG-TFTs on the location-controlled Si grain. Since there are no grain boundaries in the channel region, the leakage current is low. The field effect mobilities, which were estimated in the linear region at a low drain voltage, are 423 cm^2/Vs for electrons and 118 cm^2/Vs for holes. The carrier mobility was greatly increased compared to that of the poly-Si TFTs because the location-controlled silicon grain realized the channel region inside one single grain. The mobilities are slightly increased from the value in our publication (391 cm^2/Vs for electrons and 111 cm^2/Vs for holes) on the single-grain Si TFTs with short-pulse-laser crystallization, because of the longer laser pulse. [8] But the carrier mobility is lower than the single grain TFTs fabricated from LPCVD-Si [9], because a thinner Si layer is used in this approach, resulting in higher series resistance. Figure 3.9 shows the output characteristics of NMOS and PMOS transistors. While PMOS readily shows an increase of the drain current I_D from the origin, NMOS shows slightly non-linear behavior, indicating high series parasitic resistance. The parasitic resistance may be caused by high resistance in the S/D region due to the small thickness of the silicon layer. Figure 3.10 shows the mobilities of electrons and holes as a function of the laser energy densities (fluencies). Optimum mobilities for electrons and holes were obtained at 1000 mJ/cm^2 and 1050 mJ/cm^2, respectively. Mobility decrease at higher energy densities is presumably caused by surface roughness.

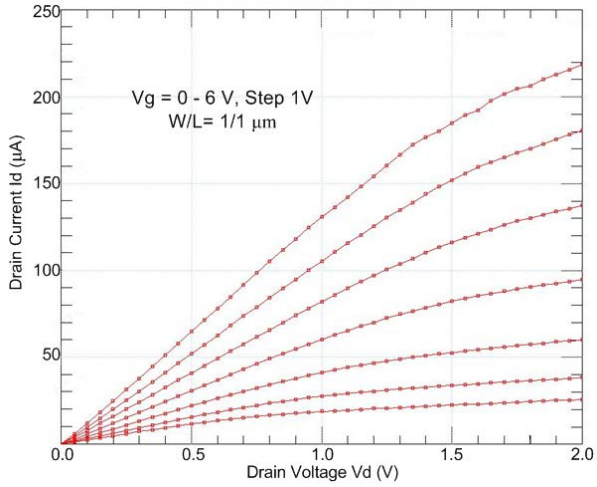


(a)

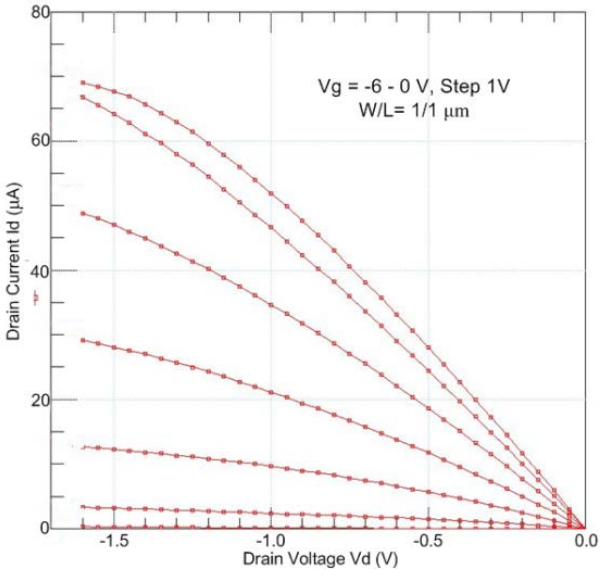


(b)

Figure 3.8 Transfer characteristic for (a) NMOS single-grain TFTs and (b) PMOS single-grain TFTs.



(a)



(b)

Figure 3.9 Output characteristics for (a) NMOS single-grain TFTs and (b) PMOS single-grain TFTs.

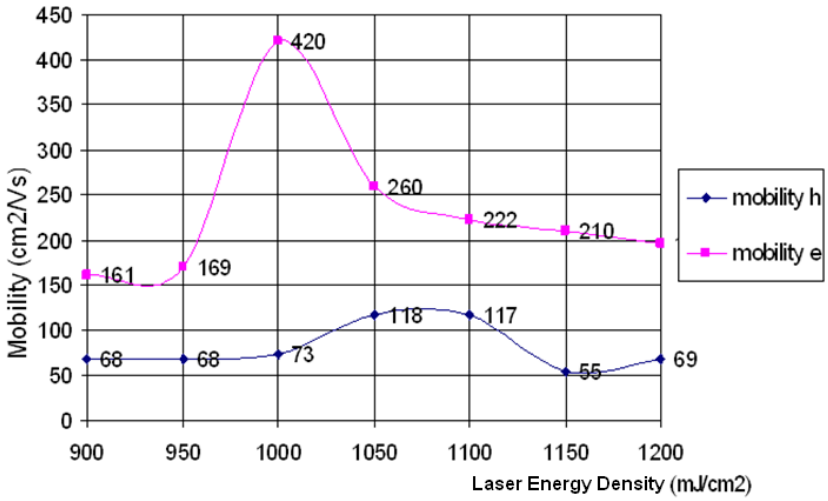


Figure 3.10 Field-effect mobilities as a function of crystallization laser energy density.

3.4 Conclusion

For the purpose of printing electronic devices and circuits, we studied the fabrication process of single-grain TFTs from spin-coated liquid-Si solution. In this chapter we showed the investigation of the excimer laser crystallization of the a-Si film from the liquid-Si precursor, using the μ-Czochralski process to make Si single grains. The maximum grain size is 3.5 μm. Single-grain Si TFTs have been fabricated with a process with a maximum temperature of 650 °C for dehydrogenation. The field-effect mobility is 423 cm^2/Vs and 118 cm^2/Vs for electrons and holes, respectively. Although the process temperature is too high (> 350 °C) for the flexible plastic substrates, the high performance of the devices in this work shows the potential for fabricating single-grain Si TFTs using the solution process.

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Chapter 4

Single-Grain Si TFTs on Flexible Polyimide Substrate Fabricated from Doctor-Blade Coated Liquid-Si

Solution processed silicon technology, which has been discussed in Chapter 3, provides high-performance single-grain TFT fabrication from spin-coated liquid-Si solution, but unfortunately the process temperature is too high for flexible plastic substrates. In this chapter an improved fabrication process at low temperature (<350 °C) is reported for the fabrication of single-grain Si TFTs on a polyimide substrate from doctor-blade coated liquid-Si. With this method different types of semiconductor devices have been fabricated, including TFTs showing a carrier mobility of 460 cm^2/Vs and 121 cm^2/Vs, for electrons and holes, respectively, and CMOS inverters with full output swing. In Section 4.1, the need for a low-temperature process for high-quality Si devices is introduced. Section 4.2 explains the process technology to realize a low temperature process for a-Si film from liquid Si solution, and Section 4.3 presents the fabrication process and the characteristics of the single-grain Si TFTs and inverters. Section 4.4 concludes the chapter.

CHAPTER 4 SINGLE-GRAIN SI TFTS ON FLEXIBLE POLYIMIDE SUBSTRATE FABRICATED FROM DOCTOR-BLADE COATED LIQUID-SI

4.1 Introduction

'Low temperature' and 'high performance' are the most desired properties in printed flexible electronics research. Low temperature is needed because of the thermal budget limit of the flexible substrates, which are usually plastic. In the frame of low temperatures, various species of semiconductor transistors are studied, for example, organic TFT, metal oxide TFTs and a-Si and poly-Si TFTs, all of which have been introduced in Chapter 1. But it seems that in the pursuit of the low process temperature, we lose the transistor performance, in terms of carrier mobility and reliability. In our earlier attempt, as shown in Chapter 3, we presented the fabrication process for single-grain Si TFTs from the liquid-Si solution, with a performance superior to that of organic, metal oxide, a-Si and poly-Si TFTs. This research shows a potential for high-performance TFTs. However, the baking temperature for liquid-Si solution to form a-Si (430 °C), the dehydrogenation temperature for a-Si film (650 °C), the substrate temperature for laser crystallization (450 °C) and the Al-Si alloying temperature (400 °C) are much too high for the polymer substrates (< 350 °C).
From the literature we know that a lower baking temperature to form a-Si results in higher hydrogen concentration in the a-Si film [1], but the extra hydrogen could be removed by a dehydrogenation step. The dehydrogenation can be done by a laser at room temperature instead of in a furnace, which was discussed in Chapter 2. The laser crystallization can also be done at room temperature, according to Chapter 3, bringing slightly smaller grain sizes than those at 450 °C, but still enough to cover the active region. The Al-Si alloying (400 °C) improves the device property. It reduces the contact resistance at the source and drain regions by forming Al silicide, and recovers the carrier mobility by passivating the Si dangling bonds at the Si-SiO_2 interface. [2] But neither the contact resistance nor the Si dangling bonds causes the devices to fail. Thus this step is skipped.

In this chapter we report on the fabrication of the world's first single-grain Si TFTs on a polyimide-coated substrate with a maximum process temperature of 350 °C from the liquid-Si solution, which is deposited by doctor-blade coating, a process compatible with the roll-to-roll process. The carrier mobility is 460 cm^2/Vs and 121 cm^2/Vs, for electrons and holes, respectively. CMOS inverters are fabricated and the characteristics are presented as well.

4.2 Formation, Dehydrogenation and Crystallization of Liquid-Si Film

The process flow of single-grain Si TFTs fabrication on a polyimide substrate is shown in Figure 4.1. First, a quasi-plastic substrate of a 10-µm-thick polyimide layer and a 4-µm-thick capping SiO_2 is prepared on top of a supporting crystalline Si wafer. Then the grain filters are made on the oxide surface. 100 % CPS (without solvents), as the liquid-Si solution, is coated using a Si_3N_4 doctor blade, or a polyimide blade, in a low oxygen-level environment (<10 ppm). After that, the liquid-Si precursor was transformed into a-Si film using UV polymerization and a baking temperature of 350 °C. This temperature is lower than the 430 °C reported in Chapter 3 and in previous studies. [3] Raman spectroscopy of the film shows a broad peak at around 480 cm^{-1}, which indicates that the film was converted into a-Si (Figure 4.4). Hydrogen concentration in the layer is measured to be 13 at% by Elastic Recoil Detection (ERD) (Figure 2.5 in Chapter 2). The cross-sectional Scan Electron Microscopy (SEM) image of a grain filter shows that it is completely filled with a-Si (Figure 4.2). Figure 4.3 is the cross-sectional Focused Ion Beam Transmission Electron Microscopy (FIB-TEM) image of the film from the diluted liquid-Si solution described in Chapter 3. Comparing Figure 4.2 and 4.3, it is found that the absence of the solvent in the case of 100 % CPS (Figure 4.2) results in a smaller gap between the wall of the grain filter and the Si inside the grain filter, due to the absence of solvent evaporation.

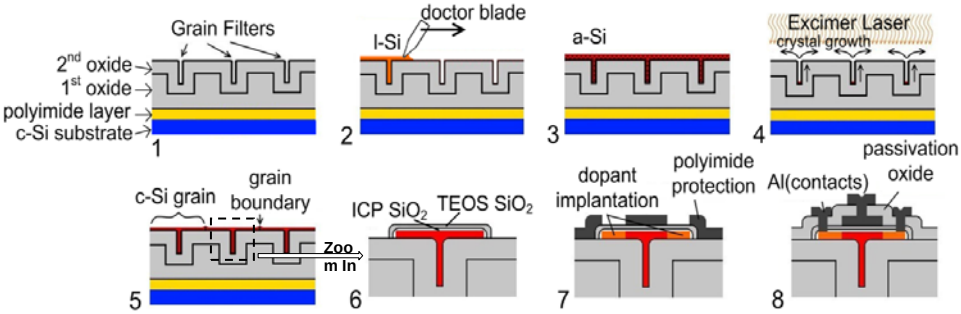


Figure 4.1 Schematic of SG-TFT fabrication process with liquid-Si on polyimide substrate

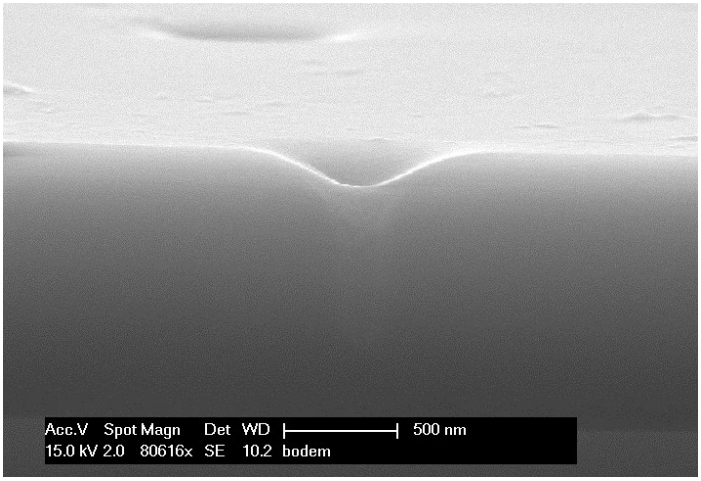


Figure 4.2 Cross-sectional Scan Electron Microscopy (SEM) image of a grain filter, completely filled with a-Si, from docter-blade coated liquid-Si solution (pure CPS), and annealed at 350 °C

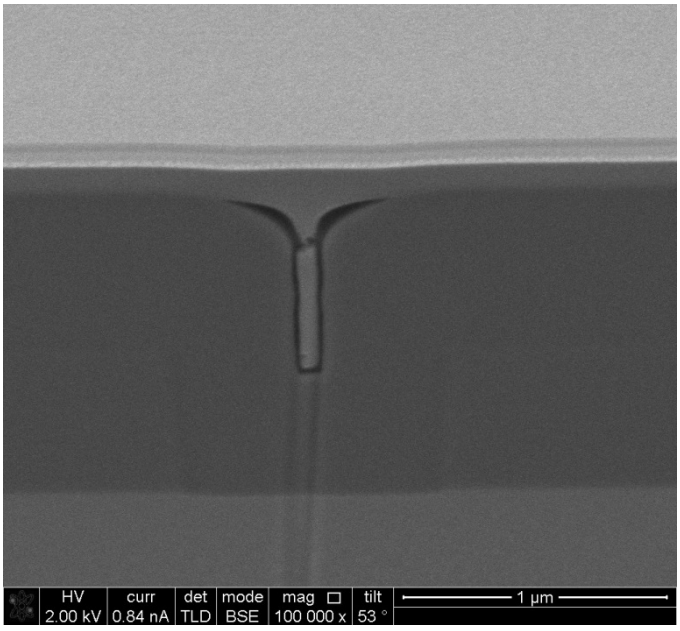


Figure 4.3 Cross-sectional TEM image of a grain filter with an a-Si seed in it after FIB etching. Gaps could be seen between the wall of the grain filter and the Si seed.

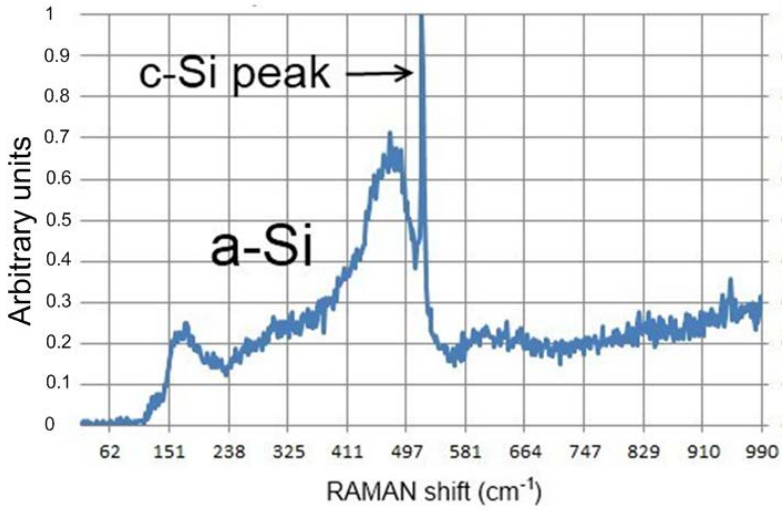


Figure 4.4 Raman spectroscopy of the a-Si film formed with liquid-Si at 350 °C. The c-Si peak is a signal of the substrate.

Filling the grain filters

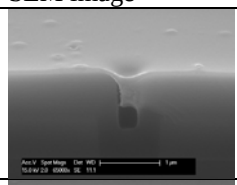
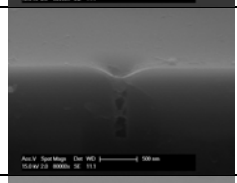
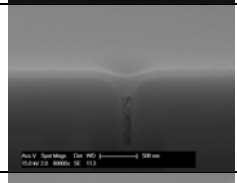
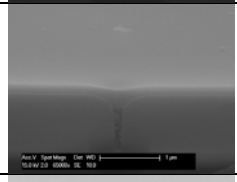
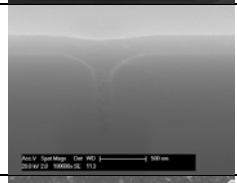
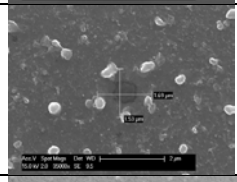
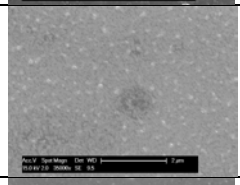
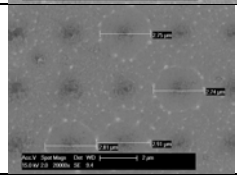
Although the CPS monomer liquid is stored in a stainless steel bottle inside the glove box, the 100 % CPS ages due to its suspected instability and polymerization. The liquid changes its viscosity and the adhesion to substrates, the oxygen and water vapor residues in the glove box, and the heating cycle during hot plate baking in the experiments accelerate the aging. The 'lucky' result of the completely filled grain filters in Figure 4.2 may not be repeatable with the less-aged or more-aged CPS liquid. To widen the process window of the 'glove box storage aged' CPS monomers, the substrate surface treatment is researched for the filling of the grain filters. The results are listed in Figure 4.1.With the surface treatment of HF dip or O_2 plasma before coating, the grain filters were not always filled, whether the ramping slope to 350 ºC is fast or slow, or the coating blade is made of SiN or polyimide. The grains cannot be formed with the laser of 25 ns pulse duration, since the trapped gas expends and breaks the Si film under the laser beam before the energy is high enough for the grains. However, when we dehydrogenate and crystallize (as described in Sections 2.2 and 2.3) the film with a XeCl excimer laser (308 nm) with pulse duration of 200 ns (cooperation of IAI Industrial Systems B.V.), 1.7 μm grains could be made. It is probably because the multiple laser shots to slowly dehydrogenate the film melt the film layer by layer and the trapped nitrogen in the non-filled grain filters could come out gently, leaving an air-free film for

crystallization. A longer pulse laser is needed for easier dehydrogenation and crystallization for longer melt duration.

Another surface treatment is to leave the wafer in the CPS vapor for 1 minute for an ultra-thin layer deposition. With the CPS vapor treatment and the spin-coating method, a more uniform layer could be coated. Even with the 25 ns pulse duration laser, almost 3 μm grain could be made on the film. The combination of the CPS vapor surface treatment and the long pulse duration laser may be the best choice to fabricate the single Si grains from liquid-Si.

For dehydrogenation and crystallization of the a-Si film, a XeCl excimer laser (308nm, 250ns) is employed. To avoid the high dehydrogenation temperature in the furnace (650 °C), which was discussed in Chapter 3, the sample was dehydrogenated at room temperature by laser annealing with multiple shots at lower energies. The a-Si layer is melted layer by layer, to prevent an abrupt hydrogen explosion and at the same time forcing the hydrogen to diffuse out. The laser dehydrogenation recipe is shown in Figure 2.5(a). After laser annealing up to 500mJ/cm^2, the peak hydrogen concentration decreased from 13 at% to 10 at%, while at the surface the concentration decreased to 3 at%, as shown in Figure 2.5(b) in Chapter 2. After the dehydrogenation, the a-Si film was crystallized by the excimer laser at room temperature with an energy density of 950 mJ/cm^2. Si grains were created on predetermined positions of the grain filters with a maximum grain size of 3 μm, as can be seen in Figure 4.5.

Table 4.1 List of results of the grain-filter filling research

	Description	SEM image	Comments
Surface treatment	4 min HF dip		Grain filter too large and not filled
	0.5 min HF dip		Grain filter not filled
	1 min O_2 plasma		Similar to 0.5 min dip, could use either of them
Change ramping slope to 350 ºC	Ramping to 350 ºC in a half hour		Grain filter not filled, could use fast ramping for time efficiency
Change blade	SiN blade		Grain filter not filled
Crystallize	200 ns pulse duration		1.7 µm grain
	25 ns pulse duration		No grain
Spin-coat+CPS vapor+25 ns crystallization			Almost 3 µm grain

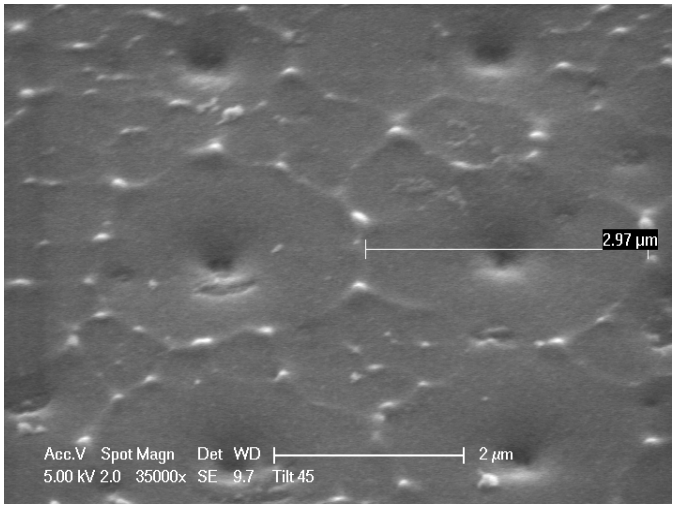
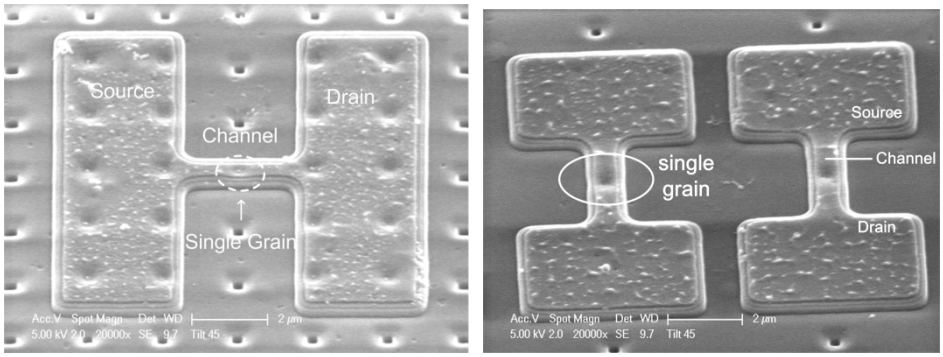


Figure 4.5 SEM image of the crystallized grains at predetermined positions with a maximum diameter of 3 µm.

4.3 Single-Grain Si TFTs

TFTs are fabricated inside the grain with a process as described in Chapter 2. The SEM image of the silicon islands shows the channel covered by a single grain, as shown in Figure 4.6. In this process the gate SiO_2 thickness is 40 nm, including 12-nm-thick SiO_2 by ICP oxidation at 250 °C and an additional 28-nm-thick SiO_2 deposited by PECVD-TEOS at 350 °C. To prevent damage to the polyimide substrate from the laser in the laser activation step for the dopants of the source and drain region, an Al mask is used to cover the area outside the gate, source and drain. The channel length and width are both 1 µm.



(a) (b)

Figure 4.6 SEM images of patterned silicon islands. Single grains covering the channel region are visible.

After the fabrication of the devices, they are transferred from the c-Si substrate to a 125-µm-thick PEN foil in the way that was illustrated in the 'Single-Polyimide Process' in Chapter 2.5. Figure 4.7 shows a photo of the transparent and flexible devices after the substrate transfer process. The substrate transfer process is not necessary, since the TFTs could be directly fabricated on the polyimide foil as the maximum process temperature is 350 °C. We have applied the substrate transfer process simply because of the ease of handling and processing in our lab if the c-Si wafer was employed as a carrier.

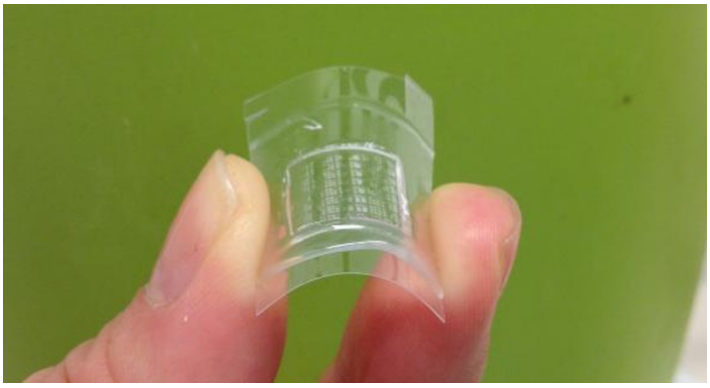


Figure 4.7 Image of SG-TFTs on polyimide layer (1x1cm2) peeled off and transferred to a PEN foil.

The curves indicated as 'Before peeled off' in Figure 4.8 and Figure 4.9, and the curve in Figure 4.10 show the transfer and output characteristics of the NMOS and PMOS TFTs just after the device fabrication and before the substrate transfer process. The carrier mobility estimated in the linear region with a low drain voltage is 460 cm^2/Vs and 121 cm^2/Vs for electrons and holes, respectively. Table 4.2 summarizes the device characteristic values. The mobilities are much higher than those of the organic (0.5 cm^2/Vs, [4]) and metal oxide (~10 cm^2/Vs, [5]) TFTs on a plastic substrate. The values are higher than poly-Si TFTs (50 cm^2/Vs, [6]), as well, because of the absence of the random grain-boundaries inside the channel. The leakage current is below 0.1 pA/μm, which is lower than that of the poly-Si TFTs and suitable for display application. [7] The curve labeled as 'Before peeled off' in Figure 4.12 shows the output characteristic of the CMOS inverter, with a full output swing (4.997 V out of 5.000 V) and with V_{TH} of 2.14 V. Table 4.3 presents the summary of the inverter characteristics.

The curves referred to as 'After transfer' in Figure 4.8 and Figure 4.9 represent the cases after the devices are transferred to a PEN foil using the 'Single-Polyimide Process', as shown in the photo in Figure 4.7. After the substrate transfer process, the circuit still shows functioning transfer characteristics of NMOS and PMOS TFTs. The NMOS TFTs before and after being peeled off are measured on the same transistor, which also applies for PMOS TFTs and inverters. The estimated carrier mobility is 310 cm^2/Vs and 110 cm^2/Vs for electrons and holes, respectively, which is lower than the carrier mobility value before the devices were transferred. The leakage current of NMOS transistors at high negative gate voltage decreases compared to that of 'before peeled off'. The reason for the reduced carrier mobility is assumed to be the mechanical stress caused by the transfer process and/or stress during the measurement since the substrate is not rigid. The leakage current at gate voltage of V_g= -5 V becomes lower than 1 pA/μm. Figure 4.11 shows the output characteristics of a PMOS and a NMOS TFT before peeling off and after the transfer. The change of the transistor characteristics is summarized in Table 4.2. Fig. 4.12 shows the output curve of the CMOS inverter on the flexible foil, with a threshold voltage V_{TH} of 1.50 V, a full output swing (4.981 V out of 5.000 V), and a less-balanced noise margin compared to before being peeled off, since the threshold voltage of both NMOS and PMOS TFTs shifted to more negative values. The summary of the inverter behavior is listed in Table 4.3.

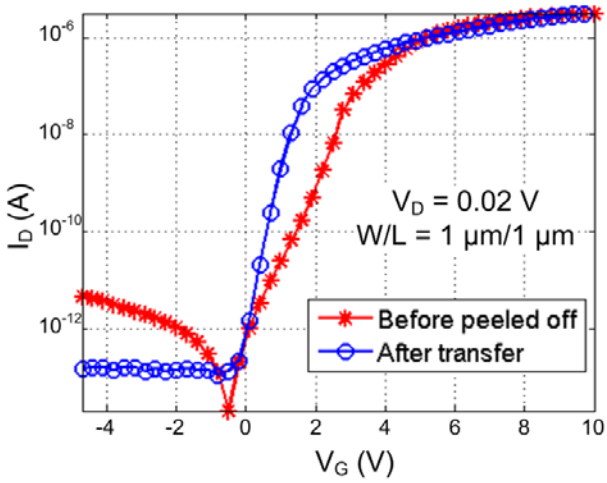


Figure 4.8 Transfer characteristics of NMOS TFTs before the peeling-off and after the transfer.

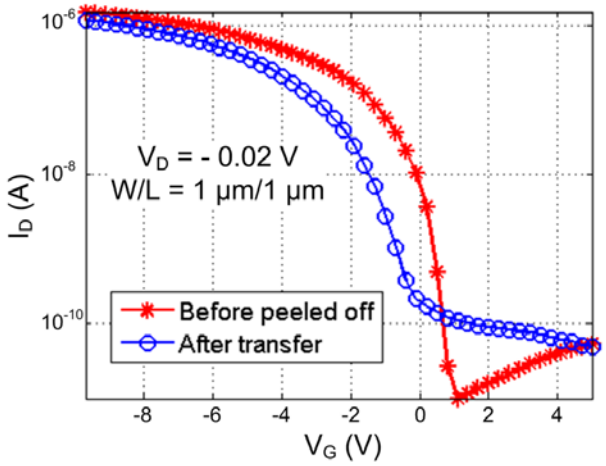


Figure 4.9 Transfer characteristics of PMOS TFTs before the peeling-off and after the transfer.

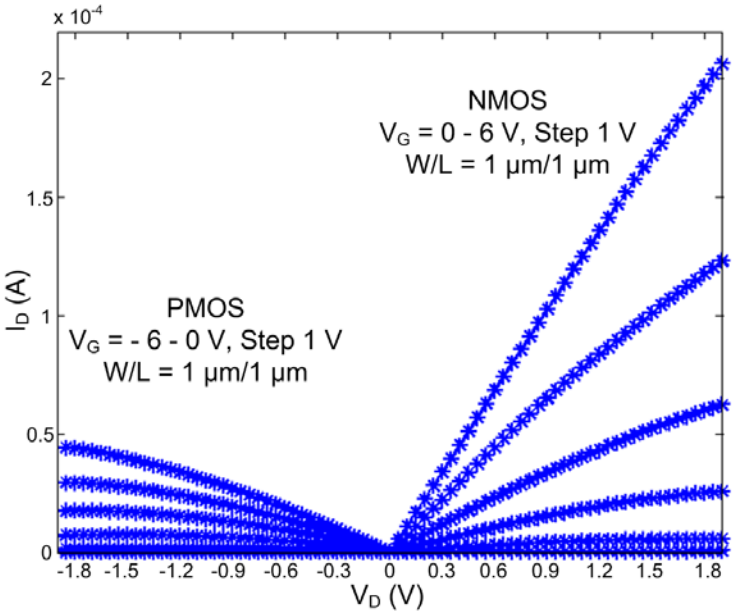
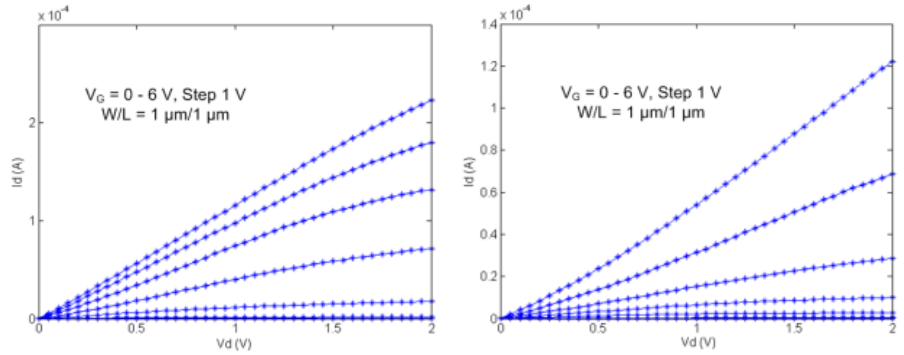
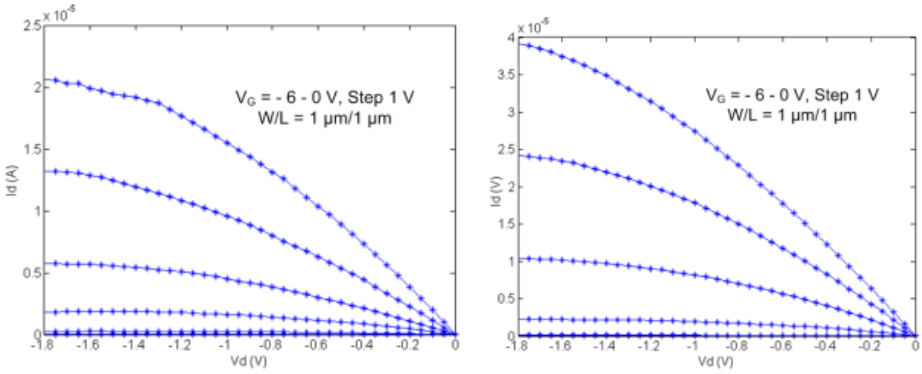


Figure 4.10 Output characteristics of NMOS (a) and PMOS (b) TFTs before the peeling-off.



(a)



(b)

Figure 4.11 Output characteristics of NMOS TFT before the peeling-off (a, left), NMOS TFT after the peeling-off (a, right), PMOS TFT before the peeling-off (b, left) and PMOS TFT after the peeling-off (b, right).

Table 4.2 Summary of NMOS TFT and PMOS TFT characteristics

TFT	NMOS	NMOS after peeling	PMOS	PMOS after peeling
µFE (cm^2/Vs)	460	310	121	110
VTH (V)	3.62	2.55	-0.94	-2.02
ION /IOFF	$7x10^5$	$2x10^7$	$3x10^4$	$2.5x10^4$
S (V/dec)	0.3	0.26	0.24	0.67

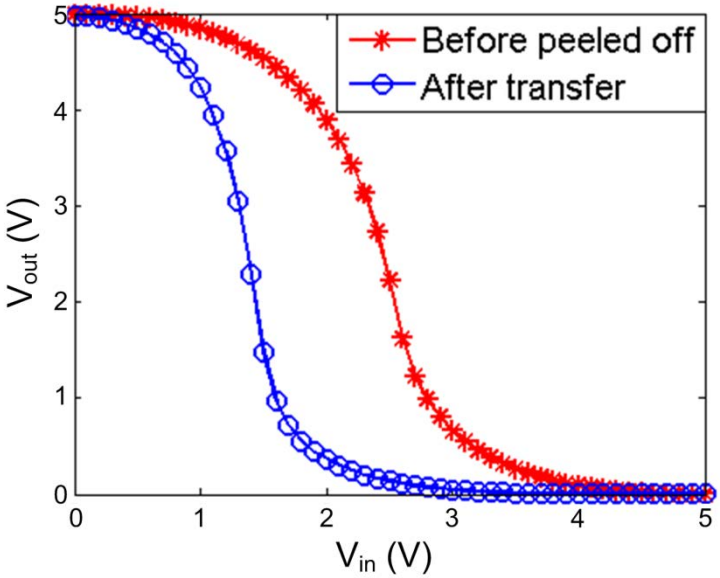


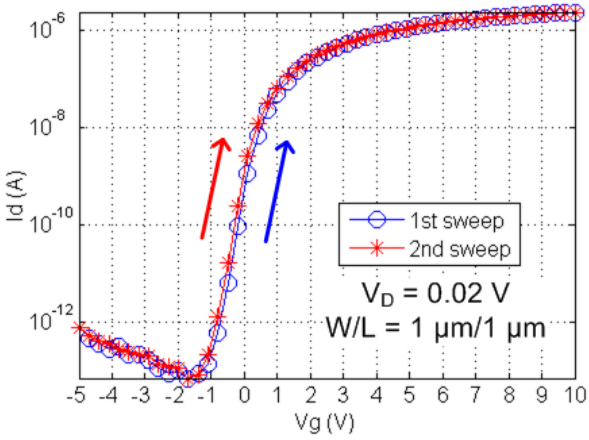
Figure 4.12 Output characteristic of the CMOS inverter with the ratio of 2 of W/L between PMOS and NMOS TFTs (red) before being peeled off and (blue) after transfer.

Table 4.3 Summary of the CMOS inverter characteristics

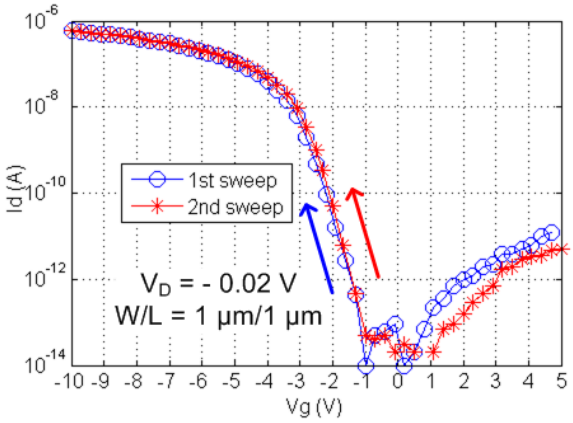
Inverter	Before Peeling	After peeling
V_{TH} (V)	2.14	1.50
V_{OH} (V)	4.9972	4.9805
V_{OL} (V)	0.0096	0.0006
NM_H (V)	2.3275	3.04
NM_L (V)	1.3968	0.76

The stability of the transfer characteristics was tested, and the result is shown in Figure 4.13 and Figure 4.14. The transistors were measured with a gate voltage V_G sweeping from the value for the off-state to the on-state of the transistors, one time immediately after another, resulting in a negligible difference in the transfer characteristics, indicating that no charges were induced in the gate oxide during the measurement. The invertors with the input

voltage V_{in} sweeping from 0 V to 5 V were measured immediately one after another, and there is no change in the output curve.



(a)



(b)

Figure 4.13 Stability of the transfer characteristics of (a) a NMOS TFT and (b) a PMOS TFT.

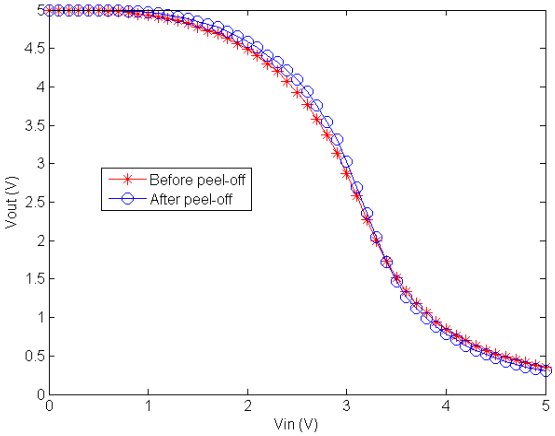


Figure 4.14 Output characteristic of CMOS invertor with the ratio of W/L between PMOS and NMOS TFTs of 2.

4.4 Conclusion

In this chapter the fabrication technique of the single-grain Si TFTs with a low process temperature is presented. Amorphous Si was formed by doctor-blade coating and the annealing of liquid-Si on a polyimide-coated substrate. With subsequent crystallization by an excimer laser, grains with a maximum diameter of 3 μm were obtained. Single-grain Si TFTs fabricated inside the grain showed mobilities of 460 cm2/Vs and 121 cm2/Vs for electrons and holes, respectively. CMOS inverters were also fabricated and showed full output swing. These results suggest that the approach presented in this paper can open a new route for achieving high-performance and flexible Si thin-film electronic devices on plastic with a printing method compatible with roll-to-roll processes.

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CHAPTER 4 SINGLE-GRAIN SI TFTS ON FLEXIBLE POLYIMIDE SUBSTRATE FABRICATED FROM DOCTOR-BLADE COATED LIQUID-SI

Chapter 5

Reliability of the Flexible Single-Grain Si TFTs

In chapter 3 and 4, we have shown the high carrier mobility of the single-grain Si TFTs fabricated from the liquid-Si solution. As the other aspect of 'high performance', the reliability has also been investigated, including the electrical reliability of NMOS and PMOS TFTs and the mechanical reliability of the flexible devices when they are transferred to PEN foil. In this chapter, the reliability of the single-grain Si TFTs is presented. Section 5.1 is a general introduction to the reliability of TFTs. The study of the electrical reliability under gate and drain stress is described in Section 5.2. In Section 5.3, the mechanical reliability and the carrier mobility degradation under bending are listed and analyzed. In Section 5.4, an improved detaching method for restraining the mobility degradation is proposed. Lastly, the chapter is summarized in Section 5.5.

CHAPTER 5 RELIABILITY OF THE FLEXIBLE SINGLE-GRAIN SI TFTS

5.1 Introduction

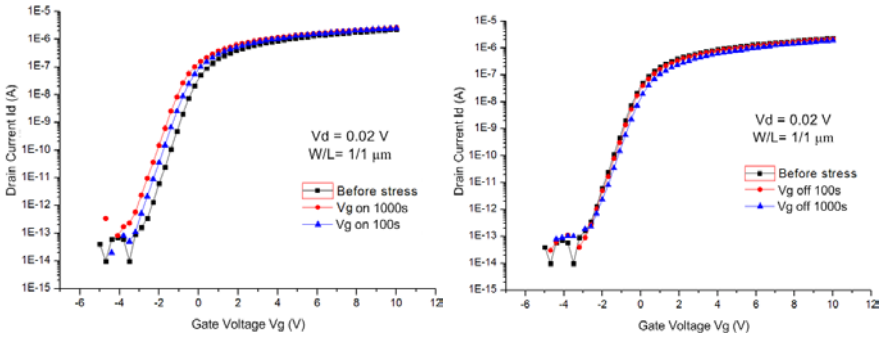
The long-term electrical stability and reliability of TFTs affect power consumption, correct circuit function and the life time of the device, the circuit and the product. TFTs with different channel materials suffer from different reliability issues. The most common sign suggesting circuit degradation is the threshold voltage shift. [1] Usually, organic semiconductor TFTs show shift in threshold voltage when exposed to moisture and oxygen, and are regarded as unreliable. [1][2] Metal oxide TFTs have the issue of threshold voltage shifting with negative bias stress and light exposure, due to the trap generation and the electron injection from the channel to the dielectric layer. [3][4][5][6] The long-term threshold voltage change in a-Si TFTs and poly-Si TFTs are caused by the breaking of the Si-H bonds in the grain boundaries in the channel region and the trap density increase due to the dangling bonds. [7][8][9][10] In terms of mechanical reliability, we usually refer to the degree of flexibility of the circuit. The bending diameter is defined as the lowest diameter one can bend a device while it is still functioning. The smaller the bending diameter, the more flexible the circuit. As we showed in Chapter 1, flexible circuits have been fabricated with all types of the TFTs mentioned above. An extreme example is given by the University of Tokyo of super-flexible organic TFTs with bending diameters of 10 μm. [11] However, by other research groups, a bending diameter down to 10 mm is commonly reported. [12][13]

In this chapter, we would like to demonstrate the electrical and mechanical reliability of the single-grain Si TFTs fabricated from the liquid-Si solution. NMOS TFTs show stable behavior under gate and drain stress, but PMOS TFTs show threshold voltage shift. The devices could be bent up to 6 mm diameter with the transistors still functioning. An improved substrate transfer method is introduced as the 'Double-Polyimide Process', which could lower the bending stress and allow the functioning of devices with bending diameter of 3 mm.

5.2 Electrical Reliability

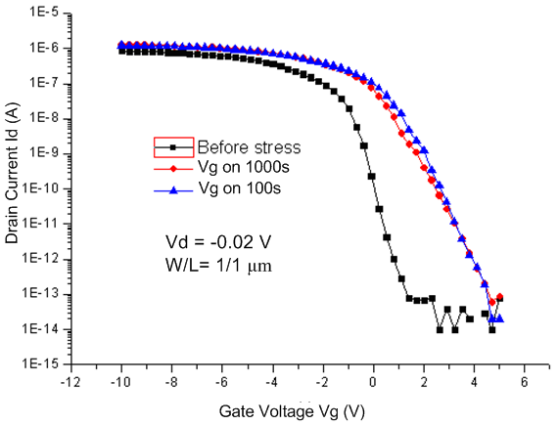
The electrical reliability of the single-grain Si TFTs is investigated on devices from spin-coated liquid-Si, which are shown in Chapter 3, including the transistor characteristics after gate and drain bias stresses, and the hysteresis behavior. Figure 5.1 and Figure 5.2 show the change of the transfer characteristics after on-state and off-state gate stress for NMOS and PMOS TFTs. After up to 1000 s of on-state and off-state gate stresses, NMOS TFTs show stable behavior. However, for PMOS TFTs, positive and negative threshold-voltage shifts were observed for on-state and off-state gate stress, respectively. We suspect that for the on-state gate stress of the PMOS TFTs,

mobile protons are generated in the gate oxide, and the negative gate voltage induced electrical field causes migration/drifting of the protons from the Si/SiO_2 interface to the metal/SiO_2 interface, as shown in Figure 5.3. [14][15][16] More holes were induced at the Si/SiO_2 interface due to the charge neutrality, causing an increase in the drain current. The source of the protons could be trapped hydrogen atoms in the SiO_2 during the annealing/alloying in the forming gas atmosphere, [14] and the mechanism of the proton motion is by hopping. [17] For the case of off-state gate-voltage stress the mechanism is the same, but the opposite characteristic was observed. The hysteresis behavior of the PMOS TFTs could be observed in the transfer characteristics in Figure 3.9 (b) in Chapter 3 and in Table 5.1, whereby the hysteresis is caused by the same reason. After the gate stress is removed, the recovery of the characteristics is shown in Figure 5.4. This is due to the fact that the induced protons would slowly diffuse back to their original location, and the drain current would slowly recover its original value.

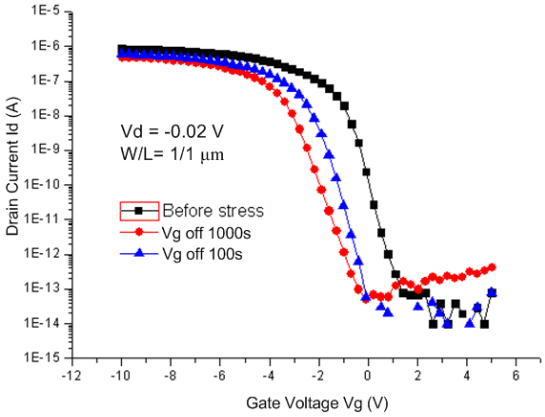


(a) (b)

Figure 5.1 Transfer characteristics of NMOS SG Si TFTs after 100 s and 1000 s (a) on-state gate stress of 6 V and (b) off-state gate stress of -6 V and a drain voltage of 0.02 V.



(a)



(b)

Figure 5.2 Transfer characteristics of PMOS SG Si TFTs after 100 s and 1000 s (a) on-state gate stress of -6 V and (b) off-state gate stress of 6 V and a drain voltage of -0.02 V.

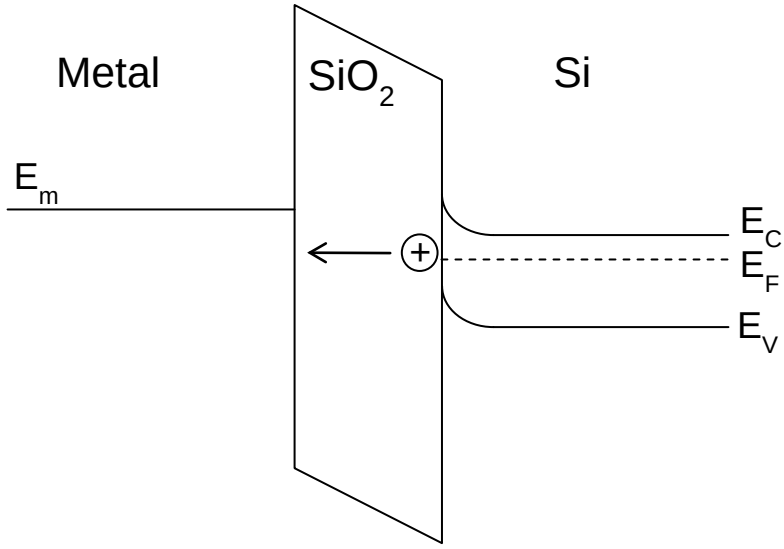
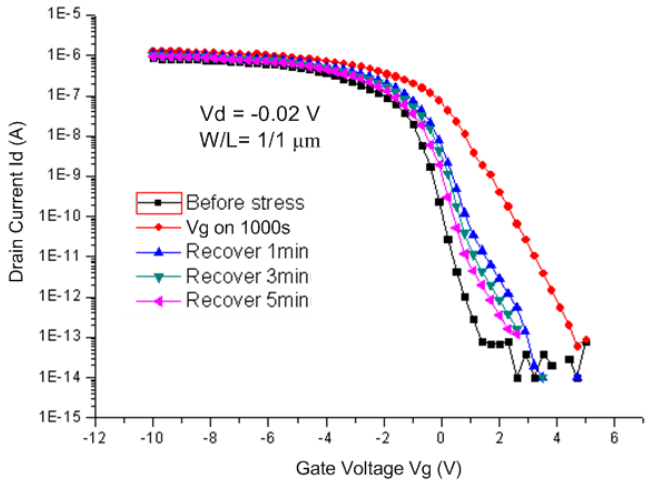


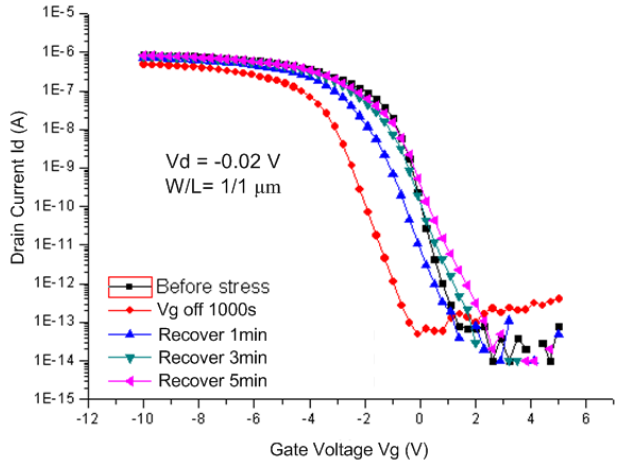
Figure 5.3 Illustration of the influence of the drifting of mobile protons.

Table 5.1 Summary of the hysteresis behavior of SG TFTs

NMOS			PMOS		
Voltage	V_{th} (V)	S (mV/dev)	Voltage	V_{th} (V)	S (mV/dec)
Up -5 to 10 V	-1.1	433	Up 5 to -10 V	-3.25	224
Down 10 to -5 V	-1.4	377	Down -10 to 5 V	-1.75	250



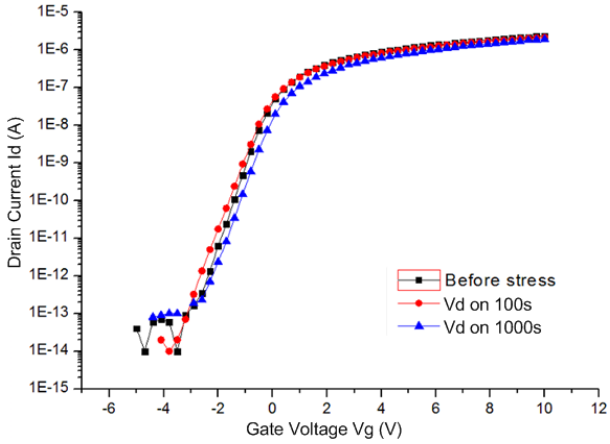
(a)



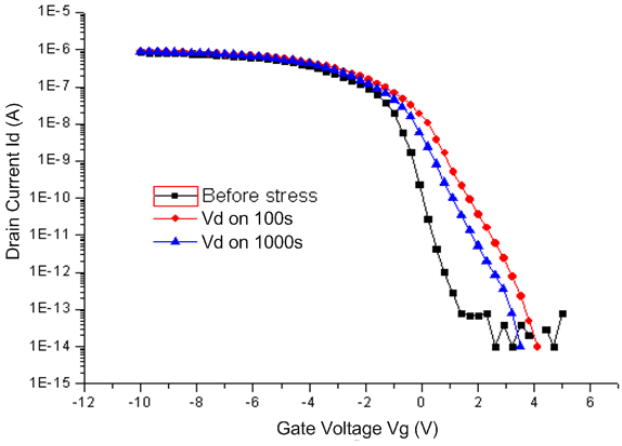
(b)

Figure 5.4 Transfer characteristics of PMOS transistors measured at 1 min, 3 mins, and 5 mins after the 1000 s of (a) on-state gate-voltage stress and (b) off-state gate-voltage stress. Clear recovery has been observed for the both cases.

The change of transfer characteristics of NMOS and PMOS TFTs under drain bias (2 V and –2 V for NMOS and PMOS TFTs, respectively) for the stressing time of up to 1000 s is shown in Figure 5.5. Only PMOS TFTs show the threshold voltage (V_{th}) shift. This is caused by the proton diffusion in the gate oxide near the drain edge where the electric field is generated from the gate to the drain.



(a)



(b)

Figure 5.5 Transfer characteristics of (a) NMOS and (b) PMOS TFTs after 100 s and 1000 s drain bias stress. The stress drain voltages are 2 and -2 V for NMOS and PMOS TFTs, respectively.

5.3 Mechanical Reliability: Device Degradation under Bending

The single-grain Si TFTs fabricated from the doctor-blade coated liquid-Si with a maximum process temperature of 350 °C are transferred onto a PEN foil, using the Single-Polyimide Process, as discussed in Chapter 4. After the transfer, the operation of the transparent and flexible devices under bending is studied.

Figure 5.6 shows a photo of the setup of the bending tests for the flexible devices. Rollable cylinders with different diameters were designed and made in steel to provide a rigid and solid surface. Devices could be fixed on the cylinder to be bent at different bending diameters. The smooth rolling of the cylinder on the supporting frame makes it possible to test the devices with bending-releasing cycles.

(a) (b)

Figure 5.6 (a) The measurement instrument for bending cycles, with (b) the cylinders with bending diameters down to 3 mm.

As shown in Figure 5.7, the flexible devices we discussed in Chapter 4 are bent with a bending diameter as low as 6 mm. The devices are functioning with a bending diameter of 6 mm, but the carrier mobility decreased with the bending. Figure 5.8 shows the normalized field-effect mobility of a NMOS and a PMOS TFT. There is a clear difference in the trend of mobility degradation between electrons and holes. As we know, the shape of the bottom of the conduction band and the top of the valence band are different, and as a result, the distribution in the heavy and light carrier effective mass is different between electrons and holes. Under the strain, the shape of the conduction band and the valence band are both changed, but in dissimilar ways. Thus, among electrons and holes, the effective mass variation and the carrier repopulation are not the same, which are the two main reasons for the carrier mobility degradation under

bending. [8] In this way we could explain why electron and hole mobilities show different trends in degradation in the bending test. Other research groups [9][10][11] observed similar trends in electron and hole mobility degradation.

Figure 5.7 SG-TFTs bend for reliability measurement on PEN foil

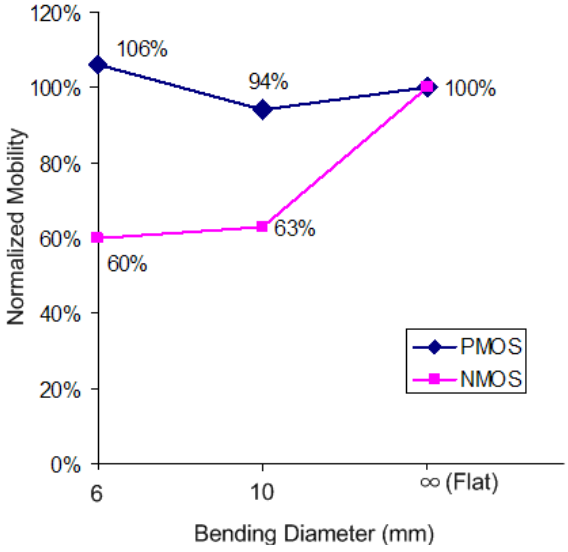


Figure 5.8 Normalized field-effect mobilities as a function of bending diameter

5.4 Improved Substrate Transfer Process: Double-Polyimide Process

To improve the device behavior and to restrain the device degradation under bending stress, another approach to the substrate transfer process was investigated, which we call the 'Double-Polyimide Process', as shown in Figure 5.9.

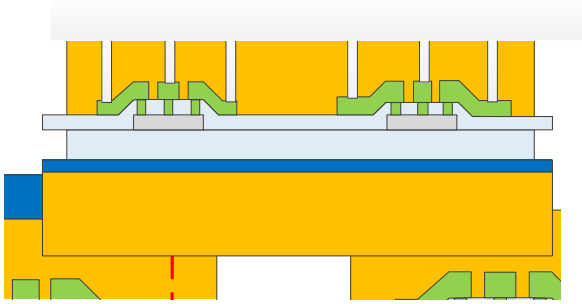


Figure 5.9 Illustration of the sandwiched structure of the 'Double-Polyimide Process'

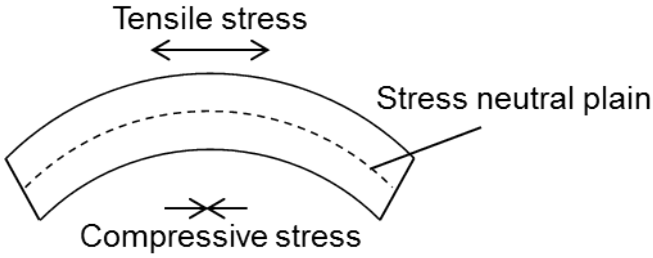


Figure 5.10 Illustration of the stress neutral plain in a film under bending

When a homogeneous film with a thickness of d is bent to the bending diameter of ϕ, the tensile strain on the upper surface of the film is $\frac{d}{\phi}$, and the compressive strain on the lower surface is also $\frac{d}{\phi}$. There is a stress neutral plain in a certain depth of the film. We could assume that it is approximately at the center of the film, as shown in Figure 5.10. [18] By using the sandwiched structure in Figure 5.6, the mechanical stress neutral plain is shifted to the device layer, and the flexible circuit could be bent to a smaller bending diameter. [18][19]

The process steps are as follows. After the single-grain Si TFTs fabrication from spin-coated liquid-Si, a polyimide layer with the thickness of 10 μm was

spin-coated on top of the devices. After that, contact holes were made to have access to the metal pads. Figure 9 is a photo of the flexible devices with the polyimide sandwiched structure. The bulk c-Si wafer was etched through from the backside of the wafer, using SiO_2 as a mask. The photo in Figure 5.11 shows the sample after the bulk etching, with the polyimide membrane supporting the detached devices. Then the devices were transferred to another polyimide substrate with a thickness of 10 μm. Figure 5.12 shows the photo of the transferred devices with the polyimide sandwiched structure.

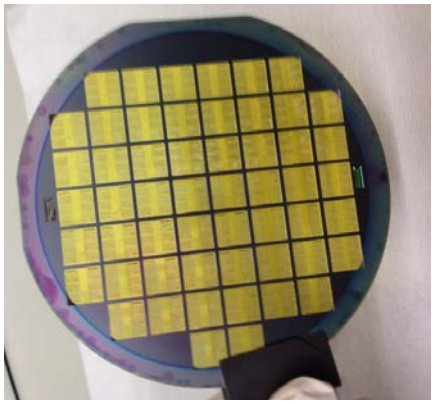


Figure 5.11 Photo of the devices after etching through the wafer from the back side

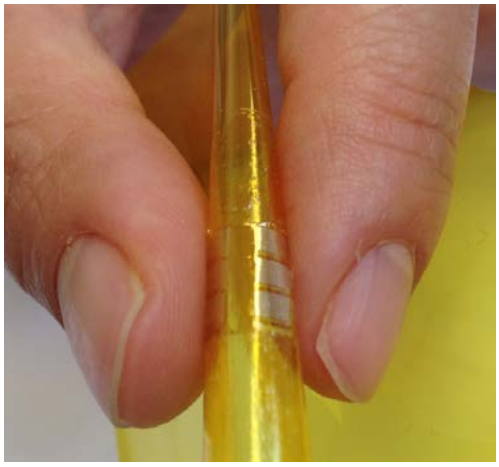
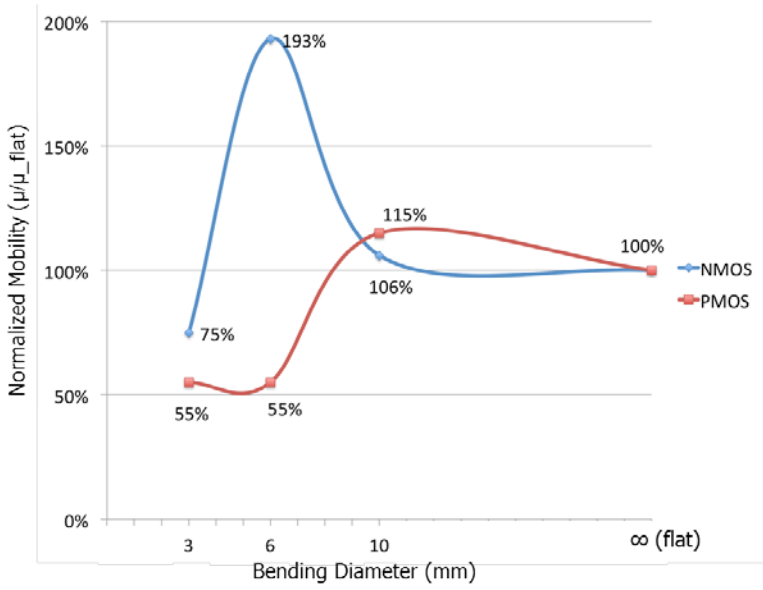
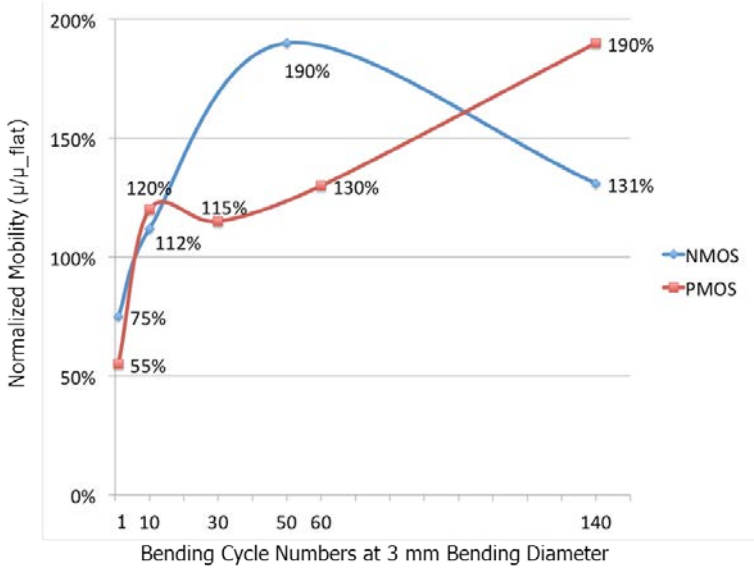


Figure 5.12 Photo of the flexible devices with the double-sided polyimide structure

Figure 5.13 (a) shows normalized mobilites of the NMOS and the PMOS TFTs with the double polyimide sandwiched structures when they are flat and bent at the diameter of 10 mm, 6 mm and 3 mm. Figure 5.13 (b) shows normalized mobilities after 10, 30 (for PMOS only), 50 (for NMOS only), 60 (for PMOS only), and 140 bending-release cycles with a bending diameter of 3 mm. Because of the minimized stress in the device layer, the cracking in the SiO_2 underlayer was limited and the devices were functional at the bending diameter down to 3 mm, which is 50 % improvement on the previous method. The bending does not affect the device performance as much as the substrate transfer process. After 140 bending-releasing cycles with a bending diameter of 3 mm, the devices were still functioning. The main reason for device failure would be the contact pad being scratched off after too many probings for the measurements, but not the transistor degradation. If the probing method is improved, the devices could function after many more bending cycles.



(a)



(b)

Figure 5.13 Normalized field effect mobilities as a function of (a) the bending diameter for the flexible devices with sandwiched structure, characterized when the devices were flat, bent at a bending diameter of 10 mm, 6 mm and 3 mm, and (b) the bending cycles after 10, 30, 50, 60, 140 bending-release cycles at a bending diameter of 3 mm.

5.5 Conclusion

To meet the growing demand and need for flexible displays, flexible TFTs have to be investigated. The substrate transfer processes to make the circuits flexible were studied and the performance of the flexible devices under the bending was characterized. The method that etches off polyimide and transfers to the PEN substrate results in the devices functioning with a bending diameter as small as 6 mm. An improved method is to etch through the wafer, landing on the devices with the polyimide layer supporting, and to transfer the devices to 10-μm thick polyimide foil. The bending behavior of the devices was improved, with the lowest bending diameter being 3 mm.

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CHAPTER 5 RELIABILITY OF THE FLEXIBLE SINGLE-GRAIN SI TFTS

Chapter 6

Low-Temperature SiO_2 Fabricated from Liquid-Si

In Chapter 1, we mentioned that a liquid-Si solution could be used for fabricating not only Si film, but also SiO_2 film. The Si film formation and the device characterization have been discussed in the previous chapters. In this chapter, we report a solution-processed SiO_2 layer. The oxide layer was fabricated from liquid-Si solution at a polyimide-compatible temperature of 350 °C. SiO_2 plays an important role in the IC industry for device insulation, the gate oxide, and the passivation of devices. A good quality SiO_2 layer with low fabrication temperature is the best choice for the gate oxide of thin-film transistors, especially in flexible circuits. In Section 6.1, we introduce the background and the application of the solution-processed SiO_2. The fabrication and the electrical characterization of the oxide layer is reported in Section 6.2. Section 6.3 discusses our attempt to make nanocrystalline Si dots by crystallizing the SiO_2 layer for the application in flash memories. Section 6.4 summarizes the chapter.

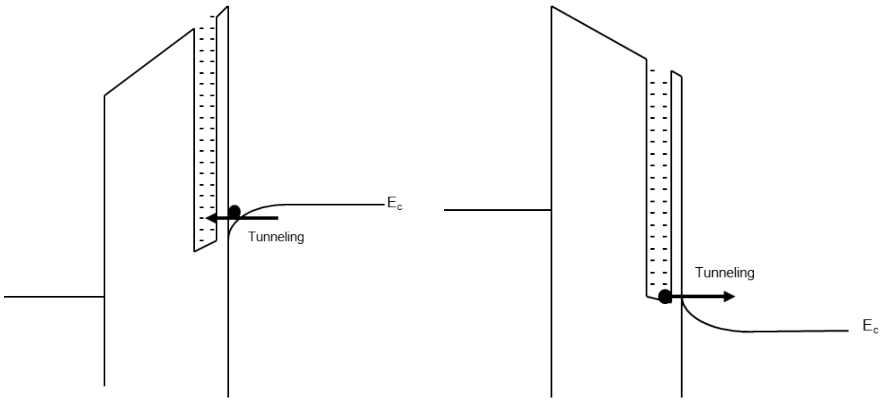
6.1 Introduction

In organic TFTs, metal oxide TFTs and Si TFTs, SiO_2 is mostly used as the gate dielectric layer, due to its ready availability by oxidizing the substrate wafer and its outstanding dielectric properties. Other types of dielectrics have been investigated, for example, high-k metal oxides (Al_2O_3, HfO, etc.) and polymer dielectrics (PMMA, PVA, etc.). High-k metal oxides have dielectric constants higher than SiO_2, thus the transistors could be operated at a lower gate voltage without scaling down the dielectric thickness, which benefits low power consumption and avoids an increase in leakage current due to a too thin dielectric layer. However, the ceramic-based metal oxides require a relatively high annealing temperature and certain substrate surface treatments to enhance their growth. Nevertheless, poor mechanical flexibility limits their application in flexible circuits. On the other hand, polymer dielectrics allow low-temperature solution deposition, and are suitable for flexible electronics, but the high leakage current is a problem. The dielectrics mentioned above are reviewed in [1]. SiO_2, with its large band gap (9 eV), low leakage current and low density of traps and defects, is therefore widely used in printed electronics research. [1]

For printed electronics, a low temperature gate oxide (lower than 350 °C) is needed to meet the temperature limit of the flexible substrate, replacing the thermal oxidized SiO_2 (900-1200 °C), used in the traditional IC industry. PECVD SiO_2 by TEOS, deposited at 350 °C is widely used in TFT fabrication, but the plasma causes interface trap states and affects the TFT performance. [2] Inductively Coupled Plasma (ICP) Enhanced CVD of SiO_2 at 250 °C includes an oxidation step and a following deposition step. It forms a good interface by using a remote plasma and reducing the bombardment. [3] But the oxidation at such a low temperature results in a too thin oxide thickness (10 - 20 nm) and a second layer of oxide is always needed for the gate oxide of the TFTs. A solution-processed SiO_2 layer was reported in [4], using a liquid-Si solution, which is composed of CPS monomer, polysilane and a solvent. Diluted liquid-Si solution was spin coated on the glass wafer substrate. It was baked at 220 °C for 60 min in an inert gas atmosphere to remove the solvent, break the Si-H bond and start the a-Si formation, followed by oxidation at 410 °C for 30 min in open air. A transparent SiO_2 film was reported. [4] It was calculated in [5] that the leakage current density of the SiO_2 processed from the liquid-Si solution was 1×10^{-8} A/cm^2 at 1MV/cm, which is sufficient for the application of the gate oxide, and TFTs using the solution processed SiO_2 as the gate oxide have been reported. [4]

Another concern about the application of solution-processed SiO_2 will be with flash memories using nanocrystalline Si (nc-Si) dots. They were first reported by Tiwari, et al. [6][7] The gate oxide of the TFT flash memory was

composed of a thin tunneling SiO_2 layer (1-3 nm), nc-Si dots, and a thicker controlling SiO_2 layer with a thickness of tens of nanometers. The nc-Si dots affect the band diagram of the gate oxide, forming quantum energy states of Si in the gate oxide layer, which was separated from the Si conduction band by the potential barrier of the tunneling SiO_2, as shown in the band diagram in Figure 6.1. Electrons could be injected into or extracted from the Si channel through the tunneling oxide layer when the 'writing' or the 'erasing' gate voltage is applied, changing the threshold voltage of the TFT.



(a) (b)

Figure 6.1 Illustration of the band diagram for MOS structure using a SiO_2 layer with nc-Si dots as the oxide layer, for the application of flash memory in a (a) a writing cycle and (b) an erasing cycle

The gate oxide layer with nc-Si dots could be processed in several ways, for example, depositing the tunneling SiO_2, Si and controlling SiO_2 sequently and annealing them at a temperature of 1100 °C [8], or depositing the SiO_2 and SiO_x ($x < 2$) in multiple cycles and annealing the stacked layer at a temperature of 600 °C. [9]

In our research, the processing temperature for the SiO_2 layer from the liquid-Si solution was reduced to a polyimide compatible temperature of 350 °C. The metal-oxide-silicon (MOS) capacitors using the resulting SiO_2 layer as the dielectric material were fabricated, and their capacitance was characterized and the interface trap density was extracted. On the SiO_x ($x = 1.66$) film, which was formed from the liquid-Si solution and oxidized at 350 °C, we applied the annealing (by excimer laser or flash lamp) of the nc-Si dots for the application of flash memories.

6.2 Low-temperature fabrication of SiO_2 using liquid-Si solution

SiO_2 film oxidized at 400 °C

In Chapter 1 and 2, we discussed SiO_2 formation from the liquid-Si solution. Similar to the a-Si process, in which CPS monomers were irradiated by UV light and polymerized to polysilane, which was then annealed in a N_2 atmosphere at a temperature higher than 350 °C to break the Si-H bonds and to form the 3D Si network, the SiO_2 layer was oxidized by baking the incompletely-annealed polysilane in air. [4] The oxidation step has to be performed after annealing the polysilane in the N_2 atmosphere to some extent, because a too early oxidation would result in a porous layer since polysilane is highly reactive with O_2, and too late oxidation would need high oxidation temperatures since the a-Si is already formed. [4] The details of the process are presented in Chapter 2.

Figure 6.2 is a photo of the SiO_2 film processed at 400 °C on top of a c-Si wafer. The film shows color changes among different regions of the wafer, which are caused by the non-uniformity due to manual coating.

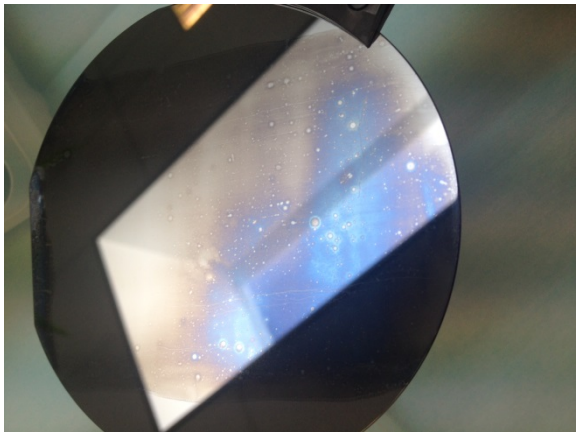
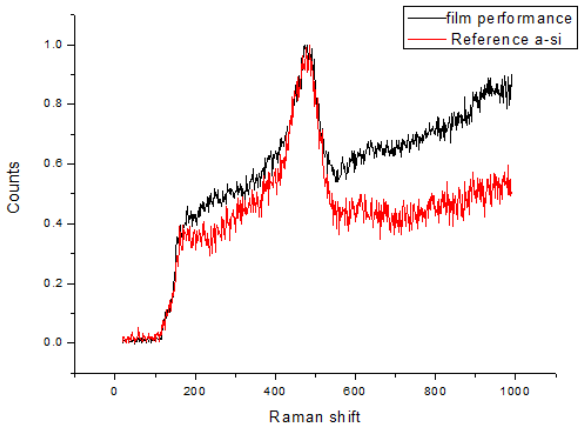
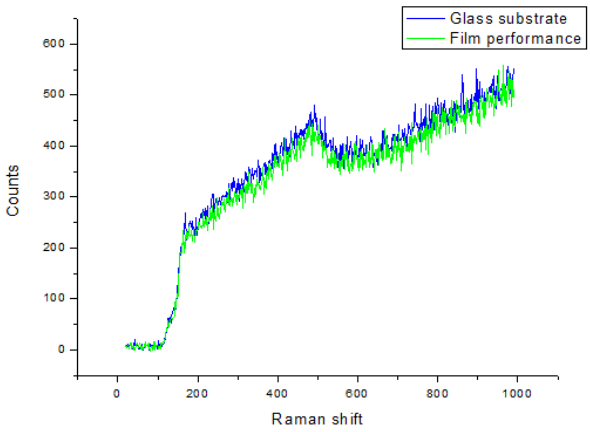


Figure 6.2 Photo of the SiO_2 film on top of a c-Si wafer, processed from liquid-Si solution at 400 °C

Figure 6.3 shows the Raman Spectrum of the a-Si film after 200 °C baking and the SiO_2 film after 400 °C baking on a glass wafer substrate. After baking at 200 °C, the a-Si film started to form but the quality was low. After 400 °C oxidation, the Raman spectrum of the film overlaps with that of the glass wafer substrate, which indicates that the film is completely oxidized or the film was too thin to be characterized. [5]



(a)

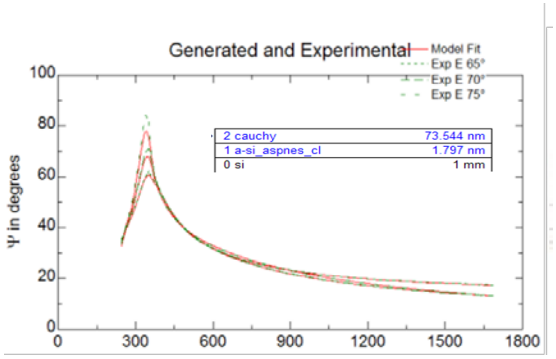


(b)

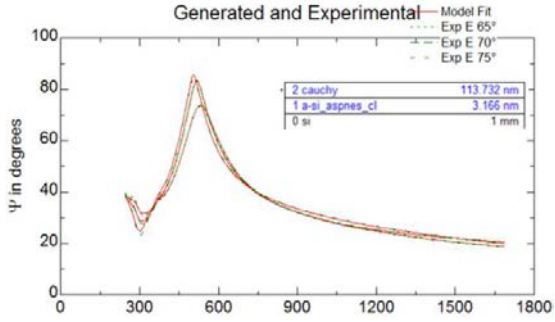
Figure 6.3 Raman spectroscopy of (a) the a-Si film after backing at 200 °C (black) compared with a reference a-Si film (red), and (b) the SiO_2 film after oxidation at 400 °C (green) compared with a glass substrate (blue)

Figure 6.4 shows ellipsometer measurement results of the SiO_2 film oxidized at 400 °C, measured in the regions with different film colors. For the location with thinner SiO_2 film, the film thickness was 73 nm and the refractive index was 1.46. For the other locations, the SiO_2 film had a thickness of 113 nm and a refractive index of 1.44. Compared with the refractive index value of the

thermal oxidized SiO_2, which is 1.458, [10], the solution-processed SiO_2 from liquid-Si solution shows a value close to thermal SiO_2. [5]



(a)



(b)

Figure 6.4 Ellipsometer measurement results of the SiO_2 film after oxidation at 400 °C, measured at (a) a thin section and (b) a thick section

Figure 6.5 is the X-ray Photoelectron Spectroscopy (XPS) of the resulting SiO_2 film, combined with the ion beam sputtering for the depth profile. [5] The average atom concentration ratio of O/Si is 1.79 in the film, which means that the film is a Si-rich SiO_2, probably caused by the low oxidation temperature. The O and Si atom concentrations changed steadily at the SiO_2-Si interface. The reason could be the inhomogeneity in the layer thickness at the measurement spot, or insufficient oxidation at the interface. Table 6.1 lists the O and Si atom concentrations at the surface. [5] Carbon atoms exist at the film surface but as

shown in Figure 6.5, the bulk SiO_2 film is carbon free. This is because the sodium ions on the film surface react with the CO_2 in the air, and carbonate was formed. [11]

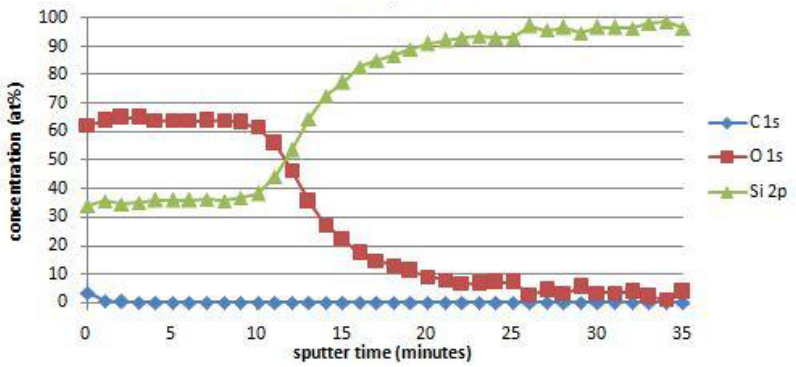


Figure 6.5 XPS spectroscopy depth profile of the SiO2 film after oxidation at 400 °C

Table 6.1 XPS result of the atomic concentrations on the surface of the SiO_2 film

Atoms	O	Si	O/Si
Concentration (at%)	65.4	32.2	2.03

MOS capacitors were fabricated to characterize the SiO_2 film electrically by means of a high-frequency capacitance-voltage (HF-CV) measurement and a current-voltage (IV) measurement. The SiO_2 film was deposited from the liquid-Si and was oxidized at 400 °C on a c-Si wafer. Al was sputtered onto both the front and the back sides of the wafer, forming the top electrode and the bottom contact. The dimension of the MOS capacitors is 720 µm by 720 µm. [5]

Figure 6.6 shows the HF-CV measurement results with a comparison to the theoretical HF-CV curve. [5] The measurement was done at the frequency of 1MHz . The curve is shifted from the theoretical curve due to the existence of fixed charges in the SiO_2. After the correction to cross the two curves at the mid-gap capacitance, in this case 95 pF, the fixed charge density and the interface trap density could be calculated. The fixed charge density in the oxide, Q_s, is 3.6×10^{11} $eV^{-1}cm^{-2}$. The interface trap states density is a function of the band bending at the interface, which is shown in Figure 6.7. [5] The mid-gap interface trap state density, D_{it}, is 5×10^{11} $eV^{-1}cm^{-2}$.

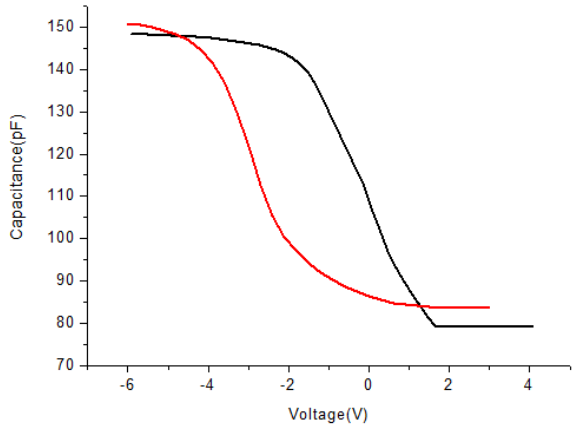


Figure 6.6 HF-CV curve (red) of the MOS capacitor fabricated with SiO_2 oxidized at 400 °C, compared to the theoretical curve (black)

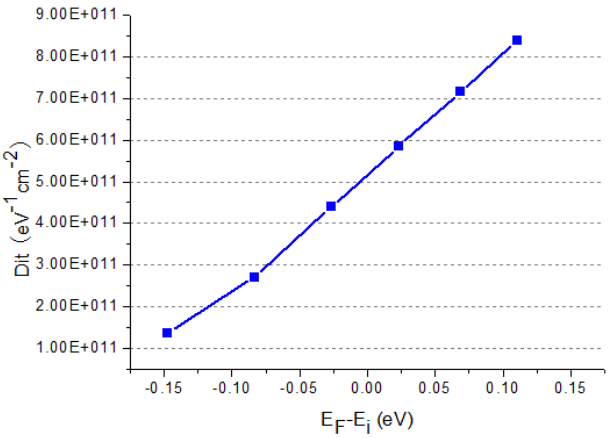


Figure 6.7 Interface trap state density D_{it} as a function of the energy band bending

Figure 6.8 shows the IV curve of the fabricated MOS capacitor. [5] The breakdown strength is defined as the electric field strength where the current density exceeds 1 μA/cm^2, and the resistivity is defined as the resistivity value at an electric field of 1MV/cm. Calculated from Figure 6.8, the breakdown electric field strength of the SiO_2 oxidized at 400 °C is 1.7 MV/cm, and the resistivity is 8×10^{12} Ωcm.

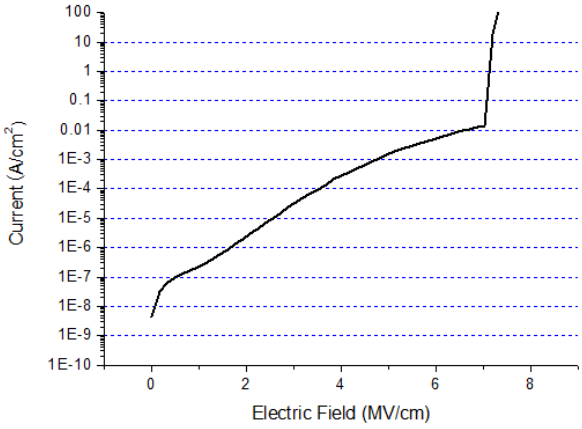
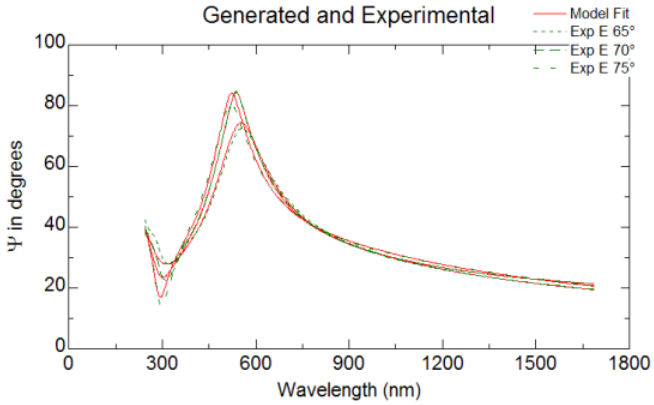


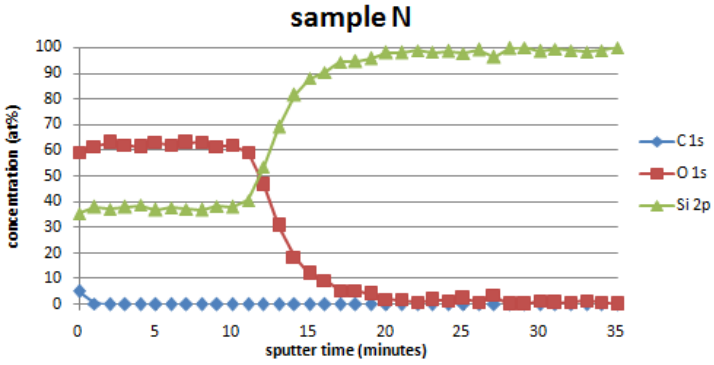
Figure 6.8 IV curve of the MOS capacitor fabricated with SiO_2 oxidized at 400 °C

SiO_2 film oxidized at 350 °C

To meet the temperature requirement of the polyimide substrate, which is a common substrate for flexible circuit processing, the fabrication of the SiO_2 film at 350 °C was studied. The process was the same as the fabrication at 400 °C, but the oxidation temperature in furnace with air was decreased to 350 °C. [5] Figure 6.9 (a) illustrates the ellipsometer results of the film, showing a 121-nm-thick SiO_2 film on top of a 49-nm-thick Si film, indicating incomplete oxidation at 350 °C. [5] The refraction index is 1.43. In Figure 6.9 (b), the XPS results are shown. The atomic ratio of O/Si is 1.66 in the film oxidized at 350 °C. [5] Compared with the value for 400 °C, which is 1.79, the lower oxidation temperature resulted in a lower O atom concentration, indicating a lower oxidation level of the film.



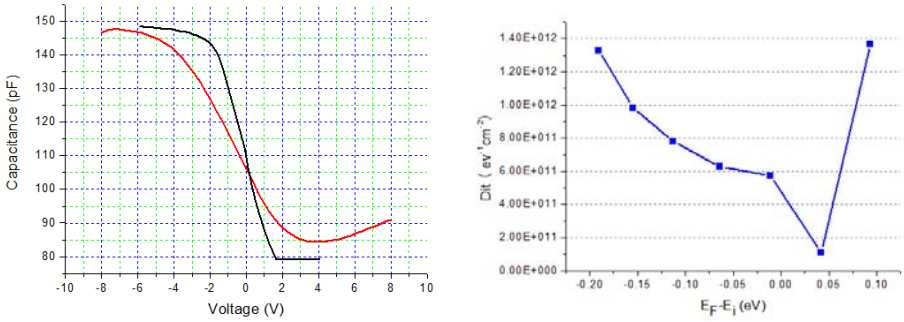
(a)



(b)

Figure 6.9 (a) Ellipsometer measurement results and (b) XPS depth profile of the SiO_2 film oxidized at 350 °C

The MOS capacitors were fabricated with the SiO_2 oxidized at 350 °C, using the same method as oxidation at 400 °C. The HF-CV curve is in Figure 6.9. [5] By shifting the measurement curve according to the mid-gap capacitance (95 pF), the fixed oxide charge, Q_s, is calculated to be -9.1×10^{10} $eV^{-1}cm^{-2}$. The interface trap density as a function of the band bending is also shown in Figure 6.10. The mid-gap interface trap density, D_{it}, is 2×10^{11} $eV^{-1}cm^{-2}$.



(a) (b)

Figure 6.10 (a)HF-CV curve and (b) calculated interface trap state density as a function of the band bending of a MOS capacitor with SiO_2 oxidized at 350 °C

The IV curve of a MOS capacitor is shown in Figure 6.11. [5] The breakdown electric field strength is 1.12 MV/cm, and the film resistivity is 1.1×10^{12} Ωcm.

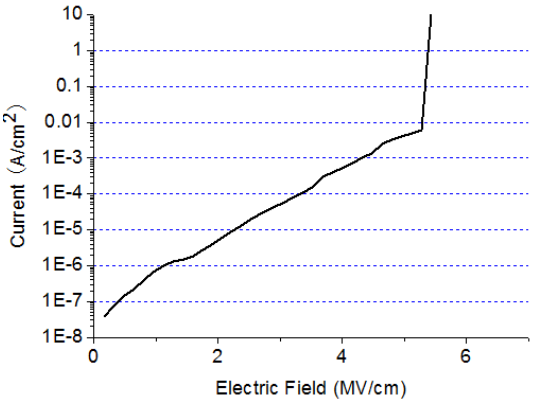


Figure 6.11 IV curve of a MOS capacitor with SiO_2 oxidized at 350 °C

6.3 Crystallization of the SiO_2 film to form nanocrystalline Si dots

Flash Lamp

The flash lamp we used is the Novacentrix Pulse Forge 1300 Photonic Curing System. It contains a Xenon strobe and provides pulsed flash light for high temperature thermal processes of thin films on low temperature substrates. Since the pulse is as short as 1 ms, the induced heat is fast enough to sinter the thin-film material before it transfers to the substrate. Its output is a relatively broad spectrum of 200-1500 nm and a relatively large shooting area of 75 x 150 mm, thus enabling high throughput. By changing the back voltage of the flash lamp, the system varies the output of photonic energy. Figure 6.12 is a photo of the flash lamp system.

Figure 6.12 Photo of a flash lamp system

Experiment

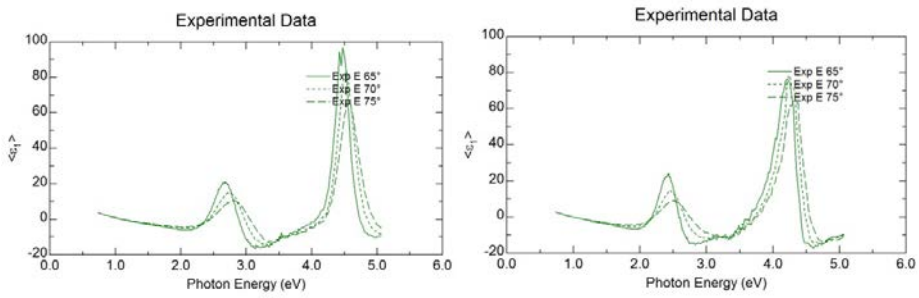
On the SiO_x (x=1.66) film, which was processed from the liquid-Si solution with the oxidation temperature of 350 °C, the XeCl excimer laser (308 nm) and the flash lamp are applied to anneal the Si-rich silicon oxide layer to investigate the crystallization of the nanocrystalline Si (nc-Si) dots.

The observation of the nc-Si dots using microscopy or scanning electron microscopy (SEM) is difficult considering the dot dimension ($<$5 nm). The direct observation could be done by transmission electron microscopy (TEM).

[7] Several indirect ways could also determine the existence of the nc-Si dots, for instance, the change of the peak in the dielectric function ε_1 , using the ellipsometer measurements [9] [12] and the change in amorphous Si and crystalline Si peak in Raman spectroscopy.

Different annealing methods and different observation methods have different requirements on the substrate. The flash lamp annealing needs a glass wafer substrate to prevent the heat conduction of the Si wafer. The Raman spectroscopy also prefers a glass wafer substrate to avoid the strong background signal of c-Si peak from the Si wafer. In contrast, the ellipsometer measurements require a Si wafer substrate for the reflection. Different energy densities of the excimer laser and the flash lamp were tested on the oxide layer, and Figure 6.13 shows the ellipsometer results of our attempt to form nc-Si dots. The second peak of the dielectric function ε_1 decreased after the excimer laser annealing of 20 shots with an energy density of 100 mJ/cm^2, 20 shots of 300 mJ/cm^2, 200 shots of 500 mJ/cm^2, and 1 shot of 800 mJ/cm^2. The decrease of the peak value indicates the formation of nc-Si. [9]

Figure 6.14 shows the TEM image of the nc-Si dots in the SiO_2 film. The image is taken with an energy filtered TEM (EFTEM), in which electrons with an element-specific energy loss are filtered for making the image. Regions containing the specific atoms become bright in the image. The bright spots in the figure indicate the existence of the nc-Si dots.



(a) (b)

Figure 6.13 Dielectric function ε_1 as a function of photon energy, measured by the ellipsometer (a) as deposited SiO_2 layer and (b) after laser annealing

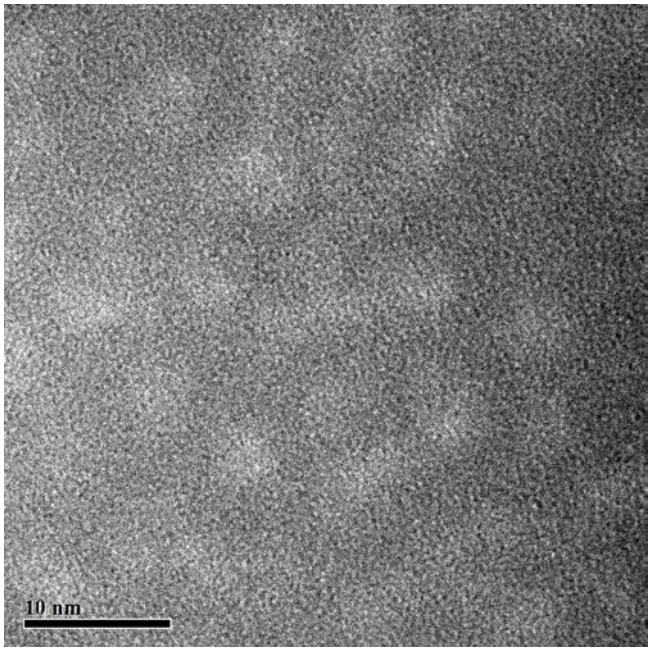


Figure 6.14 TEM image showing the existence of nc-Si dots (brighter spots in the figure) inside the SiO_2 film

Another attempt is to make the nc-Si dots by making a $(SiO_2\text{-}Si)_n$ stacked layer of the solution-processed a-Si film and SiO_2 film. Both of the layers were fabricated from the liquid-Si with a process temperature of 350 °C. Two SiO_2 films were coated on top of a glass wafer substrate with a thin a-Si film sandwiched in between. A transparent, light brown film was made at last. After the laser treatment and the flash lamp treatment, no change was observed using Raman spectroscopy.

6.4 Conclusion

In this chapter, we discussed the low-temperature fabrication of the SiO_2 film from the doctor-blade coated liquid-Si. The coated sample was first baked in an inert gas atmosphere for the early stage of the amorphous Si formation and then oxidized in a furnace with air. The oxidation procedures at 400 °C and 350 °C were investigated. The MOS capacitors were fabricated to characterize the oxide layer. For the SiO_2 film oxidized at 400 °C, the layer shows an atomic ratio of O/Si of 1.79, and a breakdown electric field strength of 1.7 MV/cm. For the film obtained at 350 °C, the atomic ratio O/Si is 1.66 and the breakdown

happens at 1.1 MV/cm. The Si-rich SiO_2 film was treated with the excimer laser and the flash lamp to form the nc-Si dots. The ellipsometer results indicate the formation of nc-Si dots.

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Chapter 7

Conclusions and Recommendations

7.1 Conclusions

This thesis focuses on single-grain Si TFTs fabricated from a printed liquid-Si solution on a flexible substrate, for the application of high-performance flexible circuits. Printing is attractive for manufacturing flexible circuits. It is low in cost since it has no lithography and does not need a vacuum. It is also compatible with roll-to-roll processes. Organic and metal oxide semiconductor TFTs have been investigated for printed circuits, but their mobility and reliability are inferior to the c-Si transistors in the IC industry. This thesis solves the problem of the low performance of low-temperature-processed TFTs, by demonstrating the creation of single-grain Si TFTs from liquid-Si solution and the µ-Czochralski process, thus balancing the high performance of the transistors and the low process temperature. The conclusions are listed as follows:

- Top-gated structures and the self-alignment source/drain doping by ion implantation are used in the process for single-grain Si TFTs. The single grains are formed from the a-Si on top of the 'grain-filters' by µ-Czochralski crystallization, using a XeCl excimer laser with a wavelength of 308 nm. The activation of the source and drain dopants are also done by the laser at room temperature. To avoid the unintended burning by the laser shot of the polyimide substrate, the devices are placed in squares with the same dimension of the laser shot, and extra Al gate patterns are needed to cover the substrate.
- The liquid-Si solution is a mixture of CPS monomer, polysilane polymers from UV-polymerized CPS, and solvent. It could be spin coated onto the substrate and annealed at the temperature of 430 °C to become a-Si. It is dehydrogenated in an inert gas atmosphere at 650 °C prior to the XeCl excimer laser crystallization. The maximum grain dimension is 3.5 µm. The carrier mobility of the single-grain Si TFTs are 423 cm^2/Vs and 118 cm^2/Vs, for electrons and holes, respectively. NMOS TFTs show stable behavior under gate and drain stress, and negligible hysteresis. On the other hand PMOS TFTs show trap generation and carrier injection from the gate.
- With doctor-blade coating of the pure CPS monomers, UV polymerization and annealing at 350 °C, an a-Si film could be fabricated on the polyimide substrate, meeting the temperature requirement of the polyimide and making it compatible to roll-to-roll process. The dehydrogenation and the crystallization are both performed by the laser at room temperature, resulting in single grains with a dimension of 3 µm. Single-grain Si TFTs and CMOS inverters are fabricated on top of the polyimide substrate, showing mobilities of

460 cm^2/Vs and 121 cm^2/Vs for electrons and holes, respectively. The devices show stability, in the sense that no charges are induced in the measurement.

- By etching off the polyimide and transferring the devices onto a flexible PEN substrate with a thickness of 125 µm, the devices become flexible. The bending diameter can be as low as 6 mm. An improved substrate transfer process is also investigated. With the polyimide substrate of 10 µm, the devices could be bent up to a diameter of 3 mm.
- The SiO_2 layer is fabricated from the liquid-Si solution at 400 °C and 350 °C, using the doctor-blade coating method. With the resulting SiO_2 layer, MOS capacitors are processed. The atomic ratio of the O/Si is 1.79 for the SiO_2 film fabricated at 400 °C, and 1.66 for that fabricated at 350 °C. The breakdown electric field strength is 1.7 MV/cm for the former and 1.1 MV/cm for the latter. The Si-rich SiO_2 film is crystallized using a laser for the nc-Si dots.
- To prepare for high-frequency applications of single-grain Si TFTs, the design rules of high-frequency transistors, ring oscillators and the sensor resistors are studied..

7.2 Recommendations for Future Work

Single-grain Si TFTs fabricated from the printed liquid-Si solution show a high performance in regard to carrier mobility and reliability. The manufacturing temperature is so low that the devices could be processed directly on top of the flexible polyimide substrate. The research we have done in this thesis reveals a promising method for printing flexible circuits in the future. For further research on this project, the recommendations are as follows.

- The high performance of the single-grain Si TFTs relies on the high quality of the grains crystallized on top of the grain filters using the µ-Czochralski process. The a-Si that is dehydrogenated at 650 °C could be crystallized by a laser with a pulse duration of 250 ns and 25 ns. While for the a-Si film dehydrogenated at room temperature by the laser, the dehydrogenation and the crystallization could only be done using a laser with 250 ns. The dehydrogenation mechanism by the laser in the grain filters needs to be studied further. The reason why a longer laser pulse results in better dehydrogenation and crystallization, and the threshold pulse duration above which the dehydrogenation and crystallization could be done, need to be investigated.
- The gate oxide fabricated from a liquid-Si solution, a result of primary research, shows reasonable values for both the atomic ratio and the breakdown electric field strength. For further research two branches of

the topic could be considered. One is to optimize the oxidation process for a completely-oxidized, dense, low-interface-state SiO_2 layer, at the same time lowering the process temperature to less than 200 °C. The resulting low-temperature high-quality SiO_2 will be a good candidate for the gate oxide in future printing processes. Another idea is to make the SiO_2 layer less oxidized, thus Si richer, as the precursor of laser-crystallized nc-Si for flash memories.

- Considering the mechanical stress induced in the substrate transfer process, a ultra-low stress substrate transfer method and a water-assisted nickel release process are of interest. [1][2] A thin nickel layer (300 nm) was sputtered onto the thermal oxide by wet oxidation on a Si wafer. On the nickel layer a polyimide substrate was spin-coated and cured, on top of which the devices were fabricated, as shown in Figure 7.1. The whole structure was soaked in water, with an edge of the nickel peeled off to start water penetration. Within a few seconds, the nickel layer (together with the devices) separated from the SiO_2/Si wafer. The water-assisted nickel release process depends on the subcritical debonding at the Ni/SiO_2 interface. The nickel layer could eventually be easily removed in the wet etchant. The releasing process would cause negligible mechanical stress on the devices, and it allows a wafer-scale process. However, nickel is not a green metal, hence special complete capping and passivation of nickel should be performed to prevent the contamination of the devices and the clean room and to avoid unexpected layer peeling in the process.

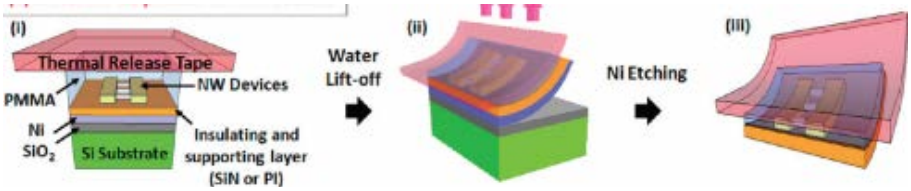

Figure 7.1 Illustration of the water-assisted nickel release process.

- The carrier mobility of the flexible single-grain Si TFTs from the liquid-Si on a polyimide substrate is as high as 460 cm^2/Vs. With this good result, our final goal, the 'super e-paper' does not seem that far away. The 'super e-paper' is the integration of the display, the display driver circuit, the RF module, the CPU, the RAM and the analog circuits on a flexible substrate. In this thesis, we have already demonstrated the CMOS invertors. A topic we could not avoid is the uniformity of the Si film on wafer and from wafer to wafer, and of the

laser beam in one shot and from shot to shot. After solving the uniformity issue, the model of the TFTs could be extracted, and complex circuits could be designed according to the model. In the Appendix, some initial work for investigating more complex circuits is shown, including ring oscillators, high-frequency transistors and sensors. Starting with the work in the Appendix, larger circuits could be designed and processed with liquid-Si technology.

- The single-grain Si TFT fabrication process from liquid-Si solution with a low process temperature (<350 °C) is worth being considered for solar-cell fabrication because of its low cost and high performance. In the future, the process temperature could be decreased even more (< 150 °C) for the fabrication on the low-cost plastic substrate, or even paper substrate. The high quality Si and SiO_2 film fabricated from the liquid-Si solution could be considered for the all-solution process as well.

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Appendix A

Circuits Using Single-Grain Si Transistors: High-Frequency Responses, Ring Oscillators and Sensors

Single grain Si TFTs on an a-Si precursor from a liquid-Si solution perform as well as their c-Si counterparts, as demonstrated in Chapter 3 and Chapter 4. Thus they could be used in RFID tags, display drivers, and other high-speed electronic circuits. In this chapter the design for the circuits using the single-grain Si TFTs is demonstrated. They include high-frequency transistors which will characterize the cut-off frequency of TFTs, ring-oscillators, and semiconductor resistor sensors for the application of piezo and temperature sensors. Section A.1 introduces the research status of high-frequency RFID tags using TFTs. The design rules for the high-frequency transistors are explained in Section A.2. Section A.3 shows our design of the circuits. The conclusion of this chapter is in Section A.4

A.1 Introduction

Radio frequency identification (RFID) technology is increasingly being developed in industry for handling goods and materials. [1] It needs transistors and circuits that function at high frequencies, but at the same time a low fabrication cost for cheap commercial applications. The printing method, which has been discussed intensively in the previous chapters of this thesis, could provide a low-cost production approach since it does not need a vacuum or a lithography process, and it could be performed on top of various substrates, including glass and plastic substrates, which reduces the costs even more. TFTs functioning at high frequencies have been reported by several groups, such as organic TFTs with a cut-off frequency of 20 MHz [2], InGaZnO TFTs with 10.7 MHz [3] and carbon nanotubes TFTs with 170 MHz [4]. All-printed RFID tags have been fabricated by using a metal oxide semiconductor for the NMOS TFTs and an organic semiconductor for the PMOS TFTs [5], and by using a single-walled carbon nanotube (SWCNT) TFTs [6], both of which function at the typical RFID frequency of 13.56 MHz [1]. While the other selected frequency for RFID, the ultra-high frequency (UHF) of 2.45 GHz, is difficult to achieve with the above semiconductors due to limitations of the materials. Saputra et al. have reported asingle-grain Si TFTs made by the μ-Czochralski crystallization process of the LPCVD Si, with an electron mobility and a cut-off frequency of 600 cm^2/Vs and 5.45 GHz. The cut-off frequency is in the range of 2.45 GHz, but the process costs are high due to the vacuum and high-temperature processes. [7]

The single-grain Si TFTs from the liquid-Si on the polyimide substrate show an electron mobility of 460 cm^2/Vs, the fabrication with a maximum process temperature of 350 °C has been discussed in Chapter 4. A high cut-off frequency is expected to be achieved in TFTs designed for the RFID circuits working at the UHF frequency of 2.45 GHz because the electron mobility is in the c-Si counterpart.

In this chapter, we would like to present our design of high-frequency transistors to characterize the cut-off frequency of single-grain Si TFTs. Ring-oscillators and sensors were also designed for the TFTs with the same process. Our final application would be the 'super e-paper', which integrates TFTs, analog and digital circuits, the memory, the display, the RFID, and the antenna, together on top of a flexible substrate.

A.2 Design rules for high-frequency TFTs

Output Power Requirement

For s-parameter measurement of the cut-off frequency, a certain output power is needed to meet the measurement resolution. If a single transistor could not provide enough power for the measurement, a solution is to increase the applied gate voltage and drain voltage until the output power could be detected. However, the transistor would be pushed to extreme working conditions, thus the output alternate current (ac) signal of the positive output and the negative output are not symmetric. The measured cut-off frequency will be lower than the original value of the devices.

One example is given in Figure A.1. The TFTs were fabricated on single Si grains from the liquid-Si solution by the μ-Czochralski excimer laser crystallization, with the manufacturing process discussed in Chapter 4. The dimension of the channel is 1μm by 1 μm. Usually the devices were biased with a drain voltage of 0.02 V for working in the linear region, as shown in the transfer characteristics in Figure 4.8. But they have to be biased at a drain voltage of 7 V and a gate voltage of 8 V to present a measureable signal for a detectable s-parameter measurement. The measured cut-off frequency of the TFTs was 167 MHz, which is much lower than our expectation.

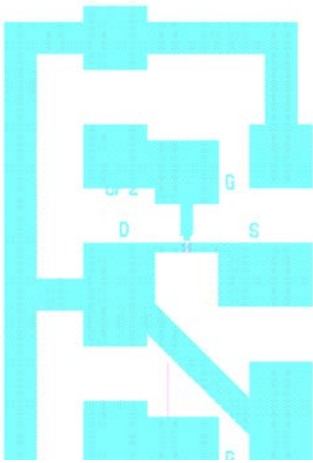


Figure A.1 Picture of the layout of a single-grain Si TFT with gate dimension of 1μm / 1 μm, with a measured cut-off frequency of 167 MHz

To solve the problem of insufficient output power, a wider transistor or even an array of transistors would be needed to obtain a higher width-length

ratio, W/L. A wide single-grain Si TFT from LPCVD Si with the length of 1.5 μm and a total width of 500 μm is shown in Figure A.2 [7]; it has a cut-off frequency of 5.45 GHz measured by a high-frequency parameter analyser. There is no clear value for the width-length ratio that will allow the detection of the signal, so a series of RF-transistors with different W/L ratios should be combined.

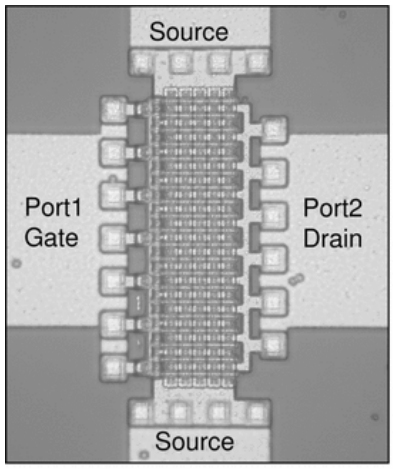


Figure A.2 A photo of an RF-transistor with agate dimension of 500 μm / 1.5 μm, with a measured cut-off frequency of 5.45 GHz

Connecting Network Requirement

The needle for high-frequency measurement is a group of 3 small needles with a fixed distance (100 μm or 125 μm), as illustrated in Figure A.3. Thus the contact pads should be designed with a distance between them of 100 μm or 125 μm, and a size of at least 60 μm by 60 μm for the probing contact. An easier way to design the pads is to make the ground signal Pad (G in Figure 7.4) longer to match both 100μm- and 125μm-pitch needles, as shown in Figure A.4.

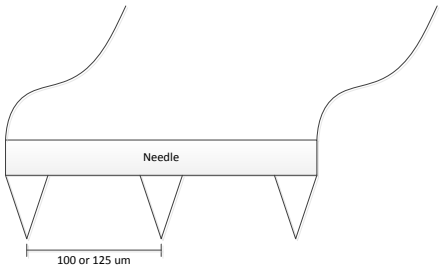


Figure A.3 Illustration of the measurement probe for high-frequency measurements.

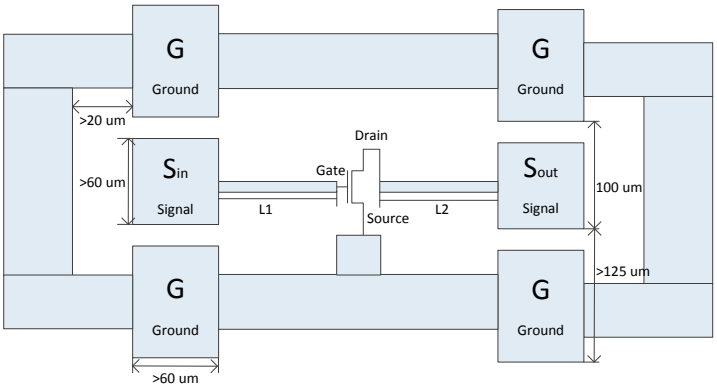
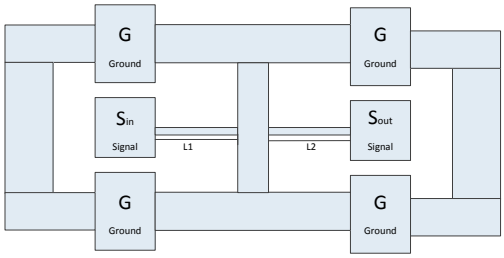
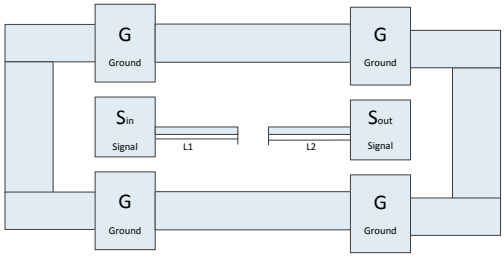


Figure A.4 Design of a connection network for a high-frequency TFT

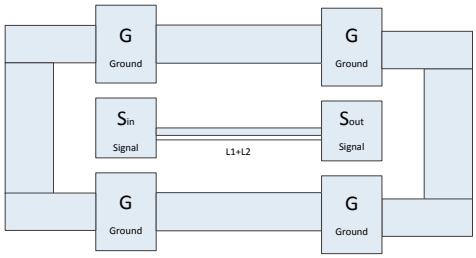
Some calibration structures must be added to remove the influence of the connecting network for more accurate measurement. The ‘Short’, ‘Open’ and ‘Through’ structures, shown in Figure A.5, are usually required.



(a)



(b)



(c)

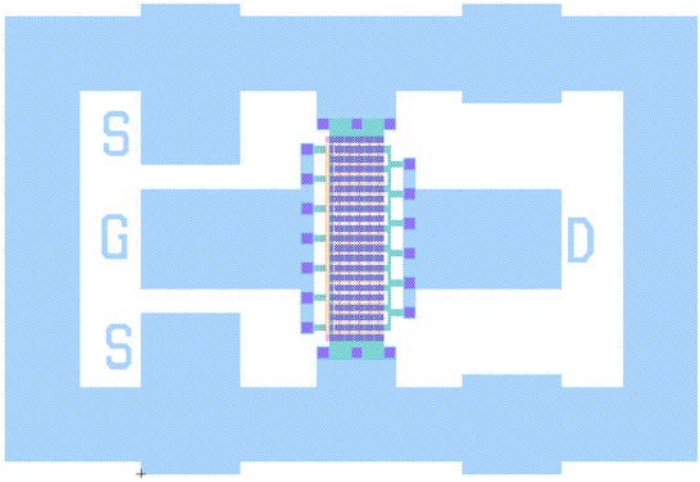
Figure A.5 Illustration of the calibration structures, (a) the 'short', (b) the 'open' and (c) the 'through' structures

A.3 Layout Design of High-Frequency Transistors, Ring Oscillators and Sensors

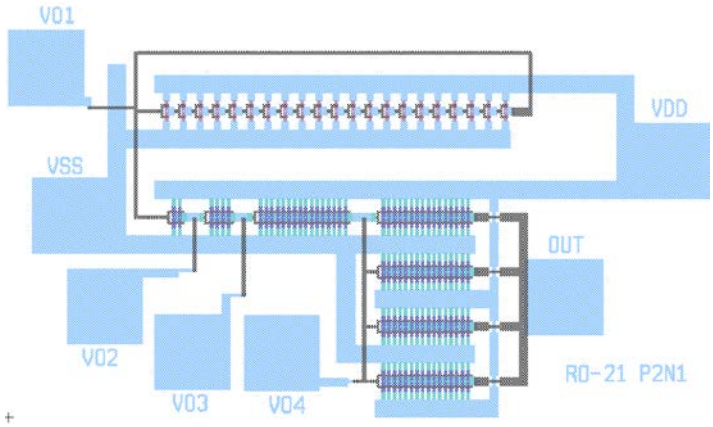
Several device layouts have been designed, including high-frequency transistors, ring-oscillators and simple resistor sensors. Figure A.6 shows the pictures of the layouts for a high-frequency transistor with the width-length ratio, W/L, of 100, a ring oscillator with 21 stages of inverters and a 4-stage output buffer with a 2-

stage invertor, a 4-stage invertor, a16-stage invertor and a 64-stage invertor, and a resistor sensor for temperature and stress sensing with a length of 450 µm and a width of 1 µm. Considering the maximum grain dimension is 3 µm, after the laser crystallization of the solution-processed a-Si film, as shown in Chapter 4, the gate length and width of all the transistors in the design are less than 3 µm. A series of circuits have been designed, including high-frequency TFTs with a width-length ratio, W/L, of 60, 100, 200 and 400, ring-oscillators with the number of the inverter stages of 5,11, 21, 31, 51, 101 and 151, and resistor sensors with a length of 300 µm, 450 µm and 685 µm.

The devices would be fabricated on top of the polyimide substrate using the same process as described in Chapter 4, with a maximum process temperature of 350 °C. The inverters have been successfully demonstrated, as shown in Chapter 4. The results of the cut-off frequency, the ring-oscillators and the sensors will be added to this work after fabrication and characterization.



(a)



(b)

(c)

Figure A.6 The layout of (a) a high-frequency TFT, (b) a ring-oscillator, and (c) a resistor sensor

A.4 Conclusion

For the application in RFIDs and 'super e-paper', low-cost fabrication of TFTs with high cut-off frequencies is needed. The printed single-grain Si TFTs on a polyimide substrate, from doctor-blade coated liquid-Si solution, uses low-cost fabrication techniques and shows a potential for high-frequency applications. In this chapter the design for characterizing the cut-off frequencies of the TFTs is shown, together with the ring-oscillators. Characterization of the circuits needs to be done in the future.

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APPENDIX A CIRCUITS USING SINGLE-GRAIN SI TRANSISTORS: HIGH-FREQUENCY RESPONSES, RING OSCILLATORS AND SENSORS

Summary

Liquid-Si Technology for High-Speed Circuits on Flexible Substrates

Recently, flexible, wearable and disposable electronics have attracted a lot of attention. Printing enables low-cost fabrication of circuits on flexible substrates. Printed organic and metal oxide thin-film transistors (TFTs) have been researched intensively due to the ease of solution-processing. But their carrier mobility and reliability are inferior to conventional CMOS transistors fabricated with crystalline Si. Printed Si TFTs have also been reported, including amorphous Si and poly-crystalline Si TFTs. Both techniques are based on a precursor of liquid-Si solution. The high temperature required for forming Si film and the low mobility due to randomly positioned grain boundaries inside the channel region are limitations for fabricating high-speed circuits on flexible substrates. In this thesis single-grain Si TFTs with high performance produced at a low temperature (< 350 °C) from a printed liquid-Si solution on a flexible substrate is presented. Applications may include display drivers, flexible memories, printed RFID tags and other high-speed circuits on flexible substrates.

Liquid Si is the mixture of a cyclopentasilane (CPS) monomer, UV-polymerized CPS and solvent. It can be spin coated on top of a substrate. Under thermal treatment, the solvent is evaporated, Si-H bonds are broken, and an amorphous Si film is formed. After the film is thermally annealed at 650 °C for dehydrogenation, it is crystallized by a XeCl excimer laser (308 nm) to make location-controlled single grains, using the μ-Czochralski crystallization method. Top-gated Si TFTs are fabricated with the channel inside a grain, and self-alignment source/drain doping by ion implantation is employed in the process. In Chapter 3, the fabrication process is discussed in detail. Due to the

absence of grain boundaries in the channel region, the TFTs show carrier mobilities of 423 cm^2/Vs for electrons and 118 cm^2/Vs for holes, which are higher than those of organic-, metal oxide-, a-Si- or poly-Si TFTs. NMOS TFTs show stable behavior under gate and drain stress, and negligible hysteresis effect. On the other hand, PMOS TFTs show trap generation and carrier injection from the gate.

To meet the temperature requirements for fabrication on flexible substrates, a low-temperature (<350 °C) process is demonstrated in Chapter 4. With doctor blade coating of pure CPS monomers, curing using UV light, annealing at 350 °C and dehydrogenating by excimer laser at room temperature, an amorphous film with low hydrogen concentration can be formed on top of a polyimide substrate without damaging the substrate. Single-grain Si TFTs are fabricated using a low-temperature a-Si film, and the carrier mobility is 460 cm^2/Vs for electrons and 121 cm^2/Vs for holes. This is the first time that single-grain Si TFTs are fabricated on top of a flexible substrate.

By etching away the polyimide substrate, the devices are released from the supporting Si wafer, and are then transferred onto a 125 μm-thick PEN foil, becoming flexible. The bending diameter, which is the diameter one can bend until device destruction, is as low as 6 mm. An improved substrate transfer process is investigated in Chapter 5. By placing the devices between two layers of 10-μm-thick polyimide, the devices could be bent to a diameter of 3 mm. They survive 140 bending-releasing cycles at 3 mm. Theoretically they function after many more cycles.

SiO_2, as the most important dielectric in the semiconductor industry, is also investigated for low-temperature fabrication from the same liquid-Si solution. SiO_2 is fabricated at 350 °C, using a doctor-blade coating method and oxidation of the incompletely thermally annealed a-Si in oxygen plasma. As shown in Chapter 6, the atomic ratio O/Si of the resulting oxide film is 1.66, and the breakdown electric field strength is 1.1 MV/cm. Besides being a dielectric layer, the Si-rich SiO_2 film can be crystallized by an excimer laser to form nanocrystalline Si dots for flash memory applications.

This thesis deals with liquid-Si technology for high-speed circuits on flexible substrates. The work focuses on flexible single-grain Si TFTs and low-temperature silicon oxide. Upon satisfactory performance of the resulting devices, future work could be done on new processes for lower-temperature fabrications, new substrate transfer methods for more flexible devices and new circuit designs for complex digital or analog circuits.

Samenvatting

Vloeibaar-Si Technologie voor hogesnelheid circuits op flexibele substraten

Flexibel, draagbaar en wegwerp elektronica heeft veel aandacht gekregen over de afgelopen jaren. Printen maakt het mogelijk om circuits op flexibele substraten goedkoop te fabriceren. Geprinte organische en metaal-oxide dunne-film transistoren (TFTs), zijn veel onderzocht vanwege het gemak van oplossing-gefabricatie. De ladingsdragermobiliteit en betrouwbaarheid daarentegen komen tekort ten opzichte van de gebruikelijke CMOS transistoren gefabriceerd met kristallijn Si. Geprinte Si TFTs zijn ook verschenen in zowel amorphous Si als in Poly-kristallijn Si vorm. Beiden geproduceerd vanuit een precursor van een vloeibaar-siliciumoplossing. Helaas vormden het gebruik van hoge temperaturen voor de vorming van een Si laag, en de lage mobiliteit door de willekeurig geplaatste kristalgrenzen binnen het kanaal gebied, beperkingen voor het fabriceren van hoge-snelheid circuits op flexibele substraten. In dit proefschrift worden hoog presterende *single-grain* Si TFTs gefabriceerd op lage temperatuur (<350 °C) vanuit een geprinte vloeibaar-Si oplossing op een flexibel substraat, voor de toepassing van beeldschermbesturing, flexibel geheugen, geprinte RFID tags en andere hoge-snelheid toepassingen op flexibele substraten.

Vloeibaar-Si is een mengsel van cyclopentasilaan (CPS) monomeer, UV-gepolymerizeerd CPS en een oplosmiddel. Het kan opgesponnen worden bovenop een substraat. Met een thermische behandeling verdampt het oplosmiddel, Si-H verbindingen worden verbroken, en een amorphous Si laag wordt gevormd. Nadat de laag is verhit tot 650°C om waterstof te verwijderen, is deze gekristalliseerd met een XeCl excimer laser (308 nm) om locatie gestuurde enkel-graan te maken via de μ-Czochralski kristallisatie methode.

Boven-gate Si TFTs zijn gefabriceerd met een kanaal binnen een graan. Zelf-uitlijning voor de source en drain doping via ion implantatie is gebruikt in dit proces. In hoofdstuk 3 wordt verder ingegaan op het productieproces. Vanwege de afwezigheid van graangrenzen binnen het kanaal hebben de TFTs ladingsdragermobiliteiten van 423 cm^2/Vs voor de elektronen en 118 cm^2/Vs voor de gaten. Deze waarden zijn hoger dan die van organische-, metaal-oxide-, a-Si- of polysilicium TFTs. NMOS TFTs zijn stabiel onder gate en drain spanning, en hebben een verwaarloosbare hysterese effect. PMOS TFTs laten echter een valgeneratie en ladingsdrager injectie zien vanuit de gate.

Om de temperatuureisen voor het gebruik van flexibele substraten te waarborgen, wordt een laag-temperatuur (<350 °C) proces gedemonstreerd in Hoofdstuk 4. Met het doctor-blade bekleding van puur CPS monomeren, uitharding met een UV belichting, verhitting op 350 °C en het verwijderen van waterstof met de excimer laser op kamertemperatuur, kan een amorphous silicium laag met lage waterstof concentratie gevormd worden bovenop een polyimide substraat zonder schade aan het polyimide laag. *Single-grain* Si TFTs zijn geproduceerd met deze lage temperatuur a-Si laag en de ladingsdrager mobiliteit resulteerde in 460 cm^2/Vs voor electronen en 121 cm^2/Vs voor gaten. Dit is de eerste keer dat *single-grain* Si TFTs zijn gefabriceerd bovenop een flexibel substraat.

Door het polyimide substraat weg te etsen, zijn de transistoren losgemaakt van de onderliggende Si wafer, en vervolgens overgedragen op een 125 μm dik PEN folie, waardoor het geheel flexibel wordt. De buigdiameter, de diameter waarnaar gebogen kan worden zonder dat het apparatuur stukgaat, is minimaal 6 mm. Een verbeterde substraat overdraagproces is onderzocht in Hoofdstuk 5. Door het apparatuur tussen twee 10-μm-dikke polyimide lagen te positioneren kan deze tot een buigdiameter van 3mm worden gebogen. Het apparatuur overleefde 140 buigcycli op 3mm. Theoretisch zou dit getal nog hoger kunnen liggen.

SiO_2 als de belangrijkste diëlektricum in de halfgeleiderindustrie, is ook onderzocht voor lage temperatuur formatie vanuit hetzelfde vloeibaar-siliciumoplossing. SiO_2 geproduceerd op 350C door middel van doctor-blade bekledlingsmethode en oxidatie van de incompleet-thermisch-getransformeerde a-Si in een zuurstof plasma. Zoals aangegeven in Hoofdstuk 6, is de atoomverhouding O/Si van de uiteindelijke oxide laag 1.66, en het instort-elektrisch veld was 1.1MV/cm. Behalve als diëlektricum, kan de silicium-rijke SiO_2 laag worden gekristalliseerd met de excimer laser om vervolgens nano-kristal Si stippen te creëren voor flashgeheugentoepassingen.

Dit proefschrift bespreekt vloeibaar-Si technologie voor hoge-snelheid circuits op flexibele substraten. Het werk richt zich op flexibele *single-grain* Si TFTs en lage temperatuur silicium oxide. Indien de eigenschappen van het apparatuur toepassingsdoeleinden behaalt kan toekomstig werk richten op

lagere temperatuur productie, nieuw substraat overdracht methodiek voor flexibelere apparatuur en nieuwe ontwerpen voor complexe digitale en analoge circuits.

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