RF Potential of a 0.18-μm CMOS Logic Device Technology

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***Abstract*—The radio-frequency (rf) performance of a 0.18-μm CMOS logic technology is assessed by evaluating the cutoff and maximum oscillation frequencies (f_T and f_{max}), the minimum noise figure (F_{min}) and associated power gain (G_a), and the $1/f$-noise of the devices. Gate-biasing and channel-length and gate-finger-length adjustments are identified as means to optimize the rf performance without any technology process modifications. Changing to N_2O gate dielectrics is shown to greatly reduce the $1/f$ noise without sacrificing the ac performance. The power amplifier characteristics of CMOS at low power levels are also discussed.**

***Index Terms*—CMOS FET's, CMOS power amplifiers, HF receivers, HF radio communication, HF transmitters, impedance matching, microwave devices, microwave FET's, microwave receivers, microwave transmitters, MOS devices, MOSFET's, semiconductor device breakdown, semiconductor device noise, semiconductor devices.**

I. Introduction

THE strongly emerging wireless communication market needs device technologies that are capable to produce high product volumes at extremely low cost. Those requirements are best met by complementary metal-oxide-semiconductor (CMOS) technology. The device physics and structure of CMOS is very similar to that of the metal-semiconductor field-effect transistor (MESFET), which has long been established as a preferred microwave device [1]. Consequently, substantial research is in progress today to investigate and optimize CMOS for rf applications. Many of those attempts invest in major modifications of the device structure in order to optimize the maximum oscillation frequency (f_{max}) and the minimum noise figure (F_{min}) of the transistor. That includes the formation of metal T-gate [2], [3] or polycide-gate structures, in order to minimize the gate resistance, and the use of silicon-on-insulator (SOI) [5]–[9], silicon-on-sapphire (SOS) [2], [3], high-resistivity silicon (HRS) [5], [6], [8], and device suspension [10] for reduced substrate losses. Other attempts stay more in line with the developments of CMOS logic in order to fully utilize the manufacturing environment of this well-established technology [11]–[19]. A good approach that has been taken by various companies is to first evaluate an existing CMOS logic process for its rf capability and then decide on the reasonable investments in order to improve the rf performance.

In this paper, we present a comprehensive evaluation of a 0.18 μm CMOS process [20] and demonstrate its excellent rf device characteristics. In addition to the CMOS transistors, this technology offers low-resistivity copper (Cu) metallization, which is benefical for the integration of spiral inductors and metal-insulator-metal (MIM) capacitors that are essential components of an rf technology [21].

In Section II, we describe the 0.18-μm CMOS logic technology. The RF characteristics will be presented and discussed in Section III, and some conclusions will be given in Section IV.

II. 0.18-μm CMOS Technology and Test Devices

A 0.18-μm CMOS logic technology has been demonstrated recently with n-MOS and p-MOS devices having channel lengths of 0.06 μm and 0.08 μm, respectively, and operating at a voltage of 1.5 V [20]. The fabrication process features a gate oxide of 3.6 nm, retrograde wells, and strong halos coupled with shallow junctions to suppress the short channel effects. The gate oxide has been implanted with nitrogen (N_2) in order to improve the device reliability; devices with an N_2O gate oxide (nitrided oxide) have been fabricated for comparisons. Excellent device behavior had been demonstrated for n-MOS and p-MOS devices down to channel lengths of 0.055 μm and 0.07 μm, respectively. The technology also features tungsten (W) local interconnects, followed by Cu interconnects at all wiring levels.

Test devices were fabricated with effective channel lengths (L_{eff}) of 0.08 μm, 0.096 μm, and 0.112 μm for n-MOS and 0.01 μm, 0.012 μm, and 0.014 μm for p-MOS. The channel width (W) was 63 μm in all cases, but the n-MOS transistors were built in versions with two, four, eight, or sixteen gate conductor fingers (m) in order to vary the gate-finger length and thus the gate resistance. The p-MOS devices were only available with four gate-conductor fingers ($m = 4$). For the $1/f$ noise measurements different transistors, which had $m = 1, W = 10\,\mu$m, and L_{eff} = 0.25 μm, were used.

Fig. 1 shows the I_g-V_{ds} and the I_d-V_{ds} characteristics of n-MOS and p-MOS transistors with effective gate lengths of 0.096 μm and 0.12 μm, respectively. It will be shown later that

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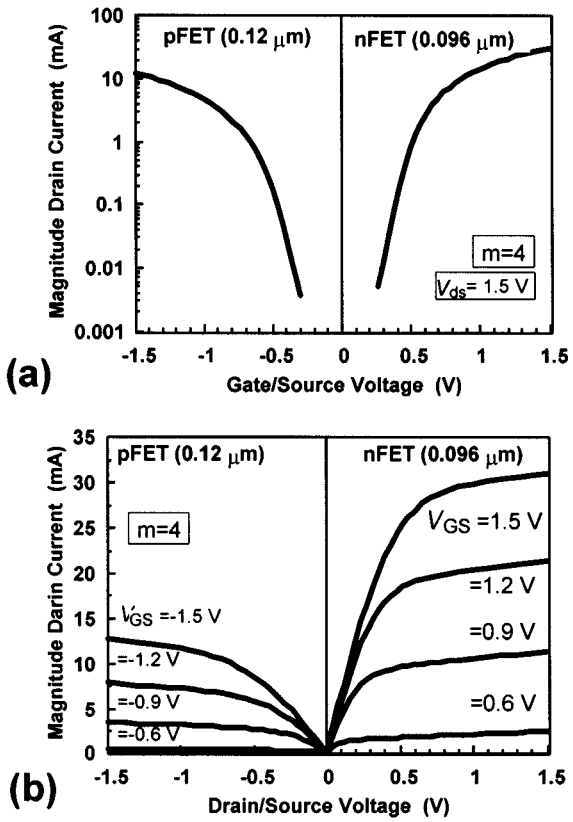

Fig. 1. (a) I_d-V_{gs} and (b) I_d-V_{ds} characteristics of a 0.096-μm n-MOS and a 0.12-μm p-MOS transistor.

those gate lengths, rather than the gate lengths for logic applications, provide an optimum set of rf figures-of-merit (FOM).

III. RF Characteristics

High-frequency measurements were carried out in order to determine the FOM's for rf applications, i.e., the frequency limits f_T (cut-off frequency) and $f_{\max}$, the $F_{\min}$, the $1/f$ noise level, and the power gain and power added efficiency (PAE) if operated as a power device at low power levels. The frequency limits were derived from S-parameter measurements using an HP8510 network analyzer with test frequencies up to 40 GHz. The parasitics associated with the probe pads were deimbedded. The noise figure and the associated gain were measured in an ATN NP5 noise measurement system without deimbedding the pad parasitics. The $1/f$ noise spectral power density was measured by using a home-built test system. Power gain and PAE were determined from tests with an ATN LP1 load-pull system.

Next, we discuss how the FOM's can vary with bias and device geometry, and how one can arrive at an optimum configuration for rf applications.

A. Bias Dependencies

The first obvious parameters that can easily be adjusted are the gate/source (V_{gs}) and drain/source (V_{ds}) voltages. Generally, it is desirable to search for conditions at which the lowest value of $F_{\min}$ can be provided with a maximum associated power gain (G_a). The operating point should also be near the peak values of f_T and $f_{\max}$. For power amplifier optimization one looks for a maximum PAE at the highest possible output power. Fig. 2 shows the dependencies of the transconductance (g_m), the output conductance (g_{ds}), the f_T, and the $f_{\max}$ for n-MOS and p-MOS as a function of V_{gs}, and thus the drain current (I_d), with a constant $|V_{ds}| = 1.5$ V. The transconductance develops a distinct maximum at a certain bias. The reduced g_m at low bias is a result of the large thickness of the channel near weak inversion condition [22], while mobility degradation can lower g_m at high fields [23]. In the discussed 0.18-μm CMOS technology the mobility degradation was obviously more pronounced for the n-MOS [Fig. 2(a)] as for p-MOS [Fig. 2(b)] within the bias boundaries. The f_T shows a similarly strong bias dependence since it relates to g_m as

$$f_T = \frac{g_m}{2\pi C_{GS}}. \tag{1}$$

The $f_{\max}$ has a weaker bias dependence than the f_T because it relates to f_T as

$$f_{\max} = \frac{f_T}{2\sqrt{(g_{ds}(R_G + R_S) + 2\pi f_T R_G C_{GD}}} \quad [14] \tag{2}$$

with the gate resistance (R_G), the source contact resistance (R_S), and the gate/drain capacitance (C_{GD}). It is first obvious from (2) that R_G appears in both terms of the denominator, indicating the importance of this parameter, as we will illustrate in Section III-B. If the second term of the denominator is much larger than the first one, $f_{\max}$ is proportional only to $\sqrt{f_T}$, diminishing somewhat the strong bias dependence of f_T and g_m. The first term of the denominator can be large if g_{ds} increases strongly, such as for the p-MOS at high bias [Fig. 2(b)]. Then, $f_{\max}$ can decay at a bias where the f_T is not yet reduced, as Fig. 2(b) shows.

Other FOM's, that have a distinct bias dependence, are the $F_{\min}$ and the G_a, as shown in Fig. 3. The lowest values of $F_{\min}$ are quite similar for n-MOS and p-MOS, which is an indication that $F_{\min}$ is limited to a large extent by the resistances of the silicided drain/source and gate regions. This is due to the fact that the silicidation makes the resistances of those regions very similar for p-MOS and n-MOS. Minima appear at different drain currents, due to the difference in majority carrier mobility. G_a, however, was higher for the n-MOS, as expected from the comparably higher $f_{\max}$ (Fig. 2). Using $F_{\min}$ as the premier FOM, the optimum bias was found at about $|V_{gs}| = 1$ V (Figs. 2 and 3). From Fig. 2 it becomes obvious that this bias condition coincides with the maxima of g_m, f_T, and $f_{\max}$ for the n-MOS, while for the p-MOS it was found somewhat below those maxima. The fact, that the optima of all FOM's cluster near about the same bias point for the n-MOS is an additional advantage of this device for rf application, besides the higher maximum values of g_m, f_T, $f_{\max}$, and G_a compared to the p-MOS.

In addition to the dependence of the FOM's on V_{gs}, we have also investigated the impact of a variation of V_{ds} at a fixed V_{gs}. Similarly to the findings in [15], we observed that this bias dependence was comparably small. A discussion of this effect was therefore not included in the paper.

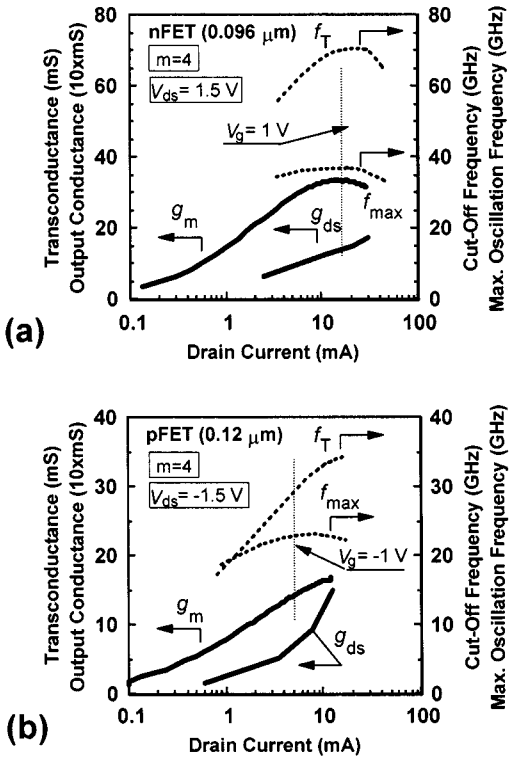

Fig. 2. Bias dependence of cut-off frequency, maximum oscillation frequency, transconductance, and output conductance of a 0.096-μm n-MOS and a 0.12-μm p-MOS transistor.

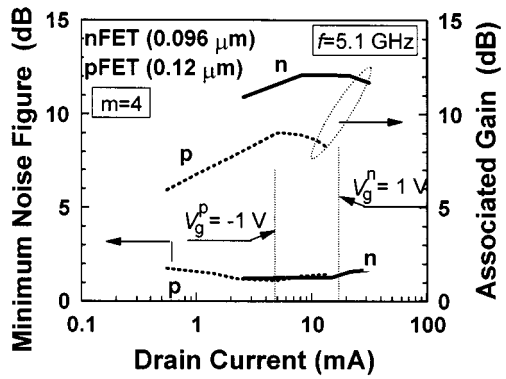

Fig. 3. Bias dependence of the minimum noise figure and the associated gain of a 0.096-μm n-MOS and a 0.12-μm p-MOS transistor.

B. Effect of Gate Resistance

The significance of the gate resistance on the most important FOM's, $F_{\min}$ and $f_{\max}$, has already been addressed in Section III-A and is extensively discussed and demonstrated in [14]. The effect of RG on $F_{\min}$ is obvious from Fukui's approximation [24], which is

$$F_{\min} = 1 + K\frac{f}{f_T}\sqrt{(g_m(R_G + R_S))} \tag{3}$$

with K being a fitting factor. A small gate resistance therefore leads to both an increased $f_{\max}$ and a reduced $F_{\min}$. To investigate the effect of R_G experimentally we have fabricated n-FET's with the same total widths but different numbers of gate fingers. This resulted in a variation of the gate finger length from $L_f = 3.95$ μm for $m = 16$ up to L_f =31.5 μm for m =

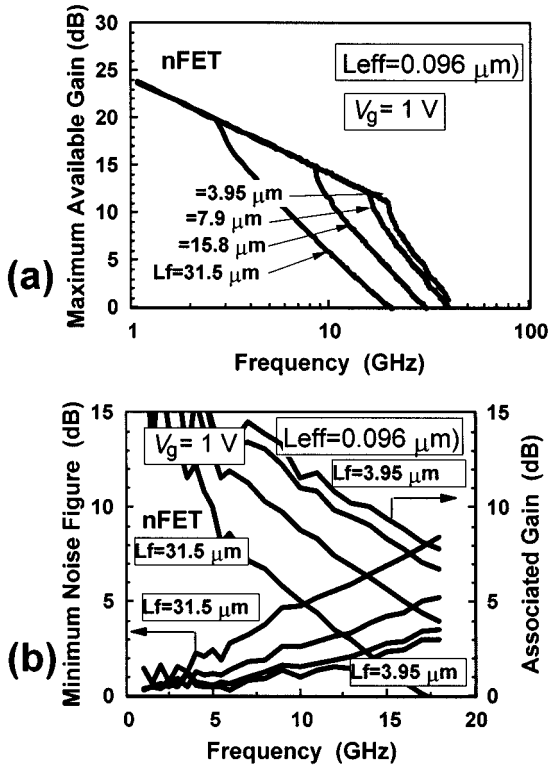

Fig. 4. Frequency dependence of (a) the maximum available gain and (b) the minimum noise figure and the associated gain of n-FET's with a total channel width of 63 μm and gate finger length ranging from 3.95 μm to 31.5 μm.

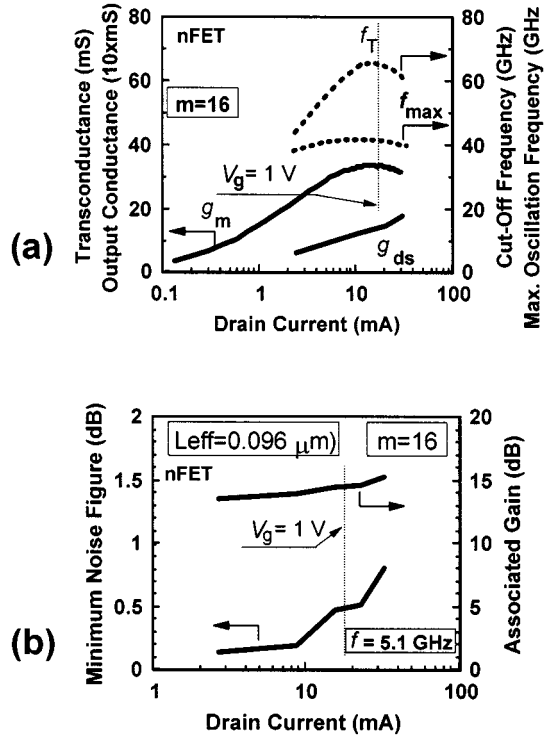

Fig. 5. Bias dependence of (a) the transconductance, the output conductance, the cut-off frequency, and the maximum oscillation frequency and (b) the minimum noise figure and the associated gain at 5.1 GHz of an n-FET with 16 gate fingers of 3.95 μm length and an effective channel length of 0.096 μm.

2. The maximum available gain $(G_{\max})$ was calculated from S-parameter measurements up to 40 GHz in order to determine

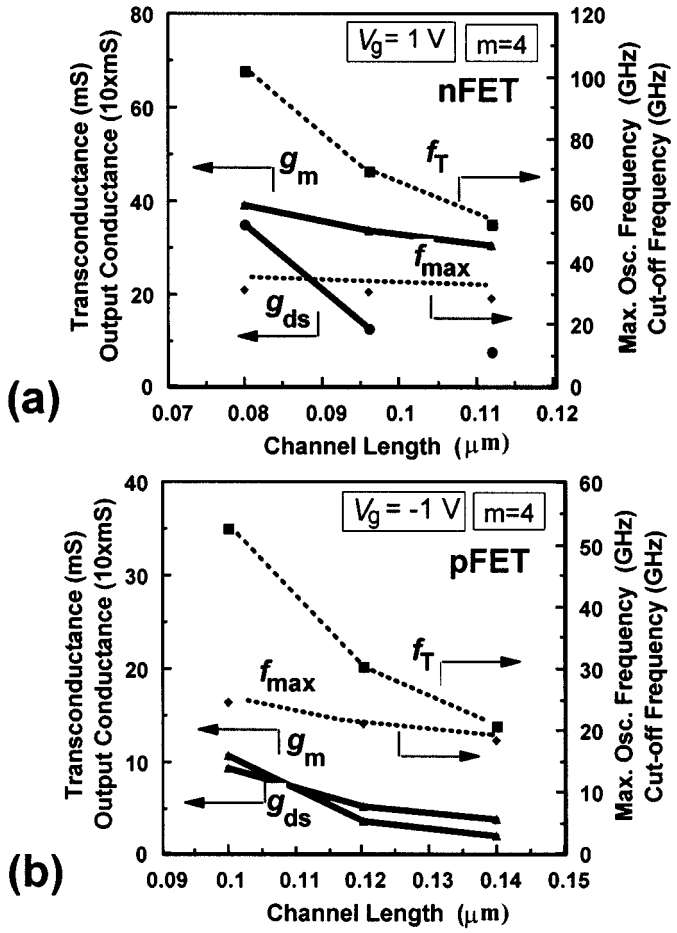

Fig. 6. Channel length dependence of the transconductance, the output conductance, the cut-off frequency, and the maximum oscillation frequency of an n-FET and a p-FET with four gate fingers of 7.9 μm length at a gate bias of $\pm$1 V.

$f_{\max}$ [Fig. 4(a)]. It is obvious that $f_{\max}$ improves steadily from a value of about 22 GHz at $m = 2$ to about 43 GHz at m = 16.

The unilateral gain (U) *versus* frequency was also determined, showing the same trend and very similar frequency limits (f_U) to those of the maximum available gain. The f_U is often used in place of $f_{\max}$ to characterize a microwave transistor if the test frequency is much smaller than the frequency limits so that one has to rely on extrapolation. Here, with measurement frequencies up to 40 GHz and $f_{\max}$ and f_U below 45 GHz, we believe that all frequency limits were determined with a very good accuracy. Differences in the f_T's due to the variation in the number of gate fingers were not noticeable, as expected.

As shown in Fig. 4(a), the degree of improvement of $f_{\max}$ decreases as the number of gate fingers approaches $m = 16$, showing that for this device structure the impact of R_G is quite small. The result also demonstrates that a reduction of R_G to a negligible level is possible through a proper device layout and does not necessarily require sophistigated T-gate structures [2]–[4]. Fig. 4(b) shows that a similar observation can be made for $F_{\min}$ and G_a. It is obvious that a ratio $G_a/F_{\min}$ of 10 dB can be maintained at frequencies $>$ 10 GHz with $L_f = 3.95$ μm $(m = 16)$.

The bias dependence of an n-FET with $m = 16$ is illustrated in Fig. 5. In comparison to the nFET with $m = 4$, $F_{\min}$ is reduced from about 1.5 dB to 0.5 dB and G_a is increased from about 12 dB to 15 dB at 5.1 GHz. The $f_{\max}$ is increased from 32 GHz to 43 GHz. The results in Fig. 5, in contrast to those in Figs. 2 and 3, suggest that V_{gs} =1 V does not present the optimum bias for this improved layout $(m = 16)$; a bias near V_{gs} =0.8 V with $I_d \simeq 10$ mA would provide $F_{\min} \simeq 0.2$ dB at 5.1 GHz and still be near the highest values of $f_{\max}$ and f_T.

C. Dependence on Channel Length

The effect of the channel length on the FOM's has been investigated by fabricating n-FET's and p-FET's $(m$ = 4) with three different channel lengths (Figs. 6 and 7). As expected, the g_m and the f_T improve toward smaller channel length, while the g_{ds} increases and thus worsens. The $f_{\max}$ of the n-FET was found to be fairly independent of channel length, but for the p-FET it increased noticeably due to the limited f_T, which was almost as low as $f_{\max}$ for the longest channel [Fig. 6(b)]. Similar observations were made for the minimum noise figure and the associated gain (Fig. 7). The n-FET had a softly marked optimum near 0.1 μm channel length [Fig. 7(a)]. The p-FET, since suffering from a relatively low f_T at all channel lengths, had the lowest $F_{\min}$ and the highest G_a for the narrowest channel [Fig. 7(b)]. Since for the n-FET $F_{\min}$ had an optimum near L_{eff} = 0.1 μm (Fig. 7(a)) and $f_{\max}$ did not show a pronounced dependence on channel length [Fig. 6(a)] we consider the n-FET layout with $m = 16$ and L_{eff}= 0.1 μm the optimum device geometry for the given CMOS technology.

D. Impact of Gate Oxide Quality

Besides the high-frequency FOM's, discussed so far, the $1/f$ noise is of importance since, e.g., it affects the phase noise of a voltage-controlled oscillator (VCO) and can appear in the output spectrum of a mixer. The $1/f$ noise level depends mainly on the conditions near the oxide-silicon interface, and therefore on interface states, oxide traps, and border traps [25]. The quality of the gate-oxide is consequenctly of premier importance. In the deep-submicrometer regime the conventional thermal gate oxide has to be replaced by a nitrided oxide in order to provide sufficient device reliability and to prevent boron penetration through the gate dielectric of the p-MOS [26]. Nitridation of the gate oxide can be achieved *in situ* by depositing N_2O or by implanting nitrogen into a thermally-grown gate oxide. The latter approach has the advantage that the thickness of the gate dielectric can be as well controlled as that of a thermal oxide, but the nitrogen implantation may result in a higher interface-state density.

We have investigated the $1/f$ noise in n-MOS and p-MOS devices which were identical to the high-frequency test transistors, except for the different gate dielectrics. The main test transistors had longer channels compared to the devices discussed earlier to reduce potential perimeter effects. But in fact, the comparison of transistors with different channel lengths has shown that edge effects are small as far as the $1/f$ noise is concerned. The first set of n-MOS and p-MOS devices had N_2O gate dielectrics, while the second and third sets of devices had nitrogen-implanted gate

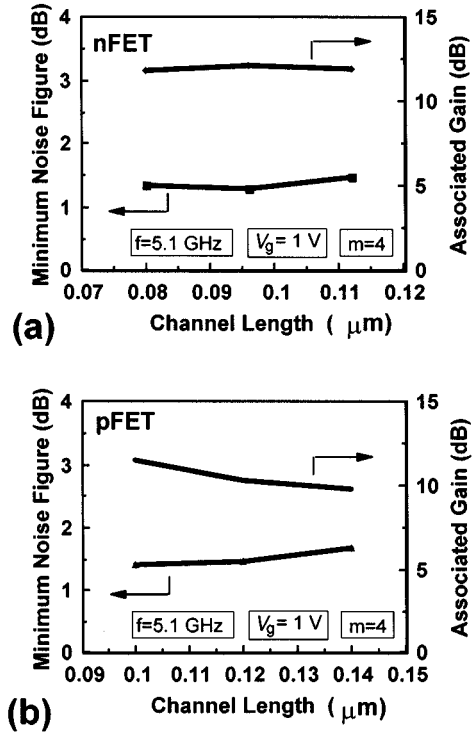

Fig. 7. Channel length dependence of the minimum noise figure and the associated gain at 5.1 GHz for an n-FET and a p-FET with four gate fingers of 7.9 μm length at a gate bias of ± 1 V.

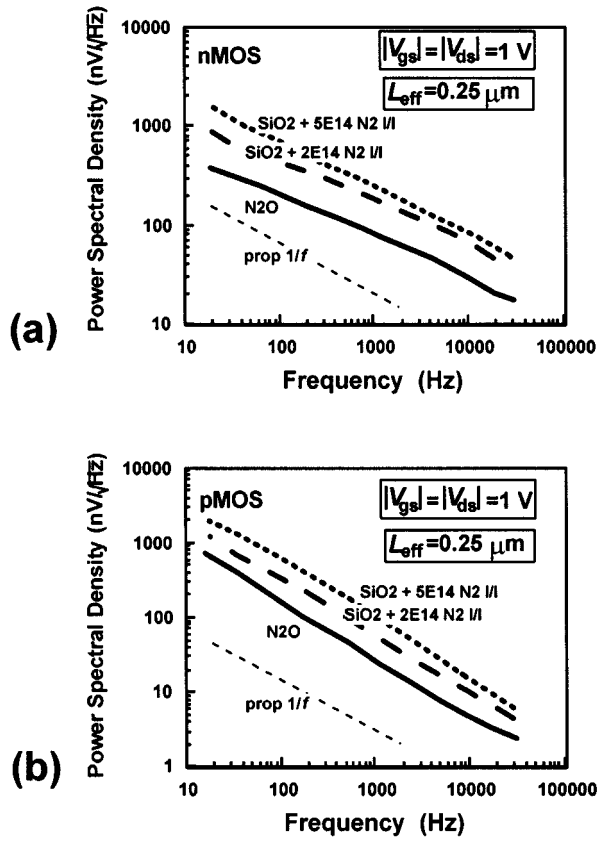

Fig. 8. Noise power spectra of (a) an n-FET and (b) a p-FET with one gate finger of 10 μm length at a gate and drain bias of ± 1 V for different types of gate oxides.

oxides with implantation doses of 2×10^{14} cm^{-2} and 5×10^{14} cm^{-2}, respectively. The measurement results showed that the $1/f$ noise level was higher for the implanted oxides and was increased with higher implantation dose for both n-MOS and p-MOS (Fig. 8).

Besides the $1/f$ noise, the ac characteristics of the test transistors were measured as well to evaluate any effect of the differences in gate dielectric quality and thickness on the device speed. The transconductances were found to be very similar, indicating that the channel lengths and thicknesses of gate dielectrics were nearly identical (Fig. 9). The cut-off frequency of the implanted-oxide devices was slightly higher than that of the N_2O-oxide transistors, but the difference was not larger than the estimated error associated with the S-parameter extraction method ($\approx 10\%$). The important result from the $1/f$ noise evaluations was therefore that the *in situ* nitridation of the gate oxide can lead to a significant reduction of the low-frequency noise behavior of MOSFET's without any significant degradation of the device speed. *In situ* nitrided gate dielectrics seem therefore to be prefereable for rf applications.

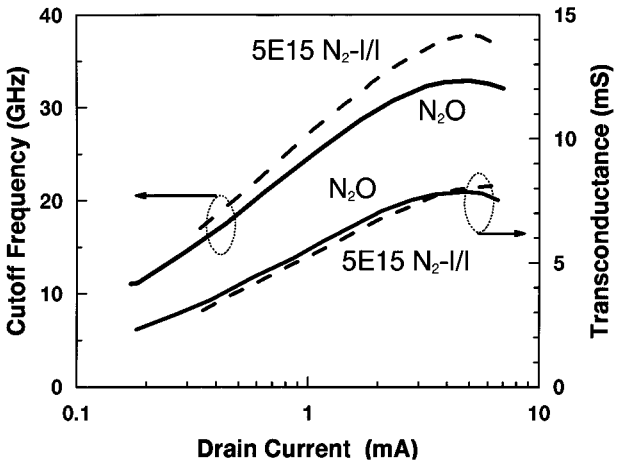

Fig. 9. Cutoff-frequency and transconductance versus the drain current of n-MOS transistors with different gate dielectrics but otherwise identical features.

E. Power Transistor Performance

For power amplifier optimization, a maximum PAE, including the output impedance matching section, at the highest possible output power is desirable. (Losses in the matching section lead to a reduced PAE, particularly if the impedance mismatch between the transistor and the antenna switch is significant.) In this work, we have investigated only the intrinsic power-amplifier performance using on-chip load-pull measurements (ATN LP1) on a comparably small transistor with an output power close to 10 mW in the range of 900 MHz to 2.4 GHz (Fig. 10). The transistor was operated at the maximum supply voltage of 1.5 V, the output matching was optimized for PAE rather than output power, and the input matching was optimized near the 3-dB output power compression point. For this low-power transistor the amplifier characteristics were excellent, as shown by a power gain of 23 dB and a maximum PAE of near 65% at 900 MHz. Those values were somewhat degraded to 19 dB and 57% at 2.4 GHz, as expected. The

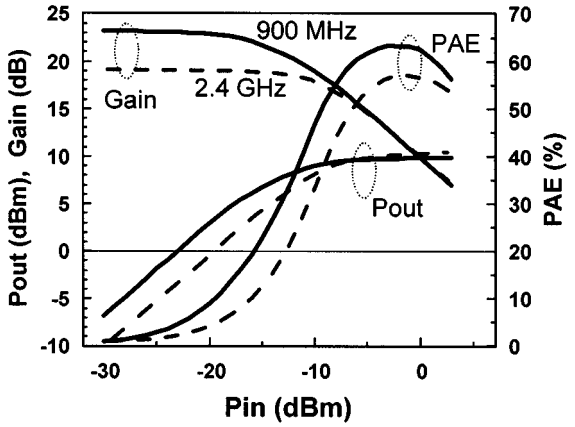

Fig. 10. Output power, power gain, and power-added-efficiency (PAE) of an n-FET with 16 gate fingers of 3.95 μm length at a gate and drain bias of 1.5 V at 900 MHz and 2.4 GHz.

PAE-maximum was shifted somewhat beyond the fall-off of the power gain due to the input matching conditions and the output matching for maximum PAE. It seems obvious to achieve higher power levels by forming arrays of such power-transistor cells with the appropriate size. But one has to consider that the performance levels discussed here only apply to the internal device. Therefore, with the lower output impedance of the larger power transistor arrays the impedance mismatch between amplifier output and antenna is higher, leading to a comparably bigger loss in the impedance matching section and thus a reduced total PAE. The PAE is further reduced in large arrays by the comparably higher losses in the interconnects [27]. As a result, power amplifiers based on scaled CMOS, as used for logic applications, may only perform sufficiently well as power transistors at very low power levels and in rf micro-cell applications [28]. MOS devices, that are not scaled and specifically designed for rf power applications, however, have been demonstrated with good rf power characteristics up to 1.9 Ghz [29].

IV. Conclusions

This paper has shown that a CMOS technology designed for logic applications can exhibit very respectful rf device characteristics. The highlights of the 0.18 μm CMOS technology discussed here are a cutoff-frequency of 68 GHz, a maximum oscillation frequency of 42 GHz, and a minimum noise figure of < 0.5 dB at 5.1 GHz with 15 dB associated gain. It was found that the $1/f$-noise could be improved by using an *in situ* nitrided gate dielectric film in place of using nitrogen implantation without sacrificing significantly the transconductance and the cutoff-frequency. For a small, 10-mW power transistor an internal power gain of about 20 dB and an internal PAE of close to 60% were measured for frequencies up to 2.4 GHz. At higher power levels, however, a reduced PAE is expected as a result of the strong impedance mismatch, and thus the high losses in the impedance matching network, due to the low output impedance of the device. Overall, scaled CMOS technology seems to be well suited with, however, the restriction to low transmission power levels.

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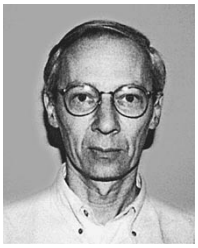

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