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Enhanced Thermal Management of a 1.2 kV SiC MOSFET Half-bridge Fan-out Panel-Level Packaging with Nanocopper Sintering Die-attachment

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***Abstract*—Sintered nano-copper (Cu) improves the thermal performance of SiC MOSFET Fan-Out Panel-Level Packaging (FOPLP), a widely adopted method for miniaturizing electronic systems and modules. This study presented, for the first time, the prototyping and characterization of a 1.2 kV SiC MOSFET FOPLP half-bridge power module using sintered nano-Cu die attachment (FOPLP_Cu), and compared it with a reference module using conductive Ag adhesive interconnects (FOPLP_Ag). Thermal, mechanical, and electrical co-simulations proved that FOPLP_Cu exhibited superior performances with lower thermal resistance, power loop parasitic inductance, and thermal deformation, achieving values of 0.14 ºC/W (with double-sided cooling), 3.15 nH (@100 kHz), and 9.05e-5 m, respectively. In contrast, FOPLP_Ag showed higher values of 0.24 °C/W, 3.27 nH, and 1.04e-4 m. It is worth noting that due to the higher elastic modulus of sintered nano Cu, FOPLP_Cu experienced increased thermal stress. The internal structure analysis of the packaged devices, conducted using CSAM, showed that both FOPLP_Cu and FOPLP_Ag had well-formed interconnections, with no signs of delamination in the EMC, RDL, or interconnect layers. Thermal testing showed that FOPLP_Cu achieved a single-side thermal resistance of 1.95 ºC/W, representing a 22% improvement compared to FOPLP_Ag's 2.5 ºC/W. Electrical testing further demonstrated that FOPLP_Cu had lower on-state resistance compared to FOPLP_Ag, while maintaining comparable breakdown voltage, threshold voltage, and body diode forward voltage drop.**

***Index Terms*—Fan-out panel-level packaging (FOPLP), Sintering nano Cu, parasitic inductance, SiC MOSFET, thermal resistance.**

I. INTRODUCTION

SiC MOSFETs offer a range of significant advantages, such as high conversion efficiency, low energy loss, fast switching speed, and the ability to function at elevated junction temperatures [1-4]. These characteristics make them highly suitable for applications in electric vehicle (EV) inverters and onboard chargers (OBCs) [5-7]. The inverter's role is to convert direct current (DC) from the high-voltage battery into alternating current (AC) to power the electric motor, while the OBC converts AC from external chargers into DC to recharge the battery. In EV systems, the efficiency, reliability, and compact form factor of SiC MOSFETs are critical, making them indispensable for the effective design of core components.

In space-limited automotive applications, high power density and miniaturized power converters can save space and extend the driving range of EVs. SiC MOSFETs with FOPLP packaging provide a compact design with reduced parasitic elements and improved reliability, offering superior performance compared to traditional TO discrete packages and stacked power module designs. In FOPLP packaging, the SiC chip is embedded in a PCB-like substrate, and a redistribution layer (RDL) routes the SiC MOSFET's functions to the package terminals. This design significantly reduces inductance and shrinks the overall size. Several companies (REAL IZM, Infineon, Schweizer, Magna and so on) and research institutions (Virginia Tech, Université Grenoble Alpes, Zhejiang University, etc.) have conducted pioneering research on SiC MOSFET FOPLP, covering single-chip discrete devices, multi-chip phase-leg modules, and inverter systems[8-11].

Sintered Cu die attachment greatly enhances the electrical, thermal, and mechanical performance of FOPLP, but no successful integration has been reported to date. This paper first designed and validated an FOPLP half-bridge with sintered Cu die attachment through simulations, then developed the packaging process and experimentally

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verified its functionality. The paper is structured as follows: Section II introduces the SiC MOSFET FOPLP half-bridge concept and packaging processes; Section III presents the simulation study of the FOPLP with sintered Cu die attachment; Section IV experimentally validates the packaging's functionality; and Section V provides the conclusions.

II. SiC MOSFET Fanout Panel Level Packaging

This section introduced the concept of FOPLP and examines the feasibility of integrating sintered Cu into the SiC MOSFET FOPLP half-bridge.

B. Fanout Panel Level Packaging Structure

FOPLP technology exhibits remarkable advantages in the packaging of SiC MOSFETs. Its miniaturized (ultra-thin) design makes it compatible with high power density applications. The high level of integration facilitates the consolidation of multiple functional modules, streamlining the design and improving system performance. Additionally, the adoption of RDLs in place of traditional wire bonds reduces inductance and minimizes switching losses, making it especially appropriate for high-frequency applications. Moreover, in large-scale production, the high efficiency and yield of FOPLP significantly reduce manufacturing costs, positioning it as an ideal choice for the miniaturization of SiC MOSFET packages. This paper aims to enhance the thermal performance and reliability of FOPLP through the introduction of sintered Cu die attachment.

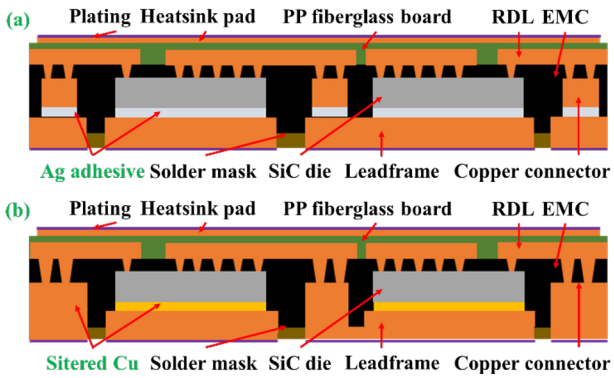

Fig. 1 Structural schematic of the SiC MOSFET half-bridge module with FOPLP packaging: (a) Ag adhesive interconnector; (b) Sintered Cu interconnector.

Efficient thermal management is essential for the proper functioning of high-power half-bridge packages. Key characteristics of high-quality packaging include parasitic parameters, electrical properties, robustness, and mechanical performance. This study presented a novel FOPLP technology for SiC MOSFET half-bridge power modules. To improve thermal performance, a nano Cu sintering die attachment was introduced into the FOPLP process, designated as FOPLP_Cu. A sample of FOPLP using silver (Ag) conductive adhesive served as a reference, labeled FOPLP_Ag. FOPLP_Ag, illustrated in Fig. 1 (a), comprised several key components: leadframe, Ag adhesive, SiC dies, Cu connector, EMC, Polypropylene (PP) fiberglass board, RDL, and heatsink pad. In contrast, FOPLP_Cu featured a sunken half-hollow leadframe, with the SiC dies connected to the leadframe's cavities via sintered Cu, as shown in Fig. 1 (b). The surface height of the dies closely matched that of the leadframe, eliminating the need for a Cu connector, which aids in flux cancellation for achieving lower stray inductance.

B. Packaging Structure process fo FOPLP

The SiC MOSFET die (S1M040120B) from SICHAIN Semiconductor, rated at 1200 V, 80 A, and 40 mOhm, was utilized for the research. The die dimensions were 4.134 × 3.74 × 0.2 mm^3. The surface metallization of the gate and source pads comprised Ni/Pd/Au, whereas the drain's surface metallization included Ti/Ni/Ag. A panel measuring 508mm × 203 mm^2 was used as the substrate.

For FOPLP_Ag, conductive Ag adhesive (WON128-T) from CORE-CHEMI was used to bond the die and Cu connector. The adhesive was cured in a nitrogen furnace (RDS Magazine Dryer, rehm-group) at 175°C for 60 minutes. Fig. 2 (a) shows the panel (substrate) with grooves outside the die and Cu connector soldering areas to prevent adhesive overflow and die displacement. Fig. 2 (b) displays the result after die attachment.

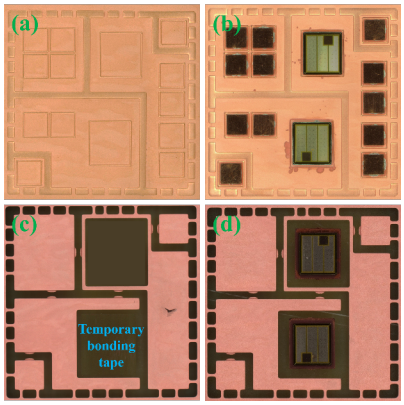

Fig. 2 The Cu substrate of a single half-bridge package unit:(a) and (b) FOPLP_Ag before and after die attachment; (c) and (d) FOPLP_Cu before and after die attachment;

For FOPLP_Cu, a hollow panel was used, as shown in Fig 2. (c). Before die attachment, temporary bonding tape was applied to the bottom surface of the hollow panel. A sandwich structure, consisting of the SiC die, sintered layer, and a 0.1 mm Cu plate, was placed in the hollow of the panel, with the temporary bonding tape providing support.

The sintering process of the sandwich structure involves the following steps: (1) The SiC die and Cu plate were prepared, with the Cu plate cleaned for 300 seconds at 200°C in a formic acid environment; (2) Nano Cu paste was screen-printed onto the copper plate; (3) The paste was dried for 300 seconds at 120°C in a nitrogen atmosphere to remove organic materials; (4) The SiC die was placed on the dried nano Cu layer with 50 N of force applied; (5) The structure was sintered for 20 minutes at 20 MPa and 250°C in a pressure-assisted sintering furnace (Sinterstar Innovate-F-XL, Boschman). Fig. 2 (d) shows the sandwich structure mounted on the hollow panel.

III. Thermal, Mechanical and Electromagnetics Simulations and Analyses

This section assessed the impact of die attachment and the package substrate on the performance of FOPLP using finite element (FE) simulations. This section performed thermal resistance testing to validate the package's heat dissipation, followed by a thermo-mechanical virtual prototyping analysis of its mechanical behavior, conducted using Ansys Workbench 2021r1. Finally, the parasitic inductance of the SiC MOSFET FOPLP was extracted using Ansys Q3D 2021, and the impact of switching frequency on it was examined.

The study commenced with the development of three-dimensional models for FOPLP_Ag and FOPLP_Cu. As shown in Fig. 3, both FOPLP_Ag and FOPLP_Cu demonstrated similar internal structures and shared identical package outline drawings (POD). Apart from the die attachment materials, both structures utilized the same packaging materials, with the heatsink pad, RDL, connector, and leadframe constructed from Cu. The material parameters, including density, thermal conductivity (K), coefficient of thermal expansion (CTE), Young's modulus (E), and Poisson's ratio (v), are detailed in TABLE 3 and were utilized in the thermal and mechanical simulations.

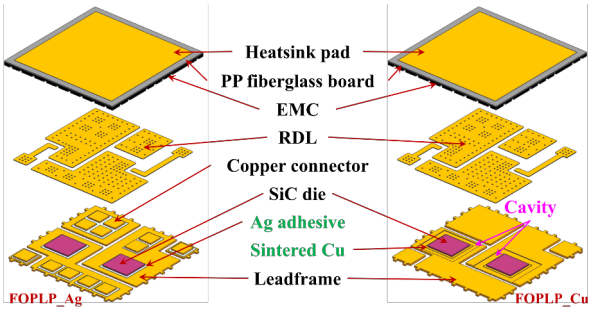

Fig. 3 The three-dimensional exploded views of FOPLP_Ag and FOPLP_Cu structures.

A. Thermal analysis

Effective heat dissipation is crucial for the long-term reliability of packaging, and thermal management constitutes a significant portion of the total system cost. For high power density and miniaturized SiC FOPLP packages, designing for heat dissipation presents a necessary challenge. Steady-state thermal simulations were performed for both FOPLP_Ag and FOPLP_Cu, with thermal power set at 58.5 W(V_{GS}=15 V, I_D=40 A, V_{DS}=1.46 V) and an ambient temperature of 25°C. Both heatsink and solder pads act as heat dissipation surfaces, each subjected to a fixed temperature constraint of 25 °C. The ambient temperature is set at 25 °C. Both the heatsink pad and solder pad can function as heat dissipation surfaces, allowing for potential double-side cooling. A fixed temperature constraint of 25°C will be applied to the heat dissipation surfaces. The material parameters employed in the thermal simulation are presented in TABLE 1. Fig. 4 illustrates the simulated temperature distributions of SiC dies in both FOPLP_Ag and FOPLP_Cu under various cooling conditions. Considering the simulated results, the thermal resistance (R) can be calculated using the following equation:

$$R = \left(T_{junction} - T_{ambient}\right) / P_{th} \quad (1),$$

where $T_{junction}$ represents the maximum simulated temperature of the die, $T_{ambient}$ denotes the ambient temperature, and P_{th} indicates the internal heat power.

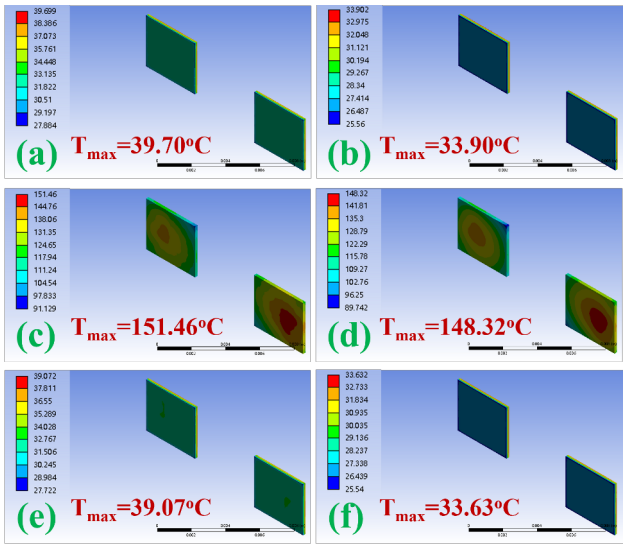

Fig. 4. The simulated temperature distribution results in the SiC dies:(a) FOPLP_Ag using the heatsink pad for cooling; (b) FOPLP_Ag using the solder pad for cooling; (c) FOPLP_Ag with double-side cooling; (d) FOPLP_Cu using the heatsink pad for cooling; (e) FOPLP_Cu using the solder pad for cooling; (f) FOPLP_Cu with double-side cooling.

The thermal resistance of FOPLP_Ag and FOPLP_Cu under different cooling conditions is shown in TABLE 2. As illustrated in Fig. 4 and TABLE 2, the heat dissipation performance was insufficient when only the heatsink pad was used. This is due to the poorly conductive PP material,

which has a thermal conductivity of approximately 1.2 W/m·ºC, positioned between the heatsink pad and both the die and the RDL. For both FOPLP_Ag and FOPLP_Cu, the improvement achieved with double-side cooling, compared to using the solder pad, was modest, around 5%. The thermal resistance for double-side cooling was 0.24 ℃/W for FOPLP_Ag and 0.14℃/W for FOPLP_Cu. The sintered Cu in FOPLP_Cu showed better thermal conductivity than the silver adhesive. In addition, the Cu connector in FOPLP_Cu was equipped with an Ag adhesive connection, which further increased thermal resistance.

TABLE 1
THERMAL-MECHANICAL PARAMETERS OF DIFFERENT MATERIALS

Materials	Density (g/cm^3)	K (W/m·°C)	CTE (ppm/ºC)	E (GPa)	ν
Cu	8.9	401	18	110	0.34
SiC	3.2	130	5.1	400	0.14
Sintered Cu	8.0	256.46	17.5	95	0.30
Ag adhesive	5.4	20	54	49	0.36
EMC	1	1.5	9	15	0.38
PP	1	1.2	56	4	0.3

TABLE 2
DEFINITIONS AND VALUES OF THERMAL RESISTANCE

Package type	symbol	Definition	Value (°C/W)
FOPLP_Ag	R_{JH}	From junction to heatsink pad	2.16
	R_{JS}	From junction to solder pad	0.25
	R_{JD}	From junction to case with double-side dissipation	0.24
FOPLP_Cu	R_{JH}	From junction to heatsink pad	2.10
	R_{JS}	From junction to solder pad	0.15
	R_{JD}	From junction to case with double-side dissipation	0.14

B. Thermal-mechanical analysis

The heat produced by SiC MOSFETs during operation induces a rise in their temperature. This increase, coupled with uneven temperature distribution, creates substantial stress within the package, particularly at interfaces between materials with different CTE. Accumulated stress can result in interface delamination and crack formation. This part discussed thermal-mechanical simulations of FOPLP_Ag and FOPLP_Cu under double-side cooling conditions. The simulations used the package's temperature distribution, shown in Fig. 4, as input and applied remote displacement constraints with fixed displacement and rotation set to zero. The material parameters are provided in TABLE 1. The simulation results are shown in Fig. 5. FOPLP_Ag reached a maximum stress of 37.9 MPa with a deformation of 1.4E-6 m, while FOPLP_Cu showed a lower maximum stress of 25.6 MPa and deformation of 8.3E-7 m, benefiting from its lower operating temperature compared to FOPLP_Ag. The maximum stress and deformation for both FOPLP_Ag and FOPLP_Cu occured at the die surface and the corners of the package, respectively.

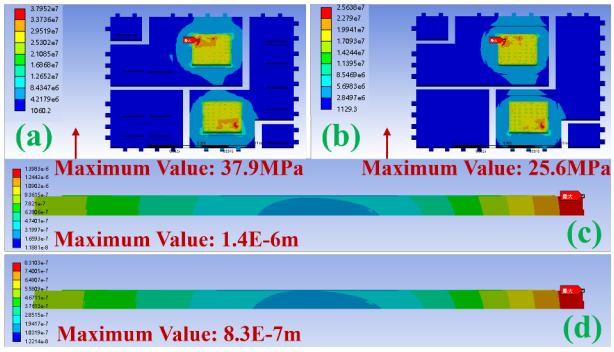

Fig. 5 Static thermo-mechanical simulation results caused by dies heating: (a) stress for FOPLP_Ag; (b) stress for FOPLP_Cu; (c) deformation for FOPLP_Ag; (d) deformation for FOPLP_Cu.

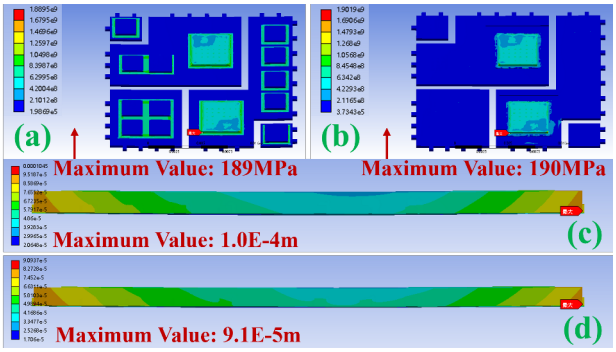

Fig. 6 Static thermo-mechanical simulation results caused by changes in environmental temperature: (a) stress for FOPLP_Ag; (b) stress for FOPLP_Cu; (c) deformation for FOPLP_Ag; (d) deformation for FOPLP_Cu.

When external environmental temperatures change, such as during thermal cycling/shock tests and reflow soldering, stress and deformation occur within the package. Simulations were conducted based on the reflow soldering temperature curve, as the environmental temperature rose from 25°C to 320°C. Using remote displacement constraints with fixed displacement and rotation at zero, the results, shown in Fig. 6, indicate that FOPLP_Ag experienced a maximum stress of 189 MPa and deformation of 1.0E-4 m, while FOPLP_Cu recorded 190 MPa and 9.1E-5 m. In the FOPLP structure, the die's solder pad side, which contains more Cu, resulted in an imbalance compared to the heatsink pad side, leading to a "smile face" deformation with temperature increases. FOPLP_Cu underwent less deformation due to its sunken half-hollow leadframe, which reduces the Cu volume on the solder pad side. The

maximum stress for both FOPLP_Ag and FOPLP_Cu occured at the corner in die's lower surface, with FOPLP_Cu showing slightly higher stress due to the higher E value of the sintered Cu.

C. Extraction of Parasitic Inductance

Parasitic inductance, an inherent characteristic of conductors, is influenced by material and structural design. It significantly limits the switching speeds of SiC MOSFETs, with higher parasitic inductance increasing switching losses. The parasitic inductance of the power loop and partial parasitic inductance of the SiC FOPLP half-bridge were extracted through simulation. The bulk conductivity of Cu and sintered Cu is set at 5.8E7 S/m, and Ag adhesive at 7E6 S/m. The relative permittivity of SiC is set at 10. The sweep frequency ranges from 0 to 1000 kHz. The power loop path from the drain of the high-side SiC MOSFET to the source of the low-side SiC MOSFET is illustrated in Fig. 7.

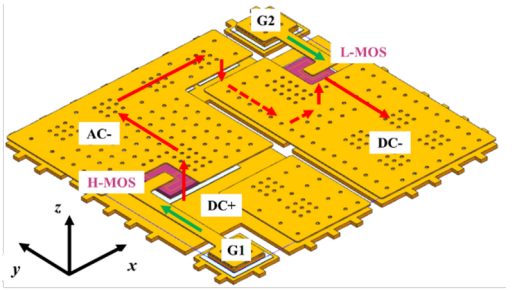

Fig. 7 The layout design of the redistribution layer and its current path in a SiC MOSFET half-bridge module with FOPLP packaging.

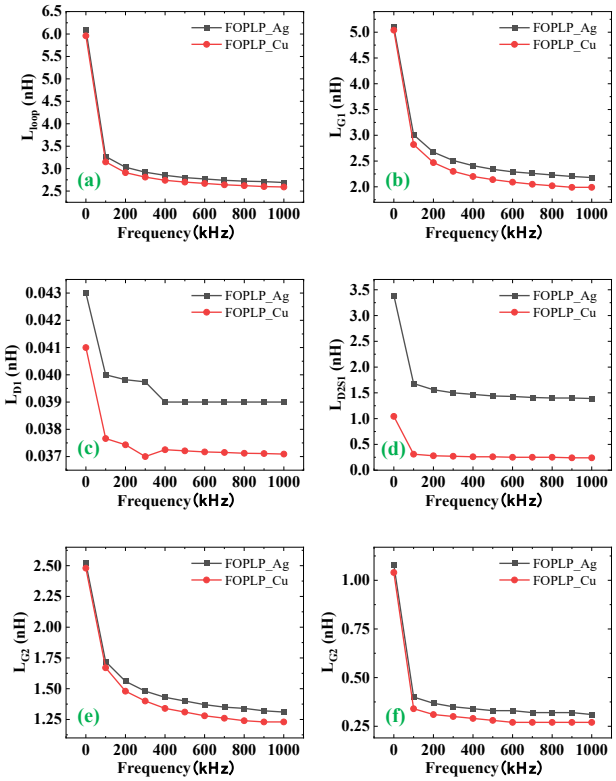

Fig. 8 The simulated parasitic inductance results for FOPLP_Ag and FOPLP_Cu: (a) Loop parasitic inductance; (b) G1 parasitic inductance; (c) D1 parasitic inductance; (d) D2S1 parasitic inductance; (e) G2 parasitic inductance; (f) S2 parasitic inductance

The simulated package parasitic inductances of both FOPLP_Ag and FOPLP_Cu are illustrated in Fig. 8. The packaging parasitic inductance is influenced by the switching frequency. Due to the skin effect and proximity effect, it decreases with increasing switching frequency. At a frequency of 100 kHz, the power loop parasitic inductances for FOPLP_Ag and FOPLP_Cu were 3.15 nH and 3.27 nH, respectively. Compared to FOPLP_Ag, the inductance value for FOPLP_Cu decreased by approximately 4%, as the height difference between the die and leadframe in FOPLP_Cu is smaller, and the sintered Cu in FOPLP_Cu exhibits greater bulk conductivity.

IV. Package Performance Analysis

In this section, to verify the functionality of both FOPLP_Ag and FOPLP_Cu packages, electrical, and thermal performances tests were conducted on the packaged devices.

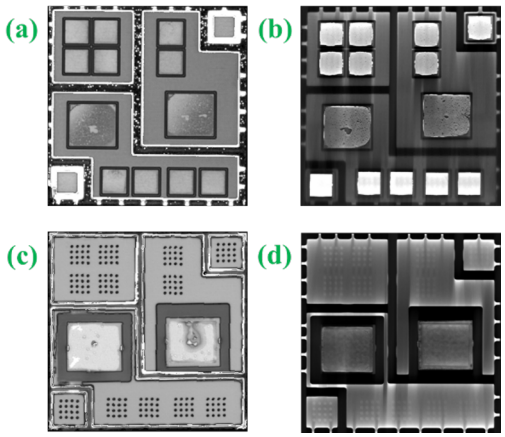

Fig. 9 Internal structural scanning of packaged samples: (a) CSAM of FOPLP_Ag; (b) X-RAY of FOPLP_Ag; (c) CSAM of FOPLP_Cu; (d) X-RAY of FOPLP_Cu.

A. Internal structure analysis

Both C-SAM (VUE 250-P, OKOS) and CT (xradia 620 versa, ZEISS) techniques were used to detect potential defects in the packages, the results are showed in Fig. 9. In the FOPLP_Ag packages, no significant delamination was observed, though some defects were found in the solder layers. Interconnects for smaller Cu connectors (2*2 mm^2) had only a few voids, while interconnects for larger SiC die

exhibited more voids, with some being quite large. The FOPLP_Cu packages showed no delamination or major void defects in the die interconnects.

After processes such as resin embedding, cutting, polishing, and grinding, cross-sectional images of FOPLP_Ag and FOPLP_Cu were obtained, as shown in Fig.10 (a) and (b). These images highlighted the use of Ag adhesive in FOPLP_Ag and sintered Cu in FOPLP_Cu, along with the groove in FOPLP_Ag and the cavity in FOPLP_Cu. For FOPLP_Cu, the images also showed the 0.1 mm Cu plate electroplated to connect with the hollow panel. Magnified cross-sectional images in Fig.10 (c) and (d) reveal that in both FOPLP_Ag and FOPLP_Cu, the Cu in the blind vias formed a strong mechanical bond with the die's top surface. The die's bottom surface was bonded to the substrate using Ag adhesive in FOPLP_Ag and sintered Cu in FOPLP_Cu, with a bond line thickness (BLT) of about 30 μm.

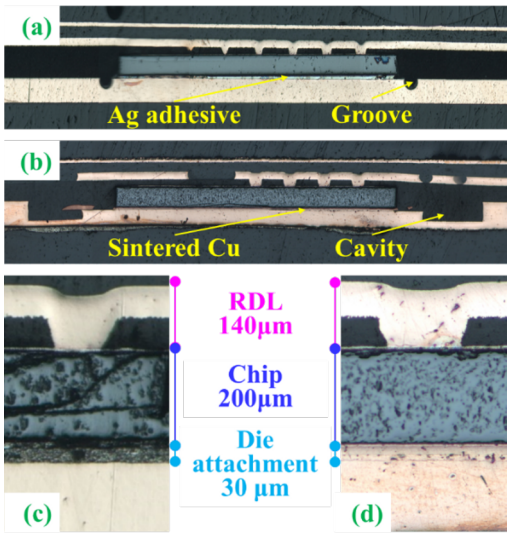

Fig. 10. Cross-section images showing high MOS in both FOPLP_Ag and FOPLP_Cu: (a) overall view of FOPLP_Ag; (b) magnified view of FOPLP_Ag; (c) overall view of FOPLP_Cu; and (d) magnified view of FOPLP_Cu.

B. Static and switching parameter analysis

To evaluate the functionality of FOPLP_Ag and FOPLP_Cu packaging, several electrical parameters were experimentally tested, including output characteristics, transfer characteristics, body diode forward characteristics, and parasitic capacitance using a curve tracer (B1506A, Keysight).

Fig. 11 (a) shows the output characteristics for both FOPLP_Ag and FOPLP_Cu, with the gate-source voltage (V_{GS}) set at 15 V and the drain-source voltage (V_{DS}) increasing from 0 V to 12 V in 0.1 V steps. The plot reveals no clear distinction between the linear and saturation regions of the SiC MOSFET, and as V_{DS} increased, the drain current (I_D) did not reach saturation. Fig.11 (b) shows the transfer characteristics of FOPLP_Ag and FOPLP_Cu, measured with a V_{DS} of 20 V and V_{GS} increasing from 0 V to 15 V in 0.1 V increments. The SiC MOSFETs exhibited high threshold voltages, sharp turn-on regions, wide operating voltage ranges, and minimal drain current saturation. Fig. 11 (c) shows the body diode forward characteristics for both FOPLP_Ag and FOPLP_Cu, with a V_{GS} of 0 V and diode forward voltage (V_{SD}) increasing from 0 V to 6 V in 0.1 V steps. The curves reveal that the SiC MOSFET body diodes exhibited a notably high forward conduction voltage. These characteristics make SiC MOSFETs ideal for applications requiring high temperature tolerance, high voltage, and high frequency.

To compare the packaging performance of FOPLP_Ag and FOPLP_Cu, static parameters such as breakdown voltage (BVDSS), $R_{DS(ON)}$, threshold voltage ($V_{GS(TH)}$), and V_{SD} were extracted, as shown in Fig. 12. The results indicate that the $R_{DS(ON)}$s for FOPLP_Ag and FOPLP_Cu were 43.4 mOhm and 42.0 mOhm, respectively. FOPLP_Cu showed a lower on-resistance compared to FOPLP_Ag, with a reduction of about 3%. Additionally, both FOPLP_Ag and FOPLP_Cu maintained similar breakdown voltage, threshold voltage, and body diode forward voltage drop.

The switching behavior of SiC MOSFETs is mainly determined by the charge and discharge cycles of parasitic capacitances, including C_{GS}, C_{DS} and C_{GD}. Among these, the C_{GD} is the most critical and complex, as it creates a feedback loop between the MOSFET's output and input. This C_{GD} consists of a fixed gate oxide capacitance (C_{OX}) and a nonlinear SiC depletion layer capacitance (C_{GDJ}).

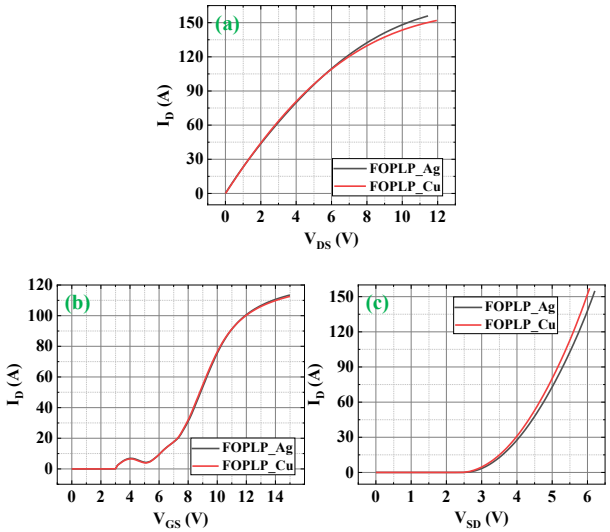

Fig.11. Characteristic curve testing of FOPLP_Ag and FOPLP_Cu: (a) output characteristics; (b) transfer characteristics; (c) body diode forward characteristics.

Under test conditions with a V_{GS} of 0 V and a frequency of 1 MHz, the input capacitance (C_{ISS}), output capacitance (C_{OSS}), and reverse transfer capacitance (C_{RSS}) for both FOPLP_Ag and FOPLP_Cu were evaluated, as shown in Fig. 13. The C_{ISS} values were similar for both, while C_{OSS} and C_{RSS} values for FOPLP_Cu were significantly lower than those for FOPLP_Ag.

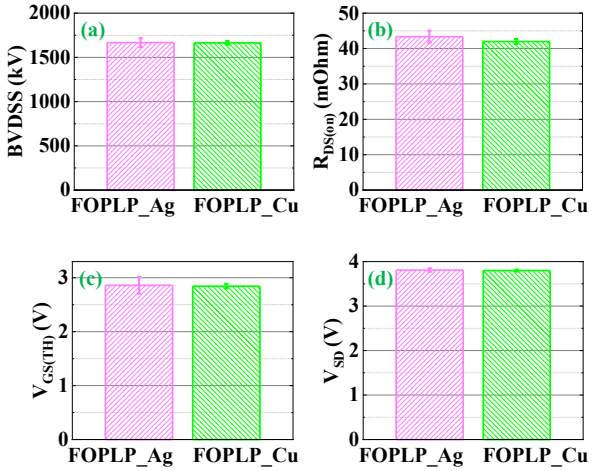

Fig. 12. Static parameter measurements of FOPLP_Ag and FOPLP_Cu: (a) BVDSS; (b) $R_{DS(ON)}$; (c) $V_{GS(TH)}$; (d) V_{SD}.

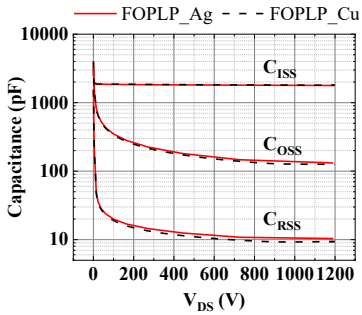

Fig.13. Parasitic input, output, and reverse capacitance testing for FOPLP_Ag and FOPLP_Cu

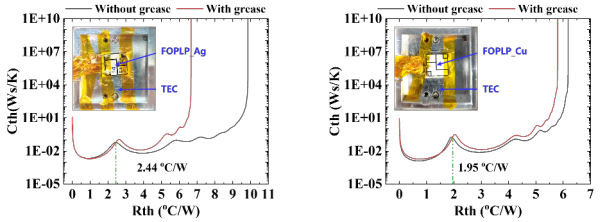

Fig.14. Differential structure function of thermal resistance from junction to heatsink pad: (a) FOPLP_Ag; (b) FOPLP_Cu.

C. Thermal resistance analysis

To evaluate thermal performance, thermal resistance measurements for FOPLP_Ag and FOPLP_Cu were conducted using the T3Ster from Mentor. The thermal resistance was measured using a dual-interface method, where the FOPLP heatsink pad was coupled with or without thermal grease to the temperature control platform. The tests applied a 2 A current to heat the body diode, with a 50 mA test current.

As shown in Fig. 14, the thermal resistance values for FOPLP_Ag and FOPLP_Cu using heatsink pad for cooling were 2.5 °C/W and 1.95 °C/W, respectively. FOPLP_Cu demonstrateed about 22% lower thermal resistance than FOPLP_Ag, mainly due to the high thermal conductivity of sintered Cu and the absence of low-conductivity interconnect layers typically introduced by the Cu connector.

V. CONCLUSION

This paper introduced a sintered Cu die attachment for the SiC MOSFET Fanout Panel Level Packaging (FOPLP) half-bridge module, offering superior thermal, electrical, and mechanical performance compared to the conductive Ag adhesive attachment used as a reference. A systematic approach, including simulation-based design, development, and performance testing, was successfully completed and validated. The key conclusions are as follows:

(1) A hollow panel was used to integrate sintered Cu into the FOPLP. The pre-sintered sandwich structure, including the SiC die, sintered layer, and 0.1 mm Cu plate, was embedded into the hollow panel and electrically connected via electroplating.

(2) Simulations showed that FOPLP with sintered Cu achieved lower inductance, thermal resistance, parasitic inductance, and thermal-mechanical deformation compared to FOPLP with Ag adhesive. However, due to the higher modulus of elasticity of sintered Cu, FOPLP with sintered Cu experienced slightly higher thermal stress.

(3) Experimental validation confirmed the proposed packaging process can be effectively implemented, with no delamination observed. The functionality of SiC MOSFETs in FOPLP was verified through static characteristics, switching characteristics, and thermal resistance measurements. FOPLP with sintered Cu also exhibited lower thermal resistance due to the high thermal and electrical conductivity of the sintered Cu.

This research advances miniaturized, high-energy-density packaging for SiC MOSFETs and lays the foundation for the commercial-scale application of SiC FOPLP.

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