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A Current Re-Use Quadrature RF Receiver Front-End for Low Power Applications: Blixator Circuit

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Abstract—This article presents the theory and implementation of a quadrature and differential RF front-end receiver. Combining balun, low-noise amplifier (LNA), mixer, and oscillator in a single stage, the proposed circuit, named the Blixator, is well suited for low-power applications. The baseband's transimpedance amplifier (TIA) also shares part of its dc current with the Blixator cell, resulting in sub-milliwatt power consumption. To avoid additional power and area by quadrature LO generation, the I/Q signals are generated at RF, employing the inductors already required for providing the dc current path of the LNA transistors. The expressions for gain, noise figure (NF), and phase noise of the voltage-controlled oscillator (VCO) are derived, and the behavior of the circuit is thoroughly investigated. The prototype of the Blixator receiver is implemented in a 0.18-μm CMOS technology. The experimental results show a NF of 10.5 dB, an IIP3 of −15.5 dBm, at the maximum gain, and an image rejection of 23 dB, which meets the requirements for the Bluetooth Low Energy (BLE) standard. The circuit consumes only 340-μW, from a 0.8-V supply, and its die area is 0.75 mm².

Index Terms—Blixator, Bluetooth Low Energy (BLE), impulse sensitivity function (ISF), Internet of Things (IoT), low-noise amplifier–mixer–voltage-controlled oscillator (LMV).

I. INTRODUCTION

THE development of Bluetooth Low Energy (BLE), ZigBee, and energy-harvesting applications, such as wireless sensor networks, wearable devices, personal body-area networks, and the Internet of Things (IoT), is justified by evolution of ultra-low-power (ULP) radios. The main challenge in the design of these ULP radios is to minimize their power consumption and footprint [1]–[11]. In such applications, the performance can be sacrificed in order to extend the battery lifetime. In BLE receivers, a noise figure (NF) better than

30 dB, an IIP3 higher than −30 dBm, and image rejection of about 21 dB are sufficient to meet the requirements [12], which leaves the voltage-controlled oscillator (VCO) as the most power-hungry block in the receiver chain. The required phase noise specification is about −105 dBc/Hz at an offset of 3 MHz [12]. Although this requirement is fairly relaxed, satisfying it at ULP radios is still challenging and requires power-efficient oscillator design. There has been a huge effort in the literature to increase the power efficiency in oscillators and their figure of merits (FoMs) [13]–[25]. On the other hand, low-noise amplifiers (LNAs), VCOs, and other RF blocks typically occupy large die areas, because of the bulky spiral inductors, which are used in biasing, impedance matching, and *LC*-tank networks. Circuit and current-reuse topologies are proper solutions to reduce both area and power consumption of the system, by incorporating multi-task blocks. The LNA, mixer, and VCO (LMV) cell introduced in 2006 by Liscidini *et al.* [26] is one of the first current and circuit reuse topologies, suited for low-power receivers. The oscillator and mixer are merged, while the oscillator also contributes in mixing, reducing the power consumption to 5.4 mW. The I/Q generation was implemented in LO, using a quadrature oscillator, which requires two dedicated *LC* tanks and additional die area. Overall, three internal inductors and one external inductor were used. In 2010, Tedeschi *et al.* [27] proposed an LMV circuit, with I/Q signal generation implemented in RF, using capacitive degeneration. As a result, the oscillator's *LC* tank was shared among the I/Q paths. Capacitive degeneration, however, produces an input impedance with negative real part, which calls for careful design and accurate simulations to avoid instability. The work was successful to reduce the power consumption to 3.6 mW. An effort in 2015 was made by Selvakumar *et al.* [12] to apply the most optimum oscillator in an LMV cell, in order to reduce the power, as much as possible. As a result, the complementary oscillator was employed, requiring only a slight increase in the minimum required supply voltage. The circuit has the minimum power dissipation, so far, among all the LMV cells. It consumes only 0.6 mW, and its die area is drastically efficient. The I/Q signals are elegantly generated by an *RC* network at the RF input, which, however, is rather sensitive to the parasitics and may result in degraded image rejection. None of the LMV structures described above have used differential RF signals and double-balanced mixers. Another circuit was introduced by Lin *et al.* [7] based on the Blixer cell (i.e., balun, LNA,

and mixer). The three blocks are stacked to share the same dc bias current. The active balun produces differential signals that are fed into a double-balanced mixer, while the power-hungry oscillator is not merged, consuming its own dc current. The overall power dissipation of the circuit is about 2.7 mW. A huge effort has also been made on receiver chain designs, without current and circuit reusing techniques. These works focused on power-efficient designing of each block, individually, and then cascading them in the chain. As an example, Yi *et al.* [28] reported a receiver chain for energy-harvesting applications in 2018, consuming only 382 μW from a 0.18-V supply voltage. The circuit, however, includes four inductors and occupies a 1.65-mm^2 die area.

This article presents another generation of circuit and current-reuse topologies, named the Blixator circuit (i.e., balun, LNA, mixer, and oscillator). In this work, balun has been added to the LMV circuit. Accompanied with the I/Q generator, this is the first circuit to produce all 0, 90, 180, and 270 phases at RF to inject the quadrature RF signals to the double-balanced mixer. The oscillator used in the introduced Blixator circuit exploits a multi-turn transformer to couple the LO signal to the gate of the double-balanced mixer. The whole system is more compact with a lower number of stacked transistors. Therefore, the minimum needed voltage and power is reduced for proper operation of the circuit. Transimpedance amplifier (TIA) shares part of its current with the LNA. Therefore, the LNA is biased at a higher dc bias current, which enhances its noise and linearity performances. A passive LC network acts as a hybrid quadrature generator at the input and, at the same time, provides the dc current path for the LNA. Only two inductors and one transformer are exerted, with no external components. It would also be possible to implement the hybrid quadrature generator only with one transformer to make it more area efficient, but at the cost of increased I/Q mismatch. To the best of authors' knowledge, implemented in a 0.18-μm CMOS technology, the presented receiver front end shows competitive performance compared with the state-of-the-art works.

This article is organized as follows. Section II presents the implementation of the Blixator cell. Section III discusses gain, input matching, and the I/Q generation circuit, followed by a noise analysis in Section IV. The pulling of the oscillator under RF blockers is investigated in Section V. Section VI presents the prototype implementation details and measurement results, and finally, the conclusions are drawn in Section VII.

II. BLIXATOR CELL

Fig. 1 shows an evolution toward the Blixator circuit, as the core of the proposed low-power RF front end. Starting from the conventional LMV cell introduced in [26], because of its low V_{DD} capability [see Fig. 1(a)], it is possible to make some modifications in the oscillator circuit to reduce the power consumption even further. For instance, the inductors can be replaced with a transformer for coupling the LO signal to the gates of M$_3$ and M$_4$ (as the main mixer), as shown in Fig. 1(b). Exploiting the signal amplification, caused by the transformer, this will either increase the conversion gain or relax the required LO level, resulting in reduced power consumption, in comparison with conventional LMVs. The

capacitor C_{diff} closes the current loop at RF frequencies while exhibiting a high impedance at IF frequencies. In this structure, the mixer transistors (M$_3$ and M$_4$) are driven deeply into the triode region. Thus, their required voltage headroom is reduced ($V_{DS} \simeq 0$), making it possible to further reduce the supply voltage. Moreover, a better $1/f$ noise performance is obtained.

The LMV, shown in Fig. 1(b), uses a single-balanced mixer to down-convert the RF signal to IF frequencies. Hence, it suffers from LO-to-IF feed through. In order to use the double-balanced mixer and to eliminate the capacitor C_{diff}, the oscillator core can be reconfigured according to Fig. 1(c). This is done by splitting each of the core transistors into two transistors, half in size compared to the previous ones and then connecting them in a semi-parallel way. The used double-balanced mixer structure suppresses the LO–IF feedthrough, compared to the single-balanced mixer. Therefore, the signal swing at the output of the mixer is significantly relaxed, improving the performance. The other advantages of a double-balanced design over a single-balanced counterpart include better rejection of common-mode noises, such as the substrate noise, increased linearity, improved suppression of spurious products, and inherent isolation between all ports. It will be shown that the double-balanced mixer also enhances the immunity to input blockers around ω_{LO} and $2\omega_{LO}$ [29]. Adding a balun and LNA to the present circuit will complete the final portrait of the Blixator (Balun + LNA + Mixer + Oscillator) circuit, as shown in Fig. 1(d). The active hybrid Balun + LNA split the RF signal into 0° and 180° RF currents. While some mismatches between the two paths may exist, the double-balanced mixer will also act as a current balancer to reject any amplitude and phase mismatches between the currents of two paths [7]. Noise cancellation in the balun-LNA improves the noise performance and makes it possible to trade it with power.

Fig. 2 shows the complete low-power receiver RF front end. An I/Q generator produces the quadrature signals at the input port. This block includes two separate inductors, which also provides the dc current path for the common-gate (CG) transistors. The input matching circuit is also realized by this stage. A high passive gain is achieved, which made it possible to obtain the input matching with a low g_{m9} of 0.5 mS, substantially lower compared to the 20 mS required to obtain an input impedance of 50 Ω. In more advanced technology node and because of the lower parasitics, one can bias the transistors even closer to the sub-threshold region to have better current efficiency (G_m/I_d) to obtain the same trans-conductances at lower dc currents.

As it is clear, all the blocks in the circuit are multi-task compatible with context of circuit and current-reuse structures for low-power applications, in which both the area and the power consumption are the most important constraints. Moreover, the Q-channel shares the same oscillator tank with the I-channel. This is one of the benefits of implementing quadrature signals at the RF port. It is possible to implement quadrature signals at the LO port by employing a quadrature oscillator, but at the cost of additional transformer and area penalty. The main drawback of quadrature signal generation at the RF port is that it deteriorates the NF of the circuit, which is less important in low-power applications.
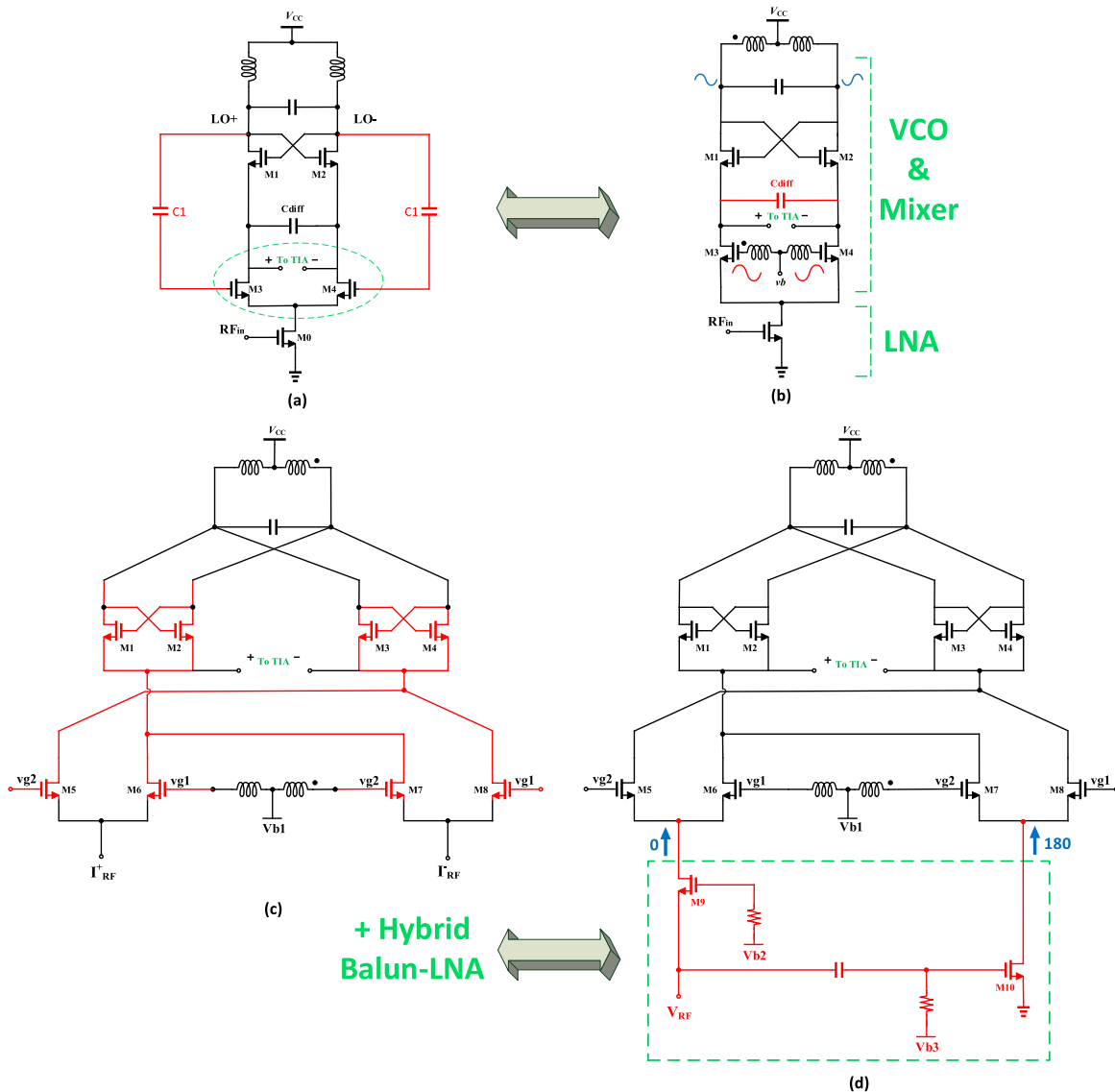
Fig. 1.   Evolution toward the Blixator circuit. (a) Conventional LMV. (b) Transformer-based LMV. (c) Double-balanced LMV based on transformer configuration. (d) Blixator circuit (I channel).

A different transimpedance amplifier with internal feedback is used in this work to reduce the input impedance at IF and to increase the conversion gain. Fig. 3 shows the differential TIA with low input impedance that is employed in the Blixator circuit. The TIA's input impedance is

$$R_{\text{in,TIA}} = \frac{1}{g_{m12}(1 + g_{m11}R)} \quad (1)$$

which is reduced by a factor of $(1+g_{m11}R)$, over a large bandwidth, in comparison with conventional CG TIAs. At higher frequencies, the loop gain is reduced, which increases the input impedance. The capacitor C_1 provides the required low impedance at higher frequencies, suppressing the out-of-band interferences. Part of the TIA's dc bias current is reused in LNA, which helps in linearity improvement and NF reduction. To obtain a good virtual ground for a given bias current, the size of M_{11} and M_{12} should be increased. The TIAs in the I/Q paths are followed by a two-stage complex baseband filter, with a topology similar to that used in [12].

III. IMPEDANCE MATCHING AND GAIN ANALYSIS

Fig. 4 shows the equivalent circuit that models the input impedance of RF port. It includes I/Q generator circuit and the parasitic elements of balun-LNA. The limited power budget does not allow to have $g_{m9} = g_{m10} = 1/Rs$ or 20 mS. Even assuming G_m/I_d of 20 V^{-1} for the LNA transistors (which corresponds to f_T of below 10 GHz in 180 nm at subthreshold), $g_m = 20$ mS would require 1-mA dc bias, which would result in a total of 4 mA for the LNA, very far from the used budget of 0.32 mA. Therefore, a value of 0.5 mS is used for g_{m9} (and g_{m10}), which leads to a CG input impedance of 2 kΩ. It should be noted that since the input impedance of the CG transistors is 2 kΩ, the parallel resistance of the inductors L_1 and L_2 also contribute in R_1 and R_2. According to our post-layout simulations, R_1 is about 1 kΩ and R_2 is about 700 Ω in Fig. 4. Fig. 5 shows that the implemented hybrid network has provided a wideband input matching. The simulated S_{11} is better than -10 dB for about 0.26-GHz bandwidth (2.27–2.53 GHz), which is more than enough for BLE applications. By some algebraic calculations, it can be shown that for
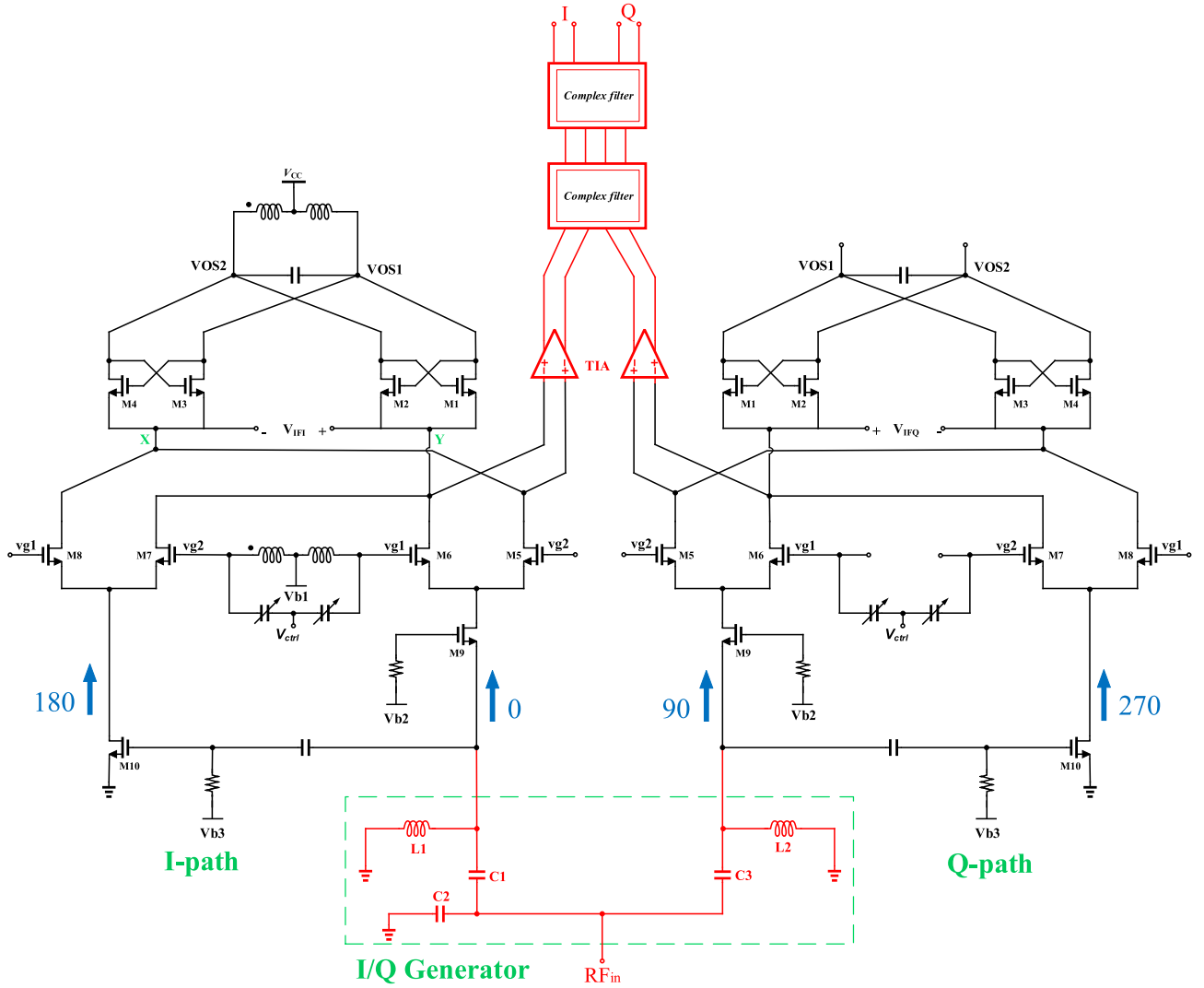
Fig. 2. Proposed current re-use low-power receiver RF front end.

the required 90° phase difference between the I and Q paths, we should have

$$\alpha_1 \alpha_2 Q_{p1} Q_{p2} = -1 \qquad (2)$$

where $Q_{p1} = (R_1/(L_1\omega))$ and $Q_{p2} = (R_2/(L_2\omega))$ are the equivalent quality factors of the inductors and $\alpha_1 = 1 - (L_1C_1 + L_1C_4)\omega^2$ and $\alpha_2 = 1 - (L_2C_3 + L_2C_5)\omega^2$. Similarly, to have equal amplitudes in I and Q paths, it requires

$$\left(\frac{L_1C_1}{L_2C_2}\right)^2 = \frac{\alpha_1^2 + Q_{p1}^{-2}}{\alpha_2^2 + Q_{p2}^{-2}}. \qquad (3)$$

Fig. 6 shows the simulated phase and amplitude mismatch between the I/Q paths over different process and temperature corners in worst cases (TT 25°, SS −40°, and FF 80°) in the designed circuit, which shows acceptable matching in the bandwidth of interest. Monte Carlo simulations (200 samples) have also been run at $f_{RF} = 2.4$ GHz to find the amplitude and phase mismatches between the I/Q paths. These simulations show that the maximum phase mismatch is about 3.5° and the maximum amplitude mismatch is about 5%. The Monte Carlo simulation (200 samples) has also been run for the overall

IRR of the receiver. The results illustrate that image rejection varies from 22.5 to 28.5 dB (almost ±3 dB around the mean value).

The simulation is repeated to find out the amplitude and phase mismatch of (0 and 180) signals in the I-channel at LNA output. As shown in Fig. 7 in the frequency band of 2.35–2.45 GHz, which covers the BLE standard, the variations for amplitude and phase of the paths are about 6% and 4°, respectively. The result is the same for (90 and 270) signals in Q-channel because of symmetry in the circuit.

The effective current gain from mixer stage through the IF load TIA is

$$A_{I,\text{Mixer}} = \frac{2}{\pi}\left(\overline{\frac{R_{CC}(t)}{R_{CC}(t) + R_{\text{in,TIA}}}}\right) = \frac{2}{\pi}\alpha_{\text{div}} \qquad (4)$$

where $\overline{(.)}$ denotes the time average and $R_{CC}(t)$ is the equivalent time-variant impedance seen at the source of the cross-coupled M_1 and M_2 and M_3 and M_4 transistors. As a matter of fact, the ideal current gain of $2/\pi$ is degraded by the non-zero $R_{\text{in,TIA}}$ and the finite $R_{CC}(t)$, which is a time-variant resistance, as shown in Fig. 8 [30]. The impedance $R_{\text{max}} = 1/g_{m,\text{ON}}$
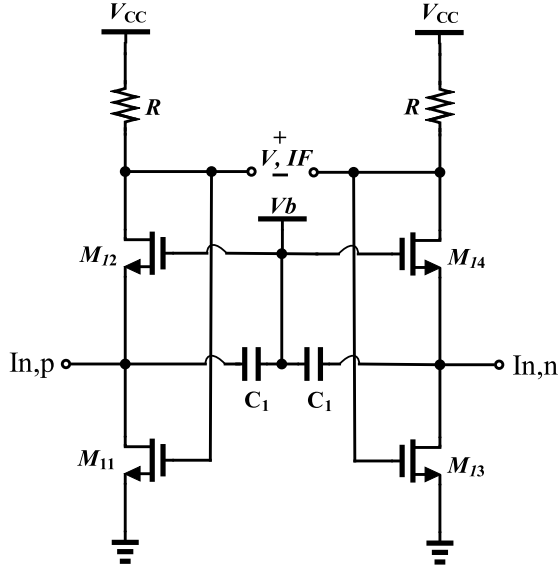
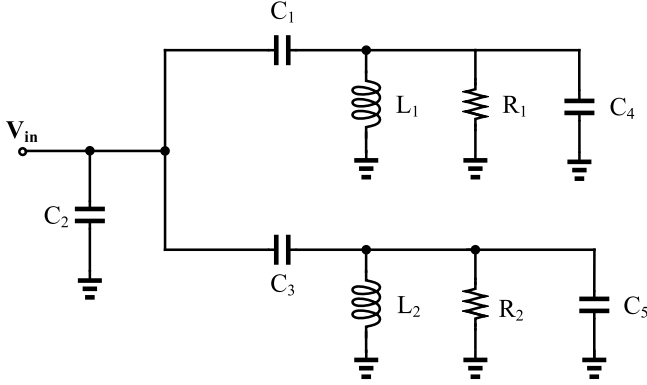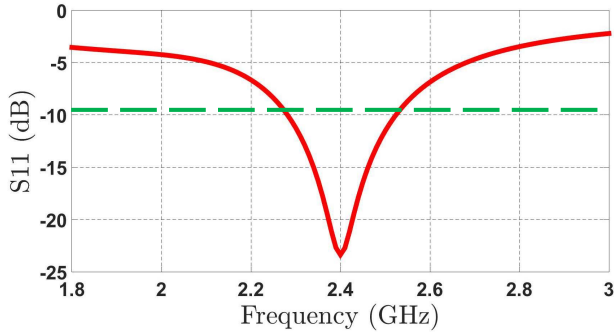Fig. 3. Low input impedance transimpedance amplifier.

Fig. 4. Equivalent circuit for calculating the input impedance of receiver.

Fig. 5. Input matching (S_{11}) of receiver.

corresponds to the source impedance of the ON-transistor; once the other transistor is turned off, $R_{\min} = 1/2g_{m,\mathrm{dc}}$ corresponds to the source impedance at equilibrium, T_{LO} is the LO period, and τ_r is the rise time. With respect to the approximate model of $R_{\mathrm{CC}}(t)$ in Fig. 8, α_{div} can be calculated as

$$
\begin{aligned}
\alpha_{\mathrm{div}} &= \frac{4\tau_r}{T_{\mathrm{LO}}}\left[1 - \frac{R_{\mathrm{in,TIA}}}{\Delta R}\ln\left(\frac{R_{\mathrm{in,TIA}}+R_{\max}}{R_{\mathrm{in,TIA}}+R_{\min}}\right)\right] \\
&\quad + \left(1 - \frac{4\tau_r}{T_{\mathrm{LO}}}\right)\frac{R_{\max}}{R_{\mathrm{in,TIA}}+R_{\max}} \\
&\approx \frac{R_{\max}}{R_{\max}+R_{\mathrm{in,TIA}}}\left[1 - \frac{4\tau_r}{T_{\mathrm{LO}}}\cdot\frac{\Delta R}{R_{\max}}\cdot\frac{R_{\mathrm{in,TIA}}}{R_{\mathrm{in,TIA}}+R_{\min}}\right].
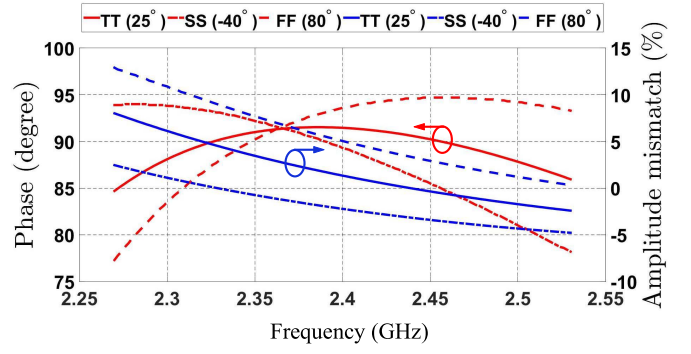\end{aligned}
\tag{5}
$$

Fig. 6. Phase and amplitude mismatch between I/Q paths over different process and temperature corners (TT corner 25°, FF corner 80°, and SS corner −40°) at LNA input.
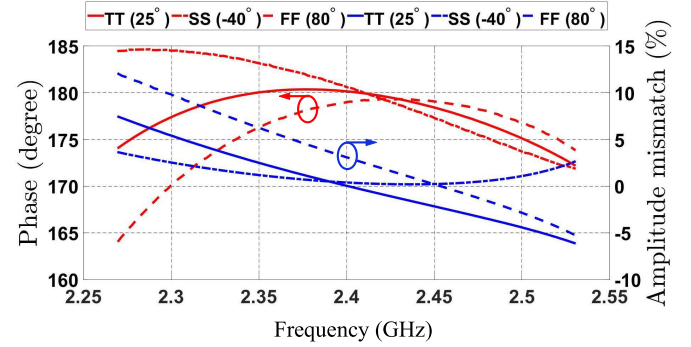
Fig. 7. Phase and amplitude mismatch between 0° and 180° signal paths over different process and temperature corners (TT corner 25°, FF corner 80°, and SS corner −40°) at LNA output.
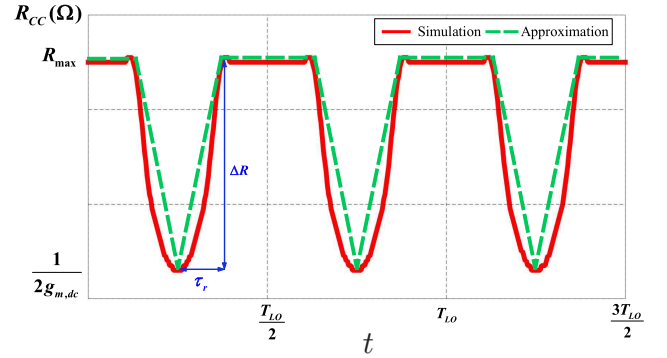
Fig. 8. Impedance at the source of oscillator cross-coupled transistors.

In the designed circuit, α_{div} is about 0.85. Finally, the transconductance of the Blixator can be written as

$$
G_{m,\mathrm{Blix}} = \frac{1}{2} \times \mathrm{Gain}_H \times g_{m,\mathrm{LNA}} \times A_{I,\mathrm{Mixer}}
\tag{6}
$$

where Gain_H is the passive gain of the hybrid section, $g_{m,\mathrm{LNA}}$ is the loaded transconductance of the LNA, and the one-half factor represents the equal current division between I/Q paths. Therefore, the total conversion gain will be

$$
\begin{aligned}
CG &= G_{m,\mathrm{Blix}} \times R_{G,\mathrm{TIA}} \\
&= \frac{1}{\pi} \times \mathrm{Gain}_H \times g_{m,\mathrm{LNA}} \times \alpha_{\mathrm{div}} \times R_{G,\mathrm{TIA}}
\end{aligned}
\tag{7}
$$

where $R_{G,\mathrm{TIA}} = R/(1 + g_{m11}R)$ is the transimpedance gain of the TIA.

It should be noted that gain control is necessary for a practical system. This can be conveniently done in IF, by adjusting

the gain in TIA (e.g., by switching R) or in the complex filter. The RF circuit is fairly linear due to the current-mode operation of the mixer and the low input impedance of the TIA. Simulations show that the input P-1 dB of the RF receiver is about -26 dBm, which is sufficient for most situations, provided that the IF gain is lowered to prevent its saturation. Nevertheless, gain control in RF can also be helpful for improving the dynamic range. A viable option is to add a switchable floating resistor array between the drains of M_9 and M_{10}, to steer part of the RF signal to the virtual ac ground.

IV. NOISE ANALYSIS

In conventional receivers, there is no noise cross effect between VCO phase noise and circuit NF, but in current and circuit reuse topologies such as the Blixator cell, the noise of different components of various parts has crosstalk with each other. Hence, the oscillator-mixer and TIA components contribute in system NF and LNA–mixer–TIA contribute in the phase noise of VCO. This makes the noise analysis more complicated. For simplicity, the noise analysis is first conducted based on the Blixator cell shown in Fig. 1(d), while the results are finally extended to the quadrature circuit shown in Fig. 2.

A. Noise Figure

Starting from the LNA, all the noise contributors are considered at the TIA's output voltage. While noise of the CG transistor M_9 is canceled at the differential output,[1] the output noise current contribution of the common-source transistor M_{10} [in Fig. 1(d)] can be calculated as

$$\overline{v_{\text{on,LNA}}^2} = 4kT\gamma\, g_{m10}\alpha_{\text{div}}^2 R_{G,\text{TIA}}^2. \tag{8}$$

It should be noted that the flicker noise of M_{10} up-converts to LO frequencies and will not appear at the IF output. Only the finite IP2 of the mixer can cause the flicker noise of M_{10} to be appeared at the output.

A high gate bias voltage of V_{B1} is chosen for biasing the mixer transistors (M_5–M_8). As a result, once being turned on, the mixer transistors are quickly driven into the triode region. Thus, it is assumed that the mixer switches are toggling between off and triode regions during the circuit operation. The thermal noise contribution of the mixer transistors (M_5–M_8) can be explained by direct and indirect mechanisms. In the direct mechanism, the noise generated by the mixer is considered during the overlap time of the switches. Following the method presented in [31], but also considering the non-zero input impedance of the TIA, the resulting differential output noise current can be approximately written as

$$\overline{v_{\text{on,Mix}}^2} \simeq \frac{32 \times 4kT\gamma}{3S \times T_{\text{LO}}}\mu_n C_{\text{ox}}(W/L)_{5-8}V_{\text{eff}}^2\beta_{\text{div}}^2 R_{G,\text{TIA}}^2 \tag{9}$$

where S is the slope of the single-ended LO during the zero crossings, T_{LO} is the oscillation period, V_{eff} is the dc effective voltage of the switches, μ_n is the electron mobility, C_{ox} is the

[1]Our simulations show that the noise contribution of M_9 can also be neglected in the quadrature circuit, as shown in Fig. 2. Moreover, there is negligible noise contribution from the I path in the Q path and vice versa, because of the adequate isolation of the hybrid circuit.

gate oxide capacitance, and $(W/L)_{5-8}$ is the aspect ratio of the mixer transistors. Also, β_{div} is the effective current division coefficient between the TIA, $R_{\text{CC}}(t)$, and the output impedance of the switches, during the overlap times, when all switches are ON. A good approximation for β_{div} is

$$\beta_{\text{div}} \simeq \frac{R_{\text{in,TIA}}^{-1}}{R_{\text{in,TIA}}^{-1} + R_{\min}^{-1} + \frac{4}{3}\mu_n C_{\text{ox}}(W/L)_{5-8}V_{\text{eff}}} \tag{10}$$

where $(4/3)\mu_n C_{\text{ox}}(W/L)_{5-8}V_{\text{eff}}$ is the average output conductance of the switches, during the overlap times, in which $R_{\text{CC}}(t)$ is also approximated by $R_{\min}$. By exploiting the transformer and enhancing the LO signal at the gate of the switches, S will also be improved, which significantly reduces the noise contribution of the mixer, as suggested by (9).

In the indirect mechanism, the parasitic capacitance at the tail node of the mixer is also considered and results in noise contribution from the switches, even outside the overlap times [31]. Our simulations, however, show that the direct mechanism is dominant in the designed Blixator. Therefore, the indirect mechanism is neglected. In theory, the switch flicker noise also appears at the output [31]. The flicker noise of the mixer can also be neglected in the designed circuit according to the simulations.

Now, let us investigate the noise contribution of the oscillator transistors (M_1–M_4). The thermal current noise of these transistors can be decomposed into two components: 1) the current that is drawn from the drains to the ground and 2) the same current flowing from ground to the sources of M_1–M_4. It can be seen that the first current (as well as the noise current contribution of the tank loss) does not appear at the differential output. Consequently, only the second current (i.e., the noise current from the ground to the source of the cross-coupled pairs) is important. A good approximation for the resulting output noise is

$$\overline{v_{\text{on,Osc}}^2} \simeq 4 \times 4kT\gamma\,\overline{g_{m1}(t)}\alpha_{\text{div}}^2 R_{G,\text{TIA}}^2 \tag{11}$$

where $\overline{g_{m1}(t)}$ is the average transconductance of the core transistors, which can be approximated as $0.5/R_{\max}$. Finally, the output noise contribution of the TIA can be written as

$$\overline{v_{\text{on,TIA}}^2} = 2 \times 4kT\left[\gamma\, g_{m11}\alpha_{\text{div}}^2 R_{G,\text{TIA}}^2 \right.$$
$$+ \gamma\, g_{m12}R^2(1 - \alpha_{\text{div}})^2$$
$$\left. + R\left(1 - \frac{\alpha_{\text{div}}g_{m11}R}{1 + g_{m11}R}\right)^2\right]. \tag{12}$$

Consequently, the total NF of the Blixator circuit (either of I or Q channels) is found as

$$\text{NF} \simeq 1 + \frac{\gamma\, g_{m10}\alpha_{\text{div}}^2}{R_S G_{m,\text{Blix}}^2}$$
$$+ \frac{32\gamma\,\mu_n C_{\text{ox}}(W/L)_{5-8}V_{\text{eff}}^2\beta_{\text{div}}^2}{3ST_{\text{LO}}R_S G_{m,\text{Blix}}^2} + \frac{2\gamma\, R_{\max}^{-1}\alpha_{\text{div}}^2}{R_S G_{m,\text{Blix}}^2}$$
$$+ \frac{2\gamma\, g_{m11}\alpha_{\text{div}}^2 + 2\gamma\, g_{m12}(1 - \alpha_{\text{div}})^2(1 + g_{m11}R)^2}{R_S G_{m,\text{Blix}}^2}$$
$$+ \frac{2R^{-1}[1 + g_{m11}R(1 - \alpha_{\text{div}})]^2}{R_S G_{m,\text{Blix}}^2} \tag{13}$$

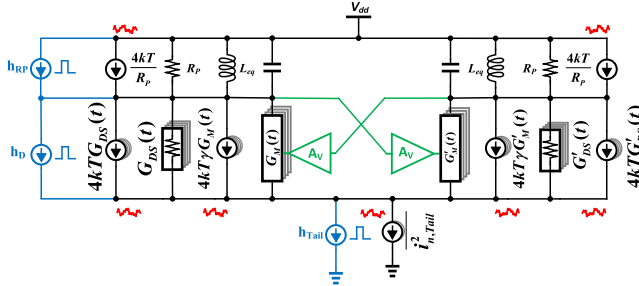| Noise Source	NF Calculation	NF Simulation
LNA	33.2%	28.7%
Mixer	15.9%	17.7%
TIA	37.3%	38.2%
Hybrid	–	1.7%
Oscillator	12.5%	13.7%
Total NF (dB)	**8.7**	**9.8**

Fig. 9. Simplified noise model of the oscillator.

where R_S is the input source impedance. Simulations show that the contributions from LNA and TIA are the most dominant terms. Increasing gain of the LNA (or $G_{m,\text{Blix}}$) will minimize the NF. Thus, increasing the LNA's bias current improves the noise performance, but at the cost of extra power budget. Reusing the TIA's current in the LNA, therefore, significantly reduces the required power consumption, as both blocks have the most impact on NF. Table I shows the calculated NF based on (13) and the simulations results. Neglected in previous current-reuse works, the NF contribution of the TIA is indeed significant, because of the limited power budget.

B. Phase Noise

Fig. 9 shows the simplified noise model for the Blixator cell. The resistor R_P models loss of the equivalent inductor obtained by the electromagnetic (EM) simulation, and $G_M(t)$ and $G_{DS}(t)$ refer to the time-variant transconductance and channel conductance of the core transistors, respectively, while the noise contribution of the rest of the circuit is modeled with $\overline{i_{n,\text{Tail}}^2}$ at the source node of the cross-coupled pair. Also, h_{RP}, h_D, and h_{Tail} are the non-normalized ISFs corresponding to tank, core devices, and tail noise sources, respectively. The non-normalized ISFs are extracted by accurate PXF simulations using SpectreRF.

According to the linear time-variant (LTV) phase noise model [32] N_i, the effective phase noise produced by the ith device is calculated by

$$N_i = \frac{1}{2\pi} \int_0^{2\pi} h_i^2(\omega_0 t) \overline{i_{n,i}^2(\omega_0 t)} d(\omega_0 t) \quad (14)$$

where $\overline{i_{n,i}^2(\omega_0 t)}$ is the ith noise current power spectral density (PSD) and $h_i(\omega_0 t)$ is its relevant non-normalized ISF function. Thus, for each R_P, we have

$$N_{RP} = \frac{1}{2\pi} \int_0^{2\pi} h_{RP}^2(\omega_0 t) d(\omega_0 t) \cdot \frac{4kT}{R_P}. \quad (15)$$

Similarly, the effective phase noise resulted by $G_M(t)$ and $G_{DS}(t)$ for each of the transistors is as follows:

$$N_{GM} = \frac{1}{2\pi} \int_0^{2\pi} h_{GM,\text{eff}}^2(\omega_0 t) d(\omega_0 t) \cdot \overline{i_{n0,GM}^2} \quad (16)$$

$$N_{GDS} = \frac{1}{2\pi} \int_0^{2\pi} h_{GDS,\text{eff}}^2(\omega_0 t) d(\omega_0 t) \cdot \overline{i_{n0,GDS}^2} \quad (17)$$

where $\overline{i_{n0,GM}^2} = 4kT\gamma \max(G_M)$, $\overline{i_{n0,GDS}^2} = 4kT \max(G_{DS})$, and

$$h_{GM,\text{eff}}(\omega_0 t) = h_D(\omega_0 t) \cdot \sqrt{\frac{G_M}{\max(G_M)}} \quad (18)$$

$$h_{GDS,\text{eff}}(\omega_0 t) = h_D(\omega_0 t) \cdot \sqrt{\frac{G_{DS}}{\max(G_{DS})}}. \quad (19)$$

The induced flicker noise by transistors can also be written as

$$N_{1/f} = \left[\frac{1}{2\pi} \int_0^{2\pi} h_{1/f}(\omega_0 t) d(\omega_0 t) \right]^2 \overline{i_{n0,1/f}^2} \quad (20)$$

where $\overline{i_{n0,1/f}^2} = (\text{KF}/f^{\text{AF}}) \cdot \max(G_M^2)$ and

$$h_{1/f}(\omega_0 t) = h_D(\omega_0 t) \cdot \frac{G_M}{\max(G_M)}. \quad (21)$$

The next step is to calculate the phase noise contribution of $\overline{I_{n,\text{tail}}^2}$ in Fig. 9. Since our simulations show that the contributions of mixer and TIA components in the total phase noise are negligible, we will only consider the LNA transistors M_9 and M_{10}. First, the time-domain noise transfer function from these noise sources through the source node of the cross-coupled pairs will be evaluated. Then, the resulting function multiplied by the tail ISF will result in the phase noise contribution of these stages. Such a calculation is valid according to the bank theory [33], and it is similar to the phase noise evaluation of the tail current source in classes B, C, and F oscillators.

The injected current noise at node X (source of the left cross-coupled pair in Fig. 2) can be written as

$$i_{n,X} = p(t) \times i_{n,M10} + p'(t) \times i_{n,M9} \quad (22)$$

where $i_{n,M9}$ and $i_{n,M10}$ are the noise currents of M_9 and M_{10}, respectively, $p(t)$ is a square wave toggling between one and zero with a period of T_{LO}, and $p'(t) = 1 - p(t)$ is its complement. Similarly, the injected current noise at node Y (source of the right cross-coupled pair in Fig. 2) is

$$i_{n,Y} = p(t) \times i_{n,M9} + p'(t) \times i_{n,M10}. \quad (23)$$

In order to obtain the noise currents injected to the oscillator cores, both $i_{n,X}$ and $i_{n,Y}$ are multiplied by the same current division coefficient of

$$\xi_{\text{div}} \simeq \frac{\overline{R_{CC}^{-1}(t)}}{R_{\text{in,TIA}}^{-1} + \overline{R_{CC}^{-1}(t)}} \quad (24)$$

where, for simplicity and similar to our previous derivations, it is assumed that the coefficient is approximately constant over the oscillation period. The ISF of both injected currents is the same and can be written as

$$h_{\text{Tail}}(\omega_0 t) = \sum_{n=0}^{\infty} a_{2n} \cos(2n\omega_0 t + \phi_{2n}). \quad (25)$$

The noise contribution of LNA components in oscillator phase noise can be calculated as

$$\phi_{n,\text{LNA}} = \xi_{\text{div}}(i_{n,X} + i_{n,Y})h_{\text{Tail}}(\omega_0 t)$$
$$\simeq \xi_{\text{div}} \sum_{n=0}^{\infty} a_{2n} cos(2n\omega_0 t + \phi_{2n}) \cdot (i_{n,M9} + i_{n,M10}).$$
(26)

Extracting the dc and harmonics of the effective ISF results in

$$\phi_{n,\text{LNA}}\big|_{\text{DC}} = \xi_{\text{div}} a_0 cos(\phi_0)(i_{1/f,M9} + i_{1/f,M10})$$
$$= h_{\text{LNA},1/f}(\omega_0 t) \cdot (i_{1/f,M9} + i_{1/f,M10}) \quad (27)$$
$$\phi_{n,\text{LNA}}\big|_{2\omega_0} = \xi_{\text{div}} a_2 cos(2\omega_0 t + \phi_2) \cdot (i_{\text{th},M9} + i_{\text{th},M10})$$
$$= h_{\text{LNA}}(\omega_0 t) \cdot (i_{\text{th},M9} + i_{\text{th},M10}). \quad (28)$$

The dc term is responsible for flicker noise up-conversion of the LNA components. Expanding and clustering the same terms in the above equations and then calculating the RMS value of the coefficients of the effective ISF($\phi_{n,\text{LNA}}$) results in

$$N_{\text{LNA},1/f} = \left[\frac{1}{2\pi}\int_0^{2\pi} h_{\text{LNA},1/f}(\omega_0 t)d(\omega_0 t)\right]^2$$
$$\cdot \left(\overline{i_{1/f,M9}^2} + \overline{i_{1/f,M10}^2}\right) \quad (29)$$
$$N_{\text{LNA}} = \frac{1}{2\pi}\int_0^{2\pi} h_{\text{LNA}}^2(\omega_0 t)d(\omega_0 t) \cdot 4kT\gamma(g_{M9} + g_{M10}). \quad (30)$$

Consequently and considering the number of components in both I and Q paths, the overall phase noise of the Blixator circuit is

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left(\frac{8N_{\text{GM}} + 8N_{\text{GDS}} + 8N_{1/f} + 2N_{\text{RP}}}{2(\Delta\omega)^2}\right.$$
$$\left. + \frac{2N_{\text{LNA}} + 2N_{\text{LNA},1/f}}{2(\Delta\omega)^2}\right). \quad (31)$$

Table II outlines the consistency between the calculated phase noise distribution according (31) and the simulated ones. The simulated total phase noise is slightly worse than the calculated one because more noise sources are considered. Besides that, some second-order effects, such as the overlap time when both M_7 and M_8 or M_5 and M_6 are ON, are neglected. The oscillator tank and core transistors have the major phase noise contributions. Nevertheless, it is interesting that the flicker noise of the LNA transistors is also considerable and should be accounted for in the circuit design flow.

V. PULLING EFFECT

The susceptibility of the Blixator circuit should be evaluated against injection pulling for blockers around both ω_{LO} and $2\omega_{\text{LO}}$. Fig. 10 shows the blocker terms produced at each node of the circuit due to RF input blockers at ω_{LO} and $2\omega_{\text{LO}}$. In particular, the terms around $2\omega_{\text{LO}}$ injected at the sources of the cross-coupled pairs may cause the oscillator to operate like an injection locking frequency divider, being pulled or even locked to half of the divider frequency or produce spurs, if exerted in a phase-locked loop (PLL) [34]–[37]. PLL has

TABLE II
CALCULATED AND SIMULATED PN DISTRIBUTION

Noise Source	PN Calculation	PN Simulation
Oscillator Tank	50.2%	56.2%
Oscillator NMOS Core (Thermal Noise)	23%	20.9%
Oscillator NMOS Core (Flicker Noise)	1.6%	1.3%
TIA (Thermal Noise)	–	0.2%
TIA (Flicker Noise)	–	0.03%
Mixer (Thermal Noise)	–	0.33%
Mixer (Flicker Noise)	–	0.04%
LNA (Thermal Noise)	6.8%	4.2%
LNA (Flicker Noise)	17.4%	16.8%
Total PN @ 1MHz (dBc/Hz)	**-120.85**	**-119.6**

not been included in this work, but the proposed Blixator circuit could easily be inserted into a traditional PLL structure. This is possible because, at RF, the merged circuit looks like a traditional *LC* oscillator, preserving the tuning capability and, hence, the possibility to be exerted in conventional PLL architectures. Generally, there is no so much issue with PLL operation in the Blixator circuit. It seems that there is no difference between this receiver and other conventional receivers from a PLL point of view. It is only known that the phase noise will be affected by the properties of the PLL. For example, the closed-in phase noise will be dominated by the PLL, instead of the VCO. As it is shown in Fig. 10, the double-balanced mixer partially cancels out the terms produced by $2\omega_{\text{LO}}$ blocker, and there will be no corresponding even harmonics at nodes X and Y. Only ω_{LO} blocker produces even harmonics at nodes X and Y, which may potentially pull or lock the oscillator. However, as can be seen in Fig. 10, these blocker terms appear out of phase at nodes X and Y. Consequently, their overall injection effect is canceled at the oscillator output. In general, and assuming any blocker V_{RF} at the input, we can write the currents injected at nodes X and Y as follows:

$$I_X = g_{m9}V_{\text{RF}}\xi_{\text{div}} \cdot p'(t) - g_{m10}V_{\text{RF}}\xi_{\text{div}} \cdot p(t) \quad (32)$$
$$I_Y = g_{m9}V_{\text{RF}}\xi_{\text{div}} \cdot p(t) - g_{m10}V_{\text{RF}}\xi_{\text{div}} \cdot p'(t). \quad (33)$$

Therefore, the overall injection will be

$$I_X + I_Y = (g_{m9} - g_{m10})V_{\text{RF}} \quad (34)$$

which is approximately zero, because $g_{m9} \simeq g_{m10}$ to have proper balun operation and acceptable noise cancellation. Similar injection cancellation also happens in the Q channel circuits. Fig. 11 shows pulling susceptibility due to nearby interferers at different frequency offsets. The plotted curve shows the (locking range $= \omega_{\text{LO}} - \omega_{\text{inj}} =$ offset from LO) versus blocker power. For each input blocker power, the offset frequency is lowered until it reaches the locking range of the receiver. It shows that at an offset frequency of 1 MHz, the oscillator can be locked only with an input power of -8 dBm, which is well above the saturation point of the receiver. This demonstrates the immunity of Blixator circuit to the pulling phenomenon since it is not possible to have such large blockers feeding directly into Blixator. Simulations also show that the proposed double-balanced circuit should be considerably more immune (about 8 dB), compared to a similar single-balanced design. It should also be noted that increasing the input power (power of input blockers) of circuit causes the LMV cell and
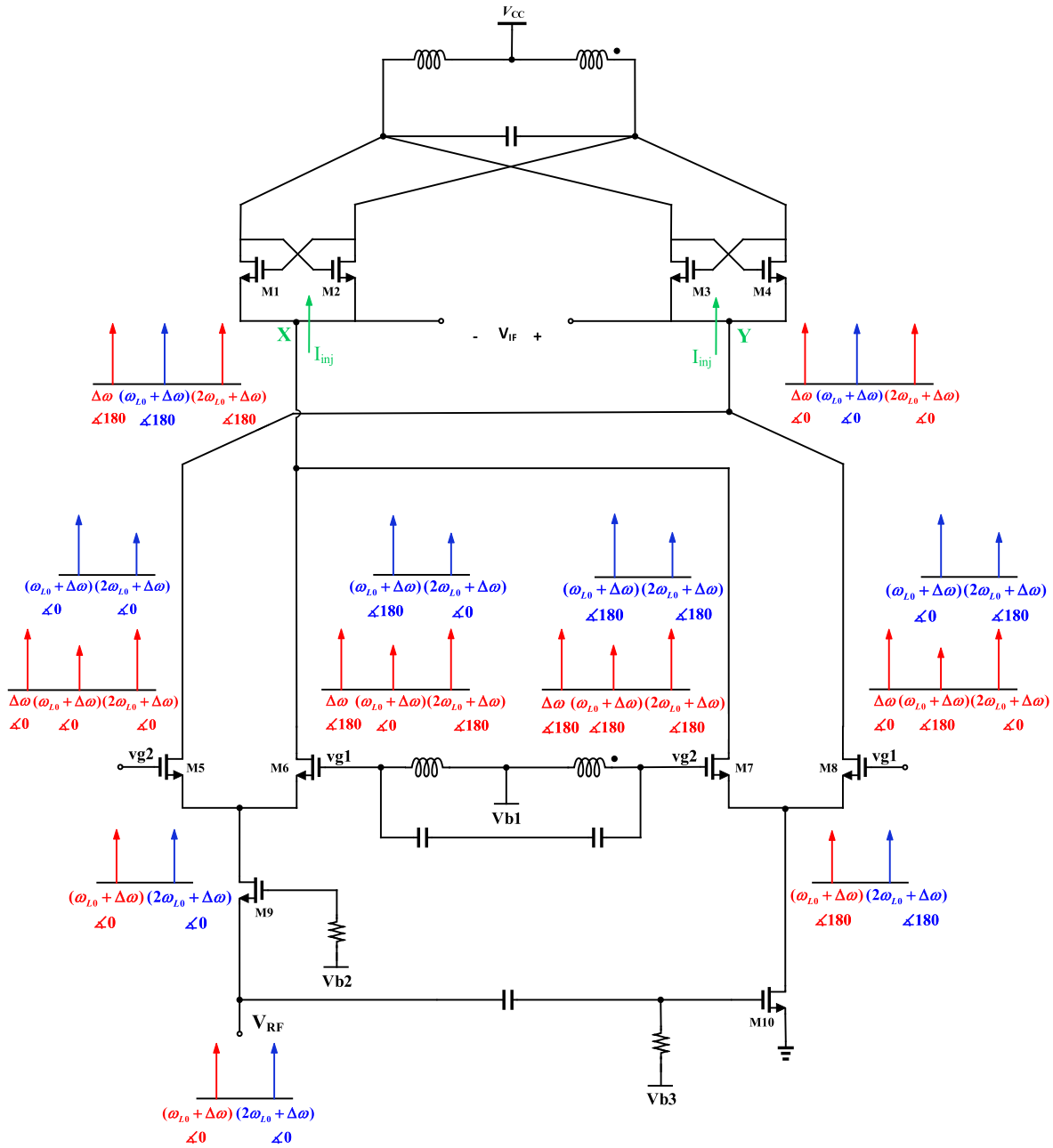
Fig. 10.   Pulling effect of fundamental and second harmonic components at RF input.
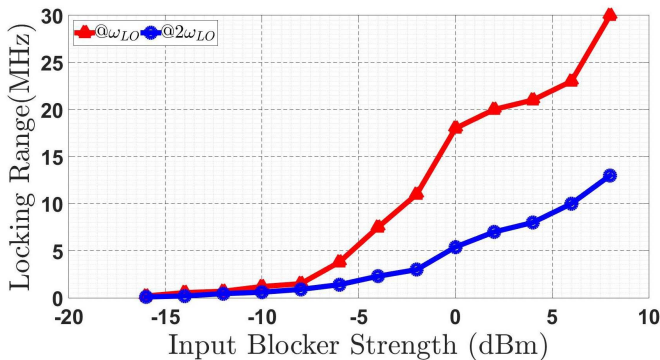

Fig. 11.   Locking range versus blockers power at input RF port.

the TIAs to operate in an abnormal state, making the analysis of the problem very difficult.

TABLE III
POWER CONSUMPTION OF SUB-BLOCKS IN THE BLIXATOR CELL

Sub-block	Consumption
Blixator+TIA	322 μA
VCO	222 μA
TIA	2 × 50 μA
LNA	322 μA
Baseband Complex Filter	103 μA
Total Current	425 μA
Total Power (supply 0.8 V)	**340 μW**

VI. IMPLEMENTATION AND MEASUREMENTS

A. Prototype Implementation

A prototype of Blixator cell is designed and implemented in a standard 0.18-μm CMOS process with a core area of 0.75 mm², for low-power applications, such as BLE. The die

TABLE IV
PERFORMANCE OF DIFFERENT RF RECEIVER FRONT-ENDS

	JSSC'14 [7]	JSSC'15 [12]	JSSC'18 [28]	ISSCC'18 [1]	ISSCC'20 [9]	JSSC'20 [11]	**This Work**
Application	2.4GHz ZigBee	2.4GHz BLE	2.4GHz BLE	2.4GHz BLE	2.4GHz BLE	2.4GHz BLE	**2.4GHz BLE**
Architecture	Blixer + Hybrid Filter + Passive RC-CR	Current Re-use Quadrature LMV	LNA + Class-D VCO + Passive I/Q Gen.	Interference-Tolerant + Hybrid-Loop	LNTA + Passive Mixer + 4th order BPF	LNTA + Mixer + FIR Filter	**Blixator + Complex Filter**
External Component	Zero	1 Inductor + 1 Cap	Zero	Zero	Zero	Zero	**Zero**
VDD (V)	0.6 & 1.2	0.8	0.18	1	0.5	0.7	**0.8**
Power (mW)	2.7	0.6	0.38	1.2*	0.89*	0.37	**0.34**
NF (dB)	9	15.1 to 15.8	11.3	6	-	5.5	**10 to 10.5**
VCO Phase Noise (dBc/Hz) @ 1 MHz	-105.4♯	-105♯	-105 to -107.5♯	-	-	-	**-118.1**
IIP3 (dBm)	-6	-15.8 to -16.8	-12.5	-	-13.1	-7.5	**-14 to -15.5**
IRR (dB)	28	30.5 to 37.3	26.2	-	-	-	**23 to 27**
Voltage Gain (dB)	55	55.5 to 56.1	34.5	68	43.1	61	**57**
BB Style	With I/Q	With I/Q	With I/Q	Without I/Q	With I/Q	With I/Q	**With I/Q**
BB Filtering	3 Complex Poles	2 Complex Poles	3 Real Poles	LPF + PGA	4th-order Butterworth	FIR Filter	**2 Complex Poles**
Active Area (mm²)	0.3	0.25	1.65	1.64♮	1.9♮	0.5	**0.75**
CMOS Tech.	65 nm	130 nm	28 nm	65 nm	22 nm FDSOI	22 nm FDSOI	**180 nm**

* Estimated from power break down, e.g. w/o VCO/PLL. different offset.   ♮ Includes more than RX path.   ♯ Normalized or estimated from phase noise plot reported at

Fig. 12.   Die micrograph.

Fig. 13.   Proposed design flow for Blixator circuit.
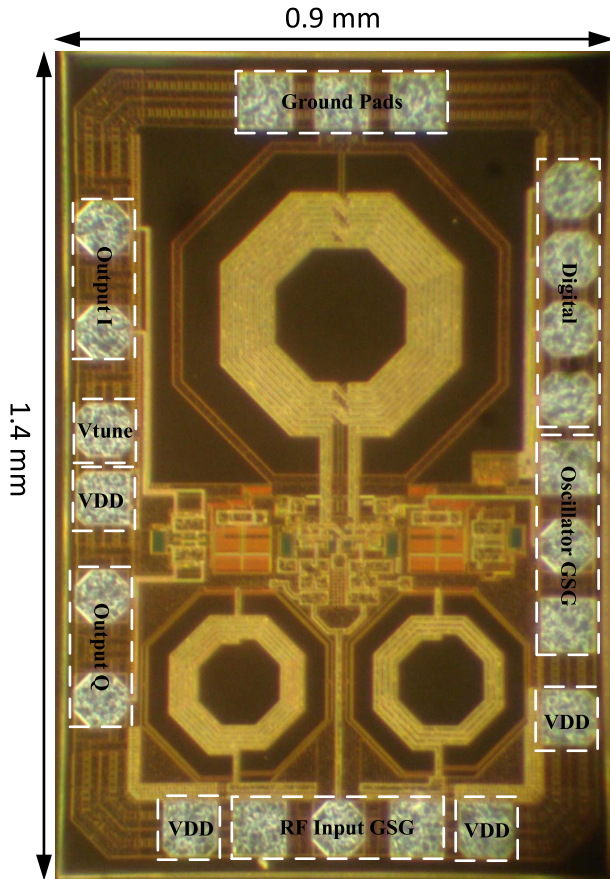
photograph is shown in Fig. 12. All used RF transistors in the Blixator circuit are thin-oxide low-V_{th} devices. A low-

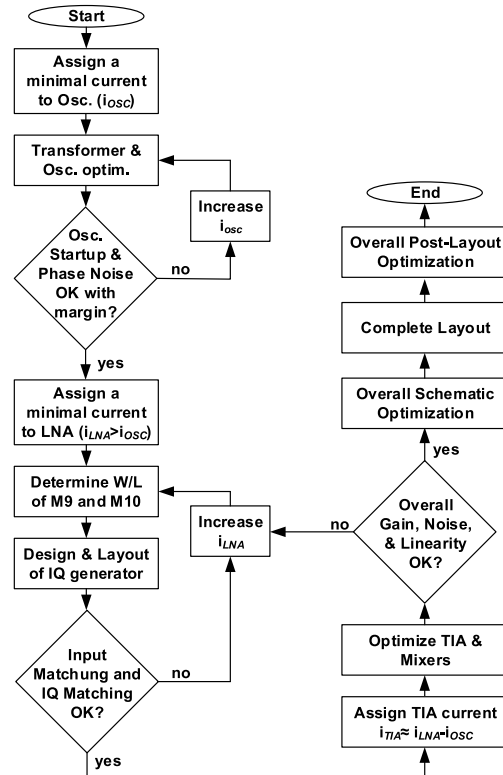IF architecture is chosen, with an IF center frequency of 2 MHz and a channel bandwidth of 1 MHz. Only two inductors and one transformer are exploited, resulting in a modest area occupation, without requiring any external component. The quadrature differential signals are produced on-chip to not
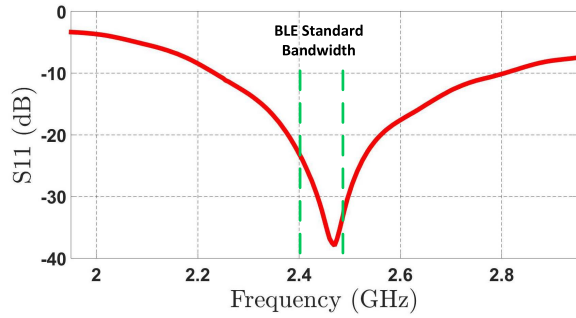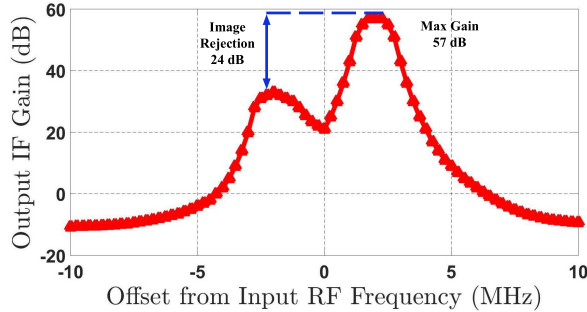
Fig. 14.   Measured input impedance matching (S_{11}).

Fig. 15.   Measured ac transfer function of the Blixator circuit.

Fig. 16.   Gain and image rejection versus BLE channel index.

Fig. 17.   IIP3 and NF versus BLE channel index.

only minimize common-mode signals induced by parasitics but also to provide good image rejection characteristics. Large on-chip supply bypass MOS capacitors are used to filter the supply noise. Fig. 13 shows a flow graph, which summarizes the design steps for the proposed RF receiver front end. As it is clear, the main goal is to minimize the power consumption while meeting the other BLE specifications. The main step is to assign minimum current to oscillator without start-up issue. Using a huge transformer (with enough quality factor) increases the parallel resistance of the tank. The transformer is designed based on extensive EM simulations. Linewidth, number of turns, line spacing, and inner radius of transformer have been optimized to obtain the highest possible quality factor. Consequently, lower trans-conductance is needed to compensate for the loss of the tank, resulting in lower required power consumption. Moreover, exploiting the signal amplification, caused by the transformer, enhances the mixer drive. This either improves the conversion gain or relaxes the required oscillator's power to maintain the same mixer drive.

Table III shows the current consumption of all blocks in the circuit. The TIA shares its current with the Blixator core, which consumes a total current of 322 μA. This current is absorbed by the balun-LNA and divided between VCO and the TIAs. Because of the used low-power oscillator topology and due to the used multi-turn 4:5 transformer, the VCO requires only 222 μA. The circuit is simulated in many corner cases to obtain the worst case scenario (SS corner $-40°$) for oscillator start-up. While the voltage swing is reduced to ± 0.1 V, the receiver is still functional. Although simulations show that the conversion gain slightly reduces (less than 2 dB), the proposed Blixator cell still meets the BLE specs. Also, in the typical corner, the supply voltage is reduced from 0.8 to 0.7 V and the oscillator spectrum is checked. While the oscillator still starts up, the phase noise has been degraded but still meets the BLE
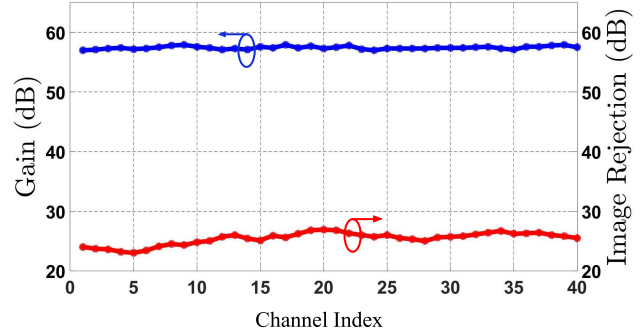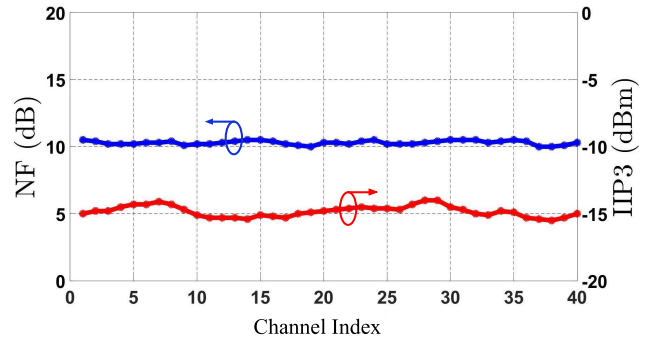
requirement of -105 dBc/Hz at 3 MHz. Consequently, it can be concluded that the proposed transformer-based oscillator and the mixed structure can safely operate with these levels of power, with no start-up issue. It should be noted that (in worse case) the oscillator start-up and the required amplitude can be guaranteed by exploiting the amplitude detection and control methods and tuning the biasing current [38], [39].

Tuning the oscillator makes it possible to select the desired IF channel. An 18% tuning range is provided for the oscillator to ensure covering of all BLE channels.

B. Measurement Results

The RF input pad is wire-bonded to the 50-Ω trace, which is connected to the Keysight E5071C vector network analyzer for S_{11} measurements. Fig. 14 shows the measured S_{11} of the proposed low-power receiver, showing a desirable return loss of better than 15 dB, over the entire BLE band. Fig. 15 shows the measured transfer function of the receiver, at the maximum gain, by sweeping the RF input frequency with respect to the LO frequency, for the first BLE channel. The results show a maximum gain of 57 dB, with less than 1-dB variations, and a minimum image rejection of 24 dB across the channel bandwidth. Fig. 16 reports the gain and image rejection measurements for all BLE channels. The gain variation is less than 1 dB across the BLE channels, which shows that the receiver bandwidth is sufficiently wide to operate in the entire ISM band. The measured image rejection varies from 23 to 27 dB, which is well above the required 21 dB for the BLE standard. Fig. 17 shows the NF and IIP3 measurements. The NF ranges between 10 and 10.5 dB that corresponds to an equivalent receiver sensitivity of better than -89.5 dBm. Measured using the two-tone intermodulation
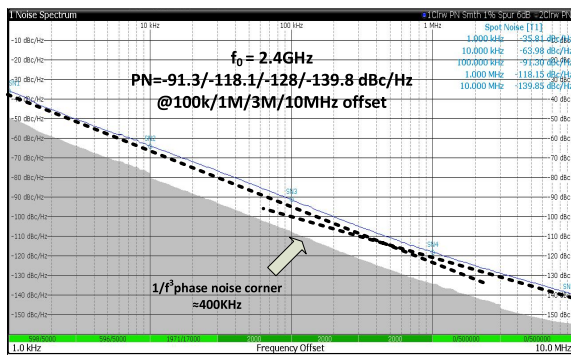
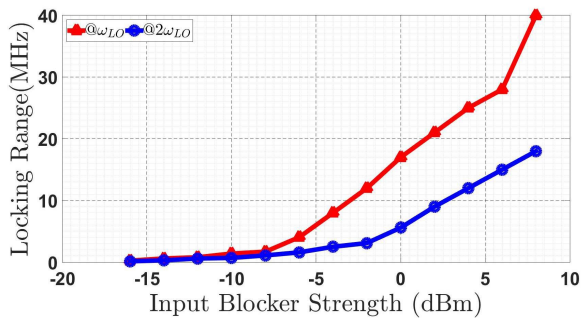Fig. 18. Blixator phase noise measurement at 1-kHz–10-MHz frequency offsets.

Fig. 19. Injection locking susceptibility due to blockers at ω_{LO} and $2\omega_{LO}$.

test, the IIP3 varies between -15.5 and -14 dBm over the entire channels. Open-drain buffers are embedded on chip at the oscillator outputs for phase noise measurements. The output of one of the buffers was wire-bonded to a 50-Ω trace on the test board, whereas the other one was terminated by a 50-Ω on-chip resistor. The 50-Ω trace was connected to Rohde & Schwarz FSWP signal-source analyzer for phase noise measurement. Fig. 18 shows the measured phase noise of Blixator for a 2.4-GHz carrier. The measured phase noise of the receiver is -118.1 dBc/Hz at 1-MHz offset, completely meeting the requirements of BLE standard. Fig. 19 reports the susceptibility of the Blixator cell to nearby blockers at ω_{LO} and $2\omega_{LO}$. Due to the selectivity of the input matching network and topology of the receiver, the Blixator cell is well immune against RF port blockers. The measurements show that at a frequency offset of 1 MHz, the oscillator can be locked only with an input power of -8.5 dBm, which is well above the saturation point of the Blixator receiver.

Table IV summarizes the performance of the Blixator receiver and compares it with some recent state-of-the-art works. Employing only two inductors and one transformer and by using circuit and current-reuse techniques, the Blixator is successful to minimize the total power consumption of the chip. It should be noted that by exploiting lower technology nodes, the power consumption can be even further reduced. As it can be seen from Table IV, the best phase noise performance is achieved, with only 340-μW power consumption, while all requirements of the BLE standards are satisfied with reasonable margins.

VII. CONCLUSION

A quadrature current-reuse receiver RF front end for low-power applications, consuming only 340 μW from a 0.8-V

supply voltage, has been reported. Exploiting current and circuit reuse techniques in the introduced Blixator circuit makes it possible to merge multiple functionalities at low power consumption. The proposed receiver has been completely analyzed, the equations describing gain, impedance matching, NF, and phase noise have been derived, and oscillator locking range has been investigated. Implemented in a 0.18 μm CMOS technology node, the proposed receiver achieves the lowest power consumption among state-of-the-art works while occupying small footprint and meeting all the specifications of the BLE standard with reasonable margins.

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