IEEE Open Journal of the
Industrial Electronics Society

Received 21 October 2025; revised 28 November 2025; accepted 7 December 2025. Date of publication 26 December 2025;
date of current version 9 January 2026. The review of this article was arranged by Associate Editor Binbin Li.

Digital Object Identifier 10.1109/OJIES.2025.3648255

New Nine-Level Common-Ground Multilevel Inverter With Boosting Capability for Renewable Energies

MAYSAM ABBASI [1] (Member, IEEE), MILAD GHAVIPANJEH MARANGALU [2] (Member, IEEE), NASER VOSOUGHI KURDKANDI [3] (Member, IEEE), EHSAN ABBASI [2] (Member, IEEE), HANI VAHEDI [4] (Senior Member, IEEE), LI LI [1] (Senior Member, IEEE), RICARDO P. AGUILERA [1] (Member, IEEE), DYLAN LU [1] (Senior Member, IEEE), AND FEI WANG [5] (Senior Member, IEEE)

[1]School of Electrical and Data Engineering, University of Technology Sydney, Broadway, NSW 2007, Australia
[2]Department of Electrical Engineering, University of Tabriz, Tabriz 51666, Iran
[3]Department of Electrical and Computer Engineering, San Diego State University, San Diego, CA 92182 USA
[4]Department of Electrical Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands
[5]Department of Electrical Engineering, Shanghai University, Shanghai 200444, China

CORRESPONDING AUTHOR: MAYSAM ABBASI (e-mail: maysam.abbasi@alumni.uts.edu.au).

ABSTRACT In recent years, several common-ground switched-capacitor transformerless (CGSC-TL) dc–ac multilevel power converters have been introduced, providing advantages such as multilevel output voltage, voltage boosting, and mitigated leakage current. However, these structures mostly suffer from drawbacks, such as limited output voltage levels (like only five levels), lack of voltage-boosting capability, and high charging current spikes of the capacitors. This article proposes a new single-stage CGSC-TL nine-level (9L) multilevel inverter (MLI) with voltage-boosting capability and limited spikes of charging current of the capacitor, designed to be employed as a single-stage power-electronics-based interface device between renewable energy sources, such as photovoltaic (PV) systems and power grid and/or load. The proposed MLI provides several merits, such as a common-ground structure that suppresses PV-to-ground leakage current associated with PV parasitic capacitances, active and reactive power support, a wide input voltage range, and higher output voltage levels (9L) compared with other structures in the same class. Comprehensive comparative analyses, as well as simulation and experimental results, are presented to verify the performance of the proposed inverter.

INDEX TERMS Common ground (CG), current spikes, leakage current elimination, multilevel dc–ac inverter, renewable energy, single stage, solar energy, switched capacitor (SC), voltage boosting.

I. INTRODUCTION

These days, power-electronics-based devices such as power converters are broadly employed in many industrial applications [1], [2], [3], [4]. In recent years, among several types of power converters, multilevel inverters (MLIs) have attracted much attention and have been broadly employed in numerous medium- and high-power applications such as renewable energy source (RES)-based systems such as electric vehicles, photovoltaic (PV) systems [5], [6], [7], [8], and flexible ac transmission systems [9], [10]. With the growing penetration of RESs in power systems, transformerless (TL) inverters with common-ground (CG) structures have been widely studied for grid-connected applications. These topologies are credited with suppressing leakage current, improving overall efficiency, and providing favorable power density relative to both size and cost. It is noteworthy that in these inverters, the leakage current is eliminated since their input dc voltage source and the grid/load have a CG [11], [12], [13], i.e., their negative and neutral points are connected. On the other hand, ensuring compatibility between the grid-voltage peak value and the dc

voltage source from renewable resources such as PV string panels is another important objective. In addition, as another objective, the power quality enhancement (PQE) problem should be considered here. The PQE has an undeniable impact on both the filter design and the quality of the current injected into the main grid [11]. So far, several TL inverters with a CG structure have been introduced, which are capable of providing a static voltage gain (equal to one) [14], [15].

In such topologies, a dc-link capacitor is required and is charged during the first half-cycle and discharged during the second half-cycle of the grid voltage. During the second half-cycle, the voltage stored in the first half-cycle is delivered to the output port. However, these inverters typically provide only two or three output voltage levels, which can adversely affect PQE. In [16] and [17], two- and three-level (2L and 3L) TL inverters with the CG feature have been, respectively, developed. A flying inductor is used in these topologies rather than the virtual dc-link capacitor. In [18], a five-level (5L) CG-based TL inverter has been introduced, which is not based on the virtual dc-link capacitors or flying inductor concepts. This inverter employs an inductor-based switched-boost (SB) module with a dc-link capacitor-based dual T-Type cell. All these structures achieve the feature of dynamic voltage gain, which is an invaluable achievement in single-stage energy conversion operations. However, these converters are large due to their flying or SB-module-based inductors and may cause an inappropriate total power density per output power.

To enhance the static voltage gain, flying capacitors and/or switched-capacitor (SC) networks can be incorporated into conventional CG-TL inverters, including the 3L designs of [19] and [20], the 5L designs of [21] and [22], and the seven-level (7L) design of [23]. With these integrations, fewer PV modules are required on the dc side to meet the grid-voltage amplitude. However, achieving this boosting capability is accompanied by undesirable charging current spikes that occur when the capacitors are charged in parallel with the dc input source [24], [25]. Consequently, the applicability of CGSC-TL inverters is constrained for low-power grid-connected systems. Recent CGSC-TL implementations typically provide only a 5L output voltage. Adopting an extendable structure is therefore advantageous, as it enables a higher number of output voltage levels and yields notable improvements in PQE and reliability [26].

In summary, for PV grid-tied systems, several CG-TL inverter topologies have been introduced to eliminate leakage current while maintaining high efficiency [11], [12], [13], [14], [15]. However, early CG structures were mainly limited to 2L or 3L output voltages [16], [17], leading to poor output quality and large filter requirements. To overcome this, multilevel CG inverters with SC or SB modules were developed [18], [19], [20], [21], [22]. These inverters can offer higher output voltage levels and voltage-boosting capability. Nevertheless, they often suffer from drawbacks, such as excessive charging current spikes in capacitors, increased device stress, and limited scalability [23], [24], [25], [26].

Recently, several advanced CG-SC inverter topologies have emerged. Azad et al. [27] introduced a 9L CG-SC inverter that effectively suppresses leakage currents, although its boosting gain and device count remain limiting factors. In [28], a 7L CG inverter with triple boosting and natural voltage balancing is presented, suffering from higher capacitor stress. Moreover, in [29], a self-balanced CG-SC inverter with a single dc source is introduced, but its voltage gain is restricted to lower values. Liu et al. [30] addressed dc bias and asymmetry in CG-SC inverters, focusing on waveform quality without considering boosting limitations. In 2025, a single-source 7L CG inverter was introduced, demonstrating good leakage suppression but still limited in boosting [31]. More recently, a CG boosting inverter with lower switch stress is presented in [32]; however, this structure faces tradeoffs in terms of increased switching losses.

Based on the literature, while progress has been made in integrating boosting, leakage elimination, and CG features, there is still a need to develop a topology that can simultaneously provide advantages such as a high number of output voltage levels (equal to or higher than nine), substantial boosting gain (approximately $2\times$), elimination of leakage current, suppression of capacitor charging current spikes, and a competitive component count with moderate device stresses. For this aim, this article proposes a new CGSC-TL MLI, employing eight power switches for modern applications such as RESs. This inverter can provide nine voltage levels at the output port, which is higher than most of the previously introduced structures, with fewer or a comparable number of power components. The main advantages of the proposed MLI can be listed as follows:

1) employing fewer/comparable number of components;
2) being CG, leading to leakage current elimination;
3) voltage-boosting ability;
4) active and reactive power supporting capability;
5) limited capacitors' charging current spikes (CCCS) resulting in lower power losses, longer life cycle for capacitors, and mitigated electromagnetic interference (EMI);
6) extensive input voltage capability;
7) TL structure;
8) no sensors for balancing the voltages of capacitors;
9) lower or similar voltage stress on the components.

Clearly, these advantages make the proposed MLI a strong candidate for modern industrial applications such as PV applications. It is noteworthy that compared to previously published MLIs, the proposed MLI is a 9L SC-TL MLI that simultaneously provides both CG and CCCS features. For validating the performance of the converter, thorough analysis, comparisons, and simulation and experimental results are presented.

The rest of this article is organized as follows. Section II introduces the proposed inverter and its operating principles. Section III provides detailed comparisons with existing topologies. Section IV discusses the simulation and experimental results. Finally, Section V concludes this article.

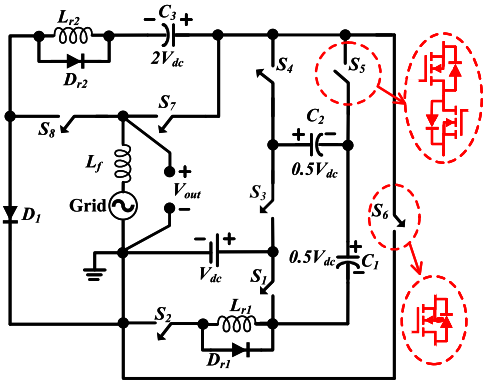


FIGURE 1. Circuit configuration of the proposed CGSC-TL 9L MLI.

II. PROPOSED INVERTER AND ITS OPERATING PRINCIPLES

Here, the configuration, operating principles, and main analysis of the proposed MLI are presented.

A. PROPOSED 9L MLI

In Fig. 1, the circuit configuration of the proposed CGSC-TL MLI is presented. This topology can generate a 9L output voltage by employing a new SC cell consisting of eight power switches and three diodes. It is noteworthy that the switches used here include seven unidirectional (S_1, S_2, S_3, S_4, S_6, S_7, and S_8) and one bidirectional switch (S_5). Here, it is essential to use this bidirectional switch due to its bipolar voltage stress. To obtain boosting capability for the proposed inverter, three capacitors (C_1, C_2, and C_3), paralleled with a single input dc source (V_{dc}), are used in this MLI, as seen in Fig. 1. Besides, for reducing the capacitor current spikes as one of the main problems in SC-based inverters, this MLI employs two units, including one inductor paralleled with one diode (L_{r1} with D_{r1} and L_{r2} with D_{r2}), in the capacitors' charging current path. As seen in Fig. 1, the grid neutral point is directly connected to the negative terminal of the source, classifying this MLI as a CG inverter. This feature, important for TL grid-tied systems, enables the mitigation of the leakage current in this MLI. Furthermore, both reactive and active power exchange with the grid are supported.

B. OPERATING MODES

The operating modes of the proposed MLI are presented and discussed here. Fig. 2 illustrates these modes along with their current paths. In each charging mode, the capacitors C_1 and C_2 are charged to $0.5V_{dc}$, while the capacitor C_3 is charged to $2V_{dc}$. Detailed descriptions of the operating modes are provided in the following.

1) MODE 1

The first operating mode for both half-cycles is illustrated in Fig. 2(a). In the negative half-cycle ($V_{zero,N}$), the zero voltage level is produced with S_8 and D_1 conducting. In the positive half-cycle ($V_{zero,P}$), the zero level is obtained with S_1, S_4, and

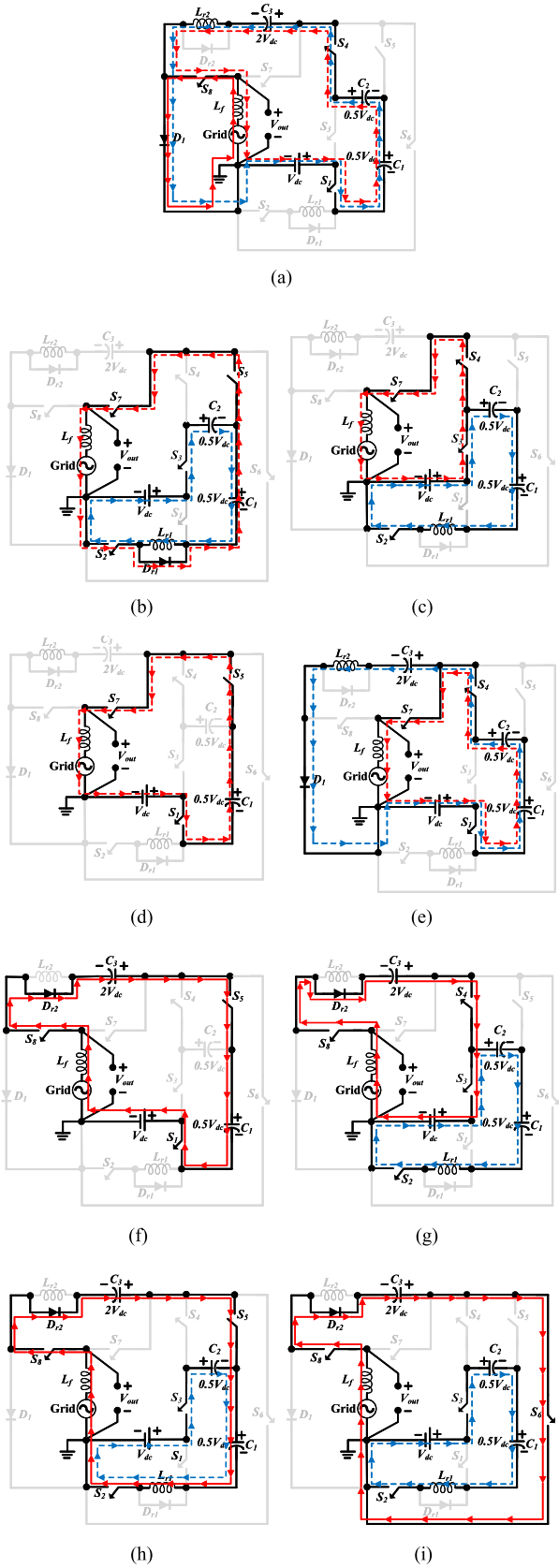


FIGURE 2. Operating modes of the proposed MLI. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7. (g) Mode 8. (i) Mode 9.

S_8 turned ON. With S_1, S_4, and D_1 ON, the charging loop is formed, as indicated by the blue dashed path in Fig. 2(a). In this configuration, C_3 is connected in series with C_1, C_2, and the input dc source, thereby allowing C_3 to be charged to $2V_{\text{dc}}$. The voltage relations for this operating mode are given as follows:

$$V_{C3} = V_{C1} + V_{C2} + V_{\text{dc}} = 2V_{\text{dc}} \tag{1}$$

$$V_{\text{zero},N} = 0 \tag{2}$$

$$V_{\text{zero},P} = -V_{\text{dc}} - V_{C1} - V_{C2} + V_{C3} = 0. \tag{3}$$

2) MODE 2

The second operating mode, which provides the first output voltage level in the positive half-cycle, is illustrated in Fig. 2(b). In this mode, S_2, S_5, S_7, and D_{r1} are turned ON. To charge C_1 and C_2 to $0.5V_{\text{dc}}$, S_2 and S_3 are placed in conduction. During the charging interval, the capacitors' charging current (blue dashed path) flows through L_{r1}, thereby limiting the charging spike. In this mode, C_3 is isolated from both the dc and ac sides. The stored energy in C_1 is delivered to the output, establishing the first voltage level in the positive half-cycle. The voltage relations for this mode are given as follows:

$$V_{Ci} = 0.5V_{\text{dc}} \quad \text{for} \quad i = 1, 2 \tag{4}$$

$$V_{\text{out}} = V_{C1} = 0.5V_{\text{dc}}. \tag{5}$$

3) MODE 3

Mode 3 is shown in Fig. 2(c). The second output voltage level in the positive half-cycle is obtained by directly connecting the dc source (V_{dc}) to the output with S_3, S_4, and S_7 turned ON. In this mode, no capacitor is included in the load current path (red dashed line). As indicated in Fig. 2(c), C_1 and C_2 are recharged to $0.5V_{\text{dc}}$ ($V_{C2} = V_{C1} = 0.5V_{\text{dc}}$) by switching S_2 and S_3 ON. The voltage equations for this mode are given as follows:

$$V_{\text{out}} = V_{\text{dc}}. \tag{6}$$

4) MODE 4

As illustrated in Fig. 2(d), the third output voltage level in the positive half-cycle is obtained with S_1, S_5, and S_7 turned ON. The output voltage is obtained by summing the voltages of the capacitor C_1 and the dc source, that is, $V_{\text{out}} = 1.5V_{\text{dc}}$. In this mode, C_1 is in discharging operation, while C_2 and C_3 are isolated from the circuit. The voltage relation for this mode is expressed as follows:

$$V_{\text{out}} = V_{\text{dc}} + V_{C1} = 1.5V_{\text{dc}}. \tag{7}$$

5) MODE 5

This mode's equivalent circuit is illustrated in Fig. 2(e), where the fourth output voltage level in the positive half-cycle is generated. In this condition, D_1, S_1, S_4, and S_7 are conducting, and the output voltage is formed by adding the voltages of C_1, C_2, and the dc source. In this mode, C_3 is being charged. The voltage relation for this mode is obtained by the following equation:

$$V_{\text{out}} = V_{C1} + V_{C2} + V_{\text{dc}} = 2V_{\text{dc}}. \tag{8}$$

6) MODE 6

Fig. 2(f) illustrates this operating condition, under which the first negative output level ($-0.5V_{\text{dc}}$) is produced. In this configuration, S_1, S_5, S_8, and D_{r2} are placed in the ON state, and C_1 and C_3, together with the input source, are connected in series and applied to the inverter output port. As shown in Fig. 2(f), C_2 remains isolated from the circuit. The voltage relation for this mode can be written as follows:

$$V_{\text{out}} = -V_{C3} + V_{C1} + V_{\text{dc}} = -0.5V_{\text{dc}}. \tag{9}$$

7) MODE 7

This operating condition is depicted in Fig. 2(g), wherein the second output voltage level during the negative half-cycle is established with S_3, S_4, S_8, and D_{r2} placed in the ON state. As indicated in Fig. 2(g), activation of S_2 and S_3 connects C_2 and C_1 to the dc source, and each capacitor is charged to $0.5V_{\text{dc}}$. During this charging interval, the blue dashed current path is routed through L_{r1}, by which the charging spike is limited. In the same mode, C_3 operates in discharge. The output voltage for this mode is therefore obtained as follows:

$$V_{\text{out}} = V_{C1} - V_{C3} + V_{C2} = -V_{\text{dc}}. \tag{10}$$

8) MODE 8

The eighth operating mode of the proposed MLI is illustrated in Fig. 2(h) and generates the third negative level of the output voltage waveform. In this condition, C_1 and C_3 are placed in series with S_2, S_5, S_8, and D_{r2} conducting. In addition, S_3 is held ON, whereby C_2 and C_1 are charged. Accordingly, the inverter output-port voltage is given by the following relation:

$$V_{\text{out}} = -V_{C3} + V_{C1} = -1.5V_{\text{dc}}. \tag{11}$$

9) MODE 9

In this mode, the fourth output voltage level during the negative half-cycle is provided. This operation is depicted in Fig. 2(i), where S_6, S_8, and D_{r2} are turned ON, thereby discharging C_3 to the inverter output port. Consequently, the peak output voltage equals twice the dc source voltage, which realizes the voltage-boosting feature of the proposed MLI. Meanwhile, with S_2 and S_3 ON, C_1 and C_2 are placed in series with the dc input source and brought to $0.5V_{\text{dc}}$ (blue dashed path). During this interval, C_3 remains in discharging operation. The voltage equations for this mode are given as follows:

$$V_{C1} = V_{C2} = 0.5V_{\text{dc}} \tag{12}$$

$$V_{\text{out}} = -V_{C3} = -2V_{\text{dc}}. \tag{13}$$

Table 1 lists the operational modes of the proposed MLI and related switching states, figures, and equations.

TABLE 1. Operational Modes of the Proposed MLI and Related Switching States, Figures, and Equations

Modes	Generated output voltage			On-state Switching devices	Capacitors in charging state	Disconnected capacitors	Figure	Voltage equations
	level	+/- half-cycle	Value					
1	Zero	+	$V_{out} = V_{zero,P} = 0$	S_1, S_4, S_8, D_1	C_3	NA	Fig. 2(a)	(1),(2),(3)
		-	$V_{out} = V_{zero,N} = 0$	S_1, S_4, S_8, D_1	C_3	NA		NA
2	1st	+	$V_{out} = 0.5V_{dc}$	$S_2, S_5, S_7, D_{r1}, S_3$	C_1, C_2	C_3	Fig. 2(b)	(4),(5)
3	2nd	+	$V_{out} = V_{dc}$	S_2, S_3, S_4, S_7	C_1, C_2	C_3	Fig. 2(c)	(6)
4	3rd	+	$V_{out} = 1.5V_{dc}$	S_1, S_5, S_7	NA	C_2, C_3	Fig. 2(d)	(7)
5	4th	+	$V_{out} = 2V_{dc}$	D_1, S_1, S_4, S_7	C_3	NA	Fig. 2(e)	(8)
6	1st	-	$V_{out} = -0.5V_{dc}$	S_1, S_5, S_8, D_{r2}	C_1	C_2	Fig. 2(f)	(9)
7	2nd	-	$V_{out} = -V_{dc}$	$D_{r2}, S_2, S_3, S_4, S_8$	C_1, C_2	NA	Fig. 2(g)	(10)
8	3rd	-	$V_{out} = -1.5V_{dc}$	$S_2, S_3, S_5, S_8, D_{r2}$	C_1, C_2	NA	Fig. 2(h)	(11)
9	4th	-	$V_{out} = -2V_{dc}$	$S_2, S_3, D_{r2}, S_6, S_8$	C_1, C_2	NA	Fig. 2(i)	(12),(13)

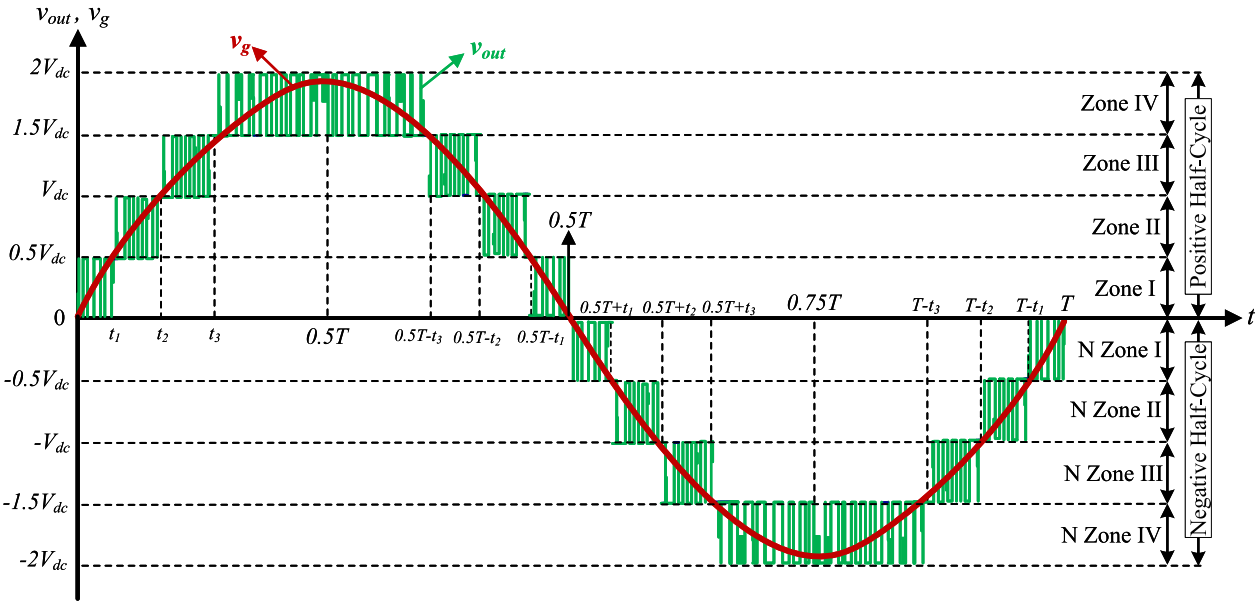


FIGURE 3. Output voltage of the proposed MLI, the grid voltage, and the operating zones of the proposed MLI.

C. DUTY CYCLE CALCULATIONS FOR SWITCHES

In this section, the switching duty cycles for the various operating modes of the proposed MLI are derived. Fig. 3 depicts the voltage waveform of the inverter output and the grid over both half-cycles, with four zones defined for each half-cycle (Zones I–IV for the positive half-cycle and N Zone I–N Zone IV for the negative half-cycle). The inverter maximum switching frequency and the sampling frequency are denoted by f_S and f_{SA}, respectively, with $f_{SA} = 2f_S$. By applying the inductor volt–second balanced (IVSB) method to the voltage across the output-filter inductor (L_f) over the full switching period (T_S), the duty cycles for these zones are obtained by (16)–(27). Generally, the grid voltage and current can be, respectively, written as follows:

$$v_g(t) = V_{g,\max} \sin(\omega t) \tag{14}$$

$$i_g(t) = I_{g,\max} \sin(\omega t). \tag{15}$$

Note that V_{out}, i_g, and v_g, respectively, denote the inverter's output voltage and the grid's current and voltage. In addition, $I_{g,\max}$, and $V_{g,\max}$, respectively, present the maximum values of the grid's current and voltage.

1) ZONE I

As indicated in Fig. 3, the inverter output voltage in this zone lies between 0 and $0.5V_{\text{dc}}$. By applying the IVSB principle to the output inductor voltage over the sampling interval, the inverter duty cycle $d_1(t)$ is obtained as (16)–(18) for $0 \le t < t_1$

$$\int_0^{d_1 T_S} (-v_g + 0.5V_{\text{dc}})\, dt + \int_{d_1 T_S}^{T_S} (-v_g)\, dt = 0 \tag{16}$$

$$d_1(t) = \frac{v_g}{0.5V_{\text{dc}}}. \tag{17}$$

Using (14) in (17), the duty cycle of Zone I is acquired as follows:

$$d_1(t) = \frac{2V_{g,\max} \sin(\omega t)}{V_{\text{dc}}}. \tag{18}$$

TABLE 2. Applied PCC Operation Approach of Switching Pulses for Positive Half-Cycle

Zones	Positive half-cycle			
	Active power mode		Reactive power mode	
	$V_g > 0$ & $i_{ref} > 0$		$V_g > 0$ & $i_{ref} < 0$	
	$i_g > i_{ref}$	$i_g < i_{ref}$	$i_g < i_{ref}$	$i_g > i_{ref}$
Zone I: $0 < V_g < 0.5V_{dc}$	S_1, S_4, S_8	S_2, S_3, S_5, S_7	S_2, S_3, S_5, S_7	S_1, S_4, S_8
Zone II: $0.5V_{dc} < V_g < V_{dc}$	S_2, S_3, S_5, S_7	S_2, S_3, S_4, S_7	S_2, S_3, S_4, S_7	S_2, S_3, S_5, S_7
Zone III: $V_{dc} < V_g < 1.5V_{dc}$	S_2, S_3, S_4, S_7	S_1, S_5, S_7	S_1, S_5, S_7	S_2, S_3, S_4, S_7
Zone IV: $1.5V_{dc} < V_g < 2V_{dc}$	S_1, S_5, S_7	S_1, S_4, S_7	S_1, S_4, S_7	S_1, S_5, S_7

2) ZONE II

As seen in Fig. 3, in Zone II, the inverter's output voltage lies between $0.5V_{\rm dc}$ and $V_{\rm dc}$. By applying the IVSB principle to the output-filter inductor's voltage over the sampling interval, the duty cycle ($d_2(t)$) is obtained, for $t_1 \le t < t_2$, as follows:

$$\int_0^{d_2T_S} (-v_g + V_{\rm dc})\,dt + \int_{d_2T_S}^{T_S} (-v_g + 0.5V_{\rm dc})\,dt = 0 \quad (19)$$

$$d_2(t) = \left(2(\frac{v_g}{V_{\rm dc}}) - 1\right) = \left(\frac{2V_{g,\max}\sin(\omega t)}{V_{\rm dc}} - 1\right). \quad (20)$$

Considering (18), (20) can be rewritten as

$$d_2(t) = d_1(t) - 1. \quad (21)$$

3) ZONE III

As indicated in Fig. 3, the inverter output voltage in Zone III lies between $V_{\rm dc}$ and $1.5V_{\rm dc}$. By applying the IVSB principle to the output-filter inductor voltage over the sampling interval, the duty cycle $d_3(t)$ is obtained, for $t_2 \le t < t_3$, as follows:

$$\int_0^{d_3T_S} (1.5V_{\rm dc} - v_g)\,dt + \int_{d_3T_S}^{T_S} (V_{\rm dc} - v_g)\,dt = 0 \quad (22)$$

$$d_3(t) = \left(\frac{2v_g}{V_{\rm dc}} - 2\right) = \left(\frac{2V_{g,\max}\sin(\omega t)}{V_{\rm dc}} - 2\right). \quad (23)$$

Using (20), (23) can be expressed as follows:

$$d_3(t) = d_2(t) - 1. \quad (24)$$

4) ZONE IV

As illustrated in Fig. 3, the inverter's output voltage in Zone IV lies between $1.5V_{\rm dc}$ and $2V_{\rm dc}$. By applying the IVSB principle to the output-filter inductor voltage over the sampling interval in this zone, the duty cycle $d_4(t)$ is obtained, for $t_3 \le t < (\frac{T}{2} - t_3)$, as follows:

$$\int_0^{d_4T_S} (2V_{\rm dc} - v_g)\,dt + \int_{d_4T_S}^{T_S} (1.5V_{\rm dc} - v_g)\,dt = 0 \quad (25)$$

$$d_4(t) = \frac{2v_g - 3V_{\rm dc}}{V_{\rm dc}} = \frac{2V_{g,\max}\sin(\omega t) - 3V_{\rm dc}}{V_{\rm dc}}. \quad (26)$$

Based on (23), (26) can be expressed as follows:

$$d_4(t) = d_3(t) - 1. \quad (27)$$

In (27), based on Fig. 3, t_k, where $k = 1, 2, 3$, can be defined as

$$t_1 = \frac{1}{\omega}\sin^{-1}\left(\frac{V_{g,\max}}{0.5k(V_{\rm dc})}\right). \quad (28)$$

In the proposed MLI, for handling both reactive and active powers and also generating the switches' gate pulses (S_1–S_8), the strategy of the peak current controller (PCC) is used [19]. Table 2 shows the applied PCC operating approach of switching pulses for the positive half-cycle. It is noteworthy that the switching zones of the negative half-cycle can be obtained by performing the similar done for the positive half-cycle.

As previously discussed, a key advantage of the proposed 9L MLI is its capability to inject power into the grid over a wide range of input dc voltages. In general, the boosting capability of the inverter imposes a first theoretical lower bound on the required dc-link voltage. This bound, however, is not sufficient on its own, because the highest output voltage level of the inverter before the output filter must exceed the grid peak voltage. For example, for a 220-V RMS grid (with a peak voltage of 311 V), this boosting-based criterion yields a theoretical minimum dc-link voltage of 156 V, whereas the actual dc-link voltage must be selected higher than this limit in order to satisfy the aforementioned design requirement. To verify this advantage, precise simulations have been performed using MATLAB/Simulink. The obtained results are presented in Fig. 4. This figure shows that the input voltage varies between 175 and 725 V. In proportion to this change, the output voltage changes from 9L to 3L, so that the proposed topology can properly inject power into the grid under this condition. As seen in Fig. 4, by step changing the input voltage from 175 to 250 V at $t = 120$ ms, the output voltage changes from 9L to 7L. In addition, this figure shows that changing the input voltage from 250 to 370 V at $t = 160$ ms changes the output voltage from 7L to 5L. Besides, when the input voltage changes from 550 to 625 V at $t = 240$ ms, the output voltage changes from a 5L to a 3L waveform; in other words, the proposed MLI can operate with a broad input voltage range if application requires it.

D. SIZING CAPACITORS AND OUTPUT FILTER

Initially, the capacitors of the proposed MLI are sized according to each device's longest discharging cycle (LDC). For C_1, C_2, and C_3, the LDC occurs during the positive and negative half-cycles, respectively. The peak discharging current for a

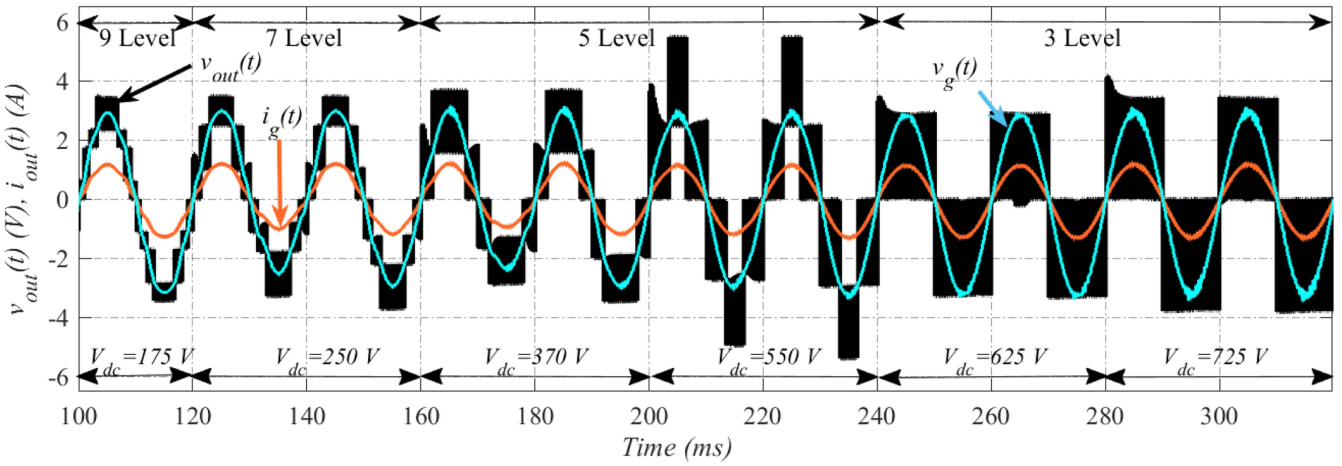


FIGURE 4. Simulation results of the proposed MLI for a wide input voltage.

capacitor over its LDC is obtained as

$$I_{\text{Cap}} = \frac{dQ_{\text{Cap}}}{dt} = \frac{d}{dt}\left(\int I_{\text{Cap}}dt\right). \tag{29}$$

Furthermore, the sizes of C_1, C_2, and C_3 are determined by calculation [33]. Here, $I_{g,\max}$ denotes the maximum amplitude of the injected current. In addition, ϕ is the phase shift between the injected current and the voltage of grid. The output voltage is modeled as a multilevel waveform; therefore, the maximum charge drawn from capacitor C_i during the half-cycle is given as follows:

$$Q_{Ci} = \int_{(\Delta t_i)} I_{g,\max}\sin(\omega t - \phi)dt \tag{30}$$

where $i = 1, 2, 3$; $I_{g,\max}$ is the peak injected grid current, T is the grid-voltage period, and the fundamental angular frequency of the output voltage is represented by ω. The interval Δt corresponds to the LDC of each capacitor, which differs for C_1, C_2, and C_3. With $\Delta V_{\max}$ taken as the permissible voltage ripple, the required capacitance satisfies the following:

$$C_{\text{opt},i} \geq \frac{Q_{C_i}}{\Delta V_{\max}}. \tag{31}$$

In the proposed system, the maximum current ripple of the output-filter inductor occurs at unity power factor and at the peak of the injected grid current ($t = T/4$). At $t = T/4$, the proposed MLI operates in mode 5 with $V_{\text{out}} = 2V_{\text{dc}}$. Over one switching period, the inductor current is obtained as

$$i_{Lf}(t) = \frac{1}{L_f}\int_0^t V_{Lf}dt + i_{Lf}(0) \tag{32}$$

where V_{Lf} is the output-filter voltage. From (32), the output-filter current ripple is calculated as follows:

$$\Delta I_{Lf} = i_{Lf}(d_4T_s) - i_{Lf}(0) = \frac{(2V_{\text{dc}} - V_g)d_4(t)}{L_f f_S} \tag{33}$$

with $d_4(t)$ the Zone IV duty cycle given in (26). Accordingly, L_f is obtained as

$$L_f = \frac{4V_{g,\max}\sin(\omega t) - 6V_{dc} + 3V_{g,\max}\sin(\omega t)}{\Delta I_{Lf} f_S} - \frac{2(V_{g,\max}\sin(\omega t))^2}{\Delta I_{Lf} f_S V_{\text{dc}}}. \tag{34}$$

For the maximum inductor current ripple, L_f evaluates to

$$L_f = \frac{7V_{g,\max} - 6V_{\text{dc}}}{\Delta I_{Lf,\max} f_S} - \frac{2(V_{g,\max})^2}{\Delta I_{Lf,\max} f_S V_{\text{dc}}}. \tag{35}$$

III. COMPARISON

Here, the proposed 9L MLI is thoroughly compared with different previously published MLIs employing a single dc input source. Table 3 lists the main parameters and characteristics of the MLIs involved in this section. In Table 3, $V.G$, L_V, N_S, N_C, and N_D, respectively, denote the voltage gain, and the number of output voltage levels, capacitors, diodes, and switches. In addition, NA, NP, and CCCS, respectively, stand for Not Applicable, Not Provided, and Capacitors' Charging Current Spikes. As seen, the proposed inverter uses even comparable number of switching devices compared to some of the MLIs, providing fewer output voltage levels. For instance, the proposed MLI employs eight switches, which is less than or comparable to that of 5L MLI of [33], and 7L MLIs of [34], [35], and [36]. It is worth noting that apart from [23], other 5L and 7L MLIs have a switch-per-level ratio (N_S/L) larger than 1. Clearly, this ratio for the proposed MLI is less than 1.

To compare the proposed MLI fairly, the main focus should be on the MLIs with similar output voltage levels. As clearly seen, in most of the 9L SC-based MLIs, including [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], the number of switches is greater than their number of output voltage levels. In other words, the switch-per-level ratio (N_S/L) of these MLIs is greater than 1. In the case of inverters of [48], [49], [50], and [51], this ratio is equal to 1. Among these MLIs,

TABLE 3. Comparing the Proposed MLI With the Previously Published Single-Phase MLIs

MLIs	L_V	N_S	N_D	N_C	$\frac{V_{ds,max}}{V_{o,max}}$	TSV_{sw}	TSV_d	$\frac{V_{C,max}}{V_{o,max}}$	$V.G$	NPC or CG	CCCS	C (mF)	f_s (kHz)	$V_{dc} \rightarrow V_{o,max}$ (V)	η% & P_o (W) & f_g (Hz)
[25]	5	6	2	2	1	4.5	1.5	1 + 0.5	2	Yes	No	1.0 + 0.47	20	180→360	98.2 & 600 & 50
[33]		9	0	1	0.5	4.5	NA	0.5	2	No	No	3.3	2.5	100→200	97.9 & NP & 50
[23]	7	6	4	3	1	4	2	1 + 0.67 + 0.33	3	Yes	No	0.22 × 2 + 4	25	130→390	96.13 & 800 & 50
[34]		10	0	1	0.67	6	NA	0.67	1.5	Yes	No	0.47	2.5	200→300	96.0 & 1000 & 50
[35]		9	0	2	1.33	7.667	NA	0.67 × 2	1.5	Yes	No	4.7 × 2	5	100→150	98.3 & 150 & 50
[36]		8	0	1	0.67	5.33	NA	0.67	1.5	Yes	No	4.4	- (ffm)	50→150	96.76 & 250 & 60
[37]	9	11	0	3	1	5.5	NA	0.5 × 2 + 0.25	4	No	No	4.3 × 2 + 2	20	80→320	96.0 & 1000*& 50
[38]		19	0	3	0.25	4.725	NA	0.25 × 3	4	No	No	4.7 × 3	2	48→192	88.93 & NP & 50
[52]		8	1	2	1	6.5	0.25	0.25 × 2	2	No	No	1.0 × 2	NP	200→400	95.5 & 1000 & 50
[39]		10	0	2	0.5	5.5	NA	0.25 × 2	2	No	No	4.7 × 2	2.5	160→320	NP & 400 & 50
[53]		8	4	4	1	4	1.5	0.5 × 2 + 0.25 × 2	4	No	No	2.3 × 2 + 4.7 × 2	4	70→280	92.75 & 1000 & 50
[54]		8	3	3	1	4	1.25	0.5 × 2 + 0.25	4	No	No	3.3 × 2 + 3.3	4	80→320	93.0 & 500 & 50
[48]		9	3	3	0.75	5.25	0.75	0.25 × 2 + 0.75	4	Yes	No	1.0 × 2 + 3.3	10	100→400	95.2 & 1000 & 50
[49]		9	0	4	1	5.5	NA	0.5 × 2 + 0.25 × 2	1	No	No	2.2 × 2 + 4.7 × 2	2.5	200→200	97.4 & 500*& 50
[40]		17	4	4	1	6	NP	0.25 × 4	4	Yes	No	4.7 × 4	5	40→227 (160 rms)	NP & 275 & 50
[41]		10	NA	3	0.5	5	NA	0.5 + 0.25 × 2	2	No	No	2.2 × 3	2.5	70→140	97.8 & 100 & 50
[55]		8	2	3	1	4.5	1	0.25 + 0.5 × 2	2	No	No	1.6 × 3	2	100→200	NP & NP & 50
[42]		10	3	3	1	5.5	0.75	0.25 × 3	4	No	Yes	4.7 × 3	3	80→320 (221.15 rms)	96 & 1400 & 50
[43]		12	0	2	0.5	5.25	NA	0.25 + 0.5	4	No	No	2.2 + 3.3	2.5×8 + (ffm) ×4	75→300	NP & 1500 & 50
[44]		11	0	3	0.5	5.25	NA	0.5 + 0.25 × 2	2	No	No	2.2 × 2 + 4.7	NP	100→200	95.5 & 250 & 50
[45]		10	3	2	0.5	4.5	1.25	0.5 + 0.25	4	No	No	4.7 + 3.3	HF×8 + (ffm) ×2	100→400	95.2 & 989.4 & 50
[46]		14	0	2	0.5	4.75	NA	0.5 + 0.25	4	No	No	2.2 × 2	2	30→120	93 & 250 & 50
[47]		10	0	2	0.5	5.5	NA	0.25 × 2	2	No	No	4.7 + 3.4	2.5	120→240	96.5 & 480 & 50
[50]		9	2	2	1	6.25	NP	0.25 × 2	2	No	No	1 + 1	40	200→400	96.4*& 1000*& 50
[51]		9	1	3	1	5	1	0.25 + 0.5 × 2	2	Yes	No	0.33 × 2 + 0.48	20	200→400	97.5 & 1200 & 400
[P]		8	3	3	1	5.25	1	1 + 0.25 × 2	2	Yes	Yes	1.0 × 2 + 2.2	20	200→400	97.9* & 250 & 50

TABLE 4. Parameters Used in the Simulations

Parameter	Symbol	Value
Grid Voltage (rms)	V_g	220 V
First and second Switched-Capacitor	C_1 & C_2	1.2 mF
Third Switched-Capacitor	C_3	2.2 mF
Grid Frequency	f_g	50 Hz
Switching Frequency	f_s	30 kHz
Output Filtering Inductor	L_f	2 mH
Charging Current's Spike Inductor	L_{r1} & L_{r2}	0.3 mH

the MLIs of [49] and [50] also do not have CG topologies. In terms of the number of power switches, the best MLIs are the proposed MLI and the inverters of [52], [53], [54], and [55]; the ratio of N_S/L is less than 1 for these converters. Although the number of switches employed by the inverters of [52], [53], [54], and [55] is equal to the proposed one, their structures are not CG, unlike the proposed MLI. This means that they (see [52], [53], [54], and [55]) cannot eliminate the leakage current of PV panels, making them inappropriate options for solar applications. According to Table 3, the proposed converter is the only inverter that provides both CCCS and CG features, leading to advantages like less EMI, longer life cycle for capacitors, and leakage current elimination. These merits make the proposed MLI the best option for modern industrial applications like solar systems among the MLIs in the same class.

As seen in Table 3, the ratio of maximum voltage stress on the components to the maximum value of the output voltage is used to have fair comparisons, i.e., $V_{ds,\max}/V_{o,\max}$ and $V_{C,\max}/V_{o,\max}$. Here, $V_{ds,\max}$, $V_{C,\max}$, and $V_{o,\max}$, respectively, denote the maximum voltage stress on the switches, maximum voltage stress on the capacitors, and the maximum output voltage value. According to Table 3, in terms of the ratio of maximum voltage stress on the power switches (with minimum and maximum values of 0.25 and 1.33) and the ratio of maximum voltages of the capacitors (with minimum and maximum values of 0.25 and 1), the proposed MLI is comparable to the previously published structures. In the proposed MLI, the ratios of maximum voltage stress on its different capacitors are equal to 0.25, 0.25, and 1. Moreover, the ratio of maximum voltage stress on its switches is equal to 1, which is less than that of other inverters. For synthesizing both the voltage stresses and numbers of the semiconductors, the normalized values of total standing voltages (TSVs) of the diodes and switches are, respectively, defined as follows:

$$\mathrm{TSV}_d\ (\mathrm{p.u.}) = \frac{1}{V_{o,\max}} \sum_{1}^{N_D} V_{di} \tag{36}$$

$$\mathrm{TSV}_{\mathrm{sw}}\ (\mathrm{p.u.}) = \frac{1}{V_{o,\max}} \sum_{1}^{N_S} V_{dsi}. \tag{37}$$

As seen in Table 3, considering all of the compared MLIs, the maximum and minimum values of $\mathrm{TSV}_{\mathrm{sw}}$ and TSV_d are, respectively, equal to (4 and 7.667) and (0.25 and 2). For the proposed inverter, these values are less than the maximum values of these parameters. By focusing on only 9L MLIs, the maximum values of these parameters, i.e., $\mathrm{TSV}_{\mathrm{sw}}$ and TSV_d, are, respectively, equal to 6.5 and 1.5. This means that the proposed MLI imposes voltage stresses less than the maximum values of 9L MLIs. As seen, the proposed MLI provides a lower $\mathrm{TSV}_{\mathrm{sw}}$ compared to 9L MLIs introduced in [37], [39], [40], [42], [47], [49], [50], and [52]. In terms of TSV_d, the proposed MLI provides a lower or comparable value compared with the MLIs in [45], [51], [53], [54], and [55]. The lowest TSV_d values are achieved by Barzegarkhoo et al. [52], followed by the authors in [42] and [48]. In addition, the sizes of capacitors used in these MLIs are listed in Table 3. As seen, the sizes of the capacitors used in the proposed MLI are also close to or smaller than those of other MLIs.

For RES applications like solar energy, it is essential for TL inverters to eliminate the leakage current of PV panels. Considering this fact, the proposed MLI and the inverter of [40], [48], and [51] are the only structures that are suitable for the mentioned application. However, in contrast to the proposed MLI, the MLIs of [40], [48], and [51], suffer from high charging current spikes of their capacitors, causing serious

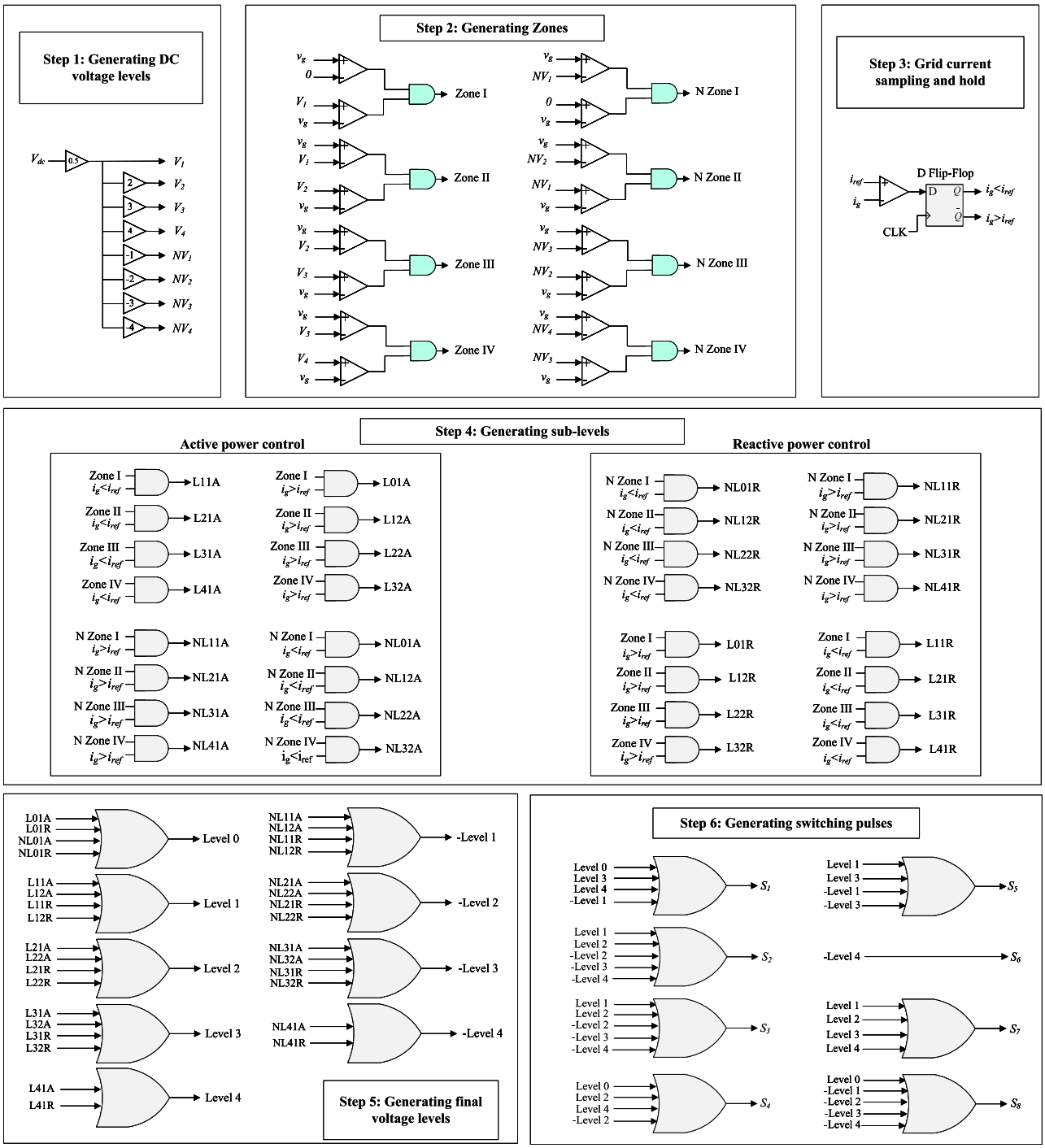


FIGURE 5. Block diagram of the employed PCC.

drawbacks like increased power losses, higher EMI, and shortening the life cycle of their capacitors. Besides the proposed MLI, only the MLI of [42] can provide CCCS. However, this MLI employs more switches and power components than the proposed one and does not have a CG structure. Notably, the MLI of [55] employs a much larger number of switches and components than the proposed one. Compared to these four MLIs, i.e., [40], [48], [51], and [55], the voltage stress on the switches, diodes, and capacitors, and the size of the passive components of the proposed MLI are close or less. It is noteworthy that in the case of the MLI of [51], the sizing of the capacitors has been done by considering the network/grid frequency of 400 Hz. Considering f_g = 50Hz and based on [51], these capacitors will be sized as 2.62, 2.62, and 3.84 mF. In addition, the proposed inverter has a high efficiency among 9L inverters based on Table 3. Hence, the proposed MLI is the superior option for RES applications, like solar PV systems.

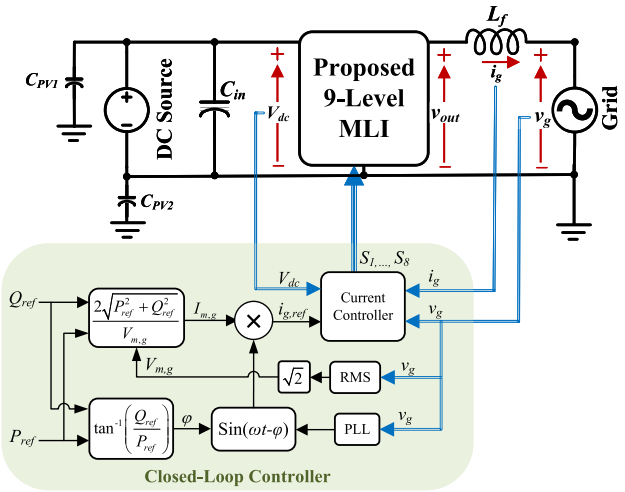


FIGURE 6. Block diagram of the test system used in the simulation.

IV. RESULTS AND DISCUSSIONS

A. SIMULATION RESULTS

Here, simulation results are presented to demonstrate the performance of the proposed MLI. All results are obtained in MATLAB/Simulink environment using nonideal device and passive models. The parameters used in the simulations are listed in Table 4. The block diagram of the test system, containing the designed closed-loop controller, is shown in Fig. 6. This controller can inject the required active and reactive power into the grid if their reference values (P_{ref} and Q_{ref}) are given. The closed-loop controller presented in [50] is used here. The switching pulses are generated based on the current controller. Fig. 5 shows the controller workflow in detail. In general, at each sampling instant, the grid current (i_g) is measured and compared with the reference current. The modulation zone is determined from the instantaneous grid voltage, and the two admissible voltage levels are identified; if $|i_g| < |i_{\text{ref}}|$, select the upper level; otherwise, select the lower level. Finally, the corresponding switching state is generated and sent to the inverter. This direct comparison-based logic provides fast current tracking with low computational burden and maintains robust operation under varying conditions due to sample-by-sample updates and zone-based voltage selection. In this article, the sinusoidal reference current i_{ref} is generated from the commanded active/reactive powers (P_{ref}, Q_{ref}).

In the context of TL PV inverters, leakage current typically refers to the PV-to-ground common-mode leakage current. This current flows through the parasitic capacitances between ground and PV. In Fig. 6, the parasitic capacitors of the PV panel are represented by C_{PV1} and C_{PV2}. It is noteworthy that the sizes of these capacitors are very small. For C_{PV2}, the voltage across its terminals is zero, i.e.,

$$v_{C_{\text{PV2}}}(t) = 0 \quad \Rightarrow \quad i_{C_{\text{PV2}}}(t) = C_{\text{PV2}} \frac{dv_{C_{\text{PV2}}}(t)}{dt} = 0 \tag{38}$$

which means no leakage current flows through C_{PV2}. For C_{PV1}, the voltage across the capacitor is constant and equal to the dc-link voltage V_{dc}, hence

$$i_{C_{\text{PV1}}}(t) = C_{\text{PV1}} \frac{dv_{C_{\text{PV1}}}(t)}{dt} = C_{\text{PV1}} \frac{dV_{\text{dc}}}{dt} \approx 0 \tag{39}$$

which results in only a negligible current. Therefore, the CG structure of the proposed converter ensures an effective reduction of the leakage current associated with these parasitic capacitances. To be more specific, the proposed CG structure maintains a constant common-mode voltage across the modeled PV parasitic capacitances, thereby suppressing the dominant PV-to-ground leakage current component linked to these capacitances. It should be noted that, in practice, the CG structure significantly reduces the PV-to-ground leakage current compared with conventional TL topologies without a CG feature, while acknowledging that small residual leakage may still exist through other parasitic paths.

The simulation results of the proposed MLI are illustrated in Fig. 7. Unlike Fig. 7(a) and (b) where only active power injection into the grid is aimed, the proposed MLI exchanges both reactive and active powers with respect to the grid in Fig. 7(c) and (d). As seen in Fig. 7(a), the proposed inverter has a desirable and stable performance under applying a step change in input dc voltage (V_{dc}), i.e., increasing dc voltage from 190 to 200 V at $t = 0.86$ s does not affect the output voltage and current. In Fig. 7(b), the reference active power is suddenly increased from 325 to 525 W at $t = 0.905$ s, leading to an increase in the amplitude of the injected current into the grid. As clearly shown, the proposed inverter can maintain its stable performance under this step change. As seen in Fig. 7(c), the proposed MLI can operate properly even under the step changes of both reference active and reactive powers. As seen, the applied step change in reactive power leads to a remarkable change in the injected current's phase angle into the grid. In Fig. 7(d), the amplitude of the apparent power injected into the grid is constant, and the step change has been applied in the phase angle of the injected current into the grid, leading to a step change only in the injected reactive power. In Fig. 7(e), the pure reactive power performance of the proposed MLI is demonstrated. It can be observed that the inverter maintains desirable operation even when a step change in the reactive power reference occurs at $t = 1.065$ s. Moreover, Fig. 7(f) illustrates that the proposed MLI can successfully sustain the injected current into the grid unchanged, even in the presence of a grid disturbance, here represented by a sudden voltage drop (10% sag) of the grid-voltage amplitude. In Fig. 8, the proposed inverter's performance in mitigating the CCCS is shown. As mentioned, the diodes D_{r1} and D_{r2} along with the inductors L_{r1} and L_{r2} are used for this aim. In other words, while charging the capacitors, the current passes through the mentioned inductors, leading to the mitigated CCCS. Unlike Fig. 8(a) where the proposed inverter circuit lacks the mentioned components (D_{r1}, D_{r2}, L_{r1}, and L_{r2}), it is clearly shown in Fig. 8(b) that the proposed MLI can remarkably mitigate CCCS. This can lead to several merits,

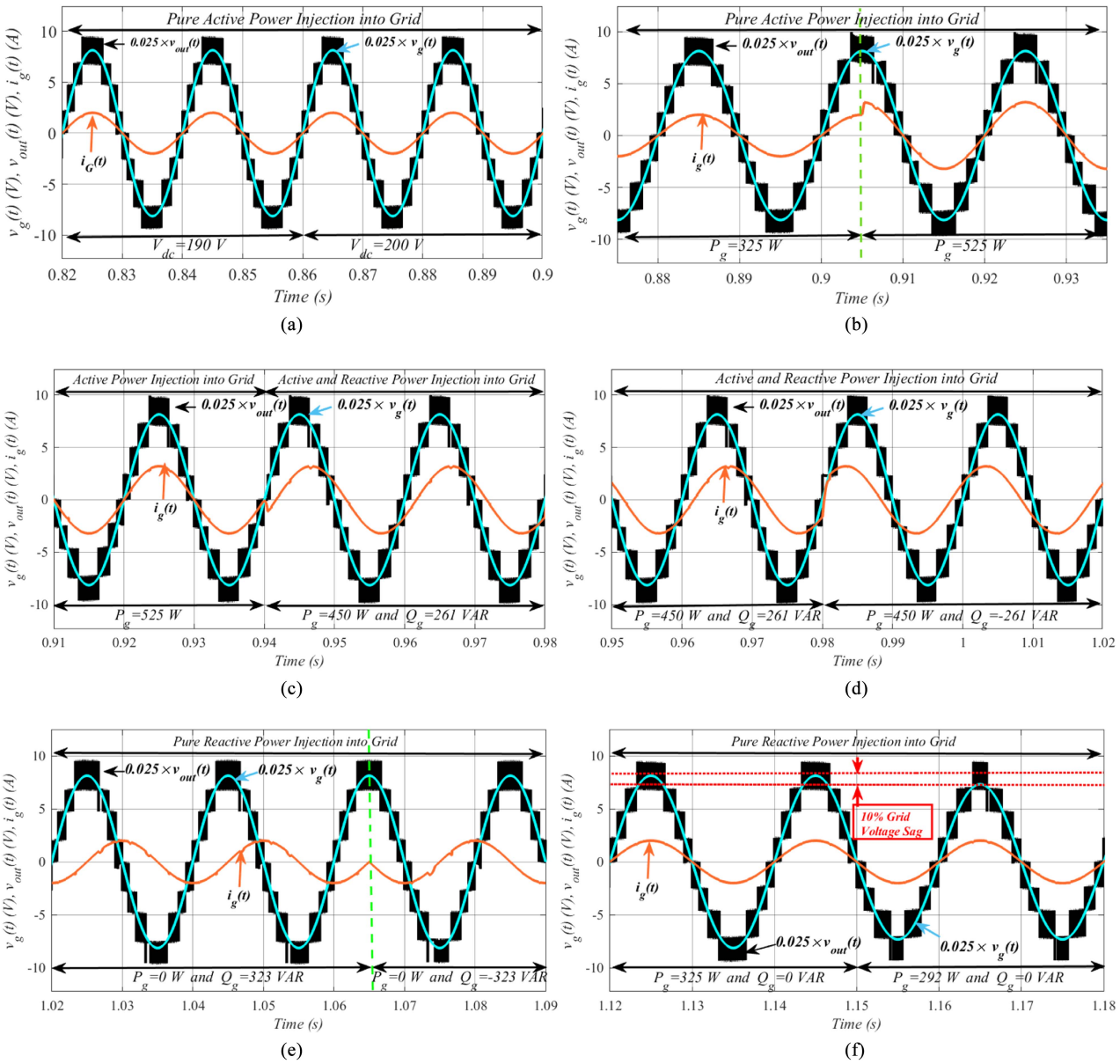


FIGURE 7. Simulation results of the proposed MLI demonstrating dynamic performance under various operating conditions. (a) Step change in the input dc voltage. (b) Step change in the reference active power. (c) Step change in both active and reactive power references. (d) Step change in the reference reactive power. (e) Injection of pure reactive power into the grid with a step change in its reference. (f) Response to a grid disturbance (10% voltage sag) during pure active power injection.

such as less EMI, higher efficiency, and longer life cycle of the capacitors. In particular, the reduction of high-di/dt currents suppresses high-frequency components, which are a major contributor to EMI. Moreover, the decrease in current spikes reduces both conduction and switching losses, thereby improving the overall efficiency. Finally, the reduction of ripple current stress in electrolytic capacitors alleviates thermal aging, which is a well-known determinant of their service life. These advantages are widely recognized in the power electronics literature [56], [57], [58]. It should be noted that the observed voltage ripple is inherent to SC operation and does not contradict the self-balancing property.

In Fig. 9, the harmonic spectra of the injected grid current are illustrated for three different operating conditions of the proposed 9L MLI. In the case of pure active power injection (325 W), the total harmonic distortion (THD) is found to be 0.98%, which satisfies the grid interconnection standards. For pure reactive power injection (323 Var), the harmonic content increases, leading to a THD of 3.36%. When both active and reactive powers are injected simultaneously (281 W and 162 Var), the measured THD is 1.30%. These results confirm that the proposed inverter maintains low distortion levels under various loading scenarios, thereby ensuring high-quality current injection into the grid.

TABLE 5. Parameters and Components Used in the Experiments

Parameter/component	Symbol	Value	Description
Load Voltage (rms)	V_L	220 V	load voltage
1st and 2nd Switched-Capacitors	C_1, C_2	1.2 mF	Electrolyte capacitors
3rd Switched-Capacitor	C_3	2 mF	Electrolyte capacitors
Fundamental Frequency	f_g	50 Hz	-
Switching Frequency	f_s	20 kHz	-
Output Filtering Inductor	L_f	1.5 mH	Ferrite core inductor
Charging Current's Spike Inductors	L_{r1}, L_{r2}	0.3 mH	-
Power Switches	S_1, ..., S_8	-	IPW65R041CFD MOSFETs
Power Diodes	D_{r1}, D_{r2} & D_1	-	C3D10060A power diodes
Micro-controller	DSP	-	TMS320F280049 DSP controller

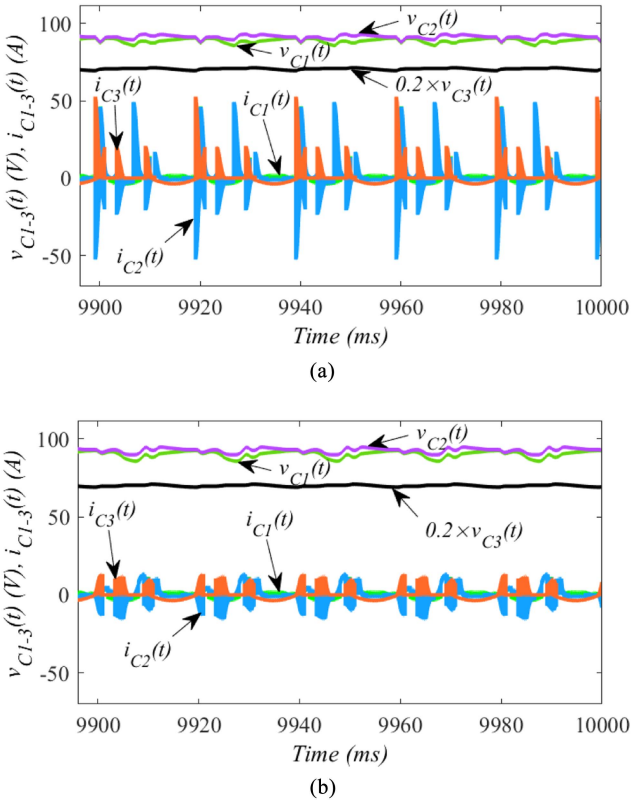


FIGURE 8. Simulation results of the proposed MLI including voltages and currents of its capacitors. (a) Without CCCS. (b) With CCCS.

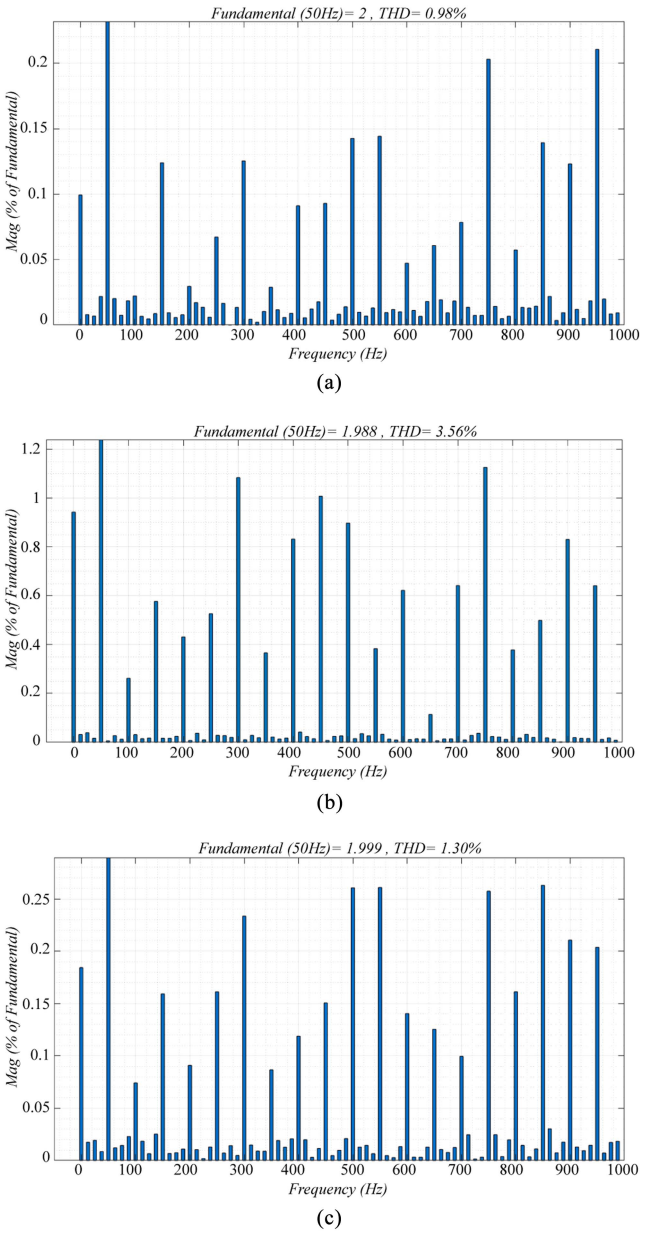
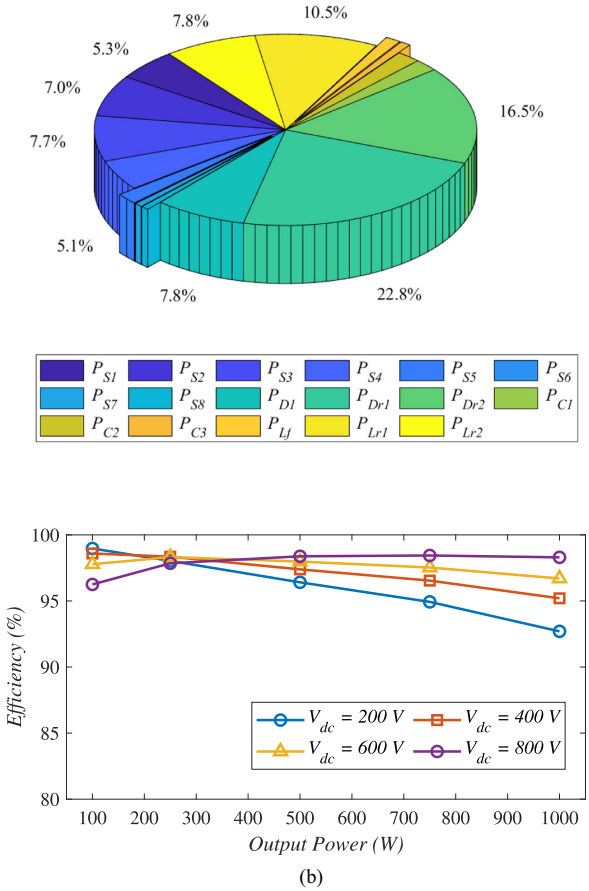


FIGURE 9. THD of the injected current to the grid by the proposed 9L MLI under different power injection scenarios. (a) Pure active power injection (325 W). (b) Pure reactive power injection (323 Var). (c) Active and reactive power injection (281 W and 162 Var).

In Fig. 10, the efficiency of the proposed converter for different output powers and power loss breakdown per components are shown. As seen, the results are acceptable. It should be noted that shown power loss breakdown is obtained when the output power, dc voltage, and maximum inverter voltage are, respectively, considered around 325 W, 200 V, and 400 V.

At this stage, the capability of the proposed MLI for bidirectional operation is evaluated. In Fig. 1, by replacing D_1 with a power switch equipped with a body diode, the proposed inverter can also operate in the bidirectional mode. The switching pattern of this additional switch follows that of D_1. In other words, during the intervals when D_1 is expected to conduct (i.e., the voltage levels of $\pm$ half-cycle zero and the +fourth level, corresponding to modes 1 and 5 in Table 1), the switch is turned ON, and vice versa. The simulation results



(b)

FIGURE 10. Power loss distribution of the proposed MLI. (a) Breakdown by components. (b) Efficiency versus output power for different dc-link voltages.

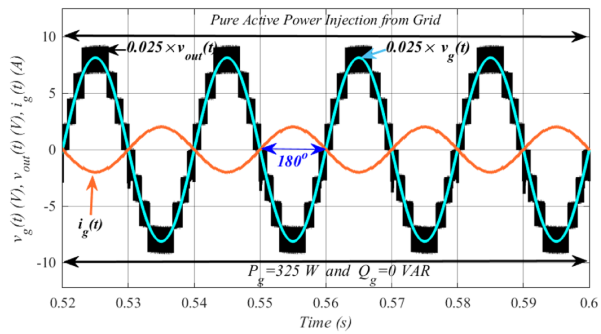


FIGURE 11. Simulation results of the proposed MLI (D_1 replace by a power switch) for bidirectional operation.

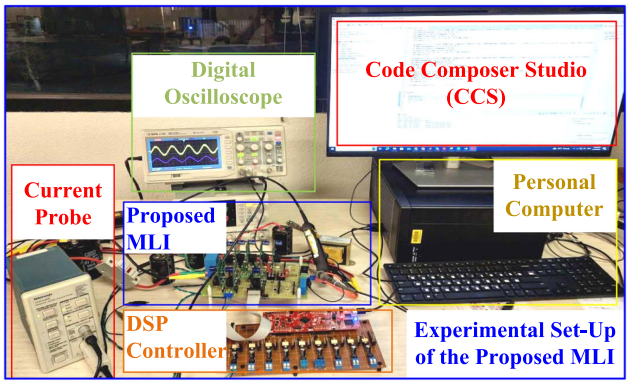
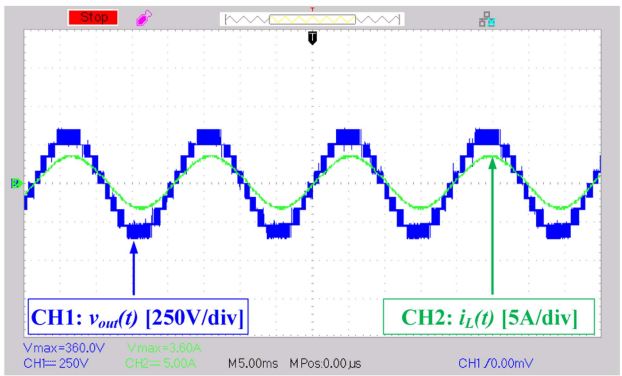
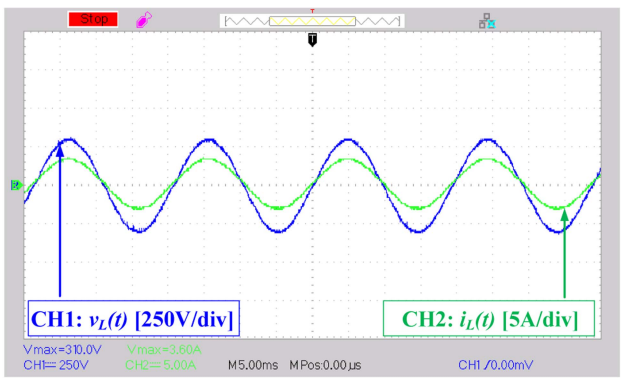


FIGURE 12. Experimental setup of the proposed 9L MLI.



(a)



(b)

FIGURE 13. For resistive load, (a) load current ($i_L(t)$) and the output voltage of the inverter ($v_{out}(t)$) and (b) load current and voltage ($i_L(t)$ and $v_L(t)$).

presented in Fig. 11 confirm this bidirectional capability. As observed, the grid voltage and current are 180° out of phase, meaning that active power is transferred from the grid side back to the input dc side. Hence, the proposed structure can function as an active rectifier simply by replacing a single diode with a power switch.

Consequently, the proposed 9L CGSC-TL MLI has a desirable performance under different operating conditions, including the step changes of the input dc voltage source and the reference values of the active and reactive power that should be generated by the inverter and injected into the power grid.

B. EXPERIMENTAL RESULTS

Here, thorough experimental results for proving the performance of the proposed MLI are presented in the presence of different types of local loads. Fig. 12 shows the experimental setup implemented to obtain the results. In Table 5, the

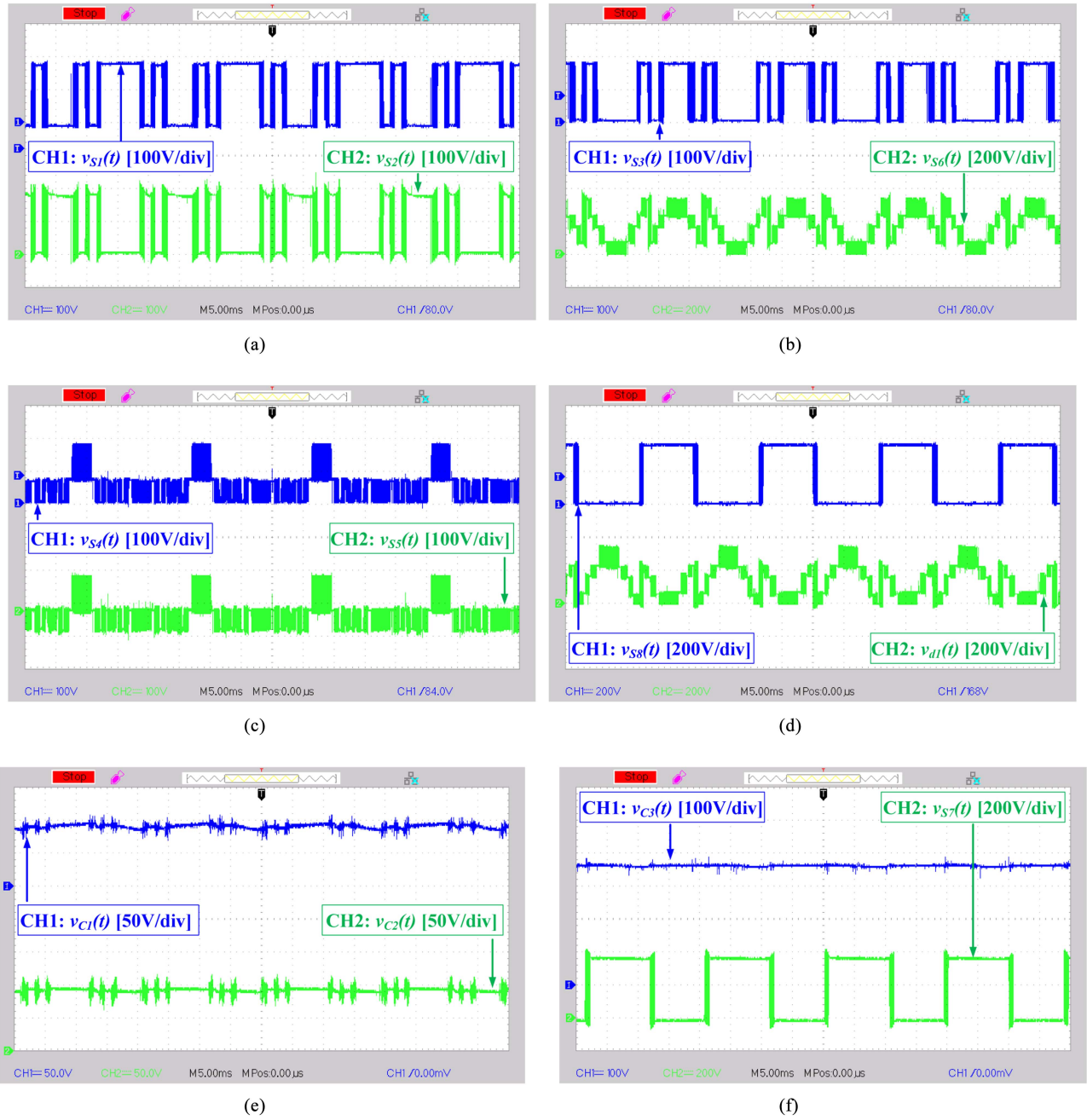
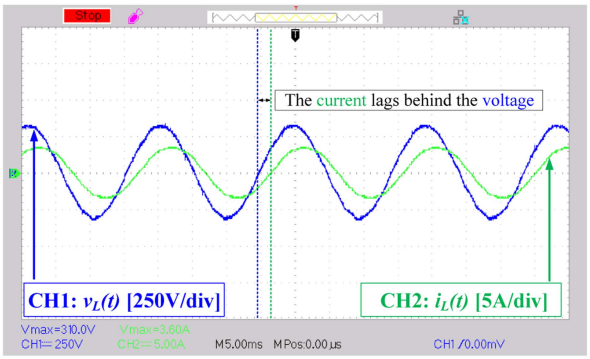


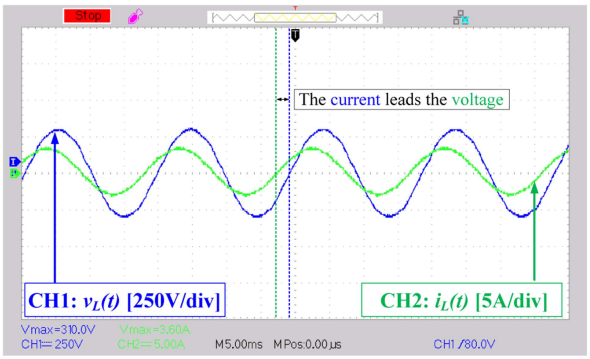
FIGURE 14. **Voltage waveforms of different components of the proposed MLI. (a) $v_{S1}(t)$ and $v_{S2}(t)$. (b) $v_{S3}(t)$ and $v_{S6}(t)$. (c) $v_{S4}(t)$ and $v_{S5}(t)$. (d) $v_{S8}(t)$ and $v_{d1}(t)$. (e) $v_{C1}(t)$ and $v_{C2}(t)$. (f) $v_{C3}(t)$ and $v_{S7}(t)$.**

parameters and components description used in the experimental setup are listed.

In the following, the experimental results are presented and discussed in detail. Note that the input dc voltage is equal to 180 V. Initially, the performance of the proposed MLI is proved while having a pure resistive load equal to $R = 86\ \Omega$. This means that only active power is generated by the inverter. Note that the load is in parallel with a 1-μF capacitor. Fig. 13(a) shows the output voltage of the inverter, and the current of load. As clearly seen, the proposed MLI can successfully generate a 9L output voltage with a peak value of 360 V. Here, the load current's peak value is equal to 3.6 A. The load voltage is shown in Fig. 13(b) whose amplitude is about 310 V. As a result, the inverter generates the active power of about 560 W. In Fig. 14, the voltages of the different components of the proposed MLI are presented. As shown, the voltages of the switches and diodes align with the analysis. Based on the results, the maximum value of $v_{S1}(t)$, $v_{S2}(t)$, $v_{S3}(t)$, $v_{S4}(t)$, $v_{S5}(t)$, $v_{S6}(t)$, $v_{S7}(t)$, $v_{S8}(t)$, and $v_{d1}(t)$ are, respectively, about 180, 180, 180, 180, 90, 360, 360, 360,

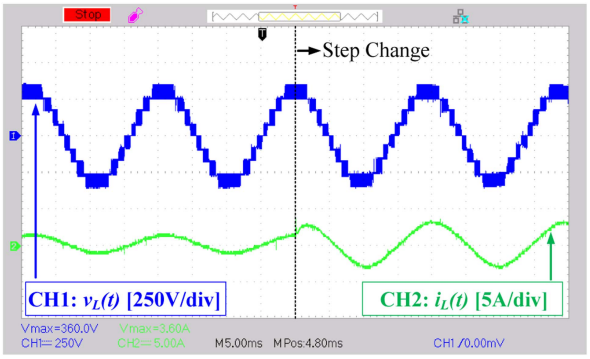


(a)

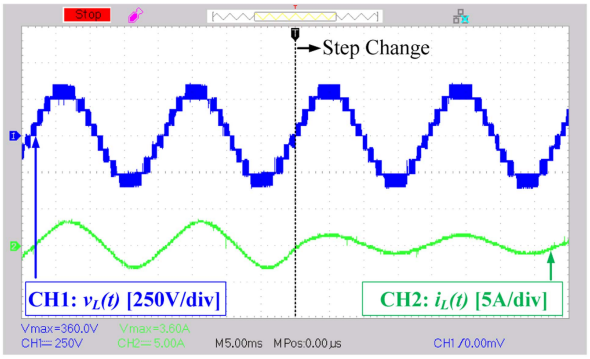


(b)

FIGURE 15. Load current ($i_L(t)$) and the load voltage ($v_L(t)$) (a) for a resistive-inductive load (b) for a resistive-capacitive load.



(a)



(b)

FIGURE 16. Load current ($i_L(t)$) and voltage ($v_L(t)$) in presence of step change (a) decreasing load (b) increasing load.

and 360 V. In other words, these values are the maximum voltage stress on the switching devices of the proposed MLI whose minimum and maximum values are equal to 90 and 360 V, respectively. As seen in Fig. 14(e) and (f), the capacitors C_1, C_2, and C_3 are charged to about 90, 90, and 360 V, which are desirable. These experimental waveforms further demonstrate that the capacitor voltages remain close to their intended average values, with bounded ripple and no long-term drift. Hence, the self-balancing feature of the inverter is proved.

The performance of the inverter in the presence of resistive–inductive and resistive–capacitive loads is shown in Fig. 15. As seen in Fig. 15(a), the proposed MLI is able to properly supply a resistive–inductive load ($R = 110\ \Omega$ and $L = 0.117$ H), where the load current lags behind the voltage of the load. Besides, as shown in Fig. 15(b), the proposed inverter can properly operate in the presence of the resistive–capacitive load ($R = 110\ \Omega$ and $C = 30$ mF), where the load current leads its voltage. In Fig. 16, the experimental results of the proposed MLI in the case of occurring step changes in the load are shown. In Fig. 16(a), the sudden load decrease from $R = 110\ \Omega$ to $R = 86\ \Omega$ leads to a step change in the load current's amplitude (2.5 to 3.6 A). In Fig. 16(b), the sudden load increase from $R = 86\ \Omega$ to $R = 110\ \Omega$ leads to a step change in the load current from 3.6 to 2.5 A. As seen, the inverter is able to generate the desired 9L output voltage leading to a sinusoidal current. Hence, the proposed MLI is able to maintain its proper operation despite the changes. All experimental results are obtained on a laboratory prototype of the proposed inverter supplying local loads at 220 V, 50 Hz, chosen to emulate typical grid-connected operating conditions. Although the prototype was operated with these grid-equivalent loads rather than being directly tied to the utility grid, full-scale grid-connected operation (such as the minimum dc-link voltage requirement, active and reactive power injection, and behavior under voltage sag) is analyzed and validated through the detailed simulation studies presented in the previous sections. Consequently, based on both experimental and simulation results, which are all in complete agreement with the analysis, the proposed CG-TL 9L MLI has desirable dynamic performance, making it a suitable option for practical modern applications such as renewable energy systems.

V. CONCLUSION

In this article, a new eight-switch 9L CGSC-TL MLI is proposed. This inverter can provide advantages, such as employing fewer or comparable number of components, having CG structure resulting in the elimination of leakage current, voltage-boosting ability (maximum value of gain equal to 2), active and reactive power supporting capability, limited CCCS resulting in lower power losses, longer life cycle for

capacitors, and mitigated EMI, extensive input voltage capability, TL structure, no sensors needed for balancing of the voltages of capacitors, and less/close voltage stress on the components. These merits are all proved by comprehensive comparison results. The performance of the proposed MLI is validated in MATLAB/Simulink environment. As proved, under step changes in input dc voltage and reference active and reactive power injection into the grid, the dynamic performance of the inverter is completely desirable. In addition, comprehensive experimental results are presented to prove the performance of the proposed inverter. The aforementioned features make the proposed CGSC-TL 9L MLI a superior option for renewable energy applications such as solar PV systems.

REFERENCES

[1] M. Abbasi, E. Abbasi, and L. Li, "New transformer-less DC–DC converter topologies with reduced voltage stress on capacitors and increased voltage conversion ratio," *IET Power Electron.*, vol. 14, no. 6, pp. 1173–1192, 2021.

[2] M. Abbasi, E. Abbasi, B. Tousi, and G. B. Gharehpetian, "New family of expandable step-up/-down DC-DC converters with increased voltage gain and decreased voltage stress on capacitors," *Int. Trans. Elect. Energy Syst.*, vol. 30, no. 3, 2020, Art. no. e12252.

[3] M. Abbasi, E. Babaei, and B. Tousi, "New family of non-isolated step-up/down and step-up switched-capacitor-based DC–DC converters," *IET Power Electron.*, vol. 12, no. 7, pp. 1706–1720, 2019.

[4] M. Abbasi, H. Shayestehkhah, and B. Tousi, "Application of an additive self-tuning controller for static synchronous series compensator for damping of sub-synchronous resonance oscillations," *Int. J. Eng., Trans. B, Appl.*, vol. 31, no. 4, pp. 564–573, 2018.

[5] N. V. Kurdkandi, M. G. Marangalu, Y. Naderi, S. H. Hosseini, and M. Sabahi, "Single-phase inverter with common grounded feature and connected into grid," in *Proc. 28th Iranian Conf. Elect. Eng.*, 2020, pp. 1–5.

[6] N. V. Kurdkandi et al., "A new transformer-less common grounded three-level grid-tied inverter with voltage boosting capability," *IEEE Trans. Energy Convers.*, vol. 36, no. 3, pp. 1896–1909, Sep. 2021.

[7] M. Aalami, M. G. Marangalu, S. G. Zadeh, E. Babaei, and S. H. Hosseini, "Ladder-switch based multilevel inverter with reduced devices count," in *Proc. 11th Power Electron. Drive Syst. Technol. Conf.*, 2020, pp. 1–5.

[8] S. K. Haghighian, H.-G. Yeh, M. G. Marangalu, N. V. Kurdkandi, M. Abbasi, and H. Tarzamni, "A seventeen-level step-up switched-capacitor-based multilevel inverter with reduced charging current stress on capacitors for PV applications," *IEEE Access*, vol. 11, pp. 118124–118143, 2023.

[9] M. Abbasi and B. Tousi, "Novel controllers based on instantaneous p-q power theory for transformerless SSSC and STATCOM," in *Proc. IEEE Int. Conf. Environ. Elect. Eng./IEEE Ind. Commercial Power Syst. Eur.*, 2017, pp. 1–10.

[10] M. Abbasi and b. Tousi, "A novel controller based on single-phase instantaneous p-q power theory for a cascaded PWM transformer-less STATCOM for voltage regulation," *J. Oper. Autom. Power Eng.*, vol. 6, no. 1, pp. 80–88, 2018.

[11] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[12] M. Islam, S. Mekhilef, and M. Hasan, "Single phase transformerless inverter topologies for grid-tied photovoltaic system: A review," *Renewable Sustain. Energy Rev.*, vol. 45, pp. 69–86, 2015.

[13] M. N. H. Khan, M. Forouzesh, Y. P. Siwakoti, L. Li, T. Kerekes, and F. Blaabjerg, "Transformerless inverter topologies for single-phase photovoltaic systems: A comparative review," *IEEE Trans. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 1, pp. 805–835, Mar. 2020.

[14] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li, and X. He, "Transformerless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 793–805, Feb. 2013.

[15] Y. P. Siwakoti and F. Blaabjerg, "Common-ground-type transformerless inverters for single-phase solar photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2100–2111, Mar. 2018.

[16] A. Kumar and P. Sensarma, "A four-switch single-stage single-phase buck–boost inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5282–5292, Jul. 2017.

[17] M. T. Azary, M. Sabahi, E. Babaei, and F. A. A. Meinagh, "Modified single-phase single-stage grid-tied flying inductor inverter with MPPT and suppressed leakage current," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 221–231, Jan. 2018.

[18] R. Barzegarkhoo, S. S. Lee, Y. P. Siwakoti, S. A. Khan, and F. Blaabjerg, "Design, control, and analysis of a novel grid-interfaced switched-boost dual T-type five-level inverter with common-ground concept," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 8193–8206, Sep. 2021.

[19] N. Vosoughi, S. H. Hosseini, and M. Sabahi, "A new single-phase transformerless grid-connected inverter with boosting ability and common ground feature," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9313–9325, Nov. 2020.

[20] N. Vosoughi Kurdkandi, S. H. Hosseini, and M. Sabahi, "Single-phase common-grounded transformer-less grid-tied inverter for PV application," *IET Power Electron.*, vol. 13, no. 1, pp. 157–167, 2020.

[21] A. Kadam and A. Shukla, "A multilevel transformerless inverter employing ground connection between PV negative terminal and grid neutral point," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8897–8907, Nov. 2017.

[22] F. B. Grigoletto, "Multilevel common-ground transformerless inverter for photovoltaic applications," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 9, no. 1, pp. 831–842, Feb. 2021.

[23] M. Chen, P. C. Loh, Y. Yang, and F. Blaabjerg, "A six-switch seven-level triple-boost inverter," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 1225–1230, Feb. 2021.

[24] R. Barzegarkhoo, Y. P. Siwakoti, and F. Blaabjerg, "A new switched-capacitor five-level inverter suitable for transformerless grid-connected applications," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8140–8153, Aug. 2020.

[25] R. Barzegarkhoo, Y. P. Siwakoti, N. Vosoughi, and F. Blaabjerg, "Six-switch step-up common-grounded five-level inverter with switched-capacitor cell for transformerless grid-tied PV applications," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1374–1387, Feb. 2021.

[26] M. Samizadeh, X. Yang, B. Karami, W. Chen, F. Blaabjerg, and M. Kamranian, "A new topology of switched-capacitor multilevel inverter with eliminating leakage current," *IEEE Access*, vol. 8, pp. 76951–76965, 2020.

[27] M. A. Azad et al., "A single phase nine level common ground switched capacitor inverter with double boosting capability," *IET Power Electron.*, vol. 17, no. 16, pp. 2900–2916, 2024.

[28] N. Vosoughi Kurdkandi, K. Varesi, J. Fallah Ardashir, W. Gao, Z. Cao, and C. Mi, "Transformer-less seven-level inverter with triple boosting capability and common ground," *Energies*, vol. 17, no. 13, 2024, Art. no. 3115.

[29] K. P. Panda, S. K. Dalai, G. Panda, R. T. Naayagi, and S. S. Lee, "Self-balanced switched-capacitor common-grounding boost multilevel inverter," *Electronics*, vol. 13, no. 13, 2024, Art. no. 2608.

[30] K. Liu, Z. Lin, X. Zhang, S. Lin, and L. Li, "A common-ground structure switched-capacitor multilevel inverter with low–DC bias characteristics," *Int. J. Circuit Theory Appl.*, 2025.

[31] M. T. Hussain et al., "Design and analysis of a single source seven level common ground SC based multilevel inverter topology with high reliability," *Sci. Rep.*, vol. 15, no. 1, 2025, Art. no. 27348.

[32] M. Zaid, M. Ali, A. Sarwar, M. Khalid, and A. Iqbal, "A reduced switch stress common-ground boosting multilevel inverter for renewable energy applications," *e-Prime-Adv. Elect. Eng. Electron. Energy*, vol. 12, 2025, Art. no. 100953.

[33] N. Sandeep, J. S. M. Ali, U. R. Yaragatti, and K. Vijayakumar, "A self-balancing five-level boosting inverter with reduced components," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6020–6024, Jul. 2019.

[34] S. S. Lee and K. Lee, "Dual-T-type seven-level boost active-neutralpoint-clamped inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6031–6035, Jul. 2019.

[35] M. J. Sathik, N. Sandeep, and F. Blaabjerg, "High gain active neutral point clamped seven-level self-voltage balancing inverter," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 67, no. 11, pp. 2567–2571, Nov. 2020.

[36] J. Liu, J. Wu, and J. Zeng, "Symmetric/asymmetric hybrid multilevel inverters integrating switched-capacitor techniques," *IEEE Trans. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 3, pp. 1616–1626, Sep. 2018.
[37] Y. Nakagawa and H. Koizumi, "A boost-type nine-level switched capacitor inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6522–6532, Jul. 2019.
[38] A. Taghvaie, J. Adabi, and M. Rezanejad, "A self-balanced step-up multilevel inverter based on switched-capacitor structure," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 199–209, Jan. 2018.
[39] J. S. Mohamed Ali and V. Krishnasamy, "Compact switched capacitor multilevel inverter (CSCMLI) with self-voltage balancing and boosting ability," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4009–4013, May 2019.
[40] H. K. Jahan, M. Abapour, and K. Zare, "Switched-capacitor-based single-source cascaded H-bridge multilevel inverter featuring boosting ability," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1113–1124, Feb. 2019.
[41] M. D. Siddique et al., "A new single phase single switched-capacitor based nine-level boost inverter topology with reduced switch count and voltage stress," *IEEE Access*, vol. 7, pp. 174178–174188, 2019.
[42] T. Debela Awas and J. Singh, "High-gain nine-level switched-capacitor multilevel inverter featuring less number of devices and leakage current," *Int. J. Circuit Theory Appl.*, vol. 51, no. 8, pp. 3746–3773, 2023.
[43] N. Sandeep, J. S. M. Ali, U. R. Yaragatti, and K. Vijayakumar, "Switched-capacitor-based quadruple-boost nine-level inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7147–7150, Aug. 2019.
[44] M. Kumari, M. D. Siddique, A. Sarwar, S. Mekhilef, and M. Tariq, "A twice boost nine-level switched-capacitor multilevel (2B-9L-SCMLI) inverter with self-voltage balancing capability," *Int. J. Circuit Theory Appl.*, vol. 49, no. 8, pp. 2578–2592, 2021.
[45] K. P. Panda, R. Naayagi, P. K. Ray, and G. Panda, "Single-source switched-capacitor boost nine-level inverter with reduced components," *CSEE J. Power Energy Syst.*, vol. 9, no. 5, pp. 1688–1697, Sep. 2023.
[46] Y. Wang, J. Ye, K. Wang, F. Nie, G. Li, and J. Liang, "A nine-level switched-capacitor step-up inverter with low voltage stress," *J. Elect. Eng. Technol.*, vol. 18, no. 2, pp. 1147–1159, 2023.
[47] G. M. Oorappan, S. Pandarinathan, and J. Arumugam, "A new nine-level switched-capacitor-based multilevel inverter with low voltage stress and self-balancing," *Elect. Eng.*, vol. 105, no. 2, pp. 867–882, 2023.
[48] M. Chen, Y. Yang, P. C. Loh, and F. Blaabjerg, "A single-source nine-level boost inverter with a low switch count," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 2644–2658, Mar. 2022.
[49] Z. Sarwer, M. D. Siddique, A. Sarwar, S. Mekhilef, and M. N. Anwar, "Switched capacitor based 7-level and 9-level multilevel inverters with single DC source and reduced voltage stress," *e-Prime-Adv. Elect. Eng. Electron. Energy*, vol. 6, 2023, Art. no. 100327.
[50] N. V. Kurdkandi et al., "An improved nine-level switched capacitor-based inverter with voltage boosting capability and limitation of capacitor current spikes for PV applications," *IET Renewable Power Gener.*, vol. 17, no. 3, pp. 725–749, 2023.
[51] R. Barzegarkhoo, M. Farhangi, S. S. Lee, R. P. Aguilera, Y. P. Siwakoti, and J. Pou, "Nine-level nine-switch common-ground switched-capacitor inverter suitable for high-frequency AC-microgrid applications," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 6132–6143, May 2022.
[52] R. Barzegarkhoo, M. Moradzadeh, E. Zamiri, H. M. Kojabadi, and F. Blaabjerg, "A new boost switched-capacitor multilevel converter with reduced circuit devices," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 6738–6754, Aug. 2018.
[53] M. Saeedian, M. E. Adabi, S. M. Hosseini, J. Adabi, and E. Pouresmaeil, "A novel step-up single source multilevel inverter: Topology, operating principle, and modulation," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3269–3282, Apr. 2019.
[54] J. Liu, W. Lin, J. Wu, and J. Zeng, "A novel nine-level quadruple boost inverter with inductive-load ability," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4014–4018, May 2019.
[55] R. Agarwal, K. K. Gupta, and S. Singh, "A double boost 9-level switched capacitor-based multilevel inverter for photovoltaic applications," *Int. J. Circuit Theory Appl.*, vol. 51, no. 7, pp. 3288–3315, Mar. 2023.
[56] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*. Hoboken, NJ, USA: Wiley, 2003.
[57] H. Wang, M. Liserre, and F. Blaabjerg, "Toward reliable power electronics: Challenges, design tools, and opportunities," *IEEE Ind. Electron. Mag.*, vol. 7, no. 2, pp. 17–26, Jun. 2013.
[58] F. C. Lee and Q. Li, "High-frequency integrated point-of-load converters: Overview," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4127–4136, Sep. 2013.

MAYSAM ABBASI (Member, IEEE) received the B.Sc. degree from Azarbaijan Shahid Madani University, Tabriz, Iran, in 2011, and the M.Sc. degree from Urmia University, Urmia, Iran, in 2014, both in electrical engineering (power), and the Ph.D. degree in electrical engineering from the University of Technology Sydney, Sydney, NSW, Australia, in 2024.

In 2024, he joined the Queensland University of Technology, Brisbane City, QLD, Australia, where he is currently an Academic Research Fellow. He reviews for high-impact journals published by IEEE, IET, Springer, and Wiley. His hands-on experience includes power converter design, battery energy storage systems, and grid-supporting control solutions for modern power systems. His expertise includes advanced power systems, power system stability, power system modeling and simulation, and dynamic and steady-state studies, as well as the design and control of renewable energy interfaces and power conversion systems. His research interests include power systems and stability, grid-forming inverter integration and control, advanced power electronics, renewable energy integration, microgrids, flexible ac transmission system devices, optimization, and smart grids.

Dr. Abbasi received two global awards for ranking among the top 1% of reviewers in "Engineering" and "Cross-Field" in 2019. He has received several competitive scholarships, grants, and travel awards supporting his research. He is a Secretary of the IEEE Queensland Power Electronics/Industrial Electronics/Industry Application Joint Chapter.

MILAD GHAVIPANJEH MARANGALU (Member, IEEE) was born in Urmia, Iran, in 1992. He received the B.Sc. degree in electrical engineering and the M.Sc. degree in power electrical engineering from Urmia University, Urmia, Iran, in 2014 and 2018, respectively, and the Ph.D. degree in power electronics and power systems from the University of Tabriz, Tabriz, Iran, in 2022.

For more than six years, he has been involved in the design and control of grid-tied power electronic converters. His Ph.D. thesis, entitled "Design of an Improved Grid-Tied Multilevel Inverter for Photovoltaic Applications," resulted in the development of three grid-tied inverter prototypes. His M.Sc. thesis focused on "Designing a Single-DC Source Five-Level Inverter for Photovoltaic Applications Considering MPPT Algorithms." He was a Ph.D. Guest Researcher with the Tallinn University of Technology, Tallinn, Estonia, where he collaborated with the power electronics research group from 2021 to 2022. He has authored and coauthored more than 36 journal and conference papers. His current research interests include multilevel inverters, grid-tied photovoltaic inverters, high step-up power electronic converters, control of power electronic systems, and renewable energy systems.

NASER VOSOUGHI KURDKANDI (Member, IEEE) received the Ph.D. degree in electrical engineering and power electronics from the University of Tabriz, Tabriz, Iran, in 2019.

From 2019 to 2020, he was a Postdoctoral Researcher with the University of Tabriz. In 2020, he joined the Tallinn University of Technology, Tallinn, Estonia, as a Postdoctoral Researcher. Since 2022, he has been a Postdoctoral Research Fellow with San Diego State University, San Diego, CA, USA. His research interests include multilevel inverters, grid-connected photovoltaic inverters, dc–dc switched-capacitor and switched-inductor converters, fast charging stations for electric vehicles, battery-based energy storage systems, solid state transformers, and induction motor drives.

Dr. Kurdkandi has been recognized as one of the world's top 2% most-cited scientists since 2021, according to a global-citation-based ranking by Stanford University, Stanford, CA, USA.

EHSAN ABBASI (Member, IEEE) received the B.Sc. degree in telecommunication engineering from the University of Bonab, Bonab, Iran, in 2016, and the M.Sc. degree in electrical engineering from the University of Tabriz, Tabriz, Iran, in 2021.

He was a Reviewer for several peer-reviewed journals. His research interests include energy hubs, advanced power electronics, advanced power systems, optimization, renewable energy integration, and smart grids.

HANI VAHEDI (Senior Member, IEEE) received the Ph.D. (Hons.) degree in electrical engineering from the École de Technologie Supérieure (ÉTS), Université du Québec, Montreal, QC, Canada, in 2016.

He has authored more than 100 IEEE conference and journal papers, a Springer Nature book, and a book chapter published by Elsevier. He is the Inventor of the five-level Packed U-Cell converter, holds several U.S. and international patents, and transferred this technology to industry, assisting in the development of a bidirectional electric vehicle (EV) charger based on his invention. After seven years in the industry working as a power electronics designer and later as Chief Scientific Officer, he joined Delft University of Technology as an Assistant Professor to advance electrification for the clean energy transition. He leads 24/7 Energy Hub, The Green Village, Delft University of Technology, Delft, The Netherlands, an operational microgrid that integrates renewables, green hydrogen production, and hybrid energy storage systems. His research interests include multilevel power converter topologies, modulation and control, and applications in smart grids, renewable energy conversion, EV charging, green hydrogen production through electrolysis, and fuel-cell systems.

Dr. Vahedi was the recipient of the ÉTS's Best Ph.D. Thesis Award (2016–2017). He has been an Active Member of the IEEE Industrial Electronics Society (IES) since 2012, serving on the local organizing committee for 2012 Annual Conference on IEEE Industrial Electronics Society (IECON) in Montreal, acting as Students and Young Professionals Chair for numerous IES-sponsored conferences from 2016 to 2024, and serving as Technical Program Chair (GreenTech Cluster) of IECON25 in Madrid, Spain, as well as Special Sessions Chair for IECON26 in Doha, Qatar. He manages IES Chapters and Joint Chapters Program. He is an Associate Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE OPEN JOURNAL OF THE INDUSTRIAL ELECTRONICS SOCIETY, and IEEE OPEN JOURNAL OF POWER ELECTRONICS.

LI LI (Senior Member, IEEE) received the B.S. degree from the Huazhong University of Science and Technology, Wuhan, China, in 1996, the M.S. degree from Tsinghua University, Beijing, China, in 1999, and the Ph.D. degree from the University of California at Los Angeles, Los Angeles, CA, USA, in 2005, all in electrical engineering.

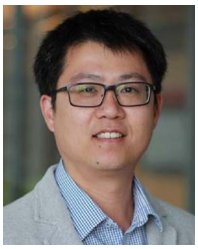
From 2005 to 2007, he was a Research Associate with the University of New South Wales at the Australian Defence Force Academy, Campbell, ACT, Australia. From 2007 to 2011, he was a Researcher with the National ICT Australia, Victoria Research Laboratory, Department of Electrical and Electronic Engineering, The University of Melbourne, Parkville, VIC, Australia. In 2011, he joined the University of Technology Sydney, Sydney, NSW, Australia, where he is currently an Associate Professor. He held several visiting positions at various universities. His research interests include power systems and control theory.

Dr. Li is an Associate Editor for IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, *IET Renewable Power Generation*, and *IET Generation, Distribution and Transmission*.

RICARDO P. AGUILERA (Member, IEEE) received the B.Sc. degree in electrical engineering from the Universidad de Antofagasta, Antofagasta, Chile, in 2003, the M.Sc. degree in electronics engineering from the Universidad Tecnica Federico Santa Maria, Valparaíso, Chile, in 2007, and the Ph.D. degree in electrical engineering from The University of Newcastle (UoN), Newcastle, NSW, Australia, in 2012.

From 2012 to 2013, he was a Research Academic with UoN, where he was part of the Centre for Complex Dynamic Systems and Control. From 2014 to 2016, he was a Senior Research Associate with The University of New South Wales, Sydney, NSW, where he was part of the Australian Energy Research Institute. Since 2016, he has been with the School of Electrical and Data Engineering, University of Technology Sydney, Ultimo, NSW, where he is currently an Associate Professor. His main research interests include theoretical and practical aspects on model-predictive control with application to power electronics, renewable energy integration, microgrid control, and smart grid digital twins.

Dr. Aguilera is an Associate Editor for IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. From 2021 to 2022, he was the Vice Chair of the IEEE NSW Joint Chapter Power Electronics Society/Industrial Electronicsy Society/Industry Application Society.



DYLAN LU (Senior Member, IEEE) received the Ph.D. degree in electronic and information engineering from The Hong Kong Polytechnic University, Hong Kong, in 2004.

In 2003, he began his professional career with PowereLab Ltd., Hong Kong, as a Senior Design Engineer, focusing on industrial switching power supply projects. From 2006 to 2016, he was a full-time Faculty Member with The University of Sydney, Sydney, NSW, Australia. In July 2016, he joined the University of Technology Sydney, Sydney, where he is currently a Professor and the Head of the Discipline of Electrical Power and Energy Systems with the School of Electrical and Data Engineering. His research interests include developing efficient, cost-effective, and reliable power conversion solutions for renewable energy sources, energy storage systems, and microgrids.

Dr. Lu was the Chair for the Joint Chapter Industry Application Society/ndustrial Electronicsy Society/Industry Application Society (IEEE New South Wales Section), from 2020 to 2023, and continues to support the Joint Chapter through his Past Chair role, since 2024. He is an Associate Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON POWER ELECTRONICS, and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.

FEI WANG (Senior Member, IEEE) received the B.Sc. degree in electrical engineering and the M.Sc. degree in power electronics from Zhejiang University, Hangzhou, China, in 2002 and 2005, respectively, and the Ph.D. degree in power electronics from the Eindhoven University of Technology, Eindhoven, The Netherlands, in 2010.

From 2005 to 2006, he was with the Philips Lighting Electronics Global Development Center, Shanghai, China. Since 2010, he has been a Faculty Member with the School of Mechatronics Engineering and Automation, Shanghai University, Shanghai, where he became a Professor in 2018. He has authored/coauthored more than 100 technical papers, one academic book, and also ten authorized invention patents. His current research interests include distributed generation, electrical drives, power quality, LED drivers, and smart grids.