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Abstract*—Silicon carbide (SiC) MOSFETs, as leading wide bandgap semiconductor devices, exhibit superior stability and reliability under high-temperature, high-switching frequencies, and high-power density operational conditions. SiC MOSFET with fan-out panel-level packaging (FOPLP) utilizes a redistribution layer (RDL) to substitute bonding wires, achieving low thermal resistance, electrical resistance, and parasitic inductance. This study proposes an optimal design strategy for SiC MOSFET FOPLP, considering parasitic inductance suppression, heat dissipation, thermal–mechanical reliability, and insulation enhancements. First, we establish the parasitic inductance, heat transfer network, and thermomechanical stress physical analytical models of SiC MOSFET FOPLP. Subsequently, the non-dominated sorting genetic algorithm (NSGA-II) and the improved multi-objective particle swarm optimization algorithm (MOPSO) are integrated to realize the co-optimization of parasitic inductance, thermal resistance, thermal stress, and electric field intensity distribution. Finally, we attain the optimal parameters of the SiC MOSFET FOPLP, i.e. chip thickness (x_1), solder thickness (x_2), RDL thickness (x_3), and chip side length (x_4) as 0.25 mm, 0.05 mm, 0.35 mm, and 6.00 mm, respectively. Additionally, according to comparison the MOPSO algorithm exhibits faster convergence and superior diversity than NAGA-II in the electrical–thermal–mechanical multiphysics co-optimization. Generally, the proposed physical analytical models combined with a multi-objective optimization method have a substantial guidance and forward-looking prospect on the design of SiC MOSFET FOPLP.

Keywords—SiC MOSFET; FOPLP; MOPSO; Analytical model; Genetic algorithms.

I. INTRODUCTION

In the Fan-out Packaging 2023 report by Yole Intelligence[1], the FOPLP market revenue was valued at approximately $41 million in 2022, with an anticipated significant CAGR of 32.5% over the next five years, reaching $221 million by 2028. Currently, silicon carbide (SiC) MOSFET is the predominant SiC power device, featuring rapid switching speed, high breakdown voltage, and excellent thermal conductivity. Widely employed in power converters to enhance conversion efficiency, SiC MOSFETs with fan-out panel-level packaging (FOPLP) utilize redistribution layer (RDL) to substitute bonding wire, achieving low thermal and electrical resistance and low parasitic inductance. Due to the higher chip occupancy ratio, FOPLP is expected to substantially decrease assembly costs while maintaining equivalent yields compared to fan-out wafer-level packaging.

The existing literature[2-4] predominantly focuses on enhancing the packaging process of power modules, such as SiC MOSFET FOPLP, to improve electromagnetic parameters, heat dissipation performance, and thermomechanical reliability individually. However, limited efforts have been devoted to the coupling relationship and simultaneous optimization of these crucial factors. Building upon our previous work[5], we propose a multi-objective optimization design method for parasitic inductance, thermal strain, and thermal resistance of SiC MOSFET FOPLP. We employ thermal cycling fatigue lifetimes to evaluate and validate our approach. However, the simulation-based data modeling method fails to capture the physical

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coupling mechanism between objective functions, and its time cost is very high.

Therefore, establishing a multi-field numerical analytical model combined with a multi-objective optimization method holds significant guiding relevance for the design and fabrication of SiC MOSFET FOPLP.

II. Electrical–Thermal–Mechanical Modeling of 1200-V Fan-Out Panel-Level SiC Mosfet Packaging

A. Structure of SiC MOSFET FOPLP

SiC MOSFET FOPLP primarily comprises SiC MOSFET chip, RDL, solder, solder pad, heatsink pad, and molding material (Fig. 1). This study employs the SiC MOSFET chip of ROHM semiconductor (S4601M), with rated voltage, current, and equivalent internal resistance of 1200 V, 136 A, and 12 m Ω, respectively. The gate surface and chip source are metalized with Ni/Pd/Au, and the drain surface is metalized with Ti/Ni/Au. Tin paste (Sn5Sb) serves as the die attach material. RDL connects the chip source and gate to their respective package pads. Part of the top radiator pad is embedded in the plastic material (EMC). The heat generated within the chip transmits through the package pad and top radiator pad, facilitating double-sided cooling.

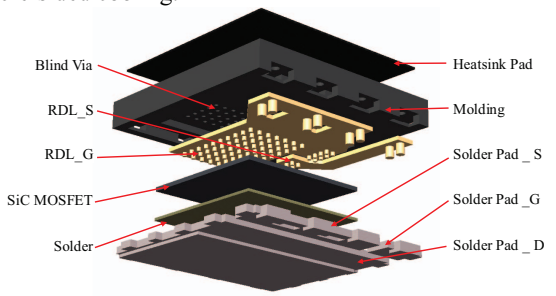

Fig. 1 Exploded view of SiC MOSFET FOPLP

B. Parasitic Inductance Modeling of SiC MOSFET FOPLP

Parasitic inductance (L) significantly influences SiC MOSFET performance. Lowering this inductor decreases turn-off loss and enhances reliability. SiC MOSFET FOPLP utilizes RDL instead of a conventional wire bonding package, substantially reducing the module's parasitic inductance. This study constructs a simplified parasitic inductance model of SiC MOSFET FOPLP to obtain lower parasitic inductance by optimizing the module's package structure.

The parasitic inductance of SiC MOSFET FOPLP comprises gate parasitic inductance (L_G), source parasitic inductance (L_S), and drain parasitic inductance (L_D). L_G and L_S are primarily determined by RDL structure. The RDL model (Fig. 1) is simplified as a series circuit segment of a rectangular conductor and two blind via arrays. The inductance of the blind via array is modeled as a multi-level parallel structure of multi-column cylinder-rectangular inductance. L_S and L_G can be expressed as follows:

$$\begin{cases} L_S = L_{SV} + L_{SB} + L_{SA} \\ L_G = L_{GV} + L_{GB} + L_{GA} \end{cases}, \tag{1}$$

where L_{SV} and L_{GV} denote the front blinds via array inductance; L_{SB} and L_{GB} represent the rectangular conductor inductance; L_{SA} and L_{GA} signify the blinds via array inductance.

The cylinder's inductance is determined using the material's electromagnetic properties and the cylinder's geometry. The self-inductance (L_r) and mutual inductance (M_r) of a cylinder can be expressed as follows[6, 7]:

$$\begin{cases} L_r = \dfrac{\mu_0\mu_r h_{via}}{2\pi}\cdot\left[\ln\left(\dfrac{2h_{via}}{r_{via}}\right)-\dfrac{3}{4}\right] \\ M_r = \dfrac{\mu_0\mu_r h_{via}}{2\pi}\cdot\left[\ln\left(\sqrt{\left(\dfrac{h_{via}}{p_{via}}\right)^2+1}\right)-\sqrt{\left(\dfrac{p_{via}}{h_{via}}\right)^2+1}+\dfrac{p_{via}}{h_{via}}\right] \end{cases} \tag{2}$$

where r_{via} and h_{via} represent the blinds via radius and height, respectively; μ_0 and μ_r denote the permeability of vacuum and relative permeability of the material; p_{via} signifies the distance between adjacent blind vias. The blind via RDL array has m rows and n columns. For the n-th row of blind vias, the self-inductance (L_n) and mutual inductance (M_n) are derived as follows:

$$\begin{cases} L_n = L_r/m \\ M_n = \sum_{i=1}^{m-1}\sum_{j=i+1}^{m} M_r \end{cases}. \tag{3}$$

The n-th column inductance (L_{rn}) is defined as the sum of its self-inductance and mutual inductance:

$$L_{rn} = L_n + M_n. \tag{4}$$

Rectangular inductance (L_b) can be expressed as follows[7]:

$$L_b = \mu_0\mu_r h/(2\quad)\cdot\left[\ln\left(2l/(a+b)\right)+(a+b)/3l\right]+0.5, \tag{5}$$

where a and b denote the length and width of the cross-section, respectively; l represents the rectangular conductor's length.

The inductance of the blind via array can be modeled as a multi-level parallel structure of n columns of cylinder-rectangular inductors (Fig. 2) as follows:

$$\begin{cases} 1/L_{A1} = 1/L_{r1} + 1/(L_b + L_{A2}) \\ \cdots \\ 1/L_{An-1} = 1/L_{rn-1} + 1/(L_{bn-1} + L_{An}) \end{cases}. \tag{6}$$

Drain parasitic inductance is primarily determined by the chip area and the thickness of the die-attach solder layer, modeled in combination with Eq. (3) as follows:

$$L_D = \sum_{j=1}^{2}\mu_0\mu_r h_j/(2\quad)\cdot\left[\ln\left(h_j/l_{chip}\right)+\left(2l_{chip}\right)/3h_j\right]+0.5, \tag{7}$$

where h_j signifies the thickness of each layer of the drain circuit; l_{chip} represents the chip side length. The total parasitic inductance of SiC MOSFET FOPLP can be expressed as:

$$L_0 = L_S + L_G + L_D. \tag{8}$$

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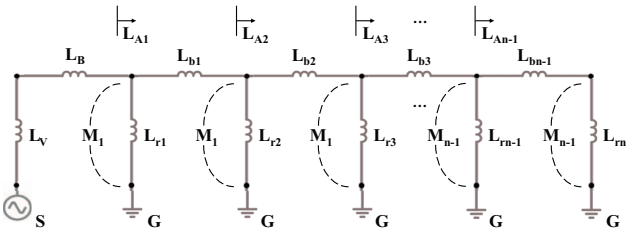

Fig. 2 Inductance Network Diagram of SiC MOSFET FOPLP

When the via pitch of RDL blind via array is defined as p_{via} = 0.4 mm, the parasitic inductance rises with higher row numbers and decreases with greater column numbers (Fig. 3) due to the parallel inductance between different columns. Moreover, maintaining a constant product of row and column numbers (effective conductive area), achieved by increasing column number and decreasing row number, yields lower parasitic inductance.

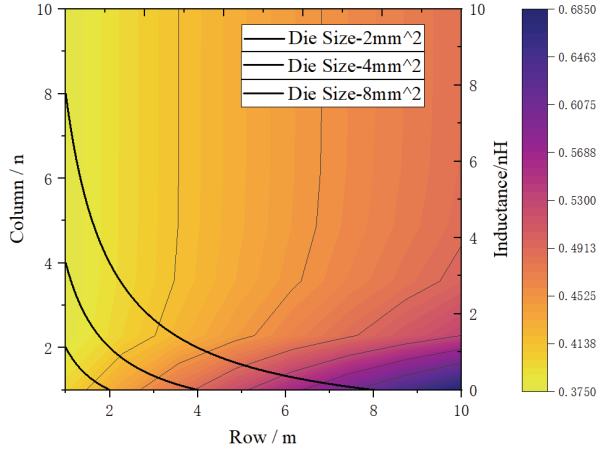

Fig. 3 The influence of row number and column number on parasitic inductance

C. Thermal Resistance Modeling of SiC MOSFET FOPLP

SiC power devices, having higher power density than conventional silicon devices, pose new challenges to the thermal reliability of SiC MOSFET FOPLP. Therefore, constructing a thermal resistance network model is essential for multi-objective collaborative optimization, considering thermal reliability as a crucial metric.

In SiC MOSFET FOPLP (Figs. 3 and 4), two heat transfer paths exist from the heat source (MOSFET chip): an upward path and a downward path. The paths are parallel to each other, enabling the computation of the thermal resistance of SiC MOSFET FOPLP crust as follows:

$$R_{thm} = R_{up}R_{down}/(R_{up}+R_{down}). \tag{9}$$

The upward heat transfer path thermal resistance (R_{up}) encompasses a rewiring layer, a plastic sealer layer, and a heat sink (i = 1, 2, 3, 4), while the downward heat transfer path thermal resistance (R_{down}) primarily includes solder and substrate (j = 1, 2). Following heat transfer theory, R_{up} and R_{down} of the upward heat transfer path can be derived as follows:

$$\begin{cases} R_{up} = \sum_{i=1}^{4} R_{thi} = R_1 + \sum_{i=2}^{4} \dfrac{h_i}{k_i A_i} \\ R_{down} = \sum_{j=1}^{2} R_{thi} = \sum_{j=1}^{2} \dfrac{h_j}{k_j A_j} \end{cases}, \tag{10}$$

where h_j, k_j, and A_j denote the thickness, thermal conductivity, and equivalent thermal conductivity area of the $i(j)$ layer respectively. Their specific values are listed in Table I.

The significant variation in thermal conductivity among different layers in SiC MOSFET FOPLP causes the heat flux in the vertical direction to undergo substantial changes, with noticeable transverse thermal expansion. Therefore, the thermal diffusion angle θ is introduced in Eq. (12) to enhance the accuracy of the thermal resistance model with the equivalent heat transfer area derived in Eq. (11).

$$\begin{cases} A_i = l_i^{\,2} = (l_{i-1} + 2h_i \tan\theta_i)^2 \\ A_j = l_j^{\,2} = (l_{j-1} + 2h_j \tan\theta_i)^2 \end{cases}, \tag{11}$$

$$\begin{cases} \theta_i = \arctan(k_{i-1}/k_i) \\ \theta_j = \arctan(k_{j-1}/k_j) \end{cases}. \tag{12}$$

In SiC MOSFET FOPLP, the significant contrast in thermal conductivity between blind vias and molding materials results in upward heat transfer along two parallel paths in the heavy wiring layer's blind via array (i = 1) of the copper blind via array and the plastic filler (R_{via} and R_{mol}). The equivalent heat transfer area of the blind via array and the plastic fillers are $A_{via} = p\pi r^2$ and $A_{mol} = A_1 - A_{via}$, respectively. The thermal resistances of the blind via array (R_{via}) and the plastic filler (R_{mol}) are expressed as:

$$\begin{cases} R_{via} = h_1/(k_{via}A_{via}) \\ R_{mol} = h_1/(k_{mol}A_{mol}) \end{cases}, \tag{13}$$

where r and P represent the radius and total number of blinds through holes, respectively. The thermal resistance (R_1) of the blind via array of RDL is deduced to be:

$$R_1 = R_{via}R_{mol}/(R_{via}+R_{mol}) \tag{14}$$

D. Thermal Stress Modeling of SiC MOSFET FOPLP

The ultra-thin power module package structure necessitates establishing an effective thermal-stress reliability evaluation model for the SiC MOSFET FOPLP package structure to yield electrical–thermal reliability collaborative optimization. During thermal cycling tests (TCT), SiC MOSFET FOPLP generates alternating stress and strain due to CTE mismatch among different layers. With an increasing number of cycles, the strain exhibits a cumulative effect, leading to potential package-level failures in the module, such as interface delamination, fatigue crack generation, and creep and creep cracking. The DARVEAUX model, an energy-based fatigue life prediction model, can be introduced as follows to evaluate crack propagation and fatigue life computation of SiC MOSFET FOPLP.

$$\begin{cases} N_0 = \tau_1 (\Delta W_{avg})^{\tau_2} \\ dA/dN = \tau_3 (\Delta W_{avg})^{\tau_4} \\ N_f = N_0 + A/(dA/dN) \end{cases}, \quad (15)$$

where N_f denotes the number of fatigue cycles (fatigue life); N_0 signifies the number of fatigue crack initiation cycles; dA/dN represents the crack growth rate; A is the characteristic area of fatigue cracks; τ_1–τ_4 are fitting coefficients obtained from fatigue experiments of packaging materials combined with Eq. (14). When the packaging material remains unchanged, the four coefficients can be approximated as constants. W denotes the average plastic strain energy density of SiC MOSFET FOPLP in each thermal cycle, determined by the thermal alternating stress from the thermal cycle aging experiment and the FOPLP's packaging structure size. Therefore, W serves as an evaluation index of the fatigue life of SiC MOSFET FOPLP during thermal cycles. The average inelastic strain energy density (ΔW_i) of each package component can be expressed as:

$$\Delta W_i = F_i \Delta h_i / V_i, \quad (16)$$

where F_i denotes the thermal stress of the i-th layer, defined by the amplitude of the vertical component of the thermal alternating stress generated by each layer packaging structure in a TCT cycle ($\Delta T = T_{max} - T_{min}$). Following the thermoelastic theory, the thermal stress (F_i) and the thermal strain ($\Delta h_i/h_i$) of the i-th layer are derived as:

$$F_i / S_i = E_i \Delta h_i / h_i, \quad (17)$$

TABLE I. MATERIAL PARAMETERS USED IN THERMAL AND MECHANICAL MODELING[3, 8]

Component	Material	K (W/m·°C)	CTE (ppm/°C)	E (GPa)	ν
Heatsink	Copper	401	18	110	0.34
Molding	EMC	1.5	9	15	0.38
RDL	Copper	401	18	110	0.34
Chip	SiC	58.6	5.1	400	0.14
Solder	SAC305	70	31	49	0.38
Baseplate	Copper	401	18	110	0.34

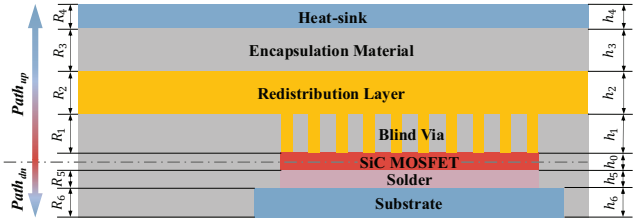

Fig. 4 Cross-section view of Fan-Out Panel-Level SiC MOSFET Packaging

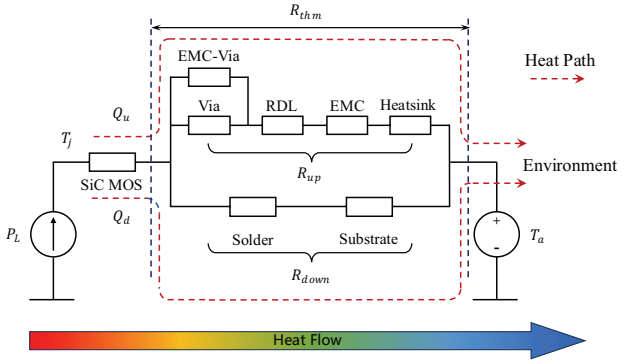

Fig. 5 Thermal network model of Fan-Out Panel-Level SiC MOSFET Packaging

$$S_i = \begin{cases} l_{mod}^2, & i = 1,2,3,7 \\ p \cdot \pi r_{via}^2, & i = 4 \\ l_{chip}^2, & i = 5,6 \end{cases}, \quad (18)$$

where E_i and α_i represent the elastic modulus and thermal expansion coefficient of the i-th layer of SiC MOSFET FOPLP, respectively; S_i denotes the normal projected area of the i-th layer, expressed as follows:

$$\Delta h_i / h_i = \alpha_i \Delta T. \quad (19)$$

The via portion of the RDL layer in SiC MOSFET FOPLP is represented by $i = 1$; r_{via} denotes the radius of a single via; p signifies the total number of via arrays in the RDL layer; l_{mod} and l_{chip} are the side lengths of the SiC MOSFET FOPLP module and the chip, respectively. Substituting equations (16) - (18) into Eq. (15) forms:

$$\Delta W_i = E_i \alpha_i^2 \Delta T^2. \quad (20)$$

Finally, the equivalent plastic work density is weighted by the volume of each part in SiC MOSFET FOPLP ($V_i = S_i h_i$) to yield the average plastic work density (ΔW_{avg}) as follows:

$$\Delta W_{avg} = \sum_{i=1}^{N} V_i \Delta W_i \Big/ \sum_{i=1}^{N} V_i. \quad (21)$$

III. Multi-Objective Optimization of SiC MOSFET FOPLP with NSGA-II and MOPSO

A. Multi-Objective Optimization Model

Following Eq. (8), Eq. (9), and Eq. (21), the parasitic inductance (L_0), module thermal resistance (R_{thm}), and average equivalent plastic work density (ΔW_{avg}), serve as optimization indices for the electrical, thermal, and mechanical characteristics of SiC MOSFET FOPLP, respectively, can be expressed as functions of chip thickness (x_1), solder thickness (x_2), RDL thickness (x_3), and chip side length x_4.

$$\begin{cases} L_m = f_1(x_1, x_2, x_3, x_4) = f_1(x) \\ R_{thm} = f_2(x_1, x_2, x_3, x_4) = f_2(x) \\ \Delta W_{avg} = f_3(x_1, x_2, x_3, x_4) = f_3(x) \end{cases}. \quad (22)$$

Utilizing parasitic inductance, module thermal resistance, and average equivalent plastic work density as optimization objectives, and chip thickness, solder thickness, RDL thickness, and chip side length as optimization variables, the multi-objective optimization model of SiC MOSFET FOPLP can be expressed as follows:

$$\begin{aligned} &\min_{x_i} F(x) = \left[f_1(x), \cdots, f_j(x) \right] \\ &s.t. \quad x = \left[x_1, \cdots, x_i \right] \in \Omega \quad \left[x_{i\min}, x_{i\max} \right] \end{aligned}, \tag{23}$$

where x denotes the decision variable; Ω signifies the decision space (Table II); i represents the dimension of the decision variable ($i = 4$); $f_1(x) \ldots f_j(x)$ are the objective functions ($j = 3$).

TABLE II. BOUNDARIES OF OPTIMIZATION OF SIC MOSFET FOPLP

Upper & Lower Bounds	Optimization Variables			
	x_1	x_2	x_3	x_4
Min (mm)	0.10	0.05	0.35	4.50
Max (mm)	0.25	0.20	0.50	6.00

B. Multi-Objective Optimization with NSGA-II and MOPSO

The electrical–thermal–mechanical collaborative optimization design of SiC MOSFET FOPLP constitutes a nonlinear mathematical model with multiple constraints and high-dimensional variables. For complex models with high-dimensional variables, the conventional multi-objective optimization algorithm exhibits poor convergence, failure to ensure individual superiority and slow processing. Therefore, the nondominated sorting genetic algorithm (NSGA-II) and multi-objective particle swarm optimization (MOPSO) algorithms are integrated to compute the Pareto solutions of the electrical–thermal–mechanical co-optimization model to form an automated multi-objective optimal design of SiC MOSFET FOPLP (Figs. 6 and 7).

NSGA-II is a rapid multi-objective optimization algorithm with an elitist strategy and based on Pareto optimal solutions, solving non-objective weight assignment problems[9]. NSGA-II exhibits exceptional performance in solving high-dimensional variable optimization problems and demonstrates superior comprehensive performance in addressing multi-objective optimization problems, mutation percentage, crossover percentage, and mutation rate are set to 0.4, 0.7, and 0.02, respectively. The maximum number of iterations and population size are set to 100 and 100, respectively.

The MOPSO algorithm is an efficient algorithm for addressing multi-objective optimization problems, relying on simulating particle motion and information exchange within the search space to determine optimal solutions. This algorithm

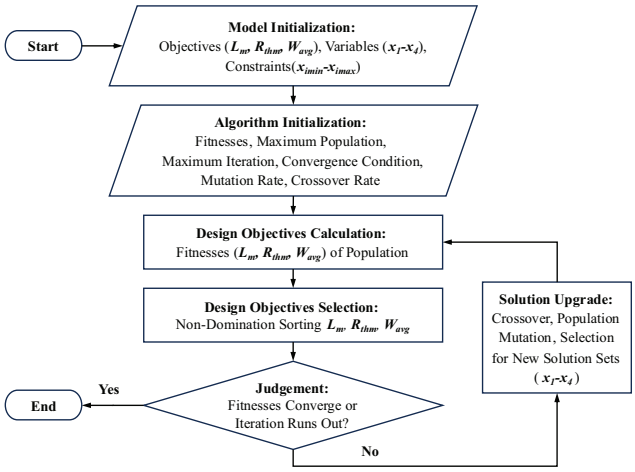

Fig. 6 Flowchart of automated multi-objective optimal design of SiC MOSFET FOPLP by using NSGA-II algorithm.

introduces a non-inferior solution set, offering several advantages in multi-objective optimization, providing decision-makers with multiple feasible solution options. Moreover, the MOPSO algorithm exhibits strong convergence and search capabilities, enabling the rapid discovery of global non-inferior solutions. The maximum number of iterations, population size, inertia weight, and its damping rate are set to 100, 100, 0.5, and 0.99, respectively, consistent with the NSGA algorithm.

C. Optimization Results and Discussion

The Pareto front of the multi-objective optimal design model for SiC MOSFET FOPLP using NSGA-II and MOPSO is illustrated in Fig. 8. Both algorithms demonstrate convergent optimization results for this multi-objective optimization problem. Convergence and diversity are crucial metrics for assessing the optimization quality of multi-objective optimization algorithms. In the objective space, the convergence ranges of objective function 3 for NSGA-II and MOPSO are [2.5, 2.85] and [2.55, 2.85], respectively, indicating superior convergence by NSGA-II in the electrical–thermal–mechanical collaborative optimization model of SiC MOSFET FOPLP. In addition, MOPSO's Pareto frontier solution set exhibits higher uniformity in the target space than that of the NSGA-II algorithm. This observation indicates that MOPSO algorithm generates more balanced and diverse solution sets in this optimization model.

When the iteration number and population size are both set to 100, the computation times of the MOPSO and NSGA-II optimization models are 39.015 seconds and 50.866 seconds, respectively. This observation demonstrates that the MOPSO algorithm achieves faster convergence while maintaining convergence and diversity. MOPSO outperforms NAGA-II in the electrical–thermal–mechanical collaborative optimization model of SiC MOSFET FOPLP.

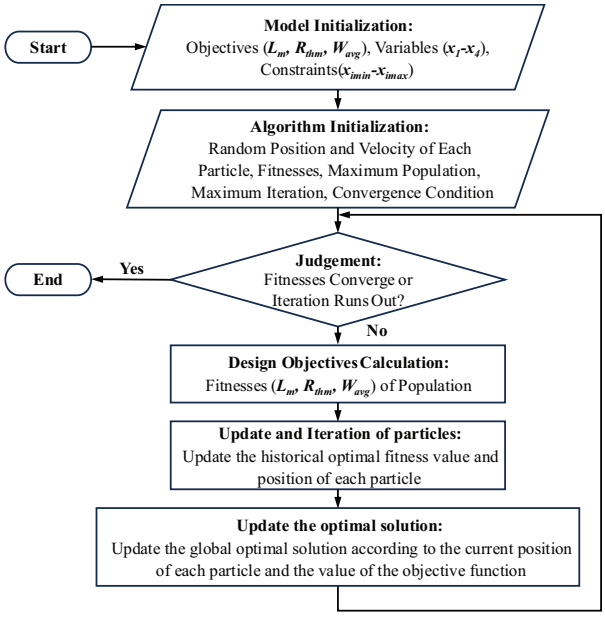

Fig. 7 Flowchart of automated multi-objective optimal design model of SiC MOSFET FOPLP by using MOPSO algorithm.

Optimizing parasitic inductance to its minimum value leads to a gradual increase in the corresponding optimal solutions of thermal resistance and equivalent plastic work density. Consequently, obtaining a solution becomes impossible within the Pareto optimal solution set that optimizes both electrical–thermal–mechanical evaluation indices simultaneously.

The electrical–thermal–mechanical optimal scheme for SiC MOSFET FOPLP is chosen from the Pareto optimal solution set using the technique for order preference by similarity to an ideal solution (TOPSIS). Using the selected optimal solution set, three objective functions serve as evaluation indicators, and TOPSIS is employed to assess and rank each solution (Fig. 9), and the top 10 solutions of the MOPSO algorithm are obtained. The forward-processing approach of evaluation indicators can be expressed as follows:

$$f_j^{'}(x)=\frac{f_{j\max}(x)-f_j^{'}(x)}{f_{j\max}(x)-f_{j\min}(x)}, \tag{24}$$

where $f_j^{'}(x)$ represents the objective functions $f_1^{'}(x)$, $f_2^{'}(x)$, and $f_3^{'}(x)$, respectively.

The top 10 solutions of the MOPSO algorithm in the Pareto optimal solution set and their decision and target space optimization results are listed in Table III. The SiC MOSFET FOPLP structure ranked first exhibits the lowest thermal resistance and thermal stress but does not minimize parasitic inductance. The structure ranked fourth achieves lower parasitic inductance but relatively inferior thermal–mechanical performance. Each module structure entails its advantages and disadvantages, allowing for selection based on the actual application scenarios of SiC MOSFET FOPLP. Consequently, the most suitable antenna structure scheme can be selected.

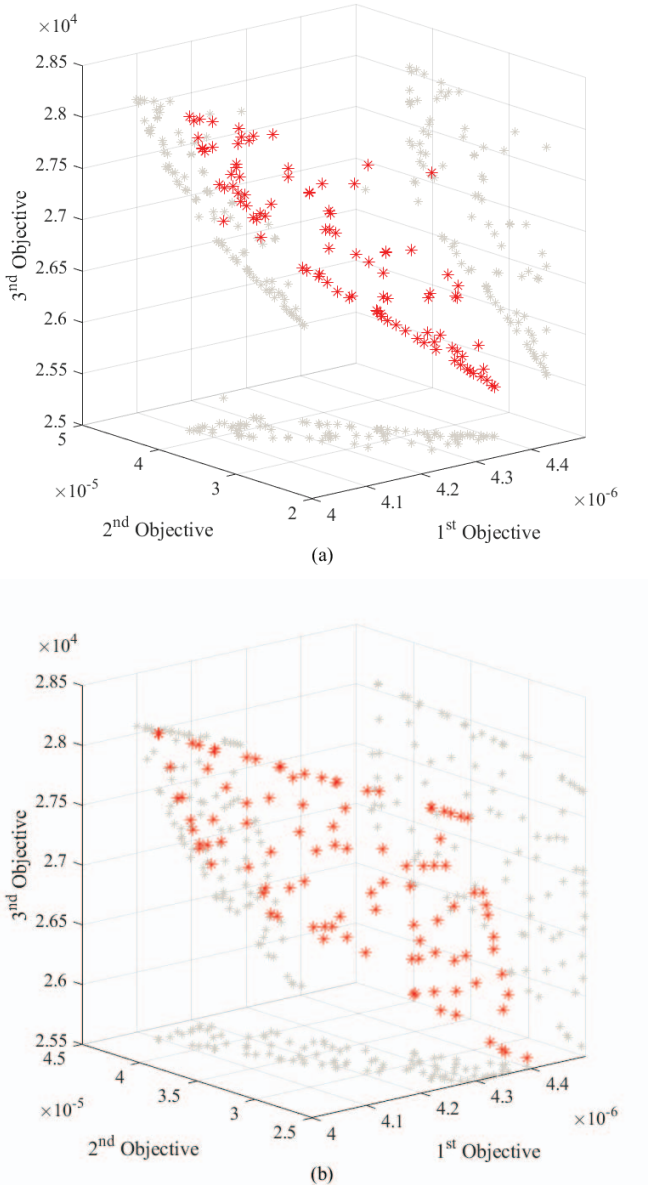

Fig. 8 Pareto front of multi-objective optimal design model of SiC MOSFET FOPLP. (a) NSGA-II, (b) MOPSO.

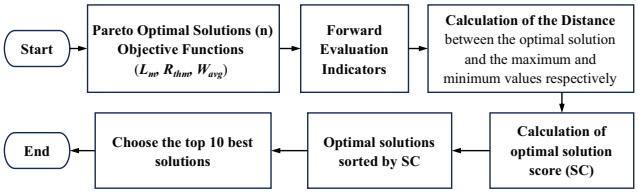

Fig. 9 TOPSIS Assessment Sequencing Flowchart.

TABLE III. TOP 10 SOLUTIONS IN PARETO OPTIMAL SOLUTION SET

N	Optimization Variables (mm)				Optimization Variables			SC
	x_1	x_2	x_3	x_4	$f_1(x)$	$f_2(x)$	$f_3(x)$	
1	0.25	0.05	0.35	6.00	4.405 E-06	2.511 E-05	2.548 E+04	8.493 E+03
2	0.25	0.05	0.35	5.98	4.402 E-06	2.531 E-05	2.550 E+04	8.500 E+03
3	0.25	0.05	0.35	5.94	4.398 E-06	2.561 E-05	2.553 E+04	8.509 E+03
4	0.25	0.05	0.35	5.92	4.396 E-06	2.573 E-05	2.554 E+04	8.513 E+03
5	0.24	0.05	0.35	5.92	4.394 E-06	2.576 E-05	2.556 E+04	8.519 E+03
6	0.25	0.05	0.35	5.87	4.389 E-06	2.620 E-05	2.558 E+04	8.527 E+03
7	0.25	0.05	0.35	5.73	4.374 E-06	2.744 E-05	2.569 E+04	8.564 E+03
8	0.24	0.05	0.35	5.77	4.366 E-06	2.707 E-05	2.581 E+04	8.603 E+03
9	0.25	0.05	0.35	5.50	4.345 E-06	2.965 E-05	2.587 E+04	8.623 E+03
10	0.25	0.05	0.35	5.49	4.342 E-06	2.971 E-05	2.587 E+04	8.624 E+03

IV. CONCLUSION

This study proposes an optimal design strategy for SiC MOSFET FOPLP, addressing parasitic inductance suppression, heat dissipation enhancement, and thermal–mechanical reliability optimization. The parasitic inductance, heat transfer network, and thermomechanical stress physical analytical models for SiC MOSFET FOPLP are established. It is observed that when the product of row and column numbers (the effective conductive area) is constant, increasing the column number and decreasing the row number yield lower parasitic inductance. The module's multi-field analytic model, the non-dominated sorting genetic algorithm (NSGA-II), and the improved multi-objective particle swarm optimization algorithm (MOPSO) are integrated to realize the cooperative optimal design of parasitic inductance, thermal resistance, and thermal stress. The optimal parameters settings of the power device FOPLP: chip thickness (x_1), solder thickness (x_2), RDL thickness (x_3), and chip side length (x_4) of 0.25 mm, 0.05 mm, 0.35 mm, and 6.00 mm, respectively, yield parasitic inductance, module thermal resistance, and average equivalent plastic work density of $4.405e^{-6}$, $2.511e^{-5}$, and $2.548e^{4}$, respectively. Comparison and evaluation of two optimization algorithms reveal that the MOPSO algorithm achieves faster convergence with superior diversity than NAGA-II in the electrical–thermal–mechanical collaborative optimization model of SiC MOSFET FOPLP. The proposed multi-field numerical analytical model combined with a multi-objective optimization method holds significant guiding implications and forward-thinking prospects for the design and manufacture of SiC MOSFET FOPLP.

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