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ARTICLE

Highly Transparent Gatable Superconducting Shadow Junctions

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ABSTRACT: Gate-tunable junctions are key elements in quantum devices based on hybrid semiconductor−superconductor materials. They serve multiple purposes ranging from tunnel spectroscopy probes to voltage-controlled qubit operations in gatemon and topological qubits. Common to all is that junction transparency plays a critical role. In this study, we grow single-crystalline InAs, InSb, and InAs$_{1−x}$Sb$_x$ semiconductor nanowires with epitaxial Al, Sn, and Pb superconductors and *in situ* shadowed junctions in a single-step molecular beam epitaxy process. We investigate correlations between fabrication parameters, junction morphologies, and electronic transport properties of the junctions and show that the examined *in situ* shadowed junctions are of significantly higher quality than the etched junctions. By varying the edge sharpness of the shadow junctions, we show that the sharpest edges yield the highest junction transparency for all three examined semiconductors. Further, critical supercurrent measurements reveal an extraordinarily high I_CR_N, close to the KO-2 limit. This study demonstrates a promising engineering path toward reliable gate-tunable superconducting qubits.

■ 100 nm

Shadowing with InAs NW Arrays

KEYWORDS: *semiconductor−superconductor nanowires, shadow junctions, ballistic transport, quantum computing, Majorana bound states, topological materials*
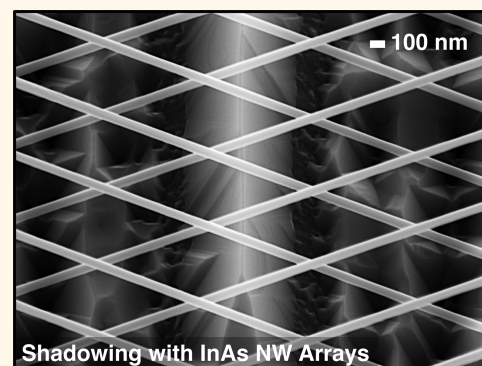
Josephson junctions (JJs) are critical circuit elements for superconducting quantum computing. Gate-tunable junctions based on proximitized semiconducting segments in hybrid semiconductor (SE)−superconductor (SU) materials are an interesting class of junctions with potential as JJ elements in transmons qubits[1,2] as well as critical operators in topological qubits.[3] Similar to all semiconducting circuit elements, they are highly susceptible to disorder and require dedicated optimization for development toward high-fidelity gate operations. In the case of topological quantum computing, achieving disorder-free junctions is desirable on several levels. Coupling a one-dimensional semiconductor with strong spin−orbit interaction and large Landé *g* factor to a conventional s-wave superconductor has the fundamental ingredients to generate topologically protected Majorana bound states (MBS).[4−8] If the material fulfills the set of requirements, MBS are expected to tolerate local perturbations and therefore making it a promising candidate for scalable quantum computing.[3,9,10] In recent years, there has been significant progress in the development of epitaxially grown SE−SU

hybrid materials to fulfill these requirements.[11−15] Even though electronic tunnel spectroscopy has yielded results that have been interpreted as signatures of MBS,[16−24] direct evidence for topologically protected MBS is still missing. Complications in the process of verifying the MBS with tunnel spectroscopy relate not only to the hybrid SE−SU nanowire (NW) segments but also to the tunnel junctions, which may contain random disorders that may give rise to local Andreev bound states that mimic the zero-bias conductance peaks expected from MBS.[25−27] Avoiding such misinterpretations is certainly desirable and a crucial reason to aim for disorder-free junctions. Junctions in spectroscopy devices have been demonstrated with a top-down etching process,[21,28,29] whereas
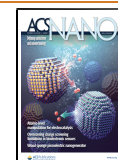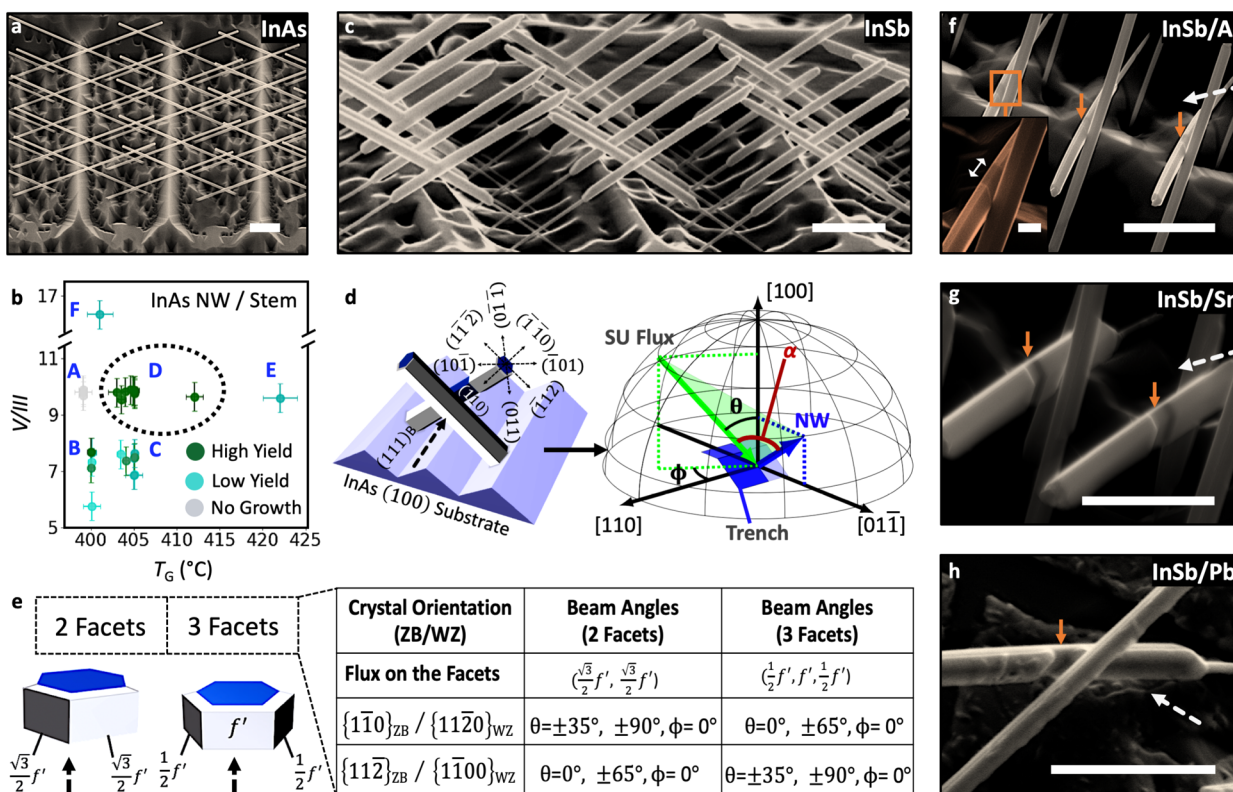
Figure 1. Semiconductor−superconductor nanowires with shadow junctions. (a) SEM (30° tilted) of Au-assisted InAs NW arrays grown on the preprocessed "V" groove (111)B faceted InAs trenches. (b) V/III ratio as a function of InAs NW growth temperature (T_G). The plot is divided into six regions (A−F), and NW growth outcome (yield, morphology, *etc.*) of each region is investigated. Region "D" ($T_G \sim 401-415$ °C with V/III ratio $\sim 9-10.5$) shows the highest yield and uniform InAs NW growth (dark green circles). (c) SEM image of InSb NWs grown from InAs stems. (d) Schematic of the hybrid NWs with a shadowed junction. Dashed arrow shows the superconductor deposition direction. On the right is a schematic of superconductor deposition geometry on the NW with respect to the beam flux direction and the NW growth direction. Here, α is the angle between these two vectors to calculate effective flux (f') on the NW facet. (e) Schematic of 2-facet and 3-facet superconductors on the NWs. The table provides beam angle requirements in the case when $\phi = 0$, for 2-facet and 3-facet superconductor coverage. (f) Tilted SEM image of InSb NWs with epitaxially grown Al. (g) SEM image of InSb/Sn NWs with junctions. (h) SEM image of an InSb/Pb NW with a junction. Orange arrows indicate the shadowed junctions. Dashed arrows indicate the direction of superconductor deposition. Scale bars for (a,c,f−h) are 1 μm. Scale bar for (f) inset is 100 nm.

a more recent alternative approach has been using an *in situ* method.[30−32] However, until now, a detailed investigation of the disorder-free junction formation along with correlations between fabrication and junction quality has been missing, which is highly required for further development of the gate-tunable junctions.

In this work, we study the synthesis of stacking-fault-free InAs, InSb, and InAs$_{1−x}$Sb$_x$ NWs with epitaxially grown superconductors containing shadowed junctions in a single-step growth process using molecular beam epitaxy (MBE). To obtain shadowed junctions at predefined positions, we use (111)B faceted trenches on InAs (100) substrates for NW growth.[31,33] This method provides freedom for controlled positioning of the shadow junctions due to the specified NW growth directions. We study the formation of junctions as a function of the interwire distance between the shadowing NW and the junction NW. We also analyze the junction profile, which directly depends on the flux distribution from the source and geometry of the shadowing. Further with different superconductors, we investigate the influence of growth kinetics on the junction sharpness. Developing a pregrowth substrate fabrication process including optimized growth condition and sharp-edge shadowing, we show high junction transparency with reproducible ballistic transport. Correlations

between the structural and electronic properties of the junctions are done by statistical characterization of the junction morphology and transport properties of junction NWs from selected positions on the growth substrate. We compare *in situ* shadowed and etched junctions on statistical ensembles of NW devices as well as on the same InAs$_{1−x}$Sb$_x$/Al NWs and confirm the superior electrical quality for the shadowed junctions. Finally, measurements at mK temperatures show $I_C R_N$ products over seven samples close to the KO-2 and KO-1 limit. Voltage bias measurements reveal the size of the induced superconducting gap, as well as a phase coherence of at least 5 times the junction length. All in all, the single-step ultrahigh-vacuum (UHV) crystal growth process with sharp-edge shadowing leads to high-quality junctions, which appears to be an ideal fabrication approach for gate-tunable superconducting junctions.

RESULTS AND DISCUSSION

Epitaxy of SE−SU Shadow Junctions. The NW substrates are fabricated using electron beam lithography (EBL) and wet-etching process to form (111)B facets in planar InAs (100) substrates, where the Au catalysts are positioned with a subsequent EBL process. As opposed to earlier works,[31,33] we do not use any masks to confine the Au

particles, which significantly reduces the preprocessing efforts and minimizes contamination during fabrication. This makes the process suitable for exploring different material combinations with high throughput. Figure 1a shows the scanning electron microscopy (SEM) image of InAs NWs grown from (111)B trenches. However, the NW growths on the trenches require careful optimization of the growth conditions. We find out that As_4 beam flux is necessary to enhance the initial NW growth rate to escape the competition with planar growth in the trenches. In Figure 1b, we show a map of InAs NW growth yield, which resembles the design of growth parameter optimization. Dark to light green color represents high (>90%) to low yield (<50%) growth of NWs, and gray resembles no growth. To help tuning in the right growth parameter space, we distinguish between six growth parameter regions, which are discussed in Supporting Information S2. The growth temperature window in region "D" with a V/III ratio of ~9−10.5 provides the highest yield and uniform morphology of the NWs, whereas outside of this region, the growth either has uneven yield issue or has nonuniform NWs. We mostly grow in the lower side of the growth temperature window in region "D", as we get a pure wurtzite (WZ) crystal structure at lower temperatures, verified by transmission electron microscopy (TEM) analysis (see Supporting Information S3). Confirming previous reports,[34] we are also not able to grow InSb NWs directly from the InAs substrate. It is speculated that the Au alloy forms a small contact angle to the substrate when Sb is present, which prevents initiation of NW growth.[34] However, once the InAs NW stem is formed, it is possible to switch into InSb NW growth. With optimized growth conditions (in region "D"), we achieve high yield InSb NWs across the substrate, as shown in Figure 1c.

Figure 1d shows the schematic of the NWs with a shadow junction as grown on the substrate. On the right, the hemisphere diagram shows the coordinates used to describe the superconductor beam flux direction with respect to NWs. Depending on the angle of the incoming flux and orientation of the NW facets, the superconductor can be grown on selected facets. The table in Figure 1e contains information on beam flux angles required for 2-facet and 3-facet superconductor coverage on $[1\bar{1}0]_{ZB}/[11\bar{2}0]_{WZ}$ and $[11\bar{2}]_{ZB}/[1\bar{1}00]_{WZ}$ oriented NWs. The amount of superconductor that is grown on each facet (for a given growth time) is proportional to the effective beam flux (f') on the selected facet. Here, f' is defined as the flux impinging on the midfacet facing the source during 3-facet deposition (see Figure 1e). If we consider 2-facet depositions, then both facets receive equal amounts of material, as an instance, for $\phi = 0$ and $\theta = 35°$, $f_{[\bar{1}01]} = f_{[011]} = \frac{\sqrt{3}}{2}f'$. For 3-facet depositions, the facet facing toward the beam receives f', whereas the adjacent facets get $f'/2$. The SEM images of InSb/Al NWs with *in situ* junctions are demonstrated in Figure 1f, where the inset shows a ~100 nm long junction. As the NW positions are controlled, it is possible to engineer multiple junctions in a single NW; see Supporting Information S5 for advanced junction schemes.

Synthesis of hybrid InSb/Sn NWs has recently been reported,[35] showing a route for deposition of alternative superconductors on bare semiconductor NW facets. Due to the simplicity of the single UHV-step process in our work, it is easy to vary not only semiconductor compositions but also superconducting materials, providing a versatile platform for exploring the wide range of interesting hybrid material

combinations. Two promising superconductor alternatives to Al are Sn and Pb, which both have higher T_c (for bulk, it is around 3.7 K for Sn and 7.2 K for Pb, compared to 1.2 K for Al). As these superconducting materials are challenging to etch selectively without damaging the semiconducting NW segments, the shadowing method may be critical for the realization of high-quality junctions. In Figure 1g,h, we demonstrate Sn and Pb films grown on InSb and $InAs_{1−x}Sb_x$ NWs (see Supporting Information S6), respectively. After the semiconductor NW growth, the Sn and Pb are grown on liquid nitrogen cooled stage in a UHV chamber connected to the MBE. Compared to Al and Sn, the growth of uniform Pb films on multiple facets of VLS NWs seems more challenging. Especially for InSb/Pb and $InAs_{1−x}Sb_x$/Pb interfaces, there is no obvious low index domain match without a high residual mismatch.[11] This indicates that the interface energy density is relatively high, which increases the thermodynamic driving force for dewetting; that is, it requires a lower growth temperature to prevent kinetic dewetting from occurring. Further, the shadowing and formation of the junction details are discussed below.

Comparison of Shadowed and Etched Junctions. Having growth conditions for InAs and InSb NWs on the trenches, the As and Sb fluxes can be tuned to grow $InAs_{1−x}Sb_x$/Al NWs,[12] as shown in Figure 2a. Similar to InSb NWs, we initiate the $InAs_{1−x}Sb_x$ NW growth with an InAs stem (using the recipe from Figure 1b, region "D"). The InAs stem is not visible in Figure 2a due to the overgrowth on the substrate. To enhance spin−orbit interaction[36] while maintaining an efficient field-effect response by keeping the carrier density low,[12,37] we aim for Sb composition around $x = 0.7$ (nominal Sb/As flux ratio of 0.8). The composition of the $InAs_{0.3}Sb_{0.7}$/Al NWs is measured applying Vegard's law[38] for the lattice parameter in ternary alloys (see Supporting Information S6 for scanning transmission electron microscopy (STEM) energy-dispersive X-ray spectroscopy analysis).

These $InAs_{0.3}Sb_{0.7}$/Al NWs are used to compare the field-effect response of etched and shadowed junctions, as shown in Figure 2b,c. The challenge for etched junctions is to find conditions that selectively etch Al while leaving the semiconductor unharmed. For instance, we have not been able to find selective etch conditions for Al on InSb. For $InAs_{0.3}Sb_{0.7}$ and InAs NWs, we use etch conditions which were optimized in previous studies and apparently leave the semiconductor intact[12,39] (see Supporting Information S7 for details). Because the electron transport characteristics vary from device to device, we need statistics for comparing quality measures. For this purpose, we compare 41 back-gated devices: 31 with shadowed and 10 with etched junctions; see Figure 2b. For etched junctions, 7 out of the 10 devices are first measured at 20 mK, out of which 6 pinch off with a threshold voltage of −3 ± 1 V, a mean saturation conductance of 1.6 ± 0.2 $2e^2/h$, and the field-effect mobility $\mu_{FE} \approx 1900 \pm 600$ cm^2/Vs (highest $\mu_{FE} \approx 4400$ cm^2/Vs). As a comparison, we measure nine shadowed devices under identical conditions, where four devices pinch-off with a mean threshold voltage of −36.0 ± 2.5 V and rest have not pinched-off within the applied gate voltage. The mean saturation conductance of all shadowed devices is 9 ± 1 $2e^2/h$.

For a higher throughput, we turn to measurement at 2 K and measure 22 devices with shadowed junctions where 20 devices pinch-off with a mean $\mu_{FE} \approx 17000 \pm 400$ cm^2/Vs (highest $\mu_{FE} \approx 35000$ cm^2/Vs). The mean threshold voltage and saturation conductance of these devices are −13 ± 2 V and 5.1 ± 0.5 $2e^2/$
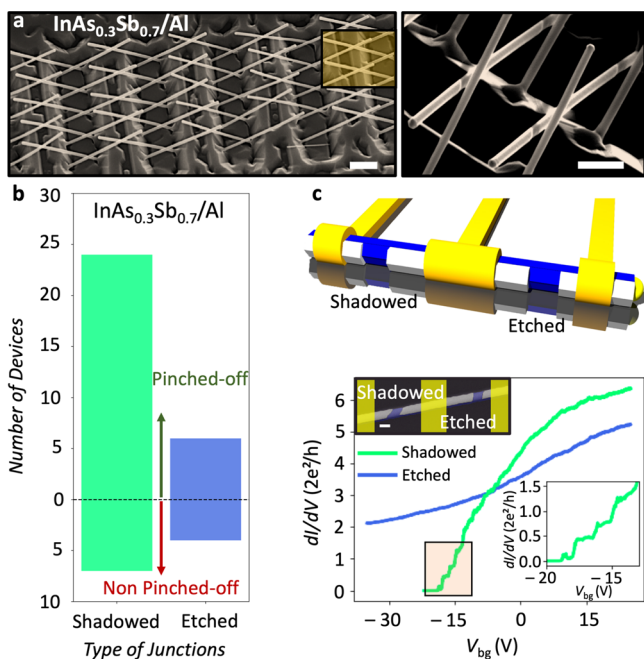
Figure 2. Gate response statistics of shadowed and etched junctions in InAs$_{0.3}$Sb$_{0.7}$/Al nanowires. (a) SEM image (30° tilted) of InAs$_{0.3}$Sb$_{0.7}$/Al NW arrays (scale bar is 1 μm). The highlighted section shows double shadowed junctions on the NWs (scale bar is 500 nm). (b) Pinch-off statistics of the back-gated devices with shadowed (green) and etched (blue) junctions. The y-axis contains the number of devices where the upper side of the dotted line shows devices that are pinched-off and the lower side shows devices that are not pinched-off. (c) Schematic of the test device with comparable size shadowed and etched junctions in a single NW. Below, electrical measurements of the test device where conductance is shown as a function of gate voltage for shadowed (green) and etched (blue) junctions. The shadowed junction shows quantized plateaus as highlighted with inset. Applied magnetic field, B = 6 T in both cases. SEM image of the exact NW is shown inset with a scale bar of 100 nm.

h, respectively. In comparison, three etched junctions are characterized at 2 K, showing a low gate response and no pinch-off within the voltage limits of the system and with mean saturation conductance of $4.1 \pm 0.7 \ 2e^2/h$. In short, according to the statistics presented above, shadow junctions exhibit a significantly higher conductance and mobility compared to the etched junctions.

As an additional comparison, we fabricate 11 devices with comparable sized etched and shadowed junctions in the same InAs$_{0.3}$Sb$_{0.7}$/Al NW (shown in Figure 2c). Among them, only three devices are functional on both sides, where the electrical measurement of one of these devices is demonstrated in Figure 2c. Despite the almost identical appearance of the etched and shadowed junctions in these devices, a radical difference is observed in the transport properties. Here, the shadow junction pinched off with clear quantized conductance plateaus around magnetic field, **B** > 4 T, whereas the etched junction is not pinched-off within the available voltage range. Similar differences are observed for the other two devices presented in Supporting Information S8. We note that there can be many reasons for disorders associated with etching such as undercut during wet-etching, increased SE surface roughness, impurities left from etchant, and leftovers from the etched metal (see Supporting Information S7). There are most likely ways to

improve etch recipes; however, unless the etch actively provides protection, it is reasonable to assume that optimized shadowed junctions will generally be of the highest possible quality. Additionally, besides obtaining higher quality junctions, shadowed junctions allow flexibility in the choice of material combinations, where selective etching may be infeasible. Based on this and the above results, we choose to solely focus on shadow junctions for all material combinations.

Evaluation of Sharp-Edge Shadowing. The influence of the junction edge morphology on the junction transparency is studied by comparing devices with varying edge sharpness. The edge sharpness is varied by changing interwire distance, l_s, between the shadowing and the shadowed NW. A junction is sketched in Figure 3a, where the transition region going from a fully shadowed region to a fully unblocked region (with nominal beam flux *f*) is given by

$$\Delta_b = \frac{W_S l_s}{L_{SW}}$$

Here, L_{SW} is the "source to wire" distance, and W_S is the width of the source opening. The effective flux in the transition region $f'(x_e)$ as a function of coordinate $0 < x_e < \Delta_b$ is directly related to the flux distribution across the source opening as

$$f'(x_e) \propto \int_0^{W_S - (L_{SW} \cdot x_e / l_s)} f_{source} \, dr$$

Here, f_{source} is the beam flux originating from a point source within a cutoff area up to $W_S - \frac{L_{SW}}{l_s} x_e$ of the source opening (cutoff determined by x_e), as shown in Figure 3a. Thus, a point in the transition region x_e sees a fraction of the source from where the effective impinging flux originates. If the outgoing flux distribution within the source opening is uniform, it can be shown that the effective flux in the transition region is given by

$$f'(x_e) = \frac{f}{\pi} \left[\frac{\pi}{2} - X_e \sqrt{1 - X_e^2} - \arcsin X_e \right]$$

where

$$X_e = \frac{2 L_{SW}}{l_s W_S} x_e - 1$$

Such an outgoing flux distribution originating from a uniform circular source opening would give a flux distribution in the transition region, as shown in the dashed green line in the inset of Figure 3a, whereas a uniform beam estimated from a 2D model (or from a hypothetical squared source opening) would provide a linearly increasing flux distribution as a reasonable approximation (as shown with the dashed black line). On the other hand, for a circular source opening with a Gaussian flux distribution, the transition region will see an effective flux closer to a step-profile flux distribution shown as a red solid line.

If the temperature is sufficiently low, such that the adatoms are kinetically limited to stick where they land ("hit and stick" model), the shape of the junction edges will directly map the flux distribution from the source opening as described above. However, the "hit and stick" model collapses if the adatoms are mobile. This will alter the broadening toward equilibrium shaped morphologies. The length scale at which kinetics plays a role can be described by a characteristic adatom migration length:[11,40]
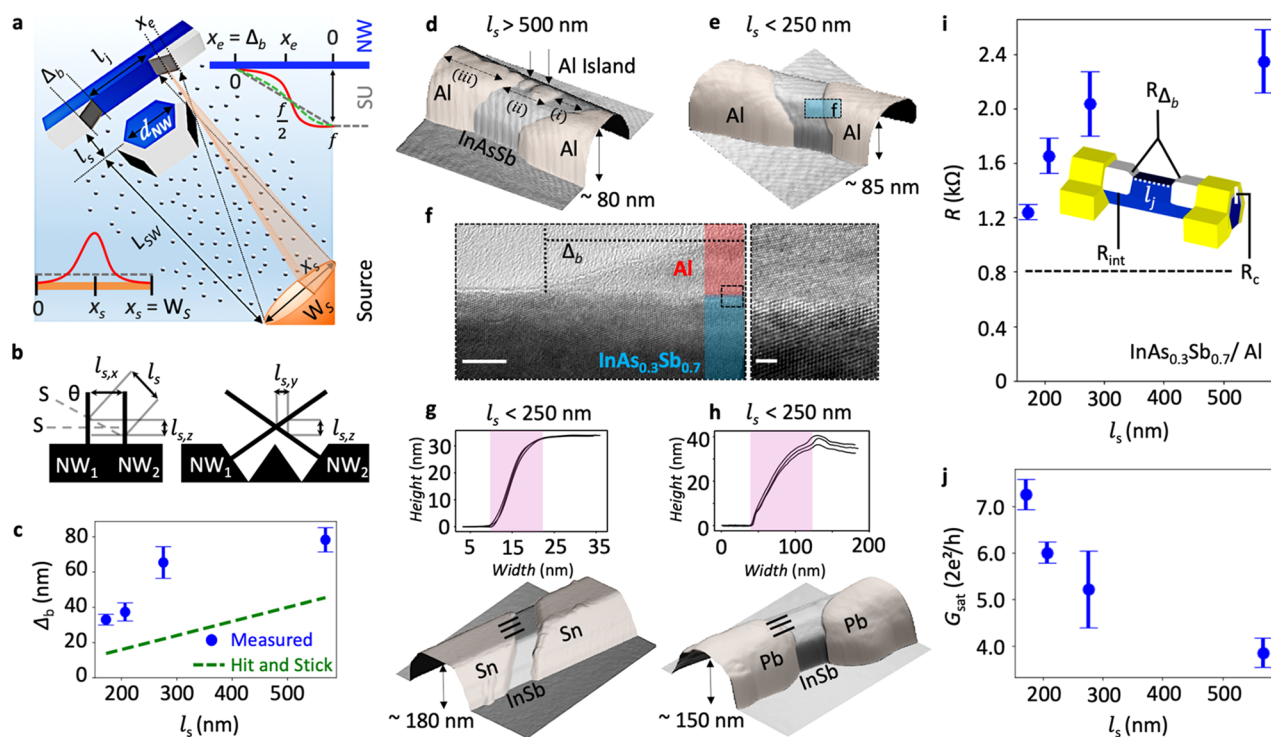
Figure 3. Edge profile effect on the junction performance. (a) Schematic of the SE−SU junction formation and the edge profile. The broadening (Δ_b) and profile of the junction edge can be determined by the flux distribution in the transition region, interwire distances (l_s), source to wire distance (L_{SW}), and effective width of the source (W_S). The junction length (l_j) depends on the size of the Δ_b and the diameter of the shadowing NW (d_{NW}) (diagram is not drawn to scale). (b) Geometry for determining the shadow position. (c) Δ_b as a function of l_s. Blue dots are measured Δ_b for Al junctions on $InAs_{0.3}Sb_{0.7}$ NWs, and green dashed lines are calculated Δ_b. (d) Atomic force micrograph (AFM) of the $InAs_{0.3}Sb_{0.7}$/Al junction for l_s > 500 nm. Large Al broadening with multiple Al grains are observed in the junction. Depending on the effective flux distribution on the transition region, the junction is divided into three sections: (i) clean segment, (ii) Al islands, and (iii) continuous film. (e) AFM of the $InAs_{0.3}Sb_{0.7}$/Al NW junction for l_s < 250 nm, where the junction is clean with a sharp-edge profile. (f) Zoomed-in TEM image from (e) shows the epitaxial SE−SU interface and small Al broadening in the junction. Scale bars are 5 and 1 nm, respectively. (g) AFM of the sharp-edge InSb/Sn junction shadowed by thinner InSb NW for l_s < 250 nm. The line scans, taken at the positions marked by black lines show the broadening of ~13 nm. (h) AFM of the InSb/Pb junction for l_s < 250 nm. The line scans show broadening of ~75 nm. (i) Gate-independent resistance of the shadow junction devices as a function of l_s. Inset is the schematic of standard device where R_{Δ_b} is the broadening resistance, R_c is the contact resistance, and R_{int} is the interface resistance. The dotted line until 0.8 kΩ represents the statistical value of contact resistance obtained by four-probe measurements. (j) Conductance saturation as a function of l_s.

$$\lambda_a \propto \sqrt{\frac{1}{\rho_a}} \exp\left(-\frac{\delta h_{aa} - \delta\mu_{inc}}{k_B T}\right)$$

where ρ_a is the adatom density, δh_{aa} and $\delta\mu_{inc}$ are a characteristic activation barrier for migration and chemical potential of the adatoms, respectively. As seen from this equation, also the beam flux (f) can play a role on λ_a, which complicates the analysis of the adatom kinetics due to the effective flux gradient in the transition region. To limit the adatom mobility, we grow the SU thin film at low substrate temperatures, where λ_a is sufficiently short to allow for the formation of a uniform thin film at the given flux.

The determination scheme of the shadow location is sketched in Figure 3b, where l_s (and therefore Δ_b) is controlled with two parameters, θ and $l_{s,x}$, the spacing between the Au dots along opposite trenches. For $\phi = 0$, the relation is simply

$$l_s = \frac{l_{s,x}}{\sin\theta}$$

These two parameters also determine the position of the shadow on the NW via the equations $l_{s,y} = \frac{l_s \cos\theta}{\tan 35.3°}$ and $l_{s,z} = l_s$

cos θ. As described above, Δ_b depends on $l_{s,x}$, which is controlled by the Au droplet positioning during substrate preparation. If the Au droplets offset on the opposite facets are within the d_{NW} range, then the NWs will merge to form nanocrosses or other type of networks.[30,33] However, for obtaining sharp-edged junctions, l_s needs to be as small as possible without merging. We vary l_s from ~170 to ~570 nm from trench to trench on a given substrate and measure the broadening on selected NWs with AFM. Figure 3c shows measured broadening (blue points) together with the calculated "hit and stick" broadening (green dashed line) for $InAs_{0.3}Sb_{0.7}$/Al junctions. Here, W_S ~ 1.6 cm and L_{SW} ~ 20 cm for Al deposition in our MBE. The measured mean broadening follows the trend of "hit and stick" model with an offset, which indicates that adatom kinetics plays an important role for Al shadow junction formation under these conditions.

A general trend is that small Al islands are formed in the junction region for l_s > 500 nm (as shown in Figure 3d). The junction edge broadening with discrete Al islands is estimated from fitting a curve over the measure islands. For l_s < 250 nm, we observe well-defined single junctions with no Al islands, as shown in Figure 3e and confirmed by a TEM image in Figure 3f. We attribute the larger broadening profile of Al shadow

edges than predicted by the "hit and stick" model to the kinetically driven equilibrium shape. For $l_s < 250$ nm, the Sn- and Pb-based junctions on InSb exhibit sharp-edge shadows, as shown in Figure 3g,h. In contrast to the Al deposition, we use e-beam evaporation of Sn and Pb, where the source opening W_S depends on how the electron beam is focused on the targeted materials. In the case of Sn, the effective area is visibly smaller than the area of the total target, which means that the effective source opening W_S and therefore Δ_b will be smaller for a given l_s in the case of "hit and stick" conditions. The outgoing flux distribution can be estimated with a Gaussian profile, as discussed in Figure 3a, leading to a sharp-edge flux profile in the transition region. Figure 3g with line scan showing $\Delta_b \sim 13$ nm confirms a sharp-edge profile of the Sn edge. Here, the measured sharpness may be underestimated due to the AFM tip diameter. On the other hand, for Pb-based shadowing, the outgoing flux distribution is more uniform from the source; as a result, Δ_b for the Pb-based junction is larger than that of Sn, ~75 nm, as extracted from line cuts in Figure 3h.

We study correlations between the junction transparency and the critical parameter for the junction profile l_s on the Al shadowed NWs. For this purpose, we calculate the gate-independent resistance R by fitting the pinch-off curves as described in Supporting Information S9. This gate-independent resistance contains mainly three contributions: contact resistance (R_c), broadening resistance (R_{Δ_b}), and SE−SU interface resistance (R_{int}). In Figure 3i, we can see that the InAs$_{0.3}$Sb$_{0.7}$/Al shadow junction resistance statistically increases with increasing l_s. Surprisingly, the junction resistance, R_{Δ_b} depends on the slope of the Al toward the junction, also for junctions without visible Al islands; however, the trend seems significant. For junctions with dewetted Al islands, it seems reasonable with a reduced junction transparency due to potential variations caused by Al islands across the junctions. Using standard four-probe measurements, the measured mean $R_c = 0.8$ kΩ, as shown in Figure 3i. Figure 3j shows conductance saturation of the devices decrease with increased l_s. We attribute this effect to the junctions with multiple Al grains for $l_s > 500$ nm. Unexpectedly, we also observe a trend of decreasing conductance for $l_s < 250$ nm, although Al grains do not form within this range. We presume the profile of broadening within that range may play a role in the conductance deviation.

Junction Transparency. We further investigate the device performances of the sharp-edged junctions for InAs, InSb, and InAs$_{0.3}$Sb$_{0.7}$ NWs. Pseudocolored SEM image of a typical single shadow junction device is shown in Figure 4a. In Figure 4b, we show the pinch-off voltages for Al-based junction devices measured at 2 K. The pinch-off voltages for InAs$_{0.3}$Sb$_{0.7}$/Al junctions show the widest span from approximately −30 to 0 V, whereas the InAs/Al junctions pinch-off in the range of approximately −5 to −20 V. On the other hand, InSb/Al junction devices show pinch-off at mainly positive V_g. We ascribe the statistical differences to the band alignment between the semiconductor and the Al.[41] An example of quantized conductance in the InAs$_{0.3}$Sb$_{0.7}$/Al junction device is shown in Figure 4c, where the conductance is measured as a function of V_g and magnetic field (**B**). A general trend is that the conductance plateaus are less pronounced at low **B** but gets gradually sharper with increasing field. This can be ascribed to lower electron backscattering rates at higher **B**. The first sub-
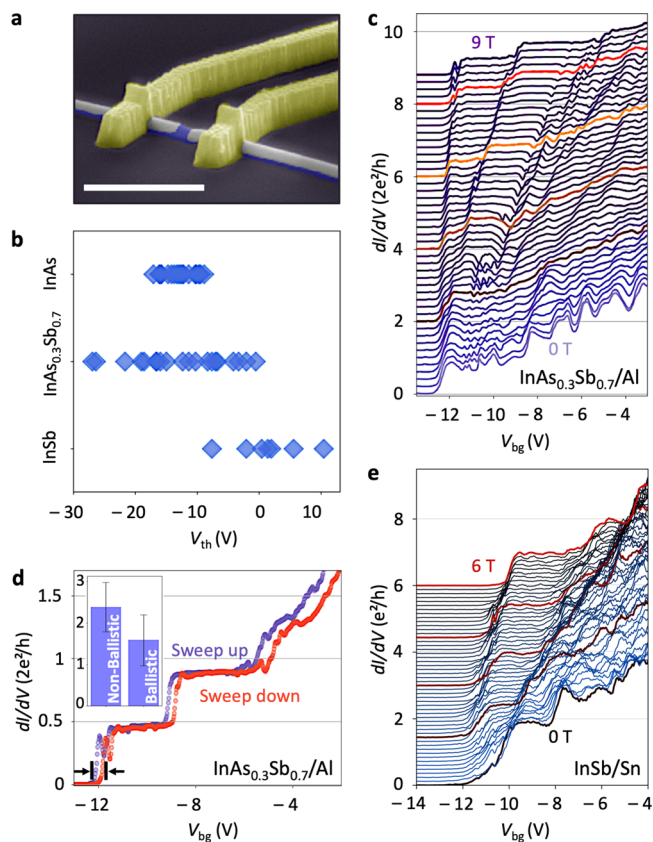

Figure 4. Ballistic transport in sharp-edged junctions. (a) Pseudocolored SEM image of a typical single-junction back-gated device. Scale bar is 1 μm. (b) Pinch-off voltage statistics for InAs, InAs$_{0.3}$Sb$_{0.7}$, and InSb NW junction devices. (c) Differential conductance as a function of gate voltage and magnetic field of an InAs$_{0.3}$Sb$_{0.7}$/Al NW junction. (d) Hysteresis of the device shown in (c), where sweeping up and down follows closely. Inset shows comparison of statistical value of hysteresis between quantized and nonquantized devices. (e) Differential conductance as a function of gate voltage and magnetic field for the InSb/Sn NW junction.

band splits into two spin-split sub-bands due to the Zeeman effect, which leads to an energy difference $g\mu_B$**B**, where g is the Landé g factor and μ_B is Bohr's magneton. For this particular InAs$_{0.3}$Sb$_{0.7}$/Al device, we see the emergence of the spin-split sub-bands around **B** > 2.2 T. However, we generally see the visible splitting appearing around **B** = 2−3 T. We speculate that the late emergence of visible spin-split bands is related to electron−electron interaction within the two sub-bands. The obtained quantized values in Figure 4c are lower than the predicted Ne^2/h because of the contact resistance, leading to the first subband at $0.45 \times 2e^2/h$, the second at $0.9 \times 2e^2/h$ and the third one is barely observed at $(1.3 \pm 0.5) \times 2e^2/h$. Figure 4d demonstrates a hysteresis that is much smaller than subband spacing in the device presented in Figure 4c. The inset shows a comparison of hysteresis statistics near the pinch-off region between quantized and nonquantized devices, where the quantized devices typically exhibit a slightly smaller hysteresis of ~1.5 V compared to others (~2.3 V). In Figure 4e, we examine a sharp-edge InSb/Sn junction device, with each trace offset by the value of the **B**. In contrast to the InSb/Al junctions, the devices with Sn show a negative pinch-off voltage around −10 V, caused by the different band alignment of Sn to InSb. In these devices, after the subtraction of the filter resistances in the refrigerator and a constant contact resistance,

a clear plateau at $2e^2/h$ is visible even at zero field, suggesting a scattering length on the order of a few hundred nanometers. Furthermore, unlike the sample shown in Figure 4c, splitting of the sub-band is visible immediately as the field is increased. A crossing of the first two spin-split sub-bands is visible around 2 T, characterized by the disappearance and re-emergence of a plateau at $2e^2/h$. This effect is expected due to the large Landé g factor of InSb.[42]

Figure 5 presents low-temperature ($T \sim 20$ mK) electrical measurements performed on seven InAs$_{0.3}$Sb$_{0.7}$/Al shadow JJs
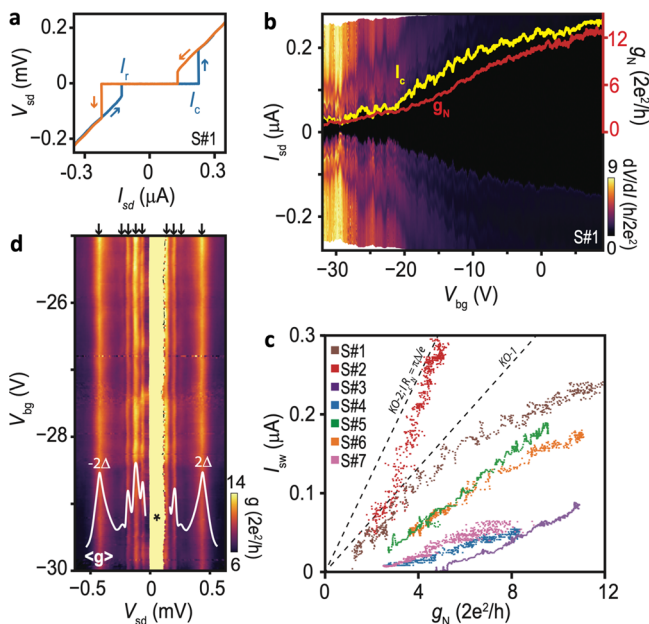

Figure 5. Supercurrent and multiple Andreev reflections in sharp-edged junctions. (a) Typical $V-I$ curve for an InAs$_{0.3}$Sb$_{0.7}$/Al shadow Josephson junction (device S#1). The switching and retrapping currents are indicated. (b) Differential resistance as a function of current and gate potential. The black region corresponds to the zero-voltage state. I_C and normal state conductance g_N measured at $B_\perp = 0.3$ T are shown. (c) I_C vs g_N for all measured devices. Dashed lines are the theoretical expectations. (d) Voltage-biased measurement of the subgap structure of S#1 showing resonances of multiple Andreev reflections. The high-conductance region asymmetric around zero bias (*) is related to a supercurrent branch enabled by the finite resistance of the cryostat wiring.

(S#1−S#7) with $l_j \sim 100$ nm. A single contact to the Al shell is fabricated from Ti/Au normal metal on either side of the shadow junction and split into separate bond-pads to allow for a pseudo-four-terminal configuration, eliminating contributions from highly resistive filters in the cryostat. The transmission of the junction is tunable by the back-gate potential V_g, and Figure 5a shows typical $V-I$ curves at $V_g = 0$ V for sample S#1. A zero-voltage state is observed corresponding to a switching current I_C exceeding 200 nA with pronounced hysteresis between up/down sweep directions, which is commonly observed in such devices and attributed to heating effects or an underdamped junction.[43,44] Figure 5b shows the differential resistance as a function of I and V_g. The zero-resistance state is clearly observed, and I_C decreases with V_g as the transparency of the n-type semiconductor weak link decreases toward pinch-off at $V_g \sim -40$ V. Also shown are the extracted gate dependence of the switching current $I_C(V_g)$ and the normal

state conductance $g_N(V_g)$ measured with a magnetic field of $B_\perp$ = 0.3 T applied perpendicular to the substrate and exceeding the critical field of the superconducting leads. The product of I_C and $R_N = 1/g_N$ is a typical voltage characterizing JJs, and Figure 5c shows I_C versus g_N for all devices where the range of g_N is spanned by sweeping V_g. For samples S#2−S#7, the curves are extracted from the data included in Supporting Information S12. The dashed line labeled KO-1 (KO−2) shows $I_C R_N = \pi\Delta/2e$ ($I_C R_N = \pi\Delta/e$) expected for a JJ in the short, quasi-ballistic and dirty (ballistic) regime with the mean-free path of $l_e \ll l_j \ll \xi$ ($l_e \gtrsim l_j$, $l_j \ll \xi$) and a superconducting gap of $\Delta = 200$ μeV expected for Al and matching voltage-biased measurements discussed below. ξ is the superconducting coherence length.[45] JJs with semiconductor NW weak links have been the subject of a large number of investigations since the original work of Doh,[43] and the critical currents in these devices are generally much lower than the KO-1 and KO-2 predictions and $I_C R_N$ significantly underestimates Δ.[46−48] The origin of this suppression is unknown but has been speculated to arise due to disorder and inhomogeneity or to heavily underdamped junctions. For the InAs$_{0.3}$Sb$_{0.7}$ shadow junctions studied here, the critical currents are relatively high, and samples S#1 and S#2 follow approximately the KO-1 and the ballistic KO-2 result. The remaining devices have suppressed I_C for high R_N, indicating the presence of channels with weak contribution to the supercurrent. At lower resistance, the increase in I_C with g_N follows the KO-1 slope, consistent with additional channels with contribution to I_C, as predicted by the model. We attribute these results to the high quality of the sharp-edge InAs$_{0.3}$Sb$_{0.7}$/Al shadow junctions and clean interface. For sample S#1, the phase coherence is confirmed by the voltage-biased measurement in Figure 5d, which shows a clear V_g-independent subgap structure which we attribute to multiple Andreev reflections (MAR) as previously studied in NW JJ.[43] The resonance resolved at lowest V_{sd} corresponds approximately to the n = fifth-order MAR $2\Delta/ne$ process requiring five coherent Andreev reflection processes. Higher-order MAR processes may be present but are inaccessible in these measurements due to the cryostat line resistances at $\sim$6 kΩ, making the measurement an effective current-biased measurement at low applied voltages.

CONCLUSION

In summary, we present a versatile single-step UHV crystal growth method to fabricate epitaxial SE-SU NWs with high quality gate-tunable superconducting junctions. The flexibility of the approach is exemplified with the growth of InAs, InSb, and InAs$_{0.3}$Sb$_{0.7}$ NWs with in situ shadowed junctions in Al, Sn, and Pb. Based on the performance statistics of field-effect InAs$_{0.3}$Sb$_{0.7}$/Al devices, we show that the quality of shadowed junctions are significantly higher than that of the etched junctions. Furthermore, for the shadowed junctions, we demonstrate that the junction transparency depends on the junction edge profile. We conclude that the junctions with sharp edges have high transparency, exhibiting extremely large supercurrents and easily resolved quantized conductance of the lowest sub-bands. The achieved results with sharp-edge shadowing in this work can also be transferable on the scalable selective area grown NW platform[13,49] through either post-growth in situ masking or prefabricated substrate with nanopillar/stencil bridge structure, which will act as a mask during SU deposition.[50] Hence, this study shows a path toward

reliable gate-tunable operations in superconducting quantum networks.

METHODS

Substrate Fabrication for NW Growth. InAs (100) undoped single side polished 500 μm thick 2 in. wafer is used to start the substrate fabrication for hybrid NW growths. Substrate preparation is discussed below:

Step 1: For exposure, we use electron-sensitive copolymer resist EL9 and spin with 4000 rpm (thickness ~320 nm) for 45 s. Next, hot plate baking of the resist is performed at 185 °C for 2 min to get rid of the solvent and improve the adhesion with the substrate. Lines for the trenches are exposed with EBL. For development, we dip the wafer into 1:3 MIBK/IPA for 45 s and IPA for 30 s, then oxygen plasma treatment for 2 min. **Step 2**: We use wet-etching to create (111) B faceted trenches. We etch the exposed lines to create V-shaped trenches with an angle of 54.7° using the following recipe: (i) Mix H_2SO_4 (1 mL)/H_2O_2 (8 mL)/H_2O (80 mL) and blend for 5 min with a magnetic stirrer. (ii) Take 4 mL of the above mixture, mix with 400 mL of H_2O, and blend for 5 min with a magnetic stirrer. The 2-in. wafer is then dipped into the solution for 30 min (for ~1 μm etching) or 60 min (for ~2 μm etching). Afterward, cleaning of the wafer is done as follows: (i) acetone for 4 min, (ii) sonication for 2 min with 80 Hz frequency and 30 W power, (iii) acetone for 10 s, (iv) IPA for 10 s and finally clean with Milli-q water for 30 s. **Step 3**: We performed dots exposure for Au particles. Two layers of resist are needed to coat homogeneously on the trenches. First, EL6 is spinned with 4000 rpm (~150 nm) for 45 s and baked subsequently for 1 min on a hot plate at 185 °C. Second, A2 is spinned with 4000 rpm (~60 nm) for 45 s and similar hot plate baking. The EBL system is used for dots exposure. For postexposure dots development, we dip the wafer into 1:3 MIBK/IPA for 45 s, IPA for 30 s, and then examine with the optical microscopy to confirm that the dots are properly aligned with the trenches. **Step 4**: Depending on the NW diameter, 7−15 nm thick Au layer is deposited at the rate of 1 Å/s on the wafer using an e-beam evaporator. If there is a time delay between resist development and Au deposition, it is crucial to remove the native oxide before Au deposition through hydrofluoric acid (HF) dipping or *in situ* Ar milling in the metal evaporation chamber. However, this is not needed if the Au deposition is immediately after the development. For lift-off, Au contained wafer is immersed into the acetone and kept for 10 min until the Au started lifting-off. Later, the acetone dipped sample is placed into a 50 °C heated bath for 1 h and then cleaning procedure of the wafer, which is similar to step 2. Finally, the ready-to-grow 2 in. InAs substrate with trenches is cleaved into four quarters to make it adjustable with the MBE growth holder and plasma ashed for 2 min (similar to step 1) to make sure no organic particles are left on the quarter.

Hybrid NW Synthesis Using MBE. Semiconductor−superconductor hybrid NWs are grown using the Veeco GEN II MBE system. Before loading in the MBE chamber, the fabricated substrate (1/4 of a 2 in. wafer) is dipped into diluted HF for 10 s and then rinsed for 20 s with Milli-q water to make sure the substrate is clean for loading. Initially, the sample is baked at 200 °C for 2 h in the entry/exit chamber of the MBE system, which confirms the vaporization of remaining water molecules from the substrate and then transfer to the buffer chamber. In the buffer chamber, the substrate is degassed for 1 h at 250 °C to confirm additional cleaning before being transferred into the growth chamber. In the growth chamber, the substrate is annealed for 2 min at 590 °C. All the intended effusion cells are heated up, and fluxes are stabilized before the growth. Here, InAs NWs on the trench are grown with As_4 overpressure maintaining the bulk temperature of the effusion cell at 345 °C and cracker temperature at 400 °C. After being annealed, the substrate is cooled to growth temperature within 5 min (linear cooling) and stabilized for 3 min before opening the In shutter for the growth. Right after the NW growth, the substrate is cool to 150 °C, and all the sources are set back to the base temperature. InSb NWs are grown with initial InAs NW stems where the growth procedure of

the stem is the same as described above. Maintaining the same substrate temperature, the As shutter is closed and the Sb shutter is opened, leading to InSb NW growth continued from the InAs stem. Finally, similar to InSb NWs, $InAs_{0.3}Sb_{0.7}$ NWs are also grown with InAs stems, where we tune the As flux for different compositions of the NWs. *In situ* Al deposition is performed in the MBE growth chamber by cooling the substrate holder to approximately −36 °C over 8−10 h right after the NW growth. When the desired temperature is reached, the substrate is aligned to the intended deposition angle. Before the deposition, the Al cell is heated to 1140 °C and flux is stabilized. Fifteen minutes of O_2 venting is performed while taking out the hybrid NW sample from the MBE chamber in order to form AlO_X to avoid dewetting. Further, Sn and Pb on the NWs are grown in the UHV metal deposition chamber (with liquid nitrogen cooling) which is connected to the MBE.

Structural Characterization of the Hybrid NWs. The morphology along with length and diameter of the grown NWs are examined with SEM. AFM is also used to characterize the surface morphology of the junctions, analyze broadening, and also to determine the thickness of SU. The atomic crystal structures of the NWs are characterized by TEM and high-resolution TEM. The structural properties, including lattice constant and atomic configuration, are analyzed using CrystalMaker for Windows (version 9.2.7, CrystalMaker Software Ltd.). For STEM tomography, NWs are transferred from the growth substrate to a TEM grid with a lacey carbon membrane using a micromanipulator. The grid is mounted on a Gatan tomography TEM holder, allowing tilting of samples from −70 to +70°. A Thermo Fisher Scientific S/TEM Talos F200X microscope is used to acquire high-angle annular dark-field STEM images at 200 kV, at steps of 1°. The Thermo Fisher Scientific Inspect 3D software is used for image alignment and reconstruction. 3D visualization is performed by the Thermo Fisher Scientific Avizo software.

NW Device Fabrication. The device fabrication process starts with transferring wires onto the prefabricated back-gated device chip using a micromanipulator. Two minutes of plasma ashing is performed before transferring NWs on the chip. Hybrid NW devices with SE−SU junctions are fabricated as follows: for InAs/Al NW devices, (1) spin resist AZ1505 on the chip with 4000 rpm for 45 s and bake the resist at 115 °C for 2 min; (2) UV lithography for source and drain electrode; (3) for development, AZ developer for 60 s, rinse in Milli-q water for 30 s, and later oxygen plasma treatment for 2 min; (4) to remove the oxidized NW surface, RF argon plasma milling is done for 8 min with 15 W power before depositing e-beam evaporated Ti and Au (5 and 200 nm) at the rate of 1−2 Å/s; (5) lift-off is done using acetone for 20 min; (6) cleaning procedure is done by hot bath of NMP at 80°C for 1 h, rinsing with acetone, dipping into IPA for 10 s, and then 2 min of oxygen plasma treatment; finally, baking the chip for 2 min at 185 °C. For $InAs_{0.3}Sb_{0.7}$/Al NW devices, (1) spin electron sensitive PMMA resist (A4) on the chip with 4000 rpm for 45 s and bake the resist at 115 °C for 2 min; (2) E-beam lithography for source and drain electrode; (3) for development, 1:3 MIBK/IPA for 45 s, rinse in IPA for 30 s, and later 30 s of oxygen plasma treatment; (4) RF argon plasma milling is done for 5 min with 7 W power before depositing evaporated Ti and Au (5 and 250 nm) at the rate of 2 Å/s; (5) 20 min of acetone dipping for lift-off; (6) for cleaning step, rinsing with acetone, dipping into IPA for 10 s, and then 2 min of oxygen plasma treatment. For InSb/Al NW devices, we follow the similar recipes as for $InAs_{0.3}Sb_{0.7}$/Al NW devices with following changes: in step (1) spin electron sensitive PMMA resist (A6) on the chip with 4000 rpm for 45 s, no hot plate baking is performed after resist spinning as the InSb/Al interface is subjected to damage at high temperature, instead the sample is dried through pumping for 2 h to get rid of the solvent of the resist; and in step (4) RF argon plasma milling for 4 min with 7 W power to remove the oxidized InSb NW surface.

PPMS Measurements. For electrical measurements, a physical property measurement system (PPMS, Quantum Design Inc.) is used with ~2 K measurement temperature and magnetic field up to 9 T. The device chip with daughterboard is mounted in the motherboard

and loaded in the PPMS system. Then the PPMS system is pumped to a pressure lower than 0.01 mTorr and then degassing is done for more than 10 h at 350 K. For InSb and $InAs_{0.3}Sb_{0.7}$ NW devices, the degassing is performed at room temperature. PPMS is then cooled to 10 K and supply evaporated liquid helium (H_4) in the chamber to further cool to the measurement temperature ($\sim$2 K).

20 mK Measurements. The devices for the superconducting measurements are fabricated on degenerately doped Si substrates with 200 nm of thermal oxide. The contact areas are patterned using standard electron beam lithography. As discussed before, the contact materials, Ti/Au (5/195 nm), are evaporated after an *in situ* argon milling process. The measurements are performed in a cryo-free dilution refrigerator at a base temperature of 20 mK. Critical current measurements are performed using standard lock-in and DC techniques with the use of a 50 kΩ shunt resistor. The clearly identifiable supercurrent shows a residual resistance. This is attributed to contact resistance and subtracted from the data set. The nature of the contact resistance lies in the measurement not being a truly four terminal; it bypasses only the filters in the refrigerator not the Ti/Au–Al contacts.

ASSOCIATED CONTENT

ⓈⒾ Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.0c02979.

Substrate preparation and NW growth (S1); growth map for InAs NWs on the trench (S2); TEM of InAs and InSb nanowire (S3); thin Al film growth on semiconductor NWs (S4); advanced shadow schemes for different junctions (S5); tomography and composition analysis of $InAs_{1-x}Sb_x$ NWs (S6); disorder in the etched junctions (S7); shadowed and etched junctions (S8); resistance calculation and field-effect mobility fit (S9); ballistic transport on InAs/Al, $InAs_{0.3}Sb_{0.7}$/Al, and InSb/Al junctions (S10); sharp-edge InSb/Sn junctions (S11); low-temperature ($T \sim 20$ mK) measurements on the junctions (S12) (PDF)

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Notes

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