Ping-Pong-Pang Instrumentation Amplifier

by

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in

Faculty of Electrical Engineering, Mathematics and Computer Science
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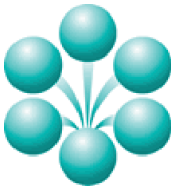

September 2010

Declaration of Authorship

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Abstract

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This thesis describes the implementation of a Precision Instrumentation Amplifier using a Current Feedback Instrumentation Amplifier topology (CFIA). CFIAs are attractive for sensor readout, because of their high CMRR and their ability to interface with ground-referenced sensors. Several chopping and auto-zeroing techniques have been developed to reduce the offset and $1/f$ noise of such amplifiers to the μV level. As a result, their dominant source of error is now gain error, which is limited by mismatch to at best 0.1%. This paper describes a CFIA that applies dynamic element matching (DEM) to achieve a gain error of less than 0.04%. Moreover, it presents the first silicon implementation of the ping-pong-pang (PPP) auto-zeroing scheme, which enables a 3.5× reduction in power consumption and 2.5× improvement in gain error as compared to state-of-the-art ping-pong auto-zeroed CFIAs.

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Dedicated to my parents and brother...

Chapter 1

Precision Instrumentation Amplifier

1.1 Introduction

Sensors are used to translate information from various physical domains (thermal, mechanical, magnetic) to information measurable in electrical domain. This electrical information is generally an analog signal and needs to be translated to digital signal for further signal processing. The system involved in the chain of converting the analog signal from sensors, to digital signal is called sensor readout system.

Figure 1.1 shows a typical sensor readout system (sensors output assumed to be in voltage). The differential voltage (V_{id}) from the sensor is amplified by the Amplifier (A) and given to an *Analog to Digital Converter* (ADC). ADC converts the signal to digital domain. This digital information is can be processed by a micro-controller. As typical sensor signals are very small (in tens of μV), an amplifier A is used to increase the signal before passing it to ADC.

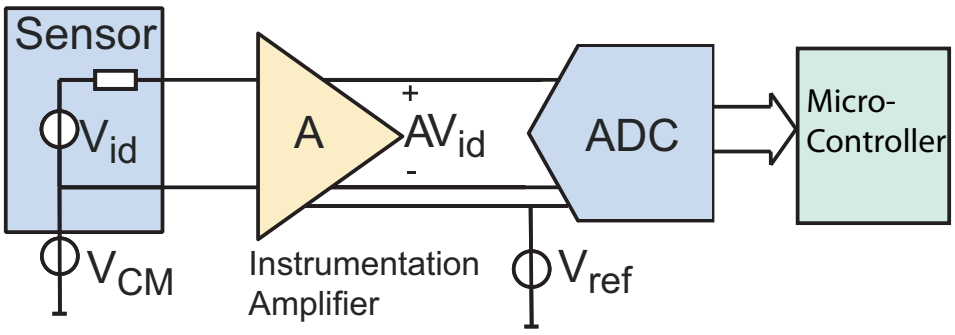

FIGURE 1.1: Typical Sensor readout system

The voltage V_{id} is a differential voltage, and can be as low as a few tens of micro-volt in case of sensors (thermocouple, strain-gauge). The voltage V_{CM} depends on the application (bridge readout or direct readout), and may vary by a few volts during the period of operation. *Instrumentation Amplifiers* (IA) are generally used for sensor readout applications, so as to accommodate the output signal characteristics of sensors. The main functions of an IA are to:

The main functions of Instrumentation Amplifier in this system are to

1. Amplify the weak differential voltage (V_{id}).
2. Reject the sensor Common Mode (V_{CM}) voltage.
3. Level shift to ADC reference voltage (V_{ref}).

As these amplifiers are used to detect very small input differential signals, the input referred errors (due to noise and offset) of such amplifiers should be well below the minimum input signal. Additionally these errors should have a very small drift over temperature, such that the IAs can be used for temperature measurements (eg for thermocouple readout). The IAs meeting such specifications are further classified as Precision Instrumentation Amplifiers. This chapter discusses about the precision IA which are generally used for sensor readout systems. It briefly discusses the practical design issues and solutions to over come them for implementing such IA. This chapter is organized as follows:

Section 1.2 discusses a topology to implement IAs, called as the *Current Feedback Instrumentation Amplifier* (CFIA). The CFIA is compared with other topologies of IAs and it's advantages over other IA topologies in sensor signal readout application are discussed.

These IAs are generally implemented in CMOS technology, owing to its low cost and low power digital processing capability. However IA designed in CMOS technology have non-idealities like offset (in the range of mV) and a very high flicker ($1/f$) noise. Sections 1.3 and 1.4 discuss the origin of offset and $1/f$ noise in CMOS amplifiers respectively. The performance of precision IA implemented in CMOS technology can be limited due to offset and $1/f$ noise. Section 1.5 discusses some techniques (particularly for CFIAs) used to cancel offset and $1/f$ noise for IAs implemented in CMOS. Section 1.6 discusses a non-ideality called gain error in CFIA. It discusses the cause for gain error in CFIA and introduces some techniques that can be used to minimize this non-ideality. A main objective of this thesis is an on-chip implementation of one of these techniques. Section 1.7 discusses the present state of the art in CMOS CFIAs, which further leads

to the specifications targeted for this work. Section 1.8 discusses the organization of the thesis and the main objectives of this work.

1.2 Current Feedback Instrumentation Amplifiers

IA can be implemented in different ways; some of the commonly used topologies are the three opamp IA, CFIA and switched-capacitor IA. The three opamp IA suffers from a limited *Common Mode Rejection ratio*(CMRR) due to resistor mismatch [1]. A switched-capacitor IA can be used to improve the CMRR, but it suffers from low input impedance. A CFIA can achieve better CMRR and input impedance as compared to three opamp and Switched Capacitor IA.

Figure 1.2 shows system level concept of CFIA. The differential input voltage (V_{in}) is converted to a differential current (I_{in}) by the input transconductor ($g_{m,in}$). When feedback voltage V_{fb} is applied to $g_{m,fb}$, it generates a differential current I_{fb}. V_{fb} is an attenuated version of V_{out} achieved through a resistive divider formed by R_1 and R_2. The amplifier A_{out} maintains V_{out} such that the sum of differential currents I_{fb} and I_{in} is zero under steady state condition. The output V_{out} is given by:

$$V_{out} = \frac{g_{m,in}}{g_{m,fb}} \cdot \frac{(R1 + R2)}{R2} \cdot V_{in} \tag{1.1}$$

$g_{m,in}$ and $g_{m,fb}$ can be made equal, giving the output voltage V_{out}

$$V_{out} = \frac{(R1 + R2)}{R2} \cdot V_{in} \tag{1.2}$$

Figure 1.2 shows the system level concept of CFIA.

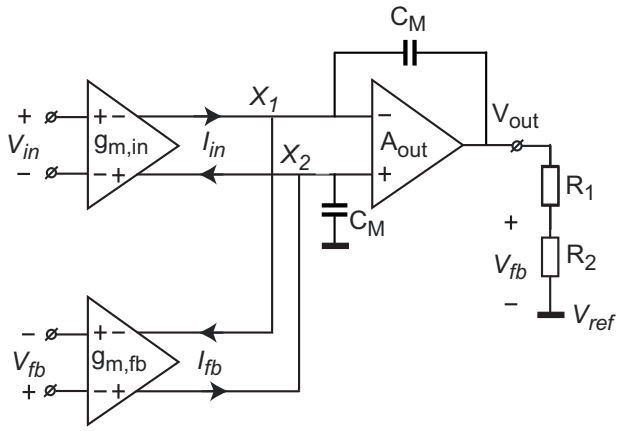

FIGURE 1.2: A Current Feedback Instrumentation Amplifier

This topology achieves a high CMRR as compared to three op-amp topology. It is because; the input transconductor $g_{m,in}$, isolates the input CM level by converting the input differential voltage to a differential current [1]. Hence, the CMRR will be determined by the CMRR of $g_{m,in}$. Another advantage of CFIA compared to the three opamp topology is that CFIAs can work in a large *Common Mode Voltage Range* (CMVR), which can include either of the supply rails [2].

1.3 Offset in CMOS amplifiers

Figure 1.3 shows a differential amplifier. The differential input signals ($V_{in+} - V_{in-}$) when applied to transistors M_1 and M_2, generate a differential output voltage ($V_{out+} - V_{out-}$). The resistors R_1 and R_2 act as a resistive load to the transistors M_1 and M_2 respectively. In ideal amplifiers, when the input differential signal is zero, the output differential signal is zero. However, in actual implementation, due to mismatch ($R_1 \neq R_2$ and $M_1 \neq M_2$), there is a finite DC voltage at the output even for zero input signal. This DC voltage is referred to as offset. The mismatch in components can be due to lithographic errors and variation in doping concentrations.

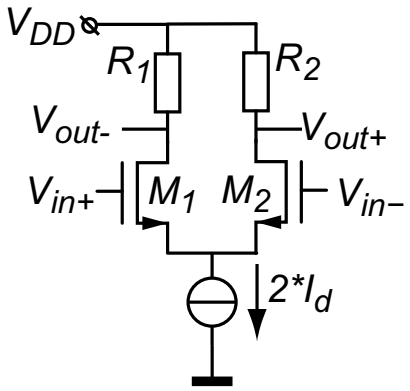

FIGURE 1.3: Differential amplifier in CMOS

This offset voltage can be expressed as:

$$V_{os} = \delta(V_{th}) + \frac{I_d}{g_m} \cdot (\frac{\delta R}{R} + \frac{\delta \beta}{\beta}) \tag{1.3}$$

Where, V_{th} is the threshold voltage of the transistors M_1 and M_2.
I_d is the drain current flowing in each transconductor.
g_m is the transconductance of the transistors M_1 and M_2.
β is given by $\beta = \mu_n C_{ox}(W/L)$

Where, μ_n is the mobility of electrons in silicon C_{ox} is the Gate capacitance of the transistors M_1 and M_2
W is the width of M_1 and M_2.
L is the Length of M_1 and M_2.

From 1.3, the first term $\delta(V_{th})$ refers to a threshold voltage mismatch between M_1 and M_2 and is in the range of $1mV$. The second term is dependent on the mismatch of resistors R_1 and R_2 and W and L mismatch of between M_1 and M_2. The second term is also multiplied by I_d/g_m, which is a temperature dependent term (the extent depends on the region of biasing). Hence, the expression 1.3 leads to an offset in mV level and a finite offset drift.

The effect of offset in CFIA is illustrated in Figure 1.4. When the input terminals are shorted, due to offset in $g_{m,in}$ a finite differential current is generated. Due to the CFIA operation discussed in section 1.2, a differential voltage (V_{fb}) will be generated at the inputs of $g_{m,fb}$, which will generate a differential current to cancel the differential offset current of $g_{m,in}$. This V_{fb}, with the inputs shorted, is the input referred offset of CFIA and is given by $V_{os1} - V_{os2}$.

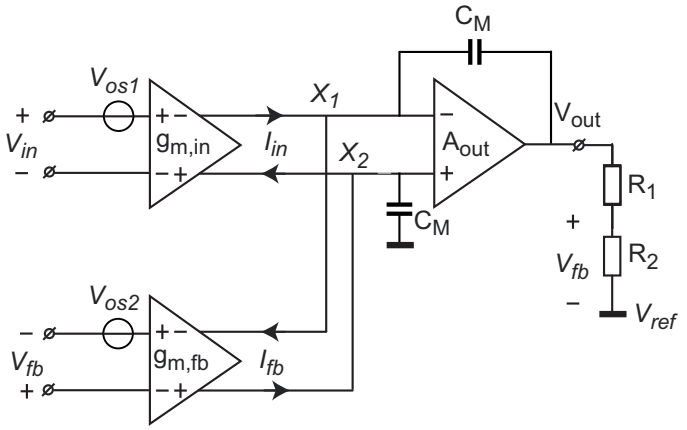

FIGURE 1.4: Error in CFIA due to offset

1.4 $1/f$ noise in CMOS amplifiers

Flicker noise is a type of noise, whose energy is mostly concentrated in low frequency regime. Its energy content at any given frequency is inversely proportional to the frequency. Hence, it is also referred to as $1/f$ noise. $1/f$ noise in a CMOS transistor is generated due to charge trapping in the gate oxide of CMOS transistors [3]. Figure 1.5 shows the typical DC and low frequency noise behavior for a CMOS amplifier. As seen

from the figure, the low frequency noise behaviour is dominated by $1/f$ noise. The frequency at which the $1/f$ noise contribution is equal to the white noise contribution is called as the corner frequency. This frequency in CMOS amplifiers can be in kHz range. Hence, $1/f$ noise in CMOS amplifiers can significantly impair its performance for low frequency applications like sensor signal readout. The presence of $1/f$ noise makes the design of precision IAs in CMOS technology more challenging.

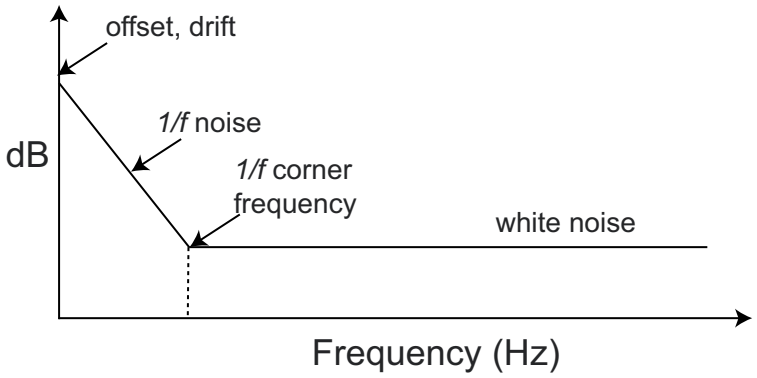

FIGURE 1.5: Noise in CFIA [4]

1.5 Offset compensation techniques in CFIA

Offset compensation techniques can be broadly classified into three basic categories: trimming, auto-zeroing and chopping. Auto-zeroing and chopping are preferred over trimming as they also cancel the offset drift and $1/f$ noise The following sub-sections discuss these techniques briefly, focusing on their application in CFIAs.

1.5.1 Trimming

Trimming involves adjusting the value of an on-chip component to cancel the offset of the circuit. An external setup is used to measure the offset of the fabricated device, and then the on-chip component is adjusted to reduce the offset. This technique requires some on-chip programmability to trim the offset. It also requires test infrastructure in the manufacturing facility. The method of trimming in CFIA is shown in Figure 1.6 [5]. An extra transconductor $g_{m,trim}$ is used, to which the offset compensation voltage V_{trim} is applied. The value of V_{trim} is changed externally until the resulting offset is minimized.

As trimming is a one-time operation it cannot compensate for non-idealities which change with time and conditions (offset drift and $1/f$ noise). Trimming can achieve

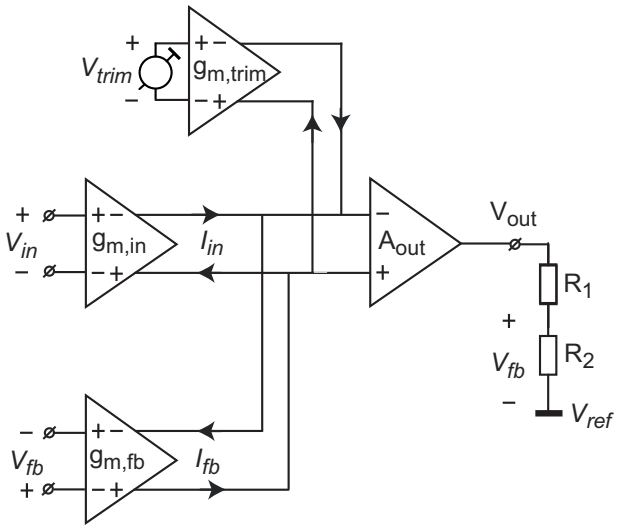

FIGURE 1.6: Offset Trimming in CFIA [5]

an offset of $200\mu V$ [ref] over the operating temperature range. To achieve better performance dynamic offset compensation techniques should be used. Dynamic offset compensation techniques can be classified into two basic techniques i.e. auto-zeroing and chopping. These techniques and their application in CFIAs are discussed in the following sub-sections.

1.5.2 Auto Zeroing in CFIA

Auto-zeroing is a technique which measures the offset and then cancels it from the signal. Auto-zeroing basically works in two phases. In phase 1 the offset is stored, and during the next phase the signal is amplified and the stored offset is cancelled from the signal. Depending on the way the offset is stored and later cancelled, the auto-zeroing technique can also be classified into two categories: input offset storage and offset storage on an auxiliary node. These techniques are briefly described below. Moreover, the noise performance of auto-zeroed amplifiers is also discussed.

Auto-zeroing with Input Offset Storage in CFIA

Figure 1.7 illustrates auto-zeroing in a CFIA using input offset storage. The input and feedback transconductor have offset V_{os1} and V_{os2} respectively. During the auto-zeroing phase F_1, the inputs of $g_{m,in}$ and $g_{m,fb}$ are shorted and they are connected in a unity-gain feedback configuration. The resulting input offsets are stored on capacitors C_{A1} to C_{A4}. During the phase F_2 the signal is applied, as the offset is stored in capacitors C_{A1} to C_{A4}, the offset is subtracted from the input signal before it is amplified. This leads to an offset free amplification of the input signal.

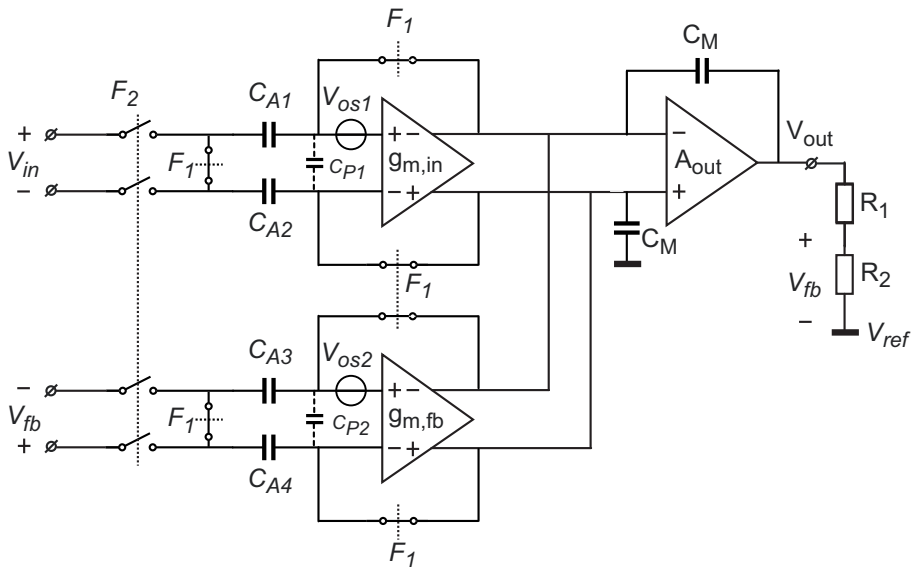

FIGURE 1.7: Auto-zeroing in CFIA using input offset storage

The input CM level of $g_{m,in}$ and $g_{m,fb}$ is separated from the input CM level by the offset storing capacitors C_{A1} to C_{A4}. Hence this topology can be used to sense a Common Mode Voltage Range (CMVR) that includes both the supplies [4]. One drawback of this topology is that the input parasitic capacitances C_{P1} and C_{P2} of $g_{m,in}$ and $g_{m,fb}$ along with the offset storage capacitors, act as a attenuation network for the input voltage. This alters the overall gain of the amplifier[4].

Auto Zeroing in CFIA with offset storage on auxiliary node

Figure 1.8 shows an auto-zeroed CFIA that uses auxiliary offset storage [6]. During phase F_1 the input terminals of $g_{m,in}$ and $g_{m,fb}$ are shorted. The net current generated due to the offsets of $g_{m,in}$ and $g_{m,fb}$ is then integrated on the auto-zeroing capacitors C_{az}. This continues until $g_{m,aux}$ generates a current I_{oc} that cancels the net offset current. The corresponding voltage required is stored in the capacitors C_{az}. During the phase F_2, the input and feedback terminals are connected. The amplifier A_{out}, generates voltage V_{out}, which makes V_{fb} such that the net sum of I_{in}, I_{fb} and I_{oc} are zero. As I_{oc} represents the offset information, hence subtracting it from the sum of I_{in} and I_{fb}, results in an offset free amplification of input voltage.

Noise in auto-zeroed CFIA

As the auto-zeroing capacitors store the output signal of the amplifier when the input is shorted, the accumulated charge along with the DC offset term also contains frequency components. Hence, these components (like $1/f$ noise) are also cancelled by the auto-zeroing operation. However a disadvantage associated with auto-zeroing is that any thermal noise component above the auto-zeroing frequency will alias into the signal

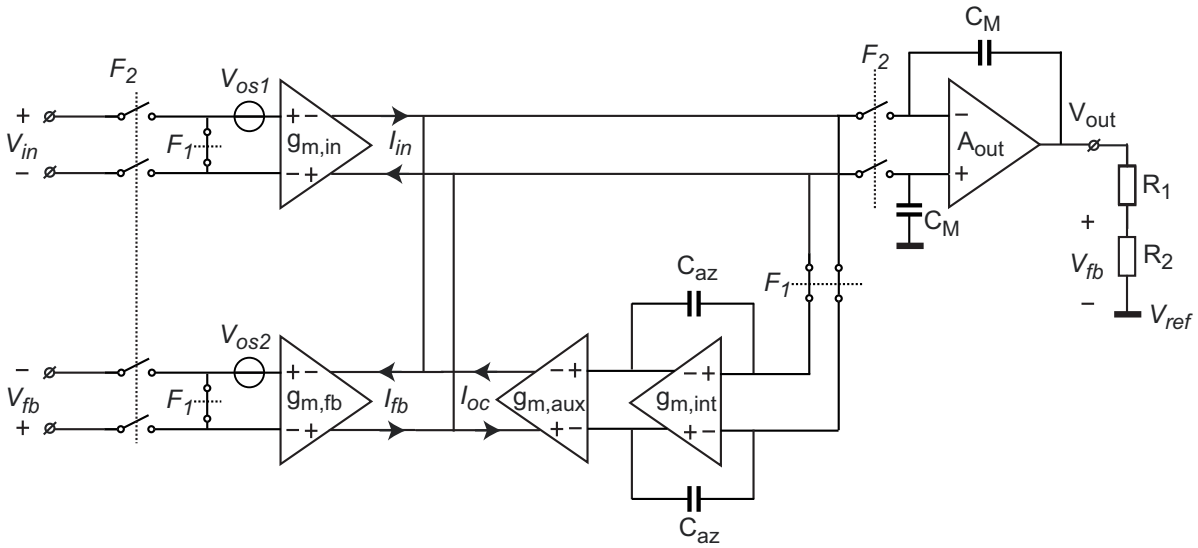

FIGURE 1.8: Auto-zeroing in CFIA with offset storage in auxiliary node

band, due to the sampling action of the auto-zeroing operation. This increases the thermal noise floor at low frequencies. Figure 5 shows the *Power Spectral Density*(PSD) of an amplifier with and without auto-zeroing [4].

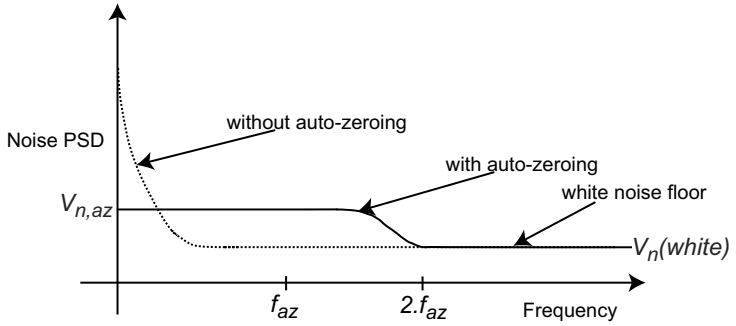

FIGURE 1.9: Noise folding due to Auto-Zeroing [4]

As seen from Figure 1.9, the $1/f$ noise is cancelled but due to aliasing of high frequency noise in signal band the noise level in frequencies below $2 \cdot f_{az}$ is higher than the thermal noise floor. To achieve a thermal noise floor in auto-zeroed amplifiers, chopping is used to modulate the folded noise to high frequencies [tang].

The extra noise added $V_{n,az}$ can be calculated by using [7]

$$V_{n,az} = V_n(white) \times \sqrt{(BW_{az})/(f_{az})} \tag{1.4}$$

Here,$V_n(white)$ is thermal noise voltage, BW_{az} is bandwidth of auto-zeroing loop and f_{az} is frequency of auto-zeroing. For complete cancellation of $1/f$ noise in amplifiers the auto-zero frequency should be higher than the $1/f$ noise corner frequency [8].

As auto-zeroing is a sampling technique, which requires time to sample the offset and then cancel it from the signal. Hence, the auto-zeroed amplifier is not amplifying the input signal in a time continuous fashion. To achieve a continuous-time signal at the output, technique like Ping-Pong auto-zeroing [7, 9] is used.

1.5.3 Chopping in CFIA

Chopping is a modulation technique which modulates the offset and low-frequency noise of the input stage away from the signal band of interest. Chopping in a CFIA is illustrated in Figure 1.10

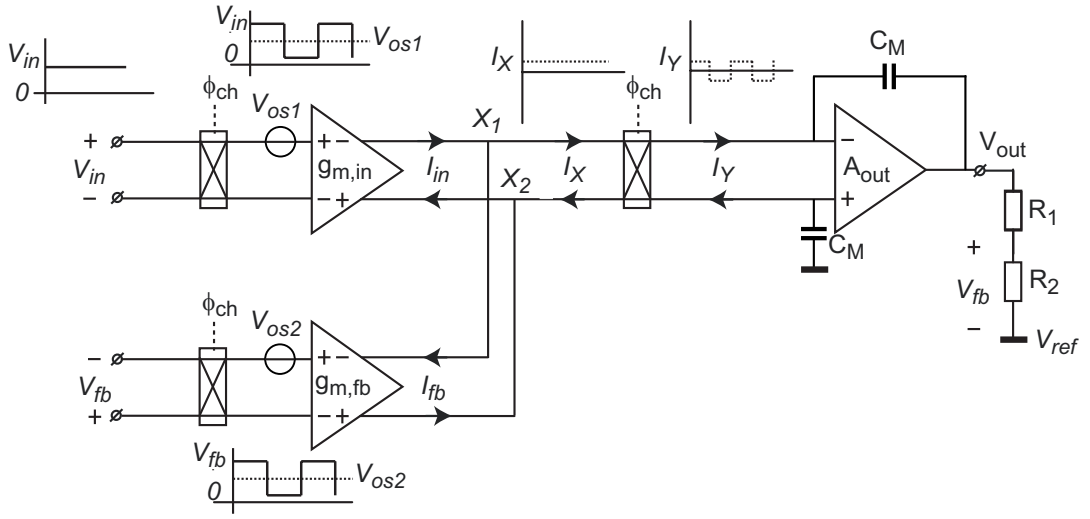

FIGURE 1.10: Chopping in CFIA

The input and the feedback signals are modulated to a higher frequency by input choppers. Then, the modulated voltages are converted to currents by transconductors $g_{m,in}$ and $g_{m,fb}$. The modulated signal current is cancelled if $V_{fb} = V_{in}$. The differential DC current I_x flowing at node X_1 and X_2 can be given by $g_{m,in} \times (V_{os1} - V_{os2})$. The chopper following the summing node I_X, modulates this current to higher frequency(I_Y). This modulated square wave current is then integrated by the Miller capacitors C_M and converted to a triangular voltage. The output voltage now consists of a DC voltage equal to the gain setting times the input voltage and a ripple voltage at the chopper frequency which is proportional to the offset. In the frequency domain, chopping can be represented as shown in Figure 1.11. The chopping action not only modulates the offset, it also modulates the low frequency noise of the amplifiers to a higher frequency. Hence with chopping, thermal noise floor at DC and low frequencies can be achieved.

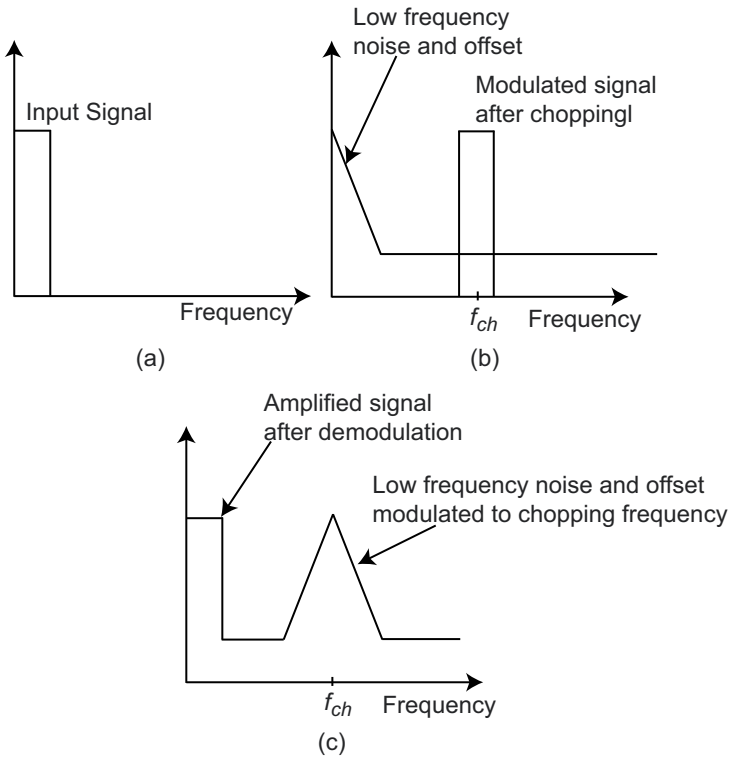

FIGURE 1.11: Chopping in CFIA[4]

In the case of chopping the modulated DC component appears as a ripple at the output of the amplifier. This ripple can cause sampling errors in the ADC following the IA[ref]. Over the years many circuit techniques have been used to reduce the ripple, [5] discusses the related advantages and disadvantages of such techniques.

1.6 Gain error in CFIA

This section introduces the problem of gain error in CFIAs and the various techniques that can be used for reducing the gain error. Figure 1.12 shows a CFIA, with input and feedback transconductance as $g_{m,in}$ and $g_{m,fb}$.

The transfer from V_{in} to V_{out} for Figure 1.12 is given by equation 1.1. In the previous discussions we have considered that for $g_{m,in} = g_{m,fb}$, this gives an ideal transfer from V_{in} to V_{out} which only depends on the resistor ratio.

Mismatch in the components defining the gain in CFIA, can lead to deviation of gain from ideal value. This deviation in CFIA can be due to two reasons, i.e. due to mismatch in $g_{m,in}$ and $g_{m,fb}$ (g_m mismatch) and due to mismatch in resistor values. The mismatch in $g_{m,in}$ and $g_{m,fb}$ is due to process variations in IC technology. The gain error related to resistor mismatch is not under designers control as the feedback network is typically

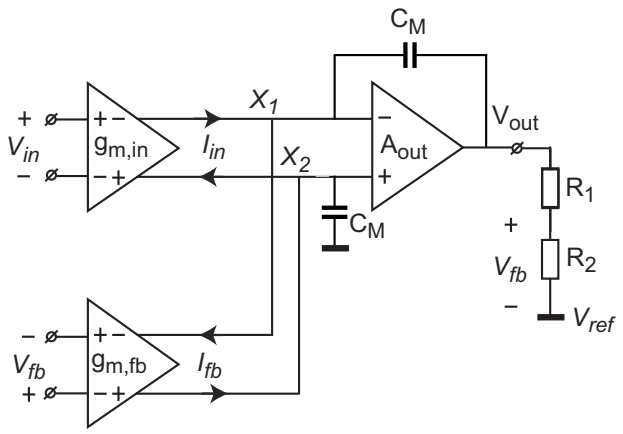

FIGURE 1.12: A typical CFIA without offset

made off chip. It is desired that the contribution of gain error from the g_m mismatch is an order less than the contribution due to the mismatch in the resistive divider. This makes the gain error of the overall amplifier dominated by the resistive mismatch rather than the g_m mismatch. In this work, unless explicitly mentioned, gain error refers to gain error due to mismatch in $g_{m,in}$ and $g_{m,fb}$.

Figure 1.13 graphically illustrates the gain error component arising from g_m mismatch. It shows the V_{in} vs I_{out} of $g_{m,in}$ and $g_{m,fb}$ (assuming $g_{m,in}$ and $g_{m,fb}$ are linear and offset free). The slope of the lines defines the value of transconductance. Ideally $g_{m,in}$ should be equal to $g_{m,fb}$, but due to mismatch they are not equal. When V_{in} is applied to $g_{m,in}$ it results in a differential current I_{in}. The output is set such that when V_{fb} is applied to $g_{m,fb}$ the net current at nodes X_1 and X_2 is zero. But as seen from the graph, due to mismatch in the g_ms this V_{fb} is not equal to V_{in}. This is the gain error component introduced by the g_m mismatch. The following sections discuss the various methods that can be used to reduce this gain error. To avoid complications in further discussions in the next sub-sections, the amplifiers are assumed to be offset free.

1.6.1 Gain trimming

As discussed in section 1.5 in the context of offset cancellation, trimming involves adjusting of on-chip components to achieve the desired performance. Gain error trimming in a CFIA can be done by trimming the transconductance of either or both $g_{m,in}$ and $g_{m,fb}$ such that they match each other. Figure 1.14 describes the system level implementation of gain trimming. An off-chip setup determines the gain error, this gain error information is then used to generate the required gain error correction information. This correction information can be used to trim the values of $g_{m,in}$ and $g_{m,fb}$. The actual

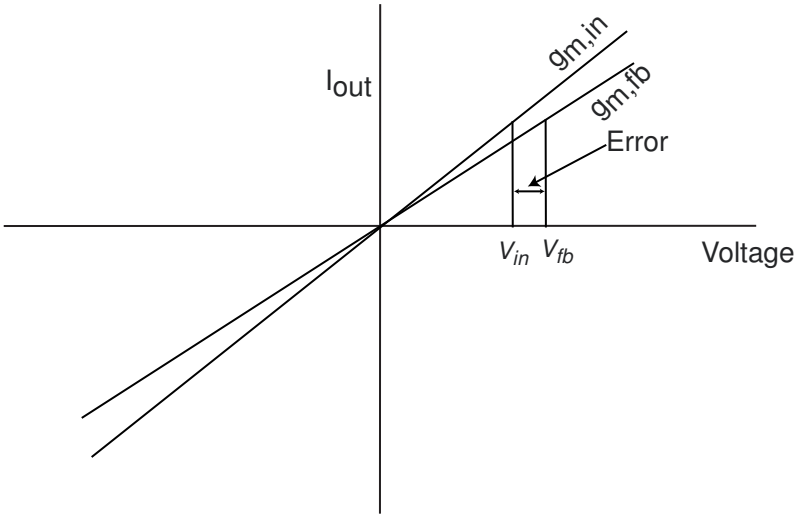

FIGURE 1.13: V_{in} vs I_{out} for $g_{m,in}$ and $g_{m,fb}$

implementation of such trimming depends on the implementation of $g_{m,in}$ and $g_{m,fb}$. It can vary from trimming resistors to trimming currents.

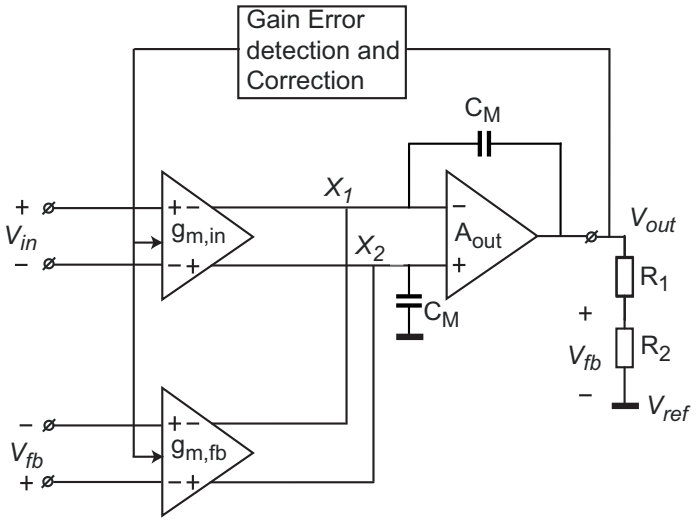

FIGURE 1.14: Gain error trimming in CFIA

As trimming is a one-time job, it cannot accommodate for any drift in gain error. Similar to the use of dynamic offset compensation techniques,dynamic techniques can also be used to minimize gain error and reduce the effect of drift.

1.6.2 Dynamic Element Matching

Dynamic Element Matching (DEM) is one of the frequently used techniques to reduce the effect of mismatch in IC components. Some of the examples where DEM is used are[10, 11]. As mentioned earlier, the gain error in CFIA is due to mismatch in components, hence DEM can be a solution to counter the effect of this mismatch. In a CFIA, DEM

can be implemented by switching the transconductors alternately between the input and feedback, as shown in Figure 1.15

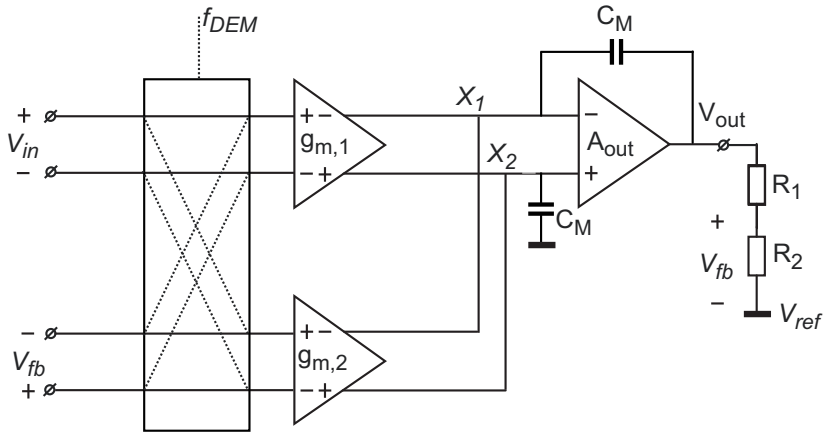

FIGURE 1.15: DEM in CFIA

If there is a mismatch of "Δ" ($g_{m,1} = g_{m,2}(1+\Delta)$) between the input and feedback transconductors, then the DC gain error over one DEM cycle can be given by.

$$|\text{Gain Error}| = 1 - \frac{1+\Delta+\frac{1}{1+\Delta}}{2} \approxeq (\Delta^2/2)(\text{for}\Delta \ll 1) \tag{1.5}$$

So the averaged DC output signal will have a gain error proportional to Δ^2. If there is mismatch of 1% between the input and feedback transconductors, then using this method we can achieve a DC gain accuracy of 0.01%. As most sensor signals are low-frequency signals, the average gain accuracy for low-frequency signals can be increased, if the DEM frequency is much higher than the signal frequency. Figure 1.16 explains the DEM action:

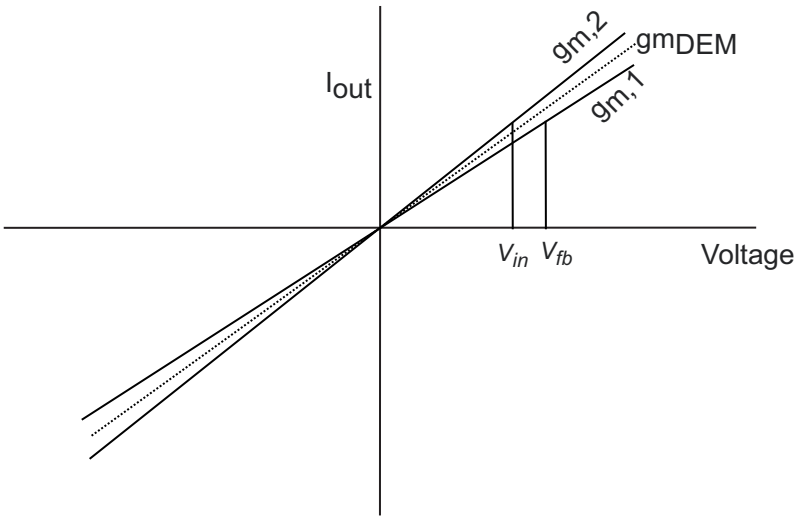

FIGURE 1.16: Explanation of DEM'ing in CFIA

As can be seen from Figure 1.16, with constant swapping of the $g_{m,1}$ and $g_{m,2}$ between input and feedback, the average g_m is equal to $g_{m,DEM}$. Hence, the effect of first-order mismatch between $g_{m,1}$ and $g_{m,2}$ can be averaged out by DEM. A significant problem associated with DEM is that it causes a ripple in the output at the DEM frequency. It is similar to the ripple caused by chopping. This ripple can cause significant errors when sampled by an ADC connected to the CFIA. Proper measures should be taken to minimize the value of this ripple.

1.6.3 Gain Error Correction

Gain Error Correction (GEC) method is similar to auto-zeroing. In this method a reference input is applied to the amplifier and the gain error is measured. Then the measured gain error is corrected by changing the value of $g_{m,in}$ and $g_{m,fb}$. Figure 1.17 shows a system-level concept for the implementation of GEC in a CFIA.

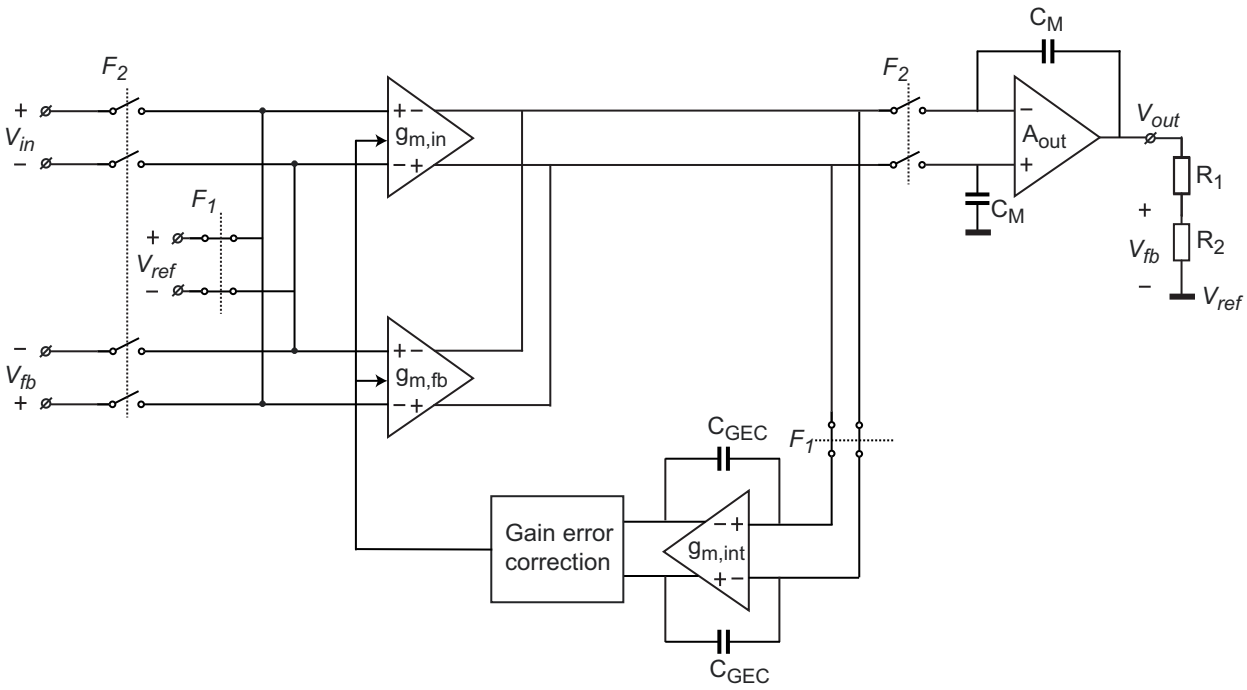

FIGURE 1.17: Gain error correction in CFIA

In phase F_1 both transconductors are given a reference input V_{ref}. Due to the mismatch in $g_{m,in}$ and $g_{m,fb}$, a differential error current will flow in nodes X_1 and X_2. This current is integrated on gain error correction capacitors C_{GEC}. The gain error correction block uses the voltage on C_{GEC} to change the value of $g_{m,in}$ or $g_{m,fb}$, until the net current flowing in nodes X_1 and X_2 is zero. In phase F_2 the signal is amplified. As the gain error correction information integrated on C_{GEC}, it holds the information during amplifying

state and "Gain error correction block" continues to control $g_{m,in}$ and $g_{m,fb}$ to an equal value.

1.7 The state-of-art in CFIA

Previously many precision CFIAs have been designed, which use dynamic offset compensation techniques discussed above to achieve a low offset and low noise performance. Table 1.1 lists the specifications of present state-of-the-art precision CFIA designs.

Parameters	Pertijs'09 [6]	Witte'08 [12]	Fan'10 [13]
Input Offset Voltage	$3\mu V$	$5\mu V$	$2\mu V$
CMRR	$140dB$	$140dB$	$137dB$
Absolute Gain Accuracy	$\pm 0.1\%$	$\pm 0.1\%$	-
Relative Gain Accuracy	-	-	$\pm 0.53\%$
Input Voltage Noise	$27nV/\sqrt{Hz}$	$142nV/\sqrt{Hz}$	$21nV/\sqrt{Hz}$
NEF [Willy Sansen]	43	143	10
GBW	$800kHz$	$1MHz$	$1MHz$
Supply Current	$1700\mu A$	$850\mu A$	$143\mu A$
Supply Voltage	$3.0V$to$5.5V$	$2.8V$to$5.5V$	$5V$

TABLE 1.1: Comparison of the state-of-the-art in precision CFIA

Using dynamic offset compensation techniques, the designs mentioned in Table 1.1 achieve a low offset, low noise and a high CMRR. The dominating source of error in these designs is gain error. The best gain error performance is achieved by [6] and [12]. These designs, however, have relatively low power efficiency. In [13] the amplifier achieves good power efficiency, but the gain error is higher as compared to other implementations. This is because; gain accuracy is determined by the extent of mismatch in $g_{m,in}$ and $g_{m,fb}$. [6, 12] uses a degenerated input stage, whereas [13] uses a non-degenarated input stage. Since resistors can be matched better as compared to transistors, [6, 12] achieves a high gain accuracy than [13]. But degeneration of input stage reduces the power efficiency of [6, 12] compared to [13].

This work targets to improve the gain accuracy performance in a precision CFIA at a high power efficiency, while maintaining the state-of-the-art offset and noise performance. The target specifications for this work are listed in the Table 1.2

Parameters	Target Specification
Offset	$< 5\mu V$
Noise	$< 27nV/\sqrt{(Hz)}$
GBW	$1MHz$
CMRR	$\geq 120dB$
Gain error	$< 0.01\%$
Temperature range	-40℃to 125℃

TABLE 1.2: Target Specifications

1.8 Overview of the thesis and main objective

This chapter gives a brief overview of precision CFIAs. We have discussed the various techniques that can be used to achieve low offset and high gain accuracy in CFIAs. The remainder of this thesis is organized as follows: Chapter 2 discusses advanced auto-zeroed instrumentation amplifiers and introduces two auto-zeroing techniques in CFIAs i.e. *Ping-Pong* (PP) and *Ping-Pong-Pang* (PPP)[4, 14]. A comparison at topology level of PP and PPP is done in chapter 2. It further motivates the choice of PPP CFIA for this work. Chapter 3 determines the system-level design considerations of the PPP CFIA. Chapter 4 discusses the transistor-level design and simulation results of the PPP CFIA. Chapter 5 presents the measurement results on a prototype chip of PPP and compares the performance of the PPP CFIA with the state of the art.

The main objective of this work is to:

1. Study the feasibility of PPP CFIA, and implement the design on silicon.

2. Use DEM to achieve a high gain accuracy in CFIA

3. To improve the power efficiency of auto-zeroed CFIA.

Chapter 2

Advanced Auto-Zeroing Techniques in CFIA

The previous chapter discussed the use of dynamic offset compensation techniques to implement precision Current Feedback Instrumentation Amplifiers (CFIAs) in CMOS technology. Depending on the type of offset compensation technique used, these CFIA can be broadly divided into chopped [12, 13, 15] and auto-zeroed amplifiers [5]. [5] discusses the advantages associated with auto-zeroed CFIA when compared to chopped CFIAs.

This chapter describes advances in auto-zeroed CFIA. Section 2.1 briefly discusses Ping-Pong (PP) auto-zeroed CFIA. In Section 2.2, an alternative approach to auto-zeroing in CFIA, i.e Ping-Pong-Pang (PPP) auto-zeroing[4], is discussed. Section 2.3 compares the two auto-zeroing approaches. Section 2.4 summarizes this chapter with the conclusions drawn form discussions in section 2.3.

2.1 Ping-Pong auto-zeroed CFIA

This section briefly discusses PP auto-zeroed CFIAs. To achieve a continuous output with an auto-zeroed amplifier, the ping-pong approach [Yu and Geiger JSSC 1994] can be used. In this method, two identical input stages are used. While one of the stages is amplifying, the other is auto-zeroed and vice-versa. Figure 2.1 shows an implementation of PP in a CFIA [5]. It consists of two pairs of input and feedback transconductors, i.e the input stage 1 and input stage 2. When one of the input-feedback pairs is being auto-zeroed, the other pair is amplifying.

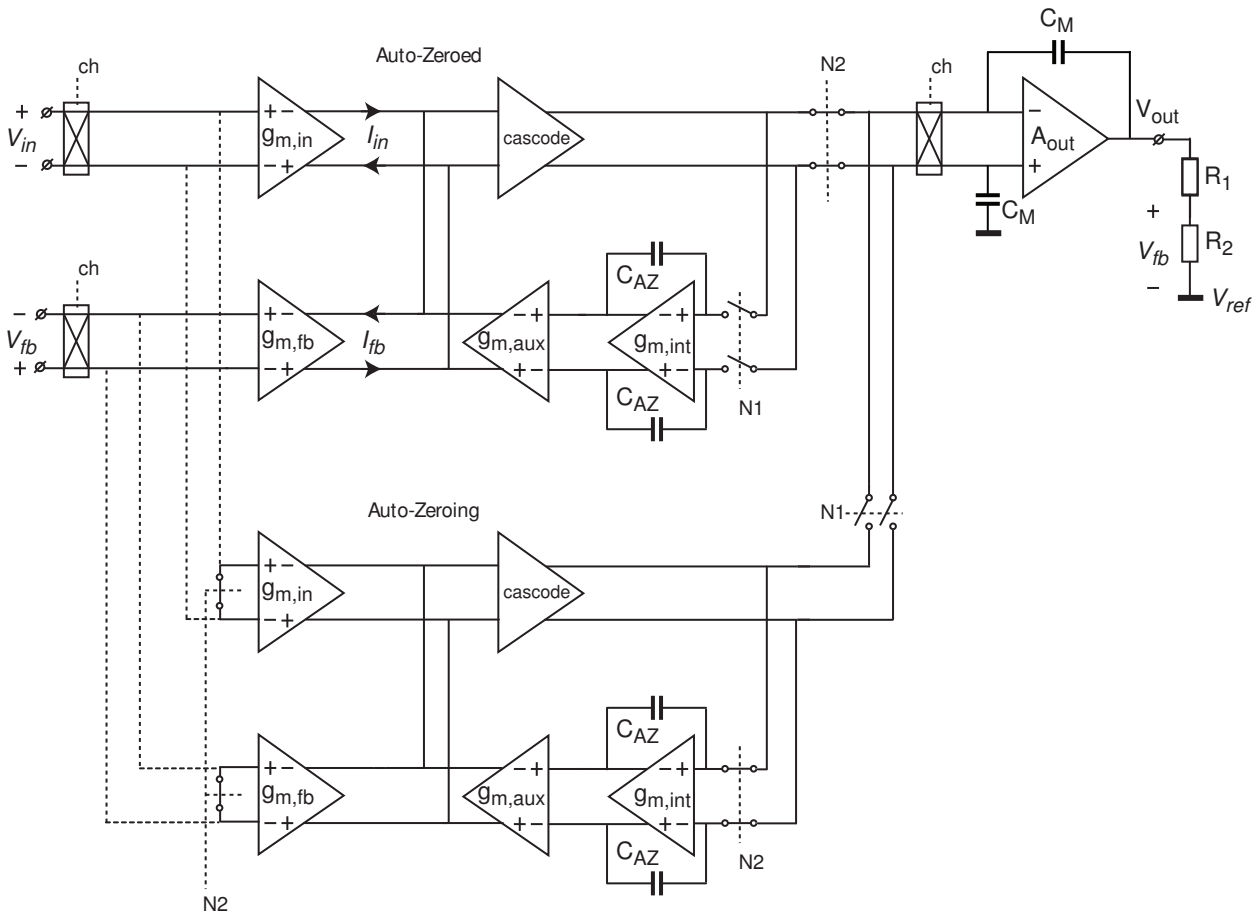

FIGURE 2.1: Ping-Pong Instrumentation Amplifier[MP ISSCC2009]

Each input stage consists of an input and feedback transconductor with a cascode stage and an associated offset nulling circuitry, which measures and cancels the offset at the summing node of the input and feedback differential currents. There are switches that switch the amplifiers from auto-zeroing to amplifying, and vice-versa.

2.2 Ping-Pong-Pang auto-zeroed CFIA

The idea behind the PPP auto-zeroing technique is to achieve a continuous-time output with only three input transconductors, instead of the four used by the PP topology. The basic idea was discussed in [4, 14]. This thesis presents the first silicon implementation of this technique.

Figure 2.2 shows the system diagram of a PPP auto-zeroed CFIA. It consists of three input G_m stages. Each G_m stage consists of a transconductor (gm), a cascode stage and an assocuated offset nulling circuitry. The details of each G_m stage which is shown in the inset of Figure 2.2 . The idea behind using three G_m stages is that each of them

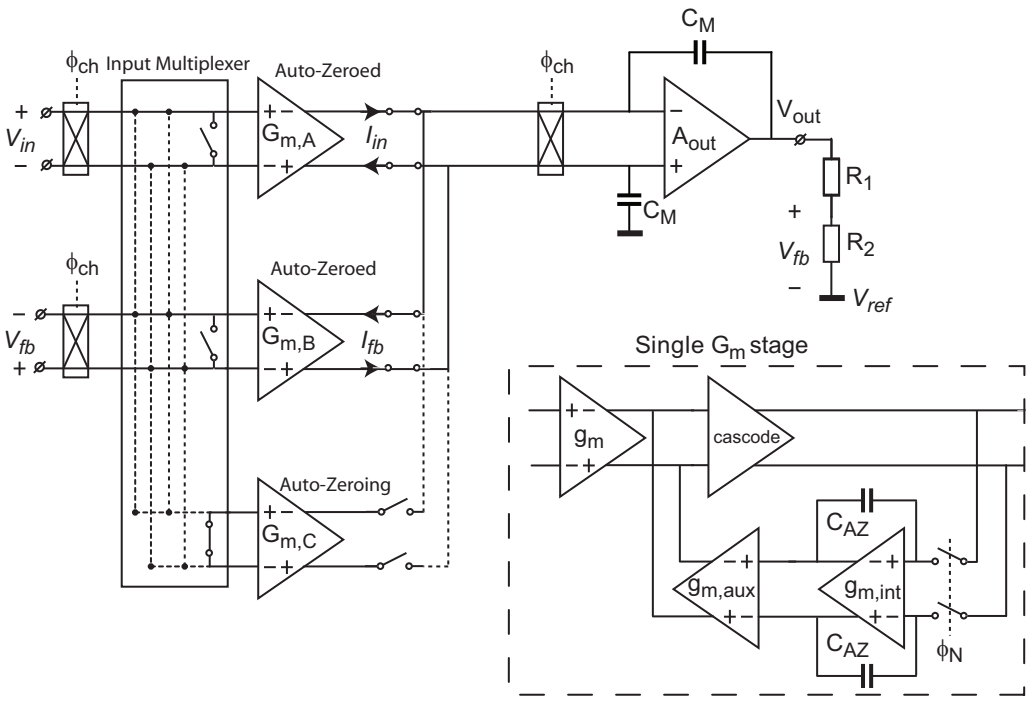

FIGURE 2.2: PPP IA block diagram

will switch to input, feedback and auto-zeroing state. When one of the input stages is auto-zeroed, the other two are available for amplifying. In the Figure 2.2, $G_{m,A}$ and $G_{m,B}$ are amplifying, and $G_{m,C}$ is being auto-zeroed. Using this scheme, it is possible to get a continuous-time signal with only three G_m stages.

The switching of input stages between different states can be implemented in various ways. These possibilities are discussed in Chapter 3. By carefully choosing the switching sequence, the input gm's can be DEM'ed. As discussed in chapter 1, DEM'ing of the input gm stages is a possible solution to increase the DC gain accuracy of CFIA.

2.3 Comparison between Ping-Pong and Ping-Pong-Pang auto-zeroing

In this section, PP and PPP auto-zeroed CFIAs are compared at the topology level

1. The PPP topology can be considered as an advancement of the PP topology. One of the significant improvements of PPP over PP is that it uses three input stages instead of four. These input stages dominate the noise performance, and for precision applications a low noise floor is required. This increases the power required per input stage. Reducing the number of input stages from four to three, impacts in a substantial reduction in terms of power consumption for PPP topology.

2. One of the advantages of PP topology is that the transconductors are used as pairs of input-feedback. Using input tarnsconductors in pairs has two significant topology level implications. First, during the auto-zeroing operation the offset of the input stage along with the offset of the cascode stage is cancelled. Secondly, since the differential input and feedback current summing node is right after the input/feedback transconductors, hence the cascode in Figure 2.1 carries only the error current. The magnitude of this error current is usually very small due to the high overall feedback factor; hence the biasing current required in the cascode stage is small.

   Comparatively, in a PPP CFIA, the input transconductors do not work in pairs. This rather complicates the implementation of summing node (where input and feedback differential currents cancel).

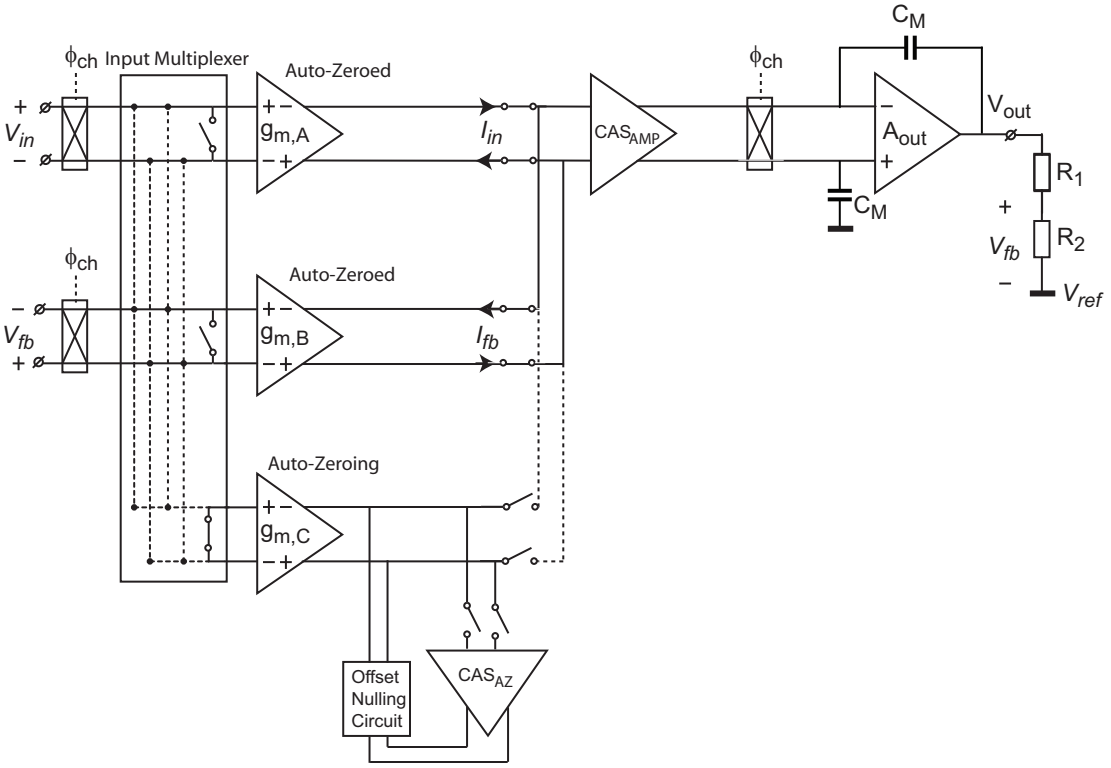

FIGURE 2.3: PPP IA block diagram with summing node after input transconductor g_m

Lets, consider a case shown in Figure 2.3 , if the summing node is to be implemented just after input transconductor. This requires two cascode blocks, one of which is used for auto-zero path (CAS_{AZ}) and other is used for amplifying path (CAS_{AMP}). Hence during auto-zeroing, transconductor is auto-zeroed along with the CAS_{AZ} block. If CAS_{AZ} is offset free then the information during auto-zeroing is purely the offset information of input stage. During amplifying the differential current from input and feedback transconductor (auto-zeroed) are cancelled and

the error current is passed to CAS_{AMP}. If CAS_{AMP} is offset free the input referred offset will be zero in this case. This implementation mandates the need of offset free cascodes CAS_{AMP} and CAS_{AZ}. This in turn needs techniques discussed in section 1.5 for the cascode blocks individually.

Another way to implement the same topology would be to move the current summing node and use an individual cascode for each stage (as shown in Figure 2.2). In this implementation each input stage (g_m) would now consist of a transconductor along with its own cascode. The summing node will now be the output of the cascode block. This implementation eliminates the need to separately compensate the offset of cascodes. Compared to PP this implementation would require an extra cascode. Another marked disadvantage in terms of power is that the cascode blocks now carry the full signal current, hence needs to be biased at higher current

3. Compared to a PP CFIA, a PPP CFIA requires extra circuitry for offset cancellation and also an extra cascode stage. Hence, the power consumed by the offset-nulling circuitry of a PPP CFIA is higher than that of a PP CFIA.

The above points mention advantages and disadvantages of PP and PPP CFIAs when compared to each other. To quantify the above observations, let us compare the implementation of a PP and a PPP CFIA in terms of the power consumption of individual building blocks.

From Figure 2.1, the building blocks of a PP CFIA consist of input transconductors (4), cascode stages (2) and auto-zeroloops (2). Assuming a current of I_{tail} in each of the input transconductors, $I_{cascode1}$ in each cascode stage and I_{az} in each auto-zero loop. The total current consumption in the input stage will be

$$I_{total} = 4 \times I_{tail} + 2 \times I_{cascode1} + 2 \times I_{az} \tag{2.1}$$

From Figure 2.2, the building blocks of the input stage of a PPP CFIA consist of input transconductors (3), cascode stages (3) and auto-zeroing loops (3). The currents for input stage and auto zero loops are assumed to be the same as in PP CFIA implementation. Let the current in cascode block be $I_{cascode2}$. $I_{cascode2} \geq I_{cascode2}$ as cascode of a PPP CFIA carries the full signal current. The total current in the input stage of PPP will be

$$I_{total} = 3 \times I_{tail} + 3 \times I_{cascode2} + 3 \times I_{az} \tag{2.2}$$

In a well designed low noise amplifier, I_{tail} is a substantial part of overall current consumption. Hence saving one I_{tail} in PPP is a substantial power reduction.

The implementation of the auto-zeroing loops determines the level of impact that I_{az} has on the power consumption comparison. If $I_{az} \ll I_{tail}$, then the extra I_{az} does not contribute significantly to an increase in power consumption in a PPP CFIA. However if I_{az} is comparable to I_{tail}, the advantage of one less transconductor in a PPP CFIA is nullified.

As $I_{cascode2} \geq I_{cascode1}$, the power saved by the elimination of one input transconductor in a PPP CFIA compared to a PP CFIA is substantially reduced, since a PPP CFIA uses one extra cascode stage. As $I_{cascode}$ is determined by differential input voltage range, it is this range that determines whether a PPP CFIA or a PP CFIA is more power efficient.

If the input differential range is small, the differential current in $I_{cascode}$ can be relatively small as well. In such a case, the overall power consumption for a PPP CFIA will be less than that of a PP CFIA.

Apart from topology level, the implementation of input transconductors also determine the overall power consumption. Hence much effort needs to be put into designing of the input transconductors for low power. In chapter 4 input stage implementation is discussed thoroughly.

2.4 Conclusion

This chapter compares the PP and PPP auto-zeroing in CFIA at a topology level. Depending on the input signal specifications, either of the auto-zeroing has their advantages and disadvantages. For small input differential signals, PPP CFIA will have lower power consumption. As the targeted input differential swing is 50mV; hence the PPP CFIA topology is more suitable for this work. The following chapters discusses the implementation details of a PPP auto-zeroed CFIA and the measurement results on a prototype chip.

Chapter 3

System-Level Design of Ping-Pong-Pang CFIA

In the previous chapter, the ping-pong-pang (PPP) instrumentation amplifier was introduced. This chapter discusses its system-level implementation. Section 3.1 describes the overall topology of PPP. The rest of the chapter describes the PPP IA system in detail and is organized as follows. Section 3.2 discusses the PPP switching sequence which enables the auto-zeroing and Dynamic Element Matching (DEM) of the amplifier's input transconductors. Section 3.3 discusses the noise folding due to auto-zeroing and how chopping can be used to move this folded noise away from DC. Section 3.4 explains the ripple associated with dynamic element matching of the input transconductors, and the techniques used to reduce this ripple. Switching transisents associated with the PPP switching sequence is discussed in Section 3.5. Section 3.6 derives the open-loop gain needed to achieve required gain accuracy. It discusses how this gain is achieved using three stages and the relevant frequency compensation technique used to make the design stable. In Section 3.7, the sources of residual offset are discussed and the specifications of various blocks are derived, such that the offset specification in table 1.2 can be achieved.

3.1 Ping-Pong-Pang overall topology

Figure 3.1 shows the system-level block diagram of the PPP IA. It consists of three identical auto-zeroed transconductors ($G_{m,A}$, $G_{m,B}$ and $G_{m,C}$), an output stage A_{out} and a resistive feedback network implemented using R_1 and R_2. The inset shows the detail of a single G_m stage. It consists of an input transconductor, a cascode stage and offset nulling circuitry. The auto-zeroed transconductors are cyclically switched between three states:

- the input state, in which they convert V_{in} to a current I_{in};
- the feedback state, in which they convert V_{fb} to a current I_{fb};
- the auto-zeroing state, in which their offset is auto-zeroed;

The details of the associated switching sequence will be discussed in Section 3.2. For now, $G_{m,A}$, $G_{m,B}$ and $G_{m,C}$ are assumed to be in the input state, the feedback state and the auto-zeroing state, respectively. The third transconductor $G_{m,C}$ is then being auto-zeroed, while the two previously auto-zeroed transconductors ($G_{m,A}$ and $G_{m,B}$) comprise the signal path, along with the output stage and the feedback network.

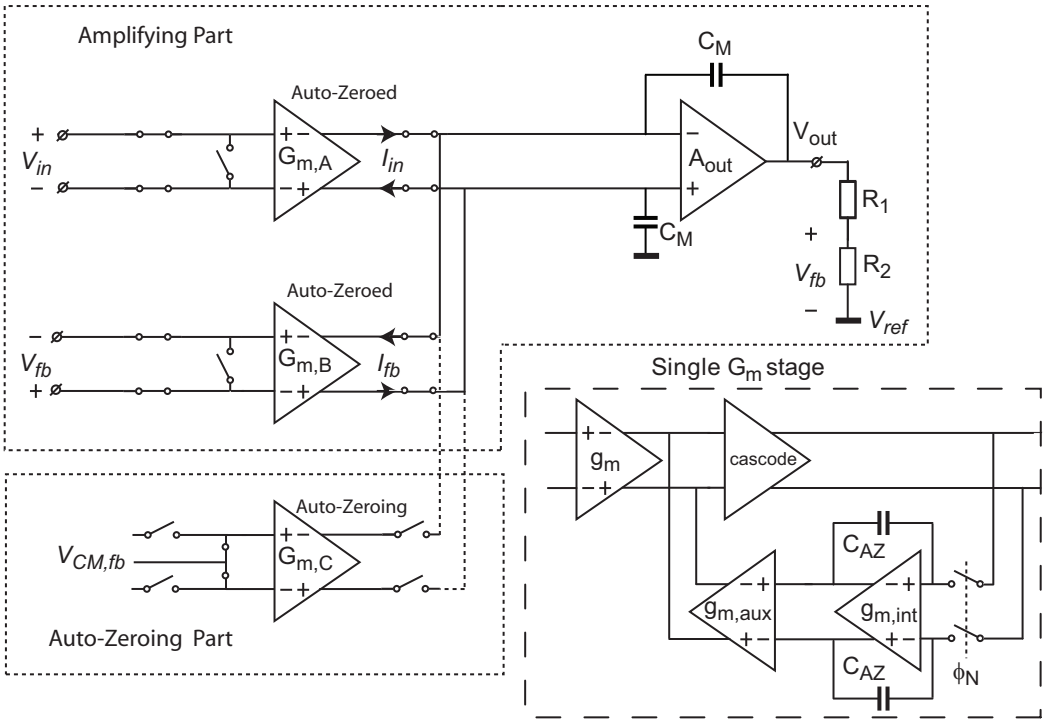

FIGURE 3.1: Ping-Pong-Pang Amplifier Topology

Figure 3.2 shows the signal path in detail. The input voltage V_{in} and feedback voltage V_{fb} when applied to $G_{m,A}$, and $G_{m,B}$ respectively, result in differential currents I_{in} and I_{fb}. These currents are summed at the nodes X_1 and X_2. V_{fb} is an attenuated version of V_{out}, and is generated by the feedback network. The amplifier A_{out} maintains V_{out} such that the differential current resulting from the sum of I_{in} and I_{fb} is zero at steady state. The $CMFB_{AMP}$ block ensures the output CM level of $G_{m,A}$ and $G_{m,B}$ are same. Hence, the current I_{in} and I_{fb} are summed at the same CM level. To implement this control, the $CMFB_{AMP}$ block detects the CM level of the nodes X_1 and X_2, and regulates the cascodes of $G_{m,A}$ and $G_{m,B}$ to maintain their output CM level.

Figure 3.3 shows the details of $G_{m,C}$ while its being auto-zeroed. Its inputs are shorted, resulting in a differential offset current, at the output of the cascode C, due to the offset of g_m and cascode C. This is integrated on the auto-zeroing capacitors (C_{AZ}) until cancelled by the differential current generated by $g_{m,aux}$. The required voltage is stored

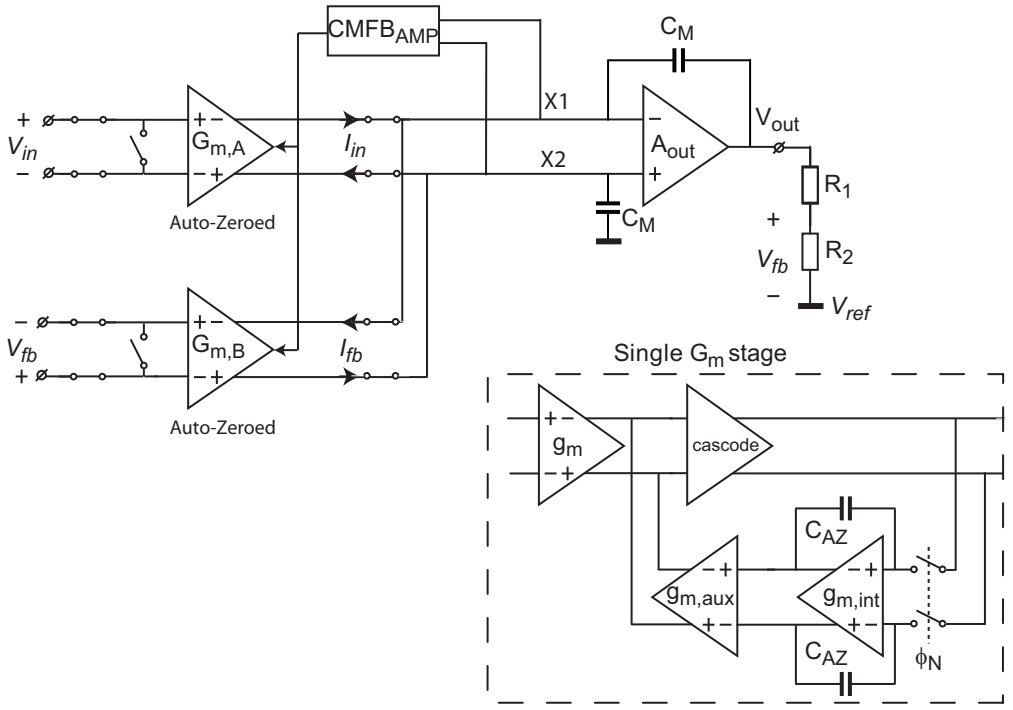

FIGURE 3.2: Signal path of the PPP amplifier

on the auto-zero capacitors C_{AZ}. During the auto-zeroing state, the output CM level of the cascode is regulated by the $CMFB_{AZ}$ block.

During auto-zeroing, the inputs of the $G_{m,C}$ will be shorted to a CM level. However, there are two possible CM levels: the one applied to the input transconductor $V_{CM,in}$ and the one applied to the feedback transconductor $V_{CM,fb}$. To avoid auto-zeroing errors due to any dependency of the offset on the CM level, the CM level used during auto-zeroing should be the same as the CM level ($V_{CM,in}$ or $V_{CM,fb}$) to which the transconductor will be switched during the subsequent input or feedback state. This scheme also prevents excessive CM transients from occurring when the transconductor is switched from the auto-zeroing state to the input/feedback state. This is because its input capacitors have already settled at the CM level to which they will be switched. To implement this scheme, two CM level detector blocks are used to determine $V_{CM,in}$ and $V_{CM,fb}$.

3.2 PPP switching sequence, DEM'ing and Auto-Zeroing

The switching sequence determines the order in which the three auto-zeroed transconductors are switched between the input, feedback and auto-zeroing states. At any moment, one of them is being auto-zeroed. The frequency at which every G_m is switched to the auto-zeroing state is called the auto-zeroing frequency (f_{az}) . To maintain the same auto-zeroing frequency for every G_m stage, the auto-zeroing state for a particular

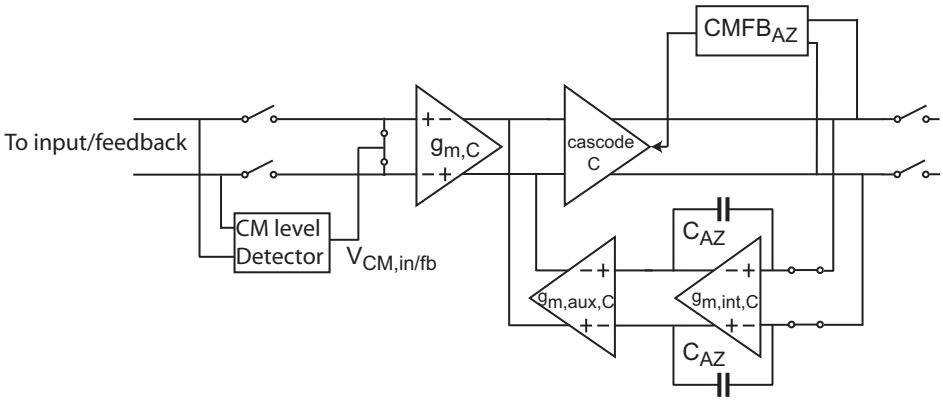

FIGURE 3.3: Transconductor in the auto-zeroing state

transconductor has to be repeated every three cycles. With this constraint in mind, tables 3.1 and 3.2 illustrate two possible switching sequences.

State/Step	1	2	3	1	2	3	1
Input	A	C	B	A	C	B	A
Feedback	B	A	C	B	A	C	B
Auto-Zero	C	B	A	C	B	A	C

TABLE 3.1: Switching Sequence 1 [14]

Switching sequence 1 is a simple cyclic rotation of the three G_m stages between input, feedback and auto-zeroing states. For every G_m, the auto-zeroing state is followed by two different states i.e. the input and feedback states. This sequence however, does not allow for the G_m stages to be auto-zeroed at the same CM level at which they are used. The sequence illustrated in Table 3.2 can counter this disadvantage.

State/Phase	1	2	3	4	5	6	1
Input	A	A	B	B	C	C	A
Feedback	B	C	C	A	A	B	B
Auto-Zero	C	B	A	C	B	A	C

TABLE 3.2: Switching Sequence 2[4]

In this switching sequence, every auto-zeroing state is followed by one amplifying state. This ensures that the G_m's are auto-zeroed and used at the same CM level. Due to this advantage, switching sequence 2 was used in this work.

Switching sequence 2 also has the advantage that it inherently DEMs the input transconductors of every G_m stage, which should improve the amplifier's DC gain accuracy (section 1.6.2). To explain this further, let us consider the gain during steps 1 and 4 of the switching sequence. It is proportional to $g_{m,A}/g_{m,B}$ and $g_{m,B}/g_{m,A}$ in steps 1 and 4 respectively. The gains during steps 2 and 5 and steps 3 and 6 have a similar reciprocal relationship. If there is a mismatch $\Delta(< 1)$ between $g_{m,A}$, $g_{m,B}$ and $g_{m,C}$, the average

gain error over the six switching steps is improved to Δ^2. However, this improvement in the DC gain accuracy is achieved at the expense of AC ripple in the output signal. This ripple occurs at the DEM frequency, and its amplitude is proportional to the initial mismatch (Δ) of the input stages.

Since the switching sequence repeats itself after every 6 steps, the DEM frequency is given by $f_{DEM}= f_{ppp}/6$, where each step corresponds to a PPP cycle and f_{ppp} is the corresponding PPP frequency. The auto-zeroing cycle for every G_m stage consists of the auto-zeroing state for one step and input/feedback state for two steps (in total three steps i.e. three PPP cycle). Hence, the auto-zeroing frequency is given by $f_{az}=f_{ppp}/3$. Or in other words, the auto-zero duty cycle is 1:2 or 33.33%. Previous implementations of auto-zeroed amplifiers [5, 7] have used 50% duty cycles. The effects of auto-zeroing with a 50% duty-cycle (1:1 auto-zeroing), or with a 33.33% duty-cycle (1:2 auto-zeroing) are discussed in the next section.

3.3 Noise Folding due to auto-zeroing and the optimum chopping frequency

Auto-zeroing has the disadvantage that under-sampled wide-band noise is folded to DC and low frequencies [8]. However, chopping can then be used to modulate the folded noise to high frequencies and move the thermal noise floor back to DC and low frequencies [5, 7]. To achieve this, the chopping must be optimized. In [7] the choice of this optimal chopping frequency, for a 1:1 auto-zeroed amplifier, is discussed. However, in this implementation 1:2 auto-zeroing is used, and so the optimal chopping frequency will be different.

To evaluate the optimal chopping frequency, a through analysis of noise folding with 1:2 auto-zeroing is required. Figure 3.4 shows an ideal circuit [8] which can be used to analyze the effect of noise folding in auto-zeroed amplifiers. This above circuit was simulated using the Periodic Steady State (PSS) noise analysis tool in Cadence. The auto-zeroing frequency in this case was 6.66 kHz. The overall bandwidth of the system was $\gg$ 6.66kHz. Figure 3.5 shows the effect of noise folding at 33.33% and 50% duty cycles.

From Figure 3.5, two duty-cycle dependent characteristics of auto-zeroing can be observed: the amount of noise folding at low frequencies and the location of the first notch in the frequency spectrum. For a 33.33% duty cycle, the noise at lower frequencies is higher than for a 50% duty cycle. In time domain, noise folding can be explained as follows: noise folding occurs because loss of correlation between the signal value at the

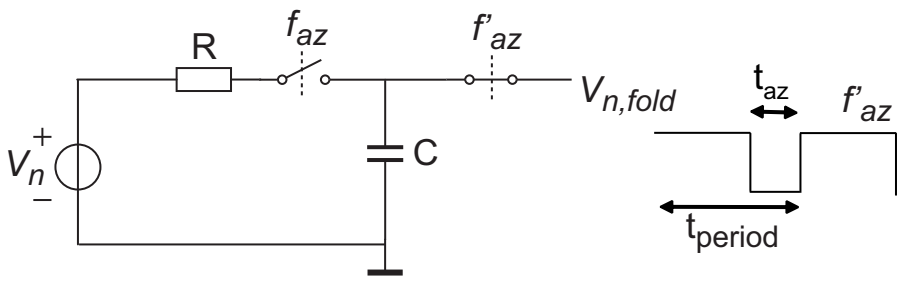

FIGURE 3.4: Circuit used to see the effect of noise folding with different auto-zeroing duty cycle

end of hold time and the actual signal value. As the hold time increases this correlation becomes more dominant for even lower frequency range. It leads to a higher noise folding. As 33.33% duty cycle has a higher hold time, the effect of noise folding is more as compared to 50% duty cycle auto-zeroing.

For 1:2 auto-zeroing the first notch in the frequency spectrum is at a lower frequency than that of 1:1 auto-zeroing. The position of the notch is determined by the length of the "hold" state. The hold action acts as a low-pass filter on the folded noise. Since the hold time with a 33.33% duty-cycle is longer than with a 50% duty-cycle, the notch associated with a 33.33% duty-cycle will be at a lower frequency.

The position of the first notch is important in auto-zeroed amplifiers, as chopping at the notch frequency will shift the notch to DC, and lead to a thermal noise floor at DC. For a 1:1 auto-zeroed amplifier [7], a chopping frequency of $2 \cdot f_{az}$ (as seen from Figure 3.5, the notch is at $2 \cdot f_{az} = 13.32kHz$) is optimal. In the case of a 1:2 auto-zeroed amplifier, the optimal chopping frequency is at $1.5 \cdot f_{az} = 10kHz$, because this is the frequency of the first notch. As the auto-zeroing frequency in a PPP amplifier is given by $f_{ppp}/3$, the ideal chopping frequency is $f_{ppp}/2$.

3.4 DEM ripple

As discussed in section 3.2, DEM'ing causes output ripple, whose amplitude is proportional to the initial mismatch of the input transconductors. For a typical mismatch of 0.5%, a gain of 100 and an input differential voltage of $50mV$, the amplitude of the DEM ripple will be $50mV$ at the output. This is quite significant, and might lead to large sampling errors when such an amplifier is interfaced to an ADC. However, this effect is dominant for systems with broadband applications. For low frequency applications, the effect of DEM ripple can be removed by synchronizing the ADC sampling frequency to the DEM frequency. In this implementation, techniques at amplifier level have been

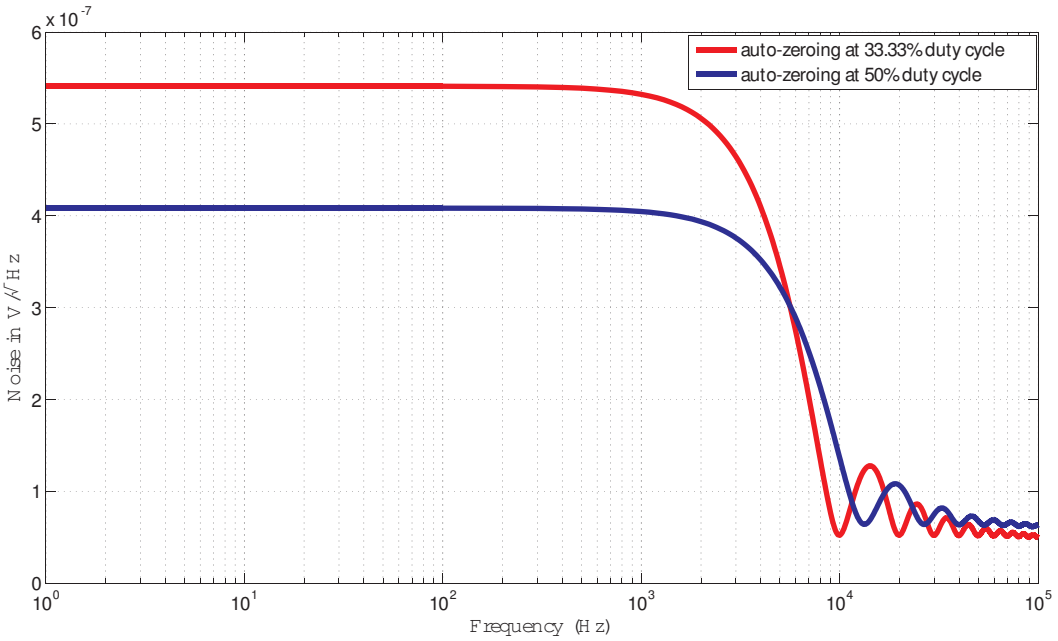

FIGURE 3.5: PSS analysis of noise folding due to different duty cycle auto-zeroing

used to reduce the ripple. This can be done in two ways: by switching at high frequencies, such that the DEM ripple is filtered by the amplifier's transfer, or by trimming the input stages to reduce their mismatch.

Figure 3.6 shows the input to output transfer of an amplifier with a GBW of 1MHz at a gain of 100.

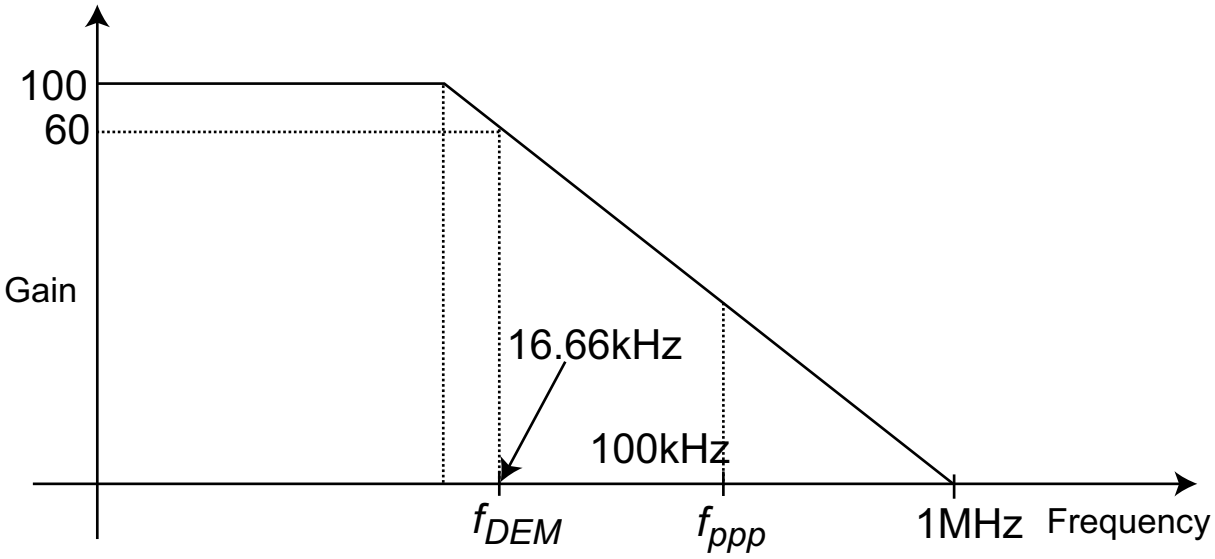

FIGURE 3.6: Effect of high f_{ppp} on DEM ripple

For a f_{ppp} = 100kHz, f_{DEM} = 16.66kHz, and so the DEM ripple would only be attenuated by a factor of 100/60 = 1.66. The higher f_{DEM} is, the greater will be the

attenuation. However, switching at higher frequencies causes the amplifier's offset performance to deteriorate (detailed discussion in Section 3.7).

Another way to reduce the DEM ripple would be to use the ripple information at the output nodes, to trim the value of input transconductors. This is similar to the method discussed in section 1.6.1. An implementation of this approach is discussed in chapter 4.

3.5 Techniques to reduce switching transients

Implementing the switching sequence using non-ideal elements (clocks, switches and transconductors) can lead to switching transients at the output. To prevent such transients from reaching the output, various techniques are used. [6] describes a ping-pong switching scheme which uses dead-banding and settling phases to minimize the effect of switching transients. In this work, a similar approach is used. This section describes the implementation of the switching sequence proposed in Section 3.2.

Before discussing the techniques used to reduce the switching transients, the clock phases which implement the switching for a single G_m stage are introduced. Stages $G_{m,A}$, $G_{m,B}$ and $G_{m,C}$ in Figure 3.1 are essentially the same, hence, every stage is driven by a similar set of clocks. The G_m stages are switched to different states, using an array of switches at their input and output terminals which are controlled using different clock phases.

Figure 3.7 shows the switch network at the output of a G_m stage and the respective clock phases which control them are shown in Figure 3.8. During the amplifying phase (ϕ_{AMP}), the G_m stage is connected to the summing nodes X_1 and X_2. During phase $\phi_{CMFB,AMP}$, the outputs of the $CMFB_{AMP}$ are connected to the cascode of the G_m stage. The $CMFB_{AMP}$ block then senses the CM level of nodes X_1 and X_2 and regulates the CM level of the cascode.

The amplifying phase is followed by an auto-zeroing phase ϕ_{AZ}. At the start of this phase,the output of the G_m stage is shorted by $\phi_{D,AZ}$. This allows any output transients associated with the signal currents to settle,. This prevents any signal-dependent information (which can lead to gain errors) from being integrated during the auto-zeroing phase. $\phi_{D,AZ}$ is followed by ϕ_N, which connects the output nodes of the cascode to the offset-nulling loop. The $CMFB_{AZ}$ block measures the CM level at the output nodes of cascode and regulates the cascode to maintain its CM level.

Figure 3.9 shows the switch network at the input of each G_m stage. The corresponding timing diagram of the clock phases controlling these switches is shown in Figure 3.10.

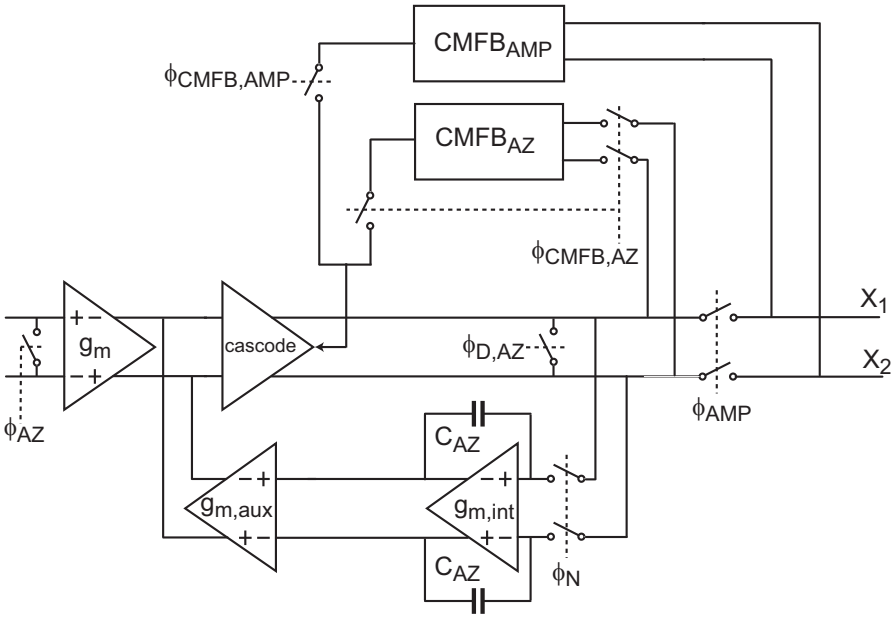

FIGURE 3.7: Switch network at the output of a single G_m stage

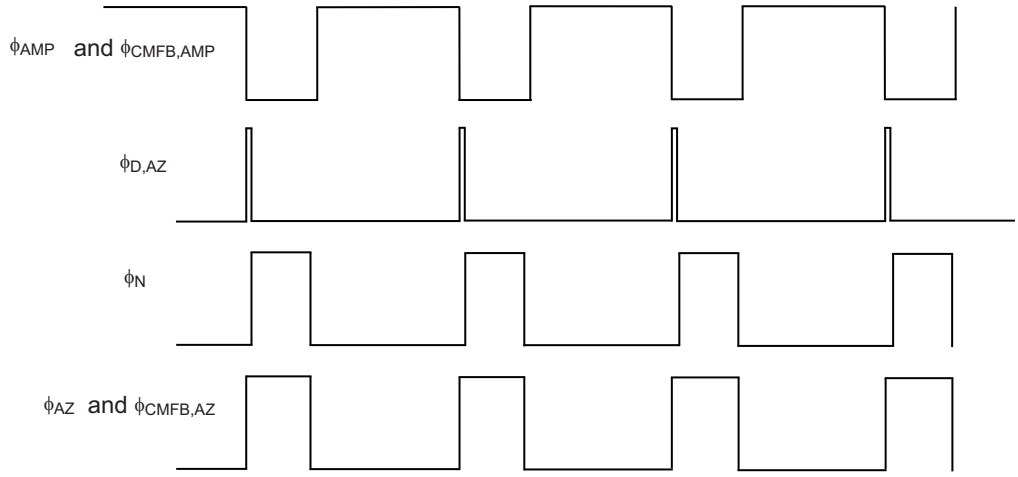

FIGURE 3.8: Timing for the clock phases in Figure 3.7

As seen from the figure, the clock phases switch the G_m stage to three different states. The clock phases $\phi_{AMP,in}$ and $\phi_{AMP,fb}$ put the G_m stage to input and feedback state respectively. Whereas $\phi_{AZ,in}$ and $\phi_{AZ,fb}$ put the G_m stage to auto-zero state with auto-zeroing at $V_{CM,in}$ and $V_{CM,ref}$ CM level respectively.

The above discussion gives an overview of the switches and the respective clock phases which switch a single G_m stage to the different states mentioned in table 3.2. The continuous switching of every G_m stage using the above discussed clock phases generates the switching sequence shown in Table 3.2. Further this section discusses effect on the output voltage due to non-idealities in the clocks phases. It also explains the measures taken reduce the effect on output voltage due to non-idealities.

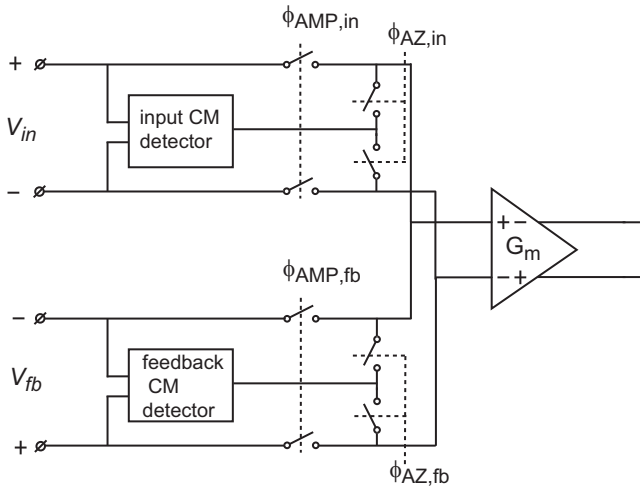

FIGURE 3.9: Switch network at the input of a single G_m stage

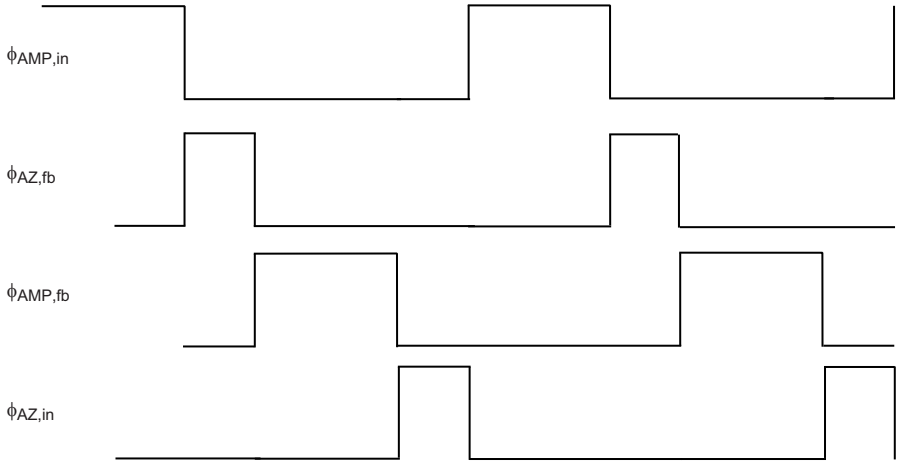

FIGURE 3.10: Timing for the clock phases in Figure 3.9

To explain this, let's consider Figure 3.11. It shows the PPP IA when $G_{m,A}$ is connected to the input, $G_{m,B}$ is connected to the feedback, and $G_{m,C}$ is being auto-zeroed. In the next state $G_{m,C}$ will be swapped with $G_{m,B}$, so $G_{m,C}$ is being auto-zeroed at the feedback CM level.

When the G_m stages are swapped, any overlap (underlap) of the their clock signals driving the output switches means that an extra (less) transconductor will be briefly present in the signal path. In turn, this will cause a brief current pulse and give rise to a signal-dependent output ripple. Figure 3.12 shows an ideal clock required to prevent such spikes. Due to process variations, in IC technology, it is difficult to implement such precise clocking scheme.

Hence, to prevent such ripples reaching the output, a dead banding approach is used. During the switching instance, the phase ϕ_O briefly disconnects the output stage, thus blocking such current pulses form reaching the output. At the same time, the summing

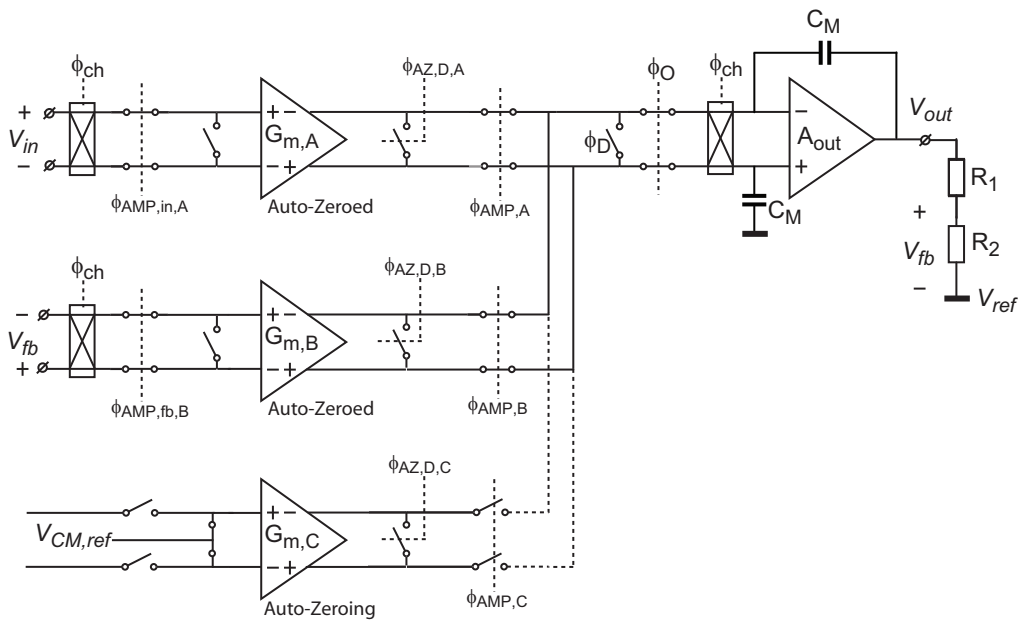

FIGURE 3.11: Switching phase with $G_{m,A}$ and $G_{m,B}$ in signal path and $G_{m,C}$ in auto-zero state, along with the respective switches

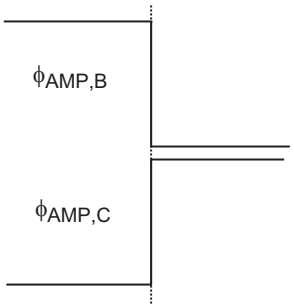

FIGURE 3.12: Ideal switching clocks during swapping of stages

node is shorted by phase ϕ_D. Hence, the current pulses are absorbed by switch ϕ_D. The time for which ϕ_O is off (ϕ_D is on), is very short as compared to the time it is on. Hence, this dead banding approach does not have significant effect on the normal operation of the amplifier. During this dead time, V_{out} is held by the miller capacitors CM, such that the amplifier's output voltage is not significantly affected. Figure 3.13 shows the circuit at this particular switching moment.

Figure 3.14 shows the timing diagram of the clock phases driving the relevant switching stages ($G_{m,B}$ and $G_{m,C}$). During the switching instance (highlighted), the clock phases $\phi_{AMP,fb,B}$ and $\phi_{AMP,B}$ disconnect $G_{m,B}$ from the feedback stage and the clock phases $\phi_{AMP,fb,C}$ and $\phi_{AMP,C}$ connect $G_{m,C}$ to the feedback path. As discussed earlier, every switching instant is marked by the phases ϕ_O and ϕ_D which prevent switching transients due to overlap in $\phi_{AMP,B}$ and $\phi_{AMP,C}$ from reaching the output. As discussed in section 3.3 , the optimal chopping frequency is $f_{ppp}/2$, it implies that the chopper clock should

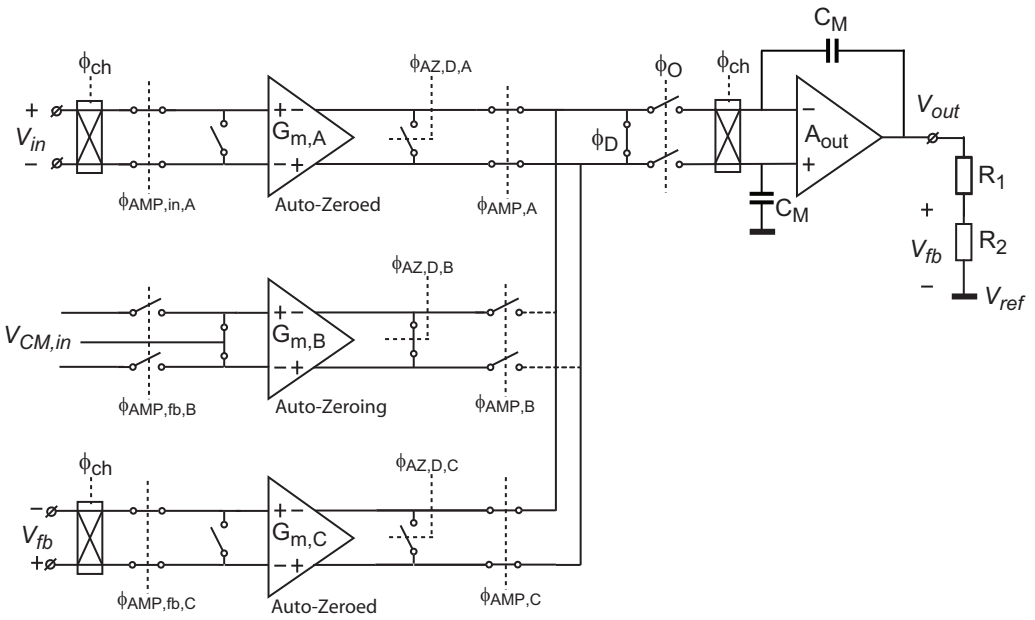

FIGURE 3.13: Circuit details between switching states along with the switches which assist transition between states

be switched every PPP cycle. The chopper clock ϕ_{ch} is also switched during the dead-band phase ϕ_D. This prevents transients associated with chopping from reaching the output.

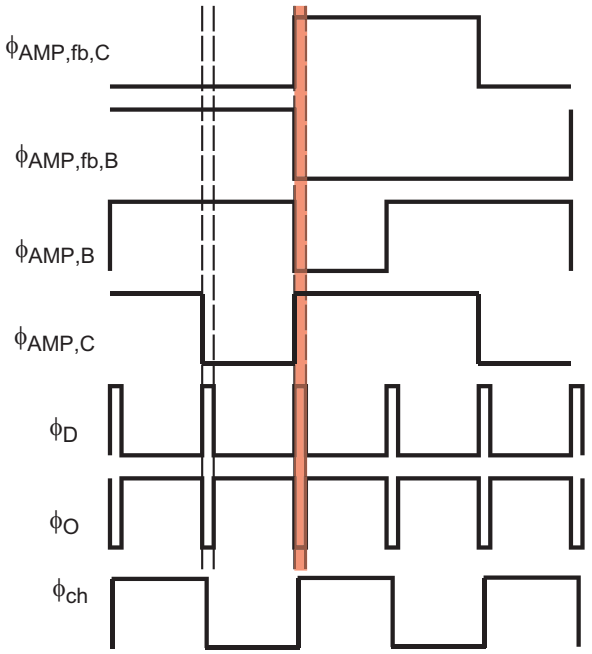

FIGURE 3.14: Timing diagram for clock phases which assist changing states

When the feedback signal is connected to $G_{m,C}$, the differential current at its output ($I_{diff,C}$) should cancel the differential current at the output $G_{m,A}$ ($I_{diff,A}$) . But due to finite bandwidth of the G_m stages, $I_{diff,C}$ will take some time to settle.Figure 3.15

shows $I_{diff,A}$ and $I_{diff,C}$ when $G_{m,C}$ is switched to feedback path. The settling phase ϕ_D allows the current $I_{diff,C}$ to settle to its correct value before the feedback loop is connected again. This prevents voltage spike at output resulting from a non-zero differential current at the summing node, arising from finite bandwidth of G_m stages.

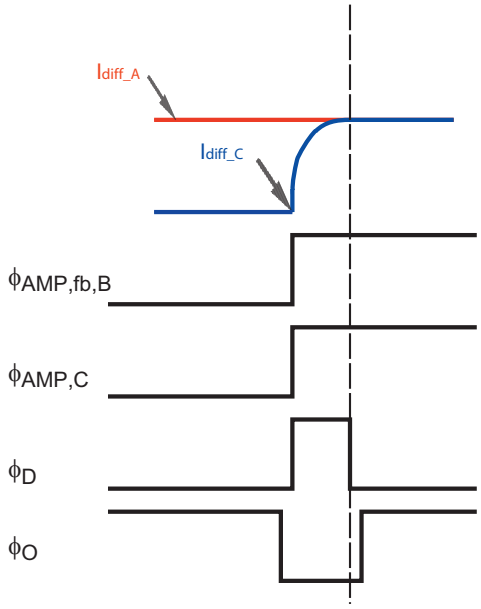

FIGURE 3.15: Differential current from cascodes C and A along with settling phase

The clock phases ϕ_O and ϕ_D (shown in Figure 3.15) are implemented in a non-overlapping fashion. This prevents the output stage from being shorted, which saves the differential voltage on Miller capacitors from being corrupted, eventually preventing a ripple at the output.

3.6 Overall configuration and frequency compensation

As discussed earlier, this amplifier targets a DC gain accuracy of $< 0.01\%$. The error introduced from the finite open-loop gain (A_{OL}) of the amplifier should be much (at least 10 $\times$) less than the desired gain error specifications. The error due to finite open-loop gain is given by,

$$err_{flg} = \frac{1}{A_{OL} \cdot \beta} \tag{3.1}$$

where A_{OL} = Open loop gain and β = Feedback factor

At a gain setting of 1000 (maximum gain setting), the error is given by

$$err_{flg} = 60dB - 20log(A_{OL}) \tag{3.2}$$

AOL should be designed such that the resulting gain error is less than 0.001% (100dB). Hence, from **??** the minimum value of A_{OL} required is 160dB. To achieve such high open-loop gain a three-stage design is used as shown in Figure 3.16 . To make this design stable, a nested miller compensation was used.

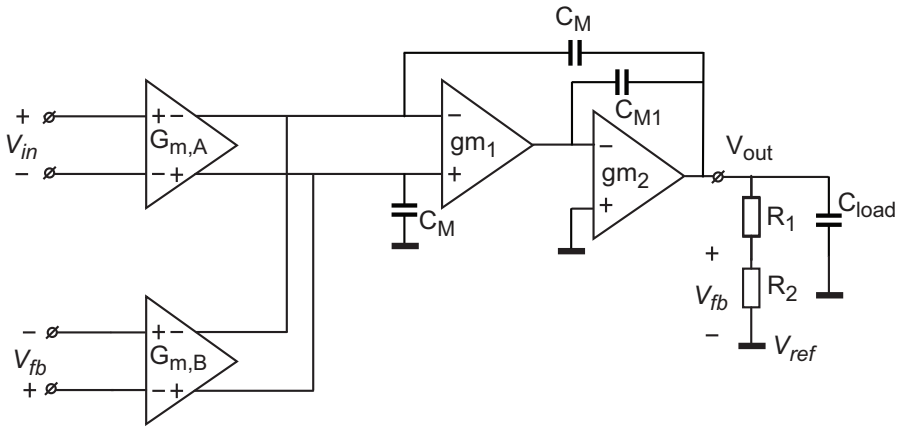

FIGURE 3.16: Overall configuration and frequency compensation

The design equations related to this frequency compensation scheme are given below.

$$\frac{g_m}{2 \cdot \pi \cdot C_M} = 1MHz \tag{3.3}$$

g_m is the transconductance of the input differential pair decided by the amplifier's thermal noise floor specifications.

For a 60 degree phase margin the design equations are as follows:

$$\frac{g_{m1}}{2 \cdot \pi \cdot C_{M1}} = 2MHz \tag{3.4}$$

and

$$\frac{g_{m2}}{2 \cdot \pi \cdot C_{load}} = 4MHz \tag{3.5}$$

value of the transconductance of the intermediate stages. In this implementation the 2nd and 3rd stage from an earlier design were used from [5].

3.7 Sources of residual offset

Residual Offset Due to Finite Open-Loop Gain

Implementing auto-zeroing with amplifiers that have finite open-loop gain, would lead to finite residual offset. In this section, the specifications of the various amplifiers necessary to achieve a residual offset less than $5\mu V$ are derived. Figure 3.17 shows the auto-zeroing loop and the related offset sources in the blocks.

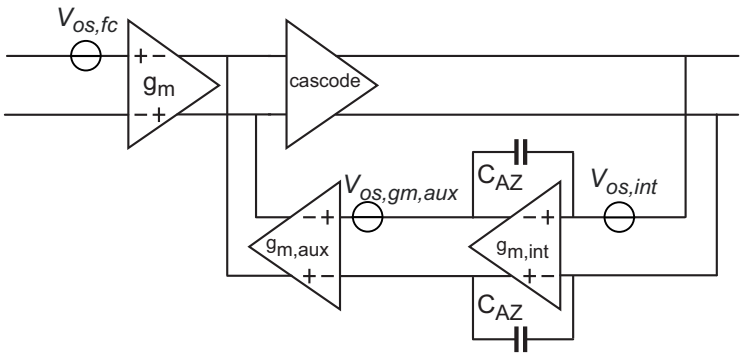

FIGURE 3.17: Sources of offset in a single G_m stage

Transconductor g_m along with the cascode represents a folded cascode amplifier. $V_{os,fc}$ and A_{fc} represent its offset and open-loop gain, respectively. $V_{os,gm,aux}$ represents the offset of the $g_{m,aux}$ block and $V_{os,int}$ is the offset of the integrator. Let A_{int} be the open-loop voltage gain of integrator. The expressions for the resulting input-referred offset of the offset sources shown in the Figure 3.17, are derived.

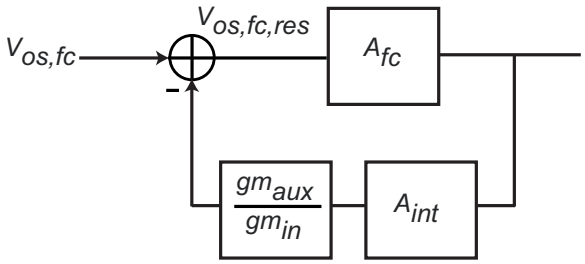

FIGURE 3.18: Offset contribution from folded cascode

The residual offset contribution of $V_{os,fc}$ can be derived using the block diagram ofFigure 3.18. It is given by

$$V_{os,fc,res} = \frac{V_{os,fc}}{1 + \frac{g_{m,aux}}{g_m} \cdot A_{int} \cdot A_{fc}} \tag{3.6}$$

The input-referred residual offset contribution of $g_{m,aux}$, can be derived using the block diagram of Figure 3.19. It is given by

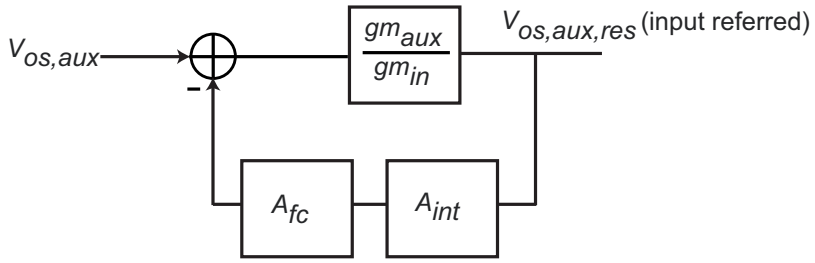

FIGURE 3.19: Input referred residual offset due to offset in $g_{m,aux}$

$$V_{os,aux,res} = \frac{V_{os,gm,aux} \cdot \frac{g_{m,aux}}{g_m}}{1 + \frac{g_{m,aux}}{g_m} \cdot A_{int} \cdot A_{fc}} \tag{3.7}$$

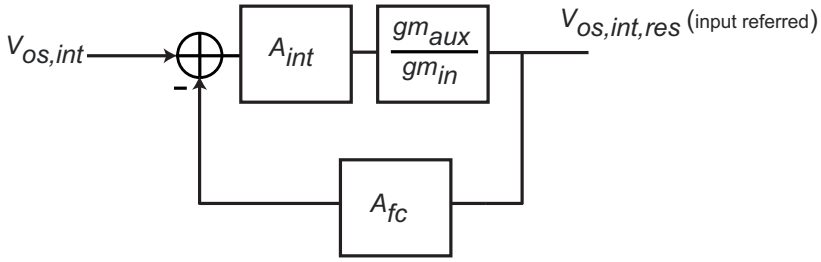

FIGURE 3.20: Input referred residual offset due to offset in integrator

The input-referred residual offset contribution of A_{int}, can be can be derived using the block diagram of Figure 3.20. It is given by

$$V_{os,int,res} = \frac{V_{os,gm,aux} \cdot A_{int} \cdot \frac{g_{m,aux}}{g_m}}{1 + \frac{g_{m,aux}}{g_m} \cdot A_{int} \cdot A_{fc}} \tag{3.8}$$

Residual Offset Due charge injection mismatch

At the end of the auto-zeroing cycle, the charge injection mismatch of the switches connected to the integrator ($\Delta_{q,inj}$), will result in a differential voltage on the auto-zeroing capacitors (C_{AZ}). This voltage, when referred to the input, is a residual offset given by

$$V_{os,ch,inj,res} = \frac{\Delta_{q,inj}}{\frac{g_{m,aux}}{g_m} \cdot C_{AZ}} \tag{3.9}$$

As seen from 3.9, $V_{os,ch,inj,res}$ is attenuated by the ratio of $g_m/g_{m,aux}$. To reduce the effect of this residual offset term, the ratio of $g_m/g_{m,aux}$ is made as high as possible (ideally limited by the supplies).

Equations 3.6 to 3.9 give the input-referred residual offset of one G_m stage , but in the signal path two G_m stages are used simultaneously. Hence, the total input-referred offset

will be twice (worst case) the value given by the sum of 3.6 to 3.9. In Table 3.3 the block specifications are derived by using some initial parameters for the offset of individual blocks.

Sources	Contribution to input-referred offset	Assumed offset of the source	Equations and block specifications
$V_{os,fc}$	$< 1\mu V$	10mV	$A_{int} \cdot A_{fc} > \frac{g_m}{g_{m,aux}} \cdot 2 \times 10^4$
$V_{os,gm,aux}$	$< 0.5\mu V$	5mV	$A_{int} \cdot A_{fc} > 2 \times 10^4$
$V_{os,int}$	$< 1\mu V$	10mV	$A_{fc} > 2 \times 10^4$
$V_{os,ch,inj,res}$	-	-	$\frac{g_m}{g_{m,aux}} \cdot C_{AZ} > 2 \times \Delta_{q,inj} \times 10^6$

TABLE 3.3: Block specifications to achieve residual offset of $< 5\mu V$

Residual Offset Due to Chopping

As this is a chopped amplifier (Section 3.3), the chopping action also gives rise to a residual offset component. Figure 3.21 shows the origin of this residual offset term.

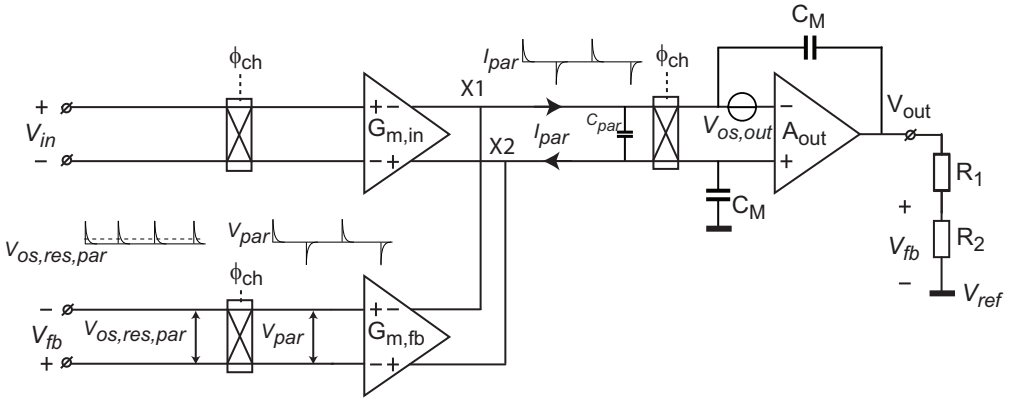

FIGURE 3.21: Residual offset due to $V_{os,out}$

The output chopper will chop the input-referred offset of the stage A_{out} ($V_{os,out}$). The charging and discharging of the parasitic capacitor (C_{par}) at the summing node causes an alternating current I_{par}. This current is provided by the feedback stage, and thus translates into an alternating voltage (V_{par}) at the input of the $G_{m,fb}$. V_{par} when referred to feedback nodes ($V_{os,res,par}$) is chopped by the feedback chopper. The average DC value of $V_{os,res,par}$ corresponds to an input-referred offset [4]. This offset is given by,

$$V_{os,res,par} = \frac{2 \cdot C_{par} \cdot V_{os,out} \cdot f_{ch}}{G_{m,fb}} \tag{3.10}$$

Here f_{ch} is the chopping frequency. To minimize $V_{os,res,par}$, the values of C_{par} ,$V_{os,out}$ and f_{ch} should be minimized and $G_{m,fb}$ should be maximized. To minimize C_{par}, and $V_{os,out}$ proper layout must be done. The value of f_{ch} depends on the switching frequency f_{PPP} and $G_{m,fb}$ is determined by the desired thermal noise floor. For $C_{par} = 500fF$ (on higher side), $V_{os,out} = 20mV$, $f_{ch} = 10kHz$ and $G_{m,fb} = 150uS$, $V_{os,res,par}$ is $1.3\mu V$. Hence, the residual offset contribution of $V_{os,res,par}$ can be substantial. A proper layout to reduce C_{par} and a low chopping frequency can reduce the residual offset contribution of $V_{os,res,par}$.

Requirements to cancel the initial offset

The offset nulling circuitry should be able to cancel the input offset. To be able to achieve this, the following criteria should be met:

- The $g_{m,aux}$ stage should be able to provide sufficient differential current so that the offset current of the input stage is can be completely cancelled. This current is given by,

$$I_{tail,gm,aux} \geq g_m \cdot V_{os,fc,max} \tag{3.11}$$

where, $I_{tail,gm,aux}$ is the tail current of auxiliary transconductor and
$V_{os,fc,max}$ is the maximum offset of folded cascode

- As discussed earlier, the ratio $g_m/g_{m,aux}$ is designed to be high. Hence, the voltage swing required at the input if the auxiliary stage should be scaled by this factor. Since the integrator provides this voltage, the output nodes of the integrator should be able to provide a differential voltage swing given by,

$$V_{swing,integ} \geq \frac{g_m}{g_{m,aux}} \cdot V_{os,fc,max} \tag{3.12}$$

where, $V_{swing,integ}$ is the differential voltage swing at the output of the integrator.

PPP switching and residual offset

A very important implication of the PPP switching is that it translates the residual offset of every G_m stage to $f_{ppp}/6$. Consider the residual offset of the three stages to be $V_{os,res,A}$, $V_{os,res,B}$ and $V_{os,res,C}$. Table 3.4 shows the effect of PPP switching on residual offset.

State/Step	1	2	3	4	5	6
Input Stage	A	A	B	B	C	C
Feedback Stage	B	C	C	A	A	B
Resulting residual offset	$V_{os,res,A} - V_{os,res,B}$	$V_{os,res,A} - V_{os,res,C}$	$V_{os,res,B} - V_{os,res,C}$	$V_{os,res,B} - V_{os,res,A}$	$V_{os,res,C} - V_{os,res,A}$	$V_{os,res,C} - V_{os,res,B}$

TABLE 3.4: Effect of PPP switching on residual offset

The residual offset during phase 1 and 4 are opposite in magnitude, and similarly the residual offset of phases 2 and 5 and phases 3 and 6 will be opposite. Hence the PPP switching translates the residual offset of each stage to $f_{ppp}/6$. Hence, the residual offset in a PPP IA will be dominated by the offset due to output stage (given by Equation 3.10). This offset is dependent on layout and the switching frequency. Hence, in the actual implementation, the switching frequency is kept variable. This allows the freedom to choose a particular switching frequency where the resulting offset is in accordance with target specifications.

Chapter 4

Ping-Pong-Pang Transistor-Level Implementation

Chapter 3 discussed the system level implementation detail of Ping-Pong-Pang (PPP) IA. This chapter discusses the implementation at transistor-level, such that the PPP IA system requirements derived in chapter 3 are fulfilled. To implement the PPP IA prototype chip on silicon, a $0.5\mu m$ CMOS process from National Semiconductor was used.

Figure 4.1 shows a block-level details of the whole PPP IA system which is implemented on silicon. It consists of a core block of PPP IA, which is the system discussed in previous chapter. Some auxiliary blocks like bias generator, switching clock generator and Serial to Parallel Interface (SPI) assist the working of PPP IA block and also allow programmability to the amplifier. An external feedback network will be used to define the gain.

This chapter is organized as follows; Section 4.1 discusses the transistor-level implementation of PPP IA block. Section 4.2 briefly explains the auxiliary circuits. Section 4.3 discusses the simulation results.

4.1 PPP IA design

The details of the PPP IA block of Figure 4.1 are shown in Figure 4.2 . The following subsections discuss the design of the three identical G_m stages and the output stage.

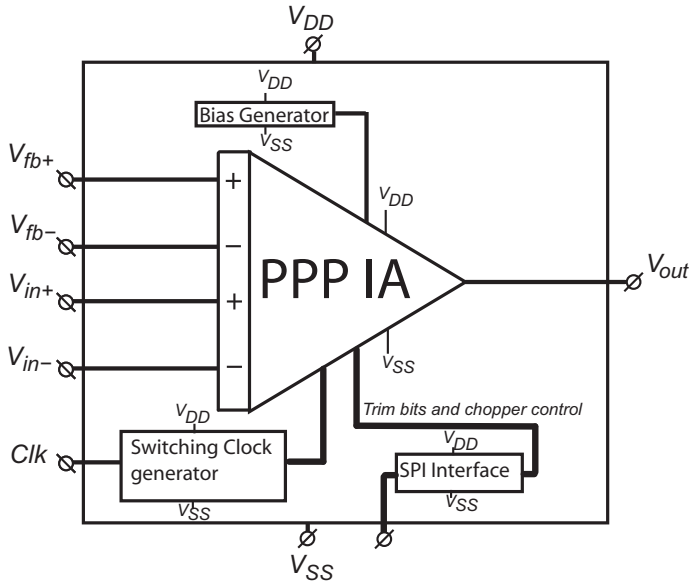

FIGURE 4.1: Block diagram of PPP IA chip

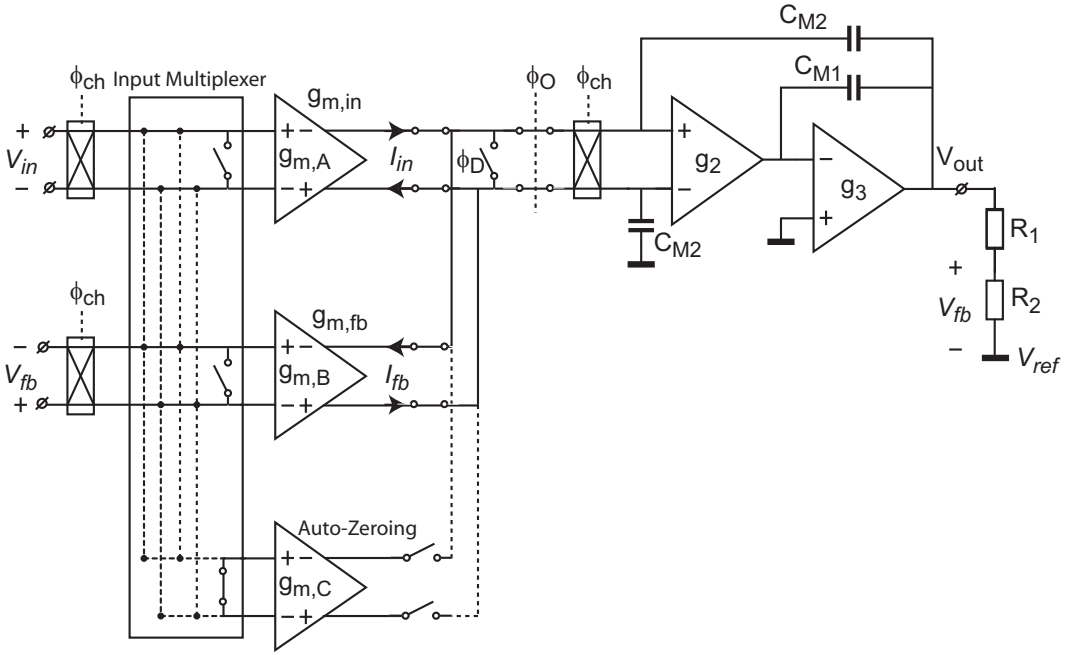

FIGURE 4.2: PPP IA Core block

4.1.1 Implementation of G_m stage

Figure 4.3 shows block-level details of a single G_m stage. The G_m stage consists of a transconductor g_m, a cascode block and an offset-nulling circuitry. The offset-nulling circuitry consists of an active integrator ($g_{m,int}$ and C_{AZ}) and an auxiliary transconductor stage $g_{m,aux}$. The circuit level implementation of G_m stage is discussed in two parts i.e. one part consisting of a combined implementation of g_m, $g_{m,aux}$ and the cascode stage and the other part discussing the implementation of the integrator stage.

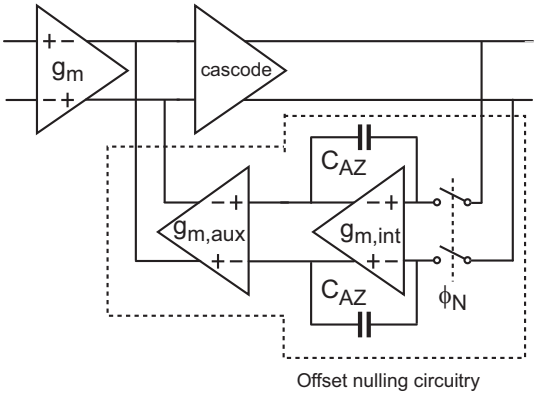

FIGURE 4.3: Block level details of the G_m stage

The input transconductor g_m along with the cascode block consists of a folded cascode. Figure 4.4 shows the transistor implementation of the folded cascode along with the $g_{m,aux}$ stage.

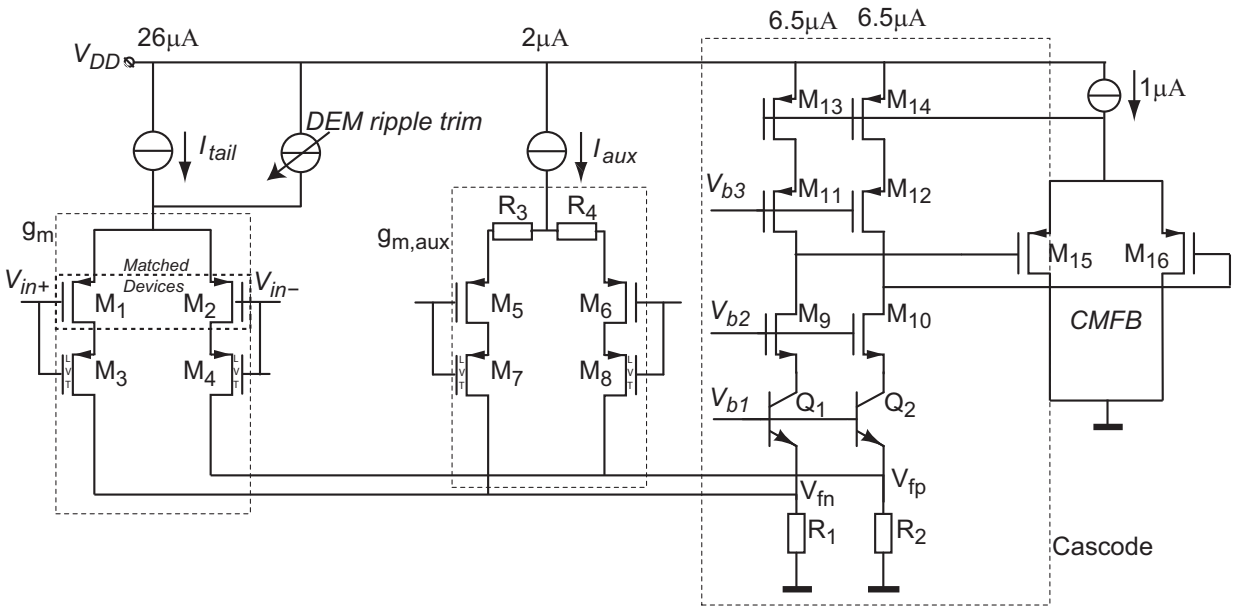

FIGURE 4.4: Folded cascode amplifier with the gm_{aux} stage

The parameters determined by the folded cascode implementation are noise and the input CMVR. The following discussion derives the design parameters required to achieve

the noise specifications and the CMVR. Further the various sub-circuits to implement this folded cascode is discussed.

Tail current value to achieve Noise Specifications

The tail current required to bias the input stage is determined as follows. The input-referred thermal noise of a simple differential pair is given by [razavi],

$$V_n^2 = \frac{16 \cdot kT}{g_m} \tag{4.1}$$

Where, V_n is noise voltage in $V/\sqrt{Hz}$,k is boltzmann's constant, T is temperature in Kelvin and g_m is the transconductance of the input stage. For the desired $V_n = 27nV/\sqrt{Hz}$, this leads to $g_m = 90.8\mu S$. However, in a CFIA, the input as well as the feedback stage contributes noise. Hence, the noise powers will add giving the effective noise .

$$V_n^2 = V_{n,in}^2 + V_{n,fb}^2 \tag{4.2}$$

Therefore the effective noise power will be doubled. To achieve a thermal noise floor of $27nV/\sqrt{Hz}$ now, the g_m should be twice the value calculated from 4.1, i.e.

$$g_m = 2 \times 90.8\mu S \tag{4.3}$$

To achieve a high transconductance from the input stages, they are biased in weak inversion. Hence,

$$I_d = n \cdot V_T \cdot g_m = 8.5\mu A \tag{4.4}$$

Where, I_d= Drain current flowing in the input transistor
V_T=Thermal voltage (26mV at room temperature)
n= process dependent parameter (between 1-2)

Hence, the tail current is given by

$$I_{tail} = 2 \times I_d = 19\mu A \tag{4.5}$$

The tail current used in the actual implementation is $26\mu A$, which corresponds to $g_m = 213\mu S$. It is somewhat higher than calculated, to compensate for the noise contribution of resistors R_1 and R_2 and transistors M_{13} and M_{14}.

Gain error, Mismatch and CMRR

Recollecting from chapter 1, the gain error in a CFIA is determined by the mismatch of the input and feedback g_m's. This mismatch has two components, one resulting from the mismatch of I_{tail} and the other resulting from CM dependency of the input transconductance (value of g_m). Methods used to counter the cause of these gain error components are mentioned below.

1. To counter against the gain error resulting from I_{tail} mismatch, a two way approach is used. Firstly, the devices implementing I_{tail} in all the three g_m's, are laid out in a matched fashion. Secondly, as discussed in chapter 3, the switching sequence inherently DEMs the input stages, hence reducing the DC gain error.

2. Fundamentally, the CM dependence of the input transconductance can be attributed to the finite CMRR of the input stage. The CMRR of the input stage can be defined as the dependency of its transconductance on the input CM level. This can happen due to two factors. Firstly, due to finite output impedance of the current source implementing I_{tail}, resulting in variation of I_{tail} with the input CM level, leading to a variation in transconductance value over the input CMVR. Secondly, the finite output impedance of the input transistors (M_1 and M_2) can also change their transconductance with the input CM level. Since, the input and reference CM level can be different, any CM dependency on the input transconductance would lead to a gain error. In the previous implementations of CFIAs [5, 15], different techniques have been used to achieve a high CMRR in the input stage. For a small input differential range, the technique used in [15] is more power efficient as compared to the technique in [MAP]. As the target differential input range for this implementation is small (-50mV to 50mV), an input stage implementation as in [15] is used.

Methods to achieve the input CMVR of $(0V - (V_{dd} - 1.75V))$

The CMVR for this amplifier is defined as the range in which the gain error is less than 0.01%. The methods used to achieve the CMVR range of $(0V - (V_{dd} - 1.75V)$ are discussed below.

1. The inputs transistors (M_1 and M_2) are cascoded with Low Threshold (LVT) devices (M_3 and M_4). This prevents the input transistors from being exposed

to the full input CM level variation, by maintaining a constant V_{ds} across the these transistors. This increases their output impedance, hence reducing the CM dependent gain error.

2. Implementing the input stage as a PMOS differential pair enables ground sensing, because of the inherent level shift provided by the gate to source voltage of the input transistors (M_1 and M_2). The lowest input CM level ($V_{CM,low}$) is determined by the input CM voltage at which the LVT cascode devices M_3 and M_4 go into their triode region. The relation between the input CM level and the saturation voltage of LVT cascode is given by:

$$V_{CM,in} + V_{gs,M3,4} - V_{dsatM3,4} - V_{R1,2} = 0 \tag{4.6}$$

To ensure that the gain error is less than 0.01%, the cascode devices should be in saturation over the full input CMVR. $V_{CM,low}$ is dependent on the values of $V_{dsatM3,4}$, $V_{gsM3,4}$ and $V_{R1,2}$. At a certain tail current level, the value of $V_{gsM3,4}$ determines the value $V_{dsM1,2}$ ($V_{gsM1,2} - V_{gsM3,4}$), which in turn determines the output impedance of the input transistors M_1 and M_2. To achieve a high output impedance, transistors M_3 and M_4 are sized to achieve the highest possible value of $V_{dsM1,2}$ (limited by threshold voltage difference of normal device and the LVT device over process corners and temperature). Hence, to go lower on the input CM level, the value of $V_{R1,2}$ has to be reduced. For a constant current $I_{R1,2}$ (sum of biasing currents of g_m, $g_{m,aux}$ and cascode), the value of $V_{R1,2}$ can be decreased by decreasing the value of R_1 and R_2. R_1 and R_2 are sized such that over process corners and temperatures, and at $V_{CM,in} = -100mV$, the gain error is less than 0.01%. The minimum values of R_1 and R_2 are limited by the thermal (current) noise contribution of these resistors.

3. The tail current source is implemented using a cascoded current source, such that the tail current is constant over the entire input CM level. Variations in tail current source with the input CM level can limit the CMRR of input stage. The impedance of the current source is designed such that over the inputCMVR the maximum resulting gain error resulting from tail current variation, is less than 0.01%.

4. The highest input CM level is given by $V_{dd} - (V_{ov6} + V_{dsat5} + V_{CM,in}$. Over process corners and the required temperature range (-40℃ to 125℃), the simulated $V_{CM,in}$ for which the gain error is less than 0.01% is $V_{dd} - 1.75V$.

Cascode implementation

The cascode block implementation is different from the normal folded-cascode structure, with the signal current being summed over resistors R_1 and R_2 (rather than a current source). This facilitates ground sensing, as a normal current source would require more headroom than a resistor. An advantage of using resistor along with a bipolar cascode Q_1 and Q_2 is that they do not contribute to $1/f$ noise. Hence, this implementation is more noise efficient compared to an implementation involving NMOS cascodes. A pair of NMOS cascode devices M_9 and M_{10} is used to increase the voltage gain of the overall cascode. The CM level at the output nodes of the cascodes is sensed by transistors M_{14} and M_{15} and controlled by the transistors M_{13} and M_{14}. Cascode transistors M_{11} and M_{12} are used to increase the impedance at the output nodes. Over process corners and temperatures, the open loop gain of the folded cascode exceeds 92dB.

Input differential range and the cascode

The cascode branches are biased at a level that corresponds to a differential input voltage of $15mV$:

$$g_m \cdot V_{in} = 2 \cdot 213\mu S \cdot 15mV = 6.5\mu A \tag{4.7}$$

Though the required input differential range is $-50mV$ to $50mV$, the cascode branch can be biased at a lower level because of the class-AB operation of transistors Q_1 and Q_2. Which can be explained as follows. The input signal current is added at their emitters (nodes V_{fn} and V_{fp}). At high differential input signals, the voltages at these nodes will vary substantially, hence changing $V_{BE,Q1,2}$. Since the value of $V_{BE,Q1,2}$ defines the current in the cascode branch, a variation in $V_{BE,Q1,2}$ with the input differential voltage would lead to a biasing which is dependent on the input signal level. However, this biasing can be non-linear due to nonlinearity of the cascode devices (Q_1,Q_2). In a CFIA, this non-linearity is cancelled by the feedback path. Hence, the overall input to output transfer remains linear. The minimum value of the bias current is limited by the stability of the CMFB loop. However in this implementation, to be on the safer side, the cascode is biased for a differential input signal of $15mV$.

CMFB for cascode

As the outputs of the cascode are always connected to a virtual ground (both in amplifying and auto-zeroing state), the output nodes of the cascode does not have a voltage swing requirement. Hence, the CMFB loop is implemented as in Figure 4.4. The CM level is given by $V_{dd} - V_{gsM13} - V_{gsM15}$. Over process corners and temperature, the CM level can vary from $V_{dd} - 1.2V$ to $V_{dd} - 2.3V$. The biasing of devices in the cascode

branch is such that with these variations in CM level, the devices in cascode branch remain in their desired operation region.

Auxiliary transconductor $g_{m,aux}$

As seen from Figure 4.4, the auxiliary transconductor ($g_{m,aux}$) drives a differential current in the folding node of the folded cascode, such that the offset of the input stage is nulled. The tail current of the auxiliary stage is decided by $g_{m,in} \cdot V_{os,max}$ (the maximum offset of the input stage). The ratio of $g_{m,aux}/g_m$ determines the order to which the charge injection mismatch error at the end of the auto-zero cycle is attenuated. In this implementation a $g_m/g_{m,aux}$ ration of 40 is used. The value of $g_{m,aux}(5\mu S)$ is set by the degeneration resistors R_3 and R_4. The minimum possible value of $g_{m,aux}$ is determined by the available voltage swing at the output terminals of the integrator.

DEM ripple trimming

As discussed in chapter 3, the DEM'ing of the input stages, while it eliminates gain errors due to transconductance mismatch, also leads to ripple. As shown in Figure 4.4, a 5-bit current DAC is used to trim the initial transconductance mismatch so as to reduce this ripple. The DAC is implemented using five binary-weighted current sources. These current sources are derived from the same current source used to implement I_{tail}, such that the trimming holds over temperature. The DAC is designed to accommodate a trim range which is twice the maximum mismatch calculated from Monte Carlo simulations (0.4%). As seen from Figure 4.4, the DAC can only add current to the tail current source. Hence, trimming can only increase the transconductance of the input stage. The method for trimming is to reset the switching sequence (discussed in section 3.2) and then measure the output ripple as the IA switches through different stages. The ripple at every state gives the mismatch information; this gives initial mismatch information from which approximate trim bits can be determined. Further the trimming is done iteratively to find the exact trim sequence for which the resulting ripple is lowest.

Implementation of Integrator

As shown in Figure 4.5, a folded cascode amplifier is used to implement the integrator. The input stage is a PMOS differential pair, which is designed to accommodate the entire output CM level variation of the cascode stage. The required voltage swing at the output of the integrator is decided by the value of $(g_m/g_{m,aux}) \cdot V_{os,max}$. For a maximum offset of 10mV ($V_{os,max}$) in the input stage, the swing at the output nodes of the integrator should be $400mV(g_m/g_{m,aux} = 40)$. The output nodes of the integrator are designed to accommodate this swing. The voltage gain of the integrators is more than 70dB over process and corners. The output CM level is maintained at mid-supply by a CMFB block.

$$BW_{az} = \frac{g_{m,aux}}{2 \cdot \pi \cdot C_{AZ}} \cdot \frac{R_{1,2}}{\frac{1}{g_{m,Q1,2}} + R_{1,2}} > 100kHz \tag{4.8}$$

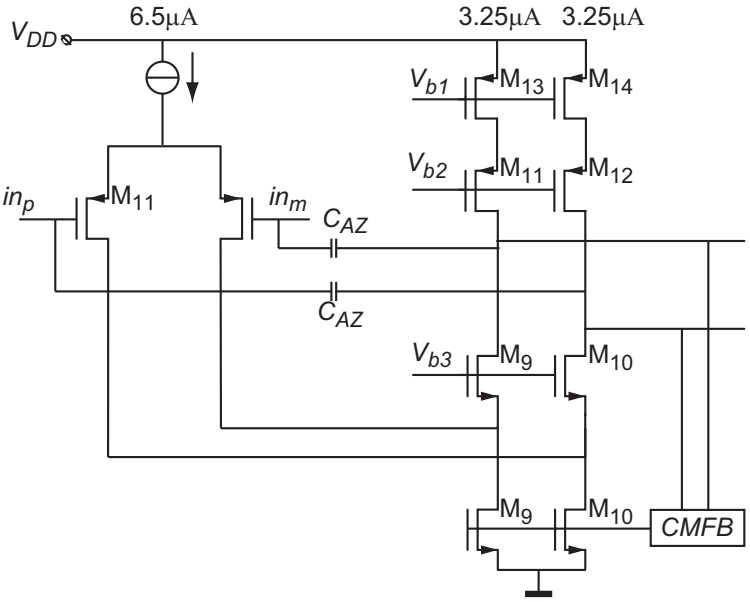

FIGURE 4.5: Implementation of Integrator

Bandwidth of the auto-zero loop

The bandwidth of the auto-zeroing should be such that, within one auto-zeroing cycle the loop must be able to settle to the offset level. The frequency f_{ppp} determines the time allowed for auto-zeroing. In this design, f_{ppp} is determined by an external clock. Hence, the auto-zeroing loop bandwidth (BW_{az}) should be such that it can accommodate the maximum desired f_{ppp}. A value of $f_{ppp,max} = 100kHz$ ($f_{ppp,max}$ is rather high owing to the discussion in section 3.4) is assumed in this design.

4.1.2 Output stage

The output stage (a two-stage Miller-compensated design) is identical to that of the [5] design, and will therefore not be discussed in detail here. The system level implementation of the output stage along with the frequency compensation has been discussed in 3.6. The value of miller compensation capacitor C_{M1} can be calculated as follows

$$C_{M1} = \frac{1MHz}{2 \cdot \pi g_m} = 54pF \tag{4.9}$$

4.2 Auxiliary circuits

As shown in Figure 4.1, apart from the PPP IA core, a few other blocks are required to implement the prototype chip. These auxiliary circuits are briefly discussed in this section.

A biasing source from LMP8358 [16] design was used, which generates a PTAT bias current. This current is distributed across the chip and used to bias all circuits.

The clock phases driving the switches are generated by an on-chip digital circuit, which is driven by an external clock. Figure 4.6 shows the block-level implementation of this circuit.

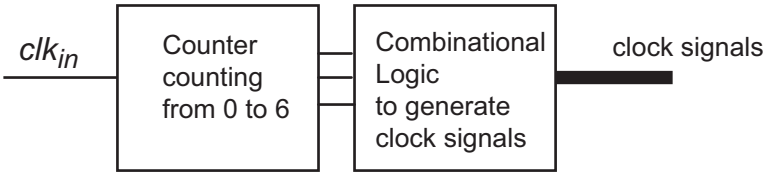

FIGURE 4.6: Implementation of digital clock generation on chip

A counter is used to count the 6 states. The output of the counter is used by combinational logic to generate the desired clocks for the switching of the stages. The non-overlapping clocks generated by using standard delay blocks from the logic library.

To control the 5-bit DACs which trim the DEM ripple, 15 bits of information is required for the three input stage. Hence, an SPI interface is used to pass this information to current DACs. This interface is also be used to switch the chopping on and off.

4.3 Simulation results

In this section, simulation results of the amplifier are shown. This includes the overall loop stability analysis, PSS noise analysis, and Monte-Carlo analysis for gain error and offset.

Figure 4.7 Shows the closed loop stability plot of the overall loop. As seen from the figure, the amplifier is stable at a gain of $5\times$ (minimum gain setting designed for) it always has a has a phase margin of more than 60 degree (over process corners, temperature and supply).

Figure 4.8 shows the output noise (using PSS) of the amplifier with chopping on and chopping off at a gain setting of 10 and $f_{ppp} = 20kHz$. When only auto-zeroing is on, the noise folding due to sample and hold action of auto-zeroing is evident from the plot. The

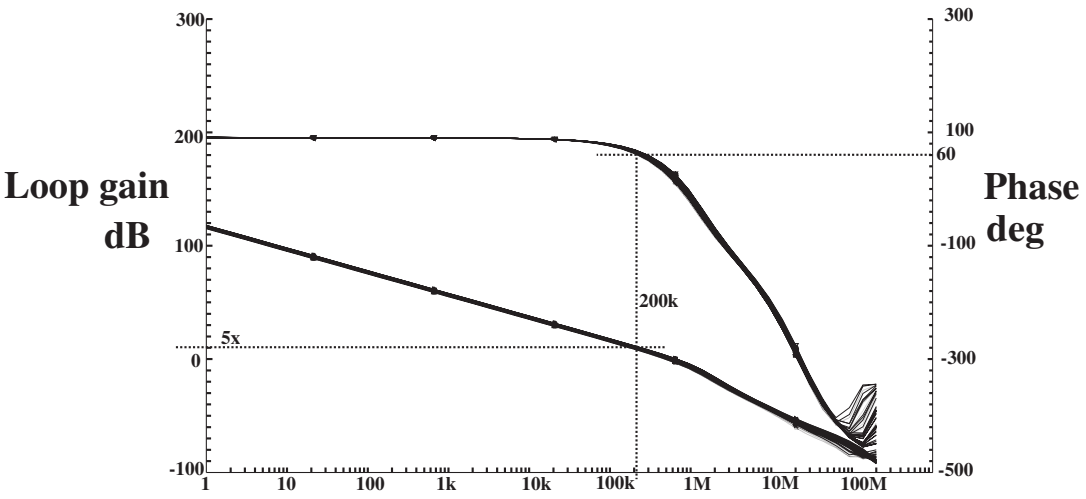

FIGURE 4.7: Closed loop stability plot

DC noise floor is $\sqrt{BW_{az}/f_{az}}$ higher than the thermal noise floor. With an auto-zeroing bandwidth $BW_{az} = 112kHz$ and an auto-zeroing frequency of$f_{az} = f_{ppp}/3 = 6.66kHz$, a factor of 4.10 higher noise is expected. With a thermal noise floor of $27nV/\sqrt{Hz}$, this corresponds to $110nV/\sqrt{Hz}$. The simulated low-frequency noise floor is $118nV/\sqrt{Hz}$. The notch due to auto-zeroing at 33.33% duty cycle is at 10 kHz ($1.5 \cdot f_{az}$).

To modulate the folded noise away from DC, chopping at 10 kHz is done. Figure 4.7 shows the PSS noise plot when the choppers are on. The folded noise is up converted to the chopping frequency. After chopping, the noise floor is equal to the thermal noise floor of $27nV/\sqrt{Hz}$.

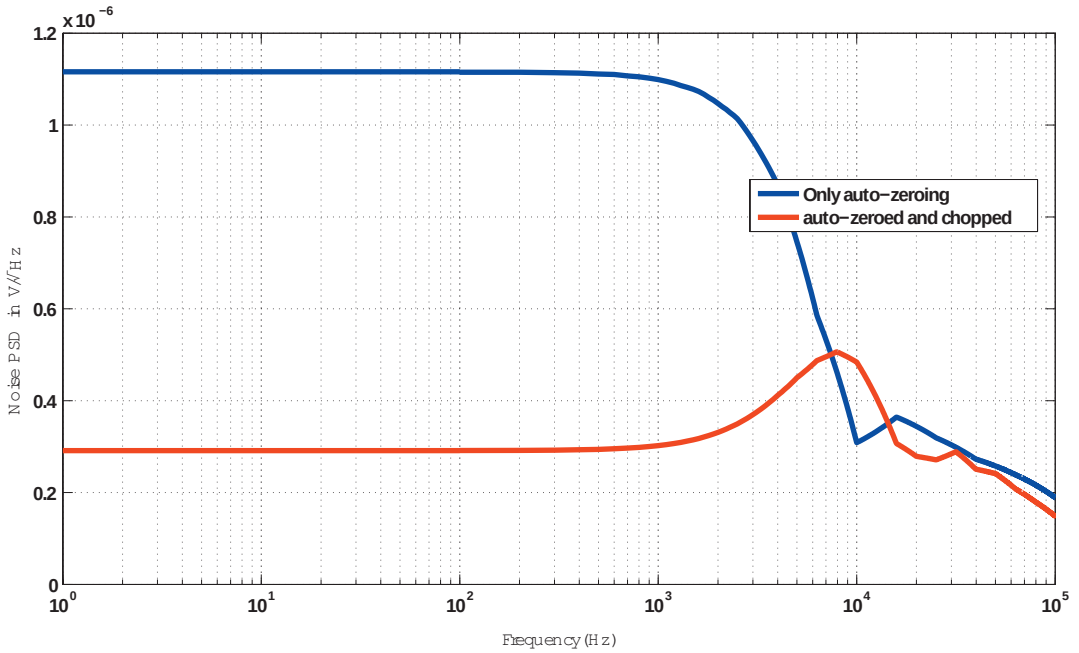

FIGURE 4.8: PSS noise analysis at a gain of 10, f_{ppp}=20kHz, with and without chopping

Monte Carlo analysis on pre and post layout extracted view was done. The worst case values for offset, gain accuracy and the DEM ripple were evaluated. Table 4.1 lists the results of the MC analysis. It shows the worst case results (3σ for 50 runs) at an $f_{ppp} = 20kHz$.

Parameter	Pre layout $V_{CM,ref} = 2.5V$		Post-layout $V_{CM,ref} = 2.5V$	
	$V_{CM,in} = 2.5V$	$V_{CM,in} = -100mV$	$V_{CM,in} = 2.5V$	$V_{CM,in} = -100mV$
Offset	$800nV$	$1.2\mu V$	$3.7\mu V$	$5.5\mu V$
Gain Error	0.003%	0.026%	0.004%	0.08%
DEM Ripple	$53mV(V_{in} = 50mV)$	$53mV(V_{in} = 58mV)$	$60mV(V_{in} = 50mV)$	$65mV(V_{in} = 50mV)$

TABLE 4.1: Monte carlo results for $f_{ppp} = 20kHz$

Chapter 5

Measurement Results and Conclusion

In the previous chapter, the transistor-level implementation of the Ping-Pong-Pang Instrumentation Amplifier was discussed. The test chip was fabricated by National Semiconductor. This chapter presents the measurement results on the fabricated devices and is organized as follows: Section 5.1 describes the fabricated devices and briefly discusses the test setup. Section 5.2 and 5.3 discusses the DC and AC measurement results respectively. Section 5.4 compares the measured results with the state-of-the-art CFIA. Section 5.5 concludes this thesis.

5.1 Fabricated devices and test setup

The test chip was implemented in National Semiconductor's $CMOS7\_5v$ process. This is a CMOS process with minimum feature size of $0.5\mu m$. Figure 5.1 shows the chip micrograph where the active area of the die is $1130\mu \times 1350\mu m (1.485mm^2)$. A DIP-16 package is used for packaging the samples. A total of 26 devices were measured.

A test PCB was designed to evaluate the performance of the test chip. Figure 5.2 shows the block diagram of the test setup. An input attenuation network ($A1$) is used to attenuate the large input voltage (the minimum voltage range of signal generator is $20mV_{p-p}$) to a small value, which is compatible with the input range of the PPP IA. A manually programmable (using jumpers) feedback network (FB) with different gain settings is used to verify the functionality of PPP IA at different gains. The on-chip SPI interface is programmed by an external USB to SPI converter provided by

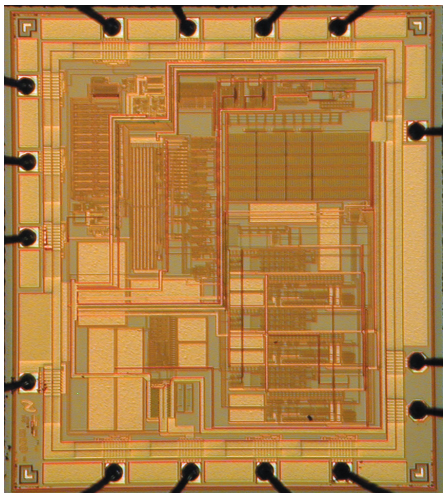

FIGURE 5.1: Die Micrograph of the Chip

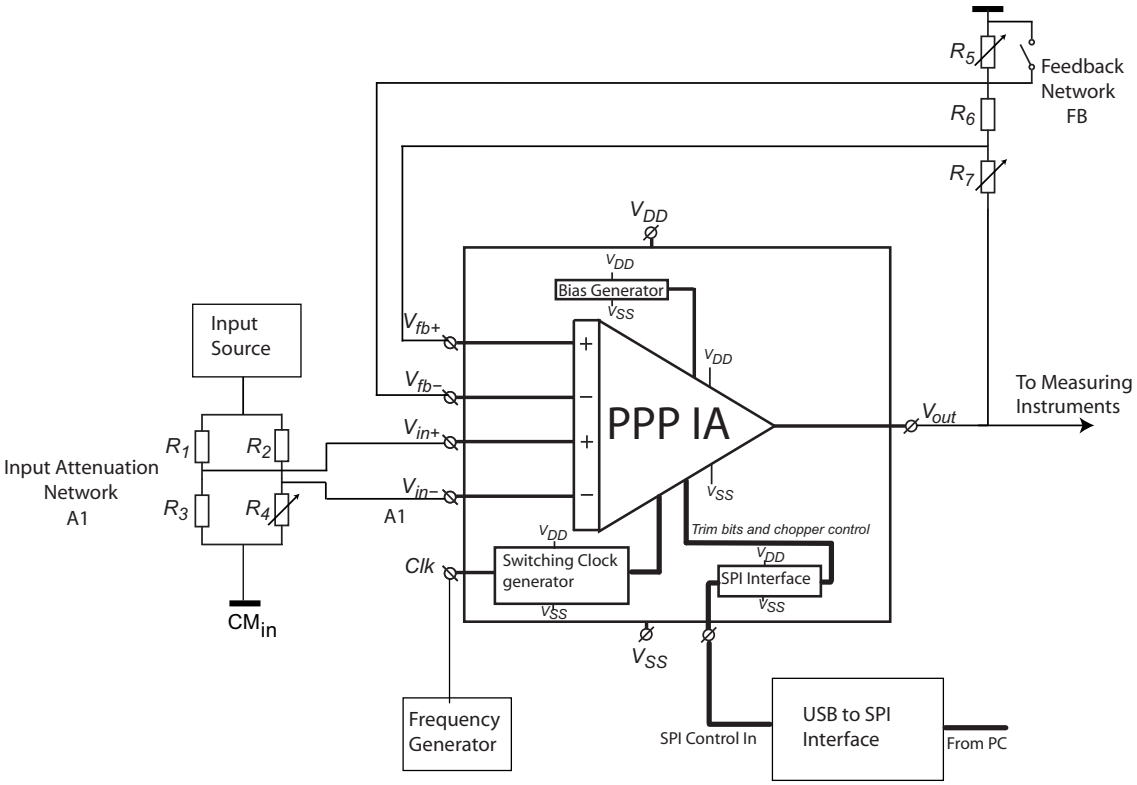

FIGURE 5.2: Block diagram of the test setup

National Semiconductor. The clock generator inside the chip is controlled by an external (programmable) square wave generator.

5.2 DC measurement results

This section presents the measurement results of parameters like offset, *Common Mode Rejection Ratio* (CMRR) , *Power Supply Rejection Ratio* (PSRR) and the DC gain error. To measure the DC value accurately, Keithley 2002 multimeter was used which can be programmed for high precision measurements. LabView was used to capture the data from the equipments and perform further mathematical calculations.

Offset Measurement Results

To determine the offset of the amplifier, the input terminals of the amplifier was shorted to a $V_{CM,in}$ of 2V (supply of 5V) and $V_{CM,ref}$ was set to 2V. The feedback network was set such that the amplifier is at a gain of 1000. A high gain setting is used such that the resulting output offset is at mV levels (for offsets at the μV level) and can be precisely measured. The DC value at the output, when divided by 1000 gives the input referred offset.

As discussed in chapter 3, the switching frequency (f_{ppp}) in this design is externally controlled. To determine the switching frequency, the offset performance of a sample was determined by varying the switching frequency. Ideally, the f_{ppp} should be as high as possible, (limited by auto-zero loop bandwidth of $112kHz$) such that the DEM ripple is suppressed by the filtering action of the overall input to output transfer (Section 3.5) . On the other hand, switching at a higher frequency increases the residual offset (discussed in Section 3.7). At $f_{ppp} = 22kHz$, this sample has an offset of $1.5\mu V$. Assuming this sample to be a typical sample, since the offset measured at $f_{ppp} = 22kHz$ is $1.5\mu V$, this value may vary for other samples. Since, the the target specification for offset was $5\mu V$, assuming a $1.5\mu V$ offset for a typical device would make sure that the other samples achieve the offset specifications. Hence, a f_{ppp}=22kHz is used for measurements of all other parameters for all the devices.

The offset measurement described above, was done for 26 samples. Figure 5.3 shows the histogram of the input referred offset voltage for the measured devices. From the histogram, the worst case offset value is $4\mu V$, and a typical offset value ($|\mu| + \sigma$) is $1.8\mu V$.

CMRR Measurement Results

To evaluate the CMRR of the test chip, the variation of offset over the input CM range

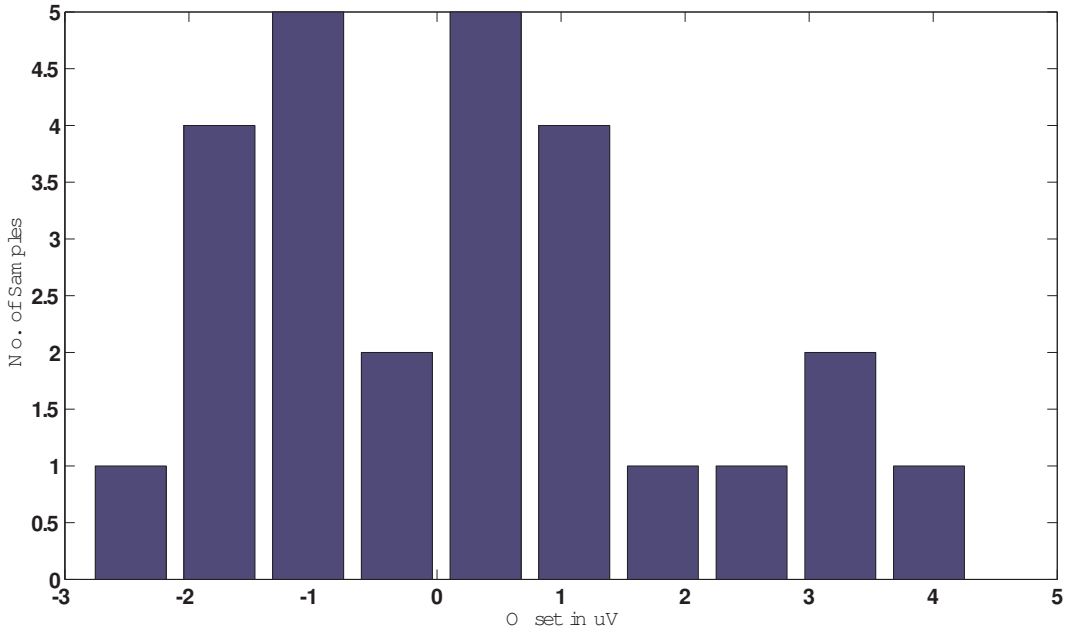

FIGURE 5.3: Histogram of offset (in μV) for 26 samples at $V_{CM,in} = V_{CM,ref} = 2V$

was determined. To perform this measurement, the offset of the test chips was measured by varying the input CM level from 0V to 3.25V. The CMRR can be evaluated as follows:

$$CMRR = 20log(\frac{3.25}{V_{os,var,CMRR}}) \tag{5.1}$$

Here, $V_{os,var,CMRR}$ is the variation of the offset when input CM level is swept from 0V to 3.25V.

Figure 5.4 shows the histogram of the DC CMRR evaluated from the measured data for 26 samples. The worst case value of DC CMRR is 122dB, and a typical value of $(|\mu|+\sigma)$ 123.5dB

PSRR Measurement results

To evaluate the DC PSRR of the test chip, the variation of the offset by varying the power supply was determined. The offset was measured by varying the power supply from 3.3V to 5.8V. The input and feedback transconductors were put at 1V CM level. The DC PSRR is then given by

$$PSRR = 20log(\frac{5.8 - 3.3}{V_{os,var,PSRR}}) \tag{5.2}$$

Here, $V_{os,var,PSRR}$ is the variation of the offset when power supply level is swept from 3.3V to 5.8V. Figure 5.5 shows the histogram of DC PSRR evaluated from the measured

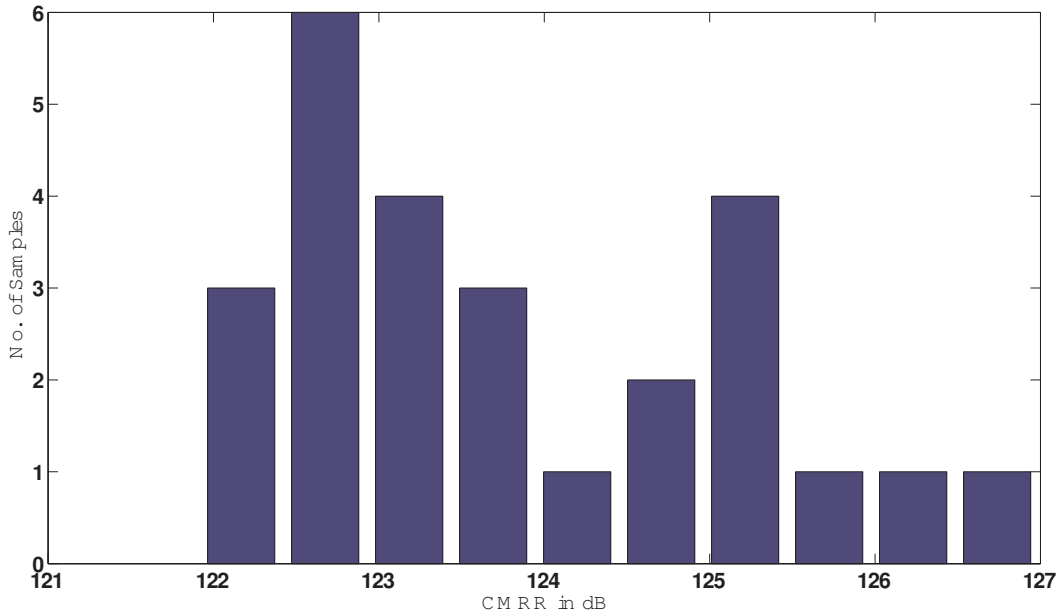

FIGURE 5.4: Histogram for CMRR of 26 samples in input CMVR 0V-3.25V

data for 26 samples. Worst-case value of PSRR is 128dB, and a typical case ($|\mu| + \sigma$) value of PSRR is 136dB.

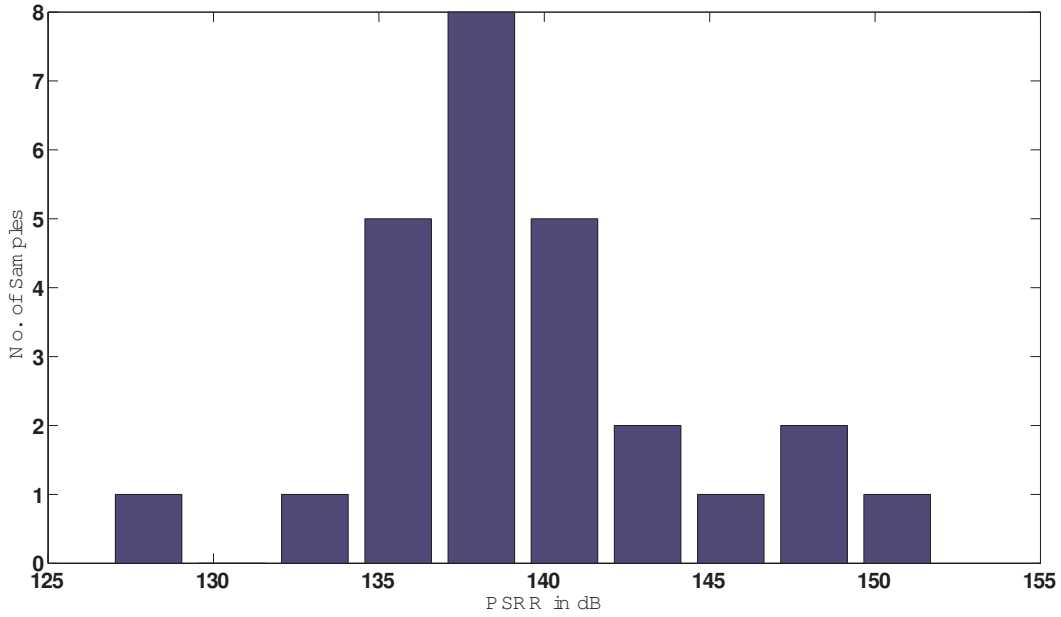

FIGURE 5.5: Histogram for PSRR with supply range from 3.3V to 5.8V

DC gain error measurement results

Since, this amplifier was desegned for an absolute DC gain error of $< 0.01\%$ it is challenging to measure the performance at such high precision. The method used for determining the gain error is described before presenting the gain error measurement data.

To determine the value of absolute gain error of the amplifier, it should be ensured that other sources in the measurement system do not introduce significant errors in the measurement. For the measurement setup shown in Figure 5.2, the input to output transfer is given by

$$T_x = \frac{FB}{A1} \cdot PPPIA_{gainerror} \tag{5.3}$$

Where, FB is the inverse of feedback factor, $A1$ is the attenuation factor of Attenuation network and $PPPIA_{gainerror}$ is the gain error introduced by the PPP IA. To calculate the exact value of $PPPIA_{gainerror}$ the value of $FB/A1$ should be determined. Since the actual value of the resistors implementing FB and A1 may vary by more than 0.1%, this mandates the need to calibrate the value of $FB/A1$ before the measurement. FB and $A1$ are implemented using very low temperature coefficient resistors ($5ppm/℃$). Since the temperature may vary across the test PCB, using a low temperature coefficient resistor will do away with the need to calibrate the value of $FB/A1$ during the measurements. Figure 5.6 shows the setup used to determine the value of $FB/A1$.

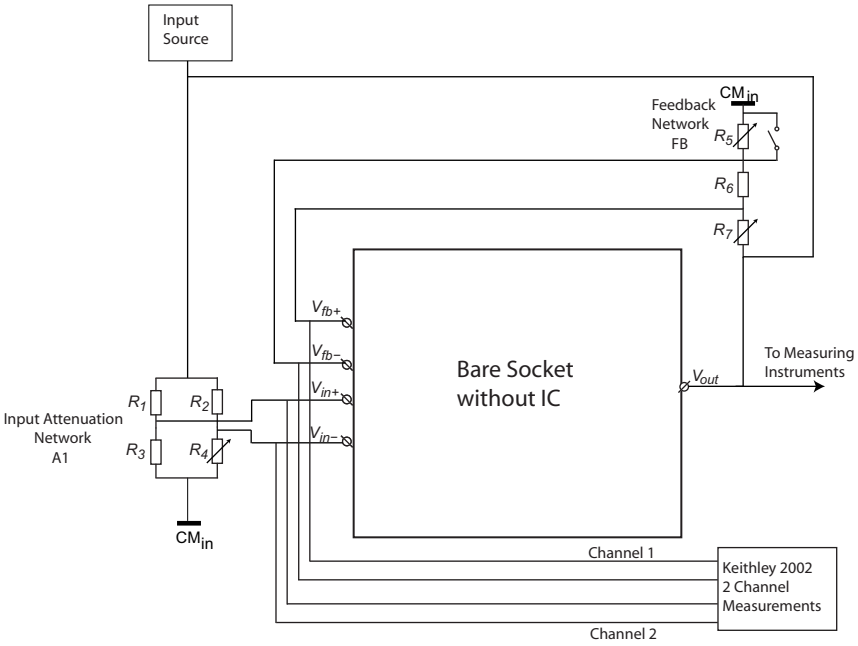

FIGURE 5.6: Setup to calibrate the resistive dividers on the PCB

The input source is swept across 100 data points and the voltages $V_{in+} - V_{in-}$ and $V_{fb} - V_{fb-}$ are measured using. Using MATLAB [] curve fitting this data is fitted to a 1st order polynomial ($y = m_{ideal}x + c$). The slope of this line (m_{ideal}) gives the value of $FB/A1$. For measuring the gain of the individual samples, the setup is shown in the Figure 5.7.

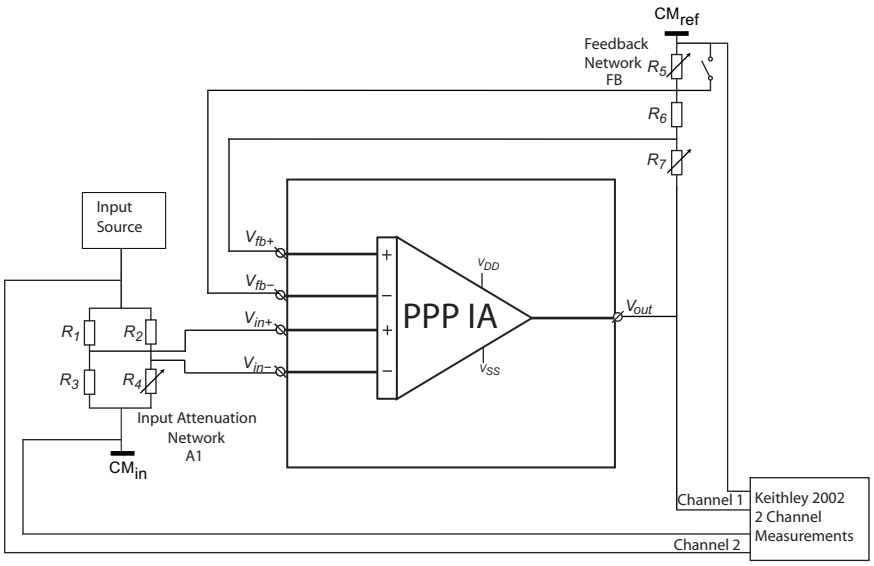

FIGURE 5.7: DC gain error measurement

The input voltage is swept such that the differential input to the amplifier ($V_{in+} - V_{in-}$) varies from $-50mV$ to $50mV$, and the input and output voltages are measured using the Keithley 2002 multi-meter. Using MATLAB curve fitting, this measured data is fit into a 1st order polynomial ($y = m_i x + c$). The slope this line (m_i) gives the transfer of the entire system (amplifier and the attenuation network). The difference between m_i and m_{ideal} gives the absolute gain error of the amplifier. In the following discussion about gain error measurements, the gain error measured is the absolute gain error determined by this method unless explicitly mentioned.

Before performing the gain error measurements, let us recall the reason for gain error in CFIA, as discussed in Section 4.2. This absolute gain error in CFIA has two components, i.e due to mismatch in transconductors and due to finite CMRR. These two error components are measured seperately in the measurements:

1. As mentioned in earlier chapters, DEM'ing improves the gain error caused due to mismatch of components. To evaluate the effect of DEM'ing the gain error of a sample was measured at $V_{CM,in} = V_{CM,ref} = 2.5V$, by switching on and off the DEM'ing. With the DEM'ing off, the measured gain error was 0.42%. When the DEM was turned on the measured gain error was 0.0008%. DEM'ing reduces the DC gain error by a factor of 52×. Theoretically the gain error after DEM'ing should be improved by $\Delta^2/2$ (Section 1.6), where Δ is the initial gain error. Hence the theoretical value of gain error after DEM'ing should be 0.0085%, which is same as the measured value. The gain error of 26 devices were measured with $V_{CM,in} = V_{CM,ref} = 2.5V$, Figure 5.8, shows the histogram for absolute gain

error in ppm. As seen from the Figure, 5.8 , the typical value of absolute gain error is 7ppm. This proves the effectiveness of DEM'ing for all the 26 devices.

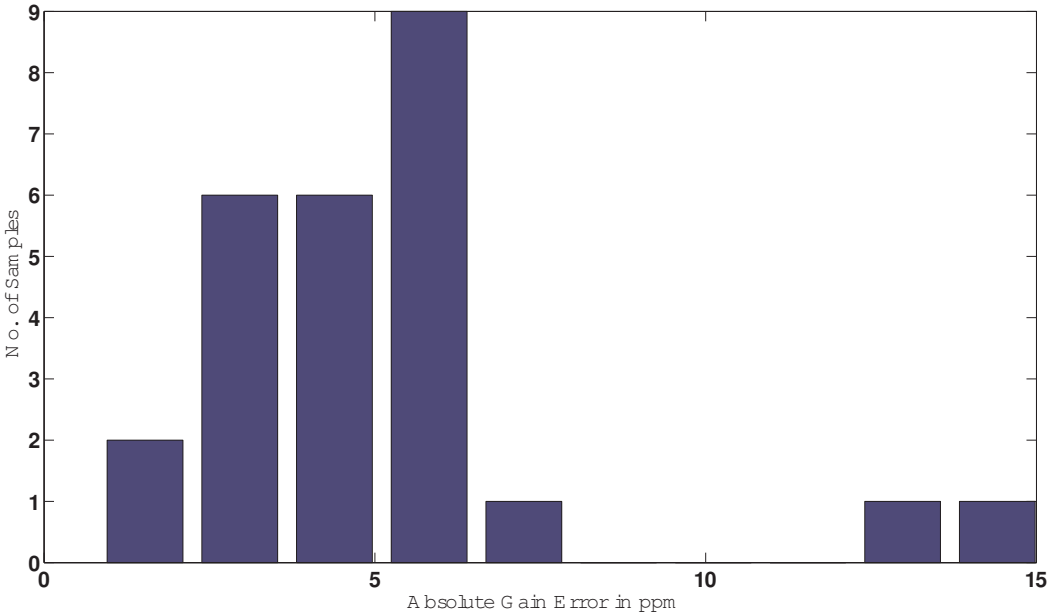

FIGURE 5.8: Histogram for gain error at same $V_{CM,in} = V_{CM,ref} = 2.5V$

2. As the finite CMRR dependence of gain error can be observer by varying the CM level.So to determine the gain error contribution due to finite CMRR of input stages, the gain error of test chips was measured at $V_{CM,in}$ of 1.0V, 0.6V and 0.0V with $V_{CM,ref}$ at 2.5V. Figures 5.9 , 5.10 and 5.11 show the histogram for absolute gain error in ppm for the measurements.

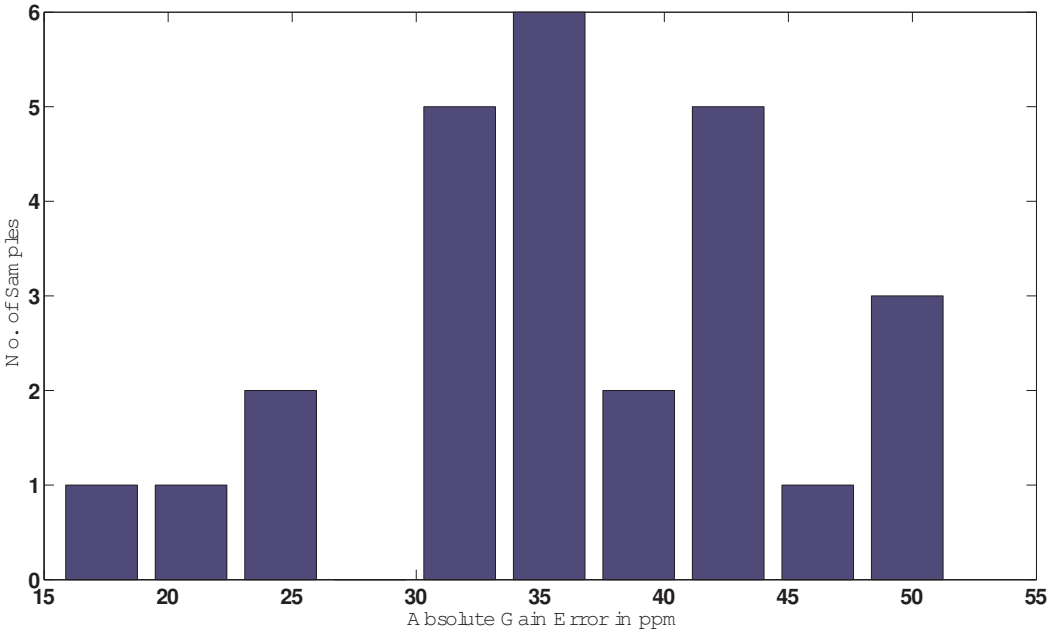

FIGURE 5.9: Histogram for gain error at same $V_{CM,in} = 1.0V and V_{CM,ref} = 2.5V$

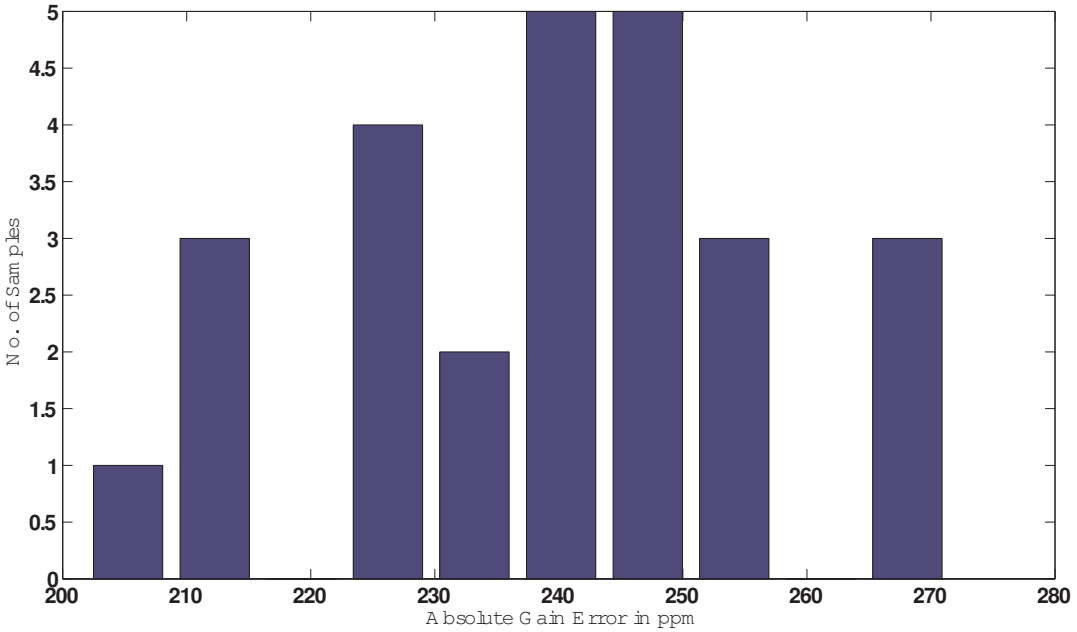

FIGURE 5.10: Histogram for gain error at same $V_{CM,in} = 0.6V and V_{CM,ref} = 2.5V$

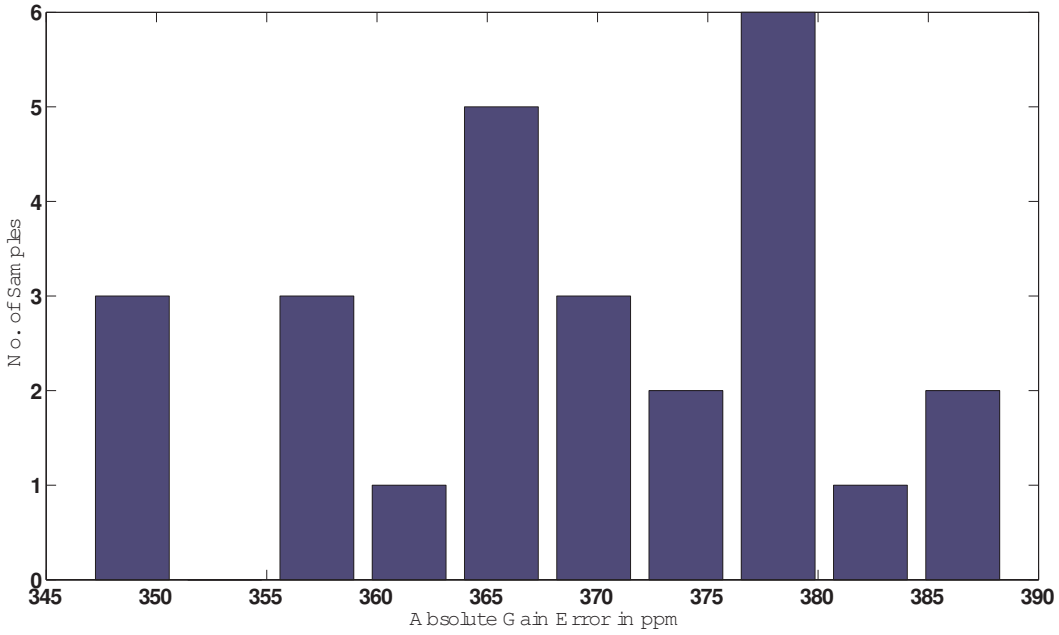

FIGURE 5.11: Histogram for gain error at same $V_{CM,in} = 0V and V_{CM,ref} = 2.5V$

The error increases as the input CM level approaches 0V. This shows the CM dependency of the input transconductance. As the input CM level approaches 0V, the output impedance of input transistors decreases, resulting in a CM dependent gain error. This error is maximum at input CM level of 0V. It can be inferred from the above graphs that over the input CMVR of 0-2.5V the absolute gain error is 0.038% (380ppm), which is better than the simulated value of 0.08% (post-layout). From the gain error measurements, we can infer that the gain error performance of the amplifier is dominated by the gain error due to finite CMRR of input stage.

From Figures 5.9 , 5.10 and 5.11 we can also see that the chip to chip spread in absolute gain error is under ± 0.003% (worst case). The spread in absolute gain error from chip to chip is referred to as relative gain error. The small spread in gain error from chip to chip is also attributed to DEM'ing. As DEM'ing reduces the gain error component arising from mismatch, the variation of gain error between chips is also reduced.

5.3 AC measurement results

Previous sction determines the DC parameters of the amplifier. This section is dedicated to the measurements of AC performance of the PPP IA. It presents two AC measurements i.e. noise and DEM ripple. As, the AC performance of the PPP IA is dependent on the value of auto-zeroing (f_{az}), chopping (f_{ch}) and DEM frequency (f_{DEM}) , let us first determine these values from the decided f_{ppp} of 22kHz. As per the discussions in chapter 3, these frequencies are related to each other by, $f_{ch} = f_{ppp}/2$ =11kHz , $f_{az} = f_{ppp}/3$ =7.33kHz and $f_{DEM} = f_{ppp}/6$ =3.66kHz.

Noise Measurements

To perform the noise measurement, the input of the amplifier was shorted and the amplifier was set to a gain of 1000. Figure 5.12 shows a plot of the output noise with auto-zeroing, and the two different plots show the effect of switching on and off the chopper. For low frequency, the input referred noise can be evalueted by dividing the output noise by 1000. With only auto-zeroing the input referred DC noise floor of the amplifier is $140nV/\sqrt{Hz}$, which is close to the simulated noise floor of $118nV/\sqrt{Hz}$(from PSS). As discussed in chapter 3, the notch due to auto-zeroing will be at $1.5 \cdot f_{az}$=11kHz, which can be seen in the measurement results. When the chooper is turned on, the input referred DC noise floor of the amplifier is $27nV/\sqrt{Hz}$, which also agrees very well with the simulated noise floor of $27nV/\sqrt{Hz}$.

DEM Ripple Measurements

As discussed in chapter 3, due to DEM'ing there will be a ripple in the output at the

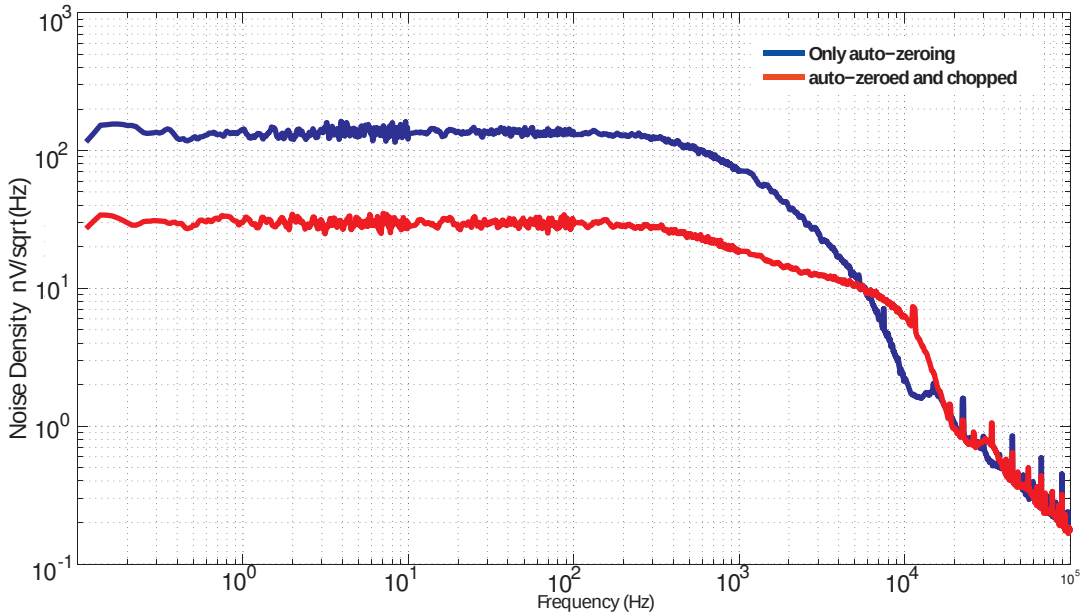

FIGURE 5.12: Output noise at a gain of 1000

DEM frequency. To measure the value of this ripple for a typical device, a differential input voltage of 50mV was applied to the test chip with gain setting of 50. Figure 5.13 shows the output ripple before and after trimming. As seen from the figure, the DEM ripple is at a frequency of 3.66kHz. After trimming the DEM ripple reduces by 18×. We can also see a ripple at a frequency of 7.4kHz, this is due to the residual offset of input transconductors being modulated by the PPP switching (section 3.7). The ripple is expected at 3.6kHz (i.e. the DEM frequency), but due to chopping this ripple is up-converted to 7.4kHz (11kHz-3.6kHz).

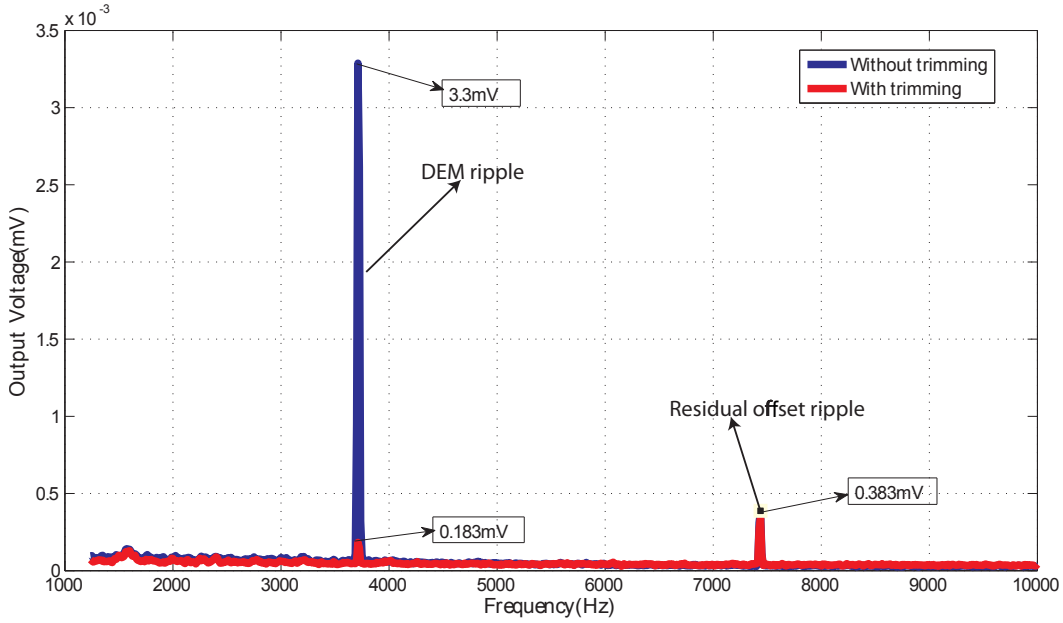

FIGURE 5.13: DEM ripple before and after trim(frequency domain)

5.4 Comparison of this work with the state of the art

Previous sections presents the measurement results of the PPP IA designed in this work. A general figure of merit for IA is the *Noise Efficiency Factor* (NEF). The NEF as evaluated from [17] for this amplifier is 24. This desin is compared to the state-of-the art CFIA in Table 5.1.

Parameters	This Work	Pertijs'09 [5]	Witte'08 [9]	Fan'10 [13]
CMOS Process	$0.5\mu m$	$0.5\mu m$	$0.8\mu m$	$0.7\mu m$
Input Offset Voltage	$4\mu V$	$3\mu V$	$5\mu V$	$2\mu V$
CMRR	$122dB$	$140dB$	$140dB$	$137dB$
Absolute Gain Accuracy	$\pm 0.038\%$	$\pm 0.1\%$	$\pm 0.1\%$	-
Relative Gain Accuracy	$\pm 0.003\%$	-	-	$\pm 0.53\%$
Input Voltage Noise	$27nV/\sqrt{Hz}$	$27nV/\sqrt{Hz}$	$142nV/\sqrt{Hz}$	$21nV/\sqrt{Hz}$
NEF [Willy Sansen]	24	43	143	10
GBW	$1MHz$	$800kHz$	$1MHz$	$1MHz$
Supply Current	$483\mu A$	$1700\mu A$	$850\mu A$	$143\mu A$
Supply Voltage	$3.3V$to$5.5V$	$3.0V$to$5.5V$	$2.8V$to$5.5V$	$5V$

TABLE 5.1: Comparison of this work with the state of the art

As seen from Table 5.1, the input offset voltage and DC noise floor of this amplifier is in line with the present state of the art. The absolute gain error is 2.5× smaller than the previous best reported value [5, 12]. However, when compared in terms of NEF, this implementation achieves a 1.8× and 6.8× better NEF than [5, 12]. The NEF of this amplifier is worse as compared to [13], but the gain error (relative) is 176× improved than [13].

Parameters	Target Specifications	Measurement Results
Input Offset Voltage	$< 5\mu V$	$4\mu V$
Gain Error ($V_{CM,in} = 2.5V, V_{CM,ref} = 2.5V$)	0	$15ppm$
Gain Error ($V_{CM,in} = 0V, V_{CM,ref} = 2.5V$)	$< 0.01\%$	0.038%
Input Voltage Noise	$\leq 27nV/\sqrt{Hz}$	$27nV/\sqrt{Hz}$
Current	As low as possible	$483\mu A$
GBW	$1MHz$	$1MHz$

TABLE 5.2: Comparison of target specifications and measurement results

Table 5.2 shows a comparison between the target specifications and the measurement results on the amplifier. As seen from the table, apart from gain error specifications the designed Ping-Pong-Pang IA achieves all the target specifications.

5.5 Conclusions and future Work

This thesis has presented the design, implementation and measurements of the first silicon implementation of a Ping-Pong-Pang Instrumentation amplifier. This design advances the state of the art in precision instrumentation amplifiers by achieving a 2.5× improvement in gain error compared to the state-of-the art.

In CFIAs, mismatch between the input and feedback transconductors, due to component mismatch and their finite CMRR, results in a gain error. In previous implementations, this was minimized by the use of resistively degenerated transconductors with local feedback [5, 12] and, if necessary, by trimming the degeneration resistors. However, this comes at the expense of increased power consumption. In this work, very low gain error is achieved by applying DEM to power-efficient non-degenerated transconductors.

In previous CFIAs employing auto-zeroing [5], $g_{m,in}$ and $g_{m,fb}$ were auto-zeroed together in a ping-pong fashion to obtain a continuous output signal. This requires a total of four transconductors, two of which are in the signal path while the other two are auto-zeroed. In the PPP CFIA, however, each transconductor is individually auto-zeroed, so that only three transconductors are needed to achieve a continuous output signal. Given that the transconductors dominate the CFIA's power consumption, this results in a significant improvement in power efficiency.

A Combination of power efficient circuits and topology, along with DEM'ing, PPP CFIA achieves better noise efficiency factor and lower gain error than previously implemented auto-zeroed CFIA [5].

The ripple due to DEM'ing was trimmed in this design using a on chip DAC. This requires an extra trim step and might not track over temperature (though not verified till now). The cause of DEM ripple is the mismatch between the input transconductors, If the mismatch can be removed with dynamic calibration, as suggested in section 1.6.3, this would lead to reduction of the extra trim costs and make this design more attractive for industrial production. Investigating and on-chip implementation of such dynamic gain error calibration technique can be a very interesting future direction for this work.

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