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Minimum Switching Losses Discontinuous PWM Strategy for Bidirectional Single-Phase AC–DC Converter With Active Power Decoupling Circuit

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***Abstract*—Active power decoupling circuits are used in bidirectional single-phase grid-connected systems to enhance the circuit lifetime by creating an alternative path for the typical dc-side power pulsating ripple. Therefore, this reduces the requirement of smoothing dc capacitors allowing compact designs even with the implementation of long life metalized film technology. However, with the necessary addition of auxiliary components, extra power losses in the added switching devices and passive components will be introduced, which will inevitably reduce the system power conversion efficiency. To relieve this issue, a new discontinuous pulsewidth modulation (PWM) strategy with minimum switching losses is proposed in this article. This method detects the converter current and reference voltages synchronously to determine the optimum clamped duration of each circuit phase-leg. With such a characteristic, the proposed strategy can realize the minimum switching losses at any instant, thus improving the power conversion efficiency and potentially the power density of the converter. The proposed modulation method is described, analyzed, validated, and compared with different PWM methods on a 2-kVA bidirectional single-phase ac–dc converter with active power decoupling circuit.**

***Index Terms*—AC–DC converter, active power decoupling, discontinuous pulsewidth modulation (DPWM), single phase, switching losses.**

I. Introduction

FULL-BRIDGE based single-phase ac–dc voltage source converters have been widely used in industrial applications, such as grid connected inverters [1], pulsewidth modulation (PWM) rectifiers [2], and static synchronous compensators (STATCOM) [3]. Unfortunately, the inherent ripple power in the converter results in an undesirable low-frequency ripple on the dc-link, which can degrade the system performance in terms of ac current distortion, and reliability [4]–[6]. To address this significant issue, the most widely used approach is to apply large energy storage devices, i.e., bulky electrolytic capacitors, on the dc side to passively smoothen up the power oscillation, which will result in bulky size of the converter and reduced lifetime of the system [7]–[10]. In order to reduce the requirement of dc capacitor bank, a great deal of researches have been conducted on active power decoupling techniques. This offers an alternative path for the ripple power to flow through by using extra energy-storage components such as capacitors or inductors and auxiliary power switches, so that it enables a considerable reduction on the requirement of smoothing capacitors on the dc-link and improve the power density remarkably [11]–[26]. Consequently, this concept has attracted considerable attentions from both industry and academia in recent years.

The active power decoupling methods can be mainly divided into two categories: 1) dc-type [12]–[14], [16], [17] and 2) ac-type [18]–[26]. The former has a unipolar voltage in the decoupling capacitor, while the latter has a bipolar one. DC-type decoupling methods consist of a buck-type circuit [see Fig. 1(a)] [12], [13], a buck–boost type circuit [see Fig. 1(b)] [14], [15], or a boost-type topology [see Fig. 1(c)] [16], [17]. AC-type decoupling methods include flying capacitors circuits [see Fig. 1(d) and (e)] [18], [19], full-bridge converter [see Fig. 1(f)] [21], [22], and half-bridge topology [see Fig. 1(g)] [21]–[26].

Due to the lower requirement for switching control bandwidth, reduced components, and less current and voltage stress on the additional decoupling capacitors and power switches [7], [21], the study of ac-type half-bridge-based active power decoupling method with the decoupling capacitor connected between the extra half-bridge and another one of the single-phase full-bridge converter [see Fig. 1(g)] and its corresponding modulation strategies have gain momentum [21]–[26]. By using the space vector pulse width modulation (SVPWM) strategy in the ac-type decoupling method, the dc voltage utilization can be maximized, and more ripple power can be decoupled [22]. In [23], the performance of an ac-type decoupling method is further analyzed including the effect of grid filter inductance with all grid power factors. Via a trivial modification from the topology in [22], a SPWM-based modulation method developed in [24]

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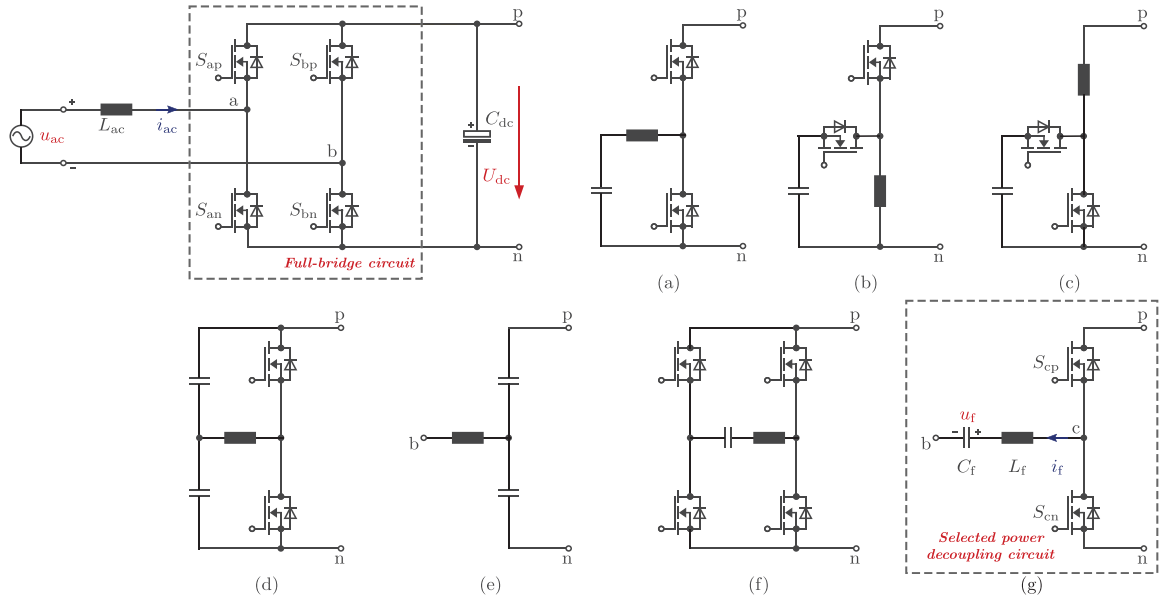

Fig. 1. Full-bridge based single-phase ac–dc voltage source converters with (a) dc buck type [12], [13], (b) dc buck–boost type [14], [15], (c) dc boost type [16], [17], (d) and (e) ac flying capacitors type [18], [19], (f) ac full-bridge type[20], (g) ac half-bridge type [22] power decoupling circuit.

can involve an extra zero-sequence voltage injection derived from the converter voltage reference without introducing higher order harmonic distortions. To handle the model uncertainty and thereby improve the steady-state performance, a novel closed-loop control scheme of the ac power compensation is studied in [25]. A direct instantaneous ripple power predictive control is proposed in [26], which can be implemented into ac-type active power decoupling circuit converters to achieve instantaneous ripple power control, and to improve the dynamic performances. However, as for all other single-phase ac–dc converters with active power decoupling technique, with the auxiliary power decoupling circuit added in the common full-bridge circuit, extra power losses on the added switching devices, and passive components will be introduced, which will reduce the system power conversion efficiency inevitably.

To relieve this shortcoming, this article proposes a new discontinuous PWM (DPWM) strategy with minimum switching losses for bidirectional single-phase ac–dc converters associated with the ac-type half-bridge active power decoupling circuit shown in Fig. 2(a). Herein, the proposed control algorithm is able to detect the current measurements and the converter voltage references, and it determines instantaneously the optimal clamped duration on each phase. With such a characteristic, the proposed strategy can realize the minimum switching losses action at any instant, thus improving the power efficiency and density, which is superior to conditional DPWM methods available in the literature, e.g., the ones used in symmetric three-phase three-wire applications [27]–[31]. Since the current and voltage measurements are also necessary for other ac-type half-bride based active power decoupling methods [21]–[26], the proposed DPWM strategy will not increase any component cost of the system.

It is noted that all of the aforementioned modulation strategies in single-phase ac–dc converters with active power decoupling circuits are using continuous PWM methods, e.g., SVPWM and

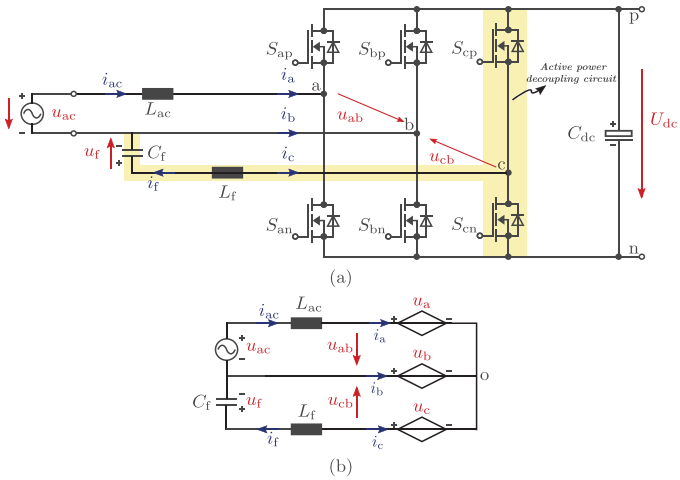

Fig. 2. Studied topology circuit and its corresponding equivalent circuit, (a) topology circuit, (b) equivalent circuit.

SPWM. To the best of the authors' knowledge, so far there is a lack of work in the literature, which applies any DPWM method into the single-phase ac–dc converter with active power decoupling circuit. Moreover, the reference voltages seen by each bridge leg of the system are naturally unbalanced and asymmetrical, and the peak value of the ac current is particularly difficult to predict, which is mainly different from traditional DPWM methods widely studied in balanced and symmetric three-phase three-wire applications, such as motor drives and grid-tied converters [27]–[31]. Note that the proof of functionality and adaptation of existing DPWM techniques to the studied circuit depicted in Fig. 2(a) is also a contribution of this article.

The rest of this article is divided as follows. In Section II, the analytical model and a general control method for the ac-type

single-phase active power decoupling converter are developed to achieve different power factor and ripple power compensation. In Section III, the detailed implementation of the proposed DPWM strategy is illustrated. In Section IV, characteristics in terms of switching losses and current distortion are investigated mathematically and compared with the SVPWM method proposed in [22] and the known DPWM methods proposed for three-phase three-wire balanced systems [27]. In Section V, the key parameters of storage capacitance and controllers are designed. Finally, in Section VI, the proposed PWM strategy is evaluated and benchmarked against different PWM methods in both simulation and a 2 kVA, 400 V, bidirectional single-phase ac–dc converter with active power decoupling circuit operating as inverter, rectifier, and STATCOM.

II. Power Analysis and Control Strategy

The full-bridge based single-phase ac–dc voltage source converter with ac-type half-bridge decoupling circuit discussed in this article is given in Fig. 2(a). Herein, $u_{\rm ac}$ and $i_{\rm ac}$ are the grid voltage and current, respectively; $u_{\rm f}$ and $i_{\rm f}$ are the voltage and current for the decoupling storage capacitor, respectively; $U_{\rm dc}$ is the dc voltage; $L_{\rm ac}$ is the grid side filter inductor; and $C_{\rm f}$ and $L_{\rm f}$ are the internal storage capacitor and filter inductor for the active power decoupling circuit, respectively. The topology shown in Fig. 2(a) can be regarded as a three-phase unbalanced system. The equivalent circuit for Fig. 2(a) with three-phase legs voltages ($u_{\rm a}$, $u_{\rm b}$, and $u_{\rm c}$) and three-phase current ($i_{\rm a}$, $i_{\rm b}$, and $i_{\rm c}$) is given in Fig. 2(b).

A. Power Analysis

The grid voltage $u_{\rm ac}$ and current $i_{\rm ac}$ with the angular frequency ω are expressed as follows:

$$u_{\rm ac} = U_{\rm ac}\sin(\omega t) \tag{1}$$

$$i_{\rm ac} = I_{\rm ac}\sin(\omega t + \varphi) \tag{2}$$

and the voltage and current of the storage capacitor in the decoupling circuit are

$$u_{\rm f} = U_{\rm f}\sin(\omega t + \theta) \tag{3}$$

$$i_{\rm f} = I_{\rm f}\cos(\omega t + \theta) = \omega C_{\rm f} U_{\rm f}\cos(\omega t + \theta) \tag{4}$$

where $U_{\rm ac}$ and $I_{\rm ac}$ are the peak value of the grid voltage and current, respectively, while $U_{\rm f}$ and $I_{\rm f}$ are the peak value of the storage capacitor voltage and current, respectively. φ is the phase angle between $u_{\rm ac}$ and $i_{\rm ac}$, and θ is the phase angle between $u_{\rm ac}$ and $u_{\rm f}$.

Thereafter, the instantaneous power coming into the converter can be expressed as

$$p_{\rm ab} = u_{\rm ac}i_{\rm ac} - L_{\rm ac}\frac{{\rm d}i_{\rm ac}}{{\rm d}t}i_{\rm ac} = \frac{1}{2}U_{\rm ac}I_{\rm ac}\cos(\varphi) + p_{2\omega} \tag{5}$$

where $p_{2\omega}$ is the power ripple component

$$p_{2\omega} = -\frac{1}{2}U_{\rm ac}I_{\rm ac}\sin\left(2\omega t + \varphi - \frac{\pi}{2}\right) - \frac{1}{2}\omega L_{\rm ac}I_{\rm ac}^2\sin(2\omega t + 2\varphi). \tag{6}$$

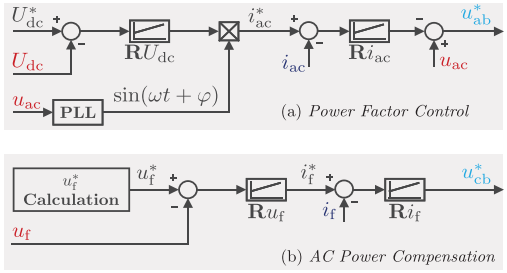

Fig. 3. Basic control structure of the system with (a) power factor control, and (b) ac power compensation.

Similarly, the instantaneous power of the power decoupling circuit is

$$p_{\rm cb} = u_{\rm f}i_{\rm f} + L_{\rm f}\frac{{\rm d}i_{\rm f}}{{\rm d}t}i_{\rm f} = \frac{1}{2}\omega^2 C_{\rm f}^2 U_{\rm f}^2\left(\frac{1}{\omega C_{\rm f}} - \omega L_{\rm f}\right)\sin(2\omega t + 2\theta). \tag{7}$$

B. Control Structure

The basic control structure is designed to realize two control functions [22], as given in Fig. 3. The first function aims to control the averaged dc-link voltage and to achieve different power factor at the ac port, while the second control function is dedicated to ac power compensation, which aims to absorb the 2ω power ripple on the dc-side and to minimizes the dc-link voltage ripple.

By tight regulation shown in Fig. 3, the power stored in the power decoupling circuit $p_{\rm cb}$ should be controlled to be equal to the ripple power coming into the converter $p_{2\omega}$. The ripple power $p_{2\omega}$ can be further derived as

$$\begin{aligned} p_{2\omega} &= \frac{1}{2}U_{\rm ac}I_{\rm ac}[\sin(2\omega t)\cos(\varphi - \tfrac{\pi}{2}) - \cos(2\omega t)\sin(\varphi - \tfrac{\pi}{2})] \\ &\quad - \frac{1}{2}\omega L_{\rm ac}I_{\rm ac}^2[\sin(2\omega t)\cos(2\varphi) - \cos(2\omega t)\sin(2\varphi)] \\ &= \frac{1}{2}[U_{\rm ac}I_{\rm ac}\sin(\varphi) - \omega L_{\rm ac}I_{\rm ac}^2\cos(2\varphi)]\sin(2\omega t) \\ &\quad - \frac{1}{2}[U_{\rm ac}I_{\rm ac}\cos(\varphi) + \omega L_{\rm ac}I_{\rm ac}^2\sin(2\varphi)]\cos(2\omega t) \\ &= \frac{1}{2}P_{\rm ab\_2\omega}\sin(2\omega t + \varphi_{\rm ab\_2\omega}) \end{aligned} \tag{8}$$

where

$$P_{\rm ab\_2\omega} = \sqrt{(U_{\rm ac}I_{\rm ac})^2 + (\omega L_{\rm ac}I_{\rm ac}^2)^2 + 2\omega L_{\rm ac}U_{\rm ac}I_{\rm ac}^3\sin\varphi} \tag{9}$$

$$\varphi_{\rm ab\_2\omega} = \arctan\frac{-U_{\rm ac}I_{\rm ac}\cos\varphi - \omega L_{\rm ac}I_{\rm ac}^2\sin(2\varphi)}{U_{\rm ac}I_{\rm ac}\sin\varphi - \omega L_{\rm ac}I_{\rm ac}^2\cos(2\varphi)}. \tag{10}$$

Therefore, based on (7)–(10), the magnitude and phase angle of the reference voltage of the storage capacitor [$u_{\rm f}^* = U_{\rm f}^*$

$\sin(\omega t + \theta^*)]$ should be

$$U_{\rm f}^* = \sqrt{\frac{P_{\rm ab\_2\omega}}{\omega C_{\rm f} - \omega^3 C_{\rm f}^2 L_{\rm f}}} \tag{11}$$

$$\theta^* = \frac{1}{2}\varphi_{\rm ab\_2\omega}. \tag{12}$$

III. Description of the Proposed Method

After obtaining the converter line-to-line reference voltages u_{ab}^* from the power factor control in Fig. 3(a) and u_{cb}^* from ac power compensation in Fig. 3(b), the converter reference voltages ($u_{\rm a}^*$, $u_{\rm b}^*$, and $u_{\rm c}^*$) can be decided by

$$\begin{cases} u_{\rm a}^* = u_{\rm a}^+ + u_{\rm a}^- = \frac{2u_{ab}^* - u_{cb}^*}{3} \\ u_{\rm b}^* = u_{\rm b}^+ + u_{\rm b}^- = \frac{-u_{ab}^* - u_{cb}^*}{3} \\ u_{\rm c}^* = u_{\rm c}^+ + u_{\rm c}^- = \frac{-u_{ab}^* + 2u_{cb}^*}{3} \end{cases} \tag{13}$$

where u_x^+ and u_x^- ($x \in \{a, b, c\}$) are the positive and negative components of each converter reference voltage. Due to the fact the system studied in this article is equivalent to a three-phase three-wire voltage source circuit, i.e., without a low impedance path for the zero-sequence components, the relation of $u_{\rm a}^* + u_{\rm b}^* + u_{\rm c}^* = 0$ in (13) is still valid.

Different from the traditional DPWM methods in [27], the proposed PWM modulator depends not only on the converter reference voltages, but also on the measured phase currents ($i_{\rm a}$, $i_{\rm b}$, and $i_{\rm c}$) passing through the converter (see Fig. 2)

$$\begin{cases} i_{\rm a} = i_{\rm ac} \\ i_{\rm c} = -i_{\rm f} \\ i_{\rm b} = -i_{\rm ac} + i_{\rm f}. \end{cases} \tag{14}$$

The converter reference voltages and measured currents work together to decide the placement of the clamped region, where the bridge-leg stop switching. The zero-sequence signal of the modulation waveform of the proposed method can be determined by

$$u_0 = \text{sign}(u_i^*) \cdot U_{\rm dc}/2 - u_i^* \qquad i \in \{a, b, c\} \tag{15}$$

where u_i^* is the selected phase reference voltage to be clamped. The selection principle of u_i^* is performed at each control period, which is illustrated in Fig. 4. If the magnitude of the phase reference voltage with maximum phase current magnitude ($u_{\rm n}^*$) is not lower than the other two phases, this reference voltage is selected as u_i^*. Otherwise, one of the other phase reference voltages with larger current magnitude is used.

Finally, the modulation waveforms $u_{\rm a}^{**}$, $u_{\rm b}^{**}$, and $u_{\rm c}^{**}$ of the proposed PWM method are obtained to compare with the modulating triangular carriers

$$u_x^{**} = u_x^* + u_0 \qquad x \in \{a, b, c\}. \tag{16}$$

Fig. 5 shows the simplified illustration of the proposed PWM method in the active power decoupling converter operating with different φ in rectifier and inverter mode, which assumes $U_{\rm ab} = U_{\rm cb} = 1.6\, U_{\rm dc}/2$ and $I_{\rm ac} = I_{\rm f}$. If only the voltage references are used to choose the clamping region [27], i.e., without the information of the converter current, the obtained DPWM can not achieve the performance of minimum switching losses, because the clamped switches are not always matched with the phase-leg with the maximum current [29], [31]. By using only the measured currents [29], the minimum magnitude of the phase reference voltage with maximum phase current magnitude can be selected, which will cause the problem of overmodulation in other phase and influence the waveform quality. It is indicated that not only the reference voltages, but also the measured converter currents are important to determine the optimal clamped intervals. As depicted in the gray area illustrated in Fig. 5, although $|i_{\rm a}| < |i_{\rm c}|$, phase a is chosen to be clamped because $|u_{\rm c}^*| = \min\{|u_{\rm a}^*|, |u_{\rm b}^*|, |u_{\rm c}^*|\}$ and $|i_{\rm a}| > |i_{\rm b}|$. Therefore, the clamped interval of the proposed method for each phase is always around the highest value of the converter current whose corresponding reference voltage is allowed to be clamped. This will lead to an optimal reduction of the switching losses.

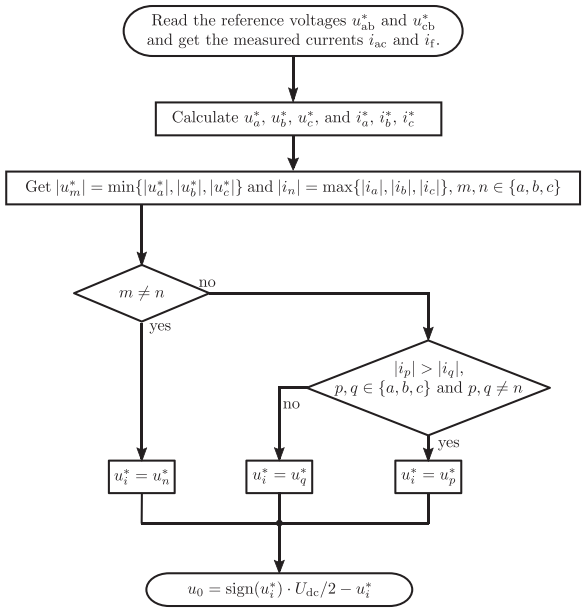

Fig. 4. Flowchart of the proposed PWM strategy to decide the zero-sequence signal u_0 of the modulation waveform.

IV. Performance Comparison

The analytical models of the modulator performance in terms of switching losses and current distortion for the proposed PWM method, SVPWM and other DPWM methods are discussed in this section. Traditional DPWM methods, e.g., DPWMMAX, DPWMMIN, DPWM1, and DPWM3 [27], which are easily implemented into the single-phase converter with active power decoupling circuit without introducing extra computation on the reference voltages phase shifting, are selected to compare with SVPWM and the proposed PWM method. The reference signal with the maximum value defines the clamped phase reference voltage u_i^* for DPWMMAX, while that with minimum value defines the u_i^* for DPWMMIN. The reference signal with the maximum magnitude defines the u_i^* for DPWM1, and that with the intermediate magnitude defines the u_i^* for DPWM3 [27]. To

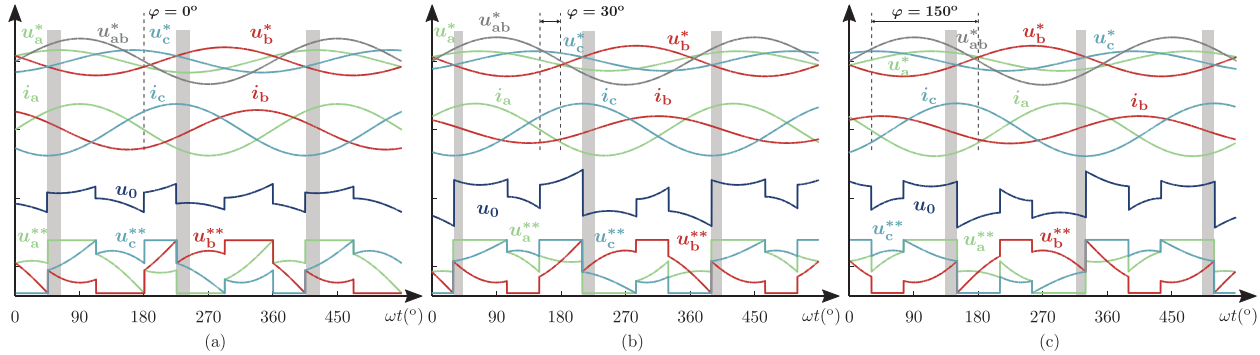

Fig. 5. Simplified illustration of the proposed PWM method at (a) rectifier mode $\varphi = 0°$, (b) rectifier mode $\varphi = 30°$, and (c) inverter mode $\varphi = 150°$ assuming $U_{ab} = U_{cb} = 1.6\,U_{dc}/2$ and $I_{ac} = I_f$.

simplify the theoretical analysis, the voltage and power losses on the filter inductors L_{ac} and L_f are neglected. Thus, according to $p_{2\omega} = p_{cb}$, the relation of $\theta = \frac{1}{2}(\varphi - \frac{\pi}{2})$ is satisfied. Only the condition $0 \le \varphi \le 180°$ is presented, which is within the range of that the active power decoupling circuit can work effectively [22] and includes most of the operating cases in practice.

A. Switching Losses

For the theoretical calculation of the switching losses, assume that $U_{ac} = U_f$ and $I_{ac} = I_f = I_m$ and the converter phase currents (i_a, i_b, and i_c) can be expressed as

$$\begin{cases} i_a = I_m \sin(\omega t + \varphi) \\ i_c = -I_m \cos(\omega t + \theta) \\ i_b = -I_m \sin(\omega t + \varphi) + I_m \cos(\omega t + \theta) \\ \quad = 2I_m \sin(\frac{\theta}{2}) \sin(\omega t + \frac{3\theta}{2}). \end{cases} \tag{17}$$

After that, the average switching power loss for the device in phase x ($x \in \{a, b, c\}$) over a fundamental period can be defined as

$$P_{sw\_x} = \frac{U_{dc}}{2\pi U_b} f_s E_{on,off,rr} \int_0^{2\pi} f_x(\omega t)\, d\omega t \tag{18}$$

where $E_{on,off,rr}$ represents a lumped switching losses per commutation for a specified dc voltage and output current; U_b is the data-sheet reference voltage; f_s represents the constant switching frequency of the devices; and $f_x(\omega t)$ equals zero in the intervals where no switching occurs and equals to the absolute value of the corresponding phase current $|i_x(\omega t)|$ otherwise.

Normalizing the total switching losses P_{sw} to P_0, the switching loss function (SLF) of different modulators for the equivalent three-phase unbalanced system studied in this article can be found

$$P_0 = \frac{4U_{dc}I_m}{\pi U_b} f_s E_{on,off,rr} \tag{19}$$

$$\mathrm{SLF} = \frac{P_{sw}}{P_0} = \frac{P_{sw\_a} + P_{sw\_b} + P_{sw\_c}}{P_0}. \tag{20}$$

Fig. 6 shows the φ and θ dependent switching current waveform (f_a, f_b, and f_c) of the proposed PWM method. Applying (18) to (20), the SLF of the SVPWM and the proposed PWM

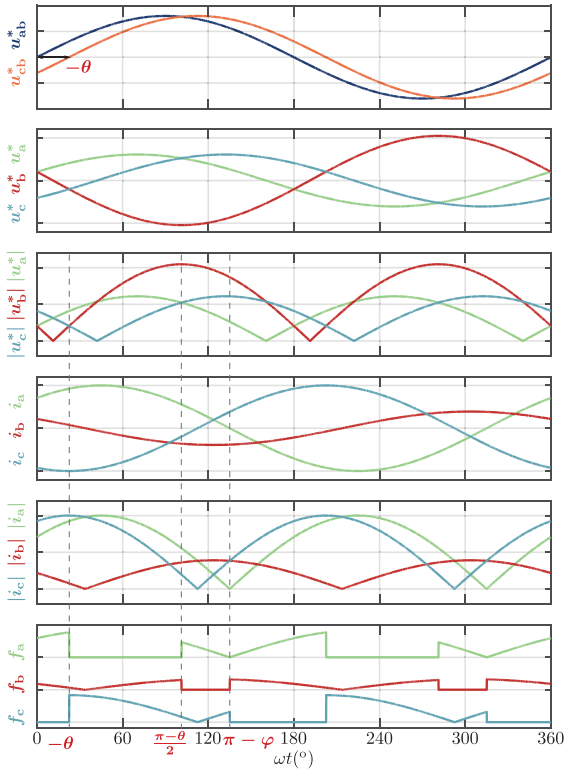

Fig. 6. Diagram of the switching model of the proposed method at $\varphi = 45°$.

method can be derived as

$$\mathrm{SLF}_{SV} = \begin{cases} 1 - \sin(\frac{\varphi}{4} - \frac{\pi}{8}) & 0 \le \varphi < \frac{\pi}{2} \\ 1 + \sin(\frac{\varphi}{4} - \frac{\pi}{8}) & \frac{\pi}{2} \le \varphi \le \pi \end{cases} \tag{21}$$

$$\mathrm{SLF}_{Pro} = \begin{cases} \sin\left(\frac{\pi}{8} - \frac{\varphi}{4}\right) - \frac{1}{4}\cos\left(\frac{\varphi}{2} + \frac{\pi}{4}\right) \\ -\frac{1}{4}\cos\left(\frac{\pi}{8} - \frac{\varphi}{4}\right) + \frac{3}{4} \quad 0 \le \varphi < \frac{\pi}{2} \\ \sin\left(\frac{\varphi}{4} - \frac{\pi}{8}\right) + \frac{1}{4}\cos\left(\frac{\varphi}{2} + \frac{\pi}{4}\right) \\ -\frac{1}{4}\cos\left(\frac{\pi}{8} - \frac{\varphi}{4}\right) + \frac{3}{4} \quad \frac{\pi}{2} \le \varphi \le \pi. \end{cases} \tag{22}$$

The SLF for other DPWM methods can also be achieved via (18) to (20). Due to the complexity of the expression, the calculations of other DPWM methods are carried out numerically and

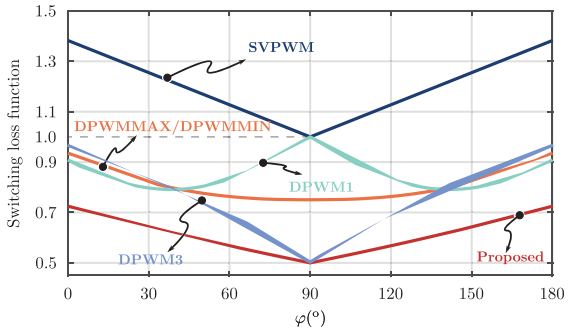

Fig. 7. SLF of the proposed and various PWM methods. Note that a smaller SLF leads to lower switching losses.

compared with that of SVPWM and the proposed PWM method. The comparison of SLF for different PWM methods is shown in Fig. 7. The application of DPWM methods can considerably reduce the switching losses, i.e., the proposed PWM method is able to reduce 50% of the losses found in the SVPWM. As Fig. 7 indicates, the proposed method can achieve the minimum switching losses action over the whole φ range, which will lead to a simplified thermal management with low cost, improved power conversion efficiency, and higher power density of the converter.

B. Current Ripple

The winding and core losses of the filter inductor are depending on the current ripple. Therefore, the rms value of the output current ripple determined by the selected modulator gives an indication about the magnetic losses. To demonstrate the performance of the current ripple, the mathematical formulation can be derived from the terminal pulse voltage and current waveforms shown in Fig. 8. The time intervals $t_1 - t_4$ can be obtained from the PWM period T_s and modulation waveforms u_{a}^{**}, u_{b}^{**}, and u_{c}^{**}. For example, t_1 and t_2 in Fig. 8(a) are

$$t_1 = \frac{2u_{\mathrm{a}}^{**}/U_{\mathrm{dc}} + 1}{2} T_s \tag{23}$$

$$t_2 = \frac{2u_{\mathrm{b}}^{**}/U_{\mathrm{dc}} + 1}{2} T_s. \tag{24}$$

Then, the squared rms value of the current ripple of i_{ac} and i_{f} can be expressed as

$$\Delta I_{\mathrm{ac,rms}}^2 = \frac{1}{2\pi} \int_0^{2\pi} \left(\frac{1}{T_s} \int_0^{T_s} \Delta i_{\mathrm{ac}}^2 \mathrm{d}\tau \right) \mathrm{d}\omega t \tag{25}$$

$$\Delta I_{\mathrm{f,rms}}^2 = \frac{1}{2\pi} \int_0^{2\pi} \left(\frac{1}{T_s} \int_0^{T_s} \Delta i_{\mathrm{f}}^2 \mathrm{d}\tau \right) \mathrm{d}\omega t \tag{26}$$

where the deviations of Δi_{ac} and Δi_{f} are

$$\Delta i_{\mathrm{ac}} = i_{\mathrm{ac}} - i_{\mathrm{ac,avg}} = \frac{1}{L_{\mathrm{ac}}} \int (u_{\mathrm{ac}} - u_{\mathrm{ab}})\, \mathrm{d}t \tag{27}$$

$$\Delta i_{\mathrm{f}} = i_{\mathrm{f}} - i_{\mathrm{f,avg}} = \frac{1}{L_{\mathrm{f}}} \int (u_{\mathrm{cb}} - u_{\mathrm{f}})\, \mathrm{d}t. \tag{28}$$

For equivalence with the three-phase voltage source converter one assumes that the modulation index is given by $M = U_{\mathrm{ac}}/(U_{\mathrm{dc}}/2) = U_{\mathrm{f}}/(U_{\mathrm{dc}}/2)$ $(0 \le M \le 2)$. By normalizing the squared rms value of the current ripple $\Delta I_{\mathrm{ac,rms}}^2$ and $\Delta I_{\mathrm{f,rms}}^2$ to ΔI_0^2 in (29), the M-φ-dependent current ripple function (CRF) can be calculated

$$\Delta I_0^2 = \frac{T_s^2 U_{\mathrm{dc}}^2}{2\pi L^2}. \tag{29}$$

The CRF of the proposed method is calculated numerically and plotted in Fig. 9. The CRF of the proposed method first increases at low M range and then decreases at high M range. The CRF characteristics of the proposed and other PWM at $M = 1.6$ are compared in Fig. 10. It is evidently observed that with the same switching frequency, except for the proposed method, the difference of CRF performance for i_{ac} and i_{f} with other DPWM methods is inconspicuous. The performance of the proposed PWM is similar to the other DPWM methods, and that of SVPWM is better than all studied DPWM methods. However, as predicted in Fig. 7, the proposed PWM method is able to reduce 50% of the switching losses in comparison to the SVPWM, which means the switching frequency of the proposed PWM strategy can be doubled under the same switching losses as the SVPWM. As a result, the CRF of the proposed PWM method can reduce four times, and becomes lower than that of SVPWM, as seen in Fig. 10. Furthermore, in practice, with high switching frequency, the difference between current harmonic between SVPWM and DPWM methods will be very small and the problem of switching losses will be prominent. Therefore, although the performance of CRF is inferior to the SVPWM under the same switching frequency, the proposed PWM method is still promising if the converter is operating at a high switching frequency, which will bring about a smaller size and cost of the passive filter with the same current ripple value.

TABLE I
KEY SPECIFICATIONS OF THE SINGLE-PHASE CONVERTER

Variables	Parameters	Value
U_{ac}	Grid voltage	220 $\mathrm{V_{rms}}$
ω	Grid angular frequency	$2\pi \times 50$ rad/s
L_{ac}	Grid inductance	1.44 mH
L_{f}	Storage filter inductance	0.72 mH
U_{dc}	DC voltage	400 V
C_{dc}	DC-link capacitance	135 μF
f_s	Switching frequency	40 kHz
S	Total power	2 kVA

V. KEY PARAMETERS DESIGN

A. Storage Capacitance Design

The main parameters of the bidirectional single-phase ac–dc converter with active power decoupling circuit are shown in Table I. According to (11), the storage capacitance C_{f} can be derived from

$$C_{\mathrm{f}} = \frac{\omega - \sqrt{\omega^2 - 4\omega^3 L_{\mathrm{f}} P_{\mathrm{ab\_2\omega}}/U_{\mathrm{f}}^2}}{2\omega^3 L_{\mathrm{f}}}. \tag{30}$$

The minimum storage capacitance should be designed at the maximum power point. For a given power, a larger U_{f} leads to a smaller capacitance. According to the full-bridge modulation,

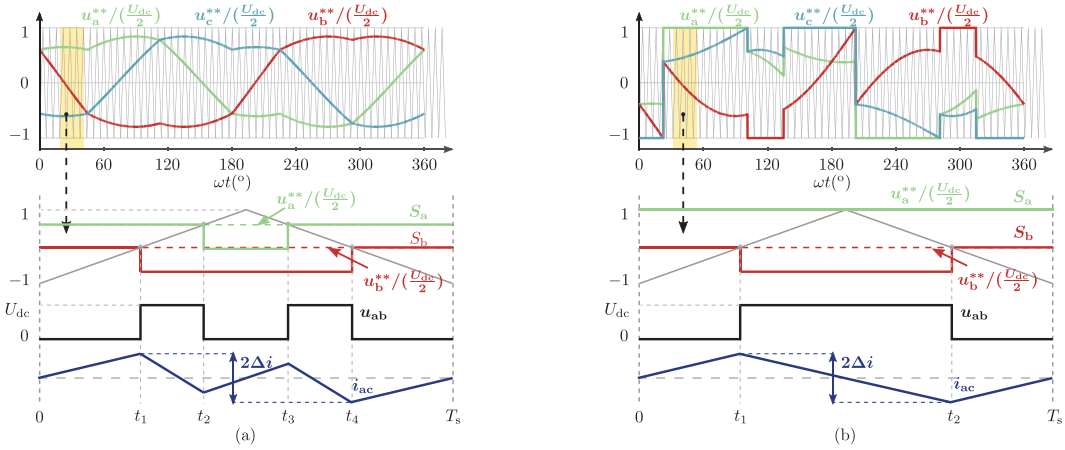

Fig. 8. Illustration of the switching sequence and current ripple of i_a in a carrier cycle period. (a) SVPWM at $\varphi = 0°$. (b) Proposed PWM at $\varphi = 45°$.

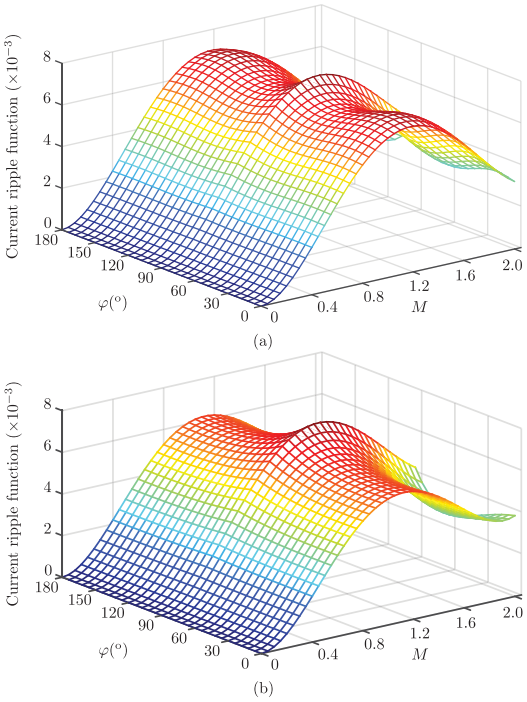

Fig. 9. CRF characteristic of the proposed method. (a) i_{ac}. (b) i_f.

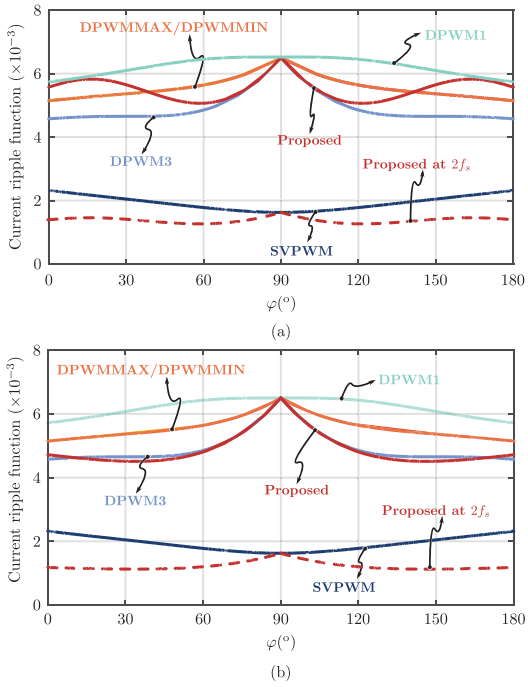

Fig. 10. CRF comparison with various PWM methods at $M = 1.6$ and different φ. (a) i_{ac}. (b) i_f.

the peak voltage on C_f can be $U_f = U_{dc} = 400$ V For the sake of cost saving, 250 V_{rms} voltage class ac film capacitors are used, and the maximum voltage of the storage capacitor is set to be 240 V_{rms}. Therefore, in the prototype the capacitance value of the storage capacitor is designed to be 110 μF, which consists of five 20 μF/250 V_{rms} (B32756G2206, TDK Electronics) and one 10 μF/250 V_{rms} (B32754C2106, TDK Electronics) ac film capacitors.

B. Controller Design

The full-bridge-based bidirectional single-phase ac–dc converter with active power decoupling circuit and its corresponding control blocks implemented in this article are shown in Fig. 11, which consist of two simplified models of the control loops. The first one in Fig. 11(b) is the model for the ac side current i_{ac} controller and the second one in Fig. 11(c) is the model for the storage capacitor voltage u_f and current i_f controllers for the active power decoupling circuit. Since all tasks executed in the digital signal processor (DSP), i.e., analog-digital conversion, control loops computation, PWM value update, and communication with host computer, cannot be finished within one switching period, i.e., 25 μs (1/40k), the controlling frequency of the system is set to be 20 kHz.

$K_{PWM} = 1$ is the gain of the PWM converter. The quasi-proportional-resonant (PR) controllers are adopted for all of the

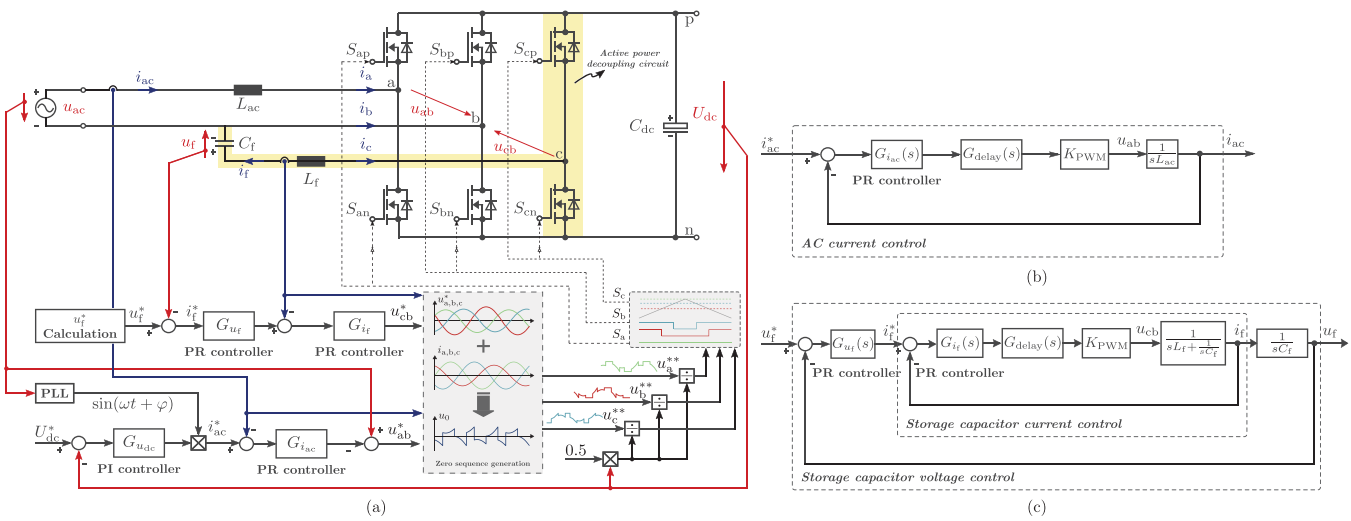

Fig. 11. Overall control block diagram of the bidirectional ac–dc converter. (a) Control block diagram. (b) Simplified model for grid current controller. (c) Simplified model for storage capacitor voltage and current controllers.

PR controllers in Fig. 11(b) and (c), whose transfer function is

$$G_{\mathrm{PR}}(s) = K_p + K_r \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega^2}. \tag{31}$$

The delay transfer function is approximated as

$$G_{\mathrm{delay}}(s) = \frac{1 - e^{-sT_d}}{sT_d} \tag{32}$$

where $T_d = 50\,\mu$s is the control period. The open loop transfer function for the ac current control loop is

$$G_{i_{\mathrm{ac}}}(s) = K_{\mathrm{PWM}} G_{\mathrm{delay}}(s) G_{i_{\mathrm{ac}}}(s) \frac{1}{sL_{\mathrm{ac}}}. \tag{33}$$

Taking $K_{p,i_{\mathrm{ac}}} = 5, K_{r,i_{\mathrm{ac}}} = 300, \omega_{c,i_{\mathrm{ac}}} = 25$, the bode plot is shown in Fig. 12(a).

Similar with the ac current, the open loop transfer function of the storage capacitor current controller is

$$G_{i_{\mathrm{f}}}(s) = K_{\mathrm{PWM}} G_{\mathrm{delay}}(s) G_{i_{\mathrm{f}}}(s) \frac{1}{sL_{\mathrm{f}} + \frac{1}{sC_{\mathrm{f}}}}. \tag{34}$$

Choosing $K_{p,i_{\mathrm{f}}} = 4, K_{r,i_{\mathrm{f}}} = 300, \omega_{c,i_{\mathrm{f}}} = 25$, the bode plot is shown in Fig. 12(b).

Accordingly, the closed-loop transfer function of the storage capacitor current controller is

$$H_{i_{\mathrm{f}}}(s) = \frac{G_{i_{\mathrm{f}}}(s)}{G_{i_{\mathrm{f}}}(s) + 1} \tag{35}$$

and the open-loop transfer function of the outer loop (storage capacitor voltage control loop), as shown in Fig. 11(c) is

$$G_{u_{\mathrm{f}}}(s) = G_{u_{\mathrm{f}}}(s) H_{i_{\mathrm{f}}}(s) \frac{1}{sC_{\mathrm{f}}}. \tag{36}$$

The parameters for PR controller are: $K_{p,u_{\mathrm{f}}} = 0.15, K_{r,u_{\mathrm{f}}} = 5, \omega_{c,u_{\mathrm{f}}} = 25$, and the bode plot is shown in Fig. 12(c).

As shown in Fig. 12, with the proper selection of K_p, K_r, and ω_c, all of the control loops have the acceptable phase margin and gain margin to be able to keep the system stable and to track the voltage and current references.

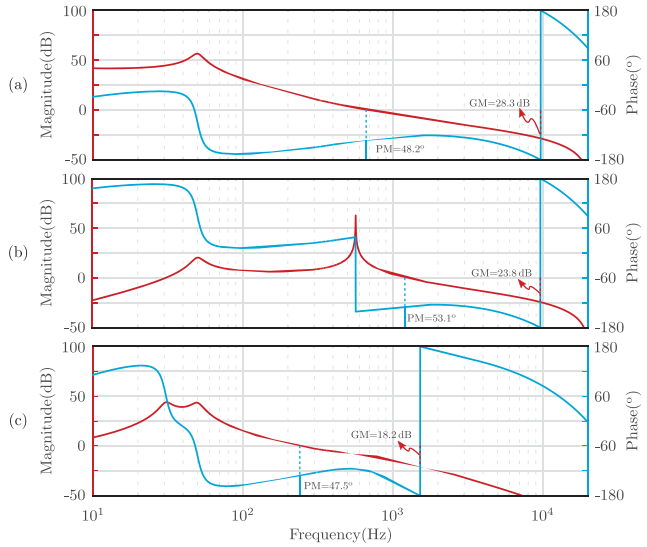

Fig. 12. Bode plot of different control loops. (a) AC current loop. (b) Storage capacitor current loop. (c) Storage capacitor voltage loop.

VI. Simulation and Experimental Results

To validate the effectiveness of the proposed PWM method, simulations and experimental tests are conducted and compared with different PWM methods. First, a PLECS-based simulation is carried out. After that, the proposed PWM method is operated on a digital-control hardware platform with digital signal processor (DSP) from Texas Instruments, TMS320F28379. In both simulation and experiment, SiC MOSFETs from CREE C3M0120090J [32] are used. Since DPWMMAX and DPWMMIN methods have the same performance in terms of switching

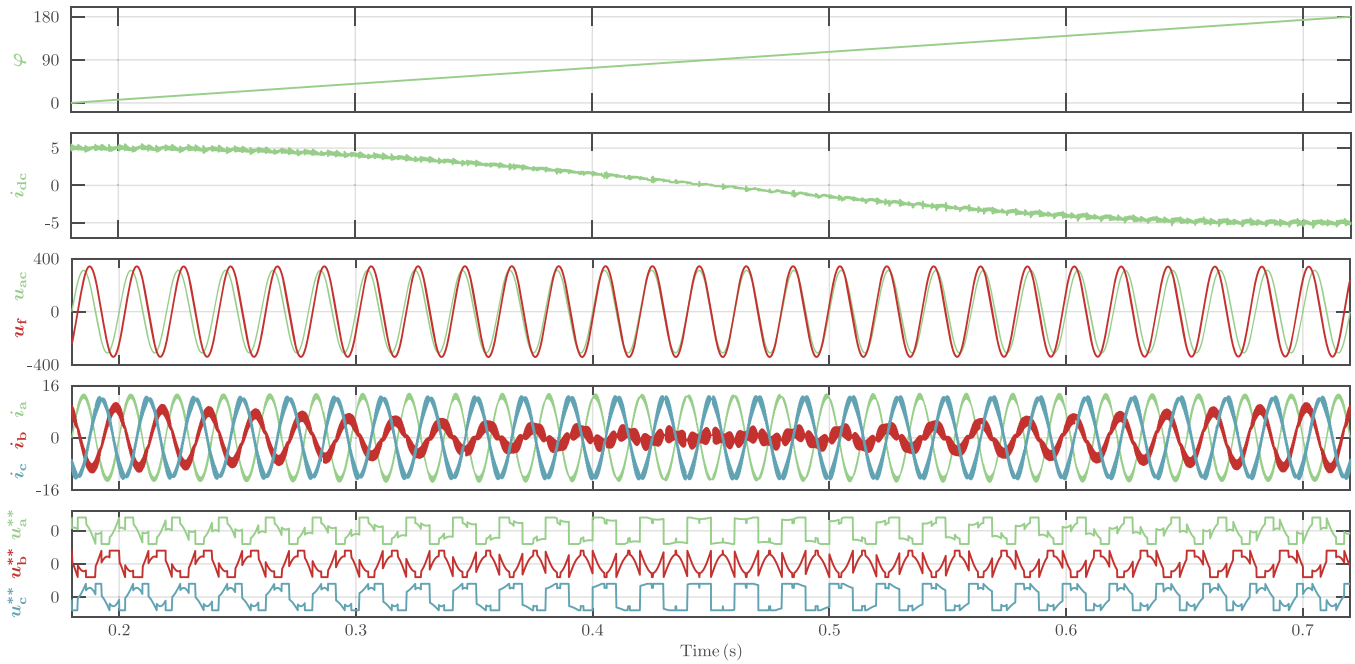

Fig. 13. Simulation waveforms of dc side current $i_{\rm dc}$, ac voltage $u_{\rm ac}$, storage capacitor voltage $u_{\rm f}$, three phase currents $i_{\rm a,b,c}$, and three phase modulation signals $u^{**}_{\rm a,b,c}$ with φ increase from 0° at $t = 0.2$ s to 180° at $t = 0.7$ s, when using the proposed PWM method.

losses and current distortion, only DPWMMIN is studied in this section.

A. Simulation Results

Fig. 13 shows the simulation waveforms of the dc side current $i_{\rm dc}$, ac voltage $u_{\rm ac}$, storage capacitor voltage $u_{\rm f}$, three phase currents $i_{\rm a,b,c}$, and three phase modulation signals $u^{**}_{\rm a,b,c}$ with φ increase from 0° at $t = 0.2$ s to 180° at $t = 0.7$ s, when using the proposed PWM method. To keep the power constant at $S = 2$ kVA, in Fig. 13, a 400 V output dc voltage source in series with a small dc filter inductor (5 μH) is used and the rms value of the grid current $i_{\rm ac}$ is controlled to be 9.09 $A_{\rm rms}$. As previously discussed, the 2ω ripple exists in the dc side current $i_{\rm dc}$ of a single-phase full-bridge ac–dc converter. With the enabling of the active power decoupling circuit, the second-order component of the $i_{\rm dc}$ can be suppressed considerably. Correspondingly, the clamping areas are determined by the calculation flow chart in Fig. 4. It is evident that the device is clamped and adjusted at the peak current with any different φ value when the converter is running, including rectifier, STATCOM, and inverter operating modes, which will reduce the switching losses at any operating cases.

Fig. 14 compares the simulation results of the $i_{\rm ac}$ and $i_{\rm f}$ with various PWM methods at $\varphi = 0°$, $S = 2$ kVA. Since the inductance of $L_{\rm f}$ is smaller than that of $L_{\rm ac}$, the current ripple on $i_{\rm f}$ is higher than the ripple on $i_{\rm ac}$. By visual inspection one can observe that the current ripple of the SVPWM is the lowest, and that the different DPWM methods do not have remarkable differences. To obtain a better insight, while keeping $S = 2$ kVA, the current total harmonic distortion (THD) for various PWM

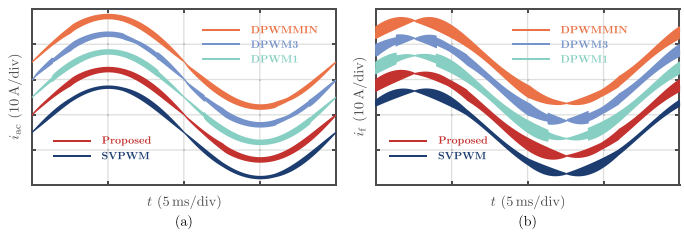

Fig. 14. Simulation comparison among various PWM method at $\varphi = 0°$, $S = 2$ kVA. (a) $i_{\rm ac}$. (b) $i_{\rm f}$.

methods with different φ are compared in Fig. 15(a) and (b), where the capacitance of $C_{\rm f}$ is implemented with the optimized value of 110 μF to attain a lower volume of the capacitors as designed in Section V-A. As shown in Fig. 15(a) and (b), DPWM1 has the highest current THD value among all DPWM methods, while DPWM3 is relatively less than the other DPWM methods, which comes to the similar result as normal DPWM methods in a three-phase three-wire balanced system [27]. The current THD of the proposed PWM is close to that of DPWM3 when φ is close to 90°. In order to verify the correctness of the CRF model in Section IV-B, the capacitance of $C_{\rm f}$ is changed to be 131.6 μF, where $U_{\rm f} = U_{\rm ac}$ and the assumptions in Section IV will be realized. In this case, the current THD comparisons for $i_{\rm ac}$ and $i_{\rm f}$ are presented in Fig. 15(c) and (d), which match well with the theoretical model in Fig. 10. Therefore, the effectiveness of the CRF model in Section IV-B is proved.

Fig. 16 shows the total switching losses comparison among different PWM methods with two capacitance configurations. The data-sheet value of $E_{\rm on}$ and $E_{\rm off}$ are used and built into

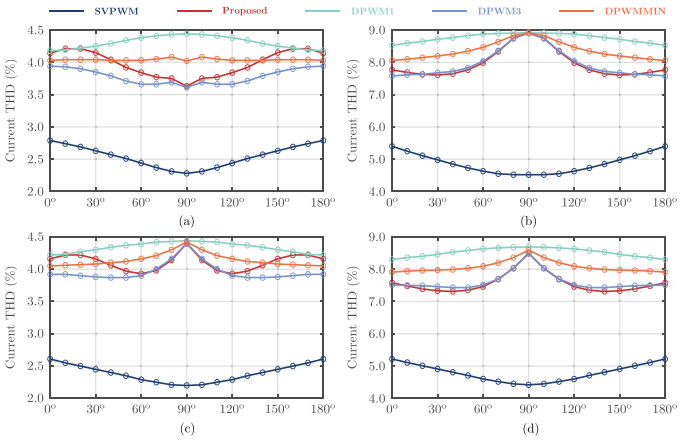

Fig. 15. Current THD comparison. (a) i_{ac} with $C_{\mathrm{f}} = 110\,\mu$F. (b) i_{f} with $C_{\mathrm{f}} = 110\,\mu$F. (c) i_{ac} with $C_{\mathrm{f}} = 131.6\,\mu$F. (d) i_{f} with $C_{\mathrm{f}} = 131.6\,\mu$F.

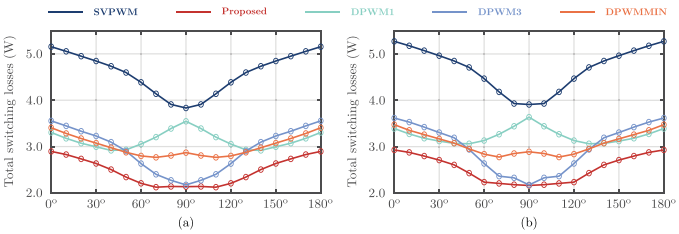

Fig. 16. Total switching losses comparison, (a) with $C_{\mathrm{f}} = 110\,\mu$F, (b) with $C_{\mathrm{f}} = 131.6\,\mu$F.

the thermal model of the SiC MOSFET in PLECS simulation. As expected, the switching losses for all DPWM methods are lower than that for SVPWM. In both cases, the switching losses for the proposed PWM method is the lowest. DPWM1 has relatively high switching losses as φ is close to 90°, while DPWM3 has the opposite trend. Since the change trend with φ of different PWM methods in Fig. 16(b) matches the SLF model given in Fig. 7, the correctness of the SLF model in Section IV-A is verified as well.

Fig. 17 shows the simulation results of the transient responses with the proposed PWM method when the active power decoupling controller is enabled at $t = 0.3$ s and the power is stepped up from 1 to 2 VA at $t = 0.38$ s. To show a clear effectiveness of the active power decoupling control, resistive loads are used on the dc side, and the capacitance value of C_{f} is 110 μF. Three specific cases are selected in Fig. 17. The first one is the unity power factor rectifier mode where $\varphi = 0°$; the second one is the rectifier mode where $\varphi = 30°$; the last one is the STATCOM mode where $\varphi = 90°$ with no dc resistive load. It can be seen that in all cases, the proposed PWM method works well to suppress the dc-link voltage ripple during the transient time, and the corresponding modulation waveform can be adjusted adaptively.

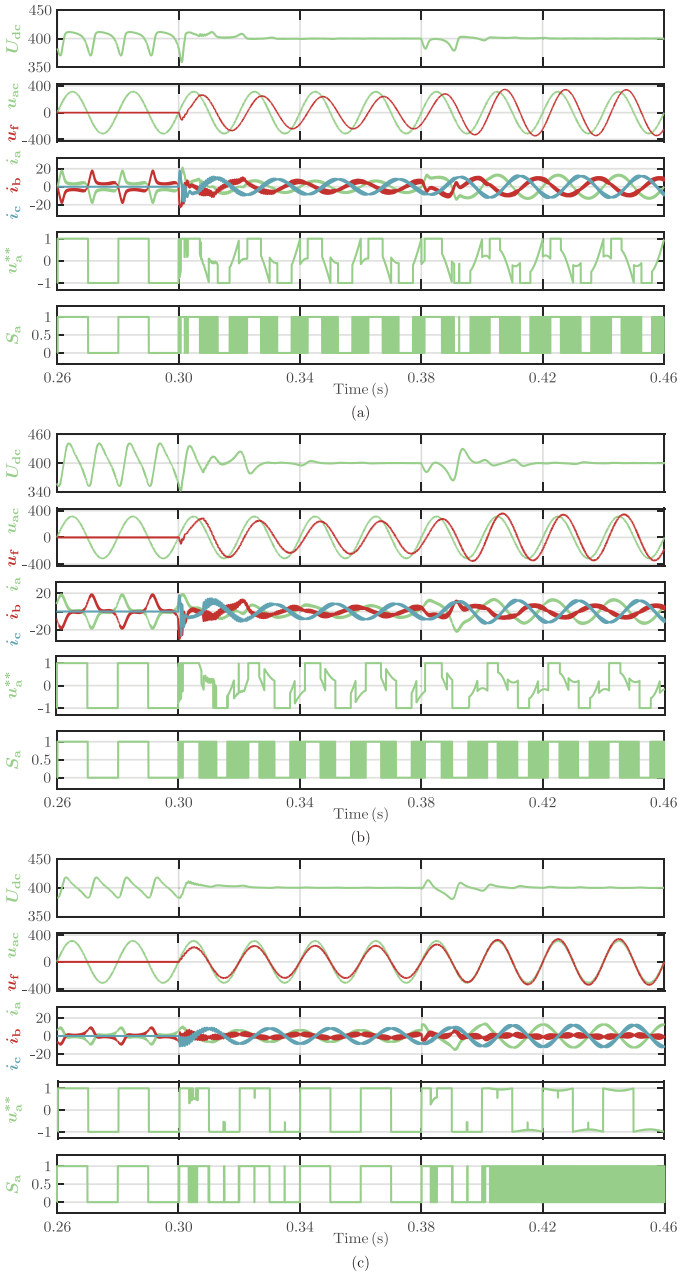

Fig. 17. Simulation results of the transient responses with the proposed DPWM method when enabling the active power decoupling control at $t = 0.3$ s and power step-up at $t = 0.38$ s. (a) $\varphi = 0°$ unity power factor rectifier mode. (b) $\varphi = 30°$ rectifier mode. (c) $\varphi = 90°$ STATCOM.

B. Experimental Results

A 2-kVA prototype based on the power electronic circuit presented in Fig. 11(a) is built to further validate the feasibility and superiority of the proposed PWM method. In experiments, the bidirectional single-phase ac–dc converter is operated in inverter, rectifier, and STATCOM modes working with different PWM methods. The experimental setup and the detailed photos for the constructed single-phase ac–dc converter are shown in Fig. 18 with $C_{\mathrm{f}} = 110\,\mu$F. The average dc voltage in all experimental cases is controlled at 400 V. All of the experimental waveforms are recorded by the oscilloscope YOKOGAYA DLM4058, and the current THD and power conversion efficiency of the converter are tested by the power analyzer YOKOGAYA WT500. To realize the proposed method in practice, additional comparison

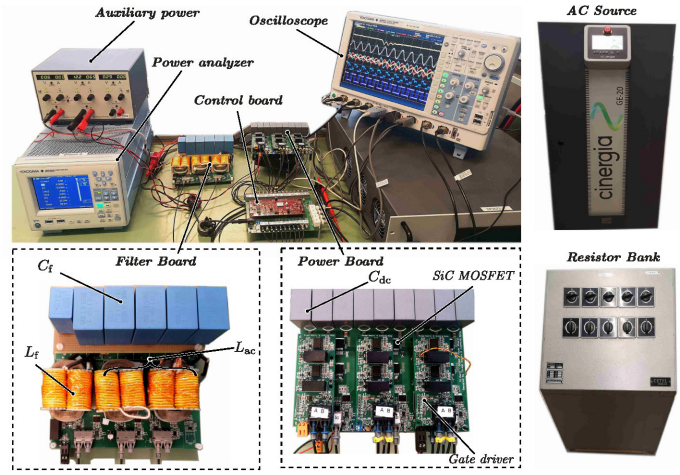

Fig. 18. Experimental setup.

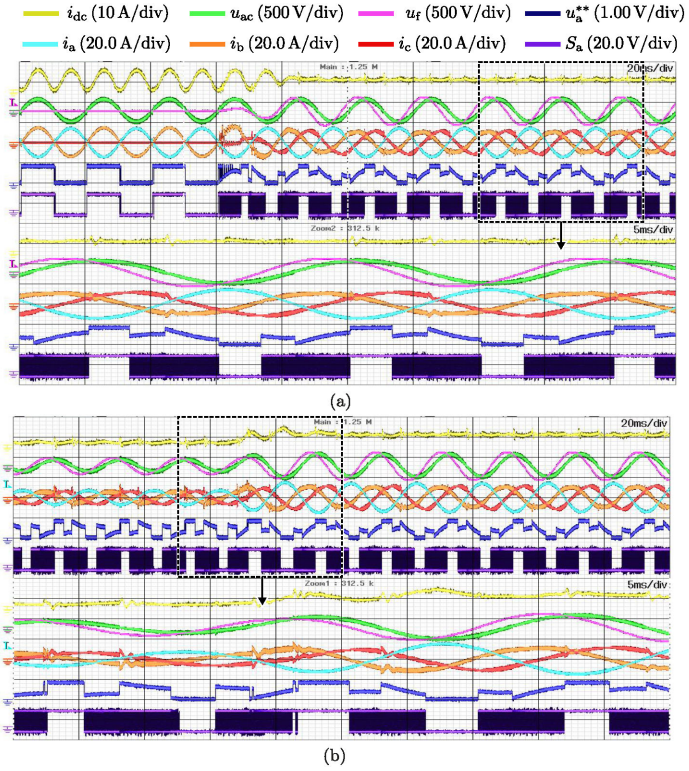

Fig. 19. Experimental results showing the steady and transient states with the proposed PWM method in inverter mode. (a) Enabling the decoupling control. (b) Load step-up. Note that the zoom function of the oscilloscope is used to show the details of the highlighted section of the experimental waveforms.

operations are needed in the DSP code. It is tested that the execution time for the proposed method is 1.27 μs, which is merely 0.45 μs longer than the implemented SVPWM in the DSP TMS320F28779D. Therefore, the complexity of the proposed method is acceptable.

Fig. 19 shows the experimental results for the steady and transient states with the proposed PWM method in inverter mode. In this case, a dc source with 400 V output and a 20 Ω ac restive load on the ac side are used, where φ is set at 180°. Due to the intrinsically large dc capacitor on the output of the commercial dc source, the 2ω ripple can be found in the dc side current i_{dc} when the active power decoupling functionality is disabled. Fig. 19(a) presents the experimental waveform before and after the active power decoupling circuit is enabled to work with 10 A_{rms}, and Fig. 19(b) presents the experimental waveform when a step-up ac current command which sets a reference change from 5 to 10 A_{rms} is used. In both cases, the ripple in i_{dc} can be reduced, and the proposed PWM method adapts well the changes of the output current when the converter is operating in the inverter mode.

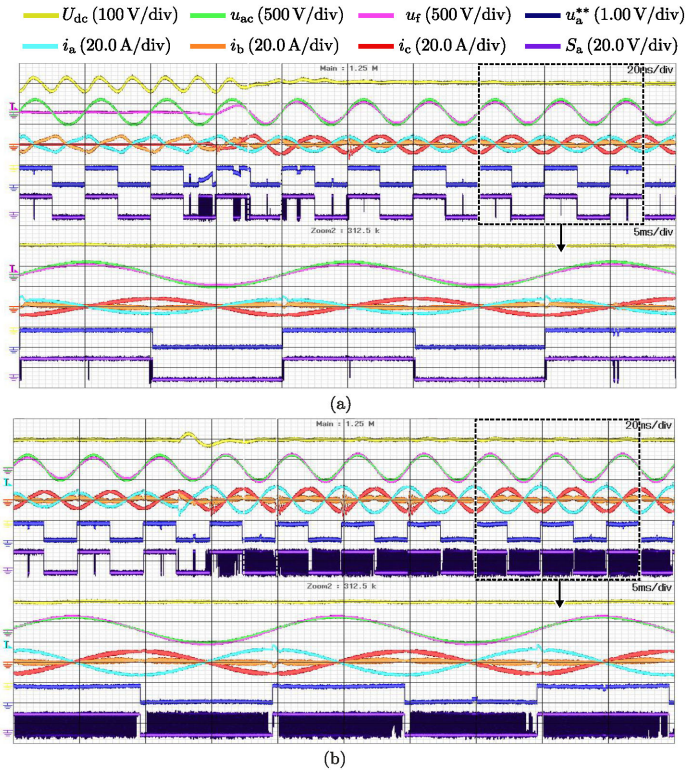

Fig. 20. Experimental results showing the steady and transient states with the proposed PWM method in STATCOM mode. (a) Enabling the decoupling control. (b) Load step-up. Note that the zoom function of the oscilloscope is used to show the details of the highlighted section of the experimental waveforms.

Fig. 20 shows the experimental results for the steady and transient states with the proposed PWM method in STATCOM mode. In this case, an ac voltage source with 220 $V_{rms}/50$ Hz is used and no load is connected to the dc-link, where φ is set to be 90°. Since a low value of smoothing dc capacitance is used on the dc side, the voltage ripple at the dc-link is particularly high. This relatively high dc voltage ripple deteriorates the performance of the current control loop and the ac side current gets distorted. Fig. 20(a) presents the experimental waveform before and after the active power decoupling circuit is enabled to work with 5 A_{rms}, and Fig. 20(b) presents the experimental waveform during the ac current command, which changes the current reference from 5 to 10 A_{rms}. In both cases, the ripple in the dc voltage reduces remarkably and the ac current waveform shape improves as well.

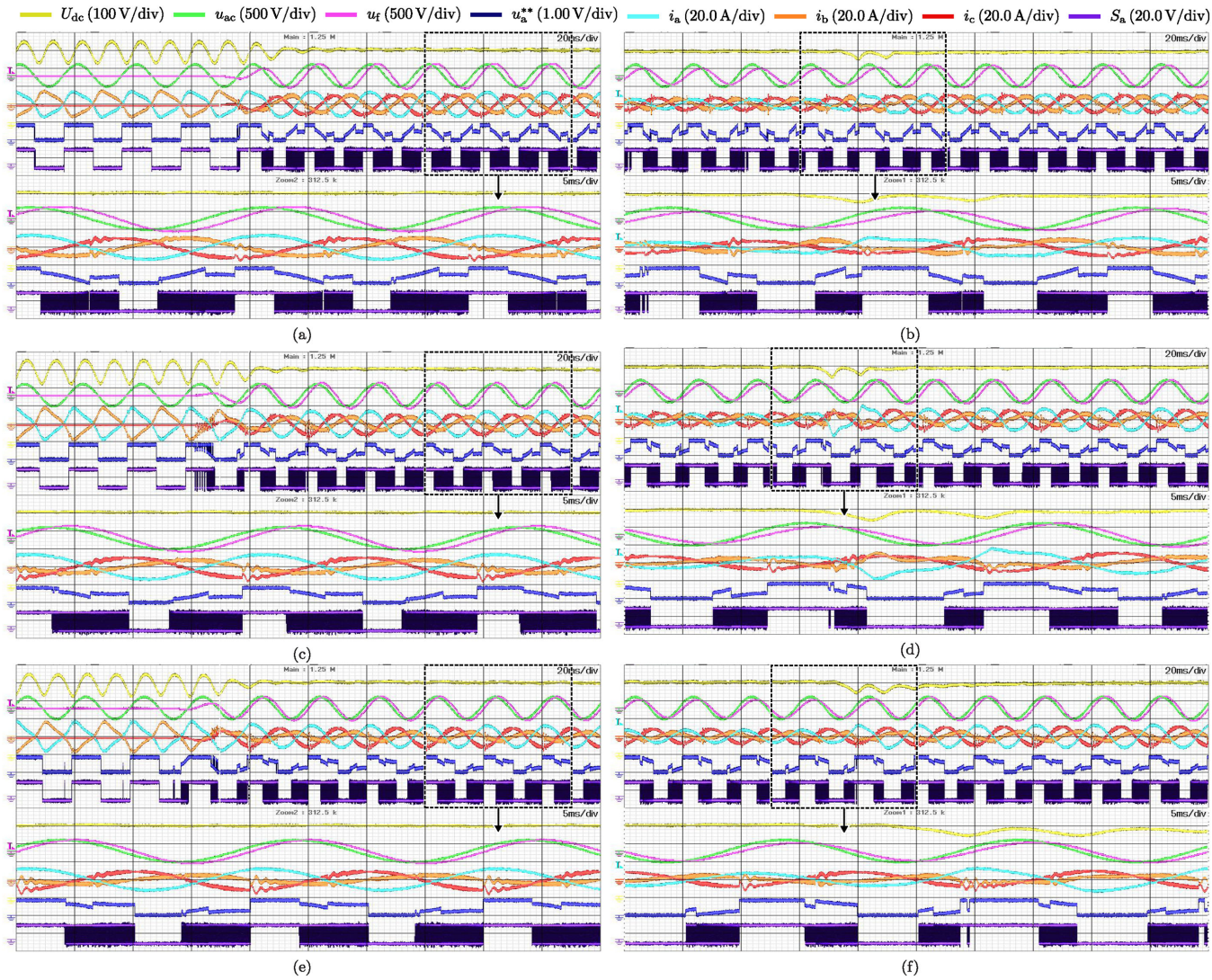

Fig. 21. Experimental results of the steady and transient states with the proposed PWM method in rectifier mode at different φ. (a) Enabling the decoupling control at $\varphi = 0^\circ$. (b) Load step-up at $\varphi = 0^\circ$. (c) Enabling the decoupling control at $\varphi = 30^\circ$. (d) Load step-up at $\varphi = 30^\circ$. (e) Enabling the decoupling control at $\varphi = 45^\circ$. (f) Load step-up at $\varphi = 45^\circ$. Note that the zoom function of the oscilloscope is used to show the details of the highlighted section of the experimental waveforms.

Fig. 21 shows the experimental results for the steady and transient states with the proposed PWM method in rectifier mode. In this case, an ac voltage source with 220 $\mathrm{V_{rms}}/50$ Hz is used and a dc resistor bank is connected to the dc-link, where φ is set as 0°, 30°, and 45°, respectively. Similar as the STATCOM mode, because of a low value of smoothing dc capacitance on the dc side, when the power decoupling circuit is not enabled a particularly high voltage ripple exists at the dc-link and a large distortion is resulted at the ac side current. Fig. 21(a), (c), and (e) presents the experimental waveform before and after the active power decoupling circuit is enabled to work, where different resistance is configured through the resistor bank to make the converter to operate at $S = 2\,\mathrm{kVA}$. With the enabling of the active power decoupling circuit and the incorporated ac power compensation components, the ripple in the dc voltage reduces remarkably and the ac current waveform shape improves as well. Fig. 21(b), (e), and (f) are the experimental waveforms for a load step-up from $S = 1$ to $2\,\mathrm{kVA}$. It can be seen that the proposed PWM method works well to suppress the dc-link voltage ripple effectively with different φ during the load step-up transient time, and the corresponding modulation waveform can also be adjusted rapidly. All of the experimental cases show that the proposed PWM method can adapt the changes of the set phase angle φ well, and the switching signal S_a is clamped along different intervals with different duration depending on the currents, as illustrated in Fig. 5.

To compare with the proposed PWM method, different PWM methods are studied in experiments as well. Experimental results of the transient states during the enabling of the decoupling control with the other PWM methods in rectifier mode at $\varphi = 0^\circ$ are shown in Fig. 22. The converter is working at $S = 2\,\mathrm{kVA}$ with dc resistor bank. The dc voltage ripple can also be suppressed in the experiment with the other studied PWM methods, while effectively tracking the sinusoidal current reference. It can be

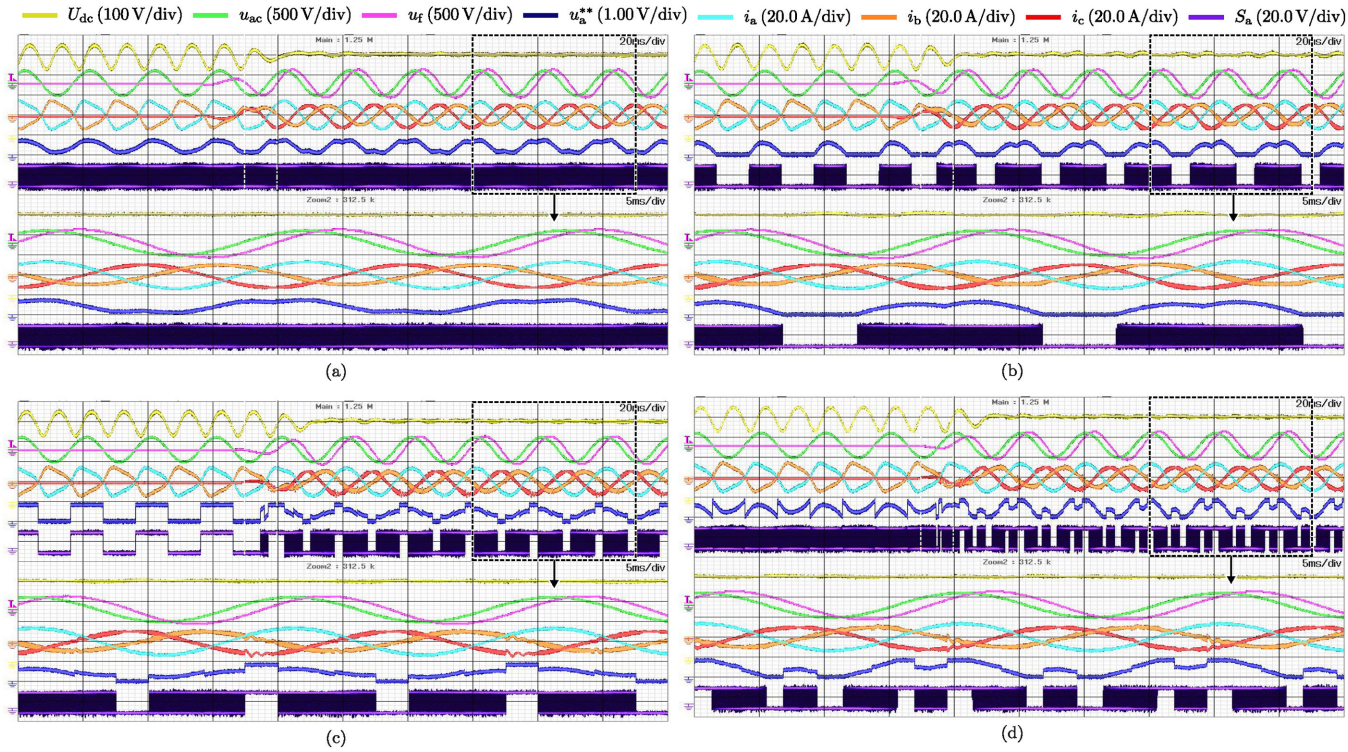

Fig. 22. Experimental results of the transient states during the enabling of the decoupling control with the other PWM methods in rectifier mode at $\varphi = 0°$. (a) SVPWM. (b) DPWMMIN. (c) DPWM1. (d) DPWM3. Note that the zoom function of the oscilloscope is used to show the details of the highlighted section of the experimental waveforms.

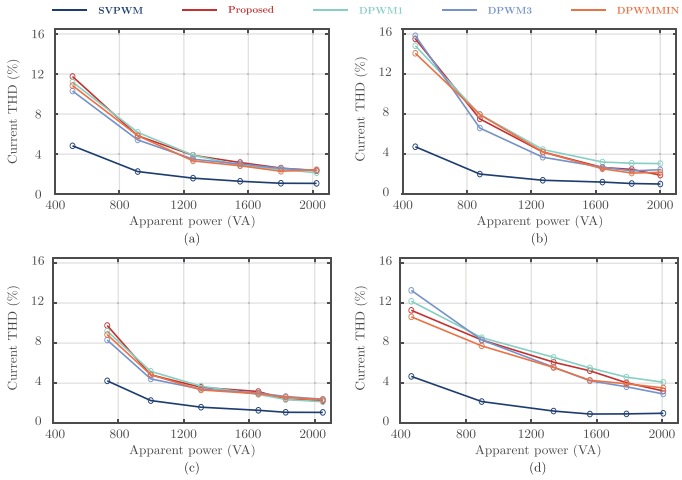

Fig. 23. Current THD comparison. (a) $\varphi = 0°$ rectifier mode. (b) $\varphi = 30°$ rectifier mode. (c) $\varphi = 180°$ inverter mode. (d) $\varphi = 90°$ STATCOM mode.

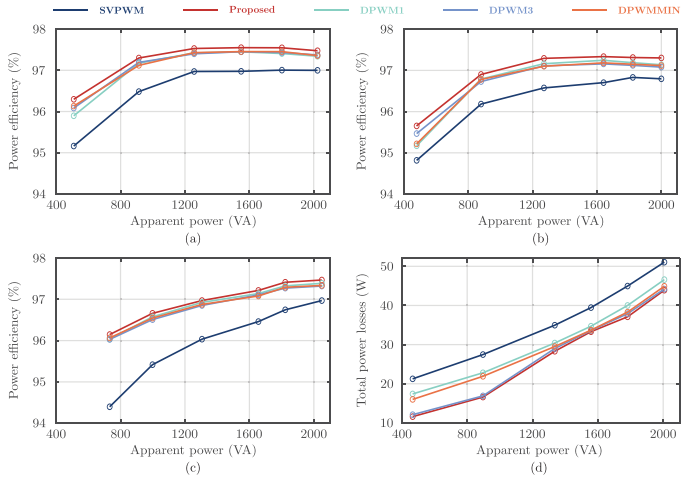

Fig. 24. Power efficiency and power losses comparison. (a) $\varphi = 0°$ rectifier mode. (b) $\varphi = 30°$ rectifier mode. (c) $\varphi = 180°$ inverter mode. (d) $\varphi = 90°$ STATCOM mode.

seen that the clamped duration time of S_a for different DPWM methods in Fig. 22 are shorter than that for the proposed PWM method. Therefore, a reduced switching losses will be achieved with the proposed method.

Fig. 23 shows the comparison of current THD between the proposed PWM method and the other studied conventional PWM methods. Since only the harmonics components below 50th order are considered in the power analyzer, the tested current THD results are lower than the one obtained from the PLECS simulation. It can be seen that with the implementation of DPWM methods, the current THD will be increased for all cases. At high power level, the current THD difference between the DPWM methods and SVPWM is relatively small. The current THD for various DPWM methods are close to each other as expected in Fig. 15.

Fig. 24 shows the power efficiency and power losses comparison between the proposed PWM method and the other studied PWM methods. In Fig. 24(d), for STATCOM mode, the output active power is zero, thus, the measured input active power is regarded as an estimation of the total losses in the converter, including the losses from the switching devices and filter components. As shown in Fig. 24, with DPWM methods, the power efficiency of the converter can be improved remarkably, and the highest power efficiency is obtained by the proposed PWM method.

All in all, the presented experimental cases have shown that a remarkable reduction on power losses with the proposed PWM method is possible when implementing a bidirectional single-phase converter with active power decoupling. This confirms the superiority of the proposed modulation method when compared to other traditional PWM strategies. Therefore, the validity and advantages of the proposed PWM method are verified.

VII. Conclusion

This article has proposed a new DPWM method for a bidirectional single-phase ac–dc converter associated with ac-type half-bridge active power decoupling circuit. The proposed method is based on the measurements of the converter's ac currents and reference voltages. This modulator adaptively clamps the switching device that conducts the largest current at any instant, which leads to the optimum clamped duration to obtain a minimum switching losses across the semiconductors, so that it could allow enhancement of the system power density by improving power conversion efficiency and, thus reducing the requirement and cost of thermal management of the semiconductors. The mathematical models have been built and shown that the proposed strategy not only has the minimum switching loss over other suitable PWM methods within all power factor angle range, but also can achieve improved current distortion performance under the same switching losses. Both simulations and experimental results have been used to verify the effectiveness of the proposed modulation method, and to prove the correctness of the presented theoretical analysis. The proposed method is proved to be able to adapt the changes of the set phase angle and load step. It is found that in the experiments, the highest power efficiency can be obtained by the proposed PWM method in comparison with other modulation methods, and the performance of the current distortion of the proposed methods is similar to other DPWM methods under the same switching frequency.

References

[1] L. Zhang, K. Sun, L. Feng, H. Wu, and Y. Xing, "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 730–739, Feb. 2013.

[2] J. R. Rodriguez, J. W. Dixon, J. R. Espinoza, J. Pontt, and P. Lezana, "PWM regenerative rectifiers: State of the art," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 5–22, Feb. 2005.

[3] T. Isobe, D. Shiojima, K. Kato, Y. R. R. Hernandez, and R. Shimada, "Full-bridge reactive power compensator with minimized-equipped capacitor and its application to static var compensator," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 224–234, Jan. 2016.

[4] Y. Tang, F. Blaabjerg, P. C. Loh, C. Jin, and P. Wang, "Decoupling of fluctuating power in single-phase systems through a symmetrical half-bridge circuit," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1855–1865, Apr. 2015.

[5] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4778–4794, Jul. 2016.

[6] W. Yao, Y. Xu, Y. Tang, P. C. Loh, X. Zhang, and F. Blaabjerg, "Generalized power decoupling control for single-phase differential inverters with nonlinear loads," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1137–1151, Jun. 2019.

[7] Z. Qin, Y. Tang, P. C. Loh, and F. Blaabjerg, "Benchmark of ac and dc active power decoupling circuits for second-order harmonic mitigation in kilowatt-scale single-phase inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 15–25, Mar. 2016.

[8] H. Wang, H. Wang, G. Zhu, and F. Blaabjerg, "An overview of capacitive dc-links-topology derivation and scalability analysis," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1805–1829, Feb. 2020.

[9] S. Li, W. Qi, S. Tan, and S. Y. Hui, "Enhanced automatic-power-decoupling control method for single-phase ac-to-dc converters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1816–1828, Feb. 2018.

[10] D. Neumayr, D. Bortis, and J. W. Kolar, "The essence of the little box challenge-part a: Key design challenges solutions," *CPSS Trans. Power Electron. Appl.*, vol. 5, no. 2, pp. 158–179, 2020.

[11] D. Neumayr, G. C. Knabben, E. Varescon, D. Bortis, and J. W. Kolar, "Comparative evaluation of a full-and partial-power processing active power buffer for ultra-compact single-phase dc/ac converter systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, early access, Apr. 14, 2020 doi: 10.1109/JESTPE.2020.298793710.

[12] R. Wang *et al.*, "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1430–1443, May 2011.

[13] M. Jang, M. Ciobotaru, and V. G. Agelidis, "A single-stage fuel cell energy system based on a buck–boost inverter with a backup energy storage unit," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2825–2834, Jun. 2012.

[14] X. Cao, Q. Zhong, and W. Ming, "Ripple eliminator to smooth dc-bus voltage and reduce the total capacitance required," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 2224–2235, Apr. 2015.

[15] M. Qiu, P. Wang, H. Bi, and Z. Wang, "Active power decoupling design of a single-phase ac–dc converter," *Electronics*, vol. 8, no. 8, pp. 841–858, 2019.

[16] W. Cai, B. Liu, S. Duan, and L. Jiang, "An active low-frequency ripple control method based on the virtual capacitor concept for BIPV systems," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1733–1745, Apr. 2014.

[17] Y. Yang, X. Ruan, L. Zhang, J. He, and Z. Ye, "Feed-forward scheme for an electrolytic capacitor-less ac/dc led driver to reduce output current ripple," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5508–5517, Oct. 2014.

[18] Y. Tang and F. Blaabjerg, "A component-minimized single-phase active power decoupling circuit with reduced current stress to semiconductor switches," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2905–2910, Jun. 2015.

[19] Y. Tang, Z. Qin, F. Blaabjerg, and P. C. Loh, "A dual voltage control strategy for single-phase PWM converters with power decoupling function," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7060–7071, Dec. 2015.

[20] H. Zhang, X. Li, B. Ge, and R. S. Balog, "Capacitance, dc voltage utilizaton, and current stress: Comparison of double-line frequency ripple power decoupling for single-phase systems," *IEEE Ind. Electron. Mag.*, vol. 11, no. 3, pp. 37–49, Sep. 2017.

[21] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, "Active power decoupling for high-power single-phase PWM rectifiers," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1308–1319, Mar. 2013.

[22] R. Chen, Y. Liu, and F. Z. Peng, "Dc capacitor-less inverter for single-phase power conversion with minimum voltage and current stress," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5499–5507, Oct. 2015.

[23] S. Bhowmick and L. Umanand, "Design and analysis of the low device stress active power decoupling for single-phase grid connection for a wide range of power factor," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 1921–1931, Dec. 2018.

[24] H. Wu, S. Wong, C. K. Tse, and Q. Chen, "Control and modulation of bidirectional single-phase AC-DC three-phase-leg SPWM converters with active power decoupling and minimal storage capacitance," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4226–4240, Jun. 2016.

[25] S. Bhowmick and L. Umanand, "A high-performance dynamic controller for an active power decoupler with ac-side storage element," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 2041–2056, Sep. 2019.
[26] B. Ge, X. Li, H. Zhang, Y. Liu, R. S. Balog, H. Abu-Rub, and L. Alpuerto, "Direct instantaneous ripple power predictive control for active ripple decoupling of single-phase inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 4, pp. 3165–3175, Apr. 2018.
[27] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1059–1071, Sep. 1998.
[28] J. Xu, J. Han, Y. Wang, M. Ali, and H. Tang, "High-frequency sic three-phase vsis with common-mode voltage reduction and improved performance using novel tri-state PWM method," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1809–1822, Feb. 2019.
[29] T. D. Nguyen, J. Hobraiche, N. Patin, G. Friedrich, and J. P. Vilain, "A direct digital technique implementation of general discontinuous pulse width modulation strategy," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4445–4454, Sep. 2011.
[30] S. L. An, X. D. Sun, Q. Zhang, Y. R. Zhong, and B. Y. Ren, "Study on the novel generalized discontinuous SVPWM strategies for three-phase voltage source inverters," *IEEE Trans. Ind. Inf.*, vol. 9, no. 2, pp. 781–789, May 2013.
[31] J. Xu, J. Han, Y. Wang, S. Habib, and H. Tang, "A novel scalar PWM method to reduce leakage current in three-phase two-level transformerless grid-connected VSIs," *IEEE Trans. Ind. Electron.*, vol. 67, no. 5, pp. 3788–3797, May 2020.
[32] *Datasheet of C3M0120090J*, CREE Power Applications, Durham, NC, USA, Jan. 2018. [Online]. Available: https://www.wolfspeed.com/media/downloads/834/C3M0120090J.pdf

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