DC-Readout of Semiconductor Spin Qubits

Opportunities and Limits

Kiene, G.; Pietx i Casas, O.; Babaie, M.; Vandersypen, L.M.K.; Sebastiano, F.

DOI
10.1109/TCSI.2025.3542335

Publication date
2025

Document Version
Final published version

Published in
IEEE Transactions on Circuits and Systems Part 1: Regular Papers

DC-Readout of Semiconductor Spin Qubits: Opportunities and Limits

Gerd Kiene, *Member, IEEE*, Oriol Pietx-Casas, Masoud Babaie, *Senior Member, IEEE*, Lieven M. K. Vandersypen, and Fabio Sebastiano, *Senior Member, IEEE*

***Abstract*— This paper presents extensive guidelines for the design of an integrated DC-readout interface for semiconductor spin qubits. Since the focus is on the readout via a single electron transistor (SET), the SET behavior and performance are first described and modeled, showing that the signal-to-noise ratio (SNR) theoretically achievable by a SET-based DC-readout is significantly beyond the state-of-the-art. Practical circuit architectures for implementing a DC-readout, such as the voltage amplifier, the transimpedance amplifier, the charge sampling, and the current pre-amplifier, are then analyzed by deriving their design equations and trade-offs. As a result, the practical performances of those different solutions are evaluated and compared, thus presenting clear selection criteria for the readout architecture and its design equations given the specific parameters of the SET sensor.**

***Index Terms*— DC-readout, Cryo-CMOS, single electron transistor, SET, quantum computing.**

I. Introduction

QUANTUM computers based on semiconductor spin qubits have promising scaling properties [1], specifically due to their demonstrated operation at higher temperatures [2], [3], their small feature size (100 nm × 100 nm) and their compatibility with CMOS manufacturing [4], [5]. These properties make them well-suited for integration with an electronic interface: first, qubit operation at comparatively high temperatures, above 4 K in [3], corresponds to more cooling power being available at the same temperature, meaning that the electronics operating close to the qubits can dissipate significantly more power, on the order of Watts [2]; second, compatibility with industrial manufacturing suggests that an eventual co-integration of electronics and qubits is possible. Thanks to such a promising outlook, numerous parts of the electronic interface for semiconductor spin qubits have already been proposed, such as microwave controllers [6], [7], ADCs [8], [9], biasing circuits [10], [11], LNAs [12], [13], and receiver chains [14], [15].

One of the most challenging operations in running a spin qubit quantum processor is the readout of the information encoded in the single spins: spin-states cannot be measured directly due to their extremely small magnetic moment, thus requiring the translation of the spin degree of freedom into a measurable quantity, e.g., charge, which can be measured with a nearby electrometer [16], [17].

Typically, a single-electron transistor (SET) is used for this purpose, e.g., as in [18]. The SET exhibits an abrupt change in impedance based on the surrounding electrostatic configuration, as described in section II. To electrically read the SET impedance, two main strategies are adopted: RF- and DC-readout. RF-readout provides the fastest single-shot readouts to date [19]. Additionally, it allows for potential frequency multiplexing [20], which can reduce the number of lines needed to interface the quantum device. This reduction is especially beneficial when operating the readout circuit at a different temperature stage. Further, the high frequencies used in the RF-readout allow for amplification far from the low-frequency noise of amplifiers in the electronic interface.

But RF-readout also carries heavy disadvantages in the perspective of scaling: it relies on bulky inductors for matching the sensor impedance [20], requires high-frequency sources and amplifiers for stimulation and amplification, as well as often relies on big off-chip passive components like directional couplers [14]. These factors contribute to a large scaling-unfriendly footprint compared to the qubit dimensions and to a significant power consumption for operating the RF interface. The same RF-readout strategy can also be adopted for gate-based readout [21], [22], which can avoid the use of the SET, still sharing the same (dis)advantages of the SET-based RF-readout.

In contrast, DC-readout has offered a much slower speed, mostly constrained by the large parasitic capacitance of the interconnect between the SET and the readout electronics. By using cryogenic amplification, however, this capacitance can be reduced, resulting in fast amplifiers being demonstrated using SiGe [23] and HEMT [24] transistors operating close to the quantum sample. An inherent downside of the DC-readout is the necessity of an individual electrical connection for each charge sensor to be read. If the sensor and the readout reside on different chips, a bond pad per sensor is required, which is a large offset to the otherwise compact readout. At the same time, no components are necessary for DC-readout that can not be efficiently integrated on the chip. This allows for a

Received 9 November 2024; revised 11 January 2025; accepted 2 February 2025. Date of publication 19 February 2025; date of current version 1 October 2025. This work was supported by Intel Corporation. This article was recommended by Associate Editor X. Fong. *(Corresponding author: Gerd Kiene.)*

Gerd Kiene and Fabio Sebastiano are with the Department of Quantum and Computer Engineering, Delft University of Technology, 2628 CJ Delft, The Netherlands, and also with QuTech, 2628 CJ Delft, The Netherlands (e-mail: g.kiene@tudelft.nl).

Oriol Pietx-Casas and Lieven M. K. Vandersypen are with the Kavli Institute of Nanoscience, Delft University of Technology, 2600 GA Delft, The Netherlands, and also with QuTech, 2628 CJ Delft, The Netherlands.

Masoud Babaie is with the Department of Microelectronics, Delft University of Technology, 2628 CJ Delft, The Netherlands, and also with QuTech, 2628 CJ Delft, The Netherlands.

Digital Object Identifier 10.1109/TCSI.2025.3542335

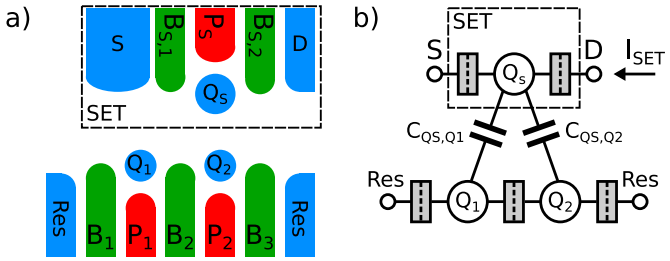


Fig. 1. a) Layout sketch of a typical double quantum dot with SET readout, b) schematic representation of setup. "Res" indicates a charge reservoir, B_x and P_y are barrier and plunger gates, Q_z the quantum dots.

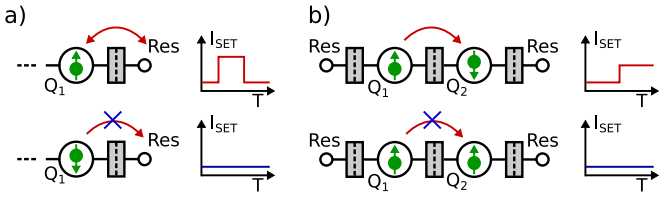


Fig. 2. Sketch of electron movement for a) energy-selective readout, adopted from [33], b) Pauli-spin-blockade readout, with the corresponding sensor response, which is smaller in b) due to the dipole nature of the signal.

potentially very dense co-integration of a CMOS-based DC-readout.

Thanks to those appealing features, several implementations of an integrated DC-readout circuit have been proposed: current comparators [25], [26], [27], trans-impedance amplifiers [28], [29], and a charge-sampling integrator [30]. While these constitute significant practical advances towards a scalable DC-readout, a systematic benchmarking of the different possible architectures and their trade-offs is still missing. Also, it is still unclear where the limits of DC-readout lie and how to approach them in practice. To aid the development of scalable amplifiers for DC-readout, we fill this gap here by deriving the limits and comparing practical readout interfaces. For such interfaces, we set the design goal of reaching a readout fidelity above 99.9%, i.e., well above the quantum-error-correction threshold [31], within a readout period of $T_b = 1\,\mu s$, i.e., a time compatible with spin qubit coherence time and gate duration [32], while minimizing the necessary power. This corresponds to bit-error-rates (BER) of 0.001 and, therefore, requires a signal-to-noise ratio (SNR) of 10 dB, as shown in the appendix.

The article is organized as follows: First, we review the SET as a charge sensor in section II to provide the understanding and modelling necessary to build the readout interface. In section III, a brief review of the CMOS and BiCMOS technologies available for the implementation of cryogenic amplifiers is given. Then, the fundamental limits for reading the SET in a DC-setup are derived in section IV, followed by an extensive architecture exploration and comparison for practical amplifier topologies in section V. Finally, a conclusion is drawn in section VI.

II. SET Model

Figure 1a) illustrates a typical planar layout of a double-quantum dot with an SET. The data-dots denoted as $Q_{1/2}$ are electrostatically defined by the potential of metal gates and can be filled with single electrons to form a two-qubit system. To measure the charge arrangement of this double-dot system, we utilize an SET. The SET itself is, in fact, a quantum dot with a high electron occupancy represented as Q_S. In this section, we describe how this example system is operated for the purpose of reading the spin information in the data-dots.

A. Spin-to-Charge Conversion

To read the spin state of the electrons in the data-dots $Q_{1/2}$, first, a spin-to-charge conversion needs to be performed. This manuscript focuses on electronics for the charge-state detection step. However, the choice of protocol for spin-to-charge conversion manuscript results in significant differences in the generated signals, which we discuss here briefly.

The main two protocols for performing a spin-to-charge conversion are energy-selective readout [33] and Pauli-spin-blockade readout [34], [35]. Energy-selective readout (or Elzerman readout) places the energy level of a neighbouring electron reservoir in-between the energy levels of the qubit, such that only one (the higher energy state, generally spin-up) of the spin-states can tunnel out of the quantum dot. This removal of an electron in the spin-up state leaves a vacant energy level, that is subsequently filled with a new electron in the ground state coming from the reservoir, leading to a transient "blip" in quantum dot charge, see the upper half fig. 2,a. On the other hand, if the spin is in the ground state the electron will stay in the quantum dot and no exchange with the reservoir takes places, thus the charge signal is expected to be flat, see the lower half fig. 2,a. Since the processes of tunneling in and out of the reservoir are probabilistic in nature, the duration of the "blip" can be statistically modified by adjusting the tunneling rate, yet the exact duration and position remain unpredictable. This method has been demonstrated to yield high fidelities [36], but it presents technical difficulties for scaling to large quantum processors, as it requires sub-K operating temperatures and complex interfacing electronics. First, this protocol is not robust against temperature: the energy level of the electron reservoir smears out rapidly with temperature, increasing the probability of tunneling of spin-down and thus increasing false-positives detection, decreasing the fidelity of the spin-to-charge conversion. Second, the uncertainty in the blip's timing implies the need for both a high sampling rate of the electrometer and performing detection algorithms on the resulting data.

Alternatively, in the PSB protocol, two electrons residing in two different quantum dots are used, this readout process is depicted in fig. 2,b. The spin-to-charge conversion is obtained thanks to the inability of electrons to occupy the exact same quantum state, i.e., the same spin-state and same orbital state in a single quantum dot. Thus, when one tries to combine two electrons of different spin-state in the same quantum dot, tunnelling happens and both electrons end up together. If the electrons are in the same spin states, however, they do not tunnel and remain in their own dots. The transition is "blockaded". Two flavors of PSB exist, known as Singlet-Triplet readout and Parity readout [37], both leading to the same pattern of charge signal. As during PSB no electrons need to be exchanged with the reservoir, the process is comparatively more robust against temperature [3], which is a crucial advantage. Moreover, the signal is much more predictable than with Elzerman readout: PSB generates a charge step response that rises at a known time. Although the

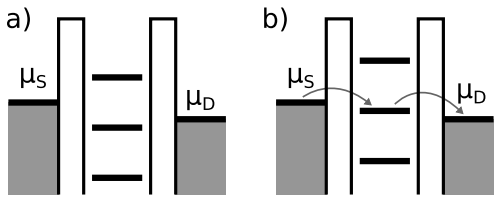


Fig. 3. SET operating principle (adapted from [16]): a) Coulomb blockade, b) single-electron transport through the dot.

duration of the signal is still governed by Poisson statistics, it is typically very long, given the lifetime of the blockaded state (typically milliseconds or more). A drawback is that, since no electrons are removed from the system (only reconfigured), the effect on the electrometer is generally weaker, and the detection, therefore, is made more challenging.

B. SET DC Characteristics

The quantum chip's overall design is such that significant capacitive coupling between the double-dot and the SET is present, depicted in the schematic of Figure 1b). The number of trapped electrons on the SET and the conductance through it can be manipulated by five control voltages: the plunger voltage (P_S) controlling the electrochemical potential of the dot and, therefore, the electron occupation number; the two barrier voltages ($B_{s,1/2}$) controlling the tunnel-barrier resistance in and out of the island; and the reservoir voltages (S, D). Due to close proximity, significant capacitive crosstalk exists between the different control voltages and the barriers/dots. Relating the SET to an NFET, we refer to the reservoir contact at lower/higher potential as source/drain, respectively, and to the plunger as a gate.

For a sufficiently small charge island Q_S, the available electrochemical potential levels on the island are spaced by the charging energy $E_C = e^2/C$, where C is the island's capacitance [38]. When a small bias window is opened between the source and drain terminals of the SET, if none of the quantized electrochemical potential levels is positioned between the lead potentials, no current can flow, the SET is in "Coulomb blockade" [fig. 3 a)] and the number of bound electrons remains fixed. If there is a level available, however, single electrons can flow through the quantum structure via the available energy state, resulting in a measurable current [fig. 3 b)]. A typical measurement to characterize the SET is shown in fig. 4 a). The data underlying this and other figures is available under [39]. Clearly visible are the parallelograms with blockaded transport, termed "Coulomb diamonds" [16]. If the bias window becomes large enough, the SET cannot be found in a blockaded state anymore. In fig. 4 b), we show a cut at fixed bias through the measured characteristic, that clearly presents Coulomb blockade regions and peaks (fig. 3 a) and b) respectively, as noted in the figure). To optimize the performance of SETs as electrometers, they are usually operated at a low-bias regime where bias-broadening effects are minimized and the steepness of the peaks maximized [16]. The SET is biased around the most responsive region of the Coulomb peak, indicated by the bias current, I_B in Figure 4b). In this specific configuration, the movement of a single electron between $Q_{1/2}$ is enough to cause a change in the SET's current levels $I_{s,0/1} = I_B \pm I_s$, that can be associated

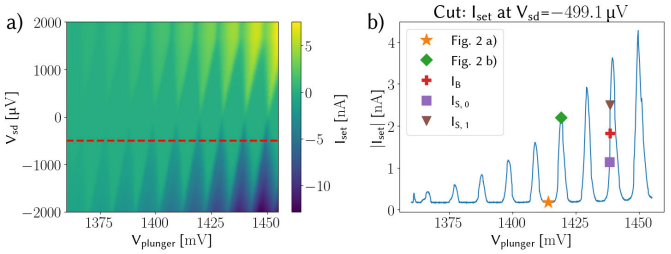


Fig. 4. a) Measured SET large signal characteristics, b) slice of characteristic for specific V_{sd}, indicating the operating modes in fig. 3 and an example for the bias points in fig. 5. Device is cooled to ≈15 mK and measures an effective electron temperature of ≈80 mK.

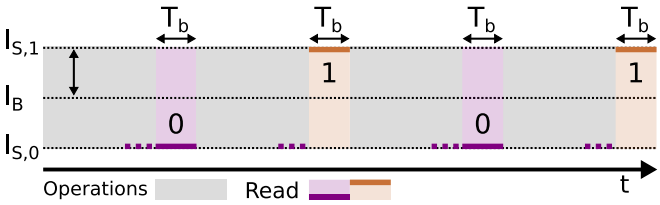


Fig. 5. SET current evolution in the readout pulse sequence.

with the corresponding spin-states via the previously discussed spin-to-charge conversion. For a detailed review of the SET operation and spins in quantum dots, the reader is referred to [16] and [38].

C. SET Readout Pulse Sequence

As briefly explained above, during PSB readout, the quantum dots are pulsed into a spin-dependent electron configuration for a finite duration of readout time, T_b. The SET current is measured during this time and registers the charge configuration change thanks to the capacitive coupling to $C_{QS,Q1/2}$ by assuming the value $I_{s,0/1}$, respectively. We assume the ideal PSB in the following, which means no decay of the blockaded states occurs during the SET acquisition time, such that the readout signal appears as a step.

Before and after the readout times, information processing in the quantum dots is executed. This processing encompasses a combination of fast bias-pulses on the gates defining the qubits, combined with microwave pulses. The pulses used to perform operations do generally not target single electrodes, but "virtual gates" that combine the effect of multiple electrodes [40]. The SET's plunger is often included in this virtualization due to its large capacitive coupling to the quantum dots. Due to the movement of electrons in the vicinity of the sensor and due to transient bias changes, the sensor current can, therefore, fluctuate prior to the readout phase, indicated by the grey areas in fig. 5. This is important for the interfacing read-out circuit as either the circuit needs to be able to cope with these sensor signal variations prior to readout, or the SET needs to be configured in the blockaded regime during qubit operation, where it is relatively insensitive to changes in its electrostatic surroundings. Depending on the choice of operation sequence, the sensor might also put out a well-defined zero level before the pulse, indicated by a dotted zero line before T_B in fig. 5. While this increases the necessary measurement time, this can provide some rejection for the low-frequency noise by employing correlated-double sampling techniques.

D. Noise in SET Devices

The SET intrinsically generates shot noise as discussed in [41] and tested experimentally [42]. In this work, we operate significantly below the transition frequency [41] (≈2 GHz for the lowest typical bias of interest for our target application I_B≈100 pA), such that a white shot noise power spectral density (PSD) can be assumed:

$$S_N^2 = 2qFI_{SET} \tag{1}$$

where q is the elementary charge, F is the Fano factor [43] and I_{SET} is the SET current. The value of the Fano factor F, also called the shot-noise suppression factor, was measured to be between 0.5 - 1 [42]; thus, for the rest of this work, we adopt a value of 1 as a conservative estimate. The intrinsic, unavoidable shot noise sets the lower limit on the SET noise.

In addition to the broadband noise, SETs are also affected by low-frequency charge noise with 1/f shape [44], [45]. This charge noise is dependent on temperature [46], with higher temperatures corresponding to higher charge noise. The charge noise is converted to a current by the SET IV characteristic. Furthermore, single traps, which can be described as two-level systems, can be strongly coupled to the sensor and cause random telegraph noise (RTN). Such strongly coupled traps cause Lorentzian shapes in the noise spectrum to rise above the 1/f background. In the following analysis, we assume the noise to be dominated by 1/f, but we comment on the possible effects of RTN in the design section.

Summarizing, the intrinsic SET single-sided power spectral density can be modeled as a combination of shot and 1/f noise:

$$S_{N,SET}(f) = 2\ qFI_{SET} + \frac{S_{LFN,f=1\,\mathrm{Hz}}}{f^{\alpha}} \tag{2}$$

with $S_{LFN,1\,\mathrm{Hz}}$ the low-frequency noise at $f = 1$ Hz and $\alpha \approx 1$ the low-frequency noise slope. $S_{LFN,1\,\mathrm{Hz}}$ is typically measured at the maximum conductance point, and, assuming a first-order model, can be scaled by the device transconductance in other operating points (op): $S_{LFN,1\,\mathrm{Hz},op} = S_{LFN,1\,\mathrm{Hz},max}\frac{g_{m,op}}{g_{m,max}}$. Typical values for $S_{LFN,1\,\mathrm{Hz}}$ lie between $10^{-23}\,\mathrm{A^2\,Hz^{-1}}$ to $10^{-24}\,\mathrm{A^2\,Hz^{-1}}$.

E. SET Model for Design

For developing the electrical interface, a small-signal model (SSM) of the SET setup as shown in fig. 6 is employed. Typical values for the parameters of the SSM are reported in table I. As detailed above, the SET produces a qubit-state-dependent current swing I_s around a bias I_B. The signal amplitude I_s is highly dependent on the coupling of the quantum dot to the sensor, the temperature and the bias conditions. For a practical readout, we assume a typical value of 300 pA, as commonly reached in experimental practice. In parallel with the qubit-dependent current, the setup model includes the setup capacitance C_S and resistance R_S. $C_S = C_p + C_{SET}$ is typically dominated by the parasitic capacitance C_p of the interconnect between the SET and the first-stage amplifier. The intrinsic C_{SET} is extremely small, and corresponds to a diffusion capacitance in a MOSFET, setting a lower bound of C_S in the order of fF, which is only achievable if co-integrating the qubits and the readout. If the SET and the amplifier are mounted on different temperature plates of a dilution refrigerator or even at room temperature as in [47], the long (≈1 m) coaxial interconnection can result in large capacitance (≈100 pF). The quoted typical $C_S = 2$ pF is estimated based on a two-chip configuration with ESD protection on both sides and direct chip-to-chip bonding. In some practical amplifier structures, the amplifier input capacitance will also add significant additional capacitance on the input node. The SET output resistance R_{SET} and setup parasitic resistance R_P define the output resistance. Typically R_{SET} dominates the setup resistance R_S.

TABLE I
MODEL PARAMETERS

Parameter	Typical	Range
I_s	300 pA	100 pA to 500 pA
I_B	1 nA	0.3 nA to 5 nA
R_S	133 kΩ	30 kΩ to 1000 kΩ
C_S	2 pF	10 fF to 100 pF
F	1	0.5 to 1
$I_{LFN,f=1\,\mathrm{Hz}}$	-	$10^{-23}\,\mathrm{A^2\,Hz^{-1}}$ to $10^{-24}\,\mathrm{A^2\,Hz^{-1}}$

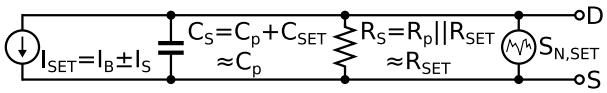


Fig. 6. Simplified SET electrical model.

III. CRYOGENIC ELECTRONICS

Figure 7 shows the measured device characteristics of a typical 40 nm CMOS process that forms the basis of the numerical estimations in this paper. A higher threshold voltage, a steeper sub-threshold slope, and a significantly increased g_m/I_d are observed, like reported in [48], [49], and [50]. Specifically, the increased g_m/I_d in weak inversion offers significant benefits for power-efficient low-noise design, however, limited by changes in the subthreshold slope leading to large variability in this regime [51]. The threshold voltage can, also in bulk technologies, be influenced by a wide range of body-bias voltages [52]. The gate-tunneling-current is, to first order, unchanged [53]. The low-frequency noise (LFN) changes when moving to cryogenic temperatures, as reported in [54], but the general amplitude of the change is often small compared to the device-to-device variability of the LFN. White noise in MOS transistors has been reported not to scale as thermal noise, but rather seems to approach a lower limit set by shot noise [55]. Possible causes for the increased noise might also be found in self-heating in CMOS [56]. As limited white noise modeling and characterization are available, we pragmatically adopt an effective (non-necessarily physically justified) thermal temperature of the MOSFET of 150 K for the noise in active devices for the reference 40 nm technology, in line with the improvement observed in comparator measurements done in the same technology [57]. This reduced scaling, however, is so far only shown in devices in saturation. If the transistors are operated in triode, the resistive channel noise is expected to scale with temperature. In the absence of current, also no shot noise is produced. As a result, sampling kT/C is expected to scale with temperature,

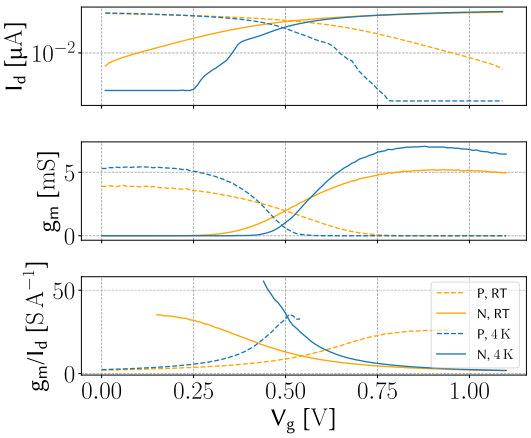


Fig. 7. Measured DC characteristics at room temperature and 4.2 K of W/L = 6 × 1.2 µm/100 nm NMOS and W/L = 6×2.4 µm/100 nm PMOS: a) I_d, b) g_m and c) g_m/I_d. All measured with V_{ds}=550 mV, NMOS/PMOS source voltage at 0/1.1 V.

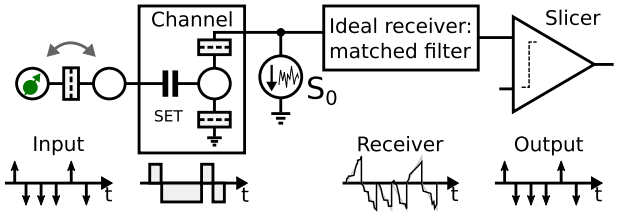


Fig. 8. Sketch of the idealized readout sequence: upon an impulse input, the channel produces current pulses based on the bit polarity alongside white noise with spectral density S_0. A matched-filter receiver integrates the signal current plus noise and a slicer recovers the bitstream.

suppressing it sufficiently to make it negligible for many of the architectures considered in the following.

Another promising technology for the implementation of cryogenic amplification is SiGe BiCMOS processes, as the SiGe BJTs show very high current gains at cryogenic temperature [58], and the associated g_m/I_d is much larger than achievable in CMOS. Discrete SiGe BJTs have been used in readout designs [23], enabling a very low power consumption, that is unlikely to be achievable with CMOS. While SiGe does offer superior noise performance, it is also significantly more difficult to co-integrate technologically. For this reason, this work focuses on a CMOS design.

IV. DC-Readout at the Shot Noise Limit

In this section, we explore the intrinsic SNR limits when reading an SET used as a charge sensor for the case of a PSB-type readout, see fig. 8. The information about the qubit spin states $b_i = \pm 1$ is modeled as a train of impulses $W_b(t)$ each separated by the bit period T_b:

$$W_b(t) = \sum_{i=0}^{\infty} b_i \delta\left(t - iT_b\right) \tag{3}$$

This neglects the spacing of readout pulses due to operations, as shown in fig. 5, but without loss of generality in describing the readout itself. As discussed in section II-C, the sensor reacts to this information with current pulses for each bit, describable by a communication channel with impulse

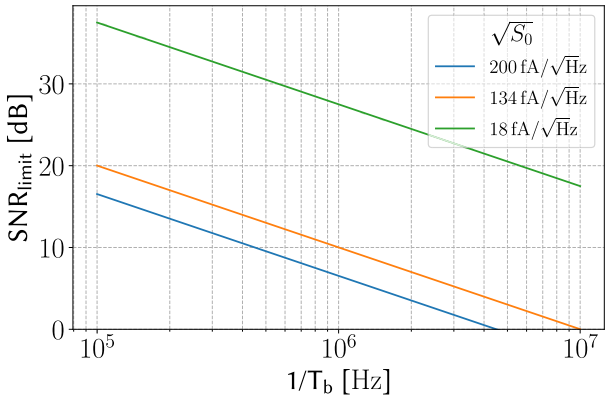


Fig. 9. Ideal receiver assuming a signal amplitude of $I_{SET} = 300$ pA and a range of noise densities S_0.

response $s(t)$:

$$s(t) = I_s\left(u(t) - u(t - T_b)\right) \tag{4}$$

with I_s the SET signal current swing and $u(t)$ the Heaviside step function. In an idealized case of manufacturing SETs with little oxide defects, the low-frequency noise is negligible, and only white noise needs to be considered. Furthermore, white noise may become dominant for the large readout bandwidth targeted in this work, while low-frequency noise can be compensated using typical dynamic compensation techniques, as for example correlated double sampling [59]. Under this assumption, the ideal filter for extracting the information from this channel is a matched filter [60]. The matched filter impulse response $h(t)$ is obtained from the channel impulse $s(t)$ by time-reversal and shifting by the bit period T_B:

$$\begin{aligned} h(t) &= s(T_B - t) = u(T_b - t) - u(T_B - t - T_B) \\ &= u(t) - u(t - T_b) \end{aligned} \tag{5}$$

This matched filter represents an ideal integrator with reset. Without loss of generality, we can assume that the integration is done on a capacitor C_R. The output signal provided to the bit slicer at the moment of making the i*th* decision can now be written as:

$$V_{out}(T_i) = \int_{(i-1)T_b}^{iT_b} \frac{\pm I_s}{C_R} dt = \pm \frac{I_s T_b}{C_R} \tag{6}$$

Noise analysis can now be performed with the methodology in [61], given the receiver impulse response and the single-sided noise spectral density $S^2_{N,SET}(f) = S_0$. The integrated noise at the time of slicing can then be calculated as:

$$n(t = T_i) = \frac{1}{2} S_0 \int_0^{T_b} |h(t)|^2 dt = \frac{S_0}{2C_R^2} T_b \tag{7}$$

Without loss of generality, for a memory-less system, we assume $i = 0$ in the following, such that evaluation happens at time $t = T_b$. The ideal white-noise limited SNR of DC-readout is then:

$$SNR_{limit} = \frac{V_{out}(T_b)^2}{n(T_b)} = \frac{\frac{I_s^2 T_b^2}{C_R^2}}{\frac{S_0}{2C_R^2} T_b} = \frac{2I_s^2 T_b}{S_0} \tag{8}$$

Solving for the current-noise density, we gain a specification

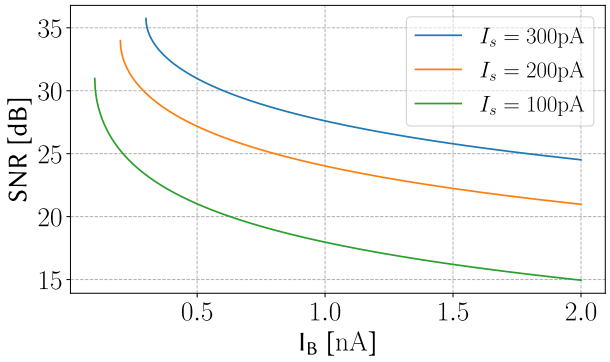


Fig. 10. SNR limit for $T_b = 1\,\mu$s, slicing level for equal SNR on both bits.

for a given SNR in the case of an ideal receiver:

$$\sqrt{S_0} = \sqrt{\frac{2I_s^2 T_b}{SNR}} \tag{9}$$

If, for example, assuming the typical values given in table I, this results in a requirement of better than $134\,\text{fA}/\sqrt{\text{Hz}}$ for the input-referred noise of the integrator if targeting an SNR of 10 dB with $T_b = 1\,\mu$s. For the values in table I, we plot eq. (8) in fig. 9, assuming a selection of noise densities.

A limiting case is reached if we consider that the *only* contribution to S_0 is the shot noise generated by the SET itself, assuming an otherwise noiseless readout. The signal swing I_s is around bias point I_B, such that the total current $I_{SET,\pm} = I_B \pm I_s$. For shot noise, we now have $S_0 = 2qI_{tot}$, which would result in a symbol-dependent SNR, as $I_{SET,\pm}$ varies with symbol. For the requirement of equal SNR for both symbols, the slicing level needs to be closer to the signal level with lower noise. This results in the limit on the average equivalent SNR of:

$$SNR_{shot} = \frac{4I_s^2 T_b}{q\left(\sqrt{I_B - I_s} + \sqrt{I_B + I_s}\right)^2} \tag{10}$$

For the typical values reported in table I, this limit is equivalent to the $\sqrt{S_0} = 18\,\text{fA}/\sqrt{\text{Hz}}$ case plotted in fig. 9, forming the fundamental limit under this signal level. To explore the effect of bias on the SNR limit, we evaluate SNR_{shot} over I_B for various I_s in fig. 10, keeping $T_b = 1\,\mu$s. A maximum occurs for a bias equal to the signal level, corresponding to no current when transmitting one of the symbols. This has a physical interpretation: if for one of the symbols the SET is in Coulomb blockade, only minimal second-order currents flow. When minimal current flows, also the intrinsic noise is minimal, allowing a slicing level very close to this bit value maximizing the overall SNR. In practical scenarios, this limit may not be optimal because the signal current swing $\pm I_s$ typically decreases with lower bias. This is illustrated in fig. 4: if lowering I_B, the peak is not intercepted at its steepest point anymore. The reduction in signal current reduces the SNR of the SET gained biasing in this regime, but most importantly it aggravates the noise constraints on the receiving circuit that are discussed in the following section.

V. Practical Front-End Requirements

To approach the limits set in the previous section in practice, we analyze and benchmark four readout strategies in the following sections: voltage-mode, current-mode with a TIA, charge-sampling, and current pre-amplification. In voltage-mode readout (fig. 11 a)), the SET is biased with a current, in current-mode (fig. 11 b)) with a voltage, while the other quantity is read, respectively. As a special case of current-mode readout, charge sampling (fig. 11 c)) is discussed separately, as it is functionally close to the optimal matched filter in section IV. Finally, the current pre-amplifier (fig. 11 d)) grants a current gain with low input and high output impedance, which in practice must be followed up by a voltage- or current-mode detection circuit.

In the discussion of these readout methods, emphasis is placed on the challenges arising in their practical implementation. Design examples are carried out with the target of the first stage, limiting the output SNR to 10 dB for a 1 µs integration time. Of course, to get a 10-dB SNR for the overall detection chain, the noise of the first stage must be decreased, but the same design equations can be adopted for the specific choice of follow-up stage without loss of generality. Further, we assume negligible low-frequency noise, requiring either sufficiently large sizing of the input transistors for this to hold, or cascading the readout with a correlated double sampling (CDS) stage [59]. If a CDS stage is used, however, the requirements on the broad-band noise become more stringent, as this noise is now sampled twice. For the remainder of this work, we assume that the amplifiers are operated in a 4 K environment.

A. Voltage Amplifier

At the core of a voltage-mode readout, see fig. 11 a), the SET is biased with a current, the signal current integration is done on the setup capacitance C_S and the output is sliced after amplification. This core setup deviates from the ideal case discussed above as now the amplifier has a high input impedance. One example of such an amplifier with high input impedance can be found in the SiGe bipolar design in [23], as the low-bias HBT has a large base resistance $r_\pi \gg R_s$. Therefore, all impedances connected to the SET node, indicated in fig. 6, need to be considered: both the lumped parasitic capacitance C_S and resistance R_S.

For the purpose of this analysis, we also assume an inter-symbol reset or settling during the operations, resulting in no channel memory. The input system constitutes a leaky integrator, with impulse response:

$$h(t) = \frac{1}{C_S} e^{-\frac{t}{\tau_s}} u(t) \tag{11}$$

with the time constant $\tau_s = R_S C_S$. For the signal, we then get period T_b:

$$s * h|_{t=T_b} = R_s I_s \left(1 - e^{-\frac{T_b}{\tau_s}}\right) \tag{12}$$

The noise power from the SET is now filtered by the leaky integrator, and can be calculated with the same method as applied in the derivation of eq. (7):

$$n^2(t = T_b) = \frac{\tau S_{n,SET}}{4C_S^2}\left(1 - e^{-\frac{2T_b}{\tau_s}}\right) \tag{13}$$

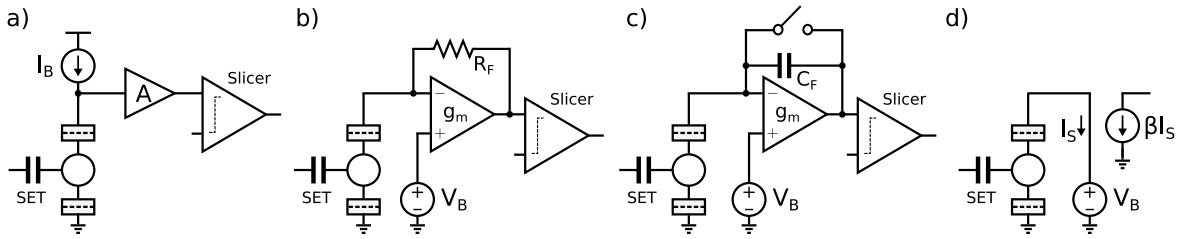


Fig. 11. Amplifiers considered here: a) voltage amplifier, b) transimpedance amplifier, c) charge-based amplifier, d) current pre-amplifier. The SET symbol is for all following analyses replaced by the small-signal model in fig. 6.

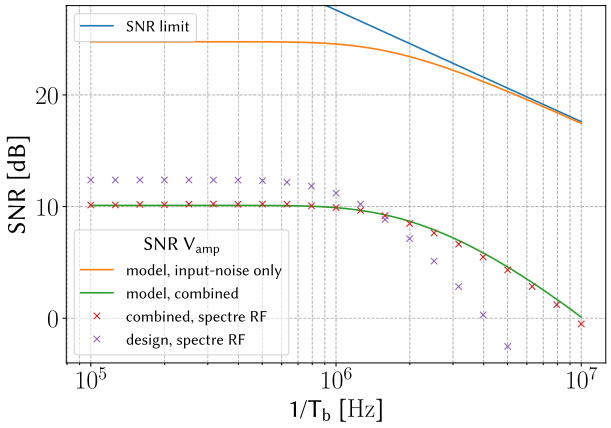


Fig. 12. SNR of the voltage amplifier in model calculations and spectre RF simulations, compared to the SNR limit.

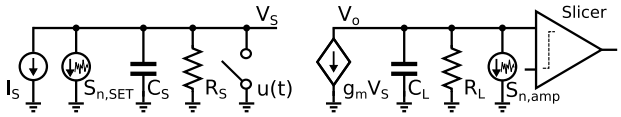


Fig. 13. Voltage-based amplifier small-signal model.

This noise needs to be combined with the RMS noise of the voltage amplifier $V^2_{n,a,rms}$:

$$SNR_V = \frac{(s * h(t = T_b))^2}{n^2(t = T_b) + V^2_{n,amp,RMS}} \tag{14}$$

$$= \frac{R_S^2 I_s^2 \left(1 - e^{-\frac{T_b}{\tau_s}}\right)^2}{\frac{R_s S_{n,SET}}{4C_S}\left(1 - e^{-\frac{2T_b}{\tau_s}}\right) + V^2_{n,amp,rms}} \tag{15}$$

In fig. 12, we plot the achievable SNR over $1/T_b$ for the typical parameters from table I and compare two special cases: $V^2_{n,a,rms} = 0$ and $V^2_{n,a,rms} = 1.5 \times 10^{-10}\,\mathrm{V}^2$. First, without amplifier noise, the SNR saturates for low readout speeds as the resistive input leakage limits the integrated signal, while for high speeds, the ideal limit is approached (model, input-noise only). In the second case, the amplifier noise amplitude has been chosen such that the SNR target of 10 dB can be reached for a 1 µs integration time (model, combined). The calculation is benchmarked against a simulation using ideal components in Spectre RF, demonstrating a close match (combined, spectre RF). In the following, we replace the abstracted amplifier with a more realistic model.

The amplifiers current noise $S_{i,n,a}$ can be modeled by:

$$S_{n,i,a} = 4kT\gamma\eta_{curr} g_m \tag{16}$$

where k is the Boltzmann constant, γ a noise non-ideality factor specific to the technology, η_{curr} the amplifiers current efficiency factor [62] and g_m the amplifier transconductance. Assuming the small signal noise model of fig. 13, the output voltage noise density at DC due to the amplifier alone is:

$$V^2_{n,o} = 4kT\gamma\eta_{curr} g_m R_L^2 \tag{17}$$

With the equivalent noise bandwith $NBW_V = \frac{1}{4\tau_a} = \frac{1}{4R_L C_L}$, the amplifier output noise is the classic kT/C result:

$$V^2_{n,amp,rms} = \frac{kT\gamma\eta_{curr} g_m R_L}{C_L} \tag{18}$$

It is important to note that this expression only holds for the settling case in which $T_b \gg \tau_a$, with $\tau_a = R_L C_L$ [61]. Referring this to the input by approximating the amplifier gain with $A \approx A_{DC} = g_m R_L$ and using eq. (15) under the assumption that the SNR is dominated by the amplifier noise, we gain a specification for the necessary capacitance:

$$C_L = \frac{kT\gamma\eta_{curr}}{A_{DC} R_S^2 I_S^2 (1 - e^{-\frac{T_b}{\tau_s}})^2} SNR_V \tag{19}$$

For this to be sufficient, g_m needs to be large enough to guarantee the required A at the symbol rate:

$$g_m = \frac{A\sqrt{1 + \omega^2 C_L^2 R_L^2}}{R_L} \approx A\omega C_L \tag{20}$$

With $\omega = 2\pi/T_b$, the last approximation holding only for a marginally settling design. For minimizing the necessary capacitance, the gain A needs to be maximized, while for minimizing the needed g_m in turn the output impedance needs to be maximized, thereby requiring the output stage to move towards current integration.

Assuming a target gain of $A = 100$, a current efficiency factor of $\eta_{curr} = 2$, a target SNR of 10dB, a bit period of $T_b = 1\,\mu\mathrm{s}$ and a MOSFET noise temperature of 150 K we gain: $C_L = 272\,\mathrm{fF}$, $g_m = 170\,\mu\mathrm{S}$. This design is then simulated alongside the ideal model in fig. 12 (design, Spectre RF),[1] showing a slight overdesign caused by the simplifying assumptions. The load resistance in the simulation $R_L = 1\,\mathrm{M}\Omega$ is chosen to be implementable with MOSFETs. To approximately estimate the area occupation of each readout, we consider the necessary load capacitor as well as the other active and passive circuits necessary for each implementation. The load capacitor can be implemented with MOS transistors,

[1]Since the simulations, here and in the following, are used to verify the analytical estimations, the exact schematics shown in the readout figures, e.g., fig. 13, are simulated, adopting the small-signal model of active devices and not employing any transistor device model.

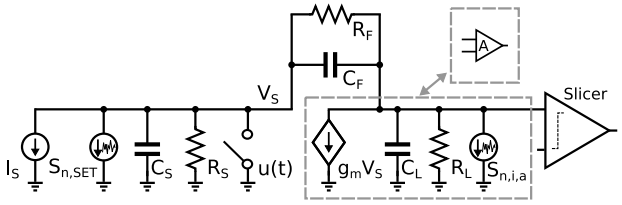


Fig. 14. Transimpedance amplifier small signal model.

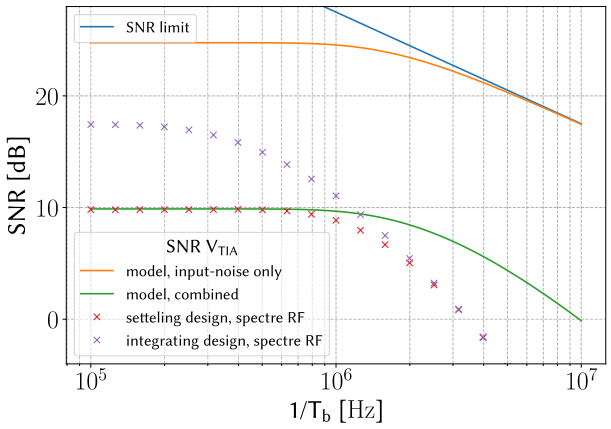


Fig. 15. SNR of the TIA in model calculations and spectre RF simulations, compared to the SNR limit.

with, e.g., $\approx$10 fF µm^{-2} in 40 nm CMOS. Additionally, the active circuitry is estimated to contribute an area of 50 µm^2 per amplifying transistor (100 µm^2 for each differential pair), including the biasing transistors. For the voltage amplifier, being a single-ended circuit, this leads to 77 µm^2.

This discussion of the voltage amplifier further assumed that the SET current is not majorly affected by the voltage swing at the amplifier input, i.e., at the SET drain. In general, this can be violated: in our measurement data, the SET would significantly change its output characteristics if experiencing just a 50 µV swing (the numerical example above would correspond to a settled swing of $\pm$40 µV). An improved sensor design, demonstrated in [63], can increase the sensor's output impedance significantly and increase the voltage range over which a stable current can be supplied to 3 mV.

B. Transimpedance Amplifier

The current-mode front-end in form of a TIA is shown in fig. 11 b). If $R_F \to \infty$, $C_F \to 0$, the TIA model reduces to the voltage amplifier in fig. 11 a). Here we concentrate on cases far from this limit, where full treatment of the TIA transfer function is necessary.

In a settled TIA design, the low-frequency transconductance is set by the feedback resistor R_F. The settling also implies that the signal is not integrated, deviating functionally from the ideal receiver in section IV.

To quantitatively evaluate the TIA, we analyze the small-signal model shown in fig. 14. If attempting a full direct solution, the corresponding equations are unsuitable for analytical estimations. Therefore, we divide the problem into two separate parts: First, we examine the effect of SET noise in the TIA; then we look at the noise of the amplifier itself. For analyzing the effect of SET noise, we replace the amplifier model in fig. 14 with a voltage amplifier with gain A_T. The impulse response of the TIA now becomes:

$$h(t) = \frac{A_T}{(1+A_T)C_F + C_S} e^{-\frac{R_F+(1+A_T)R_S}{((1+A_T)C_F+C_P)R_F R_S}t} u(t) \quad (21)$$

The signal amplitude at the time of slicing ($t = T_b$) is then:

$$s * h|_{t=T_b} = \frac{I_s R_F R_S A_T}{R_F + (1+A_T)R_S} \left(1 - e^{-\frac{R_F+(1+A_T)R_S}{((1+A_T)C_F+C_S)R_F R_S}T_b}\right) \quad (22)$$

Following the approach previously detailed for the voltage amplifier, the output noise due to the SET noise is:

$$n^2(t=T_b) = \frac{A_T^2 R_F R_S}{2((1+A_T)C_F + C_S)(R_F + (1+A_T)R_S)} \cdot \left(1 - e^{-\frac{R_F+(1+A_T)R_S}{((1+A_T)C_F+C_S)R_F R_S}T_b}\right) S_{N,SET} \quad (23)$$

The SNR is therefore:

$$SNR_{TIA} = \frac{s * h(t=T_b)^2}{n^2(t=T_b) + V_{n,rms,TIA}^2} \quad (24)$$

where $V_{n,rms,TIA}^2$ is the RMS noise of the TIA structure. We conservatively assume that the TIA is compensated for a flat response, with $C_F = \frac{R_S}{R_F} C_S$. The value of the feedback resistor R_F is mostly defined by the swing requirements of the following stage, as the resistor noise benefits fully from the temperature scaling. To reach for example an output peak-to-peak swing of 1 mV, we require a resistance of at least 1.7 MΩ, significantly exceeding the minimum resistor necessary to keep the resistor noise below the specifications ($\approx$49 kΩ@4 K would be required for a 50% contribution to the total noise). Such a resistor could either be implemented as an unsilicided n-type polysilicon resistor ($\approx 50 \times 50$ µm) or implemented with active devices in subthreshold. Evaluating eq. (23) for the case of no amplifier noise in fig. 15, we see that the TIA, if settled, drops significantly below the limiting ideal performance, but approaches it in the high-frequency limit in which the input current is integrated on the feedback capacitance (model, input-noise only). The influence of the amplifier gain A_T on SNR performance is small and for the evaluation it was assumed to be 100. Any practical amplifier, however, shows noise of its own. We show the combined performance with an amplifier noise of $V_{n,rms,TIA}^2 = 1.2 \times 10^{-7}$ V^2, which would limit the SNR to the 10dB target at $T_b = 1$ µs (model, combined). In the following we design an amplifier for the settled TIA case.

For tractable design equations, we again assume $C_F = \frac{R_S}{R_F} C_S$. For this case we have for the noise bandwidth of the TIA:

$$NBW_{TIA} \approx \frac{g_m}{4(1+\alpha)C_L} \quad (25)$$

where $\alpha = \frac{R_F}{R_S}$ and we assumed $\frac{1+\alpha}{g_m} \ll R_F + R_S$. The corresponding DC voltage noise density is, with the same amplifier current noise model as in eq. (16) for $S_{n,i,a}$:

$$S_{n,v,TIA} = \left(\frac{1+\alpha}{g_m}\right)^2 4kT\gamma\eta_{curr} g_m \quad (26)$$

Combining this with eq. (25) results in:

$$V_{n,rms,TIA}^2 = \frac{(1+\alpha)kT\gamma\eta_{curr}}{C_L} \quad (27)$$

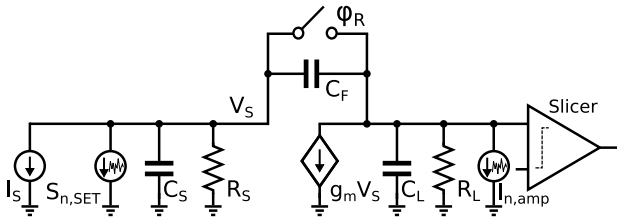


Fig. 16. Charge-based front-end.

Now assuming a settled output signal $V_{sig} = R_F I_s$, the output SNR is:

$$SNR_o = \frac{V_{sig}^2}{V_{n,rms,TIA}^2} = \frac{R_F^2 I_s^2}{V_{n,rms,TIA}^2} \tag{28}$$

The necessary output capacitance is then derived as

$$C_L = \frac{(1+\alpha)kT\eta_{curr}}{R_F^2 I_s^2} SNR_o \tag{29}$$

To calculate the necessary bandwidth, we approximate the input transfer characteristic with its dominant pole:

$$\frac{V_o}{I_{in}} \approx \frac{R_F}{1 + \frac{(C_L+C_S)R_S + C_L R_F}{g_m R_S} s} \tag{30}$$

The finite bandwidth causes a settling error E, setting a requirement on g_m:

$$g_m \approx \frac{(C_L + C_S)R_S + C_L R_F}{T_b R_S} \ln \frac{1}{E} \tag{31}$$

This estimation slightly underestimates the necessary conductance, as it neglects the effects of the input pole.

For a $R_F = 1.7\,\mathrm{M\Omega}$ and assuming a MOSFET noise temperature of $T = 150\,\mathrm{K}$, a $\eta_{curr} = 4$ for the amplifier and a settling error of $E = 2\%$ to be acceptable, we obtain $C_L = 4.4\,\mathrm{pF}$ and $g_m = 244\,\mu\mathrm{S}$. This TIA design corresponds to an area consumption of $540\,\mu\mathrm{m}^2$, following the estimation in section V-A, if implementing the resistor with active devices. When using a polysilicon resistor, the area estimation increases to $\approx 3000\,\mu\mathrm{m}^2$. The simulated behavior with the typical parameters in table I is shown in fig. 15, demonstrating that a settling TIA falls just short of the design target, due to the influence of the neglected second pole. However, if changing to a non-settling design by increasing the feedback resistance to $R_F = 10\,\mathrm{M\Omega}$ and keeping the same g_m and C_L parameters, the integrating design exceeds the target specifications as seen in fig. 15.

There is an important caveat of the non-settling TIA design: if resetting the input capacitance $C_S = 2\,\mathrm{pF}$ via $R_F = 10\,\mathrm{M\Omega}$, the reset time constant is $20\,\mu\mathrm{s}$, leading to significant inter-symbol interference. This issue could be addressed either via an adaptive time constant for resetting or by replacing the resistor by a switch. The latter approach leads to the charge-based amplification outlined in the following section.

C. Charge-Based Amplifier

To come close to the ideal matched-filter-based readout strategy, we can use a charge-integration structure, as shown in fig. 11 c). For the purpose of making this analysis analytically tractable, we will for now assume both R_L and R_S to be very large in the circuit in fig. 16. Under this assumption, the impulse response $h(t)$ of the circuit in fig. 16 is:

$$h(t) = \left(\frac{1}{C_F} - \frac{(C_F + C_L)(C_F + C_S)}{C_L C_S C_F + C_F^2 (C_L + C_S)} \cdot e^{-\frac{C_F g_m}{C_L C_S + C_F (C_L + C_S)} t} \right) u(t) \tag{32}$$

By convolution with the input step, we gain the output signal:

$$s * h(t = T_b) = \frac{I_s}{C_F} \left(T_b - \frac{(C_F + C_L)(C_F + C_S)}{C_F g_m} \cdot \left(1 - e^{-\frac{C_F g_m}{C_L C_S + C_F (C_L + C_S)} T_b} \right) \right) \approx \frac{I_s T_b}{C_F} \tag{33}$$

The approximation holds for sufficient settling of the integration loop, i.e., for a sufficiently large g_m. The SET input noise integration can be computed from the impulse response as done in the previous section, but in the interest of space, we approximate it here by assuming full integration of the noise.

In this noise analysis, we follow the methodology described in [64] and divide the operation into two phases: the reset phase (R) and the integration phase (INT). In the reset phase we can simplify the circuit by assuming C_F to be shorted, assuming that the switch conductance is sufficiently large. In this case, the transfer function for the SET and amplifier noise to the output during the R-phase (noting that the noise sources are in parallel with the reset switches closed) is:

$$H_{n,R}(s) = \frac{\frac{1}{g_m}}{1 + s\frac{1}{g_m}(C_S + C_L)} \tag{34}$$

As the equivalent noise bandwidth is $NBW = \frac{g_m}{4(C_S + C_L)}$, the total noise during the R-phase is:

$$V_{n,R,RMS}^2 = \frac{1}{4 g_m (C_S + C_L)} (I_{n,amp}^2 + S_{n,set}) \tag{35}$$

This noise is re-distributed to the feedback capacitor during the integration phase with the ratio $\alpha = \frac{C_S}{C_F}$. During the INT-phase the switch in fig. 16 is an open, resulting in the noise

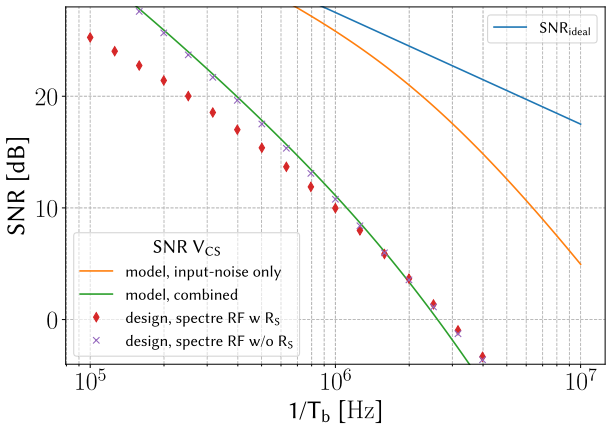


Fig. 17. SNR of the charge-based amplifier in model calculations and spectre RF simulations, compared to the SNR limit.

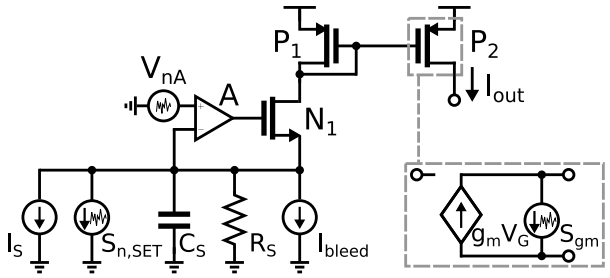


Fig. 18. Current pre-amplifier CMOS implementation.

transfer function:

$$H_{n,INT} = \frac{\frac{1+\alpha}{g_m}}{1 + s\frac{1+\alpha}{g_m}\left(\frac{\alpha}{1+\alpha}C_F + C_L\right)} \tag{36}$$

Therefore the settled noise in the INT-phase is:

$$V^2_{n,INT,RMS} = \frac{(1+\alpha)I^2_{n,amp}}{4\left(\frac{\alpha}{1+\alpha}C_F + C_L\right)g_m} + \frac{S_0}{2C_F^2}T_b \tag{37}$$

where we use eq. (7) for the SET noise integration. Using eq. (33) for the signal amplitude, the SNR becomes:

$$SNR_{CS} = (s * h(t = T_b))^2 \Bigg/ \left(\frac{S_0}{2C_F^2}T_b + \frac{\alpha^2}{4g_m(C_S + C_L)} \times (I^2_{n,amp} + S_0) + \frac{(1+\alpha)I^2_{n,amp}}{4g_m\left(\frac{\alpha}{1+\alpha}C_F + C_L\right)}\right) \tag{38}$$

As a starting point for the design, we assume a MOSFET noise temperature of 150 K, a $\eta_{curr} = 4$,$C_F = 150$ fF, $C_L = 6$ pF and $g_m = 500\,\mu$S. This corresponds to a slight overdesign, accounting for the neglected R_S. The resulting model and simulated characteristics are plotted in fig. 17, showing that the design meets the 10 dB SNR target. This charge-based design corresponds to an area consumption of 700 μm^2, following the estimation in section V-A.

D. Current Pre-Amplifier

All previously analyzed receiver topologies benefit significantly from an increase in signal current. Here, we evaluate if preceding them with a continuous-time current amplifier, as sketched in fig. 11 d), could be used to relax their specifications. In such an amplifier, we would prefer a large current gain β, a low input-referred noise current as well as low input impedance. Given the sensor output impedance of R_S, the input impedance needs to be below this by $R_{in} < \frac{R_S}{\zeta}$, we set a target of $\zeta \approx 10$, to avoid excessive signal loss at the input.

To realize a low-power current-amplifier in a CMOS technology in practice, the current mirror, see fig. 18, is a natural choice. A current mirror with a current gain of $I_{out}/I_{in} = g_{m,P1}/g_{m,P2}$ has an input referred noise of:

$$I^2_{n,in} = 4kT\gamma g_{m,P1}\left(1 + \frac{g_{m,P1}}{g_{m,P2}}\right) \tag{39}$$

For an input-referred noise of 134 fA/$\sqrt{\text{Hz}}$ (equivalent to a 10-dB SNR for $T_b = 1\mu$s as mentioned in section IV) and calculating the acceptable $g_{m,P1}$ based on the above equation and assuming a ratio of $g_{m,P2}/g_{m,P1} = 10$ as well as a MOS noise temperature of 150 K results in an upper bound for the conductance of $g_{m,P1} < 1.8\,\mu$S. As the corresponding bias current is significantly larger than the SET current, a current-bleeding path (I_{bleed} in fig. 18) in parallel with the SET needs to be used. Following this, the input resistance of the structure is $R_{in} > 540\,$kΩ, violating the input impedance specification. To avoid this loss, a common-gate (CG) stage can be employed. Even if biased in weak inversion with the same current, the input resistance of the CG-stage is still only $\approx$3$\times$ smaller than the one of the current-mirror stage in strong inversion (assuming $\frac{g_{m,N1}}{I_{d,N1}}/\frac{g_{m,P1}}{I_{d,P1}} \approx 3$), thus requiring a boosted CG stage, as shown in fig. 18 and as used in the design in [25]. The noise contributed by the boosted CG stage is approximately:

$$I_{n,CG} \approx \frac{g_{m,N1}AV_{n,A} + I_{n,N1}}{1 + R_S g_{m,N1}(1+A) + \frac{R_S}{r_{o,N1}}} \tag{40}$$

with $I_{n,N1}$ the noise current of transistor N_1. If assuming no boosting ($A = 0$), there is only weak suppression of the CG noise due to the comparatively low sensor impedance, since $R_S g_{m,N1} \approx 133\,k\Omega \cdot 5.5\,\mu$S ≈ 0.7. Also, the resulting $R_{in} \approx 180\,$kΩ input impedance still leads to a $\approx 2\times$ signal loss. If employing boosting, the amplifier noise appears across the input impedance as $I^2_{n,boost} = V^2_{n,A}/R^2_S$ (assuming a large gain A), resulting in a specification for the amplifier input stage $g_{m,boost}$ of:

$$g_{m,boost} = \frac{4kT\gamma\eta_{curr}}{R_S^2 I^2_{n,boost}} \tag{41}$$

Budgeting half the maximum input-referred noise from eq. (9) to the amplifier and assuming $\eta_{curr} = 4$ for a differential OTA leads to a requirement of $g_{m,boost} = 440\,\mu$S. The gain requirements for the amplifier are relatively moderate if targeting $R_{in} < \frac{R_S}{10}$, leading to a required gain $A \approx 35$ (also considering halving the current in P1 to make room for the amplifier noise). The boosted CG-stage has the added advantage of a well-defined input bias voltage, limited however by the pole formed by the amplifiers g_m and C_S.

We evaluate this design in simulation for $g_{m_{P1}} = g_{m_{N1}} = 1\,\mu$S, $g_{m_{P2}} = 10g_{m_{P1}}$, $A = 35$ and budgeting half the available noise to the amplifier at a MOSFET noise temperature of 150 K. For the purpose of this verification, we assume the circuit is followed by an ideal integrator as the matched receiver. The result in fig. 19 achieves sufficient performance. The drop of SNR at higher frequencies corresponds to the signal current being lost in C_S, which can be counteracted by a larger boosting via A. When assuming a compensating capacitance of 1 pF at the output of the boosting amplifier, this current pre-amplifier design corresponds to an area consumption of 200 μm^2, again following the estimation in section V-A.

An advantage of using the current pre-amplifier is the reduction of kickback from the receiver circuit. The effects of sampling or resetting in the receiver circuit will be reduced by the reverse-isolation. In fig. 18 this isolation can be further increased by adding cascodes at the output of the mirror.

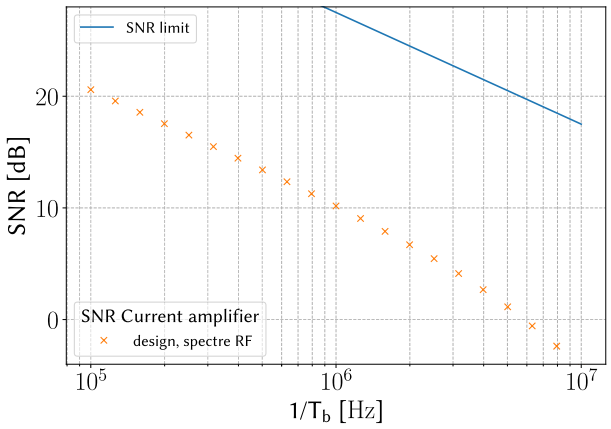


Fig. 19. SNR of current amplifier in spectre RF simulations.

TABLE II
DESIGN COMPARISON

Metric	VA	TIA	CS	IA
C_L [pF]	0.27	4.4	6	1
g_m [µS]	170	240	500	440
Power [µW]	14	19	40	35
Area [µm^2]	77	540	700	200
Fixed input bias	✗	✓	✓	✓
Reset-free	✗	(✓)	✗	✓
Two-chip	-	+	-	+
Co-integration	(+)	-	+	-

E. Benchmark

The four front-end architectures discussed above each have substantial benefits and challenges, summarized in table II. The power estimations in the table are derived from the necessary transconductance, assuming a differential pair is necessary in all cases and a $g_m/I_d = 25$ is attainable (see measurements in fig. 7). The voltage amplifier provides the lowest-power solution, but its input voltage definition relies on external resetting and is not stable during integration. The integrating transimpedance amplifier needs a significantly more complex amplifier topology that results in a worse η_{curr} and therefore more power. It however does fix the sensor voltage at the input and can work without a dedicated reset if allowing enough time for settling. The charge integration uses the most power and requires the largest output capacitance, but includes both a practical input-voltage definition and a fast reset. Finally, the current amplifier relies on one of the preceding front-ends before slicing and uses considerable power, but at the same time isolates the sensor from any switching and allows for fast settling of the input node. All approaches are small in area when compared to typical microwave passive components, typical examples can be found in [65] sized $\approx$ 100 × 200 µm. Even the largest of the amplifiers, the charge sampling amplifier, is estimated to be implementable in a $\approx 26 \times 26$ µm area.

A further consideration involves SET parameter variations, as this may be significant both due to the extremely small size of the device and limitation in fabrication uniformity in currently available processes. SET parameter variations are typically significant, requiring individual calibration of each SET sensor. In the face of this, due to the comparatively large output resistance of the SET, a voltage bias as implemented in the TIA, charge-amplifier and current amplifier might cope better with the variations than the voltage amplifier. When taking into account the expected variations in SET signal level, a trade-off appears between the amplifier power consumption to guarantee an extra margin to handle the variations and the circuit yield.

In fig. 20, we compare spectre-RF simulations of the designs presented in this work, keeping all design parameters constant and only changing the quantity of interest. For this, we use the models derived in the previous sections and the values reported in table II. By keeping all design parameters unchanged, power consumption and area of the individual circuit stays constant, allowing a direct comparison on how the swept parameter affects the design. Note that all designs approximately achieve a 10-dB SNR for 1 µs integration time given the typical parameters defined in table I, as the circuits were designed for such setting and target performance. In a), the input-signal settling observed for the voltage amplifier and TIA limits their SNR at lower frequencies, while the charge sampling architecture and the current amplifier continue to benefit due to integration. While the extent of this integration is in theory limited by the dynamic range, this is likely not problematic given the minute signal levels. For the case of the current amplifier, this improvement only holds if it is followed up by an integrating stage as detector (like the charge sampler). Towards higher readout speeds all designs offer limited performance, as surplus speed is linked to larger power consumption. In b), the charge sampling again benefits most from reducing the input capacitance, as this reduces the feedback factor α and leads to both a more complete signal integration and lower noise gain during integration. If sweeping the input resistance up from the default value of 133 kΩ, the voltage amplifier improves dramatically, as this increases the signal amplitude that can be integrated on the parasitic input capacitance. This benefit can only be exploited if the sensor can sustain the signal under the larger voltage swings.

We judge from this analysis that the charge-sampling amplifier is best suited for a potential co-integration. It requires no significant innovations on the sensor side, and benefits significantly from reducing the parasitic capacitance, allowing to scale the power of this architecture in a co-integration environment. The charge-sampler could be implemented similarly to the one in [30], but a targeted co-integration design could save much power or reach significantly higher speeds for similar power. An example design assuming a small parasitic capacitance of 50 fF targeting a 100 ns readout requires e.g. a 2 mS transconductance, $C_F = 50$ fF and $C_L = 10$ pF. This would correspond to a 160 µW power consumption assuming the above $g_m/I_d = 25$ and $\eta_{curr} = 2$. For a two-chip solution, on the other hand, without further sensor innovations, the transimpedance amplifier or current pre-amplifier are well suited, due to the comparatively lower power and good SET bias definition. If however improving the sensor design as suggested in [63], resulting in a significant increase in SET

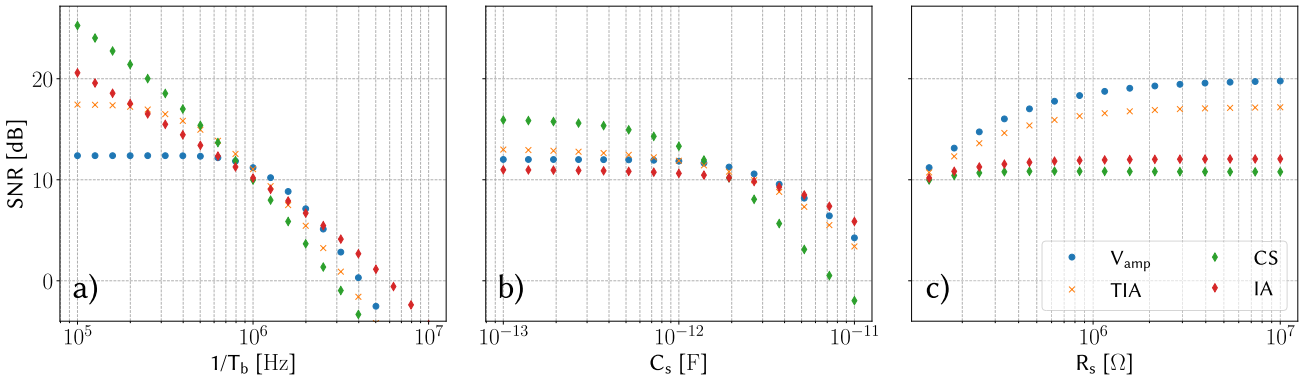


Fig. 20. SNR comparison of voltage amplifier (V_{amp}), integrating TIA and, sampler (CS) and current amplifier (IA) in response to a) symbol period, b) input capacitance, c) input resistance.

output impedance and therefore R_S, the voltage amplifier promises to perform exceptionally well for a two-chip setup, especially when implementing the g_m with a high-mobility transistor, such as, for example, a SiGe HBT. While the long-term prospects of co-integration of SiGe HBT are more difficult, such an integration could offer very low power dissipation due to the large g_m/I_d of the HBTs, significantly beyond what is attainable with CMOS technology.

VI. Conclusion

In this paper, we have modeled the electronic interface of a SET charge sensor for spin-qubit readout and derived its intrinsic limit in signal-to-noise ratio. In order to practically approach such limits, several circuit architectures are proposed and analyzed analytically and numerically, showing the advantages and disadvantages in terms of their power dissipation, kickback towards the sensor, and capability to accurately bias the SET. While the numerical results are representative of a typical case, the approach can be adjusted for the specific SET sensors, as required given the significant spread of their parameters over reported experiments. The design equations derived here represent the foundation to build future low-frequency spin-readout interfaces with minimal footprint and power dissipation, as required for large-scale quantum computers. Based on our results, for a two-chip solution, we suggest employing the TIA-based approach, while in a co-integration scenario, charge-integration seems more promising. Based on the gained insight, the model predicts that, by appropriately minimizing the parasitic capacitance between the sensor and the electronics, e.g., by adopting monolithic integration, a charge sampling DC readout could approach a 10 dB SNR even with a 100 ns integration time and 160 µW power consumption, thus meeting the needs of future quantum computers.

Appendix
BER for PAM

In reading spin qubits, the task is generally to read out spins corresponding to a spin-up or spin-down state, in the following denoted as 0 and 1. This is translated into an SET signal that is a normally distributed with mean μ_0 μ_1 and standard deviation $\sigma_0 = \sigma_1 = \sigma$. The error in this case is given by:

$$P_{error,0} = \frac{1}{2} - \frac{1}{2} erf\left(\frac{x-\mu_0}{\sqrt{2}\sigma}\right) \tag{42}$$

The optimal decision threshold for this case is the mid point, such that $x = \frac{\mu_0+\mu_1}{2}$, with this:

$$P_{error,0} = \frac{1}{2} - \frac{1}{2} erf\left(\frac{\mu_1-\mu_0}{2\sqrt{2}\sigma}\right) \tag{43}$$

Due to symmetry we have $P_{error,0} = P_{error,1} = P_{error}$. Now the power of this signal is given by:

$$P_a = \frac{1}{2}\left(\mu_0 - \frac{\mu_0+\mu_1}{2}\right)^2 + \frac{1}{2}\left(\mu_1 - \frac{\mu_0+\mu_1}{2}\right)^2 \tag{44}$$

$$= \frac{(\mu_0-\mu_1)^2}{4} \tag{45}$$

And with the Q-function $Q(x) = \frac{1}{2} - \frac{1}{2} erf\left(\frac{x}{\sqrt{2}}\right)$ and $SNR = \frac{P_a}{\sigma}$:

$$BER = Q\left(\sqrt{SNR}\right) \tag{46}$$

Reversed we recover the SNR requirements for a given BER. For example: for a readout fidelity of 99.9%, a common threshold for practical quantum error correction, we require a $BER = 0.001$, so a SNR of better than about 10dB.

Acknowledgment

The authors would like to thank Andrea Costantini and Alireza Ghafari for helpful discussions.

References

[1] L. M. K. Vandersypen et al., "Interfacing spin qubits in quantum dots and donors—Hot, dense, and coherent," *NPJ Quantum Inf.*, vol. 3, no. 1, pp. 1–10, Sep. 2017.
[2] L. Petit et al., "Universal quantum logic in hot silicon qubits," *Nature*, vol. 580, no. 7803, pp. 355–359, Apr. 2020.
[3] L. C. Camenzind, S. Geyer, A. Fuhrer, R. J. Warburton, D. M. Zumbühl, and A. V. Kuhlmann, "A hole spin qubit in a fin field-effect transistor above 4 Kelvin," *Nature Electron.*, vol. 5, no. 3, pp. 178–183, Mar. 2022.
[4] R. Maurand, "A CMOS silicon spin qubit," *Nature Commun.*, vol. 7, no. 1, p. 13575, Nov. 2016.
[5] A. M. J. Zwerver et al., "Qubits made by advanced semiconductor manufacturing," *Nature Electron.*, vol. 5, no. 3, pp. 184–190, Mar. 2022.
[6] J. C. Bardin et al., "Design and characterization of a 28-nm bulk-CMOS cryogenic quantum controller dissipating less than 2 mW at 3 K," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 3043–3060, Nov. 2019.
[7] J. P. G. Van Dijk et al., "A scalable cryo-CMOS controller for the wideband frequency-multiplexed control of spin qubits and transmons," *IEEE Sensors J. Solid-State Circuits*, vol. 55, no. 11, pp. 2930–2946, Nov. 2020.

[8] G. Kiene et al., "A 1-GS/s 6–8-B cryo-CMOS SAR ADC for quantum computing," *IEEE J. Solid-State Circuits*, vol. 58, no. 7, pp. 2016–2027, Jul. 2023.

[9] K. Yamashita, B. Hershberg, K. Yoshioka, and H. Ishikuro, "A 4.6–400 K functional ringamp-based 250 MS/s 12 B pipelined ADC with PVT-robust unity-gain-frequency-aware bias calibration," *IEEE J. Solid-State Circuits*, vol. 59, no. 3, pp. 740–752, Mar. 2024.

[10] S. J. Pauka et al., "A cryogenic CMOS chip for generating control signals for multiple qubits," *Nature Electron.*, vol. 4, no. 1, pp. 64–70, Jan. 2021.

[11] L. Enthoven, J. van Staveren, J. Gong, M. Babaie, and F. Sebastiano, "A 3 V 15 b 157μW cryo-CMOS DAC for multiplexed spin-qubit biasing," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 2022, pp. 228–229.

[12] Y. Peng, A. Ruffino, and E. Charbon, "A cryogenic broadband sub-1-dB NF CMOS low noise amplifier for quantum applications," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 2040–2053, Jul. 2021.

[13] B. Patra et al., "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 309–321, Jan. 2017.

[14] J. Park et al., "A fully integrated cryo-CMOS SoC for state manipulation, readout, and high-speed gate pulsing of spin qubits," *IEEE J. Solid-State Circuits*, vol. 56, no. 11, pp. 3289–3306, Nov. 2021.

[15] B. Prabowo et al., "29.3 A cryo-CMOS receiver with 15 K noise temperature achieving 9.8 dB SNR in 10μs integration time for spin qubit readout," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 474–476.

[16] R. Hanson, L. P. Kouwenhoven, J. R. Petta, S. Tarucha, and L. M. K. Vandersypen, "Spins in few-electron quantum dots," *Rev. Mod. Phys.*, vol. 79, no. 4, pp. 1217–1265, Oct. 2007.

[17] F. A. Zwanenburg et al., "Silicon quantum electronics," *Rev. Mod. Phys.*, vol. 85, no. 3, pp. 961–1019, Jul. 2013.

[18] S. G. J. Philips et al., "Universal control of a six-qubit quantum processor in silicon," 2022, *arXiv:2202.09252*.

[19] D. Keith, M. G. House, M. B. Donnelly, T. F. Watson, B. Weber, and M. Y. Simmons, "Single-shot spin readout in semiconductors near the shot-noise sensitivity limit," *Phys. Rev. X*, vol. 9, no. 4, Oct. 2019, Art. no. 041003.

[20] J. M. Hornibrook et al., "Frequency multiplexing for readout of spin qubits," *Appl. Phys. Lett.*, vol. 104, no. 10, Mar. 2014, Art. no. 103108.

[21] A. West et al., "Gate-based single-shot readout of spins in silicon," *Nature Nanotechnol.*, vol. 14, no. 5, pp. 437–441, May 2019.

[22] B. Prabowo, J. Dijkema, X. Xue, F. Sebastiano, L. M. K. Vandersypen, and M. Babaie, "Modeling and experimental validation of the intrinsic SNR in spin qubit gate-based readout and its impacts on readout electronics," *IEEE Trans. Quantum Eng.*, vol. 5, pp. 1–15, 2024.

[23] M. J. Curry et al., "Single-shot readout performance of two heterojunction-bipolar-transistor amplification circuits at millikelvin temperatures," *Sci. Rep.*, vol. 9, no. 1, pp. 1–8, Nov. 2019.

[24] I. T. Vink, T. Nooitgedagt, R. N. Schouten, L. M. K. Vandersypen, and W. Wegscheider, "Cryogenic amplifier for fast real-time detection of single-electron tunneling," *Appl. Phys. Lett.*, vol. 91, no. 12, Sep. 2007, Art. no. 123512.

[25] K. Das, T. Lehmann, and A. S. Dzurak, "Sub-nanoampere one-shot single electron transistor readout electrometry below 10 Kelvin," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 10, pp. 2816–2824, Oct. 2014.

[26] H. Fuketa, I. Akita, T. Ishikawa, H. Koike, and T. Mori, "A cryogenic CMOS current comparator for spin qubit readout achieving fast readout time and high current resolution," in *Proc. IEEE Symp. VLSI Technol. Circuits*, Jun. 2022, pp. 234–235.

[27] H. Fuketa, I. Akita, T. Ishikawa, H. Koike, and T. Mori, "A cryogenic CMOS current integrator and correlation double sampling circuit for spin qubit readout," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 12, pp. 5220–5228, Dec. 2023.

[28] L. Le Guevel et al., "Low-power transimpedance amplifier for cryogenic integration with quantum devices," *Appl. Phys. Rev.*, vol. 7, no. 4, Dec. 2020, Art. no. 041407.

[29] Q. Schmidt et al., "A 7.4μW and 860μm^{2}per channel cryo-CMOS IC for 70-channel frequency-multiplexed μs-readout of semiconductor qubits," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2024, pp. 1–2.

[30] M. Castriotta, E. Prati, and G. Ferrari, "Fully-integrated cryo-CMOS spin-to-digital readout for semiconductor qubits," *IEEE Solid-State Circuits Lett.*, vol. 6, pp. 185–188, 2023.

[31] J. M. Martinis, "Qubit metrology for building a fault-tolerant quantum computer," *NPJ Quantum Inf.*, vol. 1, no. 1, pp. 1–3, Oct. 2015.

[32] M. Veldhorst et al., "A two-qubit logic gate in silicon," *Nature*, vol. 526, no. 7573, pp. 410–414, Oct. 2015.

[33] J. M. Elzerman, R. Hanson, L. H. W. van Beveren, B. Witkamp, L. M. K. Vandersypen, and L. P. Kouwenhoven, "Single-shot read-out of an individual electron spin in a quantum dot," *Nature*, vol. 430, no. 6998, pp. 431–435, Jul. 2004.

[34] K. Ono, D. G. Austing, Y. Tokura, and S. Tarucha, "Current rectification by Pauli exclusion in a weakly coupled double quantum dot system," *Science*, vol. 297, no. 5585, pp. 1313–1317, Aug. 2002.

[35] A. C. Johnson, J. R. Petta, C. M. Marcus, M. P. Hanson, and A. C. Gossard, "Singlet-triplet spin blockade and charge sensing in a few-electron double quantum dot," *Phys. Rev. B, Condens. Matter*, vol. 72, no. 16, Oct. 2005, Art. no. 165308.

[36] D. Keith et al., "Benchmarking high fidelity single-shot readout of semiconductor qubits," *New J. Phys.*, vol. 21, no. 6, Jun. 2019, Art. no. 063011.

[37] A. E. Seedhouse et al., "Pauli blockade in silicon quantum dots with spin-orbit control," *PRX Quantum*, vol. 2, no. 1, Jan. 2021, Art. no. 010303.

[38] K. K. Likharev, "Single-electron devices and their applications," *Proc. IEEE*, vol. 87, no. 4, pp. 606–632, Apr. 1999.

[39] G. Kiene, O. Pietx-Casas, M. Babai, L. M. K. Vandersypen, and F. Sebastiano, "Data for: DC-readout of semiconductor spin qubits: Opportunities and limits," 4TU.ResearchData, TU Delft, Delft, The Netherlands, Tech. Rep., 2024, doi: 10.4121/8c90071e-e38b-4046-b08e-f695ab24c56f.

[40] C. Volk et al., "Loading a quantum-dot based 'Qubyte' register," *NPJ Quantum Inf.*, vol. 5, no. 1, pp. 1–8, 2019.

[41] A. N. Korotkov, "Intrinsic noise of the single-electron transistor," *Phys. Rev. B, Condens. Matter*, vol. 49, no. 15, pp. 10381–10392, Apr. 1994.

[42] S. Kafanov and P. Delsing, "Measurement of the shot noise in a single-electron transistor," *Phys. Rev. B, Condens. Matter*, vol. 80, no. 15, Oct. 2009, Art. no. 155320.

[43] U. Fano, "Ionization yield of radiations. II. The fluctuations of the number of ions," *Phys. Rev.*, vol. 72, no. 1, p. 26, 1947.

[44] E. J. Connors, J. Nelson, H. Qiao, L. F. Edge, and J. M. Nichol, "Low-frequency charge noise in Si/SiGe quantum dots," *Phys. Rev. B, Condens. Matter*, vol. 100, no. 16, Oct. 2019, Art. no. 165305.

[45] G. Zimmerli, T. M. Eiles, R. L. Kautz, and J. M. Martinis, "Noise in the Coulomb blockade electrometer," *Appl. Phys. Lett.*, vol. 61, no. 2, pp. 237–239, Jul. 1992.

[46] L. Petit et al., "Spin lifetime and charge noise in hot silicon quantum dot qubits," *Phys. Rev. Lett.*, vol. 121, no. 7, Aug. 2018, Art. no. 076801.

[47] T. F. Watson et al., "A programmable two-qubit quantum processor in silicon," *Nature*, vol. 555, no. 7698, pp. 633–637, Mar. 2018.

[48] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and compact modeling of nanometer CMOS transistors at deep-cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 996–1006, 2018.

[49] A. Beckers, F. Jazaeri, and C. Enz, "Cryogenic MOS transistor model," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3617–3625, Sep. 2018.

[50] A. Beckers, F. Jazaeri, H. Bohuslavskyi, L. Hutin, S. De Franceschi, and C. Enz, "Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures," *Solid-State Electron.*, vol. 159, pp. 106–115, Sep. 2019.

[51] P. A. T. Hart, M. Babaie, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Subthreshold mismatch in nanometer CMOS at cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 797–806, 2020.

[52] R. W. J. Overwater, M. Babaie, and F. Sebastiano, "Cryogenic-aware forward body biasing in bulk CMOS," *IEEE Electron Device Lett.*, vol. 45, no. 2, pp. 152–155, Feb. 2024.

[53] R. A. Damsteegt, R. W. J. Overwater, M. Babaie, and F. Sebastiano, "A benchmark of cryo-CMOS 40-nm embedded SRAM/DRAMs for quantum computing," in *Proc. IEEE 49th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2023, pp. 165–168.

[54] B. C. Paz et al., "Performance and low-frequency noise of 22-nm FDSOI down to 4.2 K for cryogenic applications," *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 4563–4567, Nov. 2020.

[55] K. Ohmori and S. Amakawa, "Variable-temperature broadband noise characterization of MOSFETs for cryogenic electronics: From room temperature down to 3 K," in *Proc. 7th IEEE Electron Devices Technol. Manuf. Conf. (EDTM)*, Mar. 2023, pp. 1–3.

[56] P. A. T. Hart, M. Babaie, A. Vladimirescu, and F. Sebastiano, "Characterization and modeling of self-heating in nanometer bulk-CMOS at cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 891–901, 2021.

[57] G. Kiene, A. G. Sreenivasulu, R. W. J. Overwater, M. Babaie, and F. Sebastiano, "Cryogenic comparator characterization and modeling for a cryo-CMOS 7b 1-GSa/s SAR ADC," in *Proc. IEEE 48th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2022, pp. 53–56.

[58] H. Rucker, J. Korn, and J. Schmidt, "Operation of SiGe HBTs at cryogenic temperatures," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting (BCTM)*, Oct. 2017, pp. 17–20.

[59] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1614, Nov. 1996.

[60] G. Turin, "An introduction to matched filters," *IEEE Trans. Inf. Theory*, vol. IT-6, no. 3, pp. 311–329, Jun. 1960.

[61] T. Sepke, P. Holloway, C. G. Sodini, and H.-S. Lee, "Noise analysis for comparator-based circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 3, pp. 541–553, Mar. 2009.

[62] K. Bult, M. S. Akter, and R. Sehgal, "High-efficiency residue amplifiers," in *Low-Power Analog Techniques, Sensors for Mobile Devices, and Energy Efficient Amplifiers: Advances in Analog Circuit Design 2018*, 2019, pp. 253–296.

[63] E. Kammerloher et al., "Sensing dot with high output swing for scalable baseband readout of spin qubits," *Phys. Rev. Appl.*, vol. 22, no. 2, 2024, Art. no. 024044.

[64] A. Caizzone, A. Boukhayma, and C. Enz, "An accurate kTC noise analysis of CDS circuits," in *Proc. 16th IEEE Int. New Circuits Syst. Conf. (NEWCAS)*, Jun. 2018, pp. 22–25.

[65] B. Prabowo et al., "A 6-to-8 GHz 0.17 mW/Qubit cryo-CMOS receiver for multiple spin qubit readout in 40 nm CMOS technology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 212–214.

Gerd Kiene (Member, IEEE) received the M.Sc. degree in physics from Heidelberg University, Heidelberg, Germany, in 2018, and the Ph.D. degree from the Quantum Integrated Circuits Group, Delft University of Technology, Delft, The Netherlands, in 2024. He is currently an Analog Design Engineer with Rohde and Schwarz, Germany. His research interests include cryogenic electronics, mixed-signal design, specific scientific instrumentation, and novel computing paradigms.

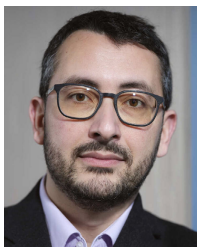
Oriol Pietx-Casas, photograph and biography not available at the time of publication.

Masoud Babaie (Senior Member, IEEE) received the B.Sc. degree (Hons.) in electrical engineering from the Amirkabir University of Technology, Tehran, Iran, in 2004, the M.Sc. degree in electrical engineering from the Sharif University of Technology, Tehran, in 2006, and the Ph.D. degree (cum laude) in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 2016.

From 2006 to 2011, he was with the Kavoshcom Research and Development Group, Tehran, with a focus on wireless communication systems design. From 2014 to 2015, he was a Visiting Scholar Researcher with Berkeley Wireless Research Center, Berkeley, CA, USA. In 2016, he joined Delft University of Technology, where he is currently an Associate Professor. He has authored or co-authored one book, three book chapters, 11 patents, and more than 100 peer-reviewed technical articles. His research interests include RF/millimeter-wave integrated circuits and systems for wireless communications and cryogenic electronics for quantum computation.

Dr. Babaie has received numerous accolades, including the 2015–2016 IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award, the 2019 IEEE ISSCC Demonstration Session Certificate of Recognition, the 2020 IEEE ISSCC Jan Van Vessem Award for Outstanding European Paper, the 2022 IEEE CICC Best Paper Award, the 2023 IEEE IMS Best Student Paper Award (Second Place), and the 2025 IEEE Solid-State Circuits Society New Frontier Award. In 2019, he was awarded the Veni grant from the Netherlands Organization for Scientific Research (NWO). Since 2021, he has served on the Technical Program Committee for the IEEE International Solid-State Circuits Conference (ISSCC), where he serves as RF Subcommittee Interim Vice-Chair in 2025. He has been the Co-Chair of the Emerging Computing Devices and Circuits Subcommittee of the IEEE European Solid-State Electronics Research Conference (ESSERC) since 2022. In addition, he serves as an Associate Editor for IEEE SOLID-STATE CIRCUITS LETTERS (SSC-L).

Lieven M. K. Vandersypen received the M.Sc. degree in mechanical engineering from KU Leuven, Leuven, Belgium, in 1996, and the M.Sc. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1997 and 2001, respectively, with a focus on quantum computing, making use of nuclear spins in molecules as quantum bits. Then, he moved to TU Delft as a Post-Doctoral Researcher, where he established his own group in 2003 and pioneered the control and read-out of single-electron spins in semiconductor quantum dot arrays. He currently focuses on scaling up spin qubits circuits, where exploratory physics goes hand in hand with high-level engineering. He was the Scientific Director of QuTech and the Co-Director of the Kavli Institute of Nanoscience. He was also co-employed by Intel for about five years. He is the Co-Founder. He was a Visiting Scientist with Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2010, and a Visiting Fellow with the University of New South Wales (UNSW), Sydney, NSW, Australia, in 2015. His research resulted in more than 180 publications that were cited over 26 000 times. He was a member of the Young Academy of the KNAW. He is a fellow of the American Physical Society (APS) and a member of the Royal Netherlands Academy of Arts and Sciences (KNAW) and the Royal Holland Society of Sciences and Humanities (KHMW). He was selected as an Outstanding Referee of the APS. He was a co-recipient of the IEEE ISSCC Jan Van Vessem Award for Outstanding European Paper in 2020, the IUPAP Young Scientist Prize for Semiconductor Physics in 2008, the Nicholas Kurti European Science Prize in 2008, and the Spinoza Prize in 2021, the highest scientific distinction in the Netherlands.



Fabio Sebastiano (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees (cum laude) in electrical engineering from the University of Pisa, Pisa, Italy, in 2003 and 2005, respectively, the M.Sc. degree (cum laude) from the Sant'Anna School of Advanced Studies, Pisa, in 2006, and the Ph.D. degree from Delft University of Technology, The Netherlands, in 2011.

From 2006 to 2013, he was with NXP Semiconductors Research, Eindhoven, The Netherlands, where he conducted research on fully integrated CMOS frequency references, nanometer temperature sensors, and area-efficient interfaces for magnetic sensors. In 2013, he joined Delft University of Technology, where he is currently an Associate Professor. He has authored or co-authored one book, 11 patents, and over 120 technical publications. His main research interests include cryogenic electronics, quantum computing, sensor read-outs, and fully integrated frequency references.

Dr. Sebastiano is on the Technical Program Committee of the ISSCC and the IEEE RFIC Symposium. He has been on the Program Committee of IMS. He was a co-recipient of several awards, including the 2008 ISCAS Best Student Paper Award, the 2017 DATE Best IP Award, the ISSCC 2020 Jan van Vessem Award for Outstanding European Paper, and the 2022 IEEE CICC Best Paper Award. He has served as a Distinguished Lecturer for the IEEE Solid-State Circuit Society. He is currently serving as an Associate Editor for IEEE JOURNAL OF SOLID-STATE CIRCUITS. He has served as a Guest Editor for IEEE JOURNAL OF SOLID-STATE CIRCUITS and an Associate Editor for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS.