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MICROFLUIDIC TISSUE BARRIER SENSOR CHIP WITH INTEGRATED MICROELECTRODES AND ULTRATHIN MICROPOROUS MEMBRANE

Pratik V. Tawade[1], Hande Aydogmus[1,2], Lovro Ivancevic[1], Jia-Jun Yeh[1,3], Vasiliki Gkouzioti,[4,5], Jean-Philippe Frimat[4,5], Jaap den Toonder[3], and Massimo Mastrangeli[1]*

[1]Department of Microelectronics, Delft University of Technology, The Netherlands
[2]Else Kooi Laboratory, Delft University of Technology, The Netherlands
[3]Department of Mechanical Engineering, Eindhoven University of Technology, The Netherlands
[4]Department of Neurology, Leiden University Medical Center, Leiden, The Netherlands
[5]Department of Human Genetics, Leiden University Medical Center, Leiden, The Netherlands

ABSTRACT

We present a novel silicon-based organ-on-chip (OoC) device featuring integrated microelectrodes to assess barrier function in biological tissue co-cultures. The microfluidic device consists of two vertically-stacked microchannels separated by a submicron-thin, microporous silicon nitride membrane, enabling *in vivo*-like proximity for co-cultured tissues. The integrated four-probe electrode geometry on slanted microchannel sidewalls ensures unobstructed optical access to the membrane and consistent measurement repeatability. Experimental validation through electrical impedance spectroscopy supported the device's sensitivity to sodium chloride concentration. Fabricated through a scalable, wafer-scale batch process, the device additionally demonstrated biocompatibility and optical transparency, representing a significant advancement for *in situ* tissue barrier assessments.

KEYWORDS

barrier-on-chip, microfabrication, microfluidics, organ-on-chip, trans-epithelial electrical resistance

INTRODUCTION

Organs-on-chip (OoCs) are advanced microfluidic cell culture devices featuring tissue perfusion and embedding into a dynamic, *in vivo*-like synthetic microenvironment [1]. Cells in OoCs are arranged to emulate tissue and organ-level microphysiology, allowing researchers to study complex tissue interfaces as well as the chemical and mechanical microenvironments characteristic of specific organs. This way, OoC technology enables the development of *in vitro* (sub)organ models that closely mimic *in vivo* counterparts, including those of *e.g.* the brain [2], heart [3], and intestine [4]. As the demand for more biologically complex and accurate OoC models grows, so does the need for precise monitoring tools to assess their functionality [5]. Reliable assessment of OoC systems requires sensing techniques that deliver continuous information on both the physical and chemical conditions within the microenvironment. Monitoring of tissue barriers is one essential need, as it serves as a critical indicator of epithelial or endothelial tissue viability and functionality. One of the most effective methods for tissue barrier assessment is the measurement of trans-epithelial electrical resistance (TEER). TEER is a rapid, non-invasive assay used to evaluate the integrity and differentiation of epithelial monolayers, with electrical impedance across the tissue correlating to the formation of tight junctions between neighboring cells [6]. While TEER measurements have become a standard for assessing cell monolayer integrity in traditional cultures, applying this method within OoC systems presents technical challenges [7]. Current designs that include TEER electrodes within OoCs often offer scarce reproducibility of electrode placement, lack stable electrical readings, and impede visual inspection of the cells [8]. In this work, we present a novel silicon-based OoC device featuring wafer-level microfabrication of stacked microchannels (200 μm-wide and 5 mm-long) with integrated microelectrodes and separated by a ultra-thin, microporous silicon nitride (SiN) membrane. The device was designed to enable highly-repeatable and sensitive TEER measurements across virtually any cell co-culture seeded across the membrane. We detail the fabrication process, alongside electrochemical and biological characterizations of the sensor chip, and outline its packaging into a compact OoC module for OoC platforms.

FABRICATION PROCESS

The full fabrication process flow of the device is sketched in Fig. 1. The process begins with pairs of 300 μm-thick, double-side polished silicon wafers. The initial step involved growing a 150 nm-thick silicon dioxide (SiO_2) layer through wet oxidation of the silicon substrates in a furnace (Tempress) at 1100 °C. This oxide layer is retained throughout most of the process and serves as a protective layer for the final membrane release, achieved via deep reactive ion etching (DRIE). Following oxidation, a 150 nm-thin low-stress SiN layer was deposited on both sides of the wafers using low-pressure chemical vapor deposition (LPCVD) (Fig. 1a). The SiN layer fulfills a twofold function: it acts as hard mask during subsequent wet etching of silicon on one side of the wafers, and provides the substrate for membrane patterning on the other. The SiN layer on the bottom wafer side was processed lithographically to define the channel outline, and then selectively etched by RIE using C_2F_6 plasma, exposing the underlying oxide layer in the patterned areas. The oxide layer was thereby etched with C_2F_6/CHF_3 plasma to reach the silicon surface (Fig. 1b).

The next step in the process involved etching the exposed silicon substrate to form shallow slanted sidewalls. Anisotropic wet etching with tetramethylammonium hydroxide (TMAOH) is commonly used for this purpose. Due to differing etch rates between Si crystallographic planes, with the (100) plane etching significantly faster than the (111), this method produces sidewalls angled at 54.7° relative to a (100) wafer's surface [9]. Etching was performed in a 25% v/v TMAOH water solution at 85 °C with constant agitation. The temperature-dependent etch rate increases as

the temperature rises; and constant agitation ensures a steady provision of reactants at the silicon surface, thus enforcing a sustained though progressively-declining etch rate. The process was carefully timed to produce approximately 15 μm-deep trenches in the silicon, corresponding to the slanted sidewalls along the channels (Fig. 1b). Following the etching process, the residual SiO₂/SiN layer stack, which served as hard mask, was removed using the previously-mentioned dry etching chemistry.

Before substrate metallization, it is crucial to electrically insulate the silicon surface to prevent potential conductivity issues. For this purpose, a 200 nm-thick SiO₂ layer was deposited on the wafer's top side using plasma-enhanced chemical vapor deposition (PECVD) with SiH₄/N₂O gases at 400 °C (Fig. 1c).
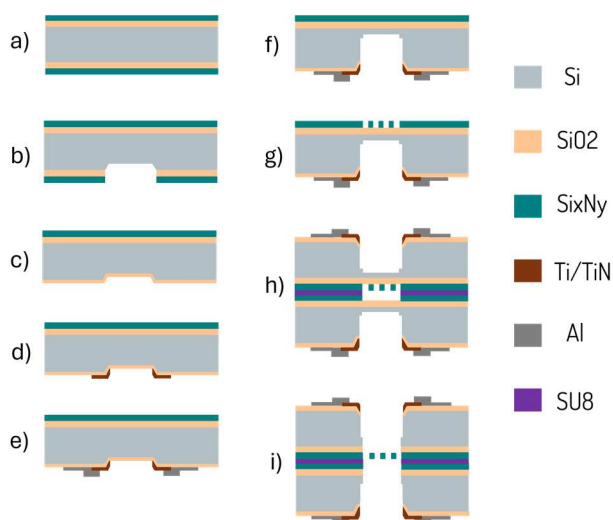

Figure 1: Fabrication process: a) Deposition of SiO₂ and SiN on both sides of 4" Si wafers, b) masked anisotropic wet etching of Si to form slanted sidewalls, c) passivation of the wafer backside with SiO₂, d) patterning of TiN electrodes on the slanted sidewalls, e) patterning of Al bonding pads, f) Deep reactive ion etching of Si to form deep straight channels, g) patterning of SiN on the frontside to form the microporous membrane, h) bonding of two wafers mediated by SU-8, i) release of the membrane by Bosch etching of the remaining Si followed by wet etching of SiO₂.

To integrate the electrodes, a 20 nm-thin titanium (Ti) adhesion layer and a 300 nm-thin layer of titanium nitride (TiN) were sequentially sputtered at 6 kW power and 350 °C and later lithographically-patterned to define the microelectrodes on the slanted sidewalls (Fig. 1d and Fig. 2d). In view of the significant topography present by this stage across the substrate, multiple passes of spray coating, each followed by soft backing, were introduced to deposit a conformal and uniform layer of photoresist, and ensure in particular accurate coverage of electrode edges. After photolithographical patterning of the resist layer, the metal stack was dry-etched using an inductively-coupled plasma reactive ion etcher (ICP-RIE, Trikon Omega 201) with a Cl₂/HBr plasma to define the electrode structures (Fig. 2e). Bonding pads were then fabricated by sputtering and subsequently patterning a 1 μm-thick Si-rich Al layer. The layer was etched through a photopatterned resist mask using Cl₂/HBr chemistry to form bonding pads connected to the electrodes (Fig. 1e and Fig. 2c).

In the subsequent step, the microfluidic channels were opened using DRIE (SPTS Rapier), which employs the Bosch process to create straight vertical walls by alternating etch and passivation phases. The etching was conducted in two stages to achieve a step profile between the channel inlet/outlet and the membrane area to separate the top and bottom channel regions. First, a 40 μm-deep trench was etched in the membrane area using SF₆/C₄F₈ plasma. After this, the channel area was patterned and etched by means of a thicker layer of photoresist, applied through multiple spray coating passes to accommodate the increased topography. The channel area was etched to a total depth of 260 μm, leaving approximately 40 μm of silicon to mechanically support the SiN membrane during the subsequent processing steps.
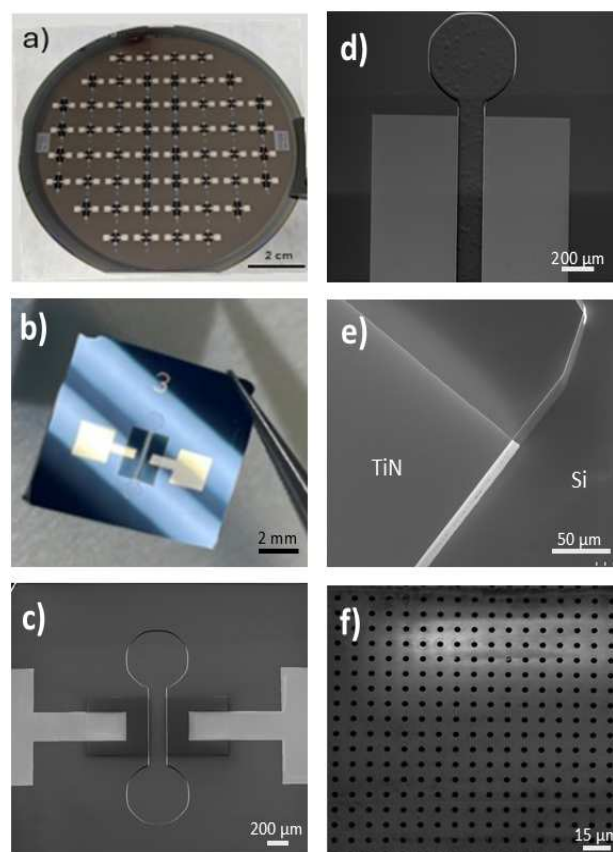

Figure 2: Fabrication highlights. a) Full wafer stack, containing 52 devices, b) single diced chip, c) scanning electron microscope (SEM) image of a fully-metallized single device, d) SEM image of the electrodes and microchannel, e) SEM close-up of a TiN electrode over a slanted sidewall, and f) SEM image of the porous membrane.

The wafers were at this stage divided into two batches: in one batch, porous membranes were patterned on the frontside, while in the other the SiN was removed from the membrane area. To create the porous SiN membrane, photoresist was spin-coated onto the first batch of wafers and exposed through a mask with 3 μm-wide circular opening and 10% porosity using a stepper (Fig. 2f). The SiN layer was then etched to form the pores using a C₂F₆ plasma. In the second batch of wafers, the SiN layer was similarly etched away from the frontside.

Next, pairs of wafers—i.e., one with a patterned porous membrane, and the other without—were aligned and bonded together to form the full device stack, including the stacked microchannels separated by the ultrathin SiN membranes. Wafer-level thermo-compression bonding was mediated by SU-8, a high-strength, biocompatible, chemically- and thermally-stable adhesive [10]. SU-8 was spin-coated on the bonding sides of both wafers, soft-baked at 95 °C and subsequently patterned by lithography. The coated wafers were aligned and bonded by means of a wafer bonder (AML) under vacuum at 120 °C, under an applied bonding force of 2.5 kN.

The final steps involved releasing the membranes and wafer dicing. Photolithographic patterning on each surface of the bonded wafers was used prior to etching away the residual 40 µm of silicon as well as SiO_2 on both sides, and finally releasing the membranes with SF_6/C_4F_8 plasma etching. Once fabrication was complete, the wafers were diced to obtain 52 10-by-10 mm² chips (Fig 2b).

EXPERIMENTAL RESULTS

The fabricated and singulated chips were tested for electrical functionality prior to *in vitro* biocompatibility and preliminary cell culture tests. The electrical characterization was conducted using an electrochemical setup with reference/counter and working electrodes using a common electrolyte. *In vitro* biocompatibility experiments were carried out using Human Umbilical Vein Endothelial Cells (HUVECs).

Electrochemical characterization

Electrochemical impedance spectroscopy (EIS) was conducted to estimate the impedance of the microelectrodes. EIS characterizes the resistance and reactance of microelectrodes by applying an alternating current or voltage across a range of frequencies and measuring the system's response. This technique provides insights into the electrochemical behavior and properties of the system [11].
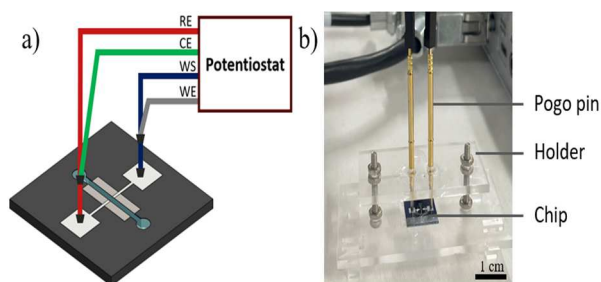
Figure 3: a) Setup of EIS measurements using 2-electrode 4-terminal connection mode, with the working (WE), working sense (WS), counter (CE), and reference (RE) electrodes. b) Connections to single chip's top electrodes.

The microfluidic channel containing TiN slanted-sidewall electrodes was filled with NaCl solutions at concentrations of 0.1 mM, 1 mM, and 10 mM. To minimize the influence of wire resistance during measurements, a 4-terminal connection was used in the 2-electrode setup (Fig. 3). The chip consisted of one TiN microelectrode serving as both the counter and reference electrode, while the other TiN microelectrode functioned as the working and sensing

electrode. The electrodes were connected to a portable potentiostat (PalmSens4) via pogo pins, which were in turn coupled to the system with crocodile clips. A sinusoidal waveform with 20 mV$_{RMS}$ amplitude and a frequency range of 1 Hz to 1 MHz was applied as the driving input. Three measurements were conducted for each NaCl concentration. The results of impedance (Fig. 4) and phase (Fig. 5) measurements evidenced the interplay of solution resistance and electric double-layer capacitance across NaCl concentrations The overall impedance decreases as NaCl concentration increases due to the improved ionic conductivity (Fig 4). At lower concentrations (0.1 mM), the system exhibits a predominantly capacitive response at low frequencies, as indicated by the highest phase angle (Fig 5). This behavior can be attributed to the pronounced double-layer capacitance effect due to the limited availability of ions for charge screening. As the concentration increases, the system transitions to a resistance-dominated regime with a more compact double-layer and reduced solution resistance.
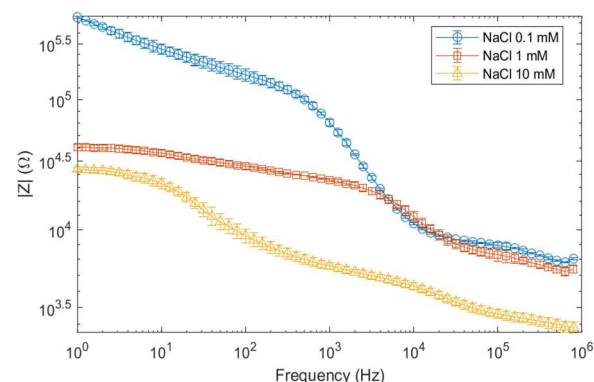
Figure 4: Impedance data recorded from two TiN electrodes in 0.1 mM, 1 mM and 10 mM NaCl solutions. Error bars represent the standard deviation out of three independent measurements for each concentration.
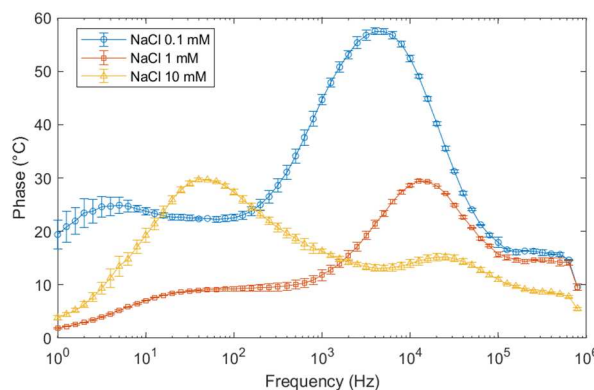
Figure 5: Phase angle data recorded from two TiN electrodes in 0.1 mM, 1 mM and 10 mM NaCl solutions. Error bars represent the standard deviation out of three independent measurements for each concentration.

Biological characterization

HUVECs were cultured in Endothelial Cell Growth Medium (ECGM) (211-500, Cell Applications Inc) supplemented with 10% Fetal Bovine Serum (FBS) and 1% Penicillin/Streptomycin (P/S). After 3 days of culture, the cells were harvested using accutase (A6964, Sigma-Aldrich)

and resuspended in ECGM to be used for seeding (125k cells per membrane) on the membranes. Prior to seeding, the membranes were coated with fibronectin (50 µg/mL) for 1 hour.

Cells on membranes were fixed with 4% paraformaldehyde for 10 minutes and permeabilized with 0.5% Triton-X100 for 10 minutes. The nuclei (NucBlue Live ReadyProbes, R37605, Thermo Fisher Scientific, Rosny-sous-Bois, France) and actin (ActinGreen 488 Ready-Probes, R37110, Thermo Fisher Scientific) were stained for 30 minutes in the dark at RT. Images were obtained using the Keyence BZ-X800 micro-scope. Fig. 6 shows that cells are able to spread and grow on the porous membrane.
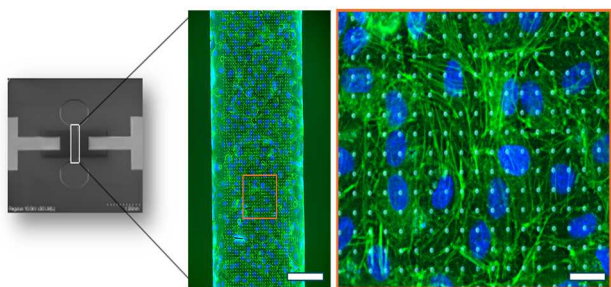

Figure 6: Human endothelial cells (HUVECS) cultured for 48h on-chip (green=actin, blue=nucleus). Scale bars: 100 µm (middle) and 15 µm (right)..

CONCLUSION

We have demonstrated the wafer-level fabrication of a novel silicon-based organ-on-chip device with integrated microelectrodes designed for TEER-based assessment of barrier function in biological tissue co-cultures. The device features two vertically-stacked microchannels separated by a submicron-thin, microporous, optically-transparent silicon nitride membrane. Electrochemical characterization confirmed the functionality of the microelectrodes, while biological testing verified the biocompatibility and optical transparency of the membrane. These results anticipate further studies with human barrier-forming induced pluripotent stem cells to quantify barrier integrity in real-time.

Future work will focus on packaging the device to enable seamless fluidic and electrical access, facilitating continuous measurements within cell co-culture microenvironments. In particular, we will aim to configure the device into a compact and standardized fluidic and electric module compatible with integration onto the fluidic board of the modular Smart Organ-on-Chip platform (Smart OoC).

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CONTACT

*M. Mastrangeli, m.mastrangeli@tudelft.nl