A Low-Complexity CMOS Receiver for UWB signals

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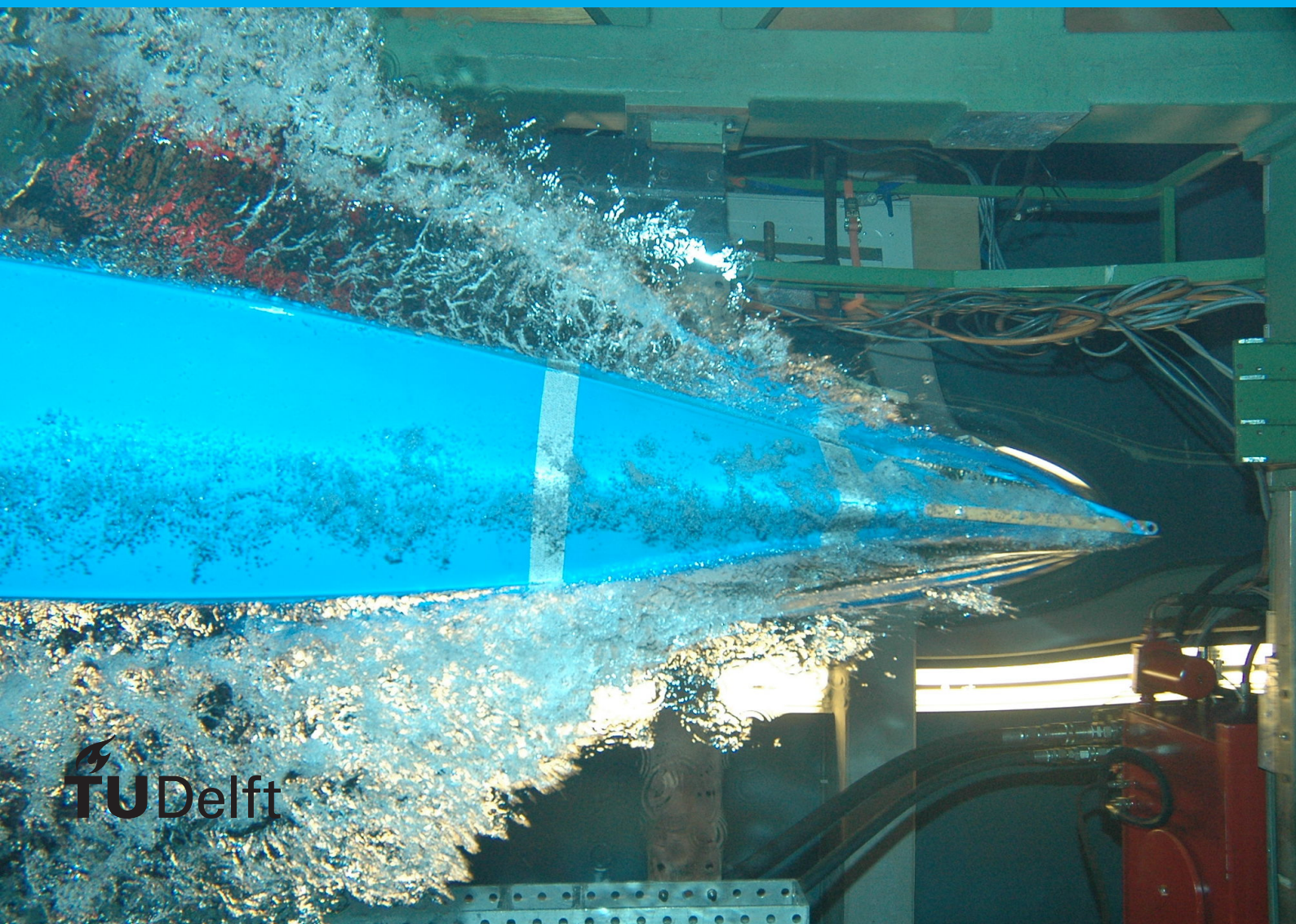
Master Research Thesis in Microelectronics



A Low-Complexity CMOS Receiver for UWB signals

by

Ernesto E. Gonzales Huamán

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Abstract

It is well-known that GPS is a widely used technology for localization in outdoors environments. Nonetheless, such standard fails to provide a practical and accurate solution for localization and ranging applications within indoor environments due to the need of satellites and meter-level accuracy, which is poor for indoor environments. It is in this context that Ultra-Wideband (UWB) emerges as the potential standard to overcome the accuracy shortcomings of other types of radio signals, which is needed for security, military and medical applications.

Based on the fact that first-path time and amplitude detection favor the ranging accuracy in indoor environments. This thesis presents the implementation of a novel low-complexity receiver concept implementing first-path time and amplitude detection with a maximum ranging error of less than $7cm$. This system is able to decouple amplitude from time detection, which improves the TOA estimation accuracy of the system. The architecture of this receiver is fully self-biased and inverter-based, which also favors process scalability. The receiver is able to perform time detection on signals with frequencies up to $900MHz$ due to technology limitations. Furthermore, a low-power consumption of $22mW$ is achieved.

Ernesto E. Gonzales Huamán
Delft, February 2017

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Next, I would also like to thank Bioelectronics PhD student Gustavo Campos for valuable discussions and feedback about different ideas that I had during the course of my research. On the other hand, I would also like to thank PhD student Yan Xie for providing me with her measurements and statistical analysis in order to clear my explanation of the thesis goals, and for valuable discussions and guidance in understanding the system as a whole. Furthermore, I would also like to thank my office-mate Marco D' Avino, Samprajani Rout, Marloes Adank and the rest of the people in the office for making the thesis time much more enjoyable.

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Ernesto E. Gonzales Huamán
Delft, February 2017

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Glossary

ADC Analog-to-Digital Converter.
AGC Automatic Gain Control.
AOA Angle-of-arrival.

CSS Chirp Spread Spectrum.

DS-UWB Direct-Sequence UWB.

ED Energy Detector.
EIRP Equivalent Isotropically Radiated Power.

GPS Global-Positioning System.

IR-UWB Impulse-Radio Ultra-Wideband.

LNA Low-Noise Amplifier.
LOS Line-of-sight.
LPF Low-Pass Filter.

MBOA-UWB Multiband OFDM Alliance for UWB.
MDS Minimum Detectable Signal.
mV mili-volts.

NLOS Non-line-of-sight.

OFDM Orthogonal Frequency Division Multiplexing.

PD Peak Detector.

Rake A radio receivers using several sub-receivers.
RSS Received signal strength.
RX Receive.

SNR Signal-to-Noise Ratio.

TDC Time-to-Digital Converter.
TDOA Time-difference-of-arrival.
TOA Time-of-arrival.
TX Transmit.

UWB Ultra-Wideband.

VGA Variable-Gain Amplifier.

WPAN Wireless Personal Area Network.

1 Introduction

In the early 60s, several U.S. government organizations were interested in the development of a satellite systems for three-dimensional localization. After years of research, the system concept for NAVSTAR GPS was developed [23]. Comprised of a large satellite constellation, GPS is able to provide geolocalization of receivers by knowing the position of several satellites and their range from the receiver through TOA measurements.

While GPS is nowadays the standard outdoor environments for positioning applications, it does not provide the desired localization precision for indoor location due to incapability of the employed signals to penetrate solid walls [20]. Equipped with promising features for highly accurate ranging and localization applications, UWB has a emerged as the equivalent of GPS for indoor environments. The standard obtained so much attention from the scientific community that the IEEE adopted the IEEE 802.15.4a WPAN standard for the creation of a physical layer for short-range and low data rate communications [30].

While other forms of communication rely on modulating the frequency, power level and/or the phase of a sinusoidal wave to transmit information, UWB systems do so by transmitting short pulses at a certain relatively low rate. Due to this low duration, the pulses have a large bandwidth. Consequently, UWB has several advantages for indoor positioning which will be explained later in this introduction.

In the following subsections, a formal definition and regulations related to UWB will be introduced, including arguments which favor its widespread use for positioning applications.

1.1. Formal Definition

A signal is called UWB if it has an absolute bandwidth (B_{abs}) of at least 500 MHz (measured at a -10 dB bandwidth) or a fractional bandwidth B_f of at least 0.2 with a maximum EIRP of -41.3 dBm/MHz.

The absolute bandwidth is defined as:

$$B_{abs} = f_H - f_L \tag{1.1}$$

and the fractional bandwidth is defined as:

$$B_f = \frac{B}{f_c} = 2\frac{f_H - f_L}{f_H + f_L} \tag{1.2}$$

1.2. Regulations

In 2002, the Federal Communications Commission (FCC) in the USA granted unlicensed use of UWB devices subject to certain emission constraints.

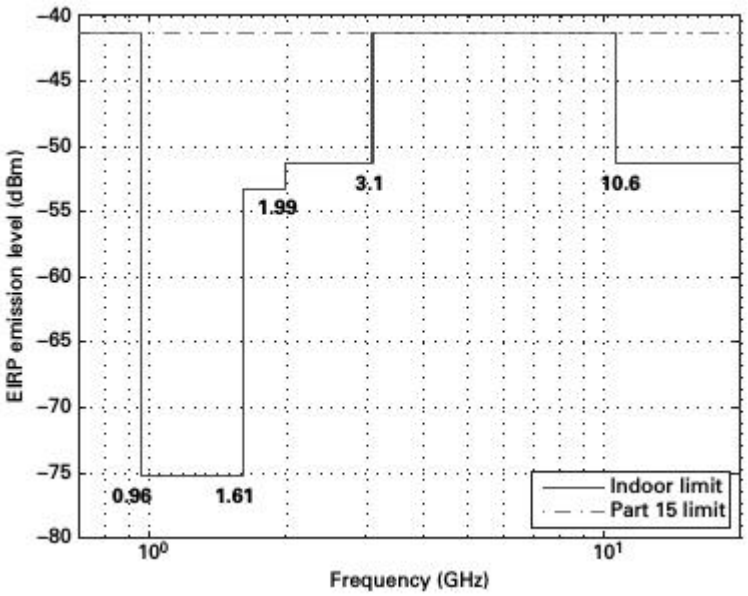


Figure 1.1: FCC emission limits for indoor UWB systems [30]

In general, most of the UWB literature read about systems designed within the 3.1 GHz and 10.6 GHz, for which an emission of EIRP of -41.3 dBm/MHz is required. This means that the maximum signal strength measured in any direction from the UWB device is such a value.

From figure 1.1, it can be seen that the EIRP requirements are tougher for the 0.96 GHz - 3.1 GHz frequency band because an UWB system has to coexist with other devices that use GPS, Wi-Fi, etc in such a frequency region.

1.3. Why UWB?

UWB technology offers attractive features to be exploited for positioning applications that can be summarized as follows.

- ***The improved resolvability of received multipath components*** Multipath resolvability is defined as the number of paths that can be distinguished by a receiver [36]. If there are 2 multipath components with delays τ_1 and τ_2 arrive, and the system bandwidth is B_x, then the following equation usually holds:

$$|\tau_1 - \tau_2| \gg \frac{1}{Bx} \tag{1.3}$$

  The minimum bandwith required for UWB is $500MHz$, which means that the pulse maximum pulse duration is $2ns$ (and the minimum $133ps$, which is that then entire bandwidth allocated for UWB is used). Therefore, it is highly unlikely that two received multipath components will overlap if they arrive separated by $2ns$. This resolution improves as the system is allocated more bandwidth.

- **Good penetration properties**

  NLOS positioning can introduce errors due to delays caused by the obstacles. They can even totally invalidate the positioning estimation due to the receiver not being able to see one or more transmitter. However, because of the RF nature of the signals $(3-10GHz)$, they have good obstacle penetration properties [30], thus making positioning possible for longer distances and severe NLOS condition.

- ***Potential low-complexity system implementation*** UWB transmitters are able to produce very short-time domain pulses which cover a wide spectrum. Therefore, no mixer is needed; low power operation can potentially be achieved [8] [30]. This also means the receiver does not have any sort of mixer. Therefore, the receiver implementation can be quite simple.

1.4. Positioning Methods - Brief Overview

Receivers for UWB signals designed for ranging purposes produce an output that is useful for performing positioning algorithms. These exploit geometric relationships between transmitters and receiver in order to estimate the user's unknown position.

Among the most important positioning algorithms, RSS, TOA, TDOA and AOA are found to be most popular ones in literature. AOA-based systems obtain the angle information from the incoming pulses at the receivers or sensors in order to estimate the position of the transmitter, while RSS-based systems calculates the distance as a function of signal strength with a closed-form expression. It basically assumes that the signal strength is inversely proportional to the distance squared between transmitter and receiver. For a more complete treatment of such methods, the interested reader is referred to [17] and [30].

The system in this work estimates the time a radio wave takes to arrive at the receiver from the transmitter. Therefore, the TOA and TDOA methods are relevant for this thesis.

If the time is known, then the distance d traveled by the wave in free space is obtained from the following simple expression:

$$d = c \times \tau_{TOA} \tag{1.4}$$

where c is the speed of light and τ_{TOA} is the time of arrival. Then, if we have two other receivers (in total three of them), then it should be theoretically possible to estimate the unknown position of the transmitter.

However, there are practical difficulties with this approach. First, the receiver should know accurately the time of transmission of the pulse, which means that both receiver and transmitter should be controlled by a common-clock. While in prototypes shown in the literature (such as [22]) one clock can be used to control both TX and RX, in practical systems each will have its own clock. If not measures are taken with respect to their drift, then synchronization between TX and RX will fail, thus degrading the TOA accuracy.

In order to overcome this synchronization difficulty, TDOA approaches have been proposed. In this approach, the principle is based estimate the difference in time-of-arrival for two pulses, therefore, the absolute time at which the first pulses was transmitted is not necessary. The synchronization requirement is then reduced to only the TXs being synchronized.

Let the received signal at some receiver i be:

$$r_i(t) = \alpha s(t - \tau_{TOA,i}) + n_i(t) \tag{1.5}$$

where α is some channel coefficient, $\tau_{TOA,i}$ is the time of arrival of the signal. To illustrate better how the signals are received, the following timing diagram is shown:

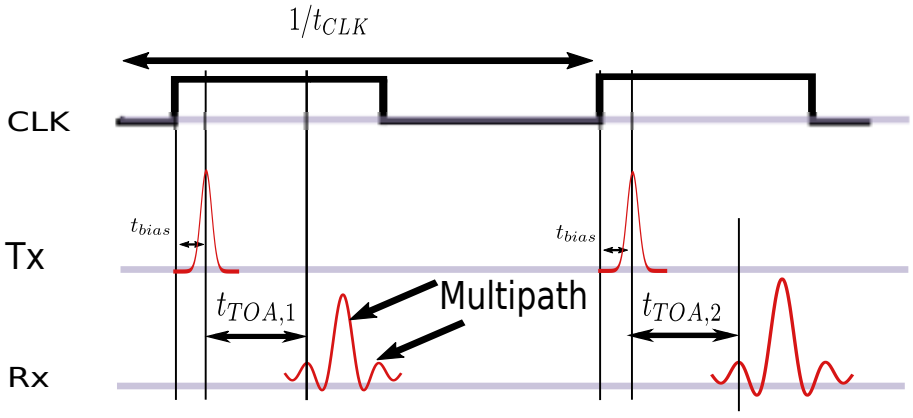


Figure 1.2: System waveforms for TDOA estimation

From the figure 1.2, we can see that the signals from TX will have some t_{bias} with respect to the rising edge of the clock CLK (whose period is given by t_{CLK}), therefore, performing only a TOA measurement will end up

being inaccurate due to this t_{bias} term which can is highly dependent on clock oscillator parameters and the external environment.

If we obtain two TOA measurements, namely, $\tau_{TOA,1}$ and $\tau_{TOA,2}$, then the TDOA is given by:

$$\tau_{TDOA} = \tau_{TOA,1} - \tau_{TOA,2} \tag{1.6}$$

Therefore, in this subtraction, the t_{bias} terms will be ideally canceled.

Another way to obtain the TDOA is by doing cross-correlation between both received signals and then calculate the delay corresponding to the largest value in the correlation function. However, this approach only works well in additive noise and single-path channels. Normally, indoor channels are rich in multipath. Therefore, it is highly likely that the highest peak in the correlation function between two received signals is not the first path but some other multipath component, which can be several hundreds of picoseconds to nanoseconds away from the first path, thus degrading TOA accuracy.

1.5. Thesis Objectives

The main focus of this thesis is to implement a low-complexity IR-UWB receiver for TOA estimation. The design is based on the system proposed in [7]. Essentially, the receiver performs threshold- and peak-detection on the first peak surpassing a predefined threshold; therefore, it has to ignore the further incoming (and possibly larger) pulses due to multipath. Further details on the operation of the system will be given in chapter 2.

Since the receiver to be designed is non-coherent, it has particular advantages and disadvantages in the implementation and in the system as a whole:

Advantages

- Low-Complexity
- Relaxed Oscillator Accuracy

Disadvantages

- Inability to increase by coherent averaging
- Suboptimal over an additive-noise channel

To perform a coherent sum of the incoming pulses for system SNR boosting purposes, high sampling frequencies (~$10GHz$) and a high performing oscillator for accurate timing are required [7].

It is for those reasons, and also to be robust against narrow-band interference, that statistical averaging of repetitive transmissions is used by this system.

In order to relax the requirements of high-performing ADCs, the system also features a simple way to slow down a signal by means of extracting its envelope and decaying it with a well-defined RC time constant which is orders magnitude greater than the inverse of the signal bandwidth, in this way, low-cost and average-performing ADCs with sampling frequencies on the order of tens of MHz can be used [7].

A simplified version of this system, which only considers the threshold detection part, was implemented by PhD student Yan Xie. Therefore, a threshold detector was also implemented at the circuit level in this thesis.

Then, the following research tasks are discussed in this thesis:

- System Design of the Receiver
- Circuit Design of the Receiver:
- Circuit Design of the Threshold detector

First, an ideal high-level system implementing the functions needed for the receiver is done to illustrate the operation of the system.

Then, to implement the peak detection functionality, a large literature research of peak-and-hold detector topologies which could potentially fit the system is done. Therefore, once the peak detector was chosen, the next step was to introduce a modification of the selected topology to implement the required function,

namely, tracking and holding onto the first peak surpassing a predefined threshold and subsequently ignoring the further incoming multipath component.

The other task at hand was the design of a threshold comparator with a low-delay uncertainty being able to drive a $2.5pF$ load, which is the digital input capacitance of the TS5A2053 analog switch used in the threshold detector that was already implemented. The threshold detector in this thesis is considered a separate system.

1.6. Thesis Outline

This thesis is organized as follows:

In Chapter 2, the working principle of the receiver in this work is explained. Then, the results of a previous receiver implemented following the same principle are presented and discussed. Then, a modification to working principle of the receiver is introduced, and its possible error sources with respect to time-of-arrival accuracy are simulated. From there, a voltage noise budget and a minimum resolution is derived. Besides that . Furthermore, a link-budget analysis is performed using such specifications and under the assumption of LOS conditions to state what the potential detection range in meters provided by the system is.

In Chapter 3, the concept of the peak detector is discussed in terms of block diagrams. Then, from the requirements established in the previous chapter, a final peak detector block diagram will be used

In Chapter 4, the circuit design of the peak detector is discussed. First, an in-depth analysis of the peak detector chosen is performed in order to predict its performance in terms of the amplitude error expected as a function of the topology parameters. Then, the circuit blocks within the peak detector are implemented using high-speed techniques.

In Chapter 5, a threshold detector is designed. The design can drive pF-level loads and it is tested against process variations to determine statistical deviations in offset. Furthermore, the propagation delay due to variations in overdrive voltage is tested across process corners. The delay is also obtained for variations in common-mode voltage, which also demonstrates the wide common-mode range of the threshold detector.

Finally, the thesis finishes with a chapter stating the conclusions, scientific contributions and recommendations for further research.

2

System Design

After the FCC allowed the limited use of UWB systems, there has been many standardization efforts. There exists two UWB IEEE standards, namely the IEEE 802.15.3a and IEEE 802.15.4a, which are amendments to the original WPAN standards for high and low-data rates, respectively.

Under the IEEE 802.15.3a standard, there exists two system proposals, namely the the Multiband OFDM Alliance for UWB (MBOA-UWB) and the direct-sequence UWB (DS-UWB). Essentially, the difference between both systems is the fact that the former divides the UWB frequency spectrum into several sub-bands, while the latter uses the entire frequency spectrum as a whole single band. There is an optional ranging capability for the MBOA-UWB architecture, which uses a two-way ranging protocol [30].

For the IEEE 802.15.4a, which describes an alternative UWB physical layer for ranging applications in WPAN, two types of signaling formats are used, namely, Chirp Spread Spectrum (CSS) and Impulse-Radio UWB (IR-UWB). Since there is an optional ranging capability for the latter [30], this type of signaling scheme is used for research in algorithms applied to ranging and positioning systems.

In this chapter, a brief introduction to IR-UWB system architectures is presented to provide a context in which the advantages of the proposed solutions are more clear. A description on the operation of the proposed system is given and measurement results of a discrete implementation of the system will be discussed. Based on this, an alternative approach to do TOA estimation based on a linear decay will be proposed, and its possible sources of error will be evaluated. Based on this, a noise budget and a minimum quantization accuracy will be determined. The uncertainty on the timing of the peak detector is added as well to compose a TOA accuracy budget of 10cm. Finally,an analysis of the link budget is provided to estimate the maximum ranging distance the system could potentially achieve under LOS assumptions.

2.1. IR-UWB System Architectures

For UWB systems, there exists a trade-off between optimality and system implementation feasibility. Coherent receivers are considered optimum in the sense that they can take advantage of the multipath characteristic for higher system SNR. However, their implementation is much more complex than their non-coherent counterparts.

2.1.1. Coherent Receivers

Coherent or homodyne receivers demodulate their input signal in a synchronous fashion. For UWB, they usually correlate the input with locally generated reference. In basic communications theory, it is well-known that matched filters are the most optimum blocks to detect signals whose shape is known and are buried in additive noise [11]. In this regard, the Rake receiver is arguably the most popular analog version of a matched filter or "digital" receiver; it implements the optimum filter with correlator block followed by an integrate-and-dump approach. A typical block diagram of its structure is given figure 2.1.

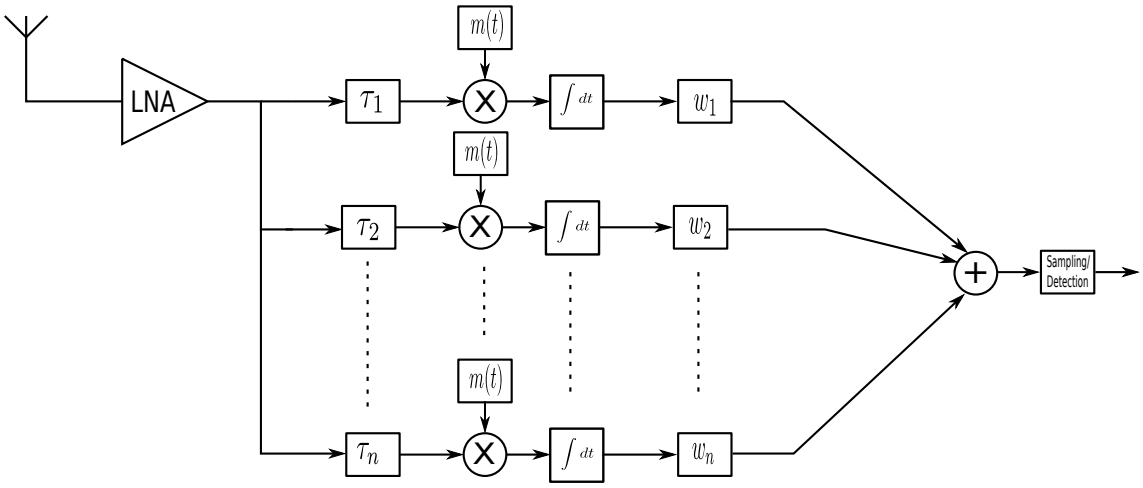


Figure 2.1: Typical RAKE receiver

In the RAKE receiver, the input signals passes through several branches which have a certain delay,respectively. This way, the several multipath components of the input signals are aligned in time and can be dealt with separately. Then, the correlators, formed by the template signal $m(t)$ and integrator block, outputs a signal with a peak, which is the result of cross-correlating the multipath component with the local template. Then, a diversity combiner is used in order to decide on weighting factors $w_1, w_2, \ldots w_n$ so that the outputs are finally summed coherently [11].

While the receiver provides tremendous performance on the SNR and ability to detect signals by doing a constructive addition of the multiple signal versions, the complexity of implementing such a system is quite significant. For instance, there has to be an accurate pulse synchronization; the delays must align the multipath components in order to provide an accurate correlation. Otherwise, the outputs will not be summed coherently and there will be loss in SNR. Another disadvantage is that indoor channels usually are rich in multipath components, therefore, the number of fingers might be in the order of tens, which adds implementation complexity.

2.1.2. Non-Coherent Receivers

Due to the high complexity cost of implementing coherent UWB receivers, the non-coherent types have received lots of attention from the research community. Non-coherent receivers do not require synchronization with a local carrier signal phase, therefore, they can only discern information out of the envelope of the pulse [38]. This means that there is a lower complexity advantage in comparison to a coherent IR-UWB receiver, which favors its use for most UWB receivers available in the literature.

A classical low-complexity architecture is shown in figure 2.2. The energy detector receiver amplifies an incoming pulse by means of an LNA, whose output is further band-pass filtered to notch out unwanted interference from other frequency bands. Next, the signal is squared, and integrated, which could be considered as a low-pass filtered autocorrelation output.

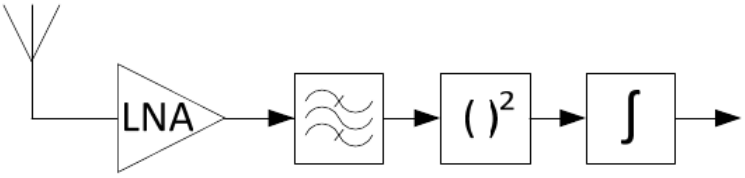


Figure 2.2: Energy Detector ED Receiver - Block Diagram

Mathematically, the operation of the ED receiver is given by [38]:

$$y_n[i] = \int_{t_{i,n}}^{t_{i,n}+T_1} r^2(t)\,dt \tag{2.1}$$

where $t_{i,n}$ represents the start time of the n-th integration window of the i-th transmitted symbol. $r^2(t)$ represents the output of the squaring stage in figure 2.2.

Practical implementations of the ED receiver can be coarsely divided into two categories: algorithm-intensive and threshold detector-based.

The algorithm-intensive systems preprocesses the signal by an ED receiver whose output has been sampled by a fast ADC, to then further apply algorithms such as designed to find the TOA. Implementations of this system concept are performed in [13] and [18]. In [13], a $500MHz$ ADC is used to obtain meter-level ranging accuracy. In [18], the sampled window is divided into small frames, and then the first frame whose center energy surpasses a certain threshold is considered to be the the TOA. A similar energy collection approach is also used in [31].

Unfortunately, it is highly sensitive to noise and interference since the receiver is based on energy detection. Furthermore, the accuracy performance is dependent on bin size; since these bins are on the order of ns, the ranging error achieved is in the order of decimeters.

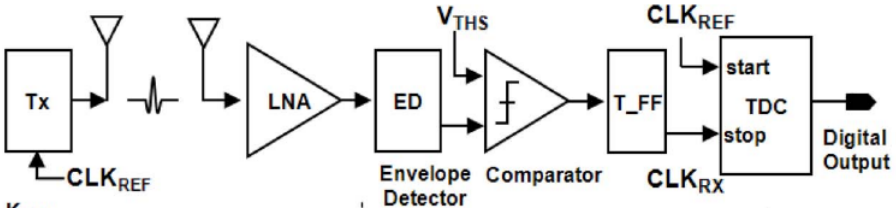


Figure 2.3: TDC-based receiver [22]

On the other hand, the threshold detector-based receivers use a comparator, flip-flop and a TDC to estimate the TOA. To do so, the output of the comparator is fed as a clock signal of the flipflop, whose output is fed as a stop signal of the TDC while the main clock of the system is fed as a start input signal. In [21] and [22] the same system concept is implemented, and a two-step TDC is used in order to obtain the TOA, with mm accuracy. However, the maximum range these receivers can achieve is below $10m$.

2.2. Proposed System

The whole system setup is composed of a gaussian-monocycle transmitter and a receiver. A simplified block diagram is shown in figure 2.4. The LNA block represents a chain of AGC and VGA stages so that the system does not saturate and can accommodate large ranges.

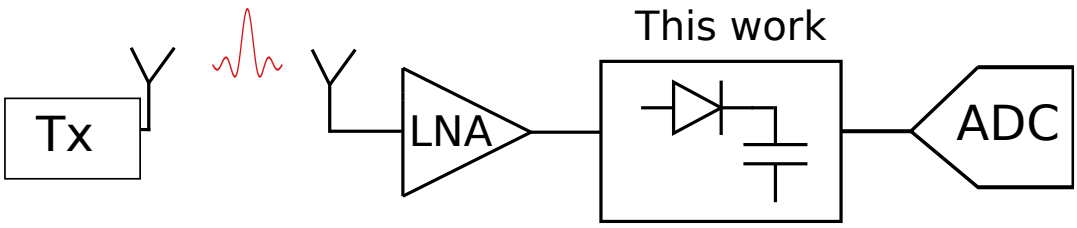


Figure 2.4: Top-Level block diagram of the whole system setup

As explained the previous section, energy-collector based receivers suffer from inaccuracies that can only be mitigated by increasing the complexity or the cost of the system (e.g GHz-sampling ADC). In addition, these type of receivers have a inherent noise enhancement due to their squaring operation. In addition, their time resolution is degraded as a the time of integration is increased [31].

The system proposed in this work, notated as a simple peak detector in Figure 2.4, achieves two purposes, namely:

- TOA estimation
- First-peak amplitude detection

The TOA estimation is inherently more precise as it is taken at the first peak arriving surpassing a predefined threshold. For highly accurate positioning systems, TOA estimation using a system bandwidth $2GHz$ can provide cm-level accuracy [7].

Furthermore, the system also estimates the first peak of an incoming pulse contaminated with noise and multipath components. Why is the first peak amplitude useful? with the first peak, we can estimate the the first path power in LOS condition, which in itself can achieve an standard deviation range error of approx. 54 cm [7].

Therefore, the receiver in this work can work can be thought of a coarse and fine positioning estimation receiver.

The system in this work is a non-coherent IR-UWB receiver. Therefore, it performs its operation directly on the received signal without preprocessing as in coherent receivers. A block diagram is shown in 2.5.

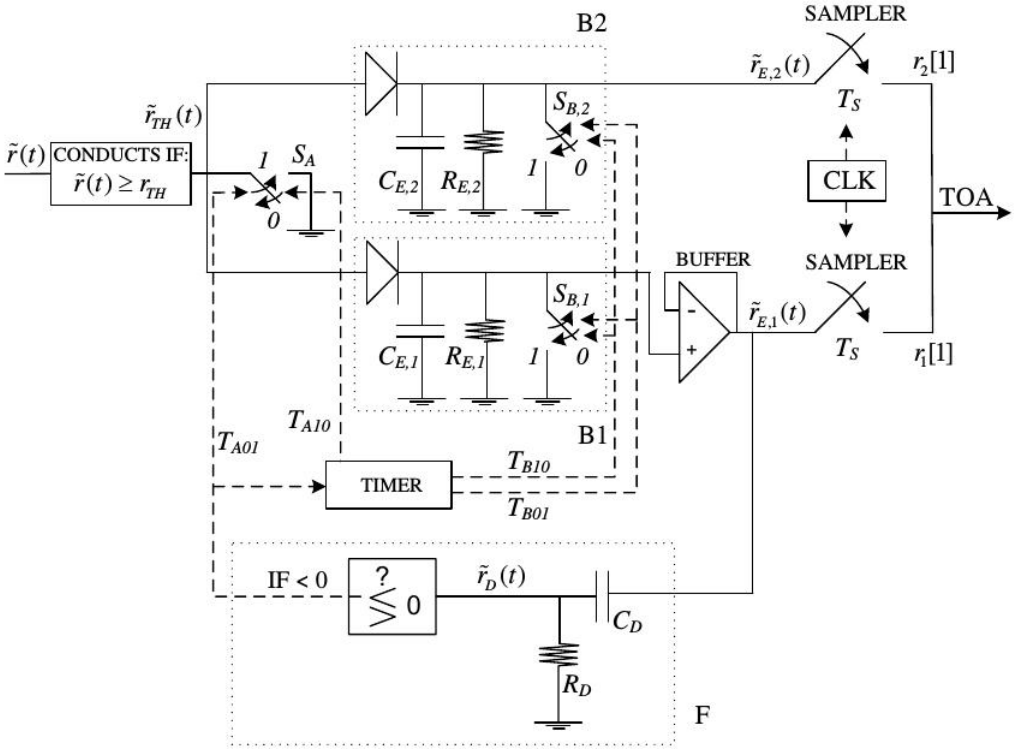


Figure 2.5: TOA Receiver Block Diagram - Block Diagram [7]

The receiver works in a time-window, in which an input pulse from the transmitter is expected. The time window, for this particular system, should appear every $10\mu s$.

The intended operation is as follows [7]: a signal $\hat{r}(t)$ is at the input. It is assumed that switches $S_{B,1}$, $S_{B,2}$ and S_A are open at $t = 0$. When $\hat{r}(t)$ surpasses a particular threshold r_{TH}, its envelope is computed by peak detectors B_1 and B_2. Both peak detector have different decay time constants. Taken to the limit, we could let $\tau_2 \gg \tau_1$, where τ_1 and τ_2 are the time constants for peak detector B_1 and B_2, respectively. The output of the fastest-decaying peak detector, B_1, is fed into a differentiator F, which computes the sign of B_1's output. When the differentiator output is negative, meaning that there is decay at its input, S_A goes into the short-circuit position at time $T_{A_{01}}$, thus ignoring subsequent possibly higher peaks at the input. This also sets a timer off, which waits for a sufficient time in which the outputs of B_1 and B_2 are sampled at the sampling period of T_s.

Then, at time $T_{B_{10}}$ $S_{B,1}$ and $S_{B,2}$ are switched on, thus erasing the stored peak from the peak detectors. Then, finally, at time $T_{B_{01}}$, $S_{B,1}$ and $S_{B,2}$ are opened again in the same way as S_A is opened. However, the latter is opened at a much later time $T_{A_{10}}$. Thus, every time window is at least separated $T_{A_{10}}$ seconds.

A more illustrative operation of the receiver is shown in Figure 2.6. The input signal at the receiver contains multipath components which can be larger than the first pah. Therefore, the receiver tracks and holds at peak of the first path that surpasses a threshold V_{th}. Then, at the output we have the first samples of two output signals $V_{out,1}[1]$ and $V_{out,2}[1]$, which are the outputs of the peak-and-hold detector B_2 and peak detector B_1 which decays the signal with time constant given by $C_{E,1}R_{E,1}$ (refer to figure 2.5). Assuming that $V_{out,1}[1]$ has negligible decay, then it becomes a DC value $V_{out,1}$. The time-of-arrival of the signal t_{TOA} can then be solved by the following simple equation:

$$V_{out,1}[1]\exp\left(\frac{-(t-\tau_{TOA})}{C_{E,1}R_{E,1}}\right) = V_{out,2}[1] \tag{2.2}$$

Then, solving for τ_{TOA}

$$\tau_{TOA} = t + C_{E,1}R_{E,1}\log\left(\frac{V_{out,2}[1]}{V_{out,1}[1]}\right) \tag{2.3}$$

where t is the time at which the sample has been taken.

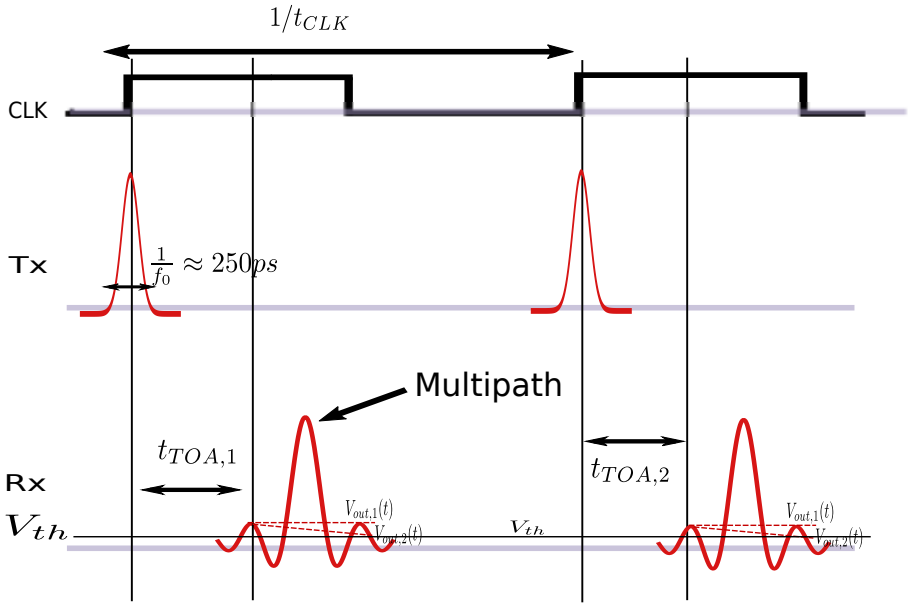


Figure 2.6: Timing diagram of the receiver operation

Then, the TDOA can be obtained from a pair of measurements. If there are five receivers, then it should be enough to perform TDOA measurements [17]. Then, once the distance collected, there will be a overdetermined system which is solved by means of numerical algorithms based on least-squares. An interesting survey of such algorithms based on least-squares is found in [32].

2.3. Threshold Detection-based system description and results

A threshold detection-based receiver was implemented by PhD student Yan Xie to prove the concept TOA estimation concept proposed in the previous section[1]. The system does not perform peak detection by storing the peak value. Therefore, only information about the time of arrival is available; no path intensity information. A coarse block system description of the circuit is presented below:

[1]The paper discussing its implementation is under writing at the moment this thesis was submitted

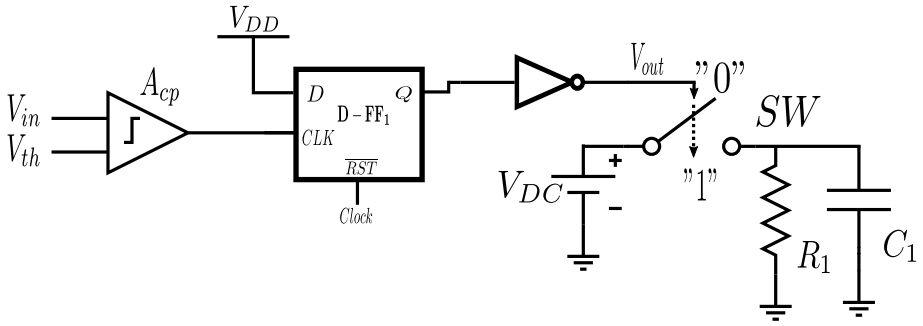


Figure 2.7: Simplified Diagram of implemented threshold detector

In Figure 2.7, an external LNA drives comparator A_{cp} at input port V_{in}. Furthermore, a user-defined threshold (which should be above the noise floor of the system) is also present at V_{th}. The output of the comparator is, then, fed into the CLK port of the latch $D-FF_1$. Its D port is fed with digital "1", and a clock signal is fed into the reset port $\overline{RST}$.

When $V_{in} > V_{th}$, A_{cp} will output a logical "1". Assuming $D-FF_1$ is positive-edge triggered, the positive edge generated by A_{cp} will cause Q to go to "1". This output is inverted and it is seen as a "0" at switch SW, which then isolates the voltage source V_{DC} from the RC network formed by R_1 and C_1, and starts a exponential decay discharge whose time constant is equal R_1C_1.

When CLK makes a transition to a digital "0", Q will still remain at "1" until the clock goes to "0" and resets the $D-FF_1$.

2.3.1. TOA measurements

The following measurements were done with a 14-bit, 10MHz ADC. The RC time constant used is $1.1\mu s$.

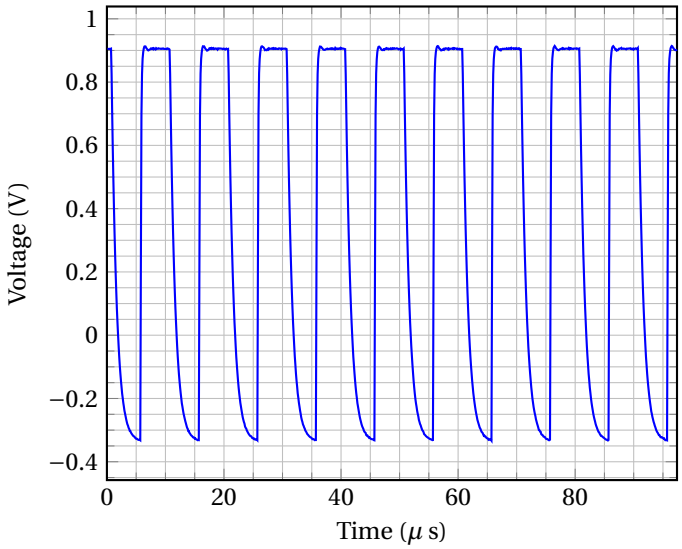


Figure 2.8: Waveform showing 9 thresholds detected in a 50ns time window each. Exponential decay time constant is $\tau = 1\mu s$

The exponential decays have been sampled. In this particular setup, 900 measurements of 9 cycles each (as shown in figure 2.8) were performed. Therefore, for the ith sampled point in the decay of the jth cycle, namely, $V_{decay}[i,j]$, we can solve back for a vector of TOAs, $\tau_{TOA}[i,j]$, for the jth cycle given the initial voltage V_1 and the time constant τ by using the following formula:

$$\tau_{TOA}[i,j] = t0 + R_1 C_1 \ln\left(\frac{V_{decay}[i,j]}{V_1}\right) \tag{2.4}$$

In each cycle, 23 samples of the exponential decay were taken. When solving back for $\tau_{TOA}[i,j]$, a list of TOAs is obtained, which are then averaged out. Therefore, for some jth cycle, the TOA average is taken:

$$\frac{1}{N}\sum_{i=1}^{N} \tau_{TOA}[i,j] = \mu_j \tag{2.5}$$

Finally, the TOA is obtained statistically.

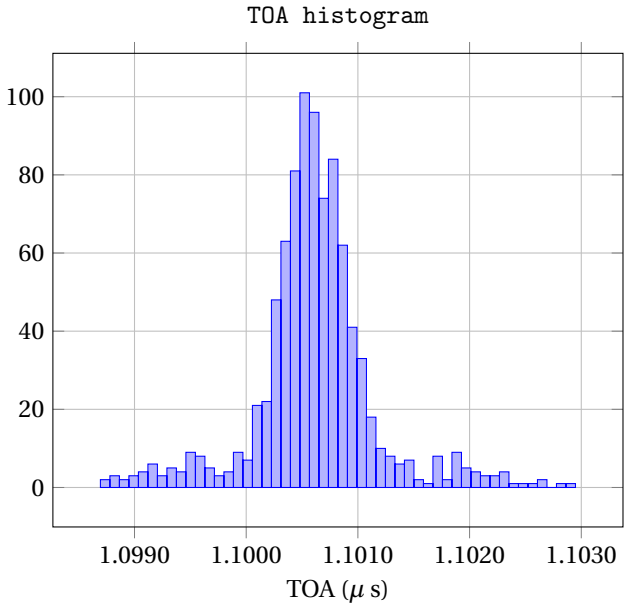


Figure 2.9: TOA histogram (50 bins) of all 900 TOA estimates. $\mu = 1.1006\ \mu s$, $\sigma = 0.547\ ns$

It can be seen that the sigma is 0.547, which translates into positioning error of 16.41 cm.

In general, it is difficult to map component performance to TOA accuracy. However, possible inaccuracy sources can come from the *RC* time constant due to not only tolerance values, but also parasitic inductances and capacitances present in both components. In addition, the quantization noise also plays a role in the error of sampled measurements.

It should be noted, though, that realizing large RC time constants is difficult and costly in an IC due to high-area consumption. An interesting option to explore, then, is that of a linear decay; a current-source in parallel with a holding capacitor.

2.4. Linear Decay Error Analysis

In previous section it was suggested that a linear decay could be used as a way to estimate the time-of-arrival. In this section, a theoretical error analysis will be done by means of numerical simulations.

The value to be decayed will also be some fixed voltage. In this case, it is assumed that it is a supply V_{DD}.

In order to obtain the time arrival τ_{TOA} from a sample, the following equation is used:

$$\tau_{TOA} = t_{sample} - (V_{DD} - V_{ADC,sampled}) \times \frac{C_0}{I_0} \tag{2.6}$$

where t_{sample} is the time at which $V_{ADC,sampled}$ is taken. C_0 and I_0 are some fixed hold capacitor and a constant current value, respectively.

An example of how the linear discharge waveform will look with it sampled values is shown in Figure 2.10.

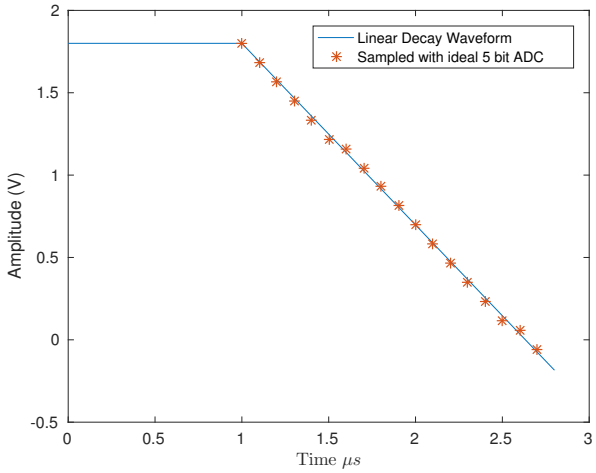


Figure 2.10: Linear Decay waveform example

The error in τ_{TOA} measurement can come from a different sources of inaccuracy, namely:

- Inaccurate value of C_0 due to fabrication errors, and parasitic capacitances in parallel with C_0 as well
- I_0 is usually implemented as a current mirror, which has a mismatch that is area dependent. In addition, if the current source is implemented on the IC, temperature variations can affect its value as well.
- Noise sources of the ADC such as quantization noise, jitter, etc.

In the following simulations presented, a DC value of $1.8V$ is decayed at $0.5\mu s$ (the time of arrival τ_{TOA}). Then, the error as modeled as follow:

1. The waveform is contaminated with artificial zero-mean Gaussian noise of RMS values ranging from $10nV$ to $100\mu V$.
2. This noisy waveform is then sampled by ideal ADCs which only take into account quantization noise. The number of bits are swept from 10 to 24 bits.
3. A percentage error is added to C_0 and I_0 in order to model possible deviations of the decay rate due to the non-idealities explained before.
4. The nominal values of I_0 and C_0 are $1\mu A$ and $1pF$, respectively.
5. The sampling frequency is fixed at 10MHz.

First, every sample of the ADC and its time-stamp[2] will be used to solve for a τ_{TOA} using equation 2.6. Then, an standard deviation σ_{TOA} of this collection of τ_{TOA} will be obtained. This is repeated for every resolution quantity (i.e. for 10,11,...,24 bits) and every RMS noise value. I_0 and C_0 are kept error-less, for now. The error is shown as $3\sigma_{TOA}$ in centimeters.

[2] An ideal DAC is used to provide the voltage out of the ADC codes

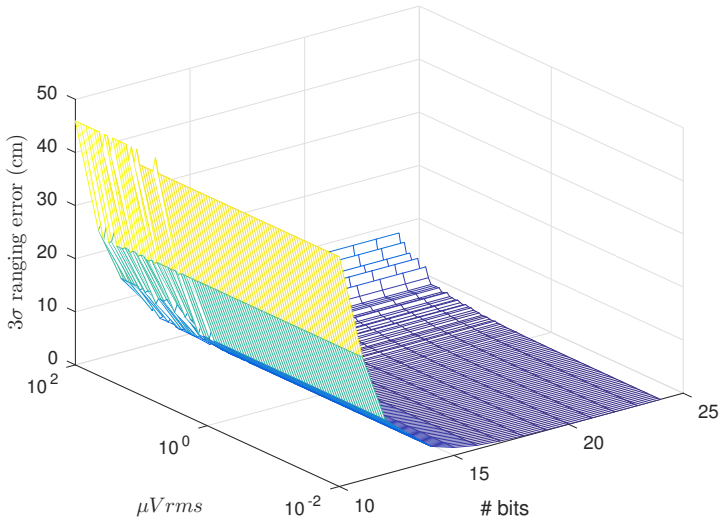


Figure 2.11: 3D surface plot of $3\sigma_{TOA}$ of the collected τ_{TOA}s as a function of noise voltage RMS and ADC resolution. $f_s = 10MHz$, $I_0 = 1\mu A$ and $C_0 = 1pF$

Under the assumptions made for the error modeling, Figure 2.11 reveals, as expected, that the standard deviation of τ_{TOA} is worse at high noise levels and low ADC resolution. In order to see this more clearly, a simple graph showing the relationship of $3\sigma_{TOA}$ as a function of noise while keeping the resolution fixed at 10 bits is shown in Figure 2.12.

Figure 2.12 shows that within the range $10nV_{RMS} - 4\mu V_{RMS}$ the error is mostly dominated by quantization noise. This is expected as the noise standard deviation is smaller than the quantization step. However, starting from approximately $10\mu V$, the error does sudden jumps. This is due to the coarse steps of the vector noise generated. Nonetheless, it can still be noticed that the variations are basically are basically around 4%, which still shows that quantization noise dominates in this entire noise range. It should be point out that, despite the variations in ranging error, the nominal ranging error is completely unacceptable for the accuracy specifications we seek in this thesis.

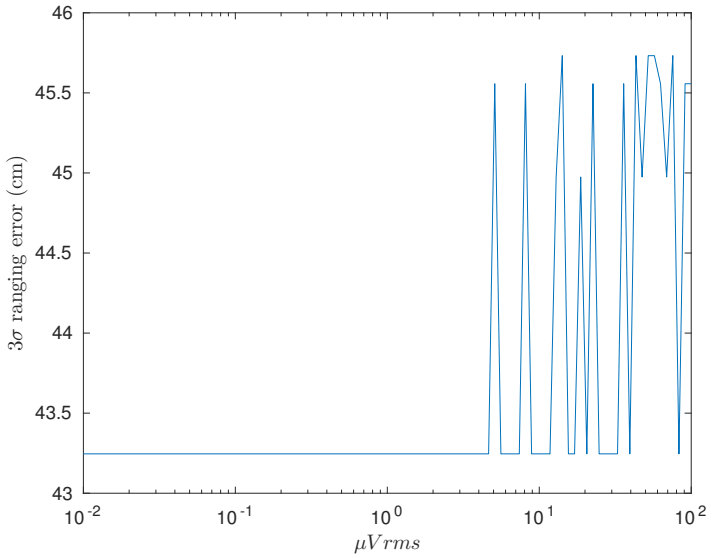


Figure 2.12: $3\sigma_{TOA}$ as a function of noise with 10 bit resolution

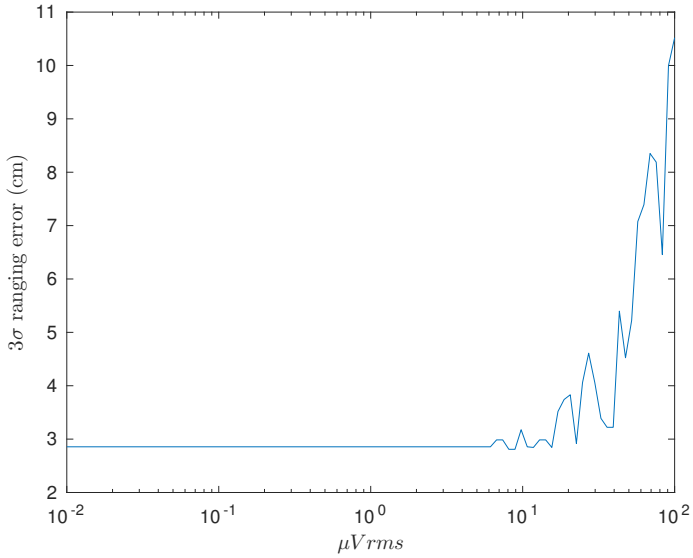


Figure 2.13: $3\sigma_{TOA}$ as a function of noise with 14 bit resolution

Noise starts to have a more pronounced effect at higher resolution values, however. In Figure 2.13, higher noise values start to affect the ranging error considerably. This is expected, as higher resolution means smaller quantization steps, which means that high noise values will be comparable to them. Consequently, the ranging error starts increasing; the linear decay function proves inaccurate then.

Now, it should be noted that all these simulations were done assuming I_0 and C_0 were ideal. The approach of averaging results in unacceptable range errors when fixed percentage deviations are considered for I_0 and C_0. For a -1% error in the current I_0 and a 20% in C_0, which could be due to considerable parasitic capacitances from the current source, the error as a function of resolution and Gaussian noise is shown in Figure 2.14.

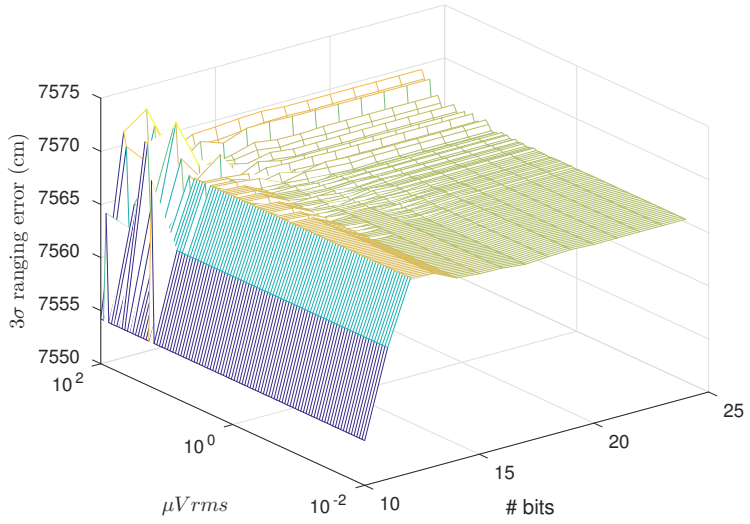


Figure 2.14: 3D surface plot of 3σ of the collected τ_{TOA}s as a function of noise voltage RMS and ADC resolution. $f_s = 10MHz$, $I_0 = 1\mu A - 1\%$ and $C_0 = 1pF + 2\%$

As expected, errors in the current source I_0 and the hold capacitor C_0 can be extremely detrimental to the ranging error. The basic problem we have to cope with is to determine the non-ideal slope from the ADC measurements. An excellent mathematical algorithm to cope with this problem is to perform a linear square

estimation of the sampled curve. The algorithm assumes that we are trying to fit a data set of the following form:

$$\mathbf{Y} = \mathbf{T}\hat{\beta} + \epsilon \tag{2.7}$$

where **T** and **Y**, in this case, would be the time-stamps and the output voltages of the DAC (converting back from the ADC operation). If we put our **T** vector in the following form:

$$T = \begin{bmatrix} 1 & 1 & 1 & \dots & 1 \\ t_0 & t_1 & t_2 & \dots & t_n \end{bmatrix}^T$$

Then, the solution that minimizes the least square of the error $\mathbf{e} = \mathbf{Y} - \mathbf{T}\hat{\beta}$ is given by [6]:

$$\hat{\beta} = (\mathbf{T}' \times \mathbf{T})^{-1} \times (\mathbf{T} \times \mathbf{Y}) \tag{2.8}$$

Applying this procedure, the slope can be estimated more precisely. As the noise has a mean of 0, then its values are expected to revolve around the decaying waveform. The surface of the $3\sigma_{TOA}$ shown in Figure 2.15 shows a dramatic reduction in its magnitude compared to that of 2.14.

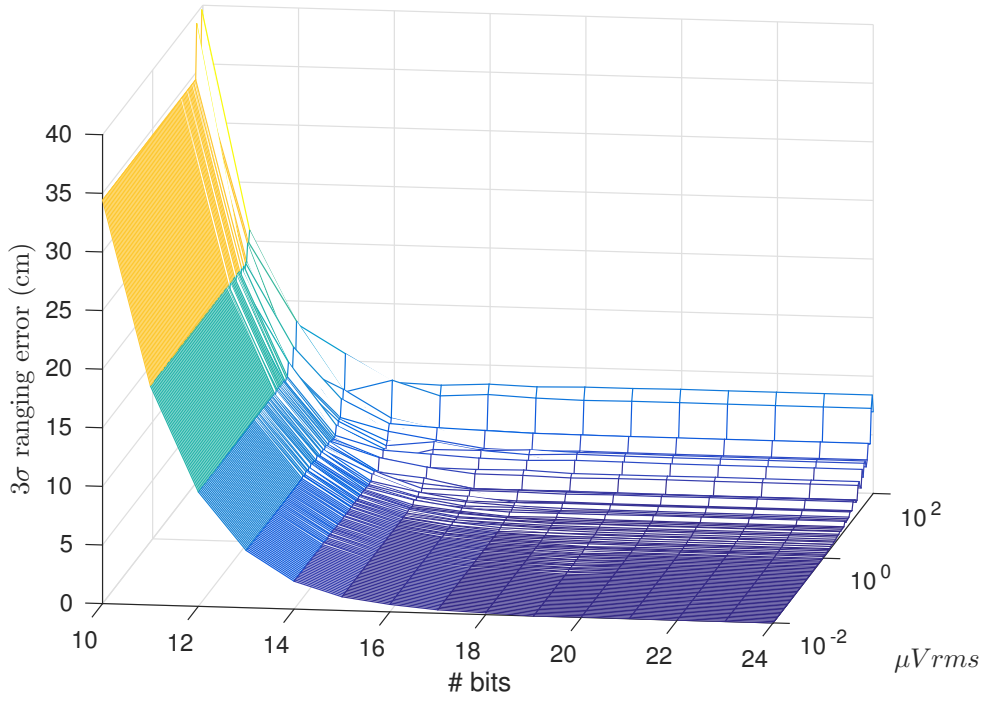


Figure 2.15: 3D surface plot of $3\sigma_{TOA}$ of the collected τ_{TOA}s as a function of noise voltage RMS and ADC resolution. $f_s = 10MHz$, $I_0 = 1\mu A - 1\%$ and $C_0 = 1pF + 2\%$. Estimation done using linear least squares

Therefore, we conclude that a linear decay provides more flexibility in the digital domain when it comes to reduce its non-idealities with respect to time of arrival τ_{TOA} accuracy. Due to its linear nature, errors will be propagated in a more linear fashion, while in an exponential decay the propagation can be highly non-linear.

2.5. Ranging accuracy budget specification

In the previous section it was demonstrated that using linear least squares under the assumption of additive Gaussian and quantization noise can provide an accurate estimation of the TOA. An important assumption

made in the simulations in the previous section was that the linear decay was going to happen from a predefined voltage and not from a detected amplitude. This implies that the peak detecting function in time can be decoupled from detecting its actual amplitude value[3].

If we assume that the peak detection in time can be a separate function in the system, then we can expect there will be a finite delay from the moment the peak has been detected until switching on a current source to perform the linear discharge. Therefore, we would like to reduce the variation or dispersion of this delay.

A decision must be made about how much of the $10cm$ error available would be allocated to the delay dispersion of peak detector and to the current source-capacitor-ADC interface. The decision in this thesis is to give the former $7cm$ of the error while only $3cm$ to the latter. This is because there are more tools available to correct for the errors produced at the current source-capacitor and ADC interface, while $7cm$ given that reducing delay dispersion is a rather difficult task.

The resolution and noise budget are determined from inspecting Figure 2.15. It can be noticed that starting from 15 bits, the ranging error starts decreasing below 5cm while having a less than $1\mu V$. In order to clarify this, we plot the ranging error as a function of noise while fixing the resolution at 15 bits..

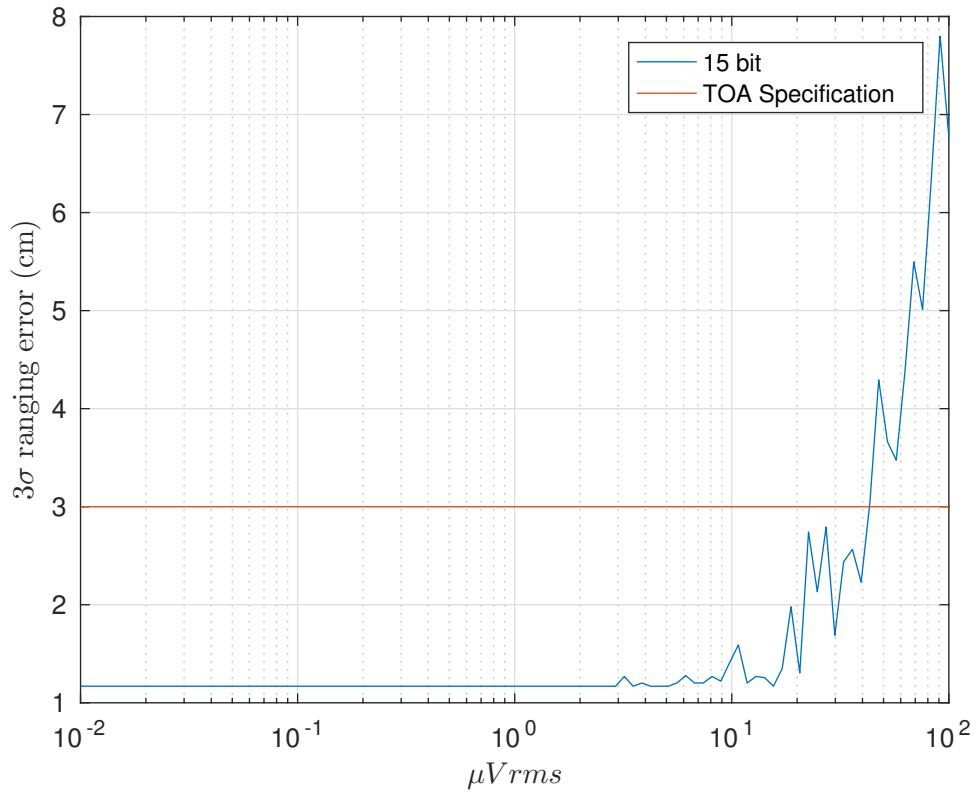


Figure 2.16: Ranging error as a function of noise RMS with a TOA or ranging error specification line

From Figure 2.16, we can deduce that the maximum noise voltage tolerated is approximately $40\mu V$.

This means that for the peak detector, we allow a maximum delay dispersion of $\frac{7cm}{3\times10cm/s} = 233ps$.

This means that the simple threshold detector to be designed (mentioned as a task in Chapter 1.6, must also have the delay dispersion accuracy.

The peak detector to be implemented will also have an error in amplitude detection. Unfortunately, no literature was found on how this error can affect the ranging accuracy using first-path (or first peak) based ranging. In addition, this error will probably need indoor wireless measurement campaigns, which are time

[3]A more in-depth treatment about this concept will be done in Chapter 3.

consuming. Therefore, we will arbitrarily set a maximum tolerable error of 50%.

2.6. Receiver specifications, sensitivity and Link Budget

The receiver in this work has the following specifications:

Table 2.1: Link Budget of the UWB-IR Receiver

Characteristic	Value
Center Frequency (f_0)	$4GHz$
Pulse Repitition Frequency ($1/T_r$ or PRF)	$100kHz$
Tx Power	-8.3 dBm
Tx Antenna gain	0dB
Bandwidth (B_w)	$2GHz$
Path Loss at $300m$ (L_{300m})	-95dB
Rx Antenna Gain	0 dB
Rx Noise Figure (NF)	3 dB
Rx Noise Power (-174dBm/Hz + $10\log_{10}(B_w)$ + NF)	-77 dBm
Link Margin (Tx Power + $10\log_{10}(B_w/PRF)$ - L_{300m} - Rx Noise Power)	11 dBm

The center frequency of $4GHz$ is chosen so as not interfere with HiperLAN band at $5GHz$. Furthermore, the system bandwidth is chosen to be $2GHz$ since an increasing beyond that does not provide significant improvement in accuracy for TOA [7].

The data rate choice is somewhat arbitrary. In general, low PRF are chosen so that they last longer than UWB indoor channel response, which lasts for about $100ns - 200ns$. Another reason is that it gives enough time to do data processing before the next pulse arrive.

Since the receiver has a highly dynamic and non-linear operation due to the peak detector after the LNA, we make an assumption that the output the of the LNA is the output of the whole receiver. This is justified by the fact that the LNA, since it is the first stage in the system chain, will have an output noise that largely dominates in comparison to that of the peak detector. From table 2.1, the minimum detectable signal (MDS) power is given by:

$$P_{in,min} = -174\text{dBm/Hz} + 10\log_{10}(B_w) + \text{NF} \approx -78dBm \tag{2.9}$$

From the UWB mask limitation, we know that the maximum transmit power is given by:

$$P_{tr} = -41.3\text{dBm/MHz} + 10\log_{10}(B_w\ [MHz]) \tag{2.10}$$

Which for a system bandwidth $B_w = 2000$ (Bandwith should be in MHz units) results in maximum transmit power P_{tr} of $\approx -8.3dBm$.

Regarding the maximum average power, an upper bound can be obtained assuming that the pulse repetition frequency is much lower than the resolution bandwidth of $1MHz$ used for average power measurement. Under those conditions, the maximum average power transmitted is approximated by [14]:

$$P_T^{MAX} \leq \frac{0.075pW \times B_w^2}{PRF} = 34.77dBm \tag{2.11}$$

P_T^{MAX} is equivalent to the following expression:

$$P_T^{MAX} = P_{tr} + 10\log_{10}\left(\frac{B_w}{PRF}\right) \tag{2.12}$$

Then, the power of the transmitted signal can be calculated as follows:

$$P_{rx} = P_T^{MAX} + G_t + G_r - L_{FP} \tag{2.13}$$

where P_{tr} is the transmitted power, G_t and G_r are the transmission and receiver antenna gain, respectively. L_{FP} is the first path loss power dependent on distance d and center frequency f_0 (assuming LOS condition, where the first path-loss exponent is 2) and it is given by the following expression [7]:

$$L_{FP} = -10\log_{10}\left(\left(\frac{c}{4\pi f_0 d}\right)^{n_{FP}}\right) \tag{2.14}$$

It is found, then, that at 300 meters, considering the noise figure of the receiver and its bandwidth, there is a link margin of 11 dB for LOS conditions.

2.7. Conclusion

Non-coherent receivers for UWB present several advantages with regards to their coherent counterparts with respect to low-complexity implementation, which has made it quite attractive for the academic community to do further research on. Essentially, it has been understood that for practical and low-cost UWB systems, optimality has to be sacrificed in favor of low-complexity implementations. The challenge relies on reducing the accuracy penalty with respect to coherent receivers..

Measurements of the threshold detector implemented show that there is an standard deviation of 16 cm. One of the most probable causes is the decay time constant and the quantization noise of the ADC. Since well-defined exponential decays with long time constants are costly to produce in an IC, a linear discharge is proposed as an alternative. Its possible of sources of error are studied and it is concluded that even at relatively large departures from the ideal linear decay slope, Linear least square fitting of the digitized samples contaminated with Gaussian noise can correct for the slope and restore the the accuracy. It was established that for a $4cm$ triple standard deviation, the maximum RMS noise allowed is $40\mu V$ with a 15 bit ADC.

Furthermore, using simple assumptions on the peak detector, a maximum delay dispersion of $233ps$ is allowed in order to have a final accuracy of $10cm$ in ranging.

The link budget analysis demonstrates that, assuming LOS conditions, the receiver can have a link margin of 11dB at 300 meters, which allows its use in short and mid-range distance positioning.

3

Analog Peak Detection

In this chapter, the functionality of the peak detector will be abstracted away in terms of a generalized block diagram. Then, the peak detectors existing in literature will be classified into 2 more detailed block diagrams which implement the generalized block diagram.

From there, we will be able to classify most peak detectors implemented in literature under any of those two block diagram implementations.

Based on the requirements derived in chapter 2, a choice will be made among the two peak detector block diagram implementations and an particular circuit architecture will be chosen.

3.1. Peak Detection concept

A peak detector function in electronics usually processes some input signal $x(t)$ in either of the following ways:

1. It produces an output that is proportional[1] to the last largest peak of the input signal $x(t)$.
2. It produces an output wherever the first derivative of $x(t)$, $\frac{dx(t)}{dt}$, equals 0.

The function described in item 1 could be best described as a continuous application of a $Max()$ mathematical function. While the second easily be described as a signum function applied to the time derivative of $x(t)$. The signum function is commonly defined as follows:

$$sgn(x) = \begin{cases} -1 & x < 0 \\ 0 & x = 0 \\ 1 & x > 0 \end{cases}$$

The following subsections 3.1.1 and 3.1.2 will expand on their block diagram and circuit implementations.

3.1.1. Max function

The peak detector function stated in item 1 above can be abstracted away mathematically by the $Max()$ function, as shown in Figure 3.1

Figure 3.1: Generalized Peak Detector Block Diagram

[1] Typically, this proportionality factor is equal to 1

The max function is applied to two values, which are either some previous peak detected x_{prev}, or the current input signal value $x(t)$. It is assumed that x_{prev} is initialized with the first value of $x(t)$.

How is this $Max()$ function implemented at the block diagram level with more recognizable electric circuit functions? Two common block diagrams implementing the function are shown in Figure 3.2:

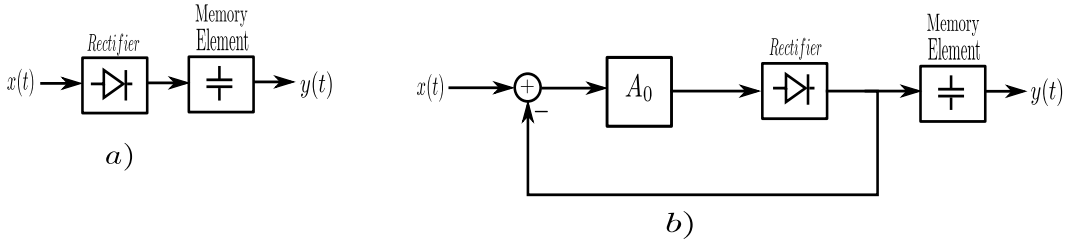


Figure 3.2: Block Diagrams implementing the $Max()$ function

Figure 3.2.a) shows the $Max()$ function being implemented by means of a rectifier (an element only conducts in one way) and a memory element (commonly, a grounded capacitor). Two practical implementations exist for 3.2.a). The rectifier function can be implemented using a diode or a transistor. They are both shown in Figure 3.3. Another way to see this topology is being noticing that the current flowing through the hold capacitor or memory element is the derivative of the voltage, and the diode opens at the zero crossing of this current. Therefore, the capacitor is working as both memory element and differentiator.

Despite its simplicity, the implementation in Figure 3.3.a) suffers from many drawbacks. In particular, diode D_1 usually has a $0.7V$ voltage drop across it, which prevents from discerning changes at the input signal lower than this value. This phenomenon can probably be tolerated in high voltage designs ($5V$ or more), but it is not applicable for low voltage ones.

On the other hand, the implementation shown in Figure 3.3.b) is more amenable to low voltage designs, since the gate-to-source voltage V_{gs} of M_1 drop can be much less than $0.7V$. In particular, if we bias the overdrive voltage $V_{gt} = V_{gs} - V_{th}$, where V_{th} is M_1's threshold voltage, close to $0V$ (sub-threshold biasing), then we can have a low V_{gs} drop, and when V_{gs} is less than 0, M_1 will not be sourcing current to charge C_{hold}.

Likewise, M_1 implements the rectifying function in figure 3.3.c). While M_1 is on, I_{in} is copied to M_2, which charges C_{hold}, integrating the current to a proportional voltage.

Unfortunately, both implementations in 3.3.b) and c) suffer from several drawbacks. In particular, the circuit shown in 3.3.b) suffers from poor high-frequency characteristics as it needs to be biased near its subthreshold region. Increasing I_{bias} with its required bias voltage at its gate improves its speed. However, M_1's behaves, then, less as a diode and more of a simple voltage buffer with asymmetric characteristics. Likewise, in 3.3.c), M_1 also suffers from poor high-frequency characteristics, as it has virtually zero drain current when M_1 is shut off.

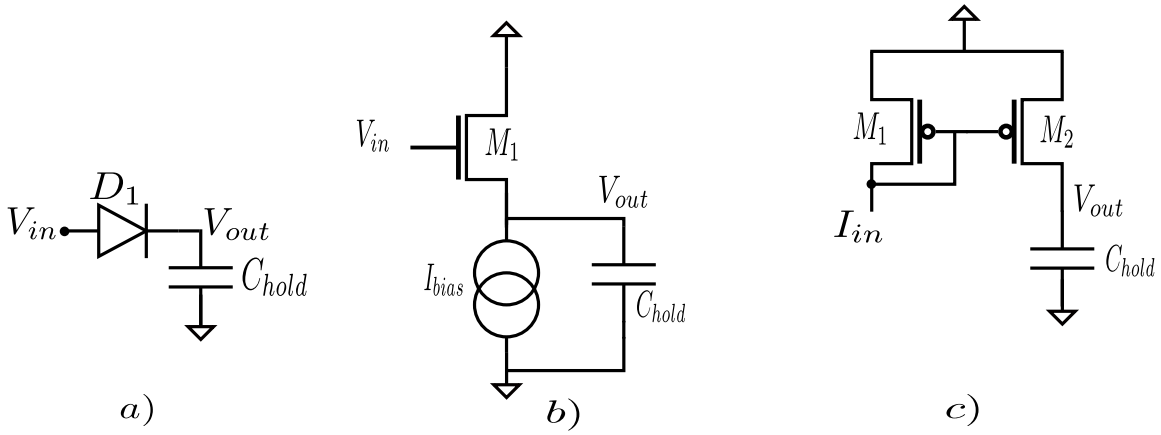


Figure 3.3: Circuit Implementations of block diagram shown in Figure 3.2.a)

Figure 3.2.b), on the other hand, implements the same function, but in a feedback configuration, where A_0 represents some gain element (which could be an Op-Amp, OTA, etc.). The advantages of feedback is a peak detectors is the error reduction due to non-ideal switching elements (such as diode, current-mirrors, etc). Figure 3.4 shows an example implementing the feedback block diagram.

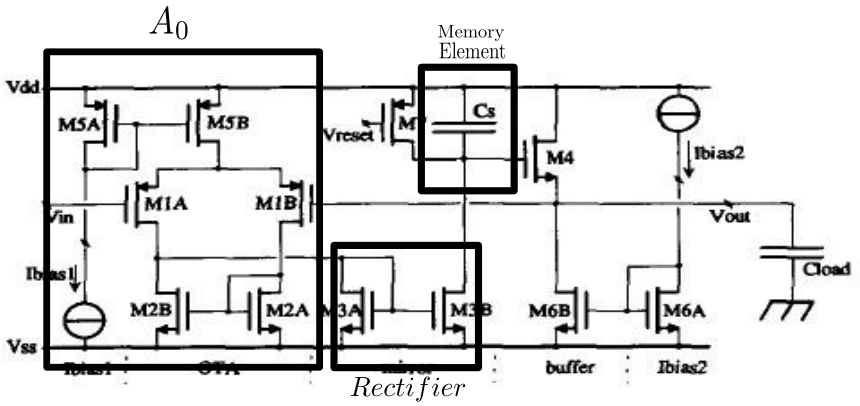


Figure 3.4: Peak Detector according to Kruiskamp [25]

The operation of the circuit can be coarsely described as follows. The block implementing A_0, will do whatever at the output to keep its input differential voltage at 0. Therefore, it will drive the rectifier

The operation of the peak detector is as follows, if there is an input with a negative excursion at V_{in} which is smaller than that of V_{out}, the drain of $M1A$ goes up, thus turning on the diode-connected transistor $M3A$, whose current is then copied into $M3B$. Therefore, $M3A,B$ form a rectifying current-mirror. $M3B$ discharges C_s and then it goes to V_{out} charging a capacitor C_{load} by means of a NMOS source follower that also level-shifts the voltage of C_s down.

3.1.2. Derivative + Signum function

Another way to implement a peak detector is by means of time-differentiating its input signal $x(t)$ and produce an output at the zero-crossing threshold, modeled as a signum function $sgn()$, as shown in Figure 3.5.

The output of this system is a digital signal generated every time $dx(t)/dt = 0$. How can we make this system output the actual value of the peak? An idea would be to have the zero-crossing output signal turn a switch sw off every time a peak has been found.

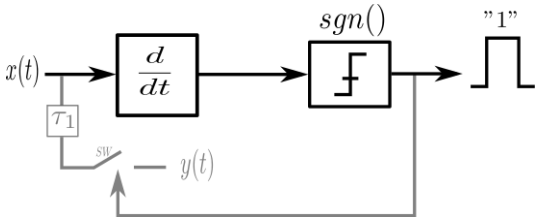


Figure 3.5: Differentiator + Zero-crossing detector Block Diagram

However, this poses a practical implementation issue. Usually, a comparator or some sort of decision stage is best suited to implement $sgn()$, and these blocks have a finite delay, which means that it is unrealistic to expect that we will be able to switch sw at the peak of $x(t)$ without incurring into an error. Therefore, a finite analog delay τ_1 is added in between $x(t)$ and sw, to compensate for the time function $sgn(t)$ will take to make decision.

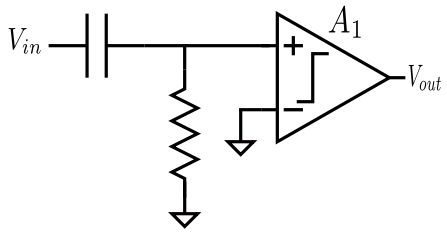


Figure 3.6: Possible peak detector implementation

A simple implementation of this block diagram, without the option of having an analog output, is shown in Figure 3.6. The simple RC circuit performs time differentiation while the zero-crossing detection is done by comparator A_1.

A drawback of this implementation is that the RC network will attenuate the input signal by some factor, and this will require comparator A_1 to have a increased resolution. Another option could be implement the differentiator actively. However, active implementations typically involve an Op-Amp or OTA, the speed advantage with respect to the feedback peak detector topologies will be limited.

3.2. Design of the Peak Detector Block Diagram

From the requirements established in Chapter 2, we see that the time detection of the peak is the most important factor. However, it was also established that the peak of the first peak is also important if we are to design a peak detector that could easily be extended into an event-driven system that is able to measure the different magnitude and time of arrival fo the multipath components.

The first decision made is to not use the the open or closed-loop topologies from the family of peak detectors which implement the $Max()$ function because of the following reasons:

- These topologies only allow for the slow linear discharge to be started at the value of the peak found. If this peak is small (e.g. transmitter is several tens of meters away), then a very small discharge current is needed, much less than $1\mu A$ for a $1pF$ capacitor, which are difficult to keep temperature-stable.
- The topologies implementing the closed-loop block diagram are limited to the speed or high frequency behavior of the block implementing A_0. High speed might be achieved by sacrificing gain, which would hinder the ability of block A_0 to overcome the diode drop[2].
- On top the last argument, at least two extra comparators would be needed to monitor that the predefined threshold is surpassed and that a peak has been found. If we are going to somehow add them to a feedback topology that is already sacrificing gain/accuracy for speed, then why not go directly to differentiator and zero-crossing detector based topology? This architecture already includes a comparator that monitors when a peak has been found.
- While it is true that the comparators mentioned above could, in theory, be replaced by a differentiator as originally proposed in [7], it is the aim of this thesis to design a topology that could be process scalable. Two comparators followed by a logic block that provides the first-peak detection functionality explained in Chapter 2 are favored by process scalability rather than analog functions.
- The topologies implementing the open-loop block diagram offer an unacceptable trade-off between high-frequency behavior and rectifier behavior[3]; biasing them in saturation causes unacceptable droop at the hold capacitor C_{hold}, which would force the use of GHz ADCs to measure the peak.

Now, we modify the block diagram shown in Figure 3.5 in order to suit our requirements. The new block diagram with recognizable circuit functions is shown in Figure 3.7.

[2] An investigation of the output DC-error and speed trade-offs between feedback-based peak detector topologies limit is proposed in detail in Chapter 6

[3] Except for the basic diode + capacitor topology, which consumes a large voltage drop. This feature is not tolerable for low supply designs, such as $1.8V$ for a $0.18\mu m$ CMOS process

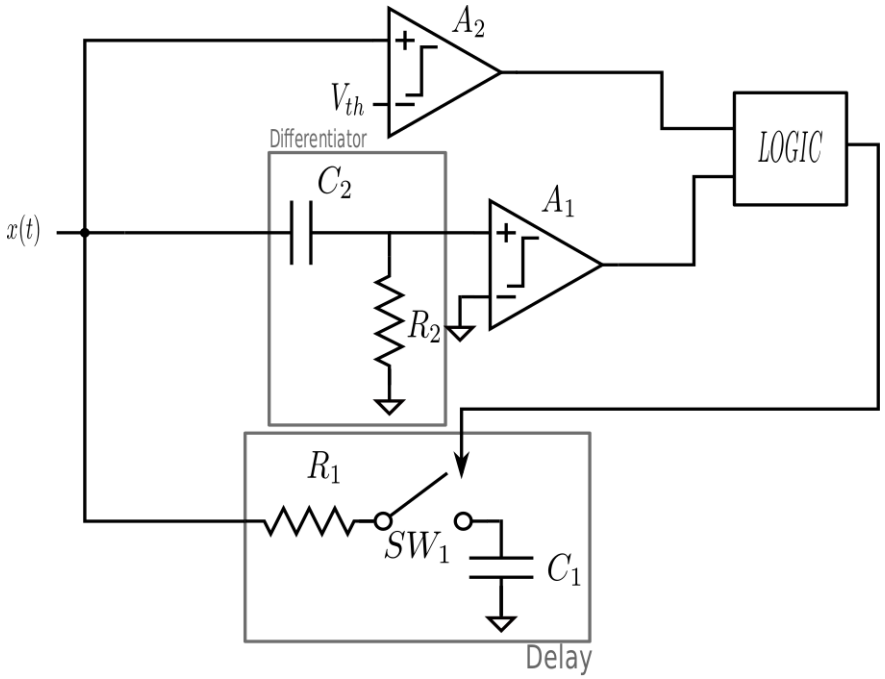


Figure 3.7: Modified differentiator and zero-crossing detector according to the system requirements

The block diagram in Figure 3.7 uses two comparators A_1 and A_2, which monitors whether $V_{in} > V_{th}$, and A_1, which produces an output at the zero-crossings of dV_{in}/dt. Finally, the LOGIC block uses the output of A_2 as a condition; within the time frame in which A_1 produces a digital "1", the LOGIC block opens SW_1 as A_1 is detects a zero crossing and prevents from being closed again due to the following multipath components from V_{in}. Figure 3.8 shows the ideal waveforms of the block diagram.

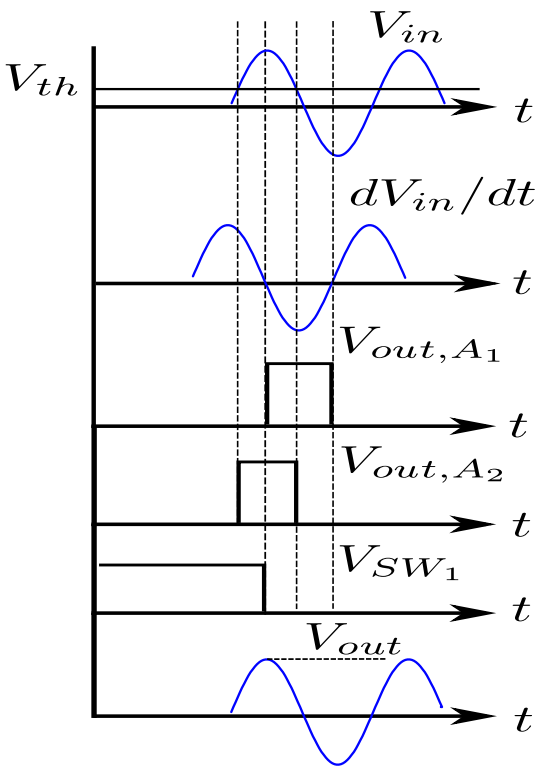


Figure 3.8: Waveforms demonstrating the ideal working principle of the block diagram in Figure 3.7 (Delay block not considered)

The block diagram of our peak detector system has a particular implementation issue. There needs to be a delay block, otherwise, the LOGIC block would not be able to switch SW_1 on time, producing an error at the peak detected.

How do we implement this delay block? The best option would be to use an all-pass filter, as they produce a delay as a function of frequency while having a constant magnitude. Unfortunately, they are usually implemented as lattice or bridge-T networks that require the use inductors [37], which are rather difficult and costly to realize on ICs. Therefore, a simple low-pass RC network is chosen.

Now, a modification can be noted in order to reduce the complexity of this implementation. The lossy RC differentiator transfer function is:

$$H_{HPF}(s) = \frac{R_2}{1/sC_2 + R_2} \tag{3.1}$$

This suggest that, in the delay block in Figure 3.7, there is also a lossy differentiator across R_1. This means that we can connect the ends of R_1 to a comparator and we would, then, have the same operation. The final modified block diagram is shown in Figure 3.9.

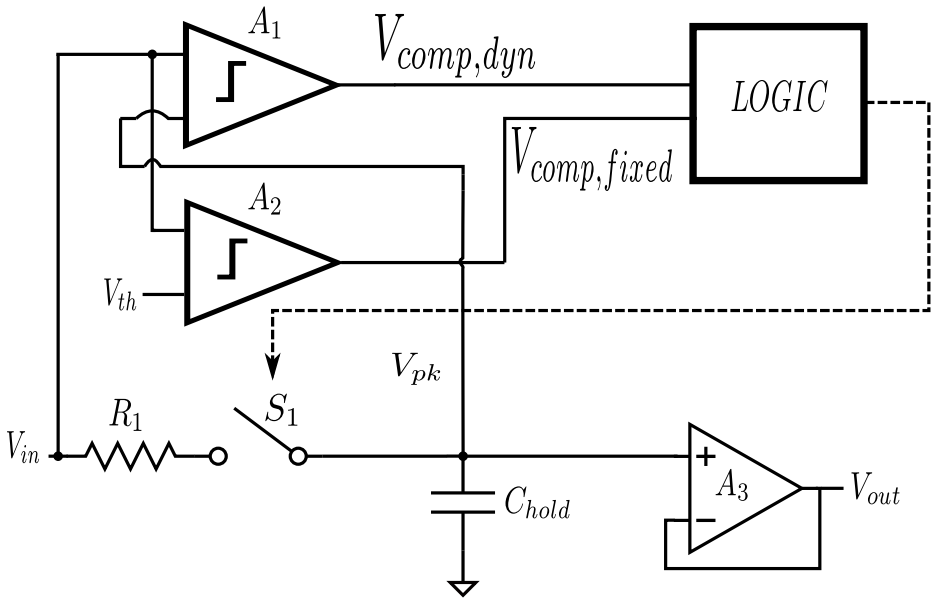


Figure 3.9: First-Path Peak Detector General Block Diagram

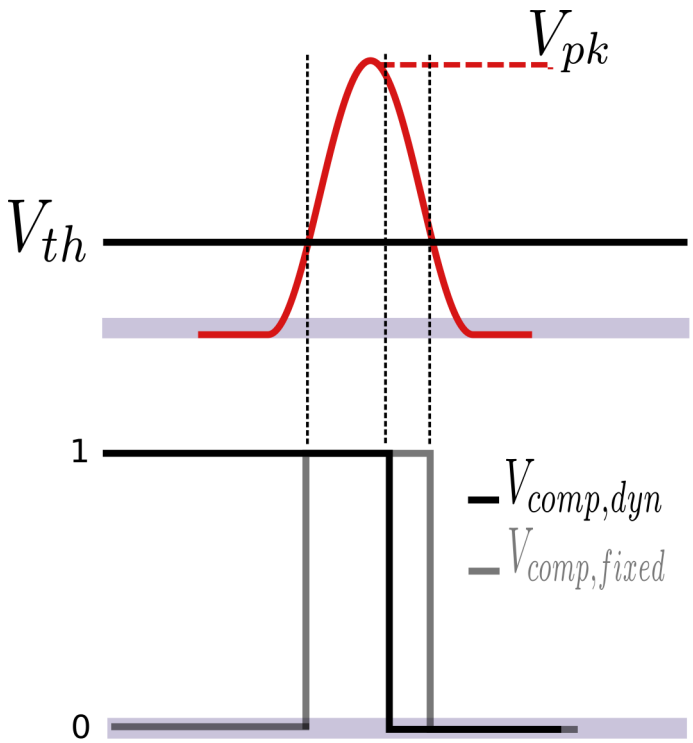


Figure 3.10: Idealized comparator outputs with respect to an input signal with a predefined threshold

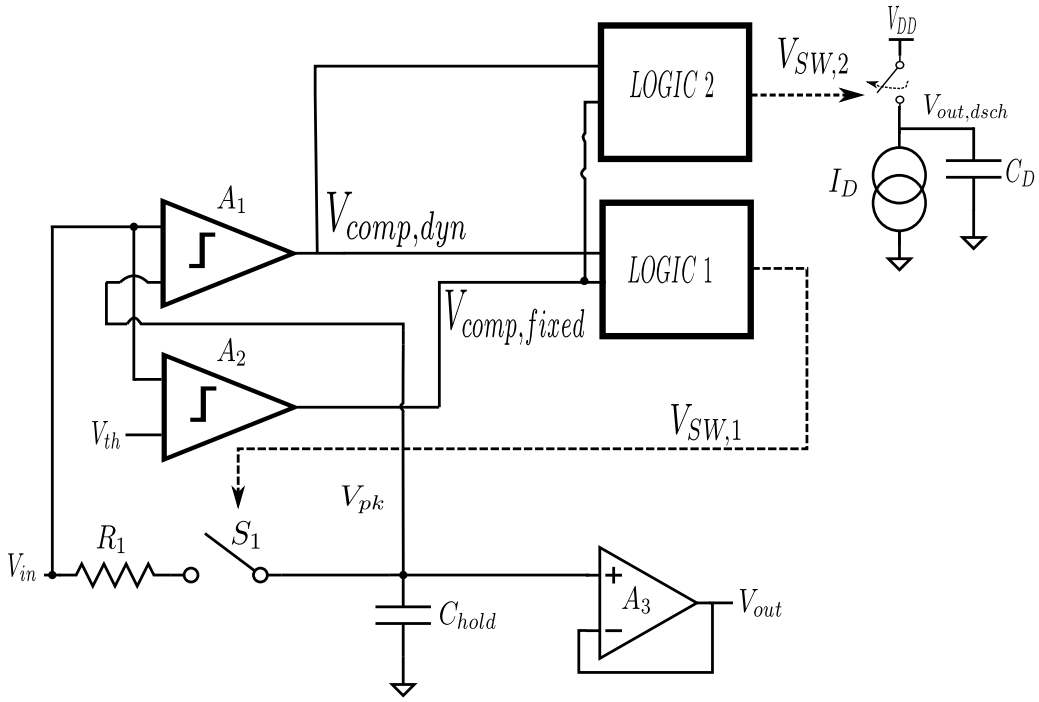


Figure 3.11: Final Peak Detector Block Diagram

The idea of comparator A_2 in Figure 3.9, is to monitor whether $V_{in} > V_{th}$. When this happens, it means there will a peak in the input. Therefore, A_1 will output a digital 1, which will make the LOGIC block close the switch so that the input is tracked. Then, once the peak has been detected, A_1 will output a digital 0, and this will force the LOGIC block to open the switch for the rest of the clock period. This will happen while A_2 will still be outputting a digital 1, which will become 0 once the signal goes below the threshold.

It should also be noted that the basic form of the peak detector including only comparator A_1, switch S_1, R_1 and C_1 has already been published in [24].

An ideal waveform showing the operation described above is shown in Figure 3.10.

Now, there needs to be an extra logic block that informs when the peak has been found. This logic block should only output a logic value once and stay there for the rest of the clock period. This logic's digital output will switch turn a current source I_D in order to decay a parallel capacitor C_D, as explained in Chapter 2. The final peak detector block diagram is shown in 3.11.

Therefore, we have finally arrived at a peak detector system that effectively orthogonalizes the amplitude detection from the time peak detection. An error in amplitude peak detection now does not affect TOA estimation anymore; the linear discharge at $V_{out,dsch}$ starts at well-defined voltage, so there is one less source of error in the TOA.

The operating principle of this block diagram is shown in Figure 3.12.

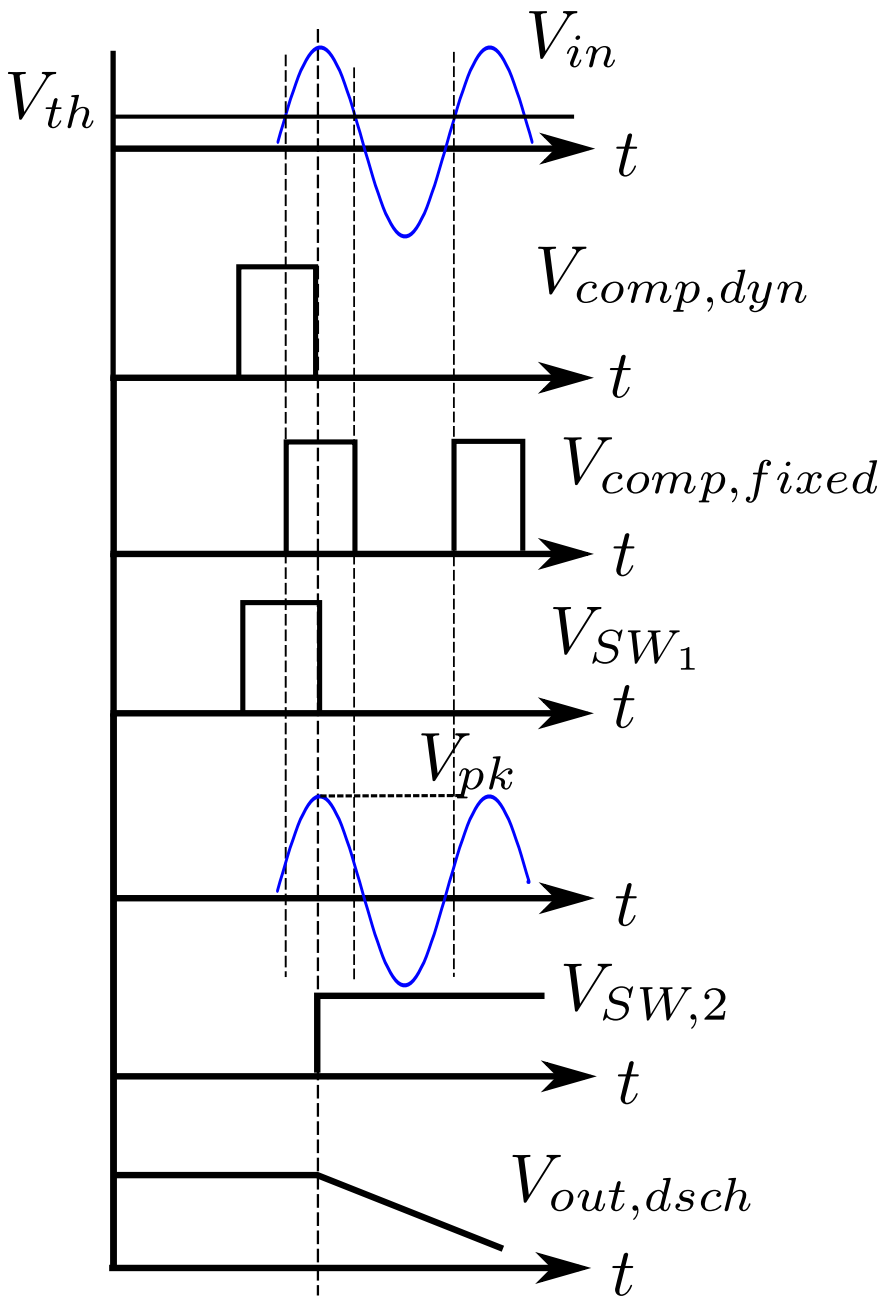


Figure 3.12: Waveforms demonstrating the operating principle of the block diagram in Figure 3.11 in one clock period

In Figure 3.12, the functions the logic blocks need to perform are more clear. $V_{SW,1}$ effectively copies the functionality of $V_{comp,dyn}$. However, when $V_{comp,dyn}$ does a transition from high to low (i.e. a peak has been detected) while $V_{comp,fixed}$ is high (i.e. the waveform instantaneous amplitude is higher than V_{th}), then $V_{SW,1}$ goes low and does not accept any incoming pulse until the next clock period. In the case of $V_{SW,2}$, this goes high only when $V_{comp,dyn}$ goes low while $V_{comp,fixed}$ is high; from then onwards no further incoming pulses are received.

3.3. Peak Detector Analysis

In this section, the basic peak detector is analyzed to predict errors in amplitude detection due to the finite delay of the comparator, logic block and the RC network. For simplicity, the delay of comparator A_1 and the LOGIC 1 block are lumped together in this analysis.

The choice of component values for the low-pass filter used in this topology is important for its correct operation. While the propagation delay of the comparator and LOGIC block from input to switch might be a limiting factor for the voltage error in detecting the peak after it has passed, an early false detection of the peak can happen due to a poor choice of R and C values for the LPF. If the LPF f_{-3dB} frequency is set more than order of magnitude higher than the frequency band of interest, then the phase shift (thus the time delay) on the input signal might be negligible. This translates into a very low voltage difference between the inputs of the comparator, which can set the comparator into a metastability condition, or it could lead it into an erroneous binary decision due its non-zero input-referred offset voltage. Furthermore, an excessive phase shift ($f_{-3dB} \ll f_{in}$) would result in the same effect, because the comparator would trip at the crossing of both inputs, which will happen before the peak of the delayed version of the signal.

The following analysis seeks for insights and trade-offs in the chosen peak detector topology in order estimate what kind of errors are expected (at least) by using some simplifying assumptions.

In order to illustrate the points made in the previous paragraphs, we model the input signal as:

$$V_{in} = A\sin(\omega_0 t)\,u(t) \tag{3.2}$$

where A is the amplitude of the signal and ω_0 the angular frequency given by $2\pi f_0$, f_0 being the frequency to be evaluated.

Given that the input signal expected is a derivative of a Gaussian monocycle with multipath components, and this only happens once every time window of the system, we decided to model the input signal in this section as causal. In this way we capture the settling behavior of the RC network on the first peak detected. Therefore, we use the complete transient plus steady-state response of the network, which is given by the following expression:

$$V_{pk} = |H_{LPF}(\omega_0)|A\sin\left(\omega_0 t + \angle H_{LPF}(\omega_0)\right) + \frac{\omega_{-3dB}\omega_0 A e^{-t\omega_{-3dB}}}{\omega_0^2 + \omega_{-3dB}^2} \tag{3.3}$$

where:

$$|H_{LPF(\omega_0)}| = \frac{1}{\sqrt{1 + (\omega_0/\omega_{-3dB})^2}} \tag{3.4}$$

and

$$\angle H_{LPF}(\omega_0) = -\arctan\left(\omega_0/\omega_{-3dB}\right) \tag{3.5}$$

where $H_{LPF}(\omega)$ represents the low-pass filter network frequency response.

The comparator A_1 effectively senses the voltage difference between V_{in} and V_{pk}, the latter being the phase shifted version of V_{in} due the low-pass filter network.

$$V_{in} - V_{pk} = [A\sin(\omega_0 t)] - \left[|H_{LPF}(\omega_0)|A\sin\left(\omega_0 t + \angle H_{LPF}(\omega_0)\right) + \frac{\omega_{-3dB}\omega_0 A e^{-t\omega_{-3dB}}}{\omega_0^2 + \omega_{-3dB}^2}\right] = 0 \tag{3.6}$$

The solution is defined as $t_{crossing}$. This is the instant where $V_{in} - V_{pk} = 0V$. The solution is function of mainly the input frequency ω_0 and the corner frequency of the low-pass filter f_{-3dB}.

$$t_{crossing} = f(\omega_0, \omega_{-3dB}) + t_{comp,delay}(V_{in,ov}, V_{cm}, SR) \tag{3.7}$$

The term $t_{comp,delay}(V_{in,ov}, V_{cm}, SR)$ is added to represent the propagation delay of comparator and LOGIC block, which is a function of the input overdrive $V_{in,ov}$, the common-mode voltage V_{cm} and the slew rate of the differential input signal SR. Without this term, we are assuming a comparator with $0s$ propagation delay.

This allows us to compare the relative error as a function of f_{-3dB} assuming zero and non-zero propagation delays. Once $t_{crossing}$ is found numerically, we obtain the relative error as follows:

$$Error = 100\% \times \frac{A - A\sin(\omega_0 t_{crossing})}{A} \tag{3.8}$$

With those expression in hand, we can evaluate the percentage error in amplitude detection as a function of the cut-off frequency f_{-3dB} of the low-pass filter network. This simulation is repeated for various values of $t_{comp,delay}$ fixed values in order to see how the delay affects the amplitude detection as well. For Figure the amplitude is chosen as $A = 0.1V$.

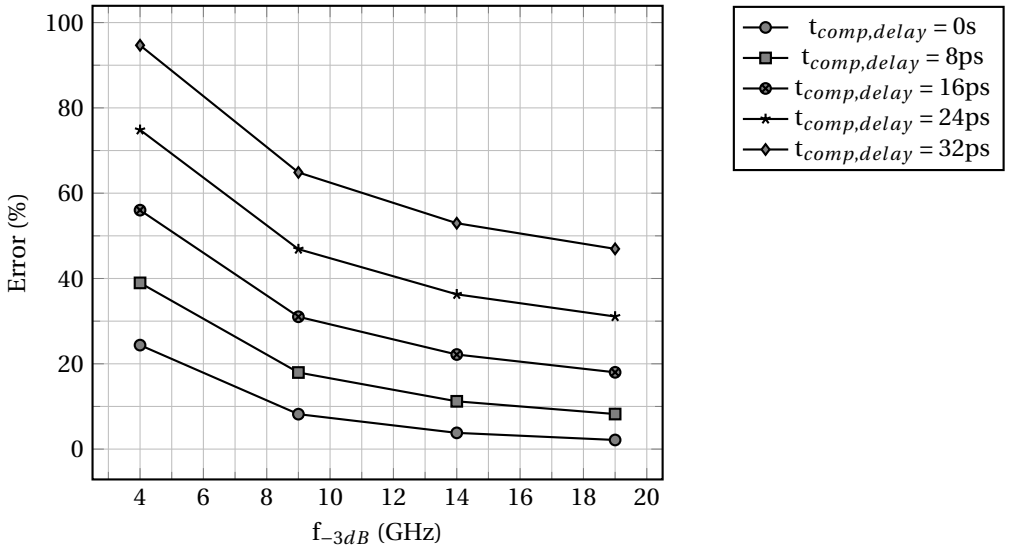


Figure 3.13: Percentage error as a function of f_{-3dB}. Input frequency is $4GHz$

The numerical simulations in Figure 3.13 reveal that if we would like to have a maximum of 40% error in detecting the amplitude, our comparator and LOGIC block must have a propagation delay between $8ps$ and $24ps$. Achieving that delay value is practically impossible to realize in $0.18\mu m$ CMOS technology, which is the process we have at hand. Therefore, in the next chapter, we will focus on designing the system to be process scalable and as fast as the technology allows.

3.4. Conclusion

In this chapter, the concept of peak detection was abstracted away in terms of block diagrams in order to understand the existing topologies in a more systematic way.

The block implementing the Derivative and signum function is found to be more amicable to the requirements of the system because it offers the possibility of separating the amplitude and time detection. This clearly favors TOA estimation since now an error in amplitude detection will not translate into TOA uncertainty.

In addition, the time detection information is given as a digital signal. Therefore, this information, combined with the output of an extra fixed-threshold comparator, can be used by logic blocks in order to implement first peak detection; further incoming peaks will be ignored if a previous peak has surpassed the threshold.

Finally, the peak detector implementation is analyzed in terms of its amplitude detecting capabilities. These simulation show that the system must have a maximum propagation delay of 24ps if we are to keep the maximum error detection below 50%. This result suggest that implementing such a system with a $0.18\mu m$ CMOS technology will be extremely difficult (if not impossible). Therefore, the peak detector system that will be designed in the next chapter will focus on being process scalable and as fast as possible.

4

Peak Detector Circuit Design

In this chapter, circuit design decisions for implementing the different circuit blocks of the peak detector system proposed in Chatper 3.

4.1. Block Circuit Design

The core of system is composed of 2 comparators, basic logic gates, a switch (which could be a pass-transmission gate), and an RC network.

4.1.1. Comparator

To design the comparator, continuous high-speed topologies were researched for. Given that $4GHz$ is at the edge of the technology at hand, it was decided that we would design a comparator as fast as the technology allowed it. However, also a relatively large dynamic range is needed due to low input SNR (which is $10dB$), in order to be able to choose from large range of thresholds.

mV-level offset will be tolerated, but it is aimed to look for the lowest propagation delay possible.

A first design choice made was that, clocked comparators, which are commonly used in ADCs, will be discarded. Even though they have a very fast operation due to its positive feedback, they are designed to produce and saturate onto one binary decision within a clock duty cycle; a subsequent binary decision within that time frame would be highly signal-dependent i.e. a large swing would be needed at the preamplifiers to override the decision stage (usually cross-coupled inverters).

In order to analyze the limitations of differential-pair based comparators in for a high-speed operation, the comparator used in [12], which is a simple differential pair with a PMOS-latch, is discussed.

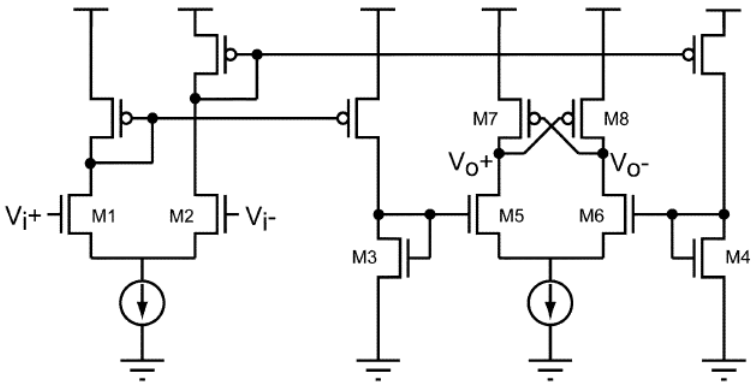


Figure 4.1: A continuous-time comparator used in [12]

For high-frequency operation, the tail bias current has to be relatively large, probably in the order of hundreds of uA to some mA. Unfortunately, this sets further difficulties: there needs to be a bigger W/L ratio for the input pair such they are able to handle such bias current (otherwise there can be safe-operating area concerns).Furthermore, they also require the common-mode level of the comparator to be raised, as such, this decreases the output voltage range of the input pair; the PMOS-mirrors need to be allocated at least $100mV$ or more to be in saturation, and the common-mode voltage could easily be increased up to 1.3 in order to be properly biased at currents higher than $500\mu A$.

An alternative could be to use a class-AB input stage, as they usually have a low-bias quiescent current and can dissipate large amounts. In addition, they offer us the opportunity to save power. In general, they are used to drive large capacitive loads or small resistive ones.

In this design, a self-biased class-AB Voltage-to-Current converter input stage will drive a current-mode comparator. These comparators are designed to have a small input impedance in order to have low nodal time constants and thus have a decent speed improvement over their voltage counterpart [39]. A low nodal time constant means that this node will not have large swings, thus the circuit does not spend time charging parasitic capacitors in order to have a large swing. Current-mode logic takes advantage of this fact in order to achieve higher speeds than their voltage-mode counter parts.

Another way to see this is that the bandwidth of the input stage will be increased for its g_m. This is due to the fact that the input impedance of the current comparator is low in comparison to the output impedance of the input stage. Therefore, the current that Voltage-to-Current is able to provide will mostly flow into the comparator.

Other similar designs using this approach have been published in [29] as an application for novel rail-to-rail transconductor stage and in [1] as part of a high-speed peak detector for a very specific application.

Now, in the following subsections, the design of the V-I converter and current-comparator will be discussed. Several current comparators exist in the literature, therefore, a throughout discussion of the options available and the final choice is made in order to grasp better why the a certain comparator is finally chosen.

High-Speed Current Comparator

A current-comparator is, in essence, a saturating transimpedance amplifier. However, its intention is to create full rail-to-rail signals based on the sign of the input current; whether there is charge flowing in or out of the input node.

The first current comparator ever published in the literature dates back to 1983, when Freitas published a current-mirror-based comparator, as shown in [15], which is based on PMOS and NMOS cascode current mirrors whose outputs are joined. The subtraction of currents happening at the output causes a voltage swing which goes up or down depending on outcome sign. Further inverters are placed in order to realize a rail-to-rail output signal.

Unfortunately, one of the main disadvantages of such comparator is its speed, since at the output node there is a high output impedance. In order to circumvent these limitations, a novel current comparator was published in 1992 by Traff [35], which realizes a clever manipulation of typical back-to-back connected inverters in order to provide nonlinear feedback and low input impedance at its input. The schematic is shown in figure 4.2. Unfortunately, the increase in speed comes with the assumption that the input current is the result of previous current-mode subtraction stage. Nonetheless, the comparator relaxes the requirement for high-output impedance of the previous current mirrors performing the subtraction thanks to its low input impedance.

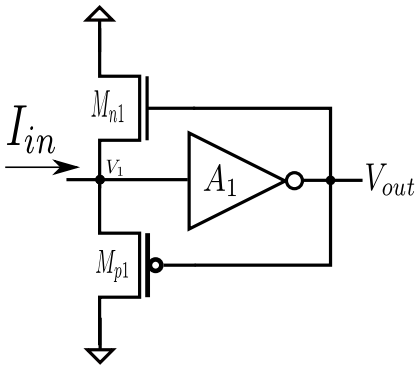


Figure 4.2: Current comparator by Traff [35]

The operation of Traff's current comparator is as follows. Assuming V_{out} is a couple of hundreds of mV away from V_{DD} [1], if there is a positive current I_{in} at the input, this produces a positive voltage swing at the input node. If the input current is big enough, then the voltage swing at V_1 will be enough to reduce the gate-to-source voltage of transistor M_{n1}, which is given by $V_{out} - V_1$, thus reducing the overdrive voltage and driving M_{n1} into deep subthreshold or switching it off. However, at the same time, the positive swing in V_1 increases the source-to-gate voltage of M_{p1}, which is given by $V_1 - V_{out}$, thus increasing its overdrive voltage (refer to figure 4.3) . In addition, V_1 drives inverter A_1 slightly down, thus reducing V_{out}, which further increases M_{p1} overdrive voltage. This causes M_{p1} to sink more current, thus driving V_1 down by means of negative feedback.

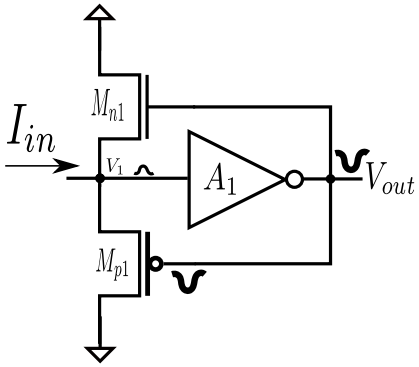


Figure 4.3: Traff's comparator - working rinciple

In other words, the comparator counteracts swings at its input by suppressing them with its loop gain. If there are small swings at the input, this means that the input impedance is small in comparison with the preceding stage output impedance.

One of the main disadvantages of Traff's comparator is the significant body effect that transistors M_{n1} and M_{p2} suffer from. This translates into poor resolution of incoming current signals with small amplitude. Several approaches to solve this problem have been presented in [33], [28], [27] and more recently in [3]. In [33], 4 current sources and a pair of diode connected transistors extra are used in order to reduce the deadband of the input transistor due to body effect. On the other hand, in [28], diode connected transistors are used in order to provide a higher gate voltage and lower voltage to the NMOS and PMOS transistors, respectively, which is not suitable for more advanced low-voltage process nodes. In [27], a resistive feedback common-source amplifier is used at the input so as to decrease its input impedance. While resistive feedback increases the voltage bandwidth of said amplifier by trading it for some gain, the amplifier needs an external biasing for its PMOS load, thus increasing current consumption and circuit complexity. Finally, in [3], a rather low-power comparator is proposed, however, the speed capability is decreased due to the rail-to-rail operation of the input stage of the comparator. In other words, only slower current signals or fast signals with a bigger

[1] This architecture is also notorious for not providing a rail-to-rail output

amplitude are needed in order to ensure high-speed operation.

However, a simple improvement on Traff's comparator is presented in [34]. The comparator simply uses extra inverters in the feedback path so as to amplify the loop gain, thus providing a faster response time and a low input impedance[34].

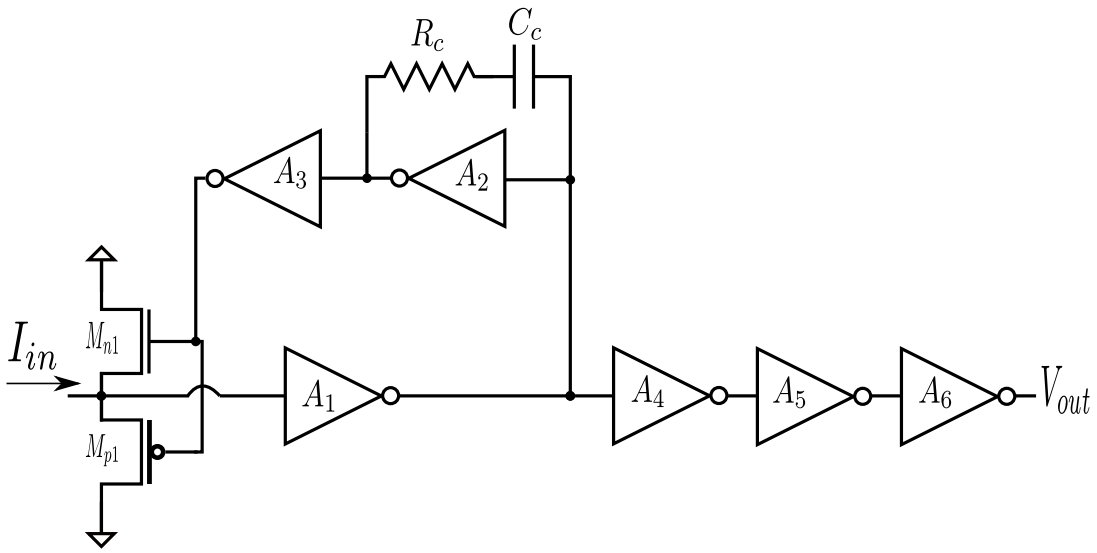


Figure 4.4: High-Speed Current Comparator according to Tang [34]

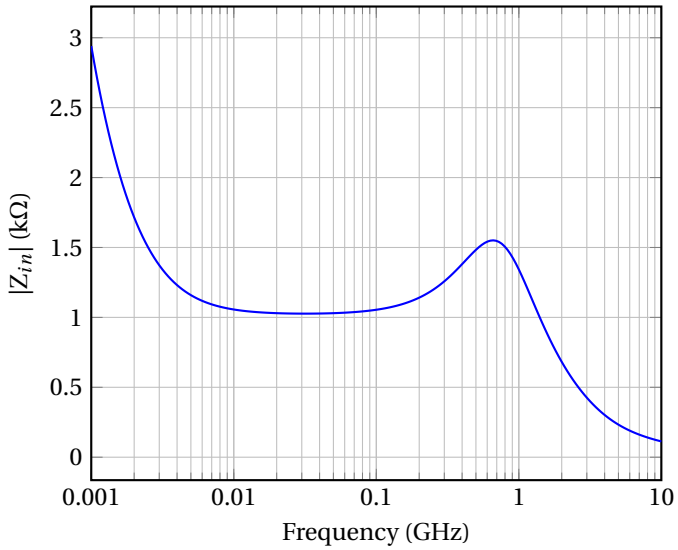


Figure 4.5: Current Comparator Input Impedance Magnitude. Input DC voltage = 867mV

A feedback RC circuit is placed in inverter A_2 in order to do frequency compensation, as the comparator can be highly unstable.

In order to estimate how stable the comparator can be, a loop gain stability test is performed by placing an *iprobe* after A_1 and before the loop happens in figure 4.4.

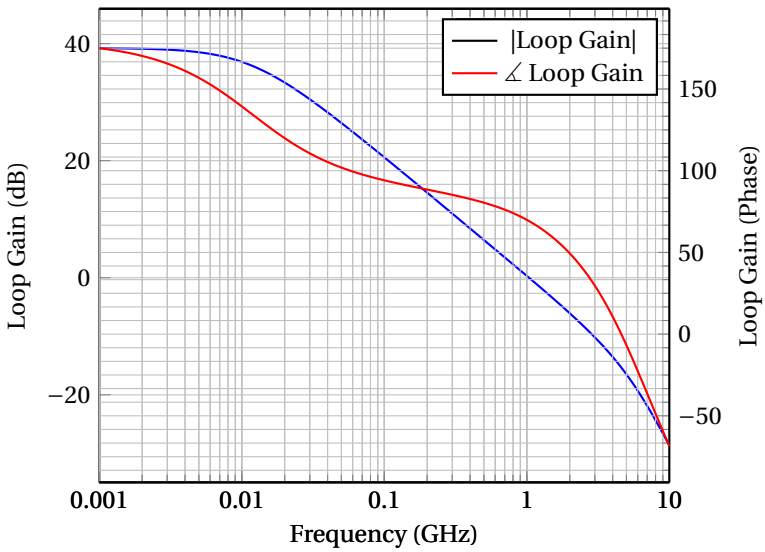


Figure 4.6: Stability

It can be seen that the phase margin is larger than 60 degrees, thus, the design is stable. Obviously, the design is tested in transient simulations together with the whole system, no oscillations were observed.

The comparator is sized with large W/L ratios in order to enhance the low-input impedance operation and high-speed. R_c is designed to be 500 and $C_c = 600fF$

V-I converter

The Voltage-to-Current (V-I) converter or (as the input amplifier will be called from now on) is shown in 4.7. The left input is used as the signal input, while the other input is used as the threshold. The output is taken as a current.

The self-biasing feature offered by this topology translates into 2 important features, namely, decoupling of slew-rate from the bias current and less sensitivity to process variations. The bias voltages of transistors M_p and M_n are stabilized by node V_{bias}. This causes both transistors to operate in the linear region, resulting in the capability of providing higher switching currents than that of the bias current set by V_{bias}.

Its operation may be understood as follows. If a positive voltage swing appears at V_{in}, then V_{bias} does a negative excursion, proportional to V_{in} by approx. $-(g_{m1}+g_{m2})/(g_{ds1}+g_{ds2})$. Then, M_p is driven deeper into the linear region, thus increasing its own output conductance and decreasing its own drain-to-source voltage. This decrease, finally, translates into an increase in V_{sg} for M_3, thus providing a positive current at the output node. A similar reasoning could be applied for a negative input swing at V_{in}.

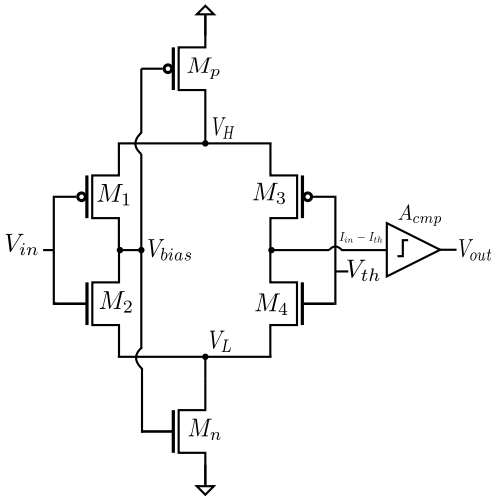


Figure 4.7: Comparator circuit showing V-I [5][4] and current-mode comparator

In order to provide a current signal, the condition $Z_{in,comp} \ll Z_{out,V-I}$ must be fulfilled, where $Z_{in,comp}$ is the input impedance of the comparator while $Z_{out,V-I}$ is the output impedance of the V-I converter. It is important to point out, as stated in [4], that the amplifier above is able to provide output currents that are much greater than its quiescent current, which suggests that the output impedance of the V-I converter could be comparable to the input impedance of the current comparator A_{cmp}. Therefore, the V-I is sized small enough such that when a signal appears at the input, V_{bias} does not have great swings that could make the output impedance of the inverter (M_3 and M_4) to be reduced.

The magnitude and phase of the small signal transconductance transfer function of the V-I converter can be seen in Figures 4.8 and 4.9, respectively. The transconductance is measured while the V-I converter is connected to the current-comparator.

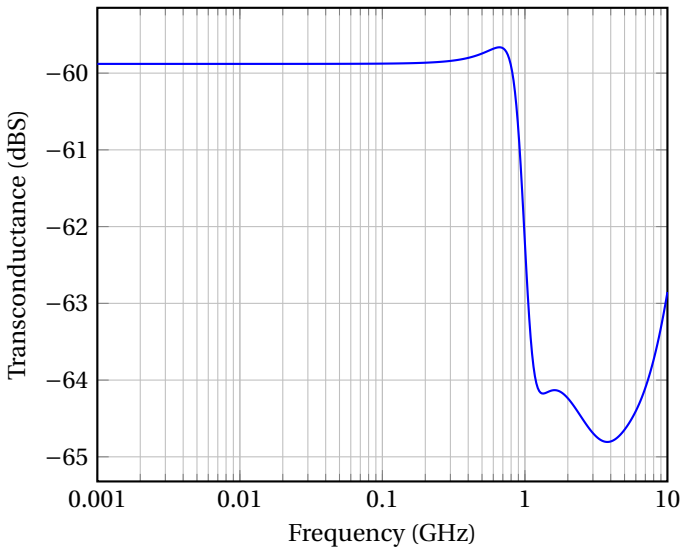


Figure 4.8: Magnitude of the Transconductance transfer function of the self-biased amplifier. $V_i = V_th = 900mV$

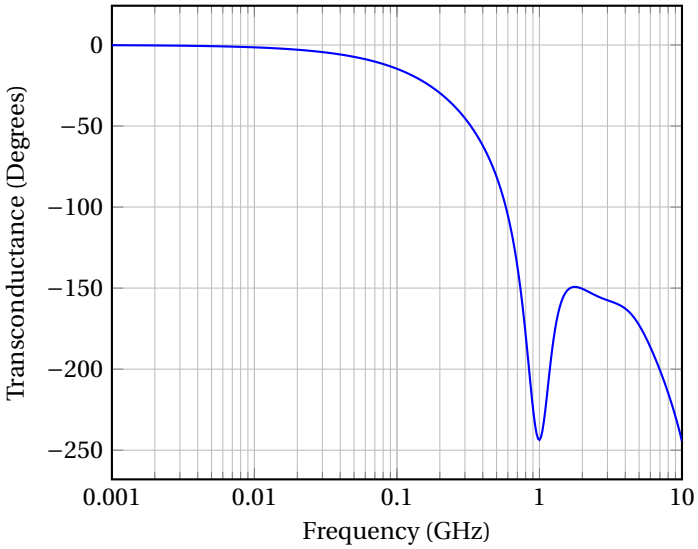


Figure 4.9: Phase of the Transconductance transfer function of the self-biased amplifier

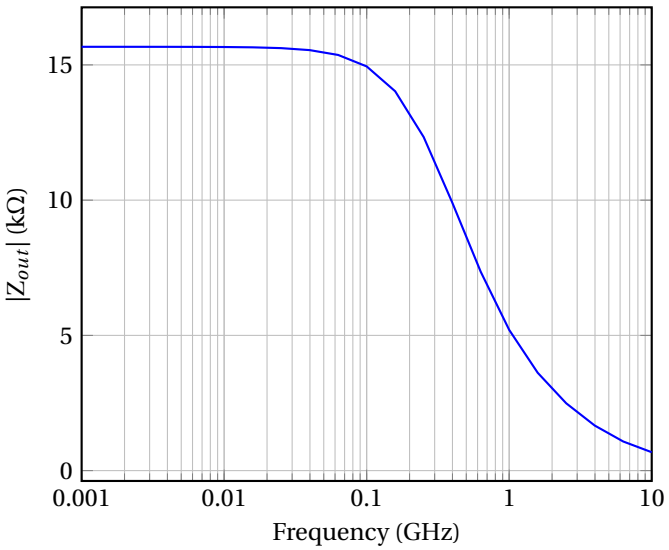


Figure 4.10: Output Impedance Magnitude

The magnitude response shown in Figure 4.8 shows that the V-I converter is able to provide about higher $-60dB$ of gm (AC voltage amplitude is 1), which is approximately $1mS$ of transconductance at low frequencies ($1MHz - 100MHz$). An small roll-off at around $800MHz$, which is due to the output capacitance of the V-I converter becoming small impedances at such frequencies, thus shorting the current through M_4 and M_n. However, a small peaking is seen before this roll-off occurs, which is due to a small resonance-mode of the input impedance of the subsequent current comparator (see Figure 4.5). There are parasitic capacitors in series with the input node of the comparator are significant at hight frequencies, since they are gate-to-source capacitors.

The sudden roll-up of the response at $4GHz$ is due to the ideal source the stage was driven with; once capacitors $C_{gd,1,2}$ give in, the entire AC current flows through $C_{ds,1}$ and $C_{ds,2}$, then a current division happens at node V_B between $C_{ds,n}$ and $C_{ds,4}$ and $C_{gs,4}$ (same reasoning can be done for node V_L), which ends up flowing into the current comparator at the output node of inverter $M_3 - M_4$.

In Figure 4.9, a 0° phase shift is seen at low frequencies as expected. It can be seen that past $1GHz$, the phase reverses back to -150°, however, this happens when the signal is completely attenuated due its high

frequency content.

In Figure 4.10, the small signal output impedance of the V-I converter is shown as a function of frequency[2]. It can been seen that the output impedance is greater than $5k\Omega$ up to 1 GHz. The roll-off is due to the parasitic output capacitance of the inverter formed by M_3 and M_4 formed by the drain-to-source capacitance (C_{ds}) and the gate-to-drain (C_{gd}).

Logic Blocks

The logic blocks in this system are essentially event-driven, which makes it more difficult to synthesize by hand compared to clock-driven circuits.

The logic blocks are shown in Figure 4.11. LOGIC 1 performs the first amplitude peak detection, while LOGIC 2 does the time detection.

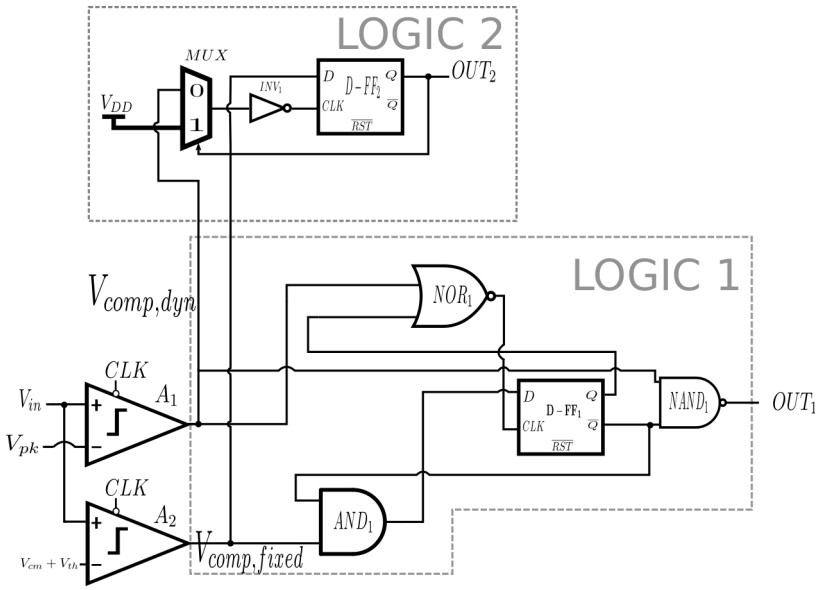


Figure 4.11: LOGIC 1 ad 2 blocks

Table 4.1: Truth table of LOGIC 1

$V_{comp,dyn}$	$V_{comp,fixed}$	CLK	Q_t	Q_{t+1}	$\overline{Q_t}$	$\overline{Q_{t+1}}$	OUT_1
0	0	1	0	0	1	1	1
1	0	0	0	0	1	1	0
1	1	0	0	0	1	1	0
0	1	1	0	1	1	0	1
0	0	0	1	1	0	1	1
1	0	0	1	1	0	1	1
1	1	0	1	1	0	1	1
0	1	0	1	1	0	1	1

[2]This was measured using an DC source connected at the output providing a DC voltage of $867mV$, which is the quiescent DC level appearing in the transien simulations

Table 4.2: Truth table of LOGIC 2

$V_{comp,dyn}$	$V_{comp,fixed}$	CLK	$Q_t = OUT_2$	$Q_{t+1} = OUT_2$
0	0	1	0	0
1	0	0	0	0
1	1	0	0	0
0	1	1	0	1
0	0	0	1	1
1	0	0	1	1
1	1	0	1	1
0	1	0	1	1

In short, the functionality of these logic block is based on a single state, which changes once a peak has been detected. After this change in state, the output of both logic blocks cannot change until they are reset by an external clock.

LOGIC 2 block is the simplest to understand. Basically, the output comparator A_1, $V_{comp,dyn}$, is used as a clock. If $V_{comp,fixed}$ is high (i.e. the input signal is bigger than V_{th}), and during this time $V_{comp,dyn}$ makes a transition from high to low (i.e. a peak has been sampled), then this negative transition is converted into a positive by INV_1, thus effectively setting Q (or OUT_2) equal to 1 (keeping in mind that D is $V_{comp,fixed}$, which we initially said is at 1), which changes the control bit at the MUX, thus setting its output to 1, which is a 0 at the CLK port of $D-FF_2$. After this has happened, no further incoming pulses will seen at OUT_2 until $D-FF_2$ is reset.

The inputs and states reflecting the transition from a waveform being tracked by A_1, surpassing V_{th} in A_2 and finally having A_1 switching off are shown in starting from row 2 to 4 in table 4.2.

An issue that could arise from the truth table is in the case when $V_{comp,fixed}$=1 while $V_{comp,dyn}$ is 0 even before $V_{comp,fixed}$ became 1. A simplifying assumption used in this logic blocks is that the threshold V_{th} for comparator A_2 is assumed to be much larger than the noise floor, since for A_1 the noise floor is its threshold when there is no signal. If V_{th} is set in this way, then there is very little probability that this state case is due to $V_{comp,dyn}$ not turning before $V_{comp,fixed}$.

LOGIC 1 block also follows a similar operating principle. There can only be a change of state when A_1 makes a transition from high to low while A_2 is high.

The same issue that can happen with LOGIC 2 can also occur in this logic block. However, if the threshold is set correctly as explained above, then this issue can be avoided.

Besides the ambiguous state issue already mentioned, another problem can happen with the timing; the setup-time t_{su} of both flip-flops in LOGIC 1 and LOGIC 2 has to be smaller than the time in which between A_1 and A_2 switch on. Therefore, this imposes a minimum limit on threshold V_{th} that can be chosen. For instance, if it is set way to close to the noise floor, there might be a possibility for A_2 to trigger at the same time as the A_1. From simulations it was found that $20mV$ is a good minimum limit in order to ensure proper operation of the logic blocks.

4.1.2. Switches

Switches S_1 and S_2 must be implemented in a T-switch configuration. If they are implemented as pass transistors, there is a significant cross-talk from $V_{in+,-}$ to $V_{pk+,-}$ when S_1 and S_2 are opened. In this implementation, the T-switches used offered higher than $50dB$ isolation from input to output. A drawback of using a T-switch in this system is the reduction in frequency operation; LOGIC 1 block has to drive a higher load, therefore, the delay propagation delay is increased.

4.2. Differential Architecture

It is advantageous to use a differential implementation because the it allows to increase the dynamic range and can somewhat palliate errors in sampling.

A simple schematic showing the differential sampling principle appears in figure 4.12.

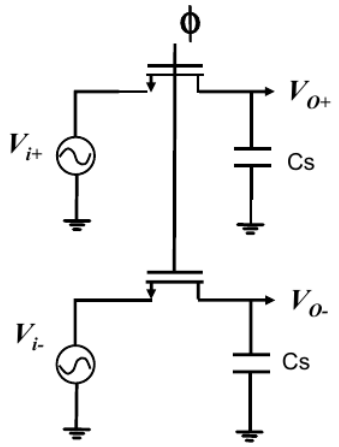


Figure 4.12: Differential Sampling Principle

If assume that the output differential voltage is $V_{od} = V_{o+} - V_{o-}$ and the input differential voltage is $V_{id} = V_{i+} - V_{i-}$, where $V_{o+} = V_{i+}(1+\epsilon_1)$ and $V_{o-} = V_{i-}(1+\epsilon_1)$ where ϵ is a gain error from input to output, then the differential output voltage is given by:

$$V_{od} = V_{id} + V_{id}\frac{(\epsilon_1+\epsilon_2)}{2} + (\epsilon_1-\epsilon_2)V_{ic} \tag{4.1}$$

where $V_{ic} = (V_{i+} + V_{i-})/2$. From the expression above, it can be noticed that the addition of the errors are averaged out and subtract from each other, which means that there is an small reduction if the error terms ϵ have the same sign. Furthermore, it offers immunity to common-mode noise, and last but least, it extends the dynamic range of the peak detector, because the output amplitude, i.e., the peak detected, is almost doubled, so it is less likely that such detected peak would be hidden by the noise of the system.

For those reasons, a differential implementation of the peak detector is used. The complete system is shown in figure 4.13.

The clock delay-line in figure 4.13 is used to give time to the comparators to settle to their nominal DC levels before enabling the D Flip-Flop. When the clock turns off, comparators A_1 and A_2 outputs remain at ground, which means that S_1 and S_2 are open. Then, CLK_{delay} signal shorts S_3 and S_4 to a predefined common-mode voltage. The delay line is implemented as a chain of inverters, where inverter A_2 is made current-starved in order to control the delay of the clock signal when activating the D flip-flop to start peak detection operation.

In the comparator block, switches have been implemented so that the DC levels within the comparator are well defined when $CLK = 0$, with the added advantage of power savings as well. For the case of the V-I converter, the switches $M_{p,sw1}$ and $M_{n,sw1}$ are left open. In the current comparator the same strategy is applied with $M_{n,sw}$ and $M_{p,sw}$, such that node V_A can be easily shorted to V_{DD} by means of $M_{p,sw2}$, making $V_{out} = 0$ for $CLK = 0$. The implementation is show in figure 4.14.

Regarding the differential output buffer B_1 and LNA, please refer to section 6.3, as it is out of the scope of this work.

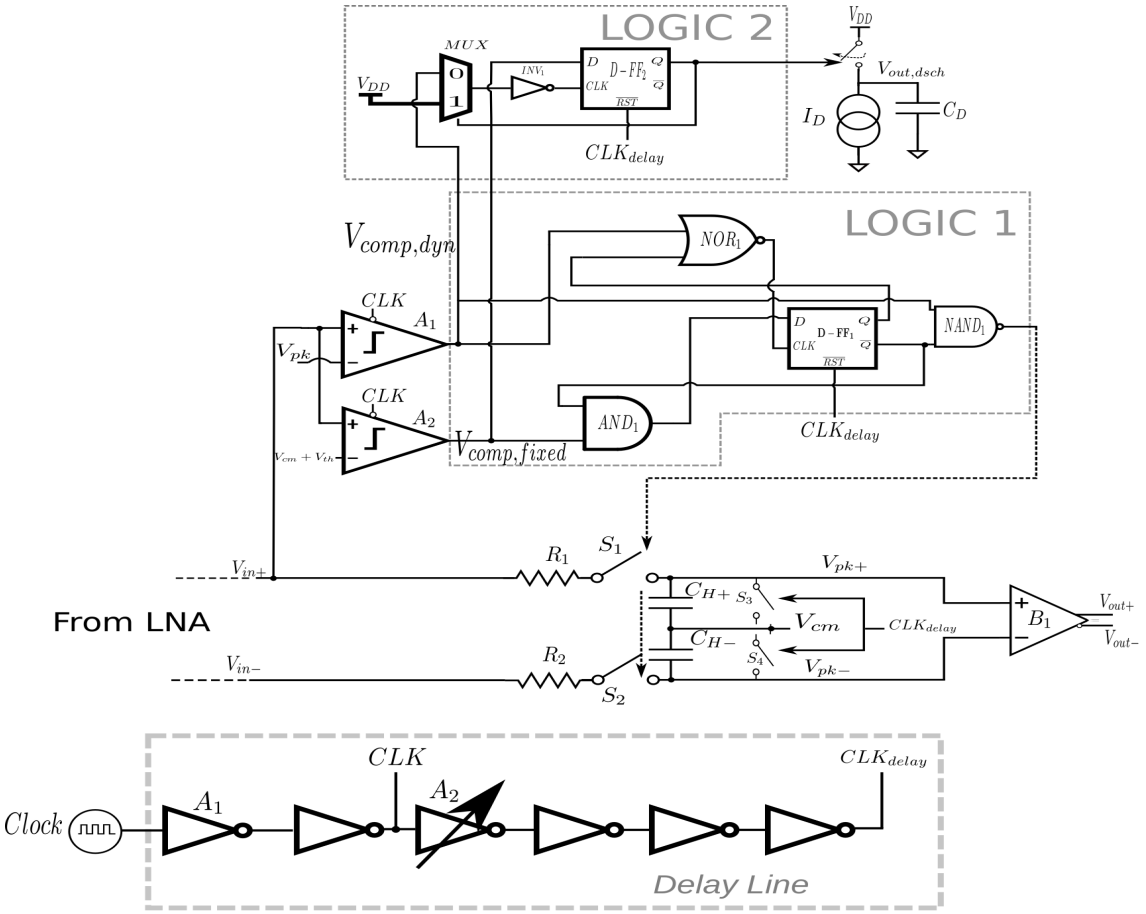


Figure 4.13: Complete differential first-path peak detector system

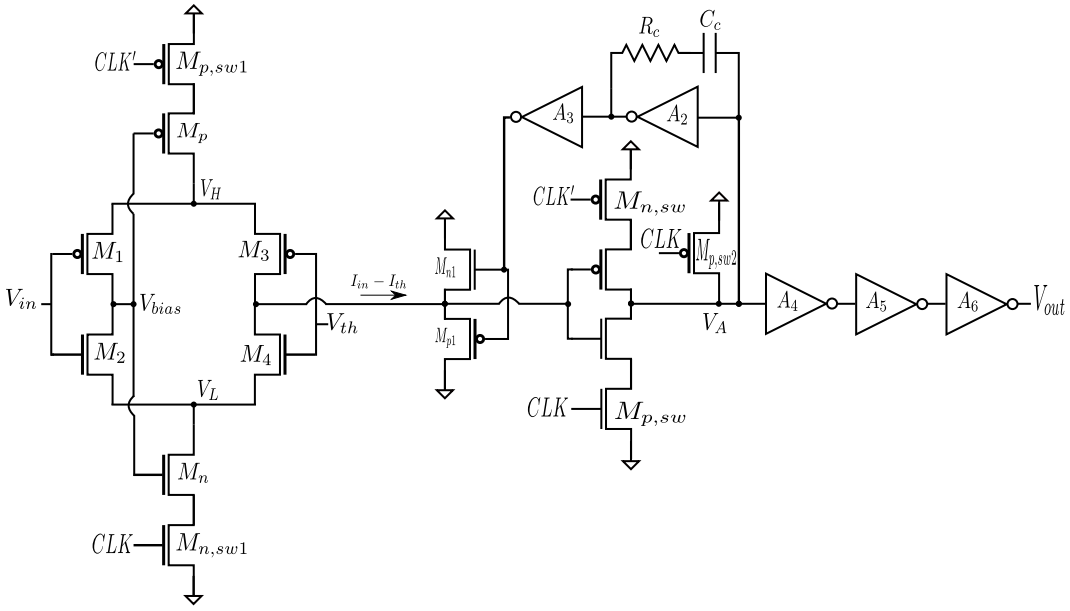


Figure 4.14: Switched implementation of the comparator

In order to drive this system, there some considerations to be made at the LNA stage. It is preferable that the LNA generates its own well-defined common-mode voltage (like some feedback LNA topologies do) in order

to avoid rebiasing by means of a high-pass filter. If this is done, then V_{cm} could be set to zero.

The RC network is designed such that f_{-3dB} at around $4.5GHz$. The fixed resistance is 200Ω and the transmission gates equivalent resistance in parallel is about 150Ω, so in total 300Ω .

4.2.1. Example Waveforms

The following two figures show the most important transient waveforms of the receiver above.

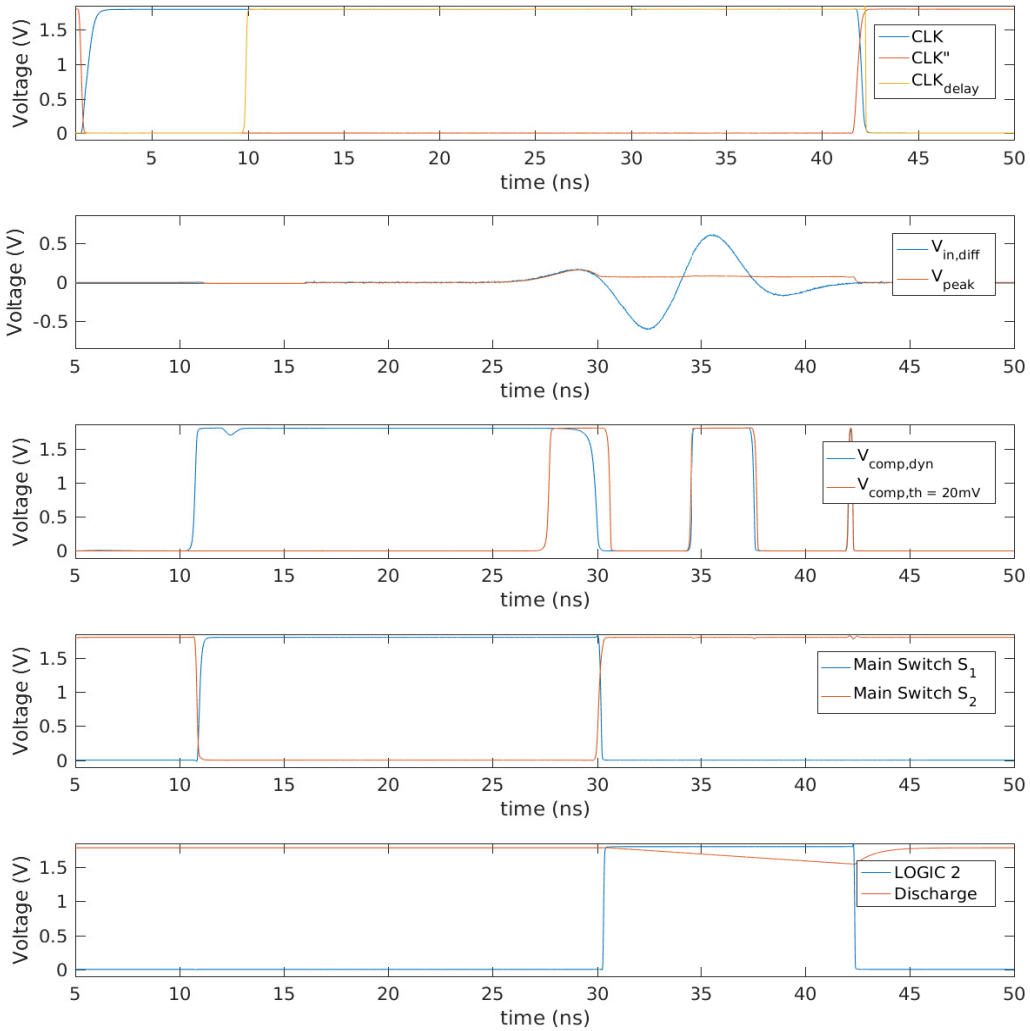


Figure 4.15: Peak Detector System waveforms - Threshold = 20mV

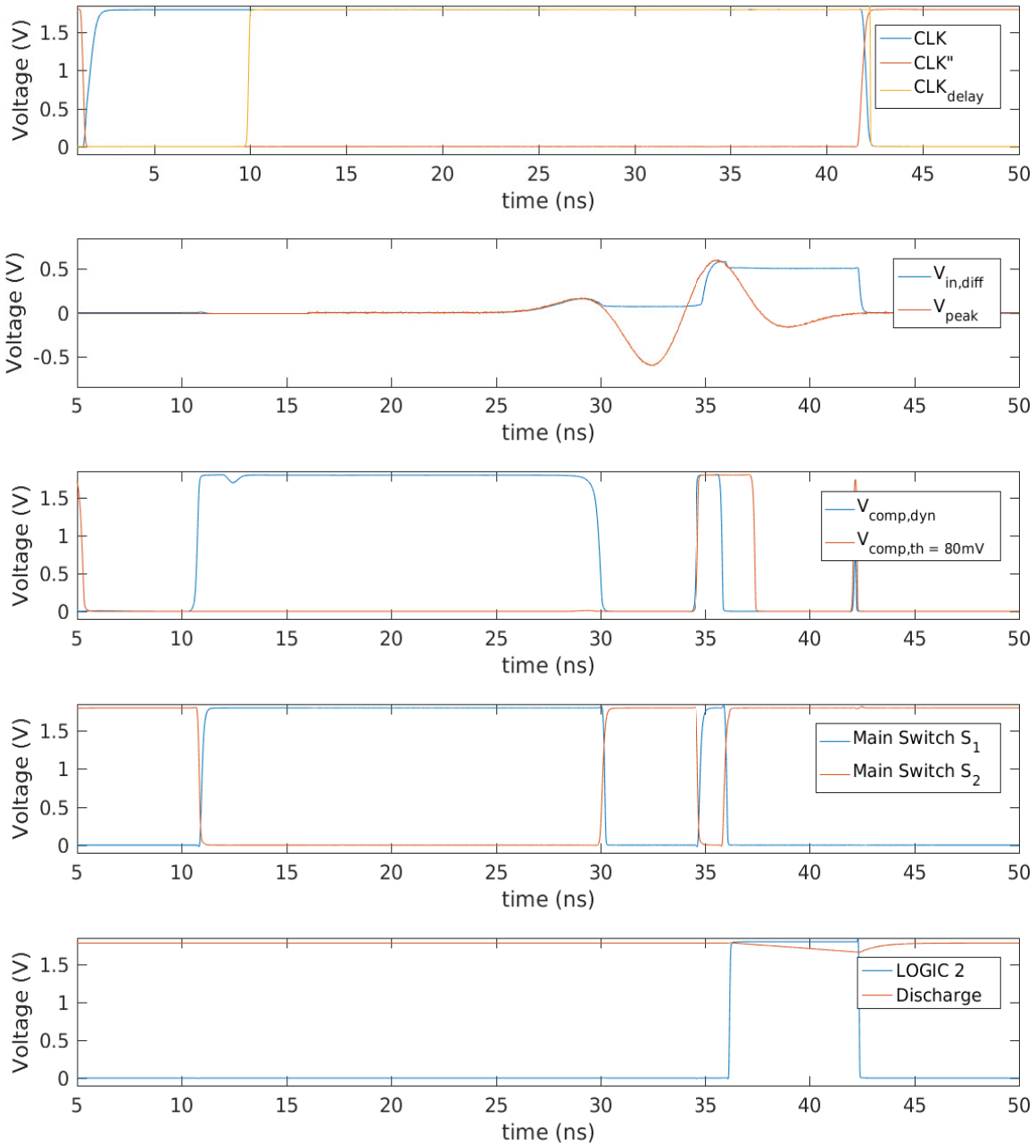


Figure 4.16: Peak Detector System waveforsm - Threshold = 80mV

In both figures 4.15 and 4.16, the waveforms from top to bottom belong to clock signal CLK, its negated version (and its delayed version CLK_{delay}), input (3_{rd} derivative of Gaussian pulse) and output, comparator outputs, main switches (S_1 and S_2 in Figure 4.13) and the output of LOGIC 2 block with the linear discharge.

The simulations are obtained using two 50Ω sources providing a differential signal. The threshold voltage V_{th} is $20mV$ above the common-mode voltage $V_{cm} = 700mV$ for Figure 4.15 and $80mV$ for Figure 4.16 in this

simulation. The threshold only works on one of the complementary input signals, therefore it does not need to be large.

For the smaller threshold, the first peak in Figure 4.15 surpasses it, which means that the peak detector holds it for the remaining of the clock period while ignoring the larger subsequent peak. In the third plot from the top, it can be seen that there are some spurious switching of the comparators before $5ns$, which is due to the settling of the initial voltages. For this reason, a delay is imposed on the D flip-flop to invalidate such signals. It can be seen that once at the D flip-flop is enabled at around $10ns$ in the top most plot, the dynamic comparator starts tracking the signal (its output $V_{comp,dyn}$ is 1), as shown in the third plot.

For the larger threshold (in Figure 4.16), we can see that the system operates as a normal peak detector, holding onto the larger peak until the end of the clock period.

In both figures the output of the LOGIC 2 and the discharge is shown in the bottom-most plot for both Figures.

4.2.2. Peak detection error

As every peak detector, the amplitude detection usually has an error that monotonically increases as the input frequency increases. The peak detector has less time to trigger on the peak as the signal period decreases.

The amplitude error as a function of frequency and amplitude is shown in figure 4.17.

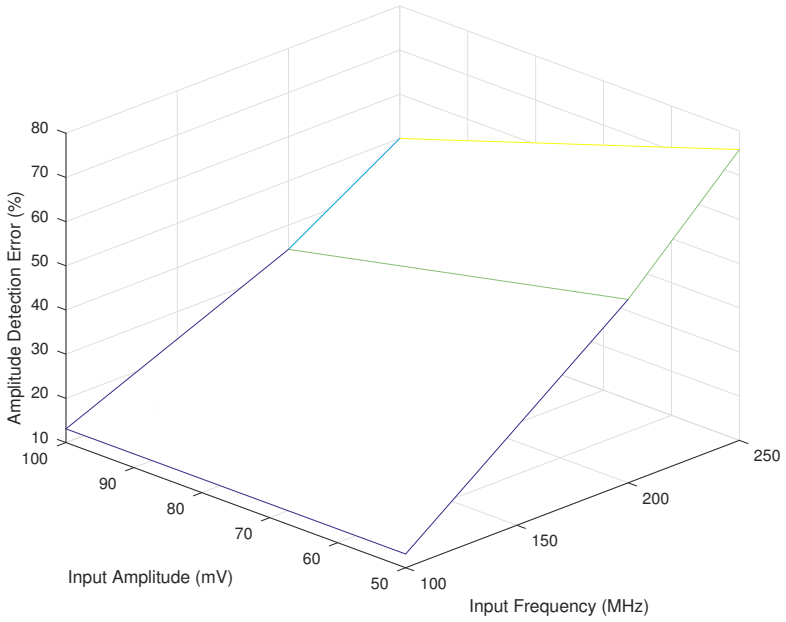


Figure 4.17: Percentage error in amplitude detection as a function of input amplitude and frequency

From Figure 4.17, it can be seen that at $100MHz$, increasing the amplitude does not improve the error. This means that this error is dominated by charge injection from the T-switches. However, as we increase the frequency, it can be seen that the error starts increasing considerably. Increasing the input amplitude reduces the error, but only for a very small percentage. Therefore, at those high frequencies, the error is mainly dominated by

4.2.3. Delay dispersion

Comparators always react faster when they are hit with a bigger voltage or a high slew-rate. In Figure 4.18, the propagation delay is shown as a function of input voltage amplitude and input frequency.

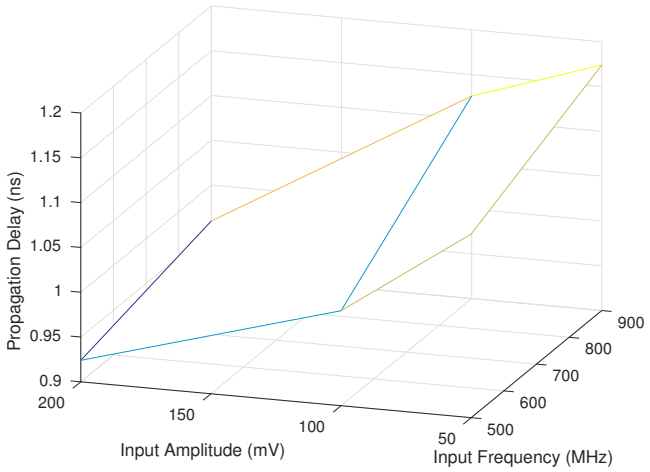


Figure 4.18: Propagation delay in amplitude detection as a function of input amplitude and frequency

As expected, it can be seen that the smallest delays are found when the input amplitude is $200mV$.

Increasing the frequency makes an slight increase in the delay as well. This is due to the fact that parasitic capacitors to ground have less impedance in comparison to lower frequencies, therefore they will attenuate the voltage at their nodes.

It was found that the delay dispersion within the frequency range of $500MHz - 900MHz$ is $214ps$, which corresponds to ranging error of $6.42cm$.

4.3. Final Specifications Summary

Characteristic	Value
Maximum Frequency of Operation (Amplitude Detection)	250MHz (50% Amplitude error)
Maximum Frequency of Operation (Time Detection)	$900MHz$
Minimum Input Voltage	35mV (at 150MHz)
Maximum delay dispersion	214ps (from 500MHz to 900MHz)
Current Dissipation (PD only)	8mA (On) | $< 1\mu A$ (Off)
Current Dissipation (Th. Detector only)	3.9mA (On) | $< 1\mu A$ (Off)
Current Dissipation (System (incl. delay line))	12.3mA (On) | $\approx 400\mu A$ (Off)

Table 4.3: Receiver specifications

Unfortunately, due to process-related limitations, the maximum frequency of operation achieved was $250MHz$. The maximum required was $5GHz$, which means that the maximum frequency has been reduced by a factor of 20.

4.4. Conclusion

In this chapter, a first peak detector that decouples amplitude detection from time detection is designed with a $0.18\mu m$ CMOS technology.

The system is composed of two comparators: one that monitors whether the input signal has surpassed a predefined threshold and another that tracks changes on the input signal. These comparators trigger two logic blocks which perform amplitude and time detection.

The comparator topologies designed are fully self-biased and inverter-based, which favors makes the design process scalable.

LOGIC 1 effectively isolates input from output once a pulse has surpassed the threshold. Therefore, can be effectively held for a large period of time that is suitable for being sampled by an slow ADC.

LOGIC 2 performs time detection and activates a current source that will decay a precharged capacitor in a linear fashion.

Simulations show that a nominal propagation delay (from input to the output of LOGIC 1 and 2) of $1ns$ is achieved. This delay causes the system to have their amplitude and time detection part work at two different frequency ranges. Naturally, the frequency of operation will be larger for the time detection as it suffices that it reacts to an input signal, not mattering how much delay there is. On the other hand, the amplitude detection is limited by the delay of the tracking comparator.

5

Threshold Detector Design

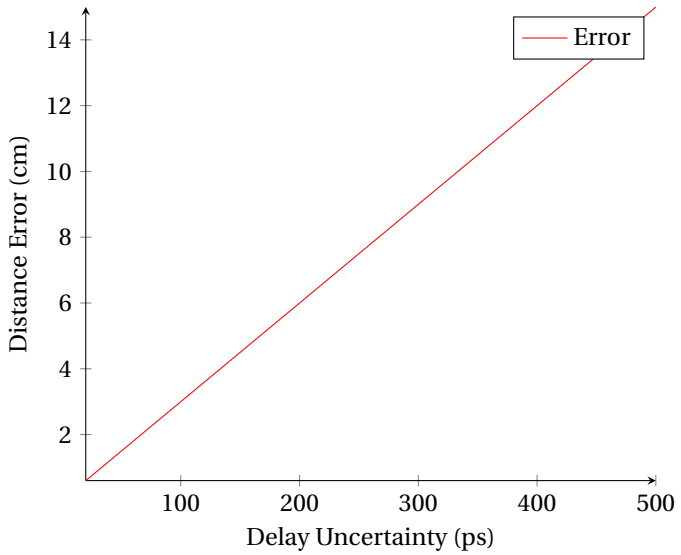
This chapter deals with the design of a simple threshold detector as stated in Chapter 1.6.

In order to suppress multipath components at the receiver end, several low-complexity UWB receivers use a threshold detector assuming that the leading edge of the incoming pulse is higher than a certain threshold, which is also set such that it is above the noise floor of the system.

One crucial design aspect of this threshold detector system is the fact that it must have as low uncertainty in its propagation delay. If the delay is known accurately to a ps level, then it can be calibrated for when solving for the RC time constant which was discussed in the 2. A large delay uncertainty directly translates into a ranging error from the system.

A simple to way to estimate the error distance is given by:

$$D_{cm} = Delay_{error} \times c \tag{5.1}$$



The following section will describe the block diagram of the system. The comparator used in this design is the same the one used in Chapter 4.

5.1. Circuit Block Diagram

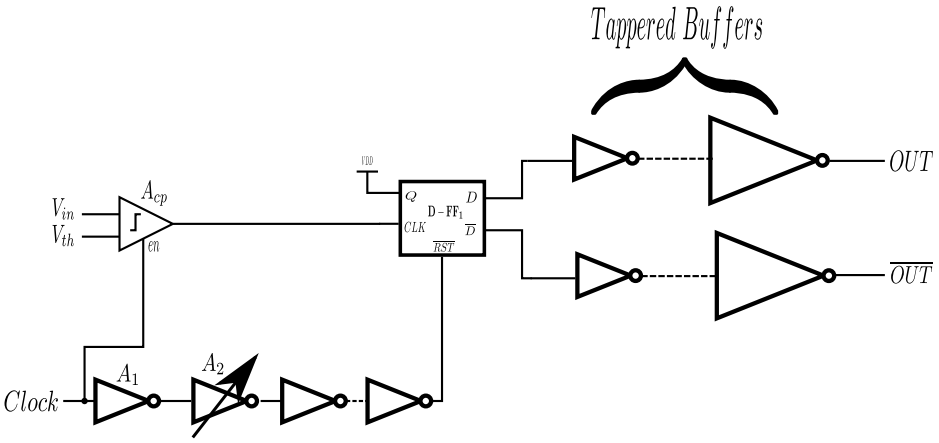


Figure 5.1: Simplified Threshold Detector System

The circuit block diagram in figure 5.1 is composed of a comparator A_{cp}, a D flip-flop, output drives, and extra drivers for the input clock which controls the reset port of the D flip-flop.

The comparator A_{cp} is the same as that of the peak detector designed in the previous section. The D flip-flop is chosen from the standard library of logic gates provided by the technology library. The output buffers are increased in size by a factor of 2 in each stage in order to be able to drive the $2.5pF$ from the specification.

The buffers and the current-starved inverter in the clock path are used in order to delay the signal resetting the D flip flop. This is done since, it was noticed that an spurious switching could occur when enabling the comparator in a new clock cycle. Therefore, the delay path is placed in order to have the D flip-flop ignore such a input if it occurs. However, such behavior was only noticed in one corner. Therefore, it is highly unlikely to happen.

5.1.1. Circuit Design Considerations

The threshold detector designed for this particular application is shown in its essence in figure 5.1. The use of the topologies were justified in the design of the comparator chapter 4.

One of the main contributors to the propagation delay uncertainty in any comparator is the shape of the input signal. This effect is called delay dispersion, and it is a function a of the amplitude, slew rate and input common-mode voltage of the comparator. A simple illustration is shown in figure 5.2.

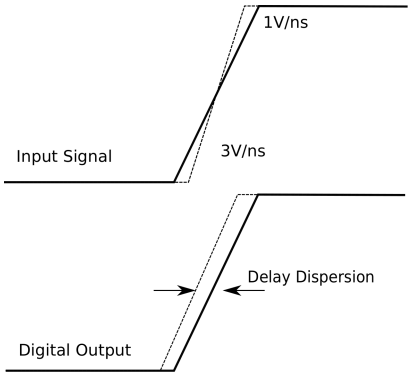


Figure 5.2: Delay dispersion due to a changing input slew rate

In order to minimize the delay uncertainty of the comparator, the current-mode comparator stage used in chapter 4 provides less variation in the propagation delay as a function of the current input amplitude than

other current comparators considered. This is due to the fact that it has an increased loop gain.

5.1.2. Threshold Detector Performance

In this section, the threshold detector's performance is tested with respect to propagation delay, delay dispersion and input offset voltage. Corner analyses and Monte Carlo simulations are provided in order to show the system's robustness to process variations.

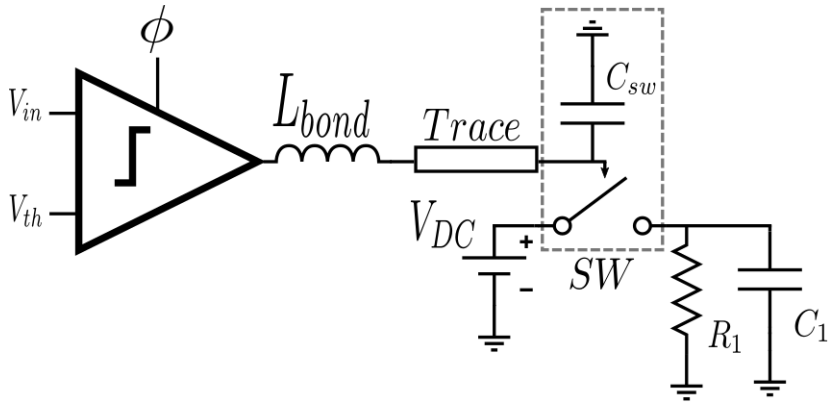


Figure 5.3: Threshold Detector Testbench

For the performance simulations done in Cadence, a testbench was setup. The output of the threshold detector is driving an $1nH$ inductor, modeling a bondwire, a PCB trace, with the following properties:

Table 5.1: Testbench Characteristics

Characteristic	Value
C_{sw}	$2.5pF$
L_{bon}	$1nH$
Trace - ε_r	4.2
Trace - Length	$4mm$
Trace - Dielectric Layer Thickness	$3.55\mu m$
Trace - Signal Line Width	$25\mu m$
Trace - Signal line Conductivity	$5.7e7\ s/m$

Input Offset Voltage

The offset voltage statistics were obtained by means of a Monte Carlo simulation using two DC sources swept in opposite directions. Both V-I converter and the current comparator were included in the test.

Table 5.2: Input Offset Testbench Setup

Characteristic	Value
V_{id}	$[-50mV, 50mV]$
Voltage step	$1mV$
Common-mode input voltage	$900mV$
# Runs	200

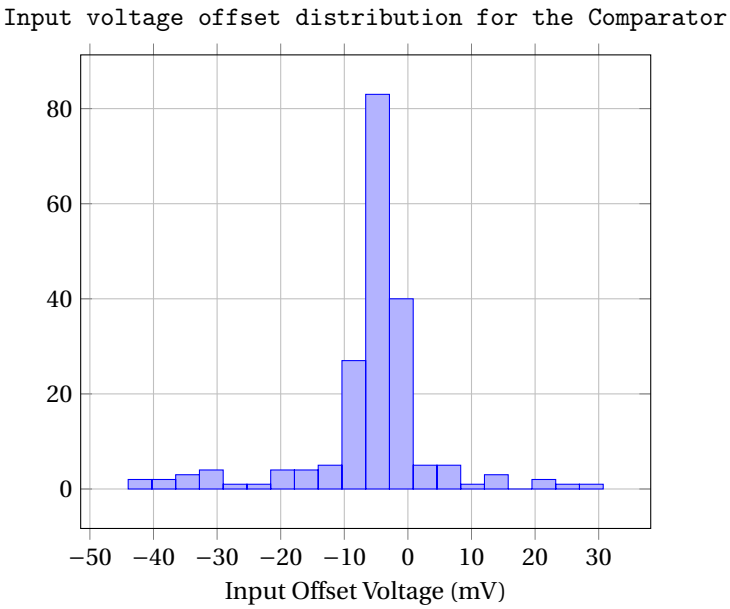


Figure 5.4: Input offset voltage histogram (V-I + Comparator). 200 Monte Carlo runs. $\mu = 5.835mV$, $\sigma = 9.94mV$

It can be seen that, despite not using any sort of offset-compensation scheme, the offset of the comparator has a relatively low standard deviation. This is due to negative feedback action of the input stage. If process variations cause a shift upwards in V_{bias}, such shift decreases the overdrive voltage of M_p, then this causes its V_H to shift downwards. At the same time, V_L shifts downwards due to the increase overdrive voltage of M_n. In this way, $V_H - V_L$ is intended to be kept almost the same, thus $V_{DS,1}$ and $V_{DS,2}$ are also similarly virtually unaffected.

In order to see how robust the V-I converter is, we can see what would be the input voltage offset of the comparator be if only the offset due to the V-I converter were considered[1]. The offset distribution is shown in figure 5.5.

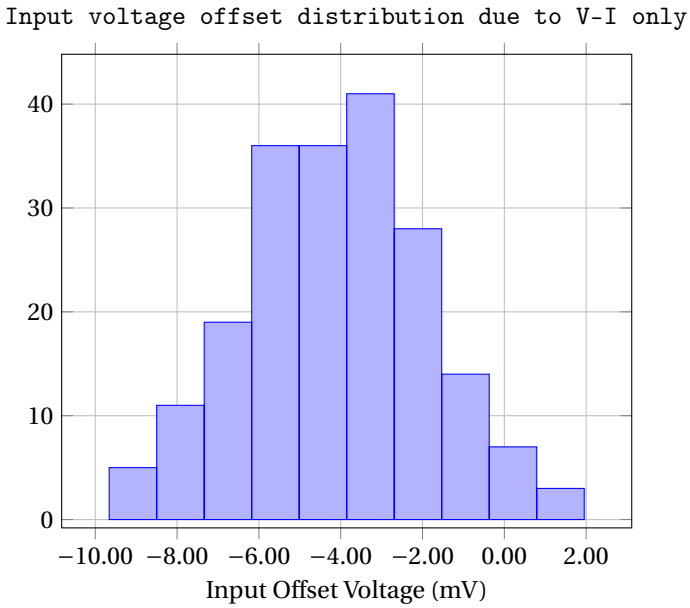


Figure 5.5: Input offset voltage histogram (V-I only). 200 Monte Carlo runs. $\mu = 4.11mV$, $\sigma = 2.24mV$

[1] The offset was considered to be the voltage input difference needed such that there is a $0\mu A$ output current

Unfortunately, the bottleneck for offset performance is the current comparator shown in section 4.1.1. This is due to the fact that inverters inner threshold voltages are highly sensitive to process variations.

In addition, it should be also noted that the $V-I$ to architecture used is inherently asymmetrical, so there will always be a systematic offset, given that the loading of one of the inverters is higher than the other. However, as mention previously, its sigma is relatively low compared to typical differential input-stage comparator. For instance, in [16], figure 6.5, a Monte Carlo simulation is shown for pre-amplifier and comparator stage; its mean offset is low, $0.6mV$, but its standard deviation is $20.2mV$, which is more than double of what we obtained for this comparator.

Delay Dispersion

Due to the inherent asymmetry in the V-I converter stage of the comparator, the system is characterized for a threshold above and below the common-mode level.

As it was shown in chapter 4 that the comparator is the bottleneck for high-speed operation in the peak detector.

Given that the expected input are derivatives of gaussian pulses of different amplitudes (due to fading of the indoor propagation channel), sinusoidal impulses of increasing amplitudes ranging from tens to hundreds of mV were used at $600MHz$ and $1GHz$, so as to obtain delay dispersion due to slew rate and amplitudes altogether.

Table 5.3: Testbench characteristics for Delay Dispersion due to overdrive

Characteristic	**Value**
Pulse type	Sinusoid
Frequencies	$100MHz, 600MHz, 1GHz$
Common-mode input voltage	$900mV$
Threshold	$\pm 20mV$
Sine Amplitude V_{pk}	$40mV - 280mV$
C_{sw}	$2.5pF$
Corners	Typical

For the following plots, the slew rate appearing in the x-axis was calculated as a simple linear approximation of the sinusoid given by:

$$SR = V_{pk}(2\pi f_0) \tag{5.2}$$

where f_0 is the frequency being evaluated.

The delay from input to the output of the comparator stage A_{cp} (refer to figure 5.1) is also included, besides the one corresponding to the entire system driving the load capacitance. Furthermore, the comparator is also tested for negative (below v_{cm}) thresholds, which can be done by easily exchanging the inputs.

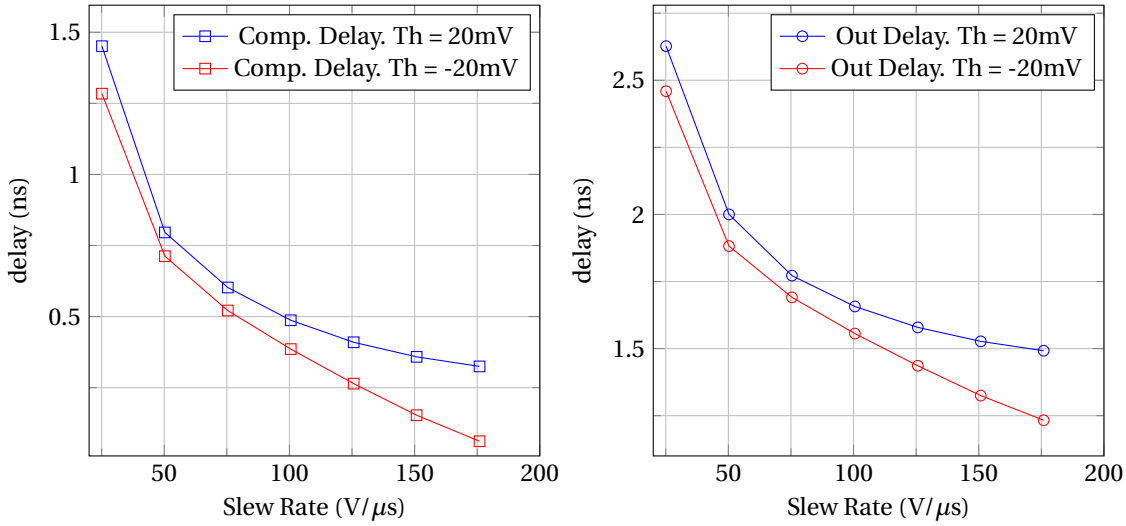


Figure 5.6: Delay as a function slew rate (input frequency = 100MHz) for both output of the comparator (left) and output of the system (right). Threshold = +20mV

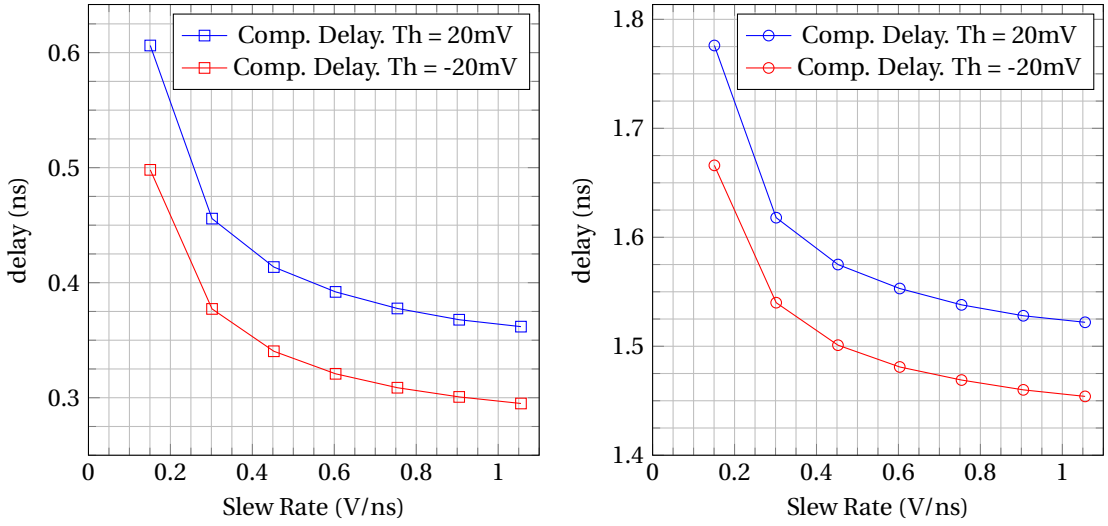


Figure 5.7: Delay as a function slew rate (input frequency = 600MHz) for both output of the comparator (left) and output of the system (right). Threshold = +20mV

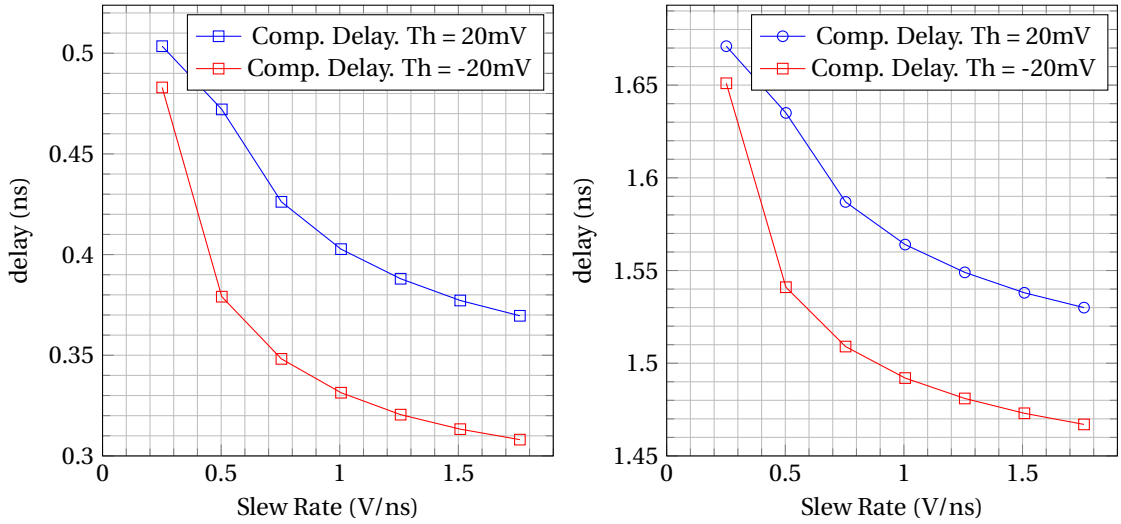


Figure 5.8: Delay as a function slew rate (input frequency = $1GHz$) for both output of the comparator (left) and output of the system (right). Threshold = $+20mV$

The first thing to be noticed, which is also expected, is that the comparator acts faster for negative thresholds. This is due to the fact that the $V-I$ converter output is not loaded by the tail transistors (refer to figure 4.7), therefore, less propagation delay is expected from its input port than from the other input port.

Furthermore, comparing figures 5.6 to 5.7 and 5.8, it can be seen that for the first figure the delay difference keeps increasing as the slew rate is increased, since its input frequency is $100MHz$, while for the rest of the plots the difference between both propagation delays seem to settle at about $60ps$ for slew rates at around $1V/ns$.

An interesting feature to note is the fact that, for instance, in figure 5.8, left plot, the delay for a $1V/ns$ slew rate is about $330ps$, while for figure 5.7, left plot, the propagation delay is about $300ps$. As expected, the frequency also plays a role in the propagation delay; a higher frequency gives less time to the comparator to resolve for bigger the signal, which leads to less time to charge the capacitive input impedance of the current comparator, thus delaying the binary output signal.

This brings to the following figures, which show the same data as a function of amplitude peaks so that the delay dispersion caused by different input frequencies is well illustrated.

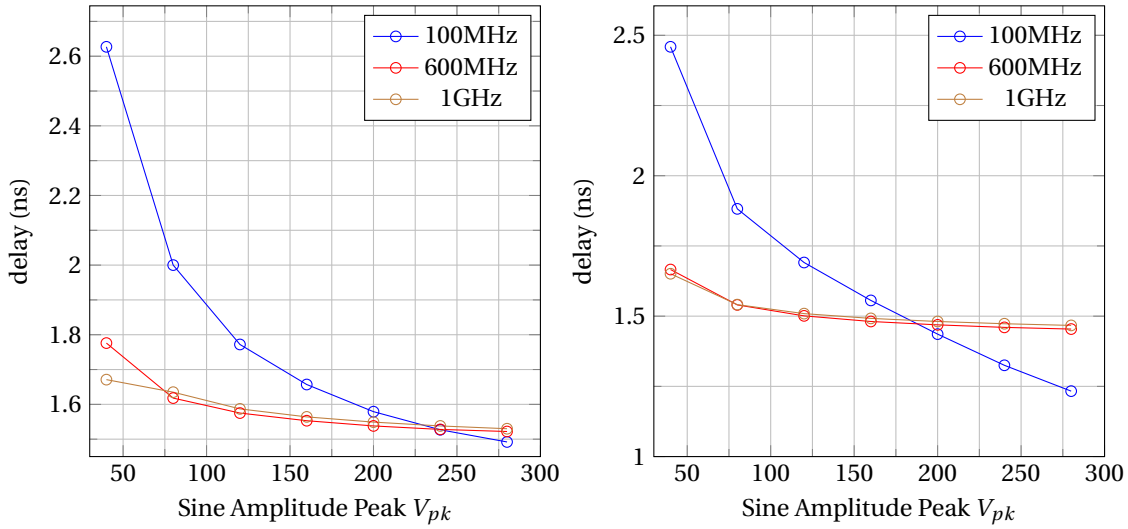


Figure 5.9: Propagation delay measured at the output of the system as a function of amplitude for different frequencies

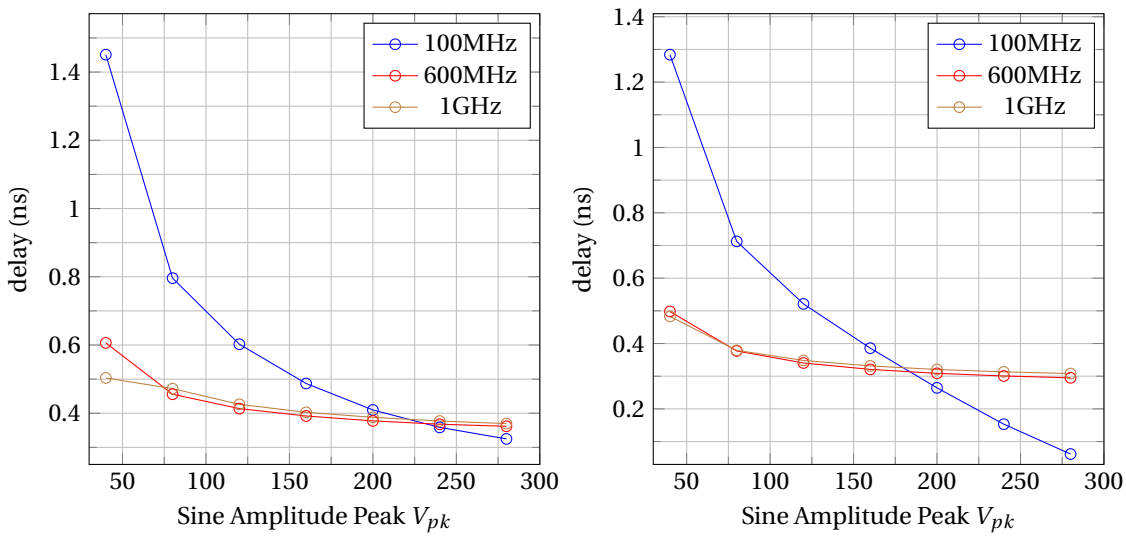


Figure 5.10: Propagation delay measured at the output of the comparator as a function of amplitude for different frequencies

It can be seen from figure 5.9, that an slow signal causes a large delay dispersion, while the delay variation between signal frequencies between 0.6-1 GHz is only bigger by about 100ps for the plot evaluating the positive threshold at a input amplitude of $30mV$, while for the negative threshold, the difference is negligible. This can be explained by the fact that, when a positive input voltage comes from loaded inverter (refer to figure 4.7), the voltage appearing at V_H is an attenuated version of V_{in} (source follower-like operation). However, while V_H is doing a positive swing, V_{bias} is doing a negative swing, thus limiting the current being sourced by such tail transistor.

On the other hand, if we take the other side as an input, the can see that speed propagation of the signal is only limited by C_{gd} of both PMOS and NMOS. The threshold current reference is already precharged by fixing the other input to a certain voltage. The extreme example is found in figure 5.10, where for the a 100MHz signal with an amplitude 290mV, less than $100ps$ of propagation delay can be seen.

5.2. Specifications Summary

Characteristic	Value
Maximum Frequency of Operation	$100MHz-1GHz$
Common-Mode Range	0.6V-1V
Delay	$400ps$ nominal ($600MHz-1GHz$)
Input Offset	$5.835mV$
Delay Dispersion	280ps ($600MHz-1GHz$)
Current Consumption	$3.9mA$ (CLK=1)

Table 5.4: Threshold Detector specifications

5.3. Conclusion

In this chapter, a high-speed low dispersive propagation delay threshold detector is designed. The system is tested against process variations and it demonstrates high performance due to the negative-feedback features of the input stage, which provides it with low offset and increase output current capability. Furthermore, between $600MHz-1GHz$, it has a propagation delay lower than $610ps$ achieving a current consumption of $3.9mA$.

On the other hand, the design of the entire comparator is purely inverter-based, which makes it highly process scalable to be able to handle much higher frequencies of operation.

6

Conclusions and Recommendations for Future Work

In this chapter, conclusions and a summary of the main points presented in this work are discussed. The first section lists the scientific contributions of this work. Finally, a list of recommendations for future research is conferred.

6.1. Conclusion

The design of accurate low-complexity UWB-IR receivers poses a challenge in speed at the circuit implementation level when trying to use the peak detection as a way to determine TOA.

In this work, an original block diagram designed to implement such functionality was reconsidered, an modifications were introduced in order to reduce the source of accuracy errors. It was found that decaying the peak with a linear discharge from a fixed can be a highly accurate way to estimate TOA if we use linear least squares estimation on samples contaminated by quantization and Gaussian additive noise. From the simulations, an upper bound on the maximum ranging error was determined.

In the peak detector block design, it was found that there are way too many topologies to be considered for the task at hand. Therefore, we resorted to classify the topologies into 2 general block diagrams. From there, it was relatively easy to determine how the best peak detector for our system at hand should look like. In particular, it was found that the topologies using a differentiator and a zero-crossing detector offer the unique opportunity to decouple the amplitude detection from time detection of the peak. This is highly desirable as we effectively can cross off a source of error for TOA estimation, which is something not originally proposed in [7]. In addition, these topologies lend themselves to be aided by digital blocks in order to implement the required first peak detection functionality.

The circuit-level design effectively showed that the technology at hand was going to be a limiting factor when trying to achieve GHz-level operation. Thereore, the design was done with process scalability. Based on solely inverters and fully self-biased, the comparators in this work were able to achieve sub-nanosecond propagation delay.

Furthermore, it was shown in the implementation of the threshold detector system that the frequency operation of the comparator greatly benefits from being driven by high amplitudes. In that system, a maximum operating frequency of $1GHz$ was achieved.

The receiver in this work is able, then, to perform time detection and amplitude peak detection for different frequency ranges. Naturally, the time detection is able to achieve much higher operating speed due to not being limited by delay.

Delay dispersion also was considered in the design. Lower than $7cm$ equivalent delay dispersion was achieved at high frequencies.

6.2. Scientific Contributions

- In Chapter 2, a linear discharge is proposed instead of an exponentially decaying one. One reason is its relatively easy implementation in an integrated circuit. However, the most important reason is that one can use linear least squares in order to adaptively determine the slope of the decay considering deviations in the components use. In addition to this, simulations are done considering quantization and additive Gaussian noise, which show reduced TOA error compared to simply averaging the samples.
- In chapter 3, a systematic analysis of general peak detector implementation is made. With this block diagrams in mind, one is able to classify more easily all the peak detectors available in literature, even coming up with one of your own.
- A fast comparator ($< 1ns$ propagation delay)input stage is proposed in order to maximize speed using current-mode techniques. The stage is proven to be robust against process variations and , due to the circuit topologies used, it possesses process scalability features. Given that the V-I converter is able to source or sink currents larger than its static bias, it was sized such that its output impedance was significant enough in order to be dominated by the low input impedance of the current comparator. In this way, we still benefit from the sourcing and sinking capabilities of the V-I converter while still maintaining $Z_{out,V-I} \gg Z_{in,comp}$.
- A high-speed peak detector which is able to trigger on the first peak surpassing a given threshold and ignoring further incoming peaks is designed. To best of my knowledge, no peak detector implementing such functionality has been done before, making this circuit the first of its kind. The functionality is achieved by means of a digital block, thus making the circuit process-scalable. The maximum frequency of operation achieved was $250MHz$ with a static current consumption of $12.3mA$. Maximum delay dispersion obtained was $214ps$ within the $500MHz$ to $900MHz$ frequency range, which is within our initial error budget defined in Chapter 2.
- An analysis of the comparator used was done in order to estimate what kind of errors to be expected given a certain input frequency, a fixed propagation delay and a f_{-3dB}corner frequency from the LPF network.

6.3. Recommendations for Future Work

The development of the UWB receiver in this thesis was limited by the speed provided by the technology at hand. Nonetheless, the research made found valuable blocks and topologies which do not require external biasing and are all inverter-based, which make them easily adaptable to more advanced process nodes. Therefore, an implementation in more advanced nodes, such as $65nm$ or lower, of the design presented in this thesis are encouraged.

In addition, the following recommendations for future work are also provided:

1. *An Alternative Peak Detector*

   During the last stages of this thesis, it was discovered that another implementation option to the peak detector implemented in this work can be conceived, which could potentially be faster, but probably will not reach GHz operating frequencies in $0.18\mu m$ CMOS technology. The block diagram is shown in Figure 6.1.

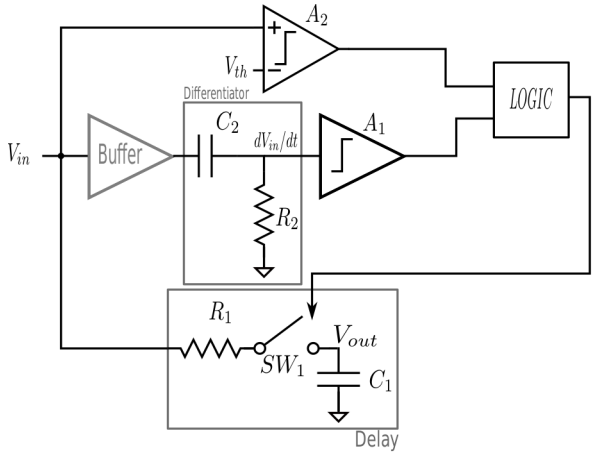


Figure 6.1: Peak Detector - Alternative Implementation

A mere modification can be done to original block diagram shown back Chapter 2, Figure 3.7: Comparator A_1 becomes a current-mode one, and a the capacitor C_2 can perform the ideal differentiator operator to the output voltage of the Buffer. This last element needs to be added since A_1 has an small input impedance if it is current-mode.

Possible issues for further study with this architecture could be the following:

- A_1 can have a high delay dispersion due to the input current that the Buffer can handle
- The amplitude detection problem is not solved yet. Ideally we would like to have an analog delay block which could shift V_{in} in time without much attenuation (Otherwise it has to be accounted in the NF of the system).

2. *Output Driving Buffer*

   An output buffer needs to be implemented in order to drive the next stage. Fortunately, such a buffer does not need to be fast-settling given that in this thesis work we have effectively decouple amplitude peak detection from time peak detection, so if the buffer is slow, it will not do anything to our TOA estimation. This buffer must definitely be optimized for low power.

3. *Differential Input LNA implementation*

   A differential-output LNA is needed in order to drive the peak detector system. A good candidate for such amplifier is the Balun-LNA presented in [9], as it does the single to differential conversion while achieving potentially low noise figures (less than $2dB$). Furthermore, low-impedance sources are needed in order to drive the peak detector. Therefore, it is important that this amplifier is cascaded with buffers with high driving capability.

4. *Digitally Programmable RC and Delay Chains*

   Since the RC network plays an important role in the amplitude error of the peak detected, they should be made programmable in order to have more flexibility when choosing how phase-shifted the dynamic threshold of the peak detector should be. In addition, a negative peak detector could easily be implemented in order to also being able to estimate a possible first-path negative peak.

   On the other hand the receiver and the threshold comparator have digital delay blocks so that the when the comparator is turned on by the clock, some time is given for it to settle and produce valid inputs. The delay chains at the moment are just implemented by current-starved inverters and ideal current sources. A straightforward implementation of a digitally programmable delay chain should be possible since that resolution are in the ns level. A interesting implementation of such a block is done, for instance, in [26].

5. *Reduction of Comparator delay dispersion*

   A lower than $300ps$ delay dispersion was achieved for input frequencies between $600MHz$ and $1GHz$ with input amplitudes ranging from $40mV - 290mV$ for the complete threshold detector system. It

can also be seen that the majority of the dispersion is due to the comparator block (refer to figure 5.9). However, there can be other sources of error from outside the system, therefore, it is always desirable to reduce the comparator delay uncertainty as much as possible. An interesting idea to reduce delay dispersion is presented in [2].

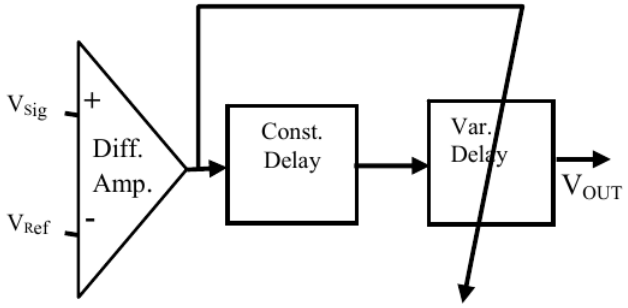
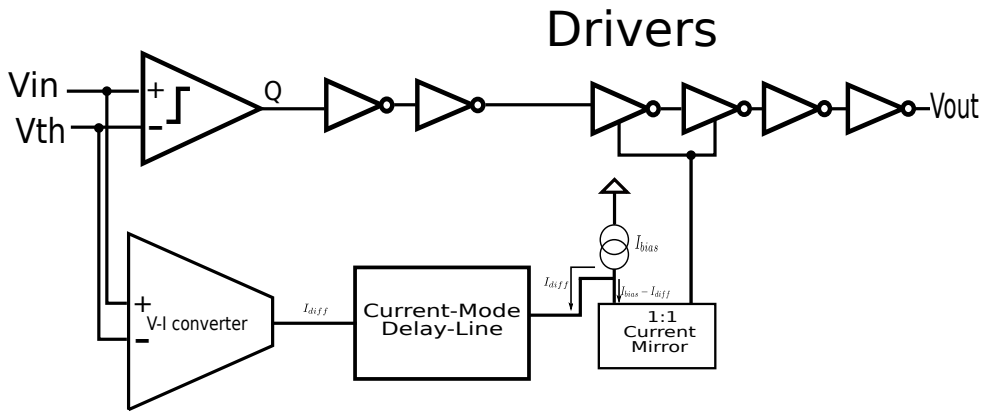


Figure 6.2: Block Diagram of the reduced delay dispersion comparator [2]

The delay dispersion reduction scheme shown in figure 6.2 is as follows: when the differential amplifier provides a positive signal V_{sig} higher than V_{ref}, the positive swing output voltage is fed at the gate PMOS tail transistor of a pair of current-starved inverters, represented by the variable delay block in the figure above. In this way, the current sourcing capability of such PMOS transistor is reduced, thus increasing the delay of such inverter drivers, which compensates for the fast action of a big input voltage. A constant delay block is provided so that the signal has enough time to reach the current-starved inverter drivers. An impressive delay dispersion of only $10ps$ is finally reported.

The problem now is that this scheme is suitable for voltage-mode comparator, while the comparator presented in this work has current-mode processing to extend the bandwidth. Since the voltage swings at the input V-I converter are really small and useless to apply the approach shown above, an analogous current-mode technique could be implemented as shown in the figure below:



A secondary $V-I$ block of the same characteristics could be placed in parallel at the input. Its output current can be fed into a current-mode delay line (see [10]). Then, the output of the this line can be of current-sinking type whose output node is connected to a current-starved inverter with NMOS tail transistor biased with a certain current. Then, when the positive output current of the $V-I$ converter is fed into the delay line, the last block of the delay-line sinks a current I_{diff} proportional to its differential input voltage (could be a unity-gain, for instance) and effectively subtracts from the current source I_{bias}, thus reducing the current the NMOS tail transistor is biased with to $I_{bias}-I_{diff}$, ultimately increasing the delay of those inverter drivers.

6. *Towards Power Delay Profile Estimation*

The power delay profile is a distribution of the signal power received over a multipath channel(such

that of indoor UWB) as a function of propagation delays, which gives relevant information about the channel environment for ranging applications.

The receiver presented in this work is essentially event-driven; it rejects any further incoming pulse after some pulse crossed a predefined threshold first. Therefore, this system can be extended for a serial mode type of operation; in other words, since there's a digital signal that indicates us that a certain peak has been received and stored, then we could use this digital information to activate another branch of the same circuit which will perform the same function (peak detection and time detection of such peak) on the next multipath component, and so on.

7. *More complex ADC model*

   The linear least squares approach to determining TOA in Chapter 2 assumes only additive Gaussian noise and quantization noise. A more realistic model of the ADC considering more noise sources, such as jitter, should be made in order to provide a more realistic prediction on the accuracy of the approach. It might be possible that it might need some modification after more realistic noise sources are modeled.

8. *Exploring Feedback Peak detector and Current-Comparator speed limits*

   Feedback peak detectors can be designed for a particular speed and amplitude error specification if a nullor is used. Once the limits in speed and error have been identified, more realistic high-frequency models of the nullor can be implemented to estimate a maximum input capacitance and minimum gain for a desired speed and amplitude error specification.

   While the peak detector in this work is open-loop, the current-comparator in this work uses non-linear feedback transistor around a saturating amplifier. This means that this amplifier can be replaced for a nullor and the same steps mentioned above can be applied to estimate, for instance, what gain or transconductance value and input capacitance is needed to achieve a certain propagation delay.

   This method can prove useful to decide whether a certain technology node is capable of achieving the high-speed operation needed for this work.

9. *Current Source Implementation and capacitor sizes*

   The current source implementation should be done having precision in mind. A temperature independent and process-variation resilient current source should be implemented. While calibration can be done to estimate fixed variations in slope, temperature changes can occur during the decay, which can translate into a time-varying change in slope. This can be difficult to compensate for in a calibration step.

10. *Digital Blocks Implementation*

    A simplifying assumption was made in the implementation of the digital blocks. These can be made more robust if more states are used. Structured methods to synthesize event-driven circuits can be used for this [19].

Bibliography

[1] 5-Gb/s Peak Detector Using a Current Comparator and a Three-State Charge Pump - IEEE Xplore Document. URL http://ieeexplore.ieee.org/abstract/document/5771061/?section=abstract.

[2] M. Abbas, T. J. Yamaguchi, Y. Furukawa, S. Komatsu, and K. Asada. Novel technique for minimizing the comparator delay dispersion in 65nm CMOS technology. In *2011 18th IEEE International Conference on Electronics, Circuits, and Systems*, pages 220–223, December 2011. doi: 10.1109/ICECS.2011.6122253.

[3] D. Banks and C. Toumazou. Low-power high-speed current comparator design. *Electronics Letters*, 44 (3):171–172, 2008. URL http://digital-library.theiet.org/content/journals/10.1049/el_20083145.

[4] M. Bazes. Two novel fully complementary self-biased CMOS differential amplifiers. *IEEE Journal of Solid-State Circuits*, 26(2):165–168, February 1991. ISSN 0018-9200. doi: 10.1109/4.68134.

[5] Mel Bazes. Self-biased, high-gain differential amplifier with feedback, June 1990. URL http://www.google.com/patents/US4937476. U.S. Classification 326/71, 326/32, 330/253, 327/541, 330/277; International Classification H03H19/00, H03K5/24, H03K17/687, H03K17/30; Cooperative Classification H03H19/004, H03K5/2472, H03K17/302, H03K17/6872; European Classification H03K17/687B2, H03K17/30B, H03K5/24F, H03H19/00B.

[6] Nathaniel Beck. *Ols in matrix form*. 2001. URL https://web.stanford.edu/~mrosenfe/soc_meth_proj3/matrix_OLS_2_Beck_UCSD.pdf.

[7] Giovanni Bellusci. *Ultra-Wideband Ranging for Low-Complexity Indoor Positioning Applications*. Delft, The Netherlands, 2011. ISBN 978-94-6108-133-9. URL http://repository.tudelft.nl/assets/uuid:442168a5-806f-4d64-97a7-0dd5f5b5d513/TR_DISS_5897.pdf.

[8] Maria-Gabriella Di Benedetto. *UWB Communication Systems: A Comprehensive Overview*. Hindawi Publishing Corporation, 2006. ISBN 978-977-5945-10-5. Google-Books-ID: 3KVHnkXnMDEC.

[9] Federico Bruccoleri. *Wide-band low-noise amplifier techniques in CMOS*. [s.n.], [S.l.], 2003. ISBN 978-90-365-1964-9.

[10] Klaas Bult and Hans Wallinga. A CMOS analog continuous-time delay line with adaptive delay-time control. *IEEE Journal of solid-state circuits*, 23(3):759–766, 1988. URL http://ieeexplore.ieee.org/abstract/document/316/.

[11] A. Bruce Carlson, Paul Crilly, and Paul B. Crilly. *Communication Systems*. McGraw-Hill Education, February 2009. ISBN 978-0-07-338040-7.

[12] E.A. Crain and M.H. Perrott. A 3.125 Gb/s Limit Amplifier in CMOS With 42 dB Gain and 1<tex>mu</tex>s Offset Compensation. *IEEE Journal of Solid-State Circuits*, 41(2):443–451, February 2006. ISSN 0018-9200. doi: 10.1109/JSSC.2005.862352. URL http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=1583808.

[13] Antonio D'amico, Umberto Mengali, and Lorenzo Taponecco. Energy-Based TOA Estimation. *IEEE Transactions on Wireless Communications*, 7(3):838–847, March 2008. ISSN 1536-1276. doi: 10.1109/TWC.2008.060545. URL http://ieeexplore.ieee.org/document/4472002/.

[14] R. J. Fontana and E. A. Richley. Observations on Low Data Rate, Short Pulse UWB Systems. In *2007 IEEE International Conference on Ultra-Wideband*, pages 334–338, September 2007. doi: 10.1109/ICUWB.2007.4380965.

[15] D. A. Freitas and K. W. Current. CMOS current comparator circuit. *Electronics Letters*, 19(17):695–697, August 1983. ISSN 0013-5194. doi: 10.1049/el:19830474.

[16] Bernhard Goll and Horst Zimmermann. *Comparators in Nanometer CMOS Technology*. Springer, September 2014. ISBN 978-3-662-44482-5.

[17] Subrata Goswami. *Indoor Location Technologies*. Springer Science & Business Media, July 2012. ISBN 978-1-4614-1377-6. Google-Books-ID: JDQDV4uHGb8C.

[18] I. Guvenc and Z. Sahinoglu. Threshold-based TOA estimation for impulse radio UWB systems. In *2005 IEEE International Conference on Ultra-Wideband*, pages 420–425, September 2005. doi: 10.1109/ICU.2005.1570024.

[19] Brian Holdsworth and Clive Woods. *Digital Logic Design*. Newnes, November 2002. ISBN 978-0-08-047730-5. Google-Books-ID: o7enSwSVvgYC.

[20] Haosheng Huang and Georg Gartner. A survey of mobile indoor navigation systems. In *Cartography in Central and Eastern Europe*, pages 305–319. Springer, 2009. URL http://link.springer.com/chapter/10.1007/978-3-642-03294-3_20.

[21] T. H. Jin, H. G. Han, and T. W. Kim. Time-of-Arrival Measurement Using Adaptive CMOS IR-UWB Range Finder With Scalable Resolution. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 63(10):1605–1615, October 2016. ISSN 1549-8328. doi: 10.1109/TCSI.2016.2583661.

[22] M. K. Kang and T. W. Kim. CMOS IR-UWB Receiver for 9.7-mm Range Finding in a Multipath Environment. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 59(9):538–542, September 2012. ISSN 1549-7747. doi: 10.1109/TCSII.2012.2206932.

[23] Elliott Kaplan and Christopher Hegarty. *Understanding GPS: Principles and Applications*. Artech House, 2005. ISBN 978-1-58053-895-4.

[24] Hans W. Klein and Sriram Narayan. Peak detector for amplitude modulated signals, February 1996. URL http://www.google.com/patents/US5491681. U.S. Classification 369/124.14, G9B/7.066, G9B/21.018, 327/58, G9B/5.218; International Classification G11B5/596, G11B7/09, G11B17/34, G11B15/60, G11B21/10, H03K5/1532; Cooperative Classification G11B7/0901, G11B5/59611, G11B7/0941, H03K5/1532, G11B21/10, G11B17/34, G11B15/602; European Classification G11B21/10, G11B7/09A, G11B5/596C1, H03K5/1532.

[25] M. W. Kruiskamp and D. M. W. Leenaerts. A CMOS peak detect sample and hold circuit. *IEEE Transactions on Nuclear Science*, 41(1):295–298, 1994. URL http://alexandria.tue.nl/openaccess/Metis122846.pdf.

[26] M. Maymandi-Nejad and M. Sachdev. A digitally programmable delay element: design and analysis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 11(5):871–878, October 2003. ISSN 1063-8210, 1557-9999. doi: 10.1109/TVLSI.2003.810787. URL http://ieeexplore.ieee.org/document/1234406/.

[27] Byung-moo Min and Soo-won Kim. High performance CMOS current comparator using resistive feedback network. *Electronics Letters*, 34(22):2074–2076, 1998. URL http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=741290.

[28] L. Ravezzi, D. Stoppa, and G.-F. Dalla Betta. Simple high-speed CMOS current comparator. *Electronics Letters*, 33(22):1829–1830, 1997. URL http://digital-library.theiet.org/content/journals/10.1049/el_19971250.

[29] William Redman-White. A high bandwidth constant g m and slew-rate rail-to-rail CMOS input circuit and its application to analog cells for low voltage VLSI systems. *IEEE Journal of Solid-State Circuits*, 32(5):701–712, 1997. URL http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=568838.

[30] Zafer Sahinoglu, Sinan Gezici, and Ismail Güvenc. *Ultra-wideband Positioning Systems Theoretical Limits, Ranging Algorithms, and Protocols*. Cambridge University Press, Leiden, 2008. ISBN 978-0-511-43681-9 978-1-281-90343-3. URL http://public.eblib.com/choice/publicfullrecord.aspx?p=367066.

[31] L. Stoica, A. Rabbachin, and I. Oppermann. A low-complexity noncoherent IR-UWB transceiver architecture with TOA estimation. *IEEE Transactions on Microwave Theory and Techniques*, 54(4):1637–1646, June 2006. ISSN 0018-9480. doi: 10.1109/TMTT.2006.872056. URL http://ieeexplore.ieee.org/document/1618591/.

[32] P. Stoica and J. Li. Lecture Notes - Source Localization from Range-Difference Measurements. *IEEE Signal Processing Magazine*, 23(6):63–66, November 2006. ISSN 1053-5888. doi: 10.1109/SP-M.2006.248717.

[33] A. T. K. Tang and Christofer Toumazou. High performance CMOS current comparator. *Electronics Letters*, 30(1):5–6, 1994. URL http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=260564.

[34] Xiaoou Tang and K.-P. Pun. High-performance CMOS current comparator. *Electronics Letters*, 45(20):1007–1009, 2009. URL http://digital-library.theiet.org/content/journals/10.1049/el.2009.1419.

[35] H. Träff. Novel approach to high speed CMOS current comparators. *Electronics Letters*, 28(3):310, 1992. ISSN 00135194. doi: 10.1049/el:19920192. URL http://digital-library.theiet.org/content/journals/10.1049/el_19920192.

[36] Wim Vereecken and Michiel Steyaert. *Ultra-Wideband Pulse-based Radio: Reliable Communication over a Wideband Channel*. Springer Science & Business Media, April 2009. ISBN 978-90-481-2450-3. Google-Books-ID: 5TlJ2ShvHcQC.

[37] Lars Wanhammar. *Analog Filters using MATLAB*. Springer Science & Business Media, June 2009. ISBN 978-0-387-92767-1. Google-Books-ID: X3k5V_NDbMEC.

[38] K. Witrisal, G. Leus, G. J. M. Janssen, M. Pausini, F. Troesch, T. Zasowski, and J. Romme. Noncoherent ultra-wideband systems. *IEEE Signal Processing Magazine*, 26(4):48–66, July 2009. ISSN 1053-5888. doi: 10.1109/MSP.2009.932617.

[39] Fei Yuan. *CMOS Current-Mode Circuits for Data Communications*. Springer, 2007. ISBN 978-0-387-29758-3.