Liquid Silicon for Printed Polycrystalline Silicon Thin-Film Transistors on Paper

Trifunovic, Miki

DOI
10.4233/uuid:361057db-a92a-4c1c-82bc-9350b8883ac0

Publication date
2016

Document Version
Final published version

Citation (APA)
Trifunovic, M. (2016). *Liquid Silicon for Printed Polycrystalline Silicon Thin-Film Transistors on Paper*. [Dissertation (TU Delft), Delft University of Technology]. https://doi.org/10.4233/uuid:361057db-a92a-4c1c-82bc-9350b8883ac0

Liquid Silicon for Printed Polycrystalline Silicon Thin-Film Transistors on Paper

LIQUID SILICON FOR PRINTED POLYCRYSTALLINE SILICON THIN-FILM TRANSISTORS ON PAPER

Proefschrift

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. ir. K.C.A.M. Luyben,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op woensdag 14 september 2016 om 12:30 uur

door

Miki TRIFUNOVIĆ

Elektrotechnisch ingenieur,
Technische Universiteit Delft, Nederland,
geboren te Kyoto, Japan.

Dit proefschrift is goedgekeurd door de

promotor: prof. dr. P.M. Sarro
copromotor: dr. R. Ishihara

Samenstelling promotiecommissie:

Rector Magnificus,	voorzitter
Prof. dr. P.M. Sarro,	Technische Universiteit Delft
Dr. R. Ishihara,	Technische Universiteit Delft
Onafhankelijke leden:	
Prof. dr. S.J. Picken,	Technische Universiteit Delft
Prof. dr. T. Sekitani,	Osaka University, Japan
Prof.dr. P. Heremans,	KU Leuven, België
Dr. D.P. Sutija,	Thin Film Electronics ASA, Noorwegen
Dr. O. Wunnike	Evonik Industries, Duitsland

Keywords: Liquid Silicon, solution-processing, flexible electronics, paper electronics, excimer laser crystallization, printed electronics

Printed by: Ipskamp Printing

ISBN/EAN 978-94-028-0315-0

An electronic version of this dissertation is available at
http://repository.tudelft.nl/.

To my family.

CONTENTS

SUMMARY

Moore's law has driven the IC technology industry over the past decades with the goal of reducing electronic feature sizes and increasing functionality of microelectronic chips per unit area. As a result, processing equipment have become increasingly complex and costly. These costs get unnecessarily high for applications that require large surface areas.

Alternative IC fabrication methods have been proposed that are based on liquids rather than gases. Similar to the graphics industry, patterned arrangement of inks could be produced on large area substrates with a high product throughput which would substantially reduce the production cost. In addition, processing by this method at low enough temperatures enables the usage of flexible substrates which would allow new applications to arise that were formerly impossible with high-cost, rigid electronics such as large area, low-cost flexible displays, solar cells, and sensor and actuator systems.

Although silicon is the preferred material for IC fabrication, it cannot directly be used as a liquid. Alternative semiconducting materials such as organics or metal-oxides are being studied due to their applicability as inks. Their properties however, are still inferior to silicon.

In order to use silicon in a solution process, a silicon hydride compound which is liquid at room temperature needs to be used. One of these liquid hydrides is cyclopentasilane (CPS), which has favorable properties among the silicon compound varieties regarding stability and photoreactivity. This material is transformed to a-Si by first curing it into polysilane under UV light, and subsequently baking it to at least 350°C.

High mobility poly-Si TFTs from CPS have been demonstrated in other works. Temperatures used to transform the CPS were however too high for low-cost substrates such as PET, PEN or paper, that generally have a low thermal budget (~150°C). As a result, the process had only limited applications.

The goal of this work was therefore to find a method to fabricate poly-Si TFTs directly on top of low-cost substrates. This would allow the production of extreme low-cost, large area and flexible silicon electronics.

The first step was to synthesize silicon without harming the temperature sensitive substrate. It was observed that the intensity of the UV light for the CPS curing process has a strong effect on the structural change of the material. A high intensity induces a high degree of Si-Si cross-linking of the polysilane chains. This makes the material approaching properties similar to when the polysilane is thermally annealed.

An extremely intense and high power UV source, such as an excimer laser, delivers sufficient energy for the polysilane to crystallize directly into poly-Si without an inter-

mediate a-Si transformation step.

The physics behind the excimer laser crystallization is predominantly thermal rather than photochemical. The substrate stays unharmed due to the short pulse duration (20 ns) and shallow absorption (40 nm). A model has been constructed by finite element analysis, where a KrF laser annealing was simulated and matched to the experimental data.

A crystallization threshold laser fluence of a single pulse was observed at 52 mJ/cm^2 for a polysilane film thickness of 200 nm. For multiple pulses of the same fluence, a decrease in this threshold fluence was observed. Another important fluctuation in the threshold level is a variation in film thickness. Below 100 nm, the threshold level increases hyperbolically due to the nearby interface of the substrate, and later the incomplete absorption of the laser pulse.

The second step was to implement this synthesis in a conventional microelectronic fabrication process, while at the same time keeping the temperature of all fabrication steps below 130 °C. This was done to evaluate the potential of this material on top of low-thermal budget substrates. Low temperature gate-oxide deposition is also an important limitation of the final device performance. The mobilities of the n-type and p-type TFTs reached 91.5 and 87.7 cm^2/Vs, respectively.

The third step was to fabricate TFTs directly on top of paper. Although using this substrate is very challenging due to high roughness and porosity, the cost is extremely low (0.1 cents/dm^2) and the material is biodegradable. For these reasons, one of the key substrates for low-cost electronics will be paper. Mobilities for these devices have reached 0.2 and 6.2 cm^2/Vs for the NMOS and PMOS devices, respectively.

Finally an additive patterning of liquid silicon was investigated that is scalable to a roll-to-roll system. This has been done by using a PDMS flexography/imprinting technique. 1 µm regular features were obtained in this process.

This work has demonstrated for the first time the transformation of liquid silicon (CPS) directly into poly-Si on top of low thermal budget substrates. The resulting material was proven to be suitable for TFTs which are the key building block of electronic circuits. This will enable the application of silicon devices for extreme low-cost large area products. Similar to the graphical printing industry, large rolls of low-cost substrate fed through a roll-to-roll liquid silicon printing system can be envisioned.

SAMENVATTING

De wet van Moore heeft in de afgelopen decennia de IC-industrie gedreven met als doel het verkleinen van de electronische componenten en het verhogen van de functionaliteit per chip-oppervlakte eenheid. Als gevolg zijn IC fabricage-apparatuur steeds complexer en duurder geworden. Deze kosten worden onnodig hoog voor toepassingen die grote oppervlakten vereisen .

Alternatieve IC fabricagemethoden zijn voorgesteld die gebaseerd zijn op vloeistoffen in plaats van gassen. Net als de grafische industrie kunnen inkten in bepaalde patronen worden overgedragen naar grote vlakken op hoge snelheid. Dit zorgt voor een substantiele vermindering van de productiekosten. Daarbij, kunnen flexibele substraten worden gebruikt wanneer de productie op laag genoeg temperaturen wordt uitgevoerd. Als gevolg zullen nieuwe toepassingen ontstaan zoals flexibele beeldschermen, zonnecellen, en sensor/actuatorsystemen die voorheen onmogelijk waren met dure, rigide electronica.

Hoewel silicium de voorkeursmateriaal is voor de IC fabricage, kan het niet rechtstreeks gebruikt worden als vloeistof. Alternatieve halfgeleidende materialen zoals organische of metaaloxiden worden bestudeerd vanwege hun toepasbaarheid als inkten. Hun eigenschappen zijn echter nog steeds inferieur aan silicium.

Om silicium te kunnen gebruiken in oplossingen moet een silicium-hydride samenstelling worden gebruikt dat vloeibaar is op kamertemeratuur. Een van deze vloeibare hydrides is cyclopentasilaan (CPS). Deze heeft gunstige eigenschappen ten opzichte van andere silicium samenstellingen wat betreft de stabiliteit en fotoreactiviteit. Dit materiaal wordt omgezet in a-Si door het eerst uit te harden in polysilaan onder UV-licht, en vervolgens uit te bakken bij minstens 350°C.

Hoge mobiliteit poly-Si TFTs van CPS zijn aangetoond in andere werken. Temperaturen die waren gebruikt om de CPS te transformeren waren echter te hoog voor goedkope substraten als PET, PEN of papier, die over het algemeen een laag thermisch budget (~ 150°C) hebben. Daardoor zijn er slechts beperkte toepassingen.

Het doel van dit werk was daarom het ontwikkelen van een methode om direct poly-Si TFTs te fabriceren bovenop goedkope substraten. Dit zou de productie van flexibele siliciumelectronica op grote oppervlakten met extreem lage kosten mogelijk maken.

In de eerste stap moest silicium gesynthetiseerd worden zonder nadelige gevolgen voor de temperatuur-gevoelige substraat. Er werd waargenomen dat de intensiteit van het UV-licht voor het CPS uithardingsproces een sterk effect heeft op de structurele verandering van het materiaal. Een hoge intensiteit leidt tot een hoge mate van Si-Si verknoping van de polysilaanketens. Hierdoor krijgt het materiaal vergelijkbare eigenschappen

als wanneer deze thermisch zou worden getransformeerd. Een zeer intense en krachtige UV bron, zoals een excimer laser, levert voldoende energie om polysilaan direct te kristalliseren tot poly-Si zonder een a-Si tussenstap.

Het mechanisme van de kristallisatie wordt overheerst door een thermisch effect in plaats van een fotochemische. Het substraat blijft ongeschonden door de korte pulsduur (20 ns) en ondiepe absorptie (40 nm). Een model is opgesteld met eindige elementenanalysie, waarbij een KrF laser verhitting werd gesimuleerd en gekoppeld aan de experimentele data.

Een kristallisatiedrempel voor de laser-energiedichtheid van een enkele puls werd waargenomen bij 52 mJ/cm^2 voor een 200 nm polysilaanlaag. Voor meerdere pulsen van dezelfde energiedichtheid werd een afname van deze drempel waargenomen. Een ander belangrijke fluctuatie van het drempelniveau is de variatie in de laagdikte. Onder de 100 nm stijgt het drempelniveau hyperbolisch door de nabijgelegen grensvlak van het substraat en later door de onvolledige absorptie van de laserpuls.

In de tweede stap werd deze nieuwe transformatiemethode toegepast in de microfabricageproces terwijl tegelijkertijd de temperatuur van alle processtappen onder de 130 °C werd gehouden. Dit werd gedaan om de potentie van deze materialen bovenop substraten met een laag thermisch budget te evalueren. Lage-temperatuur gate-oxide depositie vormde hierbij een belangrijke beperking van de uiteindelijke prestaties van de geproduceerde apparaten. De mobiliteiten van de n-type en p-type TFTs bereikten respectievelijk 91.5, en 87.7 cm^2/Vs

In de derde stap werden TFTs direct bovenop papier gefabriceerd. Hoewel dit substraat zeer uitdagend is vanwege de hoge ruwheid en porositeit, zijn de kosten extreem laag (0.1 cent/dm^2) en is het materiaal biologisch afbreekbaar. Daarom zal een van de belangrijkste substraten voor lage-kosten elektronica papier zijn. Deze NMOS en PMOS apparaten bereikten een mobiliteit van 0.2 en 6.2 cm^2/Vs, respectievelijk.

Ten slotte is een additief patroonvorming van vloeibaar silicium onderzocht die op te schalen is naar een roll-to-roll systeem. Dit is gedaan door middel van een PDMS flexografie/imprinttechniek. 1 µm regelmatige patronen waren verkregen in dit proces.

Dit werk heeft voor de eerste keer de transformatie van vloeibaar silicium (CPS) naar poly-Si aangetoond bovenop substraten met een laag thermisch budget. Het verkregen materiaal was geschikt voor TFTs wat de bouwsteen vormt voor elektronische circuits. Dit zal de toepassing van silicium apparaten voor producten met extreem lage kosten en grote oppervlakten mogelijk maken. Net als bij de grafische printindustrie, zullen later grote rollen van goedkope substraten gevoed worden aan een roll-to-roll vloeibaar silicium printsysteem.

PREFACE

This book is the result of about four years of hard work in the inspiring field of flexible electronics. Of course, as in any project, there were challenges to be overcome, and it is the solving of these challenges that one can grow as a person when pursuing a PhD.

Some of the main reasons for me to decide on pursuing a PhD candidacy, is specifically from a personal development point of view. Because, after a trajectory of 4 years, you may wonder if a company is more interested in someone having worked for them for 4 years, or having pursued a PhD in the same time. Some companies even mention that they prefer graduates, rather than PhDs since a PhD is perhaps too much focused in a specific field.

One of the reasons why I started a PhD in this sense was not to narrow my field but to see how far I can go in a specific direction. The personal development gained from such a process is invaluable, and cannot be obtained by working at a company alone.

A second reason is the topic of my PhD. In my opinion, if you do not like your project, you cannot last mentally the 4 years of your PhD process. It is crucial that you are interested and inspired by your project, in order to stay motivated in the 4 year trajectory. In my case, I was always fascinated by the field of flexible electronics, since this gave me a very visual sense of technological developments. The internship in Japan and my master thesis project were related to this main topic and I had the great opportunity to continue working in this field for my PhD. The knowledge I have gained from those other projects were particularly useful and gave me an advantage in my PhD candidacy.

The third reason is the status that you have as a PhD at the TU Delft. You are considered as an employee, have similar rights to an employee and even get a decent salary. It somehow bothers me to be looked at as someone that was "still studying". This is a strange thing to say because a person should always be studying in a way even if you work for a company. The misconception that a PhD is like a graduate student is too common in the general public. Especially to people from abroad this takes some convincing, since in many other countries the PhD is actually linked to a student status.

A PhD journey is as if you are thrown in a deep well and have to climb your way out. Often in this struggle you may fall back to where you started, but have gained valuable experience in the process. The journey towards climbing out this pit, developed me in a

significant way, and could only be done with the right people around me as well as the proper supervision that pushes my boundaries. As Ernest Hemingway stated: "It is good to have an end to journey toward; but it is the journey that matters, in the end.

"It is good to have an end to journey toward;
but it is the journey that matters, in the end."

-Ernest Hemingway

Developments in time-planning, reactions to set-backs, and both individual efforts as well as teamwork are some of the traits that are developed significantly during a PhD.

Time-planning

Although studying at a university itself exposes you to various time-planning challenges, it is the number of deadlines during the PhD that you really find yourself pushing your limits, without questioning if everything would have been worth it in the end. At times finding myself working until well past midnight in the office. Your dedication will truly be tested, and you have to wonder if time-planning could have prevented these moments.

Set-backs

I believe in any project, both small and large, set-backs are inevitable. One of the larger set-backs that I have experienced was regarding one of the most important tools for my project: the excimer laser. A well-functioning machine with high precision and cleanliness in our lab was removed for cost reasons. Coping with such sudden and unexpected changes in the environment, especially with one of the key tools for my process was particularly tested. At these times, collaborations have helped ease this pain in a sense.

Individual efforts

At a certain time in my 2nd and 3rd year of my candidacy. I found myself working on my type of project alone. In other words, no one in my department was working even remotely on my project. At these times literature studies and delving into

deep discussions with colleagues from around the world was a particularly important source of knowledge. Optimizing processes in these situations becomes however relatively slow and challenging.

Team efforts

I found that working in teams at the same project significantly advances the research. Working with chemists and physicians that approach a project in a different way was very helpful, and I gained knowledge in the process that I could not have been achieved on my own. For that, I thank my fellow colleagues.

Besides these project-related developments, I always wanted to explore more social related skills. Particularly the Micro-Electronic System and Technology association where I was president of for a bit over two years helped me gain organizational skills and stay connected to fellow PhD and master students from different departments, as well as people from the industry. In the final year of my PhD I also joined the PhD council where I have discussed at high level the development of the PhD process. I noticed that I am the type of person that likes to stay inside the loop, and being well-connected, although this was particularly difficult in my final year.

During these four years, sports played an important role in my life to release some of the stress that was accumulated during the working day. Besides going to the gym, basketball played especially an important part of my life. In my opinion, this sport is one of the few sports where you develop all your muscles in a more or less equal way, have good team-work, strategy, and makes you in general tougher due to its full-contact nature (some injuries were of course inevitable).

Finally, and most importantly, I want to mention my family, friends and especially my new family that have supported me during my PhD process. I started dating my girlfriend (soon to be wife) during the first year of my PhD. At the time, in my opinion, I had a little more time to spare and found that having a girlfriend would be the right time. I always disliked a half-relationship, where I couldn't put in enough time to make it really work. So I started to spend more time in this area, and actually found her to be the best person in my life that I could ask for. She has a strong character, and knows what she wants. She knows what is right and wrong and tells me this, which is sometimes rare to find in relationships. She is the type of person that makes me want to always improve myself, and for that I am thankful. I remember her telling me that she wants to move in with me after a few months of dating. At the time I thought that this was quite early since

we didn't know each other that well either. When I agreed, and we started living together, of course we had a lot of difference in opinion, but it was important that we understood each other to a higher level. She supports me unconditionally, and helps me with the troubles that I have both at work as well as in my private life. Now we have a beautiful child together, and are getting married. I have to say that it is mainly thanks to her that I could successfully cope with my PhD journey.

Miki Trifunović
Delft, March 2016

List of Abbreviations

1D	1 Dimensional
^{1}H NMR	Proton Nuclear Magnetic Resonance
2TA	2 Phonon Transverse Acoustic
2TO	2 Phonon Transverse Optical
3D	3 Dimensional
a-Si	amorphous silicon
a-Si:H	hydrogenated amorphous silicon
ALD	Atomic Layer Deposition
BP	Boiling Point
CHS	Cyclohexasilane
CMOS	Complementary Metal-Oxide-Semiconductor
CPS	Cyclopentasilane
CTE	Coefficient of Thermal Expansion
CV	Capacitance to Voltage
CVD	Chemical Vapor Deposition
Cz	Czochralski
c-Si	single-crystalline silicon
DI	Deionized
DRIE	Deep-Reactive-Ion-Etching
DSC	Differential Scanning Calorimetry
DTA	Differential Thermal Analysis
DTG	Differential Thermal Gravimetry
ELA	Excimer Laser Annealing
ELPA	Excimer Laser Pre-Annealing
FTIR	Fourier Transform Infrared Spectroscopy
FUV	Flood UV
FWHM	Full-Width-Half-Maximum
HMDS	Hexamethyldisilazane
HW-CVD	Hot-Wire Chemical Vapor Deposition

IC	Integrated Circuit
IPA	Isopropanol
LA	Longitudinal Acoustic
LED	Light-Emitting-Diode
LO	Longitudinal Optical
LPCVD	Low-Pressure Chemical Vapor Deposition
LTPS	Low-Temperature Polycrystalline Silicon
LVD	Liquid Vapor Deposition
MOS	Metal-Oxide-Semiconductor
MP	Melting Point
μ-Cz	micro-Czochralski
NMOS	Negative type Metal-Oxide-Semiconductor
NPS	Neopentasilane
PDMS	Polydimethylsilazane
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PEN	Polyethylene naphthalate
PES	Phosphoric/Acetic/Nitric Acid mixture
PET	Polyethylene terephthalate
PI	Polyimide
PLD	Pulsed Laser Deposition
PMOS	Positive type Metal-Oxide-Semiconductor
PP	Polypropylene
PVD	Physical Vapor Deposition
poly-Si	Polycrystalline Silicon
RFID	Radio-frequency Identification
RF-PECVD	Radio-Frequency Plasma-Enhanced Chemical Vapor Deposition
RMS	Root-Mean-Square
RT	Room-temperature
SEC-MALLS	Size-Exclusion Chromatography, Multi-Angle Laser Light Scattering
SEM	Scanning Electron Microscope
TDS	Thermal Desorption Spectroscopy
TEM	Transmission Electron Microscope
TEOS	Tetraethylorthosilicate
TFT	Thin-Film Transistor
TIS	Total Integrating Sphere
TA	Transverse Acoustic

TG	Thermal Gravimetry
TO	Transverse Optical
TOF-SIMS	Time-of-Flight Secondary Ion Mass Spectrometry
UHF-RFID	Ultra-High-Frequency Radio-Frequency-Identification
ULSI	Ultra Large-Scale Integration
UV	Ultraviolet
UWT	Upper Working Temperature

1

INTRODUCTION

As electronics are playing an ever increasing part of our daily lives, ways to advance the integrated circuits (ICs) are continuously being researched on many different levels: from material technology, to circuit design and packaging. From the material technology perspective, a number of developments have helped boost this industry.

Using silicon as the semiconductor material the development of electronics have been focusing on reducing the electronic feature sizes. By doing so, higher switching speeds and an overall increase in device density per unit area can be obtained. As a result, smaller IC areas contain higher functionality and computational power.[1]

Although many advantages exist in pursuing this feature minimization, IC fabrication processes have as a result become increasingly complex and costly. Five key aspects of the fabrication process can be analyzed that make it expensive:

1. Silicon synthesis: Extraction of high purity silicon from its raw materials is conducted in highly controlled environments at high temperatures. Commonly a process known as the Czochralski (Cz) method[2] is used to grow large, pure crystalline silicon ingots, from which high quality silicon wafers are extracted. These wafers are then used as the base substrate in which electronic devices are created.

2. Vacuum conditions: Since many of the processing steps involve gases, a vacuum environment is generally needed to deposit or treat the electronic materials. Such processes increase the total time required for a fabrication step, due to the pumping up and down times of the confined process chamber. In addition, the size of the IC is also limited to the size of the vacuum chamber, making the production of large area electronics challenging.

3. High temperatures: For film conditioning, annealing, and deposition purposes, temperatures from a few hundred up to approximately 1000 °C are necessary. Besides the costs of maintaining such a controlled, high temperature environment, another disadvantage is that low-cost flexible substrates cannot be used, since these generally have a low thermal budget.

4. Subtractive processing: Patterning in ICs is done using a photolithography process as shown in Fig. 1.1 a. For each pattern, the desired material needs to be deposited over the whole wafer first. Then the material is coated with a light-sensitive organic masking film. A patterned arrangement of light exposure allows parts of this organic film to be soluble, and subsequently be dissolved in a developing agent. The previously deposited film can then be etched in the opened areas of the mask. Finally, the organic mask is removed. This whole process of creating a pattern requires a cycle of six steps that has to be repeated many times (>30 levels in industry[3]) for the various components in the IC. As a result, patterning is very time consuming, and creates a substantial amount of waste.

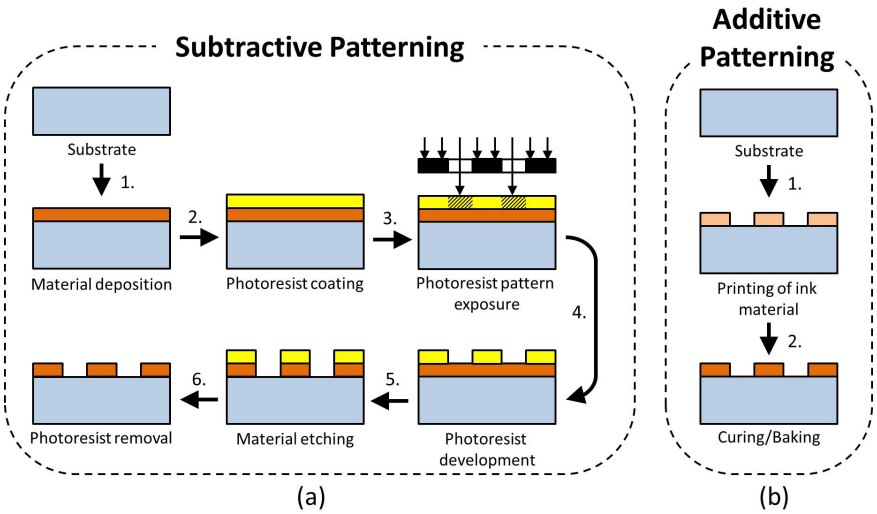

Figure 1.1: Subtractive (a) and additive (b) pattern formation.

5. Batch processing: ICs are processed in batches of wafers. These may be chemically or thermally treated in a batch at the same time. In many process steps however individual wafers need to be processed sequentially for instance for spin-coating photoresist or for dry etching or deposition processes. This leads to a relatively low product throughput.

For applications that use large areas such as displays and solar cells, this level of complexity, and the densification of the IC will require unnecessary high manufacturing costs. Alternative fabrication methods are therefore being developed. Using liquid materials rather than gases, for example, is a viable solution, and can be observed from everyday printing systems.

1.1. PRINTING ELECTRONICS

Printing is a well established process that involves patterning of liquids. It generally requires an ambient pressure, and only in limited cases does it require high treatment temperatures. It is based on additive processing, which means that the patterned material in its desired shape is directly transferred onto a target substrate, followed by a solidification treatment. Therefore, instead of six steps as observed from the typical subtractive processing method, only two are required, as shown in Fig. 1.1 b. In addition, printing can be scaled up to mass production where large sheets or webs are fed through the printing system, enabling high product throughput. All of these advantages make a printing process for electronics very attractive[4–6].

Elemental silicon cannot be used as a molten liquid: with a melting point of over 1400 K, machines that have to handle these temperatures would be extremely costly. Liquids that can be handled at room temperatures are therefore much more preferable; although the choice of materials that have both a semiconducting function, and can be treated as a liquid at room temperature is limited. In recent years, two types of semiconducting materials have been extensively researched: organic and metal-oxide materials.

1.1.1. ORGANIC SEMICONDUCTORS

Organic materials can be easily prepared as liquid solutions for printable inks. In addition, in order to become electronically active, they can be treated at relatively low temperatures which allows the usage of flexible substrates. Flexible organic devices have been created for various applications such as robot skins [7], flexible bio-sensors [8], electronic banknotes [9], and flexible displays[10], among others. Some of these applications are shown in Fig. 1.2.

This type of material, however, has a number of disadvantages compared to silicon[5]. Although sufficient for simple electronic applications, for more demanding and complex circuitry, they have insufficient charge carrier mobilities. Their mobilities are generally in the order of 1 cm^2/Vs, which is similar to the mobilities obtained by a-Si, but two to three orders of magnitude lower than mobilities of conventional crystalline silicon devices (~100 cm^2/Vs for LTPS[12], ~500 cm^2/Vs for ULSI[13]). In addition, the devices

(a) (b) (c)

Figure 1.2: Examples of organic electronic applications: flexible bio-sensors (a)[8], electronics on banknotes (b)[9], flexible displays (c)[11].

degrade fairly quickly over time, since they have a poor chemical stability to water and oxygen due to their organic nature. Finally, unlike silicon, they have a natural tendency of being positive semiconductors, and as a result, their negative counterpart has much lower mobilities. This makes power efficient complementary circuitry impractical using organic electronics alone.

1.1.2. METAL-OXIDE SEMICONDUCTORS

Metal-oxide materials can achieve typical mobilities of an order of magnitude higher than organic devices; approximately 10 cm^2/Vs [14–16]. They too can be used as a solution at room-temperatures, and can be deposited on flexible substrates for similar applications. Another important advantage for this material type is that they can reach their typical mobility in their amorphous configuration, which reduces process complexity. In addition, they are optically transparent, which leads to new applications such as optically transparent displays. Some of the applications for metal-oxide electronics are shown in Fig. 1.3.

Similar to organic devices this type of material still has an order of magnitude lower charge carrier mobilities than compared to crystalline silicon. In addition, for these materials, a good positive counterpart to their negative device is difficult to find, again leading to power inefficient complementary circuitry. Stability is also an issue in this type of devices, since the threshold voltage may shift as a result of negative bias or even light exposure [15].

(a) (b) (c)

Figure 1.3: Examples of metal-oxide electronic applications: flexible display (a)[17], transparent laptop display (b)[18], transparent display case (c)[19].

1.2. LIQUID SILICON

In 2006, the group led by Prof. Shimoda found that silicon based polymers can be handled as liquids at room temperatures, and can be transformed into solid amorphous or polycrystalline silicon. In particular, they used cyclopentasilane (CPS), a five-silicon ring-molecule with two hydrogen atoms attached to each silicon atom. They created polycrystalline silicon (poly-Si) thin-film transistors (TFT) from this precursor[20].

This group demonstrated the first solution-processed silicon device with higher mobilities than organic or metal-oxide transistors (106 cm^2/Vs). The SEM image of one of their transistors is shown in Fig. 1.4 a.

In 2011, Zhang et al. [21] used this silicon ink to create high mobility poly-Si TFTs, by using a μ-Czochralski process [22–24] in which large crystal grains of several micrometers were location-controlled. The SEM image of these grains are shown in Fig. 1.4 b. Mobilities of 391 and 111 cm^2/Vs for negative and positive type devices were reached respectively.

In 2013, Zhang et al. [25] reduced the solid silicon synthesis temperature to 350 °C, which was used to form a device on top of a polyimide substrate. This led to the first liquid silicon based flexible device, shown in Fig. 1.4 c.

Although high in electric performance, the material required relatively high annealing temperatures compared to other solution-based processes. The polymer substrate with the highest thermal resistance is polyimide and can be treated at a maximum temperature of approximately 350 °C [26]. This polymer however, is still around five to ten times more expensive than polyethylene naphthalate (PEN) and polyethylene terephthalate (PET)[27, 28], that are commonly used for soda bottles and regarded as low-cost polymers. These typically cannot be processed above 150 °C (PEN) and 120 °C (PET).

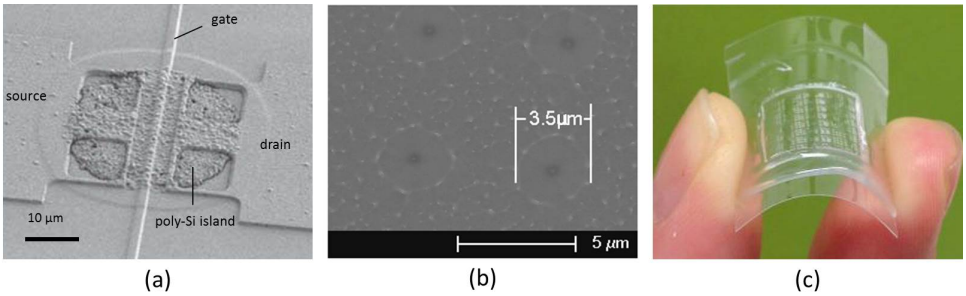

Figure 1.4: SEM images of the first liquid silicon TFT (a)[20], and location-controlled grains (b)[21]. Image of flexible liquid silicon TFTs (c)[25].

1.3. COMPARISON IN TECHNOLOGIES

The solution-based silicon was found as a way to bridge the gap between low cost solution-based materials, and high performance bulk silicon. Table. 1.1 compares mobilities, maximum process temperatures, stability, and cost per unit area for the different solution-based materials and additionally the solid silicon standard created from the Cz process.

From this table it is clear that poly-Si devices produced from liquid silicon embrace the best of both worlds, having both high electric performance and low costs. The only limitation in this process is the relatively high processing temperature that prevents the usage of truly low-cost substrates.

Table 1.1: Comparison in solution-based transistor technologies.

	Organic	Metal-oxide	poly-Si (CPS)	c-Si (Cz)
Electron Mobility (cm^2/Vs)	0.01	10	300	700
Hole Mobility (cm^2/Vs)	1	1	100	400
Temperature (°C)	<100	<100	>350	>1000
Stability	O_2 and H_2O sensitive	light sensitive	stable	stable
Cost per unit area	low	low	low	high

A method that enables the liquid silicon to solid silicon transformation process at lower temperatures, would allow the usage of low-cost, flexible substrates such as PET, PEN or even paper. The cost of various substrates together with their upper working temperatures are presented in Table 1.2. These values are taken from substrates that are produced for printed electronic purposes[29, 30], which are more robust and expensive than those used for instance in packaging of goods. By using low cost polymer or paper

sheets, large scale printing of flexible silicon electronics becomes economically attainable, and solve many of the cost issues that large area IC processes face today.

Table 1.2: Comparison of substrate cost and upper working temperature[29, 30].

	rigid		flexible			
	Si	Glass	PI	PEN	PET	Paper
Price (€/dm^2)	14.12	4.82	8.16	2.58	1.14	0.13
UWT (°C)	>1000	>1000	250-320	155	115-170	130

A large scale electronic printing process, similar to the graphics industry can be envisioned: Large printer rolls can apply different types of materials pre-patterned onto a large area, low-cost, flexible substrate. After every patterning step, a certain curing or annealing treatment is necessary to solidify and/or activate the transferred material. Different rolls apply different materials which requires high precision alignment. Using this process, high product throughput is the result that can significantly drive the fabrication cost of ICs down. This vision is illustrated in Fig. 1.5.

Widespread applications of this process include: fully flexible displays with integrated drivers, low-cost electronic packaging with displays and sensors, large area biosensors, low-cost ultra high frequency RFID tags (UHF-RFID), flexible logic/memory, and flexible Si solar cells, to name a few.

1.4. RESEARCH OBJECTIVE

Mobilities of silicon devices produced from liquid silicon have proven to excel far above those that were obtained using organic or metal-oxide semiconductors. By using this material as a solution, advantages from the printing industry would drive the processing costs to a minimum.

Finding an alternative for the limiting thermal annealing process would solve the final key disadvantage that liquid silicon has over the other printable materials. The goal of this thesis is therefore to achieve the following:

Fabricating silicon transistors by a solution-based process on top of inexpensive substrates with a low thermal budget.

This work will focus on creating a liquid-silicon based transistor, which is the main building block of electronics, at low temperatures. It is a first step towards more complex circuitry and is a good device to demonstrate and optimize the material capabilities.

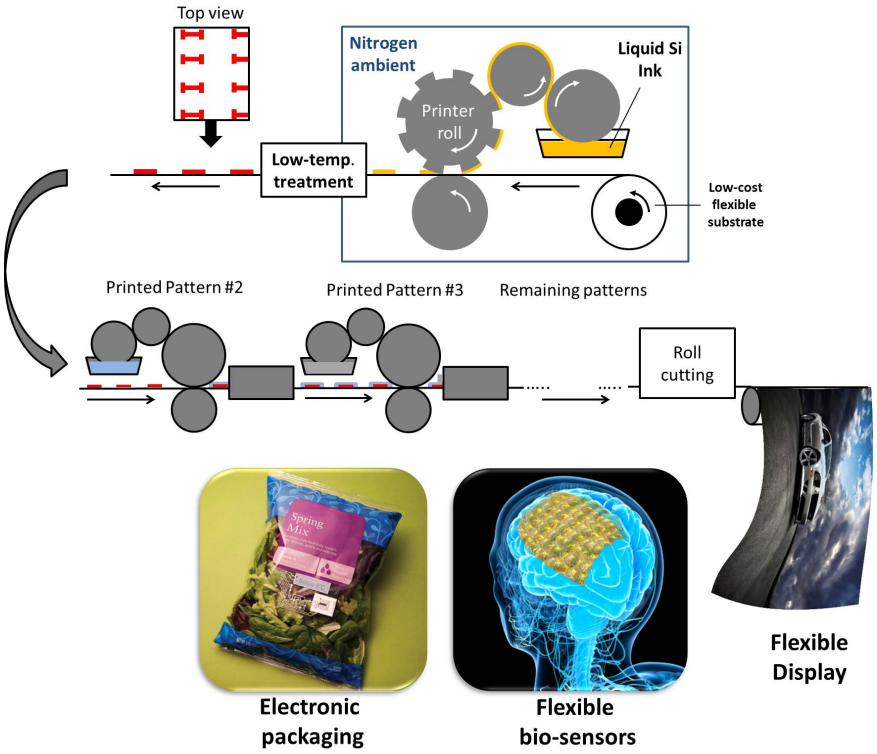

Figure 1.5: Vision of low-cost, high-performance flexible electronic fabrication and applications.

Liquid silicon in this work refers to CPS, or polymerized CPS, also referred to as polysilane. As a first step towards low thermal budget substrate usage, a temperature of approximately 150 °C will be aimed at. At these temperatures special types of PEN and paper substrates could be used. Therefore, once a low-temperature process for liquid silicon is developed, devices will be fabricated on top of paper substrates.

Initially, the liquid solution will be coated using a method that could be scaled up to a roll-to-roll compatible system, which is doctor blade coating.[31] A simple printing process will subsequently be investigated to demonstrate the capabilities of additive processing of the silicon ink.

1.5. OUTLINE OF THIS THESIS

The outline of this thesis is depicted in Fig. 1.6.

This work will introduce, in Chapter 2, the basic properties of CPS, and also present the previous research that has gone into this material concerning electronics, in order to

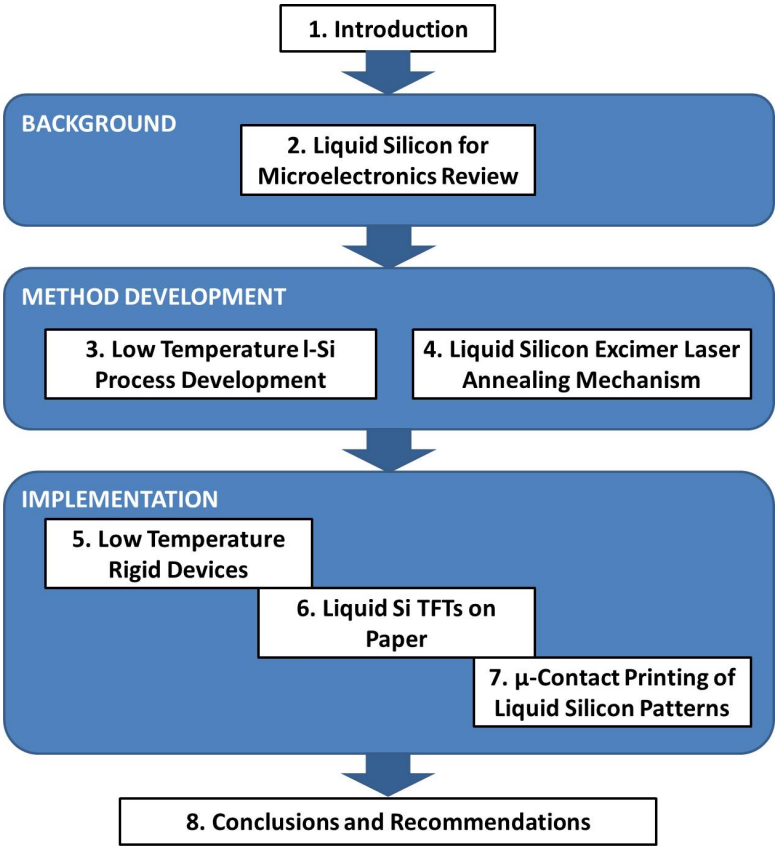

Figure 1.6: Outline of this thesis.

gain the necessary material knowledge for the process development.

Chapter 3 presents the development of a low-temperature process through experimentation. The obtained results are analyzed using various measurement tools.

The mechanism of the transformation to silicon from this newly developed process will be further investigated using transient heat simulations, and compared to the experimental results. This will be presented in Chapter 4.

In Chapter 5 the first devices that are created using this method are presented. These devices are fabricated on a rigid substrate, and conventional silicon processing steps are performed below a maximum processing temperature of 150 °C.

The first low-thermal budget substrate devices are produced and discussed in Chapter 6. A silicon device based on liquid silicon is created directly on top of paper. Its fabrication process and results are discussed.

From a coating process that still employs subtractive patterning, a step towards an actual printing process needs to be taken. Chapter 7 evaluates the printability of CPS by flexography using a polymer stamping method.

Finally, Chapter 8, concludes this thesis of printing liquid silicon on top of inexpensive substrates with low thermal budgets and gives a short discussion and recommendations for future work.

REFERENCES

[1] C. A. Mack, *Fifty years of moore's law,* Semiconductor Manufacturing, IEEE Transactions on **24**, 202 (2011).

[2] D. Neamen, *Semiconductor physics and devices* (McGraw-Hill, Inc., 2002).

[3] *Intel corporation, 22nm process technology,* online (2011).

[4] J. Perelaer, P. J. Smith, D. Mager, D. Soltman, S. K. Volkman, V. Subramanian, J. G. Korvink, and U. S. Schubert, *Printed electronics: the challenges involved in printing devices, interconnects, and contacts based on inorganic materials,* Journal of Materials Chemistry **20**, 8446 (2010).

[5] E. Cantatore, *Applications of organic and printed electronics* (Springer, 2013).

[6] S. Khan, L. Lorenzelli, and R. S. Dahiya, *Technologies for printing sensors and electronics over large flexible substrates: A review,* Sensors Journal, IEEE **15**, 3164 (2015).

[7] H. Kawaguchi, T. Someya, T. Sekitani, and T. Sakurai, *Cut-and-paste customization of organic fet integrated circuit and its application to electronic artificial skin,* Solid-State Circuits, IEEE Journal of **40**, 177 (2005).

[8] M. Kaltenbrunner, T. Sekitani, J. Reeder, T. Yokota, K. Kuribara, T. Tokuhara, M. Drack, R. Schwödiauer, I. Graz, S. Bauer-Gogonea, *et al.*, *An ultra-lightweight design for imperceptible plastic electronics,* Nature **499**, 458 (2013).

[9] U. Zschieschang, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, and H. Klauk, *Organic electronics on banknotes,* Advanced Materials **23**, 654 (2011).

[10] W.-C. Tang, C.-H. Hsu, K.-Y. Lin, P.-W. Chen, Y.-L. Hsu, Y.-L. Wang, K.-Y. Chang, Y.-S. Chang, and C.-C. Tsai, *65.4: Organic thin film transistor driven backplane for flexible electrophoretic display,* in *SID Symposium Digest of Technical Papers*, Vol. 46 (Wiley Online Library, 2015) pp. 973–975.

[11] M. Smith, *New sony flexible oled display (rollable around a pencil) to have applications in the superyacht industry,* Online (2010).

[12] S. M. Lee, C. H. Lee, T. H. Jeong, and H. J. Kim, *The electrical properties of low temperature polycrystalline si thin film transistor prepared by nickel-ald process,* ECS Transactions **13**, 367 (2008).

[13] L. Perron, A. Lacaita, A. Pacelli, and R. Bez, *Electron mobility in ulsi mosfets: Effect of interface traps and oxide nitridation,* Electron Device Letters, IEEE **18**, 235 (1997).

[14] E. Fortunato, P. Barquinha, and R. Martins, *Oxide semiconductor thin-film transistors: A review of recent advances,* Advanced Materials **24**, 2945 (2012).

[15] J. K. Jeong, *The status and perspectives of metal oxide thin-film transistors for active matrix flexible displays,* Semiconductor Science and Technology **26**, 034008 (2011).

[16] J. Park, J. K. Jeong, Y.-G. Mo, H. D. Kim, and S.-I. Kim, *Improvements in the device characteristics of amorphous indium gallium zinc oxide thin-film transistors by ar plasma treatment,* Applied Physics Letters **90**, 262106 (2007).

[17] *Small high resolution igzo displays in co-development from sharp and sel,* online (2012).

[18] I. Nedelcu, *Samsung to bring transparent commercial displays in september,* online (2012).

[19] J. Rigg, *Transview touch-sensitive transparent display case eyes-on,* online (2013).

[20] T. Shimoda, Y. Matsuki, M. Furusawa, T. Aoki, I. Yudasaka, H. Tanaka, H. Iwasawa, D. Wang, M. Miyasaka, and Y. Takeuchi, *Solution-processed silicon films and transistors,* Nature **440**, 783 (2006).

[21] J. Zhang, R. Ishihara, H. Tagagishi, R. Kawajiri, T. Shimoda, and C. Beenakker, *Single-grain si tfts using spin-coated liquid-silicon,* in *Electron Devices Meeting (IEDM), 2011 IEEE International* (IEEE, 2011) pp. 14–5.

[22] R. Ishihara and M. Matsumura, *Excimer-laser-produced single-crystal silicon thin-film transistors,* Japanese journal of applied physics **36**, 6167 (1997).

[23] R. Ishihara, P. C. van der Wilt, B. D. van Dijk, A. Burtsev, F. Voogt, G. Bertens, J. Metselaar, and C. Beenakker, *Advanced excimer laser crystallization techniques of si thin film for location control of large grain on glass,* in *Photonics West 2001-Electronic Imaging* (International Society for Optics and Photonics, 2001) pp. 14–23.

[24] R. Ishihara, J. Zhang, M. Trifunovic, J. Derakhshandeh, N. Golshani, D. M. T. Mofrad, C. Tao, K. Beenakker, and T. Shimoda, *Single-grain si thin-film transistors for monolithic 3d-ics and flexible electronics,* IEICE Transactions on Electronics **97**, 227 (2014).

[25] J. Zhang, M. Trifunovic, M. Van Der Zwan, H. Takagishi, R. Kawajiri, T. Shimoda, C. Beenakker, and R. Ishihara, *Single-grain si thin-film transistors on flexible polyimide substrate fabricated from doctor-blade coated liquid-si,* Applied Physics Letters **102**, 243502 (2013).

[26] A. Pecora, L. Maiolo, M. Cuscuná, D. Simeone, A. Minotti, L. Mariucci, and G. Fortunato, *Low-temperature polysilicon thin film transistors on polyimide substrates for electronics on plastic,* Solid-state electronics **52**, 348 (2008).

[27] J. Fjelstad, *Flexible circuit materials,* Circuit World **34**, 19 (2008).

[28] D. Tobjörk and R. Österbacka, *Paper electronics,* Advanced Materials **23**, 1935 (2011).

[29] Goodfellow, *Alphabetic list of materials,* online (2016).

[30] *Arjowiggins creative papers, powercoat,* online (2016).

[31] Y.-H. Chang, S.-R. Tseng, C.-Y. Chen, H.-F. Meng, E.-C. Chen, S.-F. Horng, and C.-S. Hsu, *Polymer solar cell by blade coating,* Organic Electronics **10**, 741 (2009).

2

Liquid Silicon for Microelectronics Review

Solution-based processing of silicon has been used at relatively high conversion temperatures of 350 °C and higher. In order to successfully employ liquid Si for electronics on low thermal budget substrates, the material has to be well understood. Many research institutes have been engaged in both the material characterization and device fabrication using it as a precursor. This chapter provides a literature review about liquid silicon characteristics.

This chapter will first give the definition of liquid silicon in section 2.1, and present the material used for this work: cyclopentasilane. Its characteristics are subsequently explained in section 2.2. This is followed by an explanation of how it is used as a precursor for solid silicon, through photochemical and thermal transformations in section 2.3. Section 2.4 deals with the research concerning Si TFT fabrication employing liquid Si. Opportunities found in this research are subsequently highlighted in section 2.5. Finally, the chapter is concluded with a brief summary in section 2.6.

2.1. INTRODUCTION

The term liquid silicon may cause confusion since it is not referred to a molten form of silicon that would require high temperatures (>1440 K). Although this would allow silicon to be in the liquid phase, processing at such high temperatures would be impractical and costly.

In this work, liquid silicon is referred to a class of Si-based polymers that are liquid at room temperature, and after a curing or annealing treatment, transform into solid silicon. A wide range of materials fall into this category, and most of them are based on silicon hydride compounds (Si_xH_y), but may also contain N, C, O or metals in the molecular structure. However, to avoid contamination or uncontrolled doping of the final product, pure hydrides are preferred.

Hydrogen in the material passivates dangling bonds and allows the material in some configurations to be liquid at room temperatures. Contrary to hydrocarbons the hydrosilanes react heavily to oxygen. These materials therefore need to be treated in an inert gas ambient such as nitrogen or argon. The compound structures have Si molecular backbones which can be linear (e.g. polydihydrosilane), branched (e.g. polysilane), cyclic (e.g. cyclopentasilane, cyclohexasilane) or even multi-cyclic (e.g. spiro-[4.4]nonasilane).

For compounds with three or more silicon atoms per molecule, the material is liquid at room temperature and can be transformed into solid silicon when a temperature of approximately 300 °C is applied. However, for compounds with less than ten silicon atoms per molecule, the liquid has a boiling point below 300 °C. A direct thermal treatment would therefore evaporate the material before it can transform into solid silicon. The boiling point of the material can be risen by increasing the molecular size. This should however, not come at the cost of liquid coating properties [1].

In a linear structured compound, the viscosity of the liquid is highly dependent on the molecular size. When the liquid consists of small molecules the viscosity is low which is preferable for coating processes but comes at the cost of an increased volatility. On the other hand, viscosity increases for longer molecules that could lead to coating difficulties. Although, high viscosity inks are generally compensated by dissolution in organic solvents, linear silicon hydride molecules are often not soluble in such solvents [1].

In a cyclic structure however, dissolution in an organic solvent is possible. The molecular rings can be opened spontaneously, thermally and photochemically, to create polysilane chains which in turn can dissolve in the original cyclic molecule mixture. The wetting properties and therefore coating can in this way be adjusted and optimized.

In various works[1–3], a ring-molecule of five silicon atoms and ten hydrogen atoms (Si_5H_{10}), cyclopentasilane (CPS), has been chosen because of its relative stability compared to silicon hydrides with similar molecular weights, and ability to ring-open polymerize. The material has been used both in its pure form[3] as well as in a solution of partially cured CPS dissolved in an organic solvent [1, 2].

Besides CPS, other materials have been investigated for solution-based processes of silicon. Molecular weights of these alternatives and the transformation process to solid a-Si are similar to CPS. The molecular structures of CPS and its alternatives are shown in Fig. 2.1 a.

One such alternative is cyclohexasilane (CHS)[4, 5], a ring-molecule that consists of six silicon atoms instead of five, with 12 hydrogen atoms (Si_6H_{12})(shown in Fig. 2.1 b). Similar to cyclopentasilane, this material could also be cured with UV and dissolved in an organic solvent and could be thermally annealed to create solid a-Si. As a result, devices such as diodes have been created using this material[5].

Another alternative is neopentasilane (NPS). A molecule that also has 5 Si atoms, but instead of being connected in a ring, one Si atom is positioned in the center and connected to 4 other silicon atoms (shown in Fig. 2.1 c). Each of these outer Si atoms are then connected to 3 hydrogen atoms (Si_5H_{12}). The advantage of this material is that the molecule has a better solubility in organic solvents due to its branched silicon structure that act as spacers. There are also material synthesis advantages that lead to lower production costs. NPS has been used to create solar cells that have reached efficiencies of 3.5%.[6, 7]

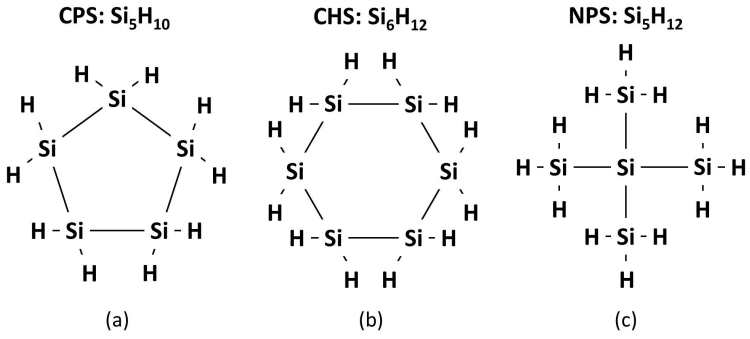

Figure 2.1: Three different types of liquid silicon inks used for solution-processed silicon electronics purposes: cyclopentasilane (a), cyclohexasilane (b), neopentasilane (c).

2.2. MATERIAL PROPERTIES OF CPS

Cyclopentasilane (CPS) is the material of choice in this work. It is an optically transparent liquid at room temperature which allows coating on various substrates. With a bandgap of 6.5 eV the material is insulating, although curing and annealing treatments can induce a transformation to solid amorphous silicon with a bandgap of around 2 eV. This material can subsequently be crystallized to form poly-Si to further improve its electrical performance.

The molecule can assume many different structural conformations, three of which are the most stable and prominent: Envelope (C_s), Twist (C_2), and Planar (D_{5h}) structures. The structures are shown in Figure 2.2. The twist and envelope structures are the most stable, the energies differ less than 0.03 meV. Therefore, only a small distortion is necessary for one to transform into the other. The planar structure is less stable with 50 meV higher in energy compared to the other two. These structures play a key role in the transformation process to solid silicon [8–10].

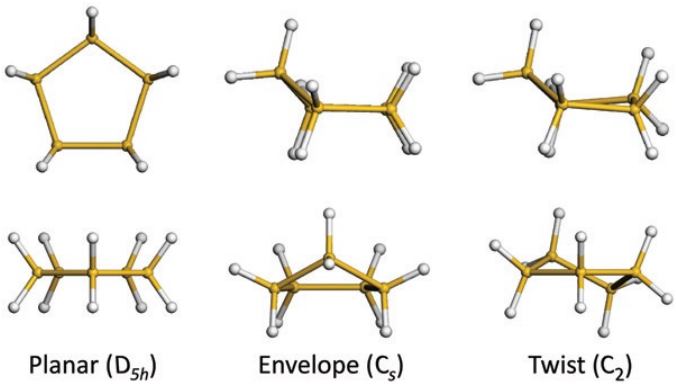

Figure 2.2: Molecular states of CPS, from [9].

With a melting point (MP) of -10.5 °C and a boiling point (BP) of 194.3 °C the material is considered relatively stable; both values are higher than silanes with comparable molecular mass (e.g. MP of -72.8 °C and BP of 153.2 °C for n-pentasilane). This is because of the relatively strong intermolecular interaction between CPS molecules. A bonding similar to hydrogen bonds are formed which play a key role in the CPS reactions. This particularly strong interaction is found where a Si-H bond of one molecule is attracted to the center of the CPS ring of a neighboring molecule [11].

Although the relative stability allows for a good coating of the material, a direct transformation is difficult to achieve since the thermal decomposition temperature lies around 300 to 350 °C. An intermediate ring-open polymerization step is therefore required, al-

though this changes the wetting properties of the ink. An optimization can be made by dissolution in an organic solvent such as toluene or cyclooctane, commonly used in other works [1, 2].

The liquid silicon ink is generally used to create intrinsic solid silicon. Doping of the ink however, is also possible. This is done by mixing the liquid with decaborane ($B_{10}H_{14}$) for p-type doping, and white phosphorus (P_4) for n-type doping [12]. Solar cells have been fabricated using this liquid silicon doping method.[13, 14]

2.3. TRANSFORMATION FROM CPS TO SOLID SILICON

The process of transforming CPS to solid silicon is visually explained in Fig. 2.3. The CPS ring-molecule opens after treatment with UV light and connects to other similarly ring-opened molecules. An incomplete curing process results in the formation of a colorless, viscous, polysilane-CPS gel. This gel can be mixed with an organic solvent to reduce the viscosity and improve the coating process. In this state the material still behaves as a porous insulator. A final annealing step of at least 350 °C allows a strong cross-linking of the polysilane chains, transforming the insulator into the a-Si semiconductor.

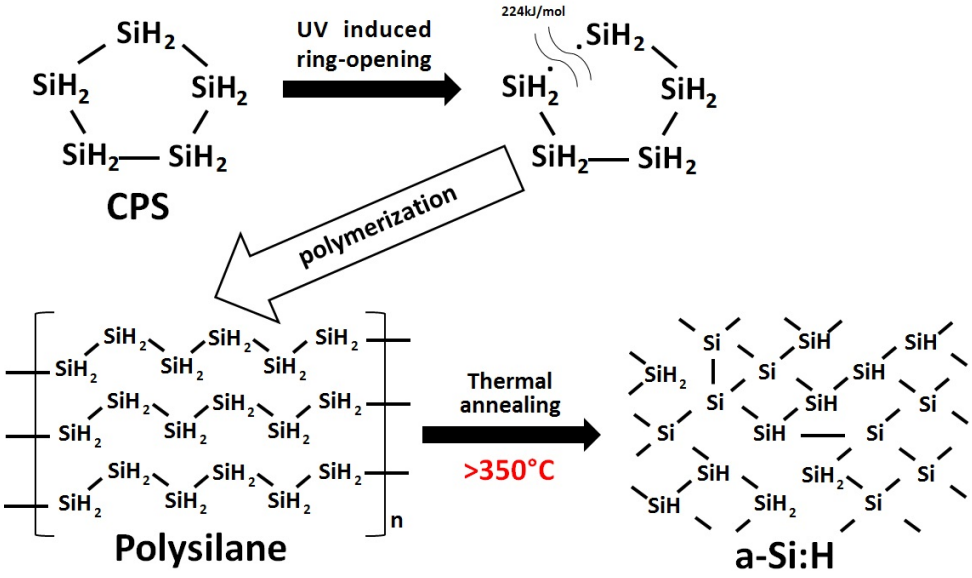

Figure 2.3: Transformation process from CPS to a-Si:H.

2.3.1. CPS RING-OPEN POLYMERIZATION

Polymerization of CPS can be enforced by a thermal or UV treatment. Ring-opening occurs when the out-of-plane silicon atom in the envelope structure of the CPS molecule is strongly distorting until molecular cleavage takes place. A ring-opened formation of the CPS molecule with a Si-H-Si bridge-bond was found to play a key role in this polymerization process [9]. This ring-opened CPS can connect to other ring-opened molecules to form longer polysilane chains.

Although UV treatments of CPS were found to be effective for polymerization, the absorption spectrum of freshly synthesized CPS revealed not only a transparency to optical wavelengths, but also to the UV light down to approximately 300 nm [15]. In many works related to solution-based silicon processing however, it was stated that CPS is photopolymerized using UV light with a wavelength of 360 nm or higher [1–3]. This misconception comes from the spontaneous ring-opening of CPS molecules at room temperature. Since polysilane does absorb UV light below 400 nm, a clear distinction was observed in the rate of polymerization when comparing the CPS immediately after synthesis, to CPS stored for a predefined time at room temperature. The measurement results of the absorption is shown in Fig. 2.4.

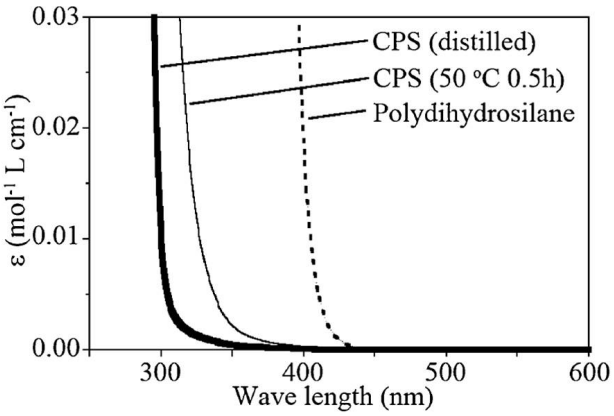

Figure 2.4: Absorption spectra of freshly synthesized CPS, CPS under accelerated aging at 50 °C for half an hour, and polysilane [15].

One theory behind this photopolymerization process is that the polysilane molecules inside the CPS mixture absorb the UV light, and transfer the energy to CPS molecules which subsequently ring-open [15]. A more detailed analysis is required to confirm this theory. In this work, when the curing of CPS is mentioned, the used material is not freshly synthesized, and polysilane molecules exist inside the liquid silicon ink.

For polysilane, it was observed that light which can deliver sufficient energy (wavelength ≤ 540 nm) is needed to break Si-Si bonds (2.3 eV). Higher photon energies (≤ 376 nm) are then necessary to break Si-H bonds (3.3 eV) [1, 12]. Cross-linking can only result where Si-H bonds are broken.

The structural result of UV photopolymerized CPS has been analyzed in other works [16] by means of size-exclusion chromatography (SEC), multi-angle laser light scattering (MALLS), and viscometry. In these experiments CPS samples were treated with a 365 nm wavelength UV source with an intensity of 1 mW/cm^2. Different irradiation times were used to see its effect on the polysilane structure. Fig. 2.5 shows the differential weight fraction to the molar mass from the SEC-MALLS measurements. For 0 minutes, the molar mass of the CPS molecules is obtained as a curve with a sharp peak at 150 g/mol. The molecular weight distribution spreads and increases after UV exposure. A large distribution from 10^2 to 10^6 g/mol is visible for samples exposed to at least 60 minutes of UV light.

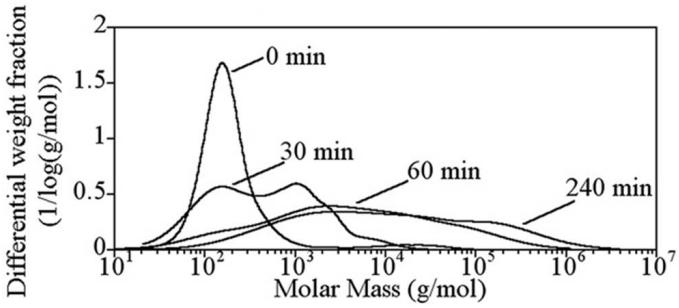

Figure 2.5: Results from SEC-MALLS measurements, plotting differential weight fraction against the molar mass of CPS samples cured with UV light for 0, 30, 60, and 240 minutes [16].

Besides the molecular weight distribution, from the calculations using viscosity, radius of gyration and molar mass, the structure of polysilane was extracted and supported by Proton Nuclear Magnetic Resonance (^{1}H NMR) and Fourier Transform Infrared Spectroscopy (FTIR) measurements [16]. The polysilane structure was found not be in a straight chain configuration. Rather the molecules are branching for every 4.1 to 4.5 monomers of SiH_2. The overall polysilane structure is particle-like and compact.

2.3.2. LIQUID SILICON PYROLYSIS

A strong cross-linking of polysilane is necessary for the formation of a 3D silicon network, which is generally obtained by an annealing treatment. Si-Si bonds break at temperatures below 280 °C, and at approximately 300 °C, Si-H bonds break[1, 12].

An analysis of the structure has been made for various annealing temperatures[17]. A gradual color change from colorless to yellow, to brown has been observed as the temperatures were increased (see Fig. 2.6). This color change was associated to the bandgap narrowing of the cross-linked polysilane material from 6.5 eV to 1.64 eV for materials annealed at 360 °C.

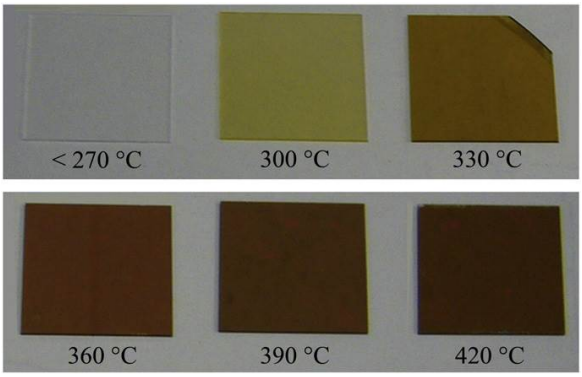

Figure 2.6: Optical images of liquid silicon samples annealed at different temperatures [17].

Differential thermal gravimetry (DTG) measurements showed a significant weight loss at 100, 200, and 300 °C that comes from the evaporation of organic solvent, CPS and SiH_x radicals, respectively. A total weight loss of approximately 58% was observed by thermal gravimetry (TG) for annealing temperatures above 350 °C. Differential thermal analysis (DTA) revealed a broad exothermal peak with a maximum at 320 °C from the polysilane bond breaking and cross-linking. The measurement results are shown in Fig. 2.7. From this, it was concluded that the a-Si transformation was particularly active between 300 and 360 °C.

The thermal annealing process brings a risk of introducing stresses inside the film. This stress is proportional to the thickness of the film and comes from the sol-gel nature of the liquid silicon ink. During the heating process of polysilane, while many of the longer chains start to cross-link, molecules with a much lower weight, can evaporate and leave voids behind. This heavy weight loss was confirmed by the TG and DTG measurements of [17]. The final film will therefore be porous and exhibit a lot of stress. This stress may become so severe that it would result in cracking of the film [18]. Since, thicker films exhibit more stress, a critical thickness can be found above which the film cracks. This thickness is dependent on the curing treatment of the ink, as well as the employed annealing temperature. To overcome this issue, for the fabrication of thicker films, multilayer deposition has been explored by some groups [19].

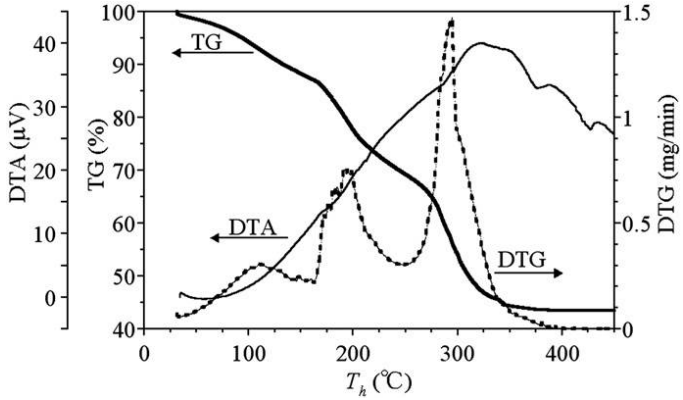

Figure 2.7: TG, DTA, and DTG measurement results for various thermal annealing temperatures of liquid silicon [17].

Once annealed at temperatures around 360 °C, the material is stable and can be taken out of the inert environment and be treated as solid a-Si:H. Optionally, the annealing temperature could further be increased to 550 or 600 °C to significantly reduce the hydrogen content and increase the density[2]. Small crystalline fractions can also start to form at these temperatures as a result of solid phase transformation. The annealed material could be crystallized with an excimer laser treatment, which is a common method for the transformation from a-Si to poly-Si thin films.

2.4. LIQUID SILICON TFT PROCESSES SO FAR

In this section, three papers are discussed that have applied solution-based silicon processes using CPS in the TFT fabrication. These applications demonstrate the potential of solution-based silicon devices and their shortcomings.

2.4.1. FIRST LIQUID SILICON TFTS

In 2006, the group led by Prof. Shimoda, published their work on solution-processed silicon devices [1]. It was the first time that a material could be used in a solution-based synthesis of silicon thin films for TFTs. The work was published in Nature, and has gained widespread attention.

In their work, the silicon ink that was used was not pure CPS but a mixture of CPS, polysilane and toluene. This combination allowed the control of wetting properties of the final ink before the solution was coated on a substrate, as explained in section 2.2.

After liquid deposition, the film was thermally annealed at 540 °C to sufficiently cross-link the silicon film and reduce the amount of hydrogen. This hydrogen removal is beneficial for the following excimer laser crystallization to minimize ablation. A simplified process flow with temperatures from CPS to poly-Si TFT is displayed in Fig. 2.8.

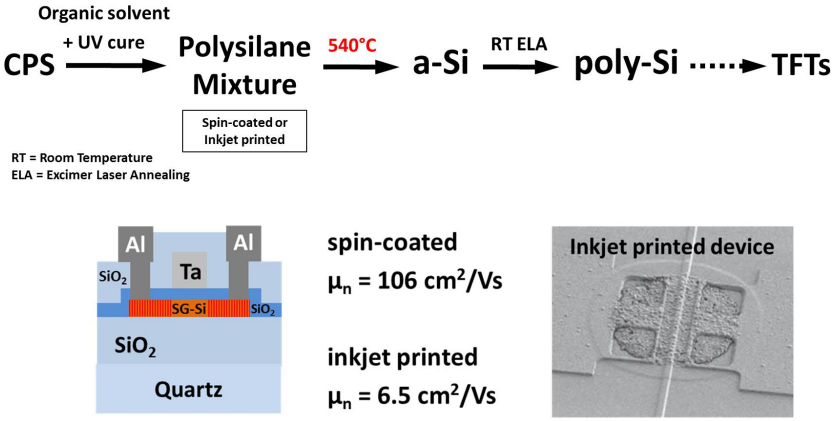

Figure 2.8: Process flow of the first liquid Si TFTs from CPS to poly-Si.

A spin-coated TFT was demonstrated in this work with an electron mobility of 108 cm^2/Vs, one that is as high as conventional CVD-based poly-Si TFTs. In addition, to demonstrate the printability of this material, inkjet printed liquid silicon TFTs were created that possessed a mobility of 6.5 cm^2/Vs. This lower mobility was attributed to the high roughness, incomplete crystallization, and high thickness among others.

This work has demonstrated the first case where a silicon precursor could be used in a solution-processed polycrystalline silicon device. Mobilities similar to CVD poly-Si TFTs could be achieved and these outperform current organic TFTs that are commonly used in solution based processes.

2.4.2. SINGLE GRAIN LIQUID SILICON TFTS ON A SILICON SUBSTRATE

Polycrystalline silicon devices generally are limited in their mobilities due to the presence of randomly distributed grain boundaries. Within the polycrystalline channel of a transistor, many small (nanometer sized) neighboring grains are present that collide with each other during the crystallization process. The boundaries that are formed between the individual grains limit the current flow. However, if a single large (micrometer sized) grain can be isolated or filtered out during crystallization, and if its location and growth is controlled, high mobility devices (several hundred cm^2/Vs)can be created by placing the channel of the transistor inside such a large grain, thereby avoiding grain

boundaries. This has been done in numerous studies by Ishihara et al.[20–22] and is known as the μ-Czochralski (μ-Cz) process. Recently, this process has been applied to liquid silicon[2].

Funnels of 100 nm in diameter were created inside an oxide layer. These funnels are subsequently filled with silicon by spin-coating the CPS-polysilane-solvent mixture. The film is then annealed at 430 °C for 1 hour resulting in a-Si:H. A dehydrogenation pre-treatment is used to reduce the hydrogen content and densify the film by thermal annealing at 650 °C for 2 hours. This higher dehydrogenation temperature compared to the previous work is needed to be able to expose the silicon to higher laser energy densities.

In the μ-Cz process, the a-Si film is molten by excimer laser annealing, until a seed is left at the bottom of the aforementioned funnel. During the subsequent cooling and crystallization process a single grain is filtered out and grows laterally on top of the funnel until its boundaries touch the opposite advancing boundaries of adjacent grains. This crystallization process improves when the cooling process is slowed down and therefore the excimer laser annealing treatment was performed at an elevated temperature of 450 °C. A simplified process flow with process temperatures from CPS to poly-Si TFT is displayed in Fig. 2.9.

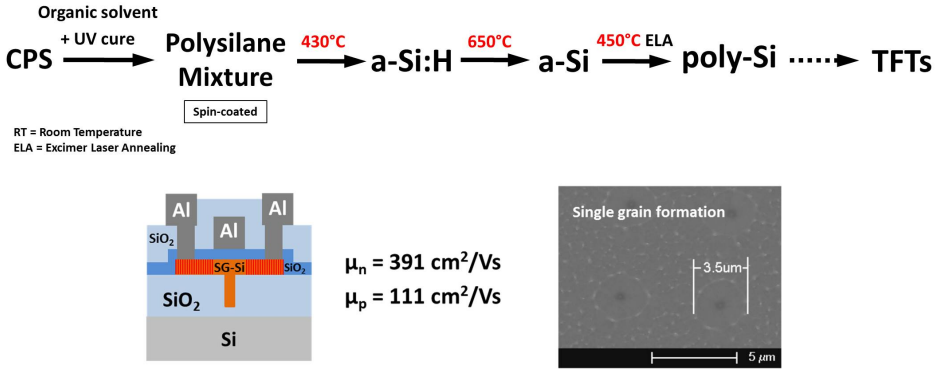

Figure 2.9: Process flow of the first SG-Si TFTs from CPS to poly-Si.

Using this process a single-grain Si TFT is created by spin-coated solution-processed CPS as the precursor. The devices fabricated in this work achieved mobilities of 391 cm^2/Vs and 111 cm^2/Vs for NMOS and PMOS devices respectively, significantly surpassing the level of standard LTPS devices (~ 100 cm^2/Vs).

2.4.3. SINGLE GRAIN LIQUID SILICON TFTS ON A POLYIMIDE SUBSTRATE

Section 2.4.2 presented a process of constructing high mobility silicon devices using a liquid Si-based precursor. The temperatures used in the process were however too high for polymer substrates that generally have a low thermal budget. Fabricating devices directly on plastic foils allows flexible device applications, as well as roll-to-roll processing. One of the polymers that have a relatively high glass transition temperature is polyimide (generally > 350 °C)[23].

In the work by Zhang et al.[3], the high-mobility liquid silicon process has been optimized for a maximum fabrication temperature of 350 °C. As the substrate, a polyimide (Durimide 115A) has been coated on top of a silicon wafer which has a glass transition temperature of 371 °C. PECVD TEOS oxide was formed on top of this film to create grain filter funnels for the µ-Czochralski process.

Pure CPS is coated on the substrate by means of a doctor blade as a roll-to-roll compatible coating method. This CPS film was subsequently cured under UV light and and annealed at 350 °C to form a hydrogenated a-Si film. Before crystallizing the film, the hydrogen content was reduced using low fluence excimer laser pulses at room temperature. A simplified process flow with process temperatures from CPS to poly-Si TFT is displayed in Fig. 2.10.

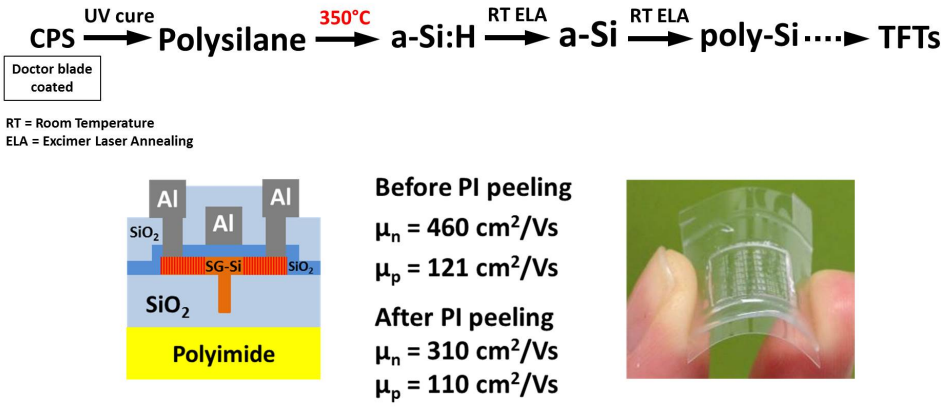

Figure 2.10: Process flow of the first SG-Si TFTs from CPS on polyimide.

The final TFTs on top of polyimide achieved mobilities of 460 and 121 cm^2/Vs for the NMOS and PMOS devices respectively. The polyimide film has then been etched away and the free-standing devices were transferred to a PEN substrate to enable full flexibility. The transferred TFTs had a reduced mobility of 310 and 110 cm^2/Vs for NMOS and PMOS devices respectively, due to transfer induced stresses.

Although this work presented a transfer of solution-processed silicon devices to a flexible substrate, the total fabrication process of the devices were conducted on top of a polyimide film which was left in tact. This work showed, for the first time, solution-processed silicon devices directly fabricated on a polymer substrate.

2.5. OPPORTUNITIES IN LIQUID SILICON RESEARCH

High mobilities and fully flexible TFTs were fabricated in [3], which show the potential of the liquid silicon material. The usage of plastic substrates however, is strongly limited by the relatively high temperature annealing of 350 °C. Low-cost plastic foils such as PET, PEN or paper that have a thermal budget of approximately 120, 150 and 130 °C respectively [23]. Truly low-cost, flexible Si TFT fabrication is therefore still not achieved with the latest processing methods.

An observation had been made[17], where simply reducing the annealing temperature leads to unstable silicon films. Adding energy to the system by an alternative route, one which avoids using the thermal annealing step, should be researched. Since the liquid silicon reacts to UV light, an investigation has to be made in this treatment. A difference in intensity for instance could cause a change in cross-linking reaction that could stabilize the material as a whole. Ideally a crystallization in the same process could make the intermediate transformation to amorphous silicon obsolete. This process is illustrated in Fig. 2.11.

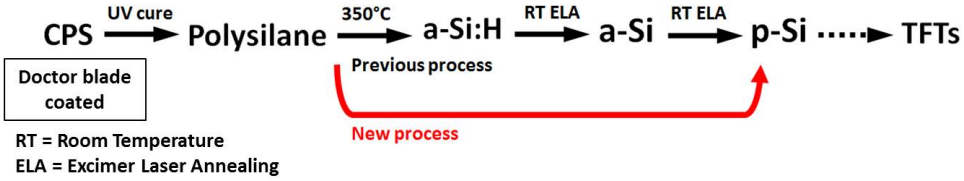

Figure 2.11: Proposed process flow of the direct transformation from polysilane to poly-Si.

By finding this low temperature alternative process, new application areas where high performance and low-cost are required can be attained. This was formerly impossible or impractical with rigid silicon devices, or organic/metal-oxide devices. This technology will combine the high performance of silicon with the low-cost of flexible and printable electronics.

2.6. CONCLUSIONS

For solution-processing of silicon devices, silicon hydride precursors have been investigated. Among the various types, cyclopentasilane is found to be a strong candidate with good stability and high photoreactivity. Alternatives to CPS have also been discussed and these include cyclohexasilane, and neopentasilane.

The material can be coated as a liquid, cured with UV to polysilane, and finally thermally annealed to create a-Si:H. Liquid properties of the material can be adjusted by partially curing the CPS and mixing it with an organic solvent prior to deposition.

Ring-opening of the CPS molecules can occur spontaneously at room temperature, or enforced by UV light or thermal treatment. Research suggests that spontaneously ring-opened CPS molecules absorb UV light and transfer the energy to unreacted CPS. Ring-opened polysilane molecules may connect to other similarly reacted molecules to form longer chains. A large weight distribution of different sized polysilanes inside the liquid silicon ink is the result.

The polysilane chains will increase their cross-linking as a result of a thermal treatment. However, only from approximately a temperature of 350 °C the transformation to a-Si is stable. Therefore, when aiming for a lower temperature process, an alternative route to delivering the energy for a stable transformation is necessary.

After the formation of a-Si:H, a dehydrogenation and an excimer laser crystallization step can transform the material into polycrystalline silicon. This material, synthesized from CPS, has been used to create TFTs in various works. The first devices have shown limited charge carrier mobilities as a result of random grain boundaries.

High mobility devices have been achieved using liquid silicon ink, by controlling the location of large crystal grains. The channel of the TFT was placed within such a large grain to avoid grain boundary issues. Mobilities of 391 and 111 cm^2/Vs were obtained for the NMOS and PMOS devices respectively.

Finally, flexible devices were created by processing liquid silicon on top of a polyimide substrate, limiting the fabrication temperature to 350 °C. Controlling the location of crystal grains have led to a mobility of 460 and 121 cm^2/Vs for NMOS and PMOS devices respectively.

The annealing temperature of at least 350 °C makes the material unsuitable for low-thermal budget substrates such as PET, PEN or paper. A method therefore needs to be developed that could avoid this relatively high temperature process. Opportunities have been found in the photoreactive process that is used in the curing of CPS. Ideally a direct crystallization from polysilane to poly-Si is desired, thereby omitting an intermediate a-Si transformation step.

REFERENCES

[1] T. Shimoda, Y. Matsuki, M. Furusawa, T. Aoki, I. Yudasaka, H. Tanaka, H. Iwasawa, D. Wang, M. Miyasaka, and Y. Takeuchi, *Solution-processed silicon films and transistors,* Nature **440**, 783 (2006).

[2] J. Zhang, R. Ishihara, H. Tagagishi, R. Kawajiri, T. Shimoda, and C. Beenakker, *Single-grain si tfts using spin-coated liquid-silicon,* in *Electron Devices Meeting (IEDM), 2011 IEEE International* (IEEE, 2011) pp. 14–5.

[3] J. Zhang, M. Trifunovic, M. Van Der Zwan, H. Takagishi, R. Kawajiri, T. Shimoda, C. Beenakker, and R. Ishihara, *Single-grain si thin-film transistors on flexible polyimide substrate fabricated from doctor-blade coated liquid-si,* Applied Physics Letters **102**, 243502 (2013).

[4] G. R. Iyer, E. K. Hobbie, S. Guruvenket, J. M. Hoey, K. J. Anderson, J. Lovaasen, C. Gette, D. L. Schulz, O. F. Swenson, A. Elangovan, *et al.*, *Solution-based synthesis of crystalline silicon from liquid silane through laser and chemical annealing,* ACS applied materials & interfaces **4**, 2680 (2012).

[5] S. Han, X. Dai, P. Loy, J. Lovaasen, J. Huether, J. M. Hoey, A. Wagner, J. Sandstrom, D. Bunzow, O. F. Swenson, *et al.*, *Printed silicon as diode and fet materials–preliminary results,* Journal of Non-Crystalline Solids **354**, 2623 (2008).

[6] T. Bronger, P. H. Wöbkenberg, J. Wördenweber, S. Muthmann, U. W. Paetzold, V. Smirnov, S. Traut, Ü. Dagkaldiran, S. Wieber, M. Cölle, *et al.*, *Solution-based silicon in thin-film solar cells,* Advanced energy materials **4** (2014).

[7] T. Sontheimer, D. Amkreutz, K. Schulz, P. H. Wöbkenberg, C. Guenther, V. Bakumov, J. Erz, C. Mader, S. Traut, F. Ruske, *et al.*, *Solution-processed crystalline silicon thin-film solar cells,* Advanced Materials Interfaces **1** (2014).

[8] P. V. Dung, P. T. Lam, N. D. Duc, A. Sugiyama, T. Shimoda, and D. H. Chi, *First-principles study of the thermally induced polymerization of cyclopentasilane,* Computational Materials Science **49**, S21 (2010).

[9] A. Sugiyama, T. Shimoda, and D. H. Chi, *Ab initio study of the polymerisation of cyclopentasilane,* Molecular Physics **108**, 1649 (2010).

[10] V. S. Mastryukov, M. Hofmann, and H. F. Schaefer, *Structure and conformations of cyclopentasilane, si5h10,* The Journal of Physical Chemistry A **103**, 5581 (1999).

[11] P. T. Lam, A. Sugiyama, T. Masuda, T. Shimoda, N. Otsuka, and D. H. Chi, *Ab-initio study of intermolecular interaction and structure of liquid cyclopentasilane,* Chemical Physics **400**, 59 (2012).

[12] H. Tanaka, H. Iwasawa, D. Wang, N. Toyoda, T. Aoki, I. Yudasaka, Y. Matsuki, T. Shimoda, and M. Furusawa, *Spin-on n-type silicon films using phosphorous-doped polysilanes,* Japanese Journal of Applied Physics **46**, L886 (2007).

[13] T. Masuda, N. Sotani, H. Hamada, Y. Matsuki, and T. Shimoda, *Fabrication of solution-processed hydrogenated amorphous silicon single-junction solar cells,* Applied Physics Letters **100**, 253908 (2012).

[14] T. Masuda, H. Takagishi, Z. Shen, K. Ohdaira, and T. Shimoda, *Phosphorus-and boron-doped hydrogenated amorphous silicon films prepared using vaporized liquid cyclopentasilane,* Thin Solid Films (2015).

[15] T. Shimoda and T. Masuda, *Liquid silicon and its application in electronics,* Japanese Journal of Applied Physics **53**, 02BA01 (2014).

[16] T. Masuda, Y. Matsuki, and T. Shimoda, *Characterization of polydihydrosilane by sec-malls and viscometry,* Polymer **53**, 2973 (2012).

[17] T. Masuda, Y. Matsuki, and T. Shimoda, *Pyrolytic transformation from polydihydrosilane to hydrogenated amorphous silicon film,* Thin Solid Films **520**, 6603 (2012).

[18] T. J. Garino, *The cracking of sol-gel films during drying,* in *MRS Proceedings*, Vol. 180 (Cambridge Univ Press, 1990) p. 497.

[19] D. Mitzi, *Solution processing of inorganic materials* (John Wiley & Sons, 2008).

[20] R. Ishihara and M. Matsumura, *Excimer-laser-produced single-crystal silicon thin-film transistors,* Japanese journal of applied physics **36**, 6167 (1997).

[21] R. Ishihara, P. C. van der Wilt, B. D. van Dijk, A. Burtsev, F. Voogt, G. Bertens, J. Metselaar, and C. Beenakker, *Advanced excimer laser crystallization techniques of si thin film for location control of large grain on glass,* in *Photonics West 2001-Electronic Imaging* (International Society for Optics and Photonics, 2001) pp. 14–23.

[22] R. Ishihara, J. Zhang, M. Trifunovic, J. Derakhshandeh, N. Golshani, D. M. T. Mofrad, C. Tao, K. Beenakker, and T. Shimoda, *Single-grain si thin-film transistors for monolithic 3d-ics and flexible electronics,* IEICE Transactions on Electronics **97**, 227 (2014).

[23] Goodfellow, *Alphabetic list of materials,* online (2016).

3

Low Temperature Liquid Silicon Process Development

In the previous chapter, the properties of cyclopentasilane and the methods for using this ink for electronic purposes were described. An opportunity is found in assessing an alternative way of silicon transformation without damaging temperature sensitive substrates. This chapter further analyses the UV curing process, and presents the development of an alternative transformation method through experimentation. This new method involves the excimer laser by which polysilane can directly transform into poly-Si. Properties of the silicon produced using this method are also presented.

In section 3.1, the equipment necessary for handling liquid silicon as well as the tools used for characterizing the solid silicon are firstly presented. In section 3.2, the effects of different UV light intensities in the curing process is explained. Treatment of cured and uncured CPS films using an excimer laser is demonstrated in section 3.3. A detailed analysis of the crystallization experiments of highly cured polysilane is discussed in section 3.4. Finally, the obtained results by this newly developed method is concluded in section 3.5.

3.1. Liquid Silicon Handling and Characterization Tools

A number of key tools are necessary for handling the highly reactive liquid silicon. In addition, characterizing the obtained results from various transformation processes are essential. The tools are presented in this section.

3.1.1. Liquid Silicon Handling

Glovebox

In this work, a contained inert ambient was used for handling the highly reactive CPS. A nitrogen gas filled glovebox (MBraun) is used, equipped with a gas purification system (MB200G) which maintains the oxygen and water vapor levels inside this space below 0.1 parts per million. This tool allows the handling of liquid silicon until it is transformed into a stable solid silicon. An image of the glovebox is shown in Fig. 3.1.

Figure 3.1: Image of the glovebox used for liquid silicon processing. *Image courtesy of Salm en Kipp B.V.*

Inside the glovebox, the liquid is coated either on a glass (Corning®, Eagle XG) substrate or a silicon substrate with PECVD TEOS SiO_2 deposited on top. The glass substrate is used for the Raman spectroscopy analysis of the silicon film. Since, the sample signal would be overwhelmed by the background signal from a Si wafer substrate. The silicon wafer with the oxide buffer interlayer is used for the device fabrication process. This substrate is also used for scanning electron microscope (SEM) characterization due to the limited charging effects.

DOCTOR BLADE COATING

In the semiconductor industry, coating of liquids on a substrate is generally performed by means of spin-coating. In such a process the liquid is dispensed in the middle of a substrate, after which it is spun at high speeds allowing the liquid to spread uniformly throughout the substrate surface. This method however leads to a lot of material waste and moreover, it cannot be scaled up to roll-to-roll processes.

A method for coating liquids that does produce minimal material waste and is scalable to roll-to-roll processes, is doctor blade coating [1]. In such a process, the liquid is dispensed onto a substrate and spread by means of material displacement by a physical blade.

Since the coating process in this work is conducted manually, the blade has to meet specific requirements. When the blade is too stiff, any variations coming from the random hand motion will directly affect the film uniformity. A highly flexible blade however, does not allow an accurate control of the liquid coating process. A custom made blade is used which balances the stiffness by bending and taping a polyimide (Kapton®) sheet onto a polypropylene base. This blade and a sample result of the blading process are shown in Fig. 3.2.

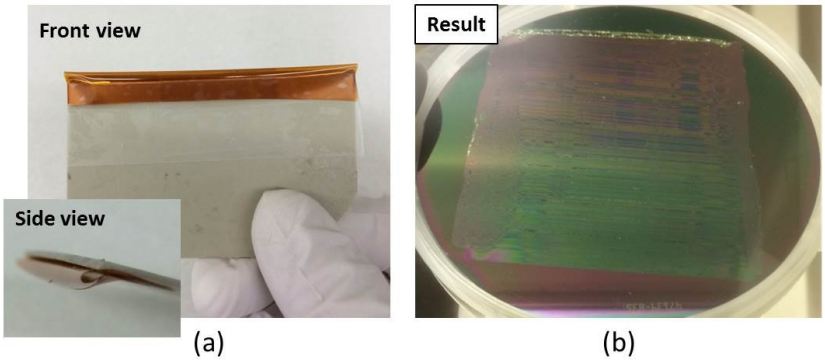

Figure 3.2: Two images of the doctor blade used in this work from the front and side (a) perspectives, and a coated sample using such a blade (b).

UV PHOTOPOLYMERIZATION

After coating of the cyclopentasilane, a curing treatment is used for the photopolymerization process. Two UV light sources have been tested and their results are presented in section 3.2. The first UV source is the UV AHAND GS with an intensity of approximately 10 mW/cm^2. The lamp is mercury based which leads to heating of the film during UV exposure to approximately 80 °C. Similar intensities have also been used in other works

[2, 3]. The second UV source is the Loctite LED Flood UV curing system with an intensity of 300 mW/cm^2. The light source is an array of LEDs and can therefore irradiate without significant heating of the substrate. Fig. 3.3 shows an image of both UV light sources.

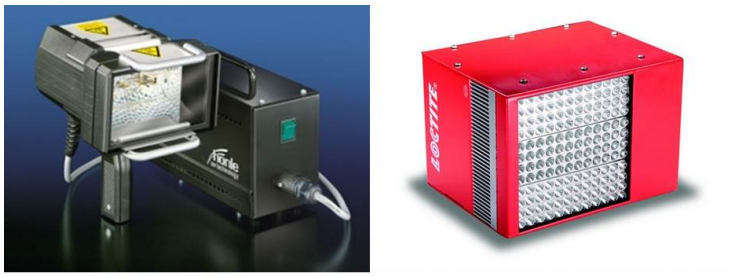

Figure 3.3: Images of the UV AHAND GS (a), and the Loctite LED Flood UV (b).

3.1.2. MATERIAL CHARACTERIZATION

SPECTROPHOTOMETER

The absorption spectrum of polysilane is needed to detect the efficiency of specific wavelengths for light-induced transformations. Absorption has been measured using the Lambda 950 (PerkinElmer) Spectrophotometer, equipped with a total integrating sphere (TIS). The tool measures the transmission and reflectance of a sample over a predefined wavelength range. Polysilane samples have been prepared on top of a quartz substrate (UV-grade / fused silica), that have a transmission of 96% and a reflection of 4%. As a result, measurements mainly apply to the sample material and not the substrate. The absorption coefficient can be approximated by using the following formula:

$$\alpha = -\frac{1}{d}\ln\left(\frac{T}{1-R}\right) \tag{3.1}$$

where α is the absorption coefficient, d the thickness of the measured film, and T and R the measured optical transmittance and reflectance, respectively.

The absorption spectrum can also be used to approximate the optical bandgap of the material by using a Tauc plot [4], for which $(\alpha h\nu)^{1/2}$ is plotted against the photon energy $h\nu$. A linear extrapolation of the curve from the onset of absorption gives the bandgap approximation.

RAMAN SPECTROSCOPY

The most commonly used tool that can detect the crystallinity, porosity and hydrogen content of the silicon material is Raman spectroscopy [5–8]. It is a non-destructive method for analyzing the molecular fingerprint of a material. The working principle lies in the irradiation of a low intensity laser onto a material, and detecting the light that is scattered by the interaction of the light with the molecules or phonons of the material.

Although the majority of the scattered light has the same frequency as the irradiated light due to elastic scattering (Rayleigh scattering), a small fraction of light is scattered with a shift in energy due to inelastic interaction with the lattice (Stokes and Anti-Stokes scattering). This shift in energy can determine both qualitatively as well as quantitatively the vibrational modes of molecular bonds. Filtering out the Rayleigh scattered component from the light, a plot can be made from the detected signal intensity versus the wavenumber (cm^{-1}), which is directly proportional to the energy. The following formula is applied:

$$\Delta\omega = \left(\frac{1}{\lambda_0} - \frac{1}{\lambda_1}\right) \tag{3.2}$$

where $\Delta\omega$ is the Raman shift in wavenumber or cm^{-1}, λ_0 the wavelength of the excited light, and λ_1 the wavelength of the scattered light. Depending on the type of material, its phase, and its crystallinity, specific shifts in scattered energy are found.

Different wavelengths can be used as the light source of this tool. In this work, an Invia Raman Spectrophotometer with a green laser of 514 nm wavelength is used. This wavelength has a penetration depth of 100 nm in a-Si:H, and 300 nm in µc-Si:H. For longer wavelength light sources, the penetration depth may reach 1 µm [6]. Typical thicknesses used in this work are ranging from 50 to 400 nm.

For the crystallinity of Si, the frequency shifts between wavenumbers 100 to 1000 $cm^{-1}$are analyzed. Table 3.1 shows a list of Si Raman signal peaks and their associated vibrational modes.[5] Using this table and the measured Raman spectra, a structural analysis can be made of the silicon material.

Specific spectra are known for both the amorphous and crystalline silicon phase, as shown in Fig. 3.4. For amorphous silicon a broad peak at 480 cm^{-1} of Si-Si TO mode is found surrounded by smaller peaks, whereas for c-Si a sharp peak of this mode at 520 cm^{-1} is observed.

The selection rules preserving the conservation of energy and momentum during Raman scattering are strictly observed. It results that the only phonons allowed to interact with incident photons must have no momentum. As a consequence the c-Si Raman shifts are sharp Lorentzian curves. On the contrary, in a-Si the short range lattice order

Table 3.1: Vibrational modes for silicon lattice and their respective wavenumber.

Wavenumber (cm^{-1})	Bond	Vibrational mode
150	Si-Si	transverse acoustic (TA) mode
300	Si-Si	2-phonon transverse acoustic (2TA) mode (c-Si)
308	Si-Si	longitudinal acoustic (LA) mode
380	Si-Si	longitudinal optical (LO) mode
480	Si-Si	transverse optical (TO) mode
510	Si-Si	shifted transverse optical(TO) mode/ Defective crystalline component (c-Si)
520	Si-Si	transverse optical (TO) mode (c-Si)
630	Si-H	bending mode
	$Si-H_2$	rocking mode
880	$Si-H_2$	bending/scissoring mode
907	$Si-H_3$	degenerate deformation
960	Si-Si	2-phonon transverse optical (2TO) mode (c-Si)
2000	Si-H	stretching mode
2090	$Si-H_2$/$Si-H_3$	stretching mode

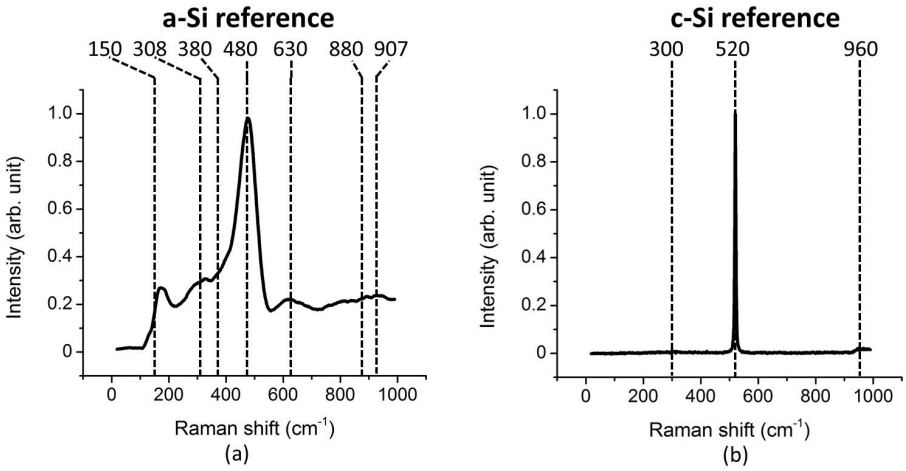

Figure 3.4: Sample Raman spectra of a-Si (a), and p-Si (b).

leads to a relaxation of these rules and phonons with momentum around zero are also involved in the Raman scattering. It follows that the signals from a-Si are much broader peaks. The FWHM is an indicator of the order range (other than strain). A mixed phase system shows therefore a superposition of the two Raman spectra. As a result, a partially crystalline structure results in both a peak at 520 cm^{-1} as well as the collection of peaks

found for a-Si. The Raman crystallinity fraction of such materials can be calculated by:

$$\phi_c = \frac{A_{520} + A_{510}}{A_{520} + A_{510} + A_{480}} \tag{3.3}$$

where A_i is the area under the curve centered at i, and ϕ_c is considered the lower limit of the actual crystalline volume fraction. The peak at 510 cm^{-1}, arises from the deconvolution of the tail of the crystalline fraction at 520 cm^{-1} and is associated to the defective crystalline phase of the material, which comes from grain boundaries of nanometer sized grains. [6]

Using the Raman spectra, besides the material crystallinity, peaks at different wavenumbers can be used to calculate additional properties such as hydrogen content and porosity. The hydrogen content can be estimated by using the following formulas:

$$\frac{I_{Si-H}}{I_{Si-Si}} = \frac{a}{2 - a/2} \cdot \frac{\sigma_{Si-H}}{\sigma_{Si-Si}} \tag{3.4}$$

$$\frac{N_{Si-H}}{N_{Si-Si}} = \frac{a}{2 - a/2} \tag{3.5}$$

where I_{Si-H} and I_{Si-Si} are intensities of the Si-H related peak at 2100 cm^{-1} and the Si peak at the 480 cm^{-1}, respectively, a the number of hydrogen atoms per silicon atom, σ_{Si-H} and σ_{Si-Si} the cross-sections of the respective bond types. This ratio indicates how much more likely one signal is to occur compared to the other. A ratio of 0.37 has been used, similar to Vora and Solin[7]. N is the number of bonds specific for Si-H and Si-Si. This ratio gives an approximation of the hydrogen content inside the film as an atomic percentage.

The porosity is calculated as the ratio of the following peak areas:

$$R = \frac{A_{2090}}{A_{2000} + A_{2090}} \tag{3.6}$$

where A_{2000} and A_{2090} are the areas under the respective peaks after baseline subtraction. The peaks at around 2090 cm^{-1} are associated to the $Si\text{-}H_2$/$Si\text{-}H_3$ bonds on the external and internal void surfaces. The peak at 2000 cm^{-1} is associated to the bulk vibrations of Si-H. In this way the ratio reveals the microstructure factor R or porosity [8].

MORPHOLOGY CHARACTERIZATION

Although the surface of the silicon samples can be observed by optical microscopy, generally this is not sufficient to analyze the sub-micrometer changes in morphology of the material.

Scanning electron microscopy (SEM) is used to more accurately analyze the surface topology of crystallized silicon materials. In this tool, a beam of electrons is scanned over a sample, and interacts with the sample atoms. These emit and scatter secondary electrons that are collected to form an image [9].

For more in depth insight as a result of the crystallization, the grain location, distribution, and grain sizes need to be analyzed. This is done by observing the cross-section of a crystallized film by transmission electron microscopy (TEM) [10]. This tool emits a beam of electrons that are transmitted through a material. De Broglie's principle is used which states that every subatomic particle has a wavelength due to its quantistic nature. The electrons have small wavelength which translates to high energies and therefore high resolution. A resolution of 1000 times the maximum resolution of the SEM can be achieved.

3.2. HIGH INTENSITY UV CURING

The transformation from CPS to a-Si involves the photopolymerization of the molecules and a cross-linking process. A decrease in thermal annealing temperatures below 350°C leads to an unstable film, because of the limited cross-linking between the polysilane chains, as explained in chapter 2. Cross-linking however, can also be triggered by the photochemical cleavage of Si-H bonds. Therefore, an investigation has been made on the possibility of efficiently replacing the thermal annealing step with a more intense UV curing treatment.

The effects of UV (365 nm) sources of different intensities have been analyzed. A comparison has been made between a Hg UV lamp of 10 mW/cm^2(also used in [3]), and a LED UV array with 300 mW/cm^2 both irradiating for 30 minutes on a CPS coated glass sample.[1] Since the mercury based UV light source causes a radiative heating of the sample to approximately 80 °C, the LED curing is conducted on top of a hotplate that heated the sample to the same temperature.

Optically, the low intensity source causes a curing of the liquid silicon film without the change of transparent color, while the high intensity source changes this color from transparent to light yellow. In order to assess the material structures, Raman and spectrophotometric measurements have been performed.

The Raman results are shown in Fig. 3.5. In both samples a peak at 480 cm^{-1} is observed, associated to the Si-Si TO mode in a-Si. For the case of the higher intensity UV treatment, this peak is more prominent and overshadowing the quartz baseline, indi-

[1] Prior to the curing of by the different UV sources, both samples were treated by the low intensity UV source for 30 minutes to compensate for the high intensity cured capping effect, as will be explained later.

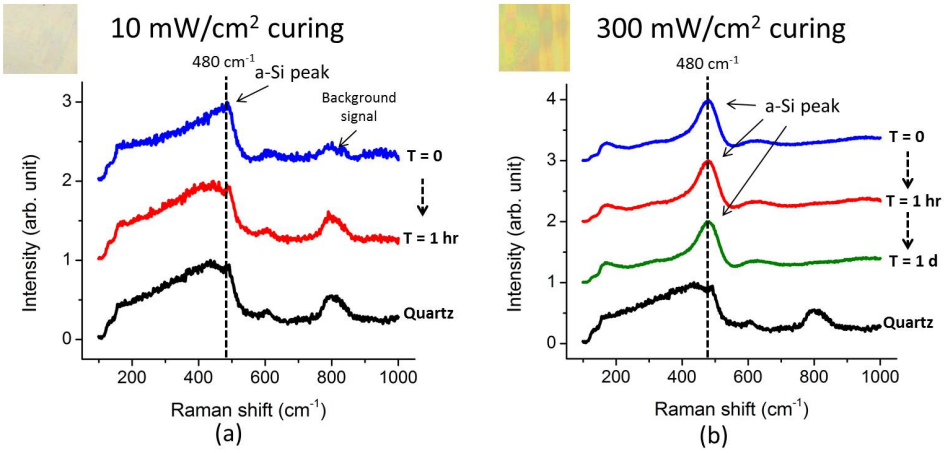

Figure 3.5: Raman spectra of CPS cured with 10 mW/cm^2 (a), and 300 mW/cm^2 (b).

cating a stronger degree of cross-linking. On the other hand, the low intensity treated sample only shows a relatively small bump at 480 cm^{-1} with strong influences of the quartz baseline. The signal intensities of the two signals were significantly different in spite of the fact that both film thicknesses were approximately the same (~200 nm).

Fig. 3.5 also shows the Raman spectra acquired over different moments of time of the sample after exposure to open air. For the high intensity UV cured sample, the Raman spectra stays approximately the same over the course of a day. On the contrary, for the lower intensity cured sample, the a-Si signal is consumed by the background signal after one hour. This suggests that a higher degree of cross-linking leads to a more stable a-Si network. This is because it is more difficult for the oxygen molecules to penetrate through a stronger cross-linked lattice.

This difference in stability has also been observed in the absorption spectra of the two types of cured CPS as shown in Fig. 3.6. Already after 1 hour the absorbance of the weakly cross-linked sample is significantly reduced, confirming the oxidation process, while that of the stronger cured sample stays approximately the same even after 1 day.

The high intensity cured sample was compared to the samples that Masuda et al. have created by thermal annealing in [8], specifically the sample annealed at 300 °C. The FWHM of the Raman bump at 480 cm^{-1} and the optical bandgap extracted from the Tauc plot are 74 cm^{-1} and 2.5 eV for the LED cured sample, and 80.5 cm^{-1} and 2.40 eV for the annealed sample. These results suggest that the quality and the structure of the two materials are comparable. Therefore, by a higher UV curing intensity of 300 mW/cm^2, cross-linking has been achieved to a similar level as when annealed to 300 °C.

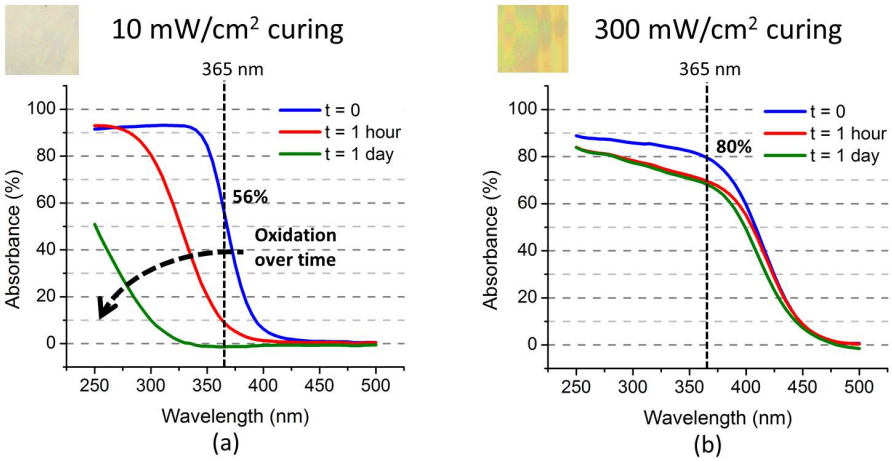

Figure 3.6: Absorption spectra of CPS samples cured with 10 mW/cm^2 (a) and 300 mW/cm^2 (b).

Further increasing the intensity of the UV curing treatment could in principle enhance the degree of cross-linking. However, this mechanism is limited by the fact that the transformation is stronger at the surface of the material. Therefore, after a certain amount of curing time, the first layers below the surface, which transform into a-Si become strongly opaque to the incident UV light(α_{365} = 1.3·10^5 cm^{-1}). A self-shielding capping layer is formed, and as a result the film cross-linking saturates at the surface, while leaving the bottom less cured.

This effect has been confirmed by observing a polysilane film coated on top of a quartz wafer. After an hour of curing the film in the 300 mW/cm^2 UV light, no color change was observed from the time of 45 minutes to 1 hour. However, when the film was exposed from the other side of the substrate, the quartz allowed the UV light to pass through and expose the bottom of the polysilane film. As a result, the yellow color of the polysilane became much darker already after 15 minutes of exposure. This effect has also been observed when heating the sample on a hotplate during the intense UV curing treatment. The increased temperature evidently improved the UV curing throughout the thickness of the film due to the molecular movement inside the material.

From the temperature measurements during the high intensity LED curing process at room temperature, only a limited temperature increase to 45 °C was detected, indicating that the polysilane transformation is a photochemical reaction rather than thermal. Although strongly curing the film does improve the cross-linking, when combining the process with thermal annealing at 300 °C, the added energy was still insufficient for the transformation from polysilane to a stable a-Si (i.e. one where the sample is annealed

at 350 °C). This means that a hybrid process of both UV curing and annealing, is not an efficient way of reducing the formation temperature of a stable silicon film.

Although cross-linking of the polysilane chains is sufficient to create a 3D amorphous silicon network, this mechanism does not enforce a crystalline arrangement of the silicon atoms. For crystallization, evidently, a higher energy has to be provided to the system where molecular ordering can be enforced. A much stronger UV light source such as an excimer laser may supply a sufficient amount of energy which could lead to a direct transformation of the film to poly-Si.

3.3. EXCIMER LASER CRYSTALLIZATION OF LIQUID SILICON

The excimer laser[11, 12] is an extremely intense UV light source that is commonly used in TFT fabrication to anneal dopants or crystallize thin a-Si films. Due to the low wavelength (200-400 nm), the absorption of the radiation occurs only within the first tens to hundreds of nanometers below the target surface. In addition, the very short pulse duration (20-200 ns), limits the excessive accumulation of heat which allows usage of low thermal budget substrates.

The working principle of the excimer laser is illustrated in Fig. 3.7 and is as follows: A noble gas atom (Xe, Kr, etc.) is ionized by an incident electron, and becomes highly reactive. The ion will thus form a dimer with a halogen atom, which is also present in the chamber. This dimer is in an excited energy state and decays spontaneously emitting a UV photon in the process. Along with irradiation the dimer breaks up into the constituent atoms, which are ready again to react once the electron beam is again available to ionize the noble gas. From the excitation of a dimer the term excimer came into being. Depending on the type of molecules different UV wavelengths could be irradiated. In addition, depending on the type of system, the pulse duration can be varied.

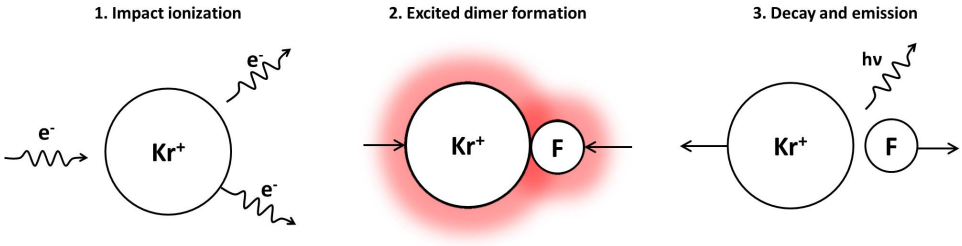

Figure 3.7: Schematic of the working principle of an excimer laser. First, a noble gas is ionized (a), then a dimer in an excited state is formed with a halogen atom (b), finally, the molecule decays and emits a UV photon (C).

In this work, two different excimer laser systems have been used: KrF (248 nm, 20 ns) and XeCl (308 nm, 28 ns). For lower wavelength lasers, the penetration depth of the laser inside the film is shorter. Therefore more energy is absorbed in a shallower volume of the silicon film. Pulse duration on the other hand is related to the crystal growth, a longer pulse duration is desired to increase the time for crystal grain formation which in general leads to larger crystal grains. Different liquid silicon candidates for excimer laser crystallization have been investigated and the first results are presented in the following sections.

3.3.1. EXCIMER LASER CRYSTALLIZATION OF CPS

Since UV wavelengths are used in the curing process of CPS, inevitably the excimer laser would have an effect on this material. To investigate this effect, CPS was coated on top of a glass substrate and treated with a XeCl excimer laser. After a single pulse of just 50 mJ/cm^2, the CPS film transformed into poly-Si as it was confirmed by Raman spectroscopy (see Fig. 3.8).

Along with crystallization, the exposed area has a high roughness due to the aggressive reaction from the high UV energy, specifically due to ablation. Ablation is caused by hydrogen eruption and phase explosion of the irradiated material. The hydrogen content of CPS is high, and the boiling point of the material is low. As a result, silicon hydride radicals will also be ejected when the irradiated laser pulse is absorbed by the film.

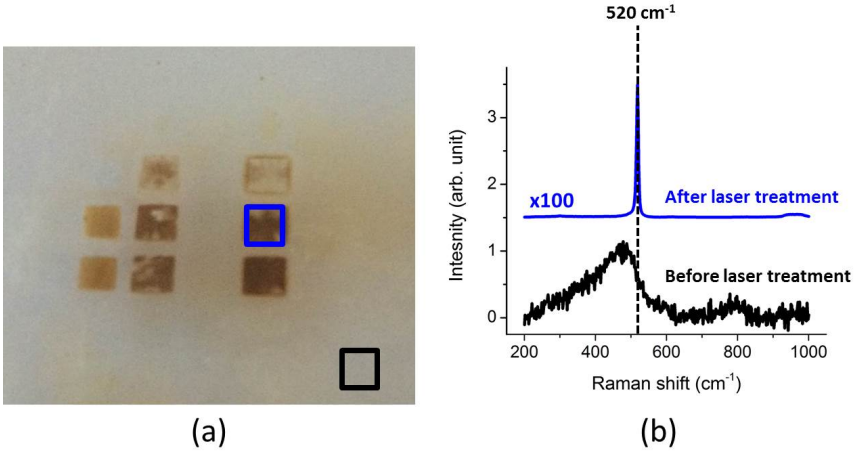

Figure 3.8: CPS film on glass crystallized by an excimer laser. Optical image (a), and the Raman spectra (b).

This sudden reaction is difficult to avoid and the roughness makes further processing of the film impractical and the yield low. In addition, ablation residues cause difficulties in subsequent electronic fabrication processes.

To overcome this drawback, the boiling point needs to be risen, and the hydrogen content reduced. Both can be achieved by using a milder UV treatment before excimer laser crystallization.

3.3.2. ELA OF WEAKLY CROSS-LINKED POLYSILANE

Polysilane, resulting from low intensity UV curing (10 mW/cm^2) of CPS also highly absorbs UV wavelengths as was shown by the absorption spectra in Fig. 3.6. As a result, this material could also be crystallized by the excimer laser (see Fig. 3.9). The boiling point of polysilane is much higher than CPS and therefore the level of ablation caused by silicon hydride radicals is significantly reduced.

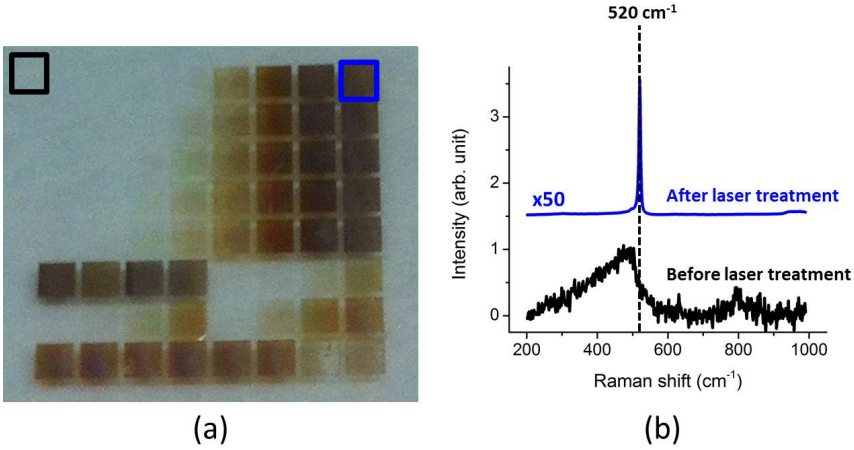

Figure 3.9: Optical image of polysilane cured with a UV intensity of 10 mW/cm^2, exposed to various excimer laser energy densities (a). Raman spectrum of one of the exposed areas and a non-exposed area (b).

Using polysilane as the ink, and excimer laser as the tool for crystallization, thin films could be treated while keeping the substrate intact. In this way, crystallization has also been achieved on top of paper, as shown in Fig. 3.10. The backside of the paper shows no damage from the heat induced by the laser, as shown in Fig. 3.10. A more in depth analysis of this process on paper is presented in Chapter 6.

Ablation could further be reduced by decreasing the hydrogen content of polysilane. This can be done by intensifying the curing treatment. As a result, more Si-H bonds are cleaved which also improves the cross-linking.

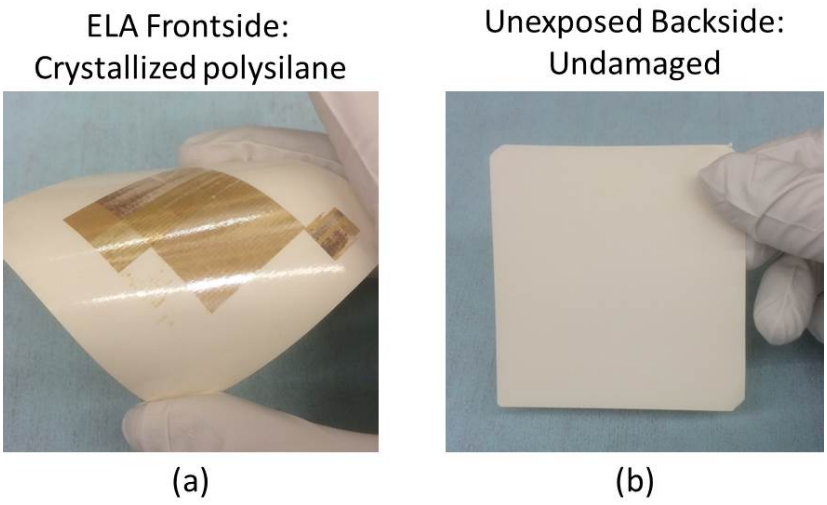

Figure 3.10: Optical image of first polysilicon directly created on top of paper (a), the undamaged backside (b).

3.3.3. ELA OF STRONGLY CROSS-LINKED POLYSILANE

The absorption spectrum of more intense UV curing treatments (300 mW/cm^2) shows in the same way as the weaker cured sample that UV light is absorbed by the film (see Fig. 3.6).Excimer laser crystallization has also been achieved using this material. In addition, ablation is significantly reduced compared to weaker UV treatments due to the reduction in hydrogen content. The higher degree of cross-linking also creates a system that has a lower tendency of breaking apart due to ablation.

The ablation of the polysilane as a result from the excimer laser treatment can be visualized by covering the sample with a quartz substrate during crystallization. In this way, the ablated material attaches to the surface of the quartz substrate. A comparison has been made between the quartz cover of the weakly and strongly cross-linked polysilane materials after excimer laser crystallization, and is shown in Fig. 3.11. The cover of the low intensity cured sample shows darker and more opaque colors than the high intensity cured sample due to the heavier ablation, for the same excimer laser energy densities.

A wider process window was found for the stronger UV source and this curing procedure is therefore pursued and will be the main type of film used for device fabrication in Chapter 5. The obtained results are further analyzed and discussed in the following section.

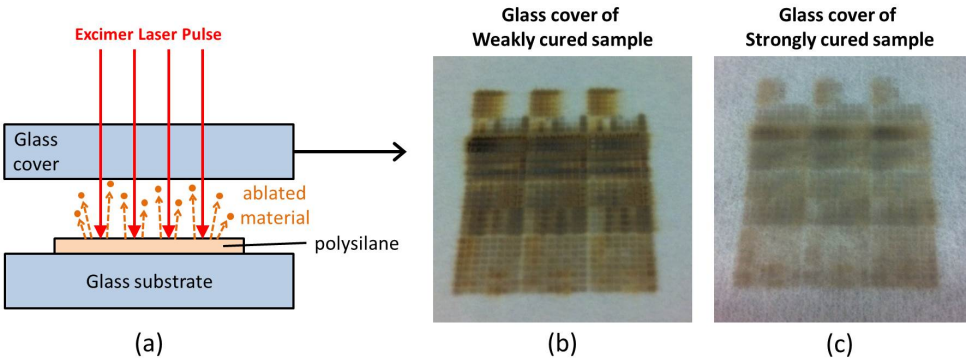

Figure 3.11: Schematic of the ablation detection process (a), and the glass covers that collected the ablation from the weaker cured sample (b), and the stronger cured sample (c).

3.4. PROPERTIES OF THE LASER CRYSTALLIZED POLYSILANE

In order to evaluate the quality of the polysilane films treated by different laser conditions, an in depth investigation is necessary. In this section, mainly the results from the KrF laser treatments are discussed, since the different excimer lasers gave similar results, only at a shifted laser fluence. Crystallization of the treated films is analyzed by Raman spectroscopy and TEM analysis. A deeper analysis of the Raman spectra will be given in the next section, this will not only reveal the crystallinity of the film but also the hydrogen content and the porosity. A TEM analysis gives a better understanding of the crystallization process by revealing the grain sizes, location and distribution. SEM analyses show the change in morphology of the crystallized films.

3.4.1. PHASE CHARACTERIZATION

For single pulse laser exposures a certain threshold laser fluence is observed above which the film shows signs of crystallization. At a relatively low excimer laser fluence of 40 mJ/cm^2 the film slightly changes its color as a result of an increase in degree of cross-linking of the film. As the fluence increases to 50 mJ/cm^2, this color change becomes more apparent and a stronger a-Si signal is detected. This effect is confirmed in the decrease of the FWHM of the a-Si TO peak at 480 cm^{-1} in the Raman spectrum.

For a laser pulse of 60 mJ/cm^2, the film shows signs of crystallization by the appearance of the crystalline silicon peak at 520 cm^{-1}. The relative intensity of this peak increases further for 70 mJ/cm^2 due to the increasing crystalline fraction. The Raman spectra of these single pulse laser treatments are shown in Fig.3.12 a.

Even higher laser fluences would lead to higher intensity Raman peaks although this does not guarantee the quality necessary for good electrical operation. From a fluence of 60 mJ/cm^2 and higher, the roughness of the film significantly increases, as observed in Fig.3.12 b. Which is harmful for the electronic device performance.

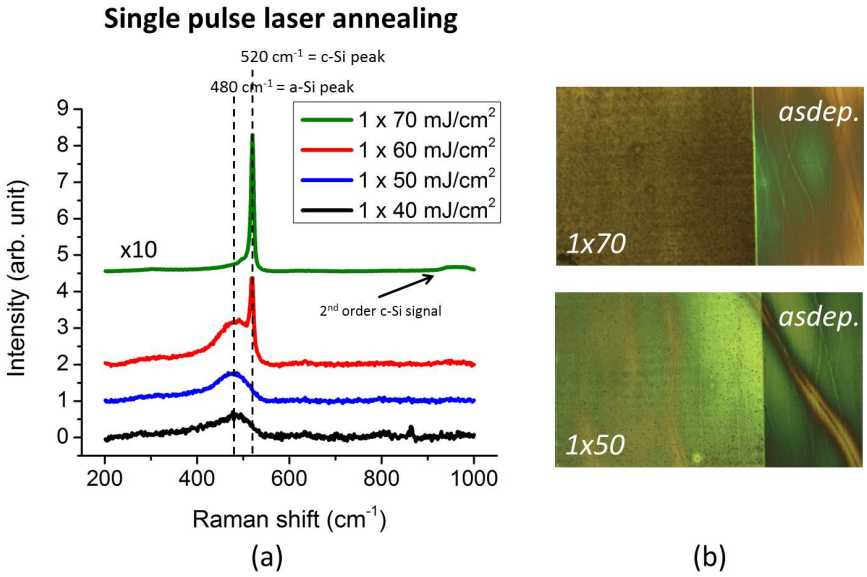

Figure 3.12: Raman spectra of polysilane exposed to single KrF excimer laser pulses (a), and the optical microscope image results of a crystallized and not crystallized sample (b).

When exposing the film to multiple pulses different results can be obtained. At 40 mJ/cm^2 regardless of the number of pulses, a phase change does not occur. However, the a-Si peak in the Raman spectrum does gradually increase, indicating an increase in cross-linking of polysilane. This can be observed in Fig. 3.13 a.

At 50 mJ/cm^2, while for a single pulse amorphous silicon was observed, for multiple pulses of the same fluence, a poly-Si peak at 520 cm^{-1} in the Raman spectra could be identified after 10 pulses, and this peak increases in intensity for even higher numbers of pulses. This is shown in Fig.3.13 b.

This effect is the result of the change in polysilane properties after the initial laser treatments that had insufficient energy for crystallization. This change allowed subsequent pulses to affect the film more strongly and as a result reduce the crystallization threshold fluence to 50 mJ/cm^2. How these properties affect the lowering of the threshold value is discussed in Chapter 4. For multiple pulses at higher laser fluences, since crystallinity is already reached, any remaining amorphous fraction will be crystallized.

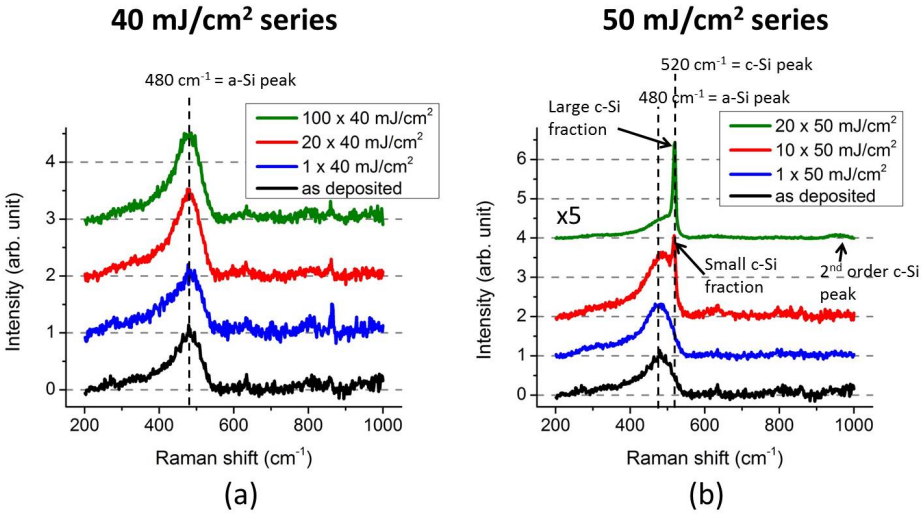

Figure 3.13: Raman spectra of polysilane exposed to multiple KrF excimer laser pulses. Difference from single to multiple pulses of 40 mJ/cm^2 (a) and 50 mJ/cm^2 (b).

A summary of the excimer laser crystallization results for different fluence and different numbers of pulses are expressed in the form of the FWHM of the 480 cm^{-1} peak for a-Si samples, and crystallinity fraction ϕ_c in Table 3.2.

Table 3.2: Single and multiple pulse KrF laser treatments and the associated a-Si peak FWHM, and crystalline fraction ϕ_c.

# of pulses	40 $^{mJ}/_{cm^2}$	50 $^{mJ}/_{cm^2}$	60 $^{mJ}/_{cm^2}$	70 $^{mJ}/_{cm^2}$
1x	a-Si FWHM: 107 cm^{-1}	a-Si FWHM: 89 cm^{-1}	p-Si ϕ_c= 39 %	p-Si ϕ_c= 90 %
20x	a-Si FWHM: 88 cm^{-1}	p-Si ϕ_c= 61 %	p-Si ϕ_c > 90 %	p-Si ϕ_c > 90 %

Cross-sectional TEM analyses of the treated film reveals the grain sizes and locations in Fig. 3.14. Crystallization is observed to occur at the surface of the polysilane film. This crystallization depth increases for higher numbers of pulses as well as laser fluences.

In the Raman spectra, a threshold fluence was observed to be around 50 mJ/cm^2. From the TEM images, for a single pulse of 50 mJ/cm^2 crystallization initiates at the surface. This crystalline fraction is too small to appear in the Raman spectrum. For multiple pulses of the same fluence however, the crystalline fraction increases and becomes observable by the Raman measurements.

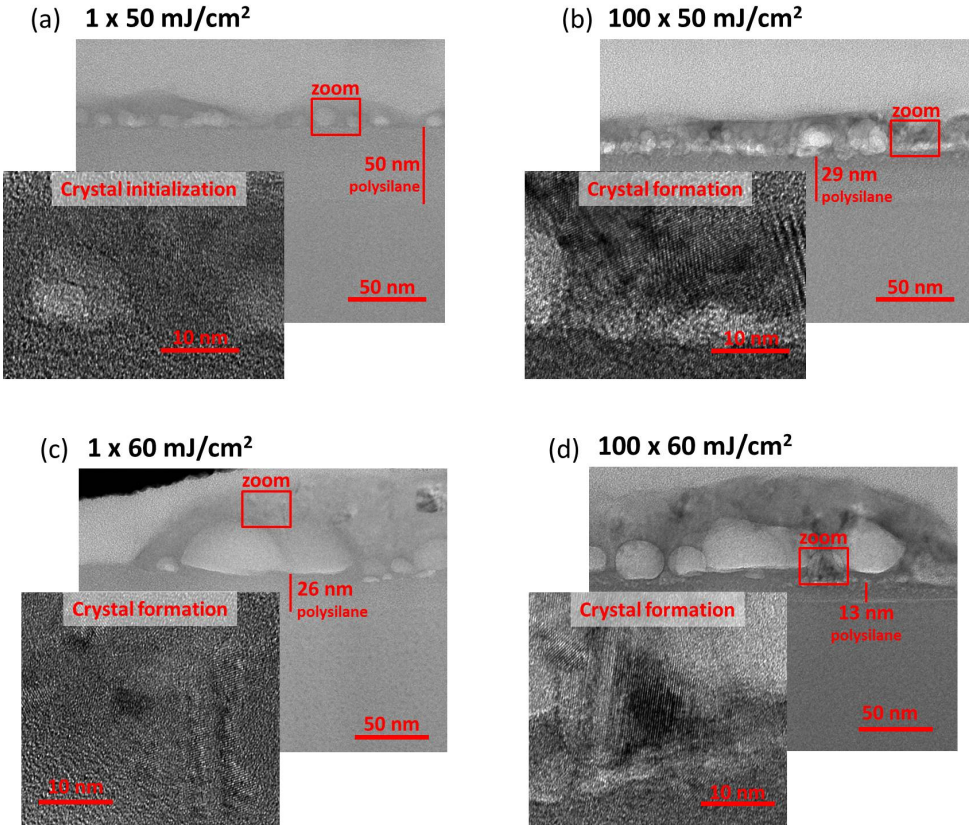

Figure 3.14: Cross-sectional TEM images of polysilane exposed to a KrF laser with different treatments: 1x 50 mJ/cm^{2}2 (a), 100x 50 mJ/cm^2 (b), 1x 60 mJ/cm^2 (c), and 100x 60 mJ/cm^2 (d).

Above 50 mJ/cm^2, although a stronger crystalline signal was observed for the Raman spectra, it also increased the roughness of the film. This was also observed in the cross-sectional TEM images, where clusters of crystals with white spheres appeared at the surface of the polysilane film. These white spheres grow in size for higher fluences (70 mJ/cm^2), but disappear for even higher fluences (100 mJ/cm^2). These white spheres are voids generated by the outgassing of the polysilane film, and trapped by a crystallized capping layer. They are detrimental to the structure of the final electronic device and should therefore be avoided. This effect can be reduced by using a dehydrogenation treatment prior to the crystallization. For multiple pulses of 50 mJ/cm^2 these white spheres are not present and the roughness of the film is relatively low. This laser procedure is therefore a preferred condition for TFTs.

3.4.2. HYDROGEN CONTENT AND POROSITY

Hydrogen content can be obtained from comparing Raman spectrum peaks at 2090 (Si-H stretching mode) to 480 cm^{-1} (Si-Si TO mode). A film that is cured with the high intensity UV light, has a hydrogen content of 50% which is close to the theoretical hydrogen content of a pure polydihydrosilane film which is 67%. This is because only the top few nanometers have a stronger cross-linking, while the film below stays as polysilane and is also being probed by the Raman green (514 nm) laser light source.

A polysilane film exposed to the excimer laser releases more hydrogen when it is treated with higher energy densities. Multiple pulses of the same energy also promotes the hydrogen removal and could therefore be beneficial for pre-annealing treatments to limit ablation. Pre-annealing using the excimer laser is further explained in App. A.

Porosity can be obtained from the Raman peaks at 2000 and 2090 cm^{-1}. The porosity of the as deposited material is similar to the one that was annealed at T>330 °C [8]. For the crystallized samples, porosity stays at a similar level. This means that structurally the material remains porous, and that only a fraction of the film may have reduced in porosity. Table 3.3 compares the hydrogen content and porosity with respect to the different KrF laser sequences.

Table 3.3: Single and multiple pulse KrF laser treatments and the associated hydrogen content and porosity.

	asdep	1x 50 $^{mJ}/_{cm^2}$	20x 50 $^{mJ}/_{cm^2}$	1x 70 $^{mJ}/_{cm^2}$
Hydrogen content	50 %	22 %	18 %	7 %
Porosity	0.81	0.79	0.80	0.79

3.4.3. SURFACE MORPHOLOGY

Excimer laser treatment of polysilane has shown a phase change depending on the laser fluence, and this is generally accompanied by the roughening of the surface. For samples exposed to any number of pulses of 40 mJ/cm^2, the film does not change its morphology. For both single as multiple pulses of 50 mJ/cm^2, a wavy texture of the sample surface is observed that is the first sign of superficial melting. For a single exposure of higher energy densities, the film melts deeper and agglomerates resulting in a film with droplet textures, as can be observed in the SEM images in Fig. 3.15.

At increasing fluences for multiple pulses the film increasingly agglomerates until finally the surface is covered with silicon spheres owing to the Gibbs free energy minimization. This is because silicon has a poor wettability on SiO_2 [13], shown in Fig. 3.16. The TEM suggested that there is gas formation during the laser annealing process. These gas bubbles get encapsulated by a crystalline silicon layer. This theory is supported by

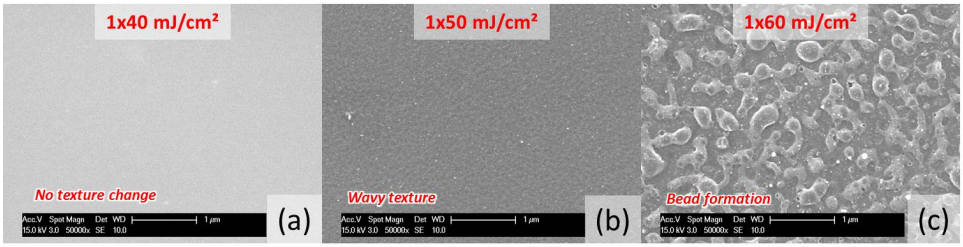

Figure 3.15: SEM image of single KrF ELA pulses at 40 mJ/cm^2 (a), 50 mJ/cm^2 (b), 60 mJ/cm^2 (c).

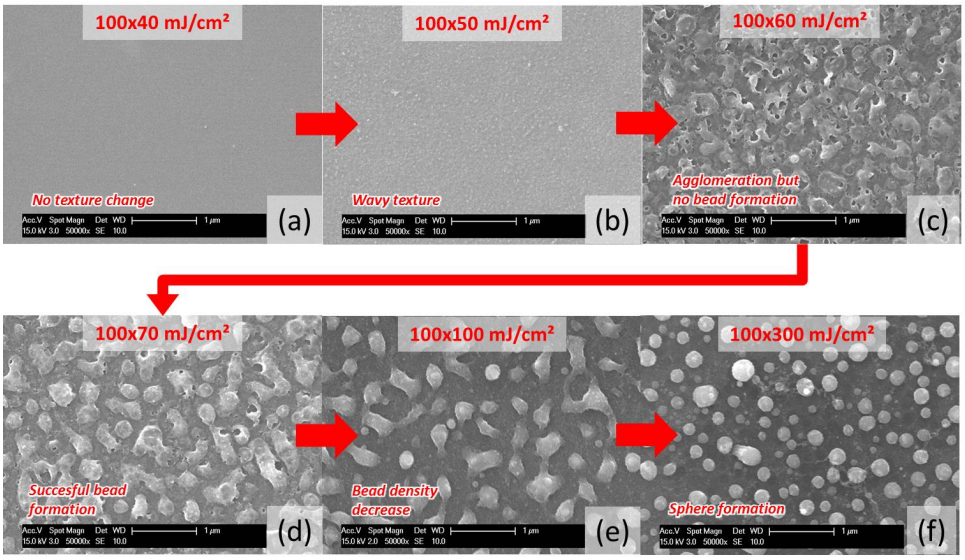

Figure 3.16: SEM image of 100 KrF ELA pulses per energy density area: 40 mJ/cm^2 (a), 50 mJ/cm^2 (b), 60 mJ/cm^2 (c), 70 mJ/cm^2 (d), 100 mJ/cm^2 (e), 300 mJ/cm^2 (f).

the images of 100 pulses of 60 and 70 mJ/cm^2, where some of the agglomerated droplet shapes are bursted, revealing a hollow bubble interior.

An analysis of the surface morphology around the threshold laser fluence gives an indication on the initialization of the surface deformation and is shown in Fig. 3.17. As the laser fluence increases, the film surface starts to melt and show a wavy texture. Increasing the fluence further small openings are created which increase in size, which is due to ablation of hydrogen as well as radicals with a low molecular weight. At the same time, the edge of these openings collect parts of the removed silicon film to form beads. These beads further increase in size while more of the original film is consumed at even higher fluences. This is due to stronger ablation effects, and longer melting times.

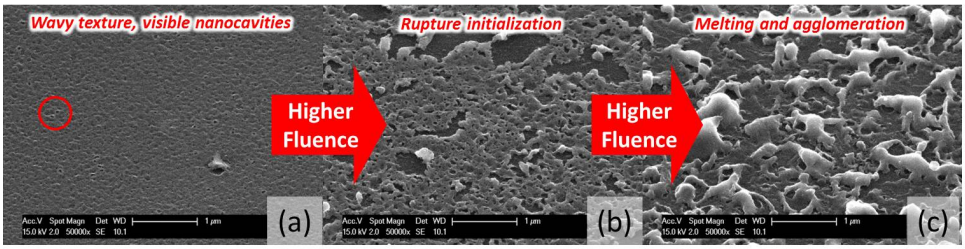

Figure 3.17: SEM images showing the texture change from wavy(a), to rupture(b), to agglomeration(c), in increasing laser fluences.

For solar cell applications, texturing is an advantage. In order to trap light, deliberate texturing of the solar cell film is a common practice. For TFT applications however the roughness harms the charge carrier transportation in the device and will significantly decrease the maximum obtainable charge carrier mobility. Therefore, an agglomerated film for these applications is not desired, and a crystallized film that has a low roughness such as the one that is exposed to multiple pulses of 50 mJ/cm^2 as described above, is expected to give the highest mobility devices.

3.4.4. PROCESS WINDOW

In this Chapter various KrF excimer laser conditions have been analyzed using Raman spectroscopy, SEM, and TEM, and a right balance has to be found between crystallization and low roughness. The results are presented in Fig. 3.18.

In the image, the green and orange colored areas are conditions for which the Raman spectra showed crystallization. The orange colored areas are those that have shown a high roughness during the morphology analyses. The yellow color was assigned to those areas that have shown a higher intensity a-Si Raman peak compared to the original as deposited polysilane material. Finally, the colorless areas are those that have absorbed insufficient laser energy for any structural transformation.

From the obtained results, for TFT purposes an excimer laser treatment of multiple pulses of 50 mJ/cm^2 is advised. This condition may change however due to process variations, therefore in the TFT process in this work, besides 50 mJ/cm^2, 40 and 60 mJ/cm^2 have also been used to account for these variations.

The results obtained in this chapter have been confirmed by a number of different excimer laser sources and samples, however, it is important to note that the process window of the liquid silicon crystallization process depends on many factors:

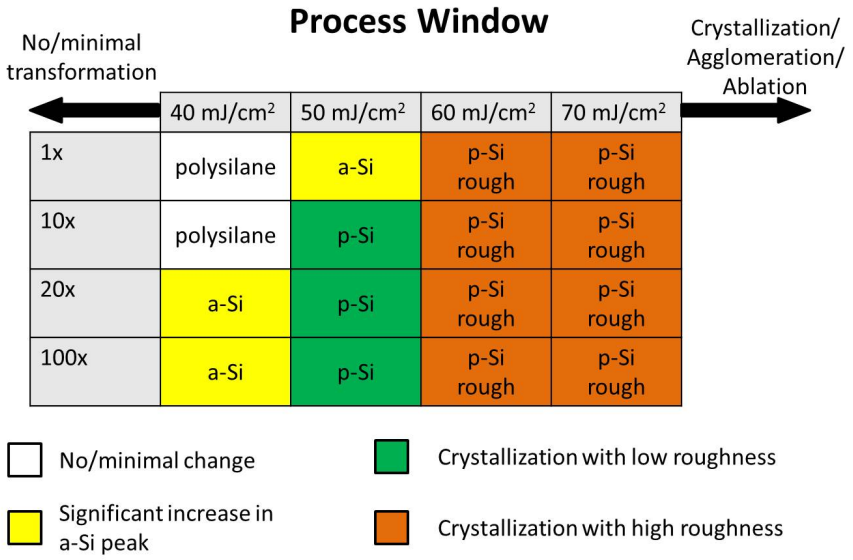

Figure 3.18: Process window of KrF excimer laser treatment on polysilane.

Laser

First of all, the type of excimer laser used has a big impact on the process window. Three aspects of the laser need to be assessed: laser wavelength, pulse duration and beam uniformity. A change in the laser wavelength changes the penetration depth of the light inside the film. For lower wavelengths, the energy is absorbed in a smaller volume of the film, which could lead to a more aggressive ablative result, and therefore a decrease in the threshold fluence which limits the process window. Therefore, a relatively long wavelength within the UV range is favorable.

The laser pulse duration has a strong impact on the melting time and depth. The laser energy as a function of pulse duration changes. For a specific laser fluence, the area under this curve stays the same. As a result, shorter pulse durations will lead to larger peak energies. This would therefore lower the threshold fluence. A prolonged melting time as a result of a longer pulse duration, generally leads to larger crystal grain sizes which is advantageous for transistor performance.

The laser beam profile uniformity has and additional impact on the film uniformity. Local variations in fluence levels around the threshold, could lead to crystallization in some parts while leaving the other parts of the irradiated area amorphous.

Thickness

A variation in thickness may lead to a variation in absorbed laser energy as shown in Fig. 3.19. For thinner films, higher laser fluences are required in order to reach crystallization compared to thicker films. At the same time, thicker films are more likely to ablate, while also more likely to produce large crystal grains. Uniform film deposition is therefore of essence for finding a more accurate process window.

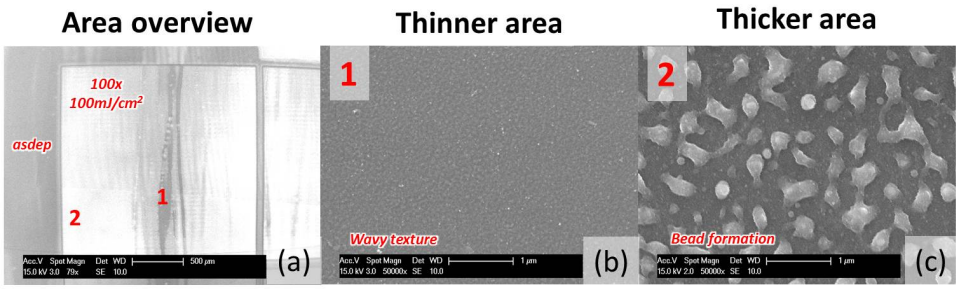

Figure 3.19: SEM images of an area exposed to 100 pulses of 100 mJ/cm^2. General overview of the area defining the two areas with different thicknesses 1 and 2 (a). Zoomed area of thickness 1 (b), and zoomed area of thickness 2 (c).

Ink

Depending on the starting material, the crystallization properties can vary. The degree of cross-linking or the size of the molecules inside the film will have a direct impact on the absorption, density, melting temperature, thermal capacity, and thermal conductivity among others. As shown in this chapter, a stronger polymerized material will have a different crystallization result compared to one that is weakly polymerized or even non-cured pure CPS. In this work all three kinds were crystallized and there were different laser fluence requirements observed for each type of material.

Substrate

The type of substrate will also influence the required fluence for crystallization of liquid silicon. It may change the way the film crystallizes as a result of the laser treatment, and change the way the liquid is coated and therefore vary in thickness. A highly thermally conductive surface for instance will require higher fluences compared to surfaces with a low thermal conductivity. Another parameter is the adhesion which can in some cases prevent ablated film from being ejected from the substrate. Coating variations include the wettability by surface energy of the ink to the substrate surface.

3.5. CONCLUSIONS

In this chapter, a new method has been introduced that allows the production of polycrystalline silicon directly on low thermal budget substrates when using liquid silicon as a precursor.

It has been observed in the steps taken to create poly-Si from CPS, that the intensity of UV curing has a strong impact on the properties of the cured material. Changing the UV curing intensity from 10 mW/cm^2 to 300 mW/cm^2 leads to an optical change in color from transparent to yellow, as a result of a narrowing of the bandgap from 6.5 eV to 2.5 eV. In addition, Raman spectroscopy analysis revealed a stronger a-Si signal which is due to the increase in degree of cross-linking inside the material. The results were similar to those obtained by liquid silicon having annealed at 300°C.

The curing process is a photochemical effect since the temperature of the film during curing did not increase over 45°C. A combination of high intensity UV curing with a heating treatment did not result in an efficient way of decreasing the CPS processing temperature. Moreover the process does not introduce a molecular arrangement of silicon atoms that could lead to crystallization. Therefore an alternative route is needed that could deliver much higher energies.

An excimer laser could crystallize liquid silicon without significant heating of the substrate. In this way poly-Si could even be created directly on top of paper. CPS could be crystallized, although this did not result in a controllable process due to severe ablation. A curing step of 10 mW/cm^2 before the excimer laser treatment significantly reduced the outgassing of silicon hydride radicals. An even further reduction of ablation was found when the material was cured with 300 mW/cm^2 due to hydrogen reduction.

The polycrystalline silicon produced by this process has been analyzed using Raman spectroscopy, TEM, and SEM. For a single pulse, a threshold laser fluence was found (50 mJ/cm^2) above which the film crystallizes, and below which the film only increase its cross-linking. At crystallization fluences, outgassing from ablation still causes the film to significantly increase its roughness. This roughness needs to be avoided to ensure high electronic performance.

Multiple pulses facilitates the laser transformation process. At the threshold fluence of 50 mJ/cm^2, a single pulse resulted in a-Si, while multiple pulses led to the crystallization of the film. This laser procedure of multiple pulses of 50 mJ/cm^2 gave the best trade-off in terms of crystallization and relatively low surface roughness. Although process variations, in particular the laser type, precursor thickness and quality, and the substrate type, may change the threshold level and process window.

In this way an intermediate transformation step of the liquid silicon material to amor-

phous silicon is omitted, and a direct transformation of polysilicon from cured CPS could be achieved by using a tool that is commonly used in the TFT industry for thin film crystallization: the excimer laser.

REFERENCES

[1] Y.-H. Chang, S.-R. Tseng, C.-Y. Chen, H.-F. Meng, E.-C. Chen, S.-F. Horng, and C.-S. Hsu, *Polymer solar cell by blade coating,* Organic Electronics **10**, 741 (2009).

[2] T. Masuda, N. Sotani, H. Hamada, Y. Matsuki, and T. Shimoda, *Fabrication of solution-processed hydrogenated amorphous silicon single-junction solar cells,* Applied Physics Letters **100**, 253908 (2012).

[3] J. Zhang, M. Trifunovic, M. Van Der Zwan, H. Takagishi, R. Kawajiri, T. Shimoda, C. Beenakker, and R. Ishihara, *Single-grain si thin-film transistors on flexible polyimide substrate fabricated from doctor-blade coated liquid-si,* Applied Physics Letters **102**, 243502 (2013).

[4] J. Tauc and A. Menth, *States in the gap,* Journal of Non-Crystalline Solids **8**, 569 (1972).

[5] G. Lucovsky, R. J. Nemanich, and J. Knights, *Structural interpretation of the vibrational spectra of a-si: H alloys,* Physical Review B **19**, 2064 (1979).

[6] C. Droz, E. Vallat-Sauvain, J. Bailat, L. Feitknecht, J. Meier, and A. Shah, *Relationship between raman crystallinity and open-circuit voltage in microcrystalline silicon solar cells,* Solar Energy Materials and Solar Cells **81**, 61 (2004).

[7] P. Vora, S. Solin, and P. John, *Raman scattering from pristine and oxidized polysilanes,* Physical Review B **29**, 3423 (1984).

[8] T. Masuda, Y. Matsuki, and T. Shimoda, *Pyrolytic transformation from polydihydrosilane to hydrogenated amorphous silicon film,* Thin Solid Films **520**, 6603 (2012).

[9] U. o. W. Susan Swapp, *Scanning electron microscopy (sem),* online (2016).

[10] *The university of iowa, central microscopy research facility,* online (2016).

[11] P. van der Wilt, *Formation of Crystalline-Silicon Islands for Thin-Film Transistors by Excimer-Laser-Induced Lateral Growth*, Ph.D. thesis, Delft University of Technology (TU Delft) (2003).

[12] N. H. Nickel, *Laser crystallization of silicon,* (Elsevier, 2003) Chap. Introduction to Laser Crystallization of Silicon - N.H. Nickel, pp. 1–9.

[13] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI: Materials to Vlsi* (Springer Science & Business Media, 2004).

4

Liquid Silicon Excimer Laser Annealing Mechanism

In the previous chapter, a new method of silicon formation from liquid silicon has been developed and the experimental results have been analyzed. The fundamental dynamics behind the process, need to be understood in order to develop optimized process conditions or more efficient transformation methods. The first step to fulfill this aim is to define a semi-empirical model that can reliably predict the effects of excimer laser annealing (ELA) on liquid silicon films and that can trace the short time evolution of the process. If this model is in accordance with the experimental observations, it can be used to analyze the ELA behavior as a function of various parameters, without the need to invest long time and many resources in performing dedicated experiments.

In this chapter, the ELA is assumed to be governed by the classical heat transfer theory in solids. The related differential equation, whose solution gives the film temperature space profile as a function of time, is handled using a transient heat analysis. This chapter first deals with the excimer laser annealing theory, the various laser-matter interaction models, and the model used in this work in section 4.1. This model is then applied to LPCVD a-Si that forms the reference for the liquid silicon simulations in section 4.2. In order to simulate for polysilane, the physical parameters are measured, or deduced, in section 4.3. In section 4.4, the simulation results are presented and compared to the experimental data obtained in chapter 3. The chapter subsequently discusses the effectiveness and limitations of the chosen model in section 4.5, and finally concludes the liquid silicon excimer laser transformation theory in section 4.6.

4.1. INTRODUCTION

4.1.1. LASER-MATTER INTERACTIONS

The excimer laser was found to be an effective tool to heat the surface layers of thin films while leaving the bulk material unharmed. The causes behind this mechanism are the shallow absorption of UV light and the limited laser pulse duration to few tens or hundreds of nanoseconds. The first applications of this treatment were found in the field of dopant activation [1]. Only later the laser crystallization of a-Si had increasingly attracted attention and a great deal of research has been done on characterization and modeling of this process[2, 3]. In these studies, heat was found to play a dominating role, since the incoming photons produce heat through the generation of lattice vibrations (phonons). In general, as illustrated in Fig. 4.1, a semiconductor (or dielectric) film absorbing laser light can be heated by 4 different mechanisms:

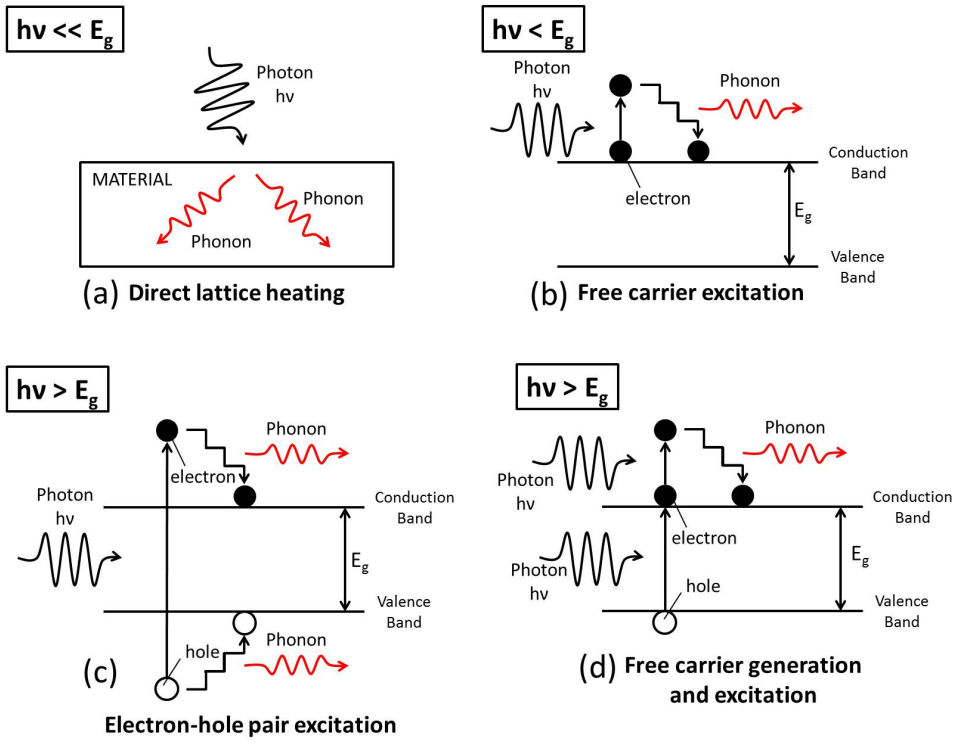

Figure 4.1: Illustrations of laser energy absorption mechanisms for photon energy $h\nu \ll$ bandgap energy E_g (a), $h\nu < E_g$ (b), $h\nu < E_g$ (c), and $h\nu < E_g$ with high intensity (d).

1. For photon energy $h\nu \ll$ bandgap energy E_g: Lattice vibrations of specific molecular bonds are directly excited through absorption of light.

2. For $h\nu < E_g$: The incident photons excite free charge carriers in highly doped semiconductors. Phonons are then created by thermalization of the excited free electrons.

3. For $h\nu > E_g$: Electron-hole pairs are generated and phonons are created by their intra-band thermalization and non-radiative recombination

4. For $h\nu > E_g$ and high light intensities: photo-generated charge carriers are excited to higher energies before their thermalization. This is known as laser induced metallic mechanism

For the case of excimer laser ($h\nu$ > 3.4 eV) crystallization of intrinsic a-Si (indirect band gap of 1.9 eV)[1], only the third mechanism is relevant. In the crystallization of amorphous silicon(a-Si) films, a crucial parameter is the melting point of a-Si that is several hundred degrees lower (depending on the synthesis, T_{ma} =~1400 K) than that of crystalline silicon (c-Si) (T_{mc} = 1687 K)[1]. Therefore, when the a-Si film is treated with a high power laser and the temperature reaches its melting point, the molten silicon is supercooled. When there are no nucleation sites and the cooling rate is high, the liquid will resolidify to a-Si.

In most cases however, the cooling rate is sufficiently low. The molten silicon will thus solidify into polycrystalline Si by nucleation and growth of crystalline grains. The excimer laser annealing has different influences on the film depending on the temperature that it reaches as a result of the laser treatment, as well as film variations. Six different phenomena can be distinguished[4, 5]. The first three are related to laser annealed heating above T_{ma}, also shown in Fig. 4.2. The last three are related to the laser annealed heating above T_{mc}, as shown in Fig. 4.3.

$T < T_{ma}$

No melting: The film is heated, but the melting point is not reached. This mechanism is usually used for dehydrogenation and dopant activation.

$T_{mc} > T > T_{ma}$

Partial melting of pure a-Si: Only part of the amorphous silicon film is molten. At the solid-liquid interface, nucleation sites form that become seeds for crystalline

[1] High intensity UV cured polysilane has a bandgap of approximately 2.5 eV. KrF, and XeCl lasers used in this work have energies of 5 and 4 eV, respectively.

grain growth. The molten volume resolidifies as polycrystalline silicon, and latent heat of solidification is released. Since this latent heat of solidification is higher than the latent heat of melting, there is a net flux of released heat. As a consequence, the temperature of the a-Si layer beneath the liquid-solid interface rises above the melting point. As a result, the newly molten material resolidifies into poly-Si which in turn produces again latent heat. The process is self-sustaining and a melt-front propagates deeper in the film, leaving a thick volume of fine-grained poly-Si behind. This process is known as explosive crystallization and is halted when the heat losses become sufficient to obstruct any further melting. In this way, a maximum crystallization depth is reached.

$T_{mc} > T > T_{ma}$

Partial melting of a-Si with crystalline fractions: Since the crystalline particles inside the a-Si film have higher melting points, they stay solid and only the amorphous fraction is molten. The liquid Si then solidifies into course-grained poly-Si since the crystalline inclusions act as seeds. This crystallization again produces latent heat which initiates explosive crystallization.

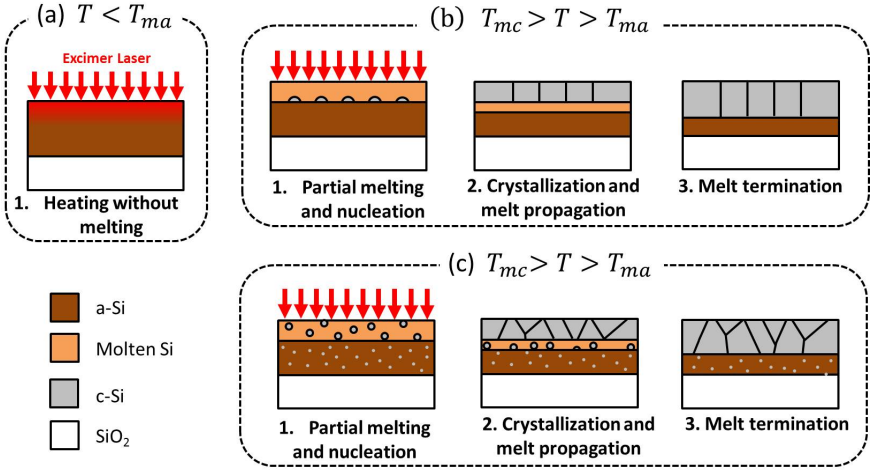

Figure 4.2: Schematic of excimer laser annealing where film reaches temperature below Tma (a), between Tma and Tmc for pure a-Si (b), and between Tma and Tmc for a-Si with crystalline fraction (c).

$T > T_{mc}$

Partial melting: The previously (explosively) crystallized silicon at the surface will initiate a secondary melt. Since the molten silicon is now much less supercooled, the solidification rate is slowed down and much larger grains are produced.

$T > T_{mc}$

Near-complete melting: In this scenario, most of the film is molten however traces of solid silicon remains which initiate the crystallization process similar to the melting of a-Si with crystalline fractions. A phenomenon known as super-lateral growth has been observed. During this process the silicon traces or seeds grow in all directions. Crystal growth of neighboring seeds may meet and form a grain boundary at the line of collision. Relatively large grain sizes are formed in this process.

$T \gg T_{mc}$

Complete melting: The entire film under the laser beam is molten. Crystallization initiates with random nucleation of crystalline grains. Since nucleation takes time, the liquid film is again supercooled. As a result, relatively small grains are formed.

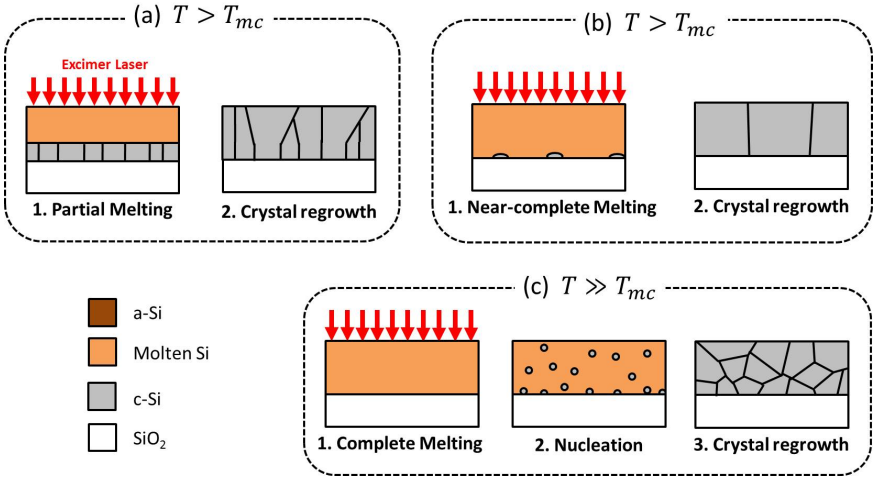

Figure 4.3: Schematic of excimer laser annealing where c-Si film reaches temperature above Tmc. Allowing it to partially melt (a), reach near-complete melt (b), and completely melt (c).

4.1.2. LASER ANNEALING MODELS

In order to accurately model the laser-induced heat transfer in solids, two models are available. The choice of this model depends on the lifetime of electron-hole pairs during laser irradiation and the transfer of energy from the system to the lattice[3]:

Plasma model

For femto- or pico-second laser pulses, the density and the energy of photo-generated charges are so high that they massively diffuse beyond the absorbing volume, faster than the heat transfer to the lattice. As a consequence, the temperature of charge carriers is higher than the local temperature of the lattice and the two systems are not in equilibrium. Plasma models with appropriate relaxation times (time for energy transfer of carrier to lattice through carrier-phonon coupling) should be used. These relaxation times should be comparable to the length of the laser pulse. For Si and Ge these relaxation times were found to be approximately 0.4 to 1.0 ps. Therefore for the pico-second regime, the recombination time is comparable with the pulse duration itself and the dynamics of plasma must be included to describe lattice heating.

Thermal model

For the nanosecond pulse durations, which is commonly the case for excimer laser systems, pure thermal models are sufficient. For these cases it is assumed that the photo-generated charges thermalize before far diffusion, therefore they establish local equilibrium with the lattice.

For thermal modeling, the finite element analysis solver and simulation software COMSOL Multiphysics® version 4.4 has been used. Within this program a time-dependent study was applied on the method: Heat Transfer in Solids. This model analyzes the temperature space profile evolution within the irradiated film considering a continuous material structure. The material is subdivided in multiple geometric parts called meshes, which are individually analyzed during the simulation.

An alternative modeling type considers the material as a molecular or atomic system. This would make the simulations more accurate, but also are more complex and require longer simulation times.

The continuous model has the advantage of computational efficiency, however its predictive power is limited since a-priori knowledge of the material properties is needed in order to be able to rely on the outcomes. This makes the modeling of new materials challenging. However, sufficient insight of the heating process can be gained when the simulation results are compared to the experimental results.

In this work, the heat transfer is analyzed excluding convective transport within the film, degassing and ablation. Furthermore, the model is restricted to the surface heating path of the film cross-section (1D), since the laser beam spot size (2x2 mm^2) is much larger than the thermal diffusion length (few hundred nanometers to micrometers), and the fluence within the spot is uniform.

In this work the geometry of the simulation sample is set up as 200 nm of silicon ink material on top of a 5 µm SiO_2 substrate. Although it is common to crystallize a-Si on top of a silicon wafer with an oxide barrier layer, the difference in temperature between simulating an all glass substrate, and an 850 nm barrier layer on a silicon wafer is negligible. This is because the absorption of short-wavelength laser light occurs solely within the Si ink film.

The film has been modeled with mesh elements of 0.1 nm in size. On the other hand for the substrate a coarser mesh size of 1 nm is chosen. The simulation sample geometry is shown in Fig. 4.4.

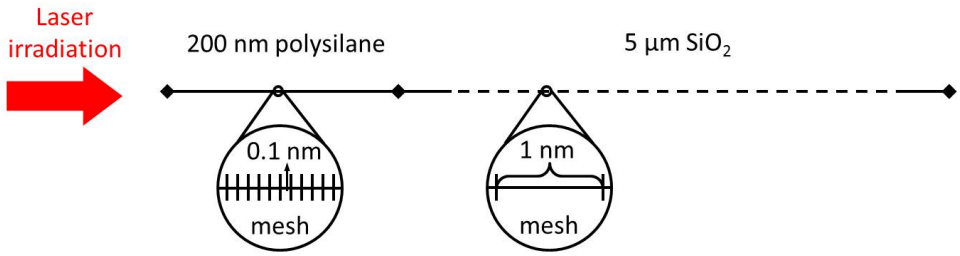

Figure 4.4: Schematic of simulation geometry and meshing for the 1-dimensional sample of 200 nm polysilane on top of 5 µm glass.

In the simulations carried out in this work, the transport of heat induced by laser absorption is described by the one dimensional Stefan equation[2, 3, 6]:

$$\frac{\partial T}{\partial t} = \frac{\alpha}{\rho \cdot C_p} I(x,t) + \frac{1}{\rho \cdot C_p} \frac{\partial}{\partial x}\left(\kappa \frac{\partial T}{\partial x}\right) \tag{4.1}$$

where $\frac{\partial T}{\partial t}$ is the transient term, and accounts for the non-stationary behavior of temperature, and $I(x,t)$ is the power density of the laser pulse at depth x and time t. For the treated material, the employed properties are reflected in the equation as: α the absorption coefficient, ρ the density, C_p the specific heat, κ the thermal conductivity, and $\frac{\partial T}{\partial x}$ accounts for the heat conduction in the solid.

The power density can be described by the Beer-Lambert law since it is assumed that the material is uniformly absorbing.

$$I(x,t) = I_0(t)(1-R)e^{-\alpha \cdot x} \tag{4.2}$$

where I_0 is the output power density of the laser and R is the reflectivity of the material. This equation does not take into account the temperature dependence of the refraction index and the extinction coefficient that play a role in the reflectivity and absorption coefficient of the material.

The boundary condition at the bottom of the system is a fixed temperature of 293.15 K (Dirichlet condition), since the sample is always placed on a metallic chuck during laser annealing. The boundary condition at the top of the system is described by

$$\overrightarrow{n}(\kappa\frac{\partial T}{\partial t}) = h(T_{ext} - T) \tag{4.3}$$

where n is the vector, normal to the surface, h the convective heat transfer coefficient, and T_{ext} the constant ambient temperature of 293.15 K. For h, a value between 1 and 100 W/m^{2}K is common for open air. In this work, a value of 1 W/m^2 is has been used since the treatment is conducted within a confined ambient, although variations of this value has a negligible effect on the final simulation result.

In order to take into account the possibility of phase transition from a-Si to molten Si, a Heaviside step-function is used to change specific parameters of the sample when a melting temperature is reached in the simulation process, which is defined by:

$$X_{sim} = X_{solid}(1 - H(T_m)) + X_{molten}H(T_m)) \tag{4.4}$$

where X_{sim} is the value of a specific parameter used in the simulation, X_{solid} and X_{molten} the value of the solid and molten parameters, respectively, $H(T_m)$ the Heaviside step-function that is triggered when the sample temperature increases above the melting point.

Additionally, latent heat is implemented for the phase change of solid a-Si to molten silicon. A Gaussian curve is used with a standard deviation of 0.5 K, which allows a smooth triggering of the latent heat around the melting temperature.

The laser pulse time profile used in this simulation was extracted from an excimer laser source with pulse duration (FWHM) of 25 ns and was corrected for a pulse width of 20 ns. The solver time-step of the simulations is 0.1 ns.

This model assumes that melting and solidification occur at equilibrium phase-change temperature and that the introduction of interfacial kinetics into the modeling is not necessary.

4.2. MODELING LPCVD SILICON ELA

Using the aforementioned simulation model, the excimer laser annealing of LPCVD amorphous silicon has been simulated as a reference to the treatment on polysilane. For this modeling, a prior knowledge of the parameters that are used in the thermal simulations is necessary, such as melting point, thermal capacity, thermal conductivity, latent heat, etc. Although these parameters are fixed for c-Si, for a-Si they change depending on its synthesis.

4.2.1. LPCVD SI MATERIAL PARAMETERS

The parameters that are used for the thermal computations are similar to the ones used in [6] and are listed in table 4.1.

Table 4.1: Parameters for thermal analysis of a-Si:H and molten silicon.

Parameter	a-Si:H	molten silicon
Melting point (K)	1440	-
Density (g/cm^3)	2.26	2.52
Latent heat (J/g)	1320	-
Absorption coefficient (cm^{-1})	$1.75{\cdot}10^6$	$1.63{\cdot}10^6$
Reflectivity	0.58	0.72
Heat Capacity (J/kgK)	$952+0.0917T$	860
Thermal Conductivity (W/m·K)	$1.3\cdot10^{-9}(T-900)^3+$ $1.3\cdot10^{-7}(T-900)^2+$ $1.0\cdot10^{-4}(T-900)+1$	$50.2+0.0293(T-1687)$

Some of the parameters that are listed in table 4.1 are temperature dependent. Parameters such as reflectivity and absorption coefficient change as a function of temperature, although this change is sufficiently small to be omitted [2, 6]. Only for the thermal conductivity and heat capacity this thermal dependence has been implemented.

4.2.2. LPCVD SI SIMULATION RESULTS

A sample of 200 nm LPCVD a-Si on top of 5 µm SiO_2 has been considered as a reference, which is irradiated with a 20 ns KrF laser. The model has been tested and compared to the results of Förster and Vogt [6], who have supported their simulation results with experimental data. Similar simulation results were obtained in this work, therefore the model used for LPCVD a-Si is valid. In this work, a threshold fluence of 69 mJ/cm^2 has been observed for reaching the melting temperature of a-Si.

4.3. LIQUID SILICON MATERIAL PARAMETER EXTRACTION

For the simulation of polysilane ELA, knowledge of the necessary parameters are necessary. Rather than speculating, extracting these parameters directly from the material would make the simulations more accurate. To measure such parameters however, generally larger quantities of the material is necessary, which is difficult to handle unless sealed, since it is not stable in open air.

In the choice of polysilane, a difference in stability has been observed for samples that are cured with different UV light intensities, as explained in section 3.2. CPS cured with a higher intensity UV light was found to be more stable, due to the increased amount of cross-links formed from the photopolymerization. In addition hydrogen was removed that reduced the damage from ablation from the laser annealing treatment. As a result, a wider process window could be obtained using this type of polysilane.

For the parameter extraction, measurements should be conducted on polysilane that is prepared in a similar way to the experimental samples. This material was prepared by first curing CPS for 30 minutes under a UV light with intensity of 10 mW/cm^2, followed by a UV curing of 300 mW/cm^2 for 30 minutes at 80°C.

Since a self-capping effect is present when curing with higher intensities, a weakly cured bulk is still present. This makes parameter measurements of large quantities of this material not a good representation of the actual material used for this model, since the model only takes into account structurally uniform geometries. The irradiated laser pulse will primarily interact with the surface of polysilane, although bulk parameters are mainly being measured in many of the measurement equipment. Therefore, when extracting the parameters that are necessary for the thermal simulations, care has to be taken not to confuse the results from the bulk with the results from the material surface.

4.3.1. ABSORPTION COEFFICIENT AND REFLECTION

Transmission, reflection and absorbance of polysilane has been measured using the Lambda 950 (PerkinElmer) spectrophotometer equipped with a total integrating sphere (TIS). The sample was prepared on a quartz substrate. The absorption coefficient for polysilane is 2.5·10^{5}cm^{-1} for the KrF wavelength of 248 nm, and is calculated using equation 3.1. Reflectance at this wavelength was found to be 10 %. The absorption spectrum and reflectance are shown in Fig. 4.5.

4.3.2. DENSITY

For the density of polysilane cured with 300 mW/cm^2 a value of 2.1 g/cm^3 is chosen. This is due to the strong similarity in both Raman as well as absorption spectra between

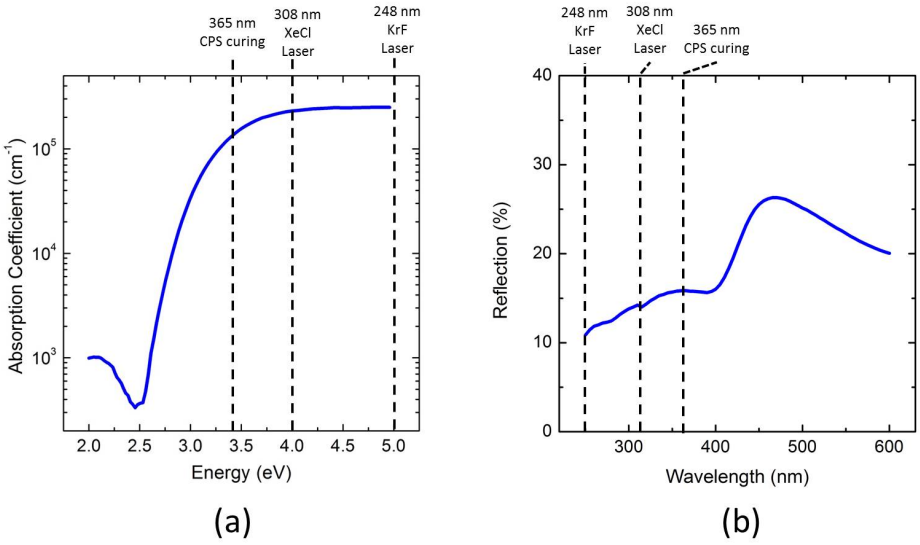

Figure 4.5: Absorption spectrum (a), and the Tauc plot of 200 nm thick polysilane cured with an intensity of 300 mW/cm^2 (b).

this sample and the sample created by Masuda et al. [7] which was annealed at 300°C, as was discussed in detail in section 3.2. The density for this sample was found to be approximately 2.0 to 2.1 g/cm^3.

4.3.3. HEAT CAPACITY

Heat capacity has been measured using differential scanning calorimetry (PerkinElmer DSC7), where a heated sample is monitored while being compared to an equally heated reference.

For these measurements 10 µL of CPS was poured into a small aluminum container and was cured for 30 minutes under 10 mW/cm^2 UV light. Subsequently the sample was cured with the stronger 300 mW/cm^2 UV light for 30 minutes at 80°C. The container was air-tight sealed and brought outside of the glovebox for measurements. Fig. 4.6 shows the results of the DSC measurements.

The initialization of the experiment caused the first heat capacity jump from 0 to approximately 1.6 J/gK close to room temperature. A thermal dependence was found when the temperature is further increased. This thermal dependence of heat capacitance is much stronger for the polymer (~1.11 J/kgK^2) than for a-Si(0.0917 J/kgK^2)[6]. The measurement range however, was limited up to 150 °C since the material would slowly transform into amorphous silicon for increasing temperatures as a result of cross-linking.

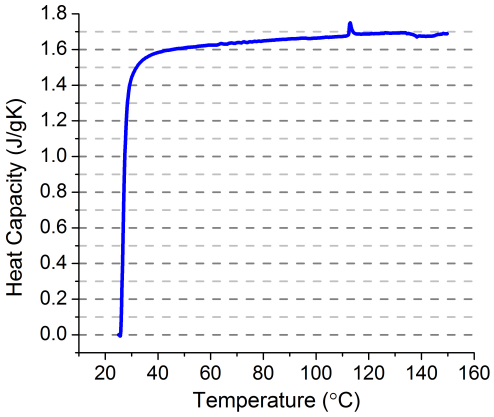

Figure 4.6: Differential scanning calorimetry measurements of polysilane.

Due to the slow temperature increment of the measurement setup of 10°C per minute, the gradual increase of the specific heat is likely a result of the change of material properties. The polysilane exposed to the laser light however, would rapidly heat up to over a 1000 K in a few nanoseconds, thus it will not have time to undergo the transition into a-Si, and a strong thermal dependence such as the one observed is unlikely to occur.

Polyethylene is similar to polysilane with the same monomer structure, but instead of silicon atoms as the molecular backbone, carbon atoms are present. Because it has a similar structure to polysilane, it will form a good reference for parameter comparison. The heat capacity of polyethylene is 1900-2300 J/kgK (high density-low density). The measured heat capacity of 1600 J/kgK is similar but lower due to two important reasons:

First, the polysilane found in the bulk of the measured content, is branched. It is more branched than the low density polyethylene[2] (2 % of carbon atoms[8] as opposed to approximately 20 % for polysilane[9]), which as a result would decrease the heat capacity of a polymer.

The second reason is that a high intensity curing treatment is employed to more strongly cross-link the top fraction of the measured polysilane. If this value is close to the one of a-Si (~980 J/kgK) the total value should be somewhat lower. A fixed heat capacity of 1600 J/kgK as observed from the DSC measurement results.

[2] In Chapter 2, work by Masuda et al.[7] revealed that polysilane branches approximately every 4 Si atoms. This result was however extracted from a sample cured with an intensity of 1 mW/cm^2 while in this work an intensity of 10 and subsequently 300 mW/cm^2 has been used, which would lead to a stronger cross-linking.

4.3.4. MELTING TEMPERATURE

In general the melting point of a material is strongly depending on its molecular structure. The molecular weight, spatial arrangement (packing density) and intermolecular interactions are key parameters in the melting point [10, 11]. As explained in Chapter 2, polysilane chain sizes vary from approximately 10^2 to 10^6 g/mol [9], and a precise melting temperature is therefore difficult to define a-priori. Cross-linking also plays a strong role and the the higher degree of cross-linking between the polysilane chains, the more it would behave as a-Si. Considering the heavily cured polysilane for these simulations, it has been concluded that the a-Si melting point of 1440 K is a reasonable assumption for the polysilane used in this work.

4.3.5. THERMAL CONDUCTIVITY

For the thermal conductivity of the material, it was difficult to make accurate measurements since the measurement setup requires a large amount of material which would make the curing treatment not feasible. Thermal conductivity is dependent on the type of bonds in the material, since heat is transferred through lattice vibrations and free electrons. The carbon counterpart of polysilane, polyethylene, has a thermal conductivity that varies between 0.4 to 0.5 W/(m·K), depending on its density. Polysilane used in this work is more branched and cross-linked compared to polyethylene which would increase the thermal conductivity since it approaches the 3D connectivity of a-Si, which has a conductivity of 1 W/(m·K). A thermal conductivity of 0.7 W/(m·K) has therefore been chosen.

A summary of the parameters used for polysilane is shown in Table 4.2.

Table 4.2: Parameters for thermal analysis of polysilane.

Parameter	Polysilane
Melting point (K)	1440
Density (g/cm^3)	2.1
Latent heat (J/g)	1320
Absorption coefficient (cm^{-1})	2.5e-5
Reflectivity	0.1
Heat Capacity (J/kgK)	1600
Thermal Conductivity (W/(m·K))	0.7

4.4. EXCIMER LASER ANNEALING SIMULATIONS FOR LIQUID SILICON

Different simulations have been analyzed and compared to the experimental results. First the different laser fluence effects have been observed while looking at the SEM and Raman measurements from the physical samples. Although, SEM images have only been taken from the samples on Si wafers, and Raman measurements have only been obtained from the samples on glass substrates, from the simulations no difference has been observed, due to the sufficiently thick SiO_2 buffer layer on top of the c-Si wafer.The model therefore considers only the sample on a glass substrate. The effects related to the variation of film thickness is also analyzed, since the doctor blade coating introduces a lot of these variations in the coated film. Although these simulations only reproduce the single pulse irradiations, multiple pulse cases are also discussed from the single pulse outcomes. Other effects that influence the simulation results are type of laser, type of starting material, and type of environment. Finally, short-comings of this model are presented.

4.4.1. LASER FLUENCE

Experimental results have indicated that the melting threshold of polysilane lies between 50 and 60 mJ/cm^2. Fluences around this threshold energy density have been simulated, that is: 40, 50, 60 and 70 mJ/cm^2. The simulation results are presented in Fig. 4.7. Both SEM images as well as Raman spectroscopy experimental data are compared to the simulation results.

At 40 mJ/cm^2 the film surface temperature increased to 1187 K in 23.7 ns. The melting temperature of 1440 K was not reached, therefore, no phase transition takes place. Accordingly, the SEM image shows no signs of morphological change, and the Raman spectrum shows a slight increase in the a-Si peak indicating an increase in cross-linking. Hydrogen and SiHx groups may also have ejected from the film at this energy density.

At 50 mJ/cm^2 the melting temperature of 1440 K has almost been reached with a temperature of 1411.7 K, also reached in 23.7 ns. At this temperature the material may have softened. A small change in surface morphology is visible in the SEM image showing a wavy texture. The Raman spectrum shows an increase in the a-Si peak, but no crystalline peak is observed. More hydrogen as well as silicon based radicals are removed after this treatment. At the same time cross-linking has improved. A porous a-Si structure as a result is left behind.

At 60 mJ/cm^2 the melting temperature has been reached in 16.7 ns. A further signifi-

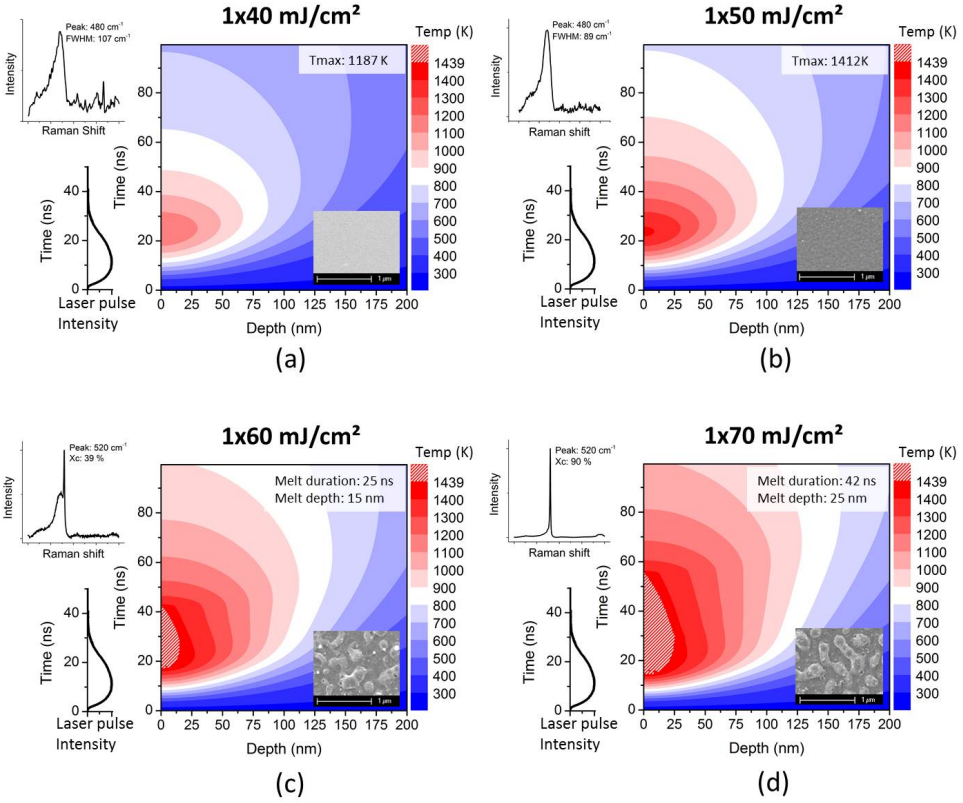

Figure 4.7: Transient heat simulation results of 200 nm polysilane exposed to a single KrF laser pulse with various energy densities: 40 mJ/cm^2 (a), 50 mJ/cm^2 (b), 60 mJ/cm^2 (c), 70 mJ/cm^2 (d). All samples have an associated SEM image and Raman measurement obtained from experimental data.

cant increase in temperature is prevented since the film melting absorbs heat(latent heat of fusion) at a constant temperature of 1440 K. The melt depth for this fluence is approximately 14.3 nm, and the melt duration is 26.2 ns. Surface morphology has significantly changed: bead shaped structures have formed from the agglomerating molten film. This is due to the minimization of the surface free energy of the liquid material. The Raman spectrum shows a visible crystalline silicon peak, with an amorphous silicon shoulder.

At 70 mJ/cm^2 the temperature of the surface does not further increase significantly due to the phase change, compared to the case of 60 mJ/cm^2. The melting point is reached in 14.2 ns, and the melt depth and duration both increased to approximately 23.6 nm and 39.3 ns respectively. The surface morphology is not much different from the 60 mJ/cm^2 case, but the Raman spectrum does show a much stronger c-Si peak due to the doubling of the melt depth.

Increasing the fluence further would lead to an even longer melt duration and larger melt depths that would lead to bigger crystal grains. In practice however, strong degassing and ablation effects have been observed, which adds to the increase in surface roughness. For transistor applications these effects are undesirable. A summary of the melt duration, time to melt, and melt depth results are presented in Fig. 4.8.

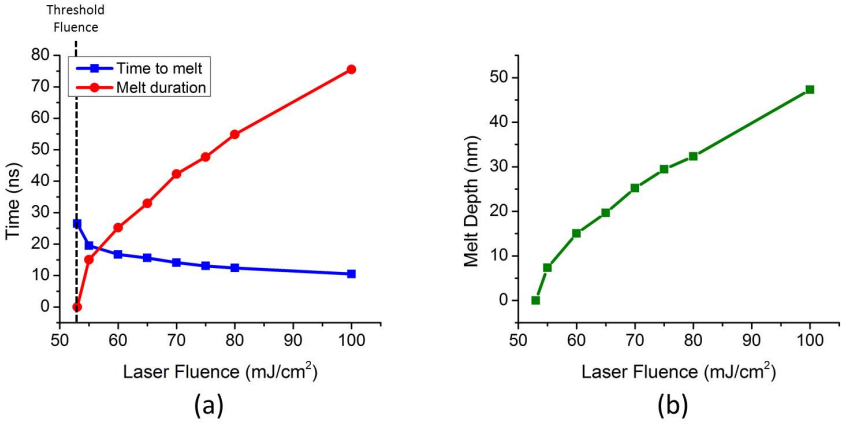

Figure 4.8: Simulation results regarding melt depth and melt duration.

These graphs suggest that the time to melt decreases with increasing laser fluence. This curve decreases and saturates to 11.2 ns which is the time necessary for the laser pulse to reach its peak. Substantial fluence increase is necessary to reach even faster times to melt. For the melt duration, a proportional increase to the laser fluence is visible. Finally, the melt depth also increases proportionally to the laser fluences, although from a certain energy the effect of the SiO_2 interface will start to play a role and will decrease the speed of melt depth progression. Explosive crystallization in these simulations have not been taken into account, and these would increase the actual melt duration and depth.

Compared to LPCVD a-Si simulations, the laser energy absorbed by the film is significantly higher due to the lower reflectance of the polysilane film (10% compared to 58 %). As a result, crystallization occurs at much lower laser fluences. A threshold fluence of 52 mJ/cm^2 was found for polysilane (69 mJ/cm^2 for LPCVD a-Si). In addition, the melt depth is larger, resulting a much larger crystalline fraction after the laser treatment. This indicates that an out-of-equilibrium transition from polysilane to polycrystalline silicon is in effect, and an intermediate transition to a-Si is unlikely to occur, since the properties for a-Si do not allow crystallization at such low fluences.

4.4.2. THICKNESS VARIATION

When thickness of the polysilane film reduces, the SiO_2 interface gets closer to the heated surface, allowing heat to transfer more easily to the substrate which cools the sample to a certain extent.

There is however a minimum polysilane thickness from which the threshold voltage does not change. This is because the thickness of the polysilane itself is sufficient to have no influence from the SiO_2 interface. The effect other than the threshold fluence, for higher energy densities, may still change depending on the film thickness. The simulation results of the threshold fluence associated to various polysilane thicknesses are presented in Fig. 4.9.

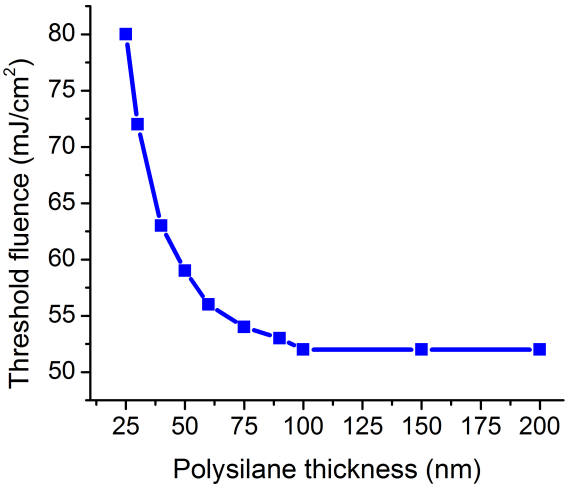

Figure 4.9: Simulation results of the excimer laser threshold fluence against the thickness of the polysilane.

The thickness of the polysilane material is therefore an important factor in the crystallization process. A non-uniform thickness leads to a variation in laser threshold fluences that lead to film inhomogeneity issues. The coating method used in this work however, is conducted fully manually, a variation in thickness is therefore common in these samples. Typically the thickness is approximately 100-150 nm, although liquid silicon film thickness may vary in extreme cases between a few tens of nanometers to approximately 400 nm, since higher thicknesses lead to film cracking due to accumulated stress. As a result, variation in crystallization has been observed in both SEM images as well as Raman measurements within a single laser spot.

4.4.3. MULTIPLE PULSES

The model that we has been used only accounts for single pulse situations. For multiple pulses however, a change in the starting material needs to be considered. For the case of high energy densities, the starting material changes to poly-Si, and the associated simulation properties change. Silicon with a higher crystalline fraction leads to a different type of material cooling after being molten, than pure a-Si. In these cases, after multiple pulses, the film will increase its crystallinity fraction.

Below threshold fluence levels however, experimentally it has been observed that for limited cases a transition is made from a-Si to p-Si, such as for the case of 50 mJ/cm^2. In the simulation, at 50 mJ/cm^2, the material did not receive sufficient energy to reach the melting temperature of a-Si. The reason behind its successful crystallization for multiple pulses, is that the first pulse changed the material properties. The rise in temperature from the initial pulse leads to hydrogen and radical evaporation from the material. The material stays in a solid phase losing part of its material. This means that the material that is left behind still has a similar thickness, although the porosity has increased. The reduction in density from 2.1 g/cm^3 to 1.9 g/cm^3 is simulated in Fig. 4.10. at 50 mJ/cm^2. Melting temperature for this lower density film is reached already at 50 mJ/cm^2 fluence. The 1.9 g/cm^3 comes from the measured density of thermally annealed polysilane at 350 °C. This density change may not be sudden, and it may therefore take more than a second pulse to crystallize the film, depending also on the material conditions. The simulation result shows that the melting temperature is now reached, in accordance to experimental results.

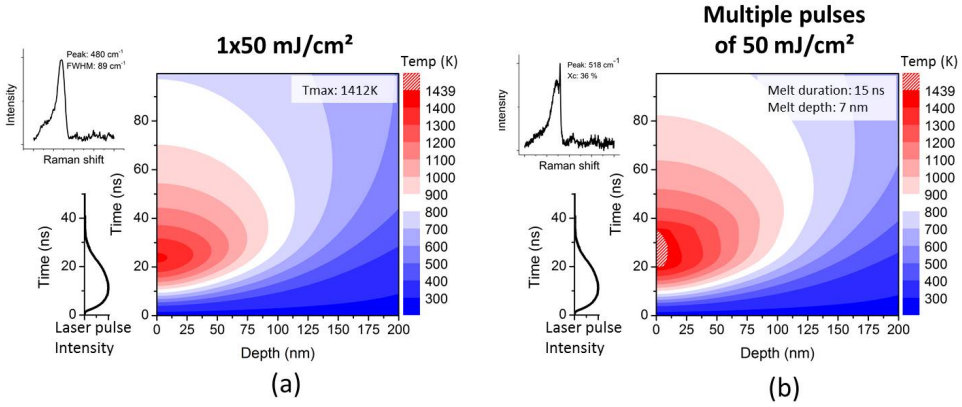

Figure 4.10: Transient heat simulation of a film exposed to a single pulse of 50 mJ/cm^2 (a), and multiple pulses of 50 mJ/cm^2 (b).

Other parameters however, may change as well although approaching a-Si would ultimately lead to a decrease in film temperature at a specific fluence. When density is decreased however, it is likely to assume that the material also reduces its thermal conductivity, which would increase the film heating. Absorption and heat capacity will decrease on the other hand, and lead to a decrease in film temperature. A well balanced combination should reach the melting point at 50 mJ/cm^2 that would reflect on the experimental results. As a first approximation however, a decrease in density suffices.

At even lower fluences however, the approach to the a-Si properties becomes dominant, and the film does not reach the melting temperature, due to increases in density, decrease in heat capacity, and increase in thermal conductivity. This is further explained in App. A.

4.4.4. OTHER VARIATIONS

Other system variations that could change the outcome of the experimental results as well as the simulation results are:

1. Laser type: In the simulation and experiments a KrF laser with a pulse duration of 20 ns has been used. Changing to XeCl which has a higher wavelength of 308 nm, will lead to an absorption of this light in a wider volume. This leads to a deeper crystallization, although higher fluences are required. A change in the pulse duration would have a similar effect. In addition, increasing the pulse duration would lead to a longer melt time, which would in practice lead to bigger crystal grains. Since the energy is now spread over a longer timeframe, the fluence will have to increase to reach the melting temperature.

2. Starting material: In this work, polysilane has been cured with an intensity of 300 mW/cm^2. If only a low intensity UV treatment is used, such as 10 mW/cm^2, the material will have different absorption properties. The degree of cross-linking is reduced, therefore, while the sample is heated, more of the material may evaporate during the laser treatment. As was also observed experimentally. Crystallization is reached at slightly lower fluences. When the starting material on the other hand is more severely cross-linked by means of a higher intensity UV light or temperature, the sample would approach a-Si quality, and crystallization will occur at higher fluence.

3. Environment: These simulations have accounted for a nitrogen environment. When the sample is treated however in vacuum, temperatures would significantly increase since there is no more convective cooling.

4.5. MODEL LIMITATIONS

The model that has been used could explain up to a certain extent the mechanism behind the polysilane crystallization process. A number of limitations to this model are however present and these need to be addressed:

Parameter data variation

A good simulation requires a careful parameter extraction of the materials used. Although absorption coefficient could be extracted in a way that represents the material used for our processes, for other parameter measurement types this becomes less accurate.

Some variation in the density extraction is present, since the curve used for extraction is based on scattered points. In addition, the density of an 300 °C annealed sample is used. Although the Raman spectrum shows similar results, at this temperature some of the radicals may already be evaporated. This evaporation is less in the high intensity UV cured case, and density could therefore be higher than the value used.

For the specific heat, a relatively large amount of material had to be used in a small container. For the weaker UV polymerization step, the chance of having a capping layer is limited and we can assume that the full contents of the container is polymerized. For the stronger UV source however, a capping layer would form leaving the bulk of the material unexposed. Heat capacity results would represent more closely the bulk polysilane material. The heat capacity of the surface of the polysilane which interacts with the excimer laser beam, could therefore be lower than the one measured.

Thermal conductivity has been approximated from a carbon-based counterpart which has similar bonding. Although in the polysilane case a stronger cross-linking and branching is present. A value that is therefore between the thermal conductivity of polyethylene (0.52 W/(m·K)) and a-Si (1 W/(m·K)) of 0.7 W/(m·K) was assumed, and this value could vary.

Outgassing/ evaporation

When the material is heated, outgassing and evaporation occur due to hydrogen and silicon radicals. This outgassing is accounted for by the decrease in density in the multiple pulse section, however, the model does not include the dynamic loss in energy due to this outgassing. On the other hand, matching with the experimental results shows that ELA is a thermal treatment, and is supported by the high temperatures reached by the samples.

Explosive crystallization

As a result of the latent heat produced by crystallization, temperature of underlying layers may increase over the melting point. This explosive crystallization has not been modeled, and an actual melt depth and duration may therefore be higher than the simulated results suggest.

Photochemical effect

The model only focuses on thermal effects from the UV laser light. However, the material also reacts to the UV light in a photochemical way. This was confirmed when the temperature of the sample was monitored during the LED UV curing.

4.6. CONCLUSIONS

Excimer laser annealing is used as a common process for crystallizing thin films while leaving the substrate unharmed. This is useful in thin film applications where the thermal budget of the substrate is limited. A good understanding of the physics behind this process is necessary. Using simulation software, this process can be monitored and predicted. A thermal mechanism was found to play an important role in the excimer laser annealing.

In this work, COMSOL multiphysics has been used with the time-dependent simulation module of heat transfer in solids. This model allows analysis at a continuum-level rather than molecules or atoms. Here a one-dimensional model is used to describe the effect of the laser treatment onto 200 nm of polysilane, on top of a glass substrate. An alternative substrate of Si with a buffer layer of 850 nm showed similar results to the simulations conducted on the glass substrate. As a reference, LPCVD a-Si ELA has been analyzed to compare to polysilane.

In order to construct an accurate model, parameters need to be extracted from polysilane. Physically, polysilane was prepared by first curing at a UV intensity of 10 mW/cm^2 for 30 minutes, and later curing at 300 mW/cm^2 for 30 minutes at 80°C. The higher intensity leads to a stronger cross-linking of the polysilane film. Experimentally, this led to a larger process window. The parameters that were extracted and deduced are: absorption, thermal capacity, thermal conductivity, density, and melting temperature.

Although polysilane transforms into an a-Si 3D network photochemically due to UV light, the thermal induced transformation from the excimer laser is overwhelming. The melting temperature is reached at relatively low fluences. Fluences of 40, 50, 60, and 70 mJ/cm^2 were analyzed, and compared to experimental data. The melting temperature is reached for fluences higher than 52 mJ/cm^2, and this was confirmed by the SEM images

by a change in morphology, and in the Raman spectra by a change in crystallinity. Compared to 200 nm LPCVD a-Si that has a melting threshold of approximately 69 mJ/cm^2, a much lower threshold was found, therefore it is unlikely that the polysilane material transforms into a-Si in an intermediate step.

Since uniformity is an issue in the manual doctor blade coating process, an analysis has been made on the effect of thickness variations. Thinner polysilane films have a closer interface to the oxide layer and therefore cool down more rapidly. As a result, higher fluences are needed in order to reach the melting temperature. This was also observed in the SEM images.

The model used in this work is primarily meant for single pulse treatments. Although for multiple pulse scenarios could be implemented by adjusting the starting material. It has been experimentally observed that for fluences slightly below the threshold, the film may crystallize after irradiating multiple pulses. The simulations revealed that it is reasonable to infer that the material after the first pulse, increases in temperature while not reaching the melting point. This temperature increase leads to evaporation of silicon and hydrogen radicals. The material that is left behind is porous, and after exposing the film with a lower density to the same fluence, the melting temperature is reached.

Other situations that were analyzed by simulations include, different laser types, a different starting material, and the excimer laser environment. A longer wavelength laser leads to a deeper absorption of the light, and the fluence must be increased to reach the same melting threshold. A longer pulse duration leads to a longer melting time, although the pulse energy density is spread over a longer timeframe and a higher fluence is again required to reach the melting threshold. Differently cured materials would heat in a different way, and an analysis of absorption, out-gassing, and similarities to a-Si need to be evaluated. The temperature significantly increases in the case of a vacuum environment, compared to a nitrogen environment due to convective cooling.

Limitations in this model consist of the accuracy in the parameters used for the polysilane in this model, as well as the focus on the thermal effect. This model does not account for energy lost in outgassing of the material, explosive crystallization, and the photochemical effect.

With these simulations we show that the polysilane laser crystallization process is thermally dominated, and that lower fluences are needed compared to conventional LPCVD a-Si.

REFERENCES

[1] N. H. Nickel, *Laser crystallization of silicon,* (Elsevier, 2003) Chap. Introduction to Laser Crystallization of Silicon - N.H. Nickel, pp. 1–9.

[2] R. Wood and G. Giles, *Macroscopic theory of pulsed-laser annealing. i. thermal transport and melting,* Physical Review B **23**, 2923 (1981).

[3] N. H. Nickel, *Laser crystallization of silicon,* (Elsevier, 2003) Chap. Modeling Laser-Induced Phase-Change Processes: Theory and Computation - R. Černỳ and Přikryl, pp. 43–76.

[4] P. van der Wilt, *Formation of Crystalline-Silicon Islands for Thin-Film Transistors by Excimer-Laser-Induced Lateral Growth*, Ph.D. thesis, Delft University of Technology (TU Delft) (2003).

[5] N. H. Nickel, *Laser crystallization of silicon,* (Elsevier, 2003) Chap. Heat Transfer and Phase Transformations in Laser Melting and Recrystallization of Amorphous Thin Si Fims - C. P. Grigorapoulos, S.-J. Moon, M.-H. Lee, pp. 11–40.

[6] J. Förster and H. Vogt, *Excimer laser-annealing of amorphous silicon layers,* Simulation **88**, 90 (2011).

[7] T. Masuda, Y. Matsuki, and T. Shimoda, *Pyrolytic transformation from polydihydrosilane to hydrogenated amorphous silicon film,* Thin Solid Films **520**, 6603 (2012).

[8] www.chemdot.com, *Polyethylene (pe),* online (2016).

[9] T. Masuda, Y. Matsuki, and T. Shimoda, *Characterization of polydihydrosilane by sec-malls and viscometry,* Polymer **53**, 2973 (2012).

[10] A. R. Katritzky, R. Jain, A. Lomaka, R. Petrukhin, U. Maran, and M. Karelson, *Perspective on the relationship between melting points and chemical structure,* Crystal Growth & Design **1**, 261 (2001).

[11] M. R. Kamal, L. Feng, and T. Huang, *A generalized equation for the prediction of melting temperatures of homopolymers and copolymers,* The Canadian Journal of Chemical Engineering **80**, 432 (2002).

5

Low Temperature Rigid Devices

In chapters 3 and 4, a new method is presented that allows silicon to be transformed from polymerized cyclopentasilane to polycrystalline silicon, directly on top of low thermal budget substrates such as paper. This film has also been characterized to determine its suitability for electronics, and the process has been analyzed by means of simulations. The next step is to observe the electric performance of this material by creating resistors and subsequently TFTs, which are used as the main building block for electronic circuits. As a first approach toward flexible liquid-silicon devices, they will be fabricated on top of a rigid silicon substrate, to allow the usage of conventional microelectronic processing equipment.

This chapter begins by explaining the tools that are used and the steps that are taken to fabricate the TFT on a silicon wafer at a maximum process temperature of 130 °C, in section 5.1. Because of the limited process temperature, a low temperature process for the oxide is investigated in section 5.2. Section 5.3 and 5.4 present the electrical measurement results of the fabricated resistors and TFTs respectively. Finally, in section 5.5, the chapter is concluded by summarizing the fabrication process and measurement results.

5.1. INTRODUCTION

Conventional silicon device fabrication requires vacuum processes, photolithography and high temperatures, all of which are undesirable for low-cost fabrication. Printing processes were found as an alternative that can simplify the process and increase the product throughput similar to those used in the graphics industry. At the same time, liquid silicon allowed printing of a solution that can later be converted to solid silicon. In this work, a new method was developed that allowed the usage of low-cost flexible substrates.

While material characterization gives an indication on the quality of the crystallized silicon, electrical characterization gives another, complementary, evaluation. Devices such as resistors and transistors give a good indication for this since these are commonly used elements for electronic circuits.

Although the final goal is the usage of solution-based silicon in electronics by a printing production on low thermal budget substrates, intermediate steps need to be taken in order to achieve this goal. Therefore, liquid silicon devices using the low temperature transformation are created on a rigid substrate with conventional microelectronic fabrication techniques at a limited thermal budget of 130 °C.

The limited temperature is needed to accurately judge the quality of the liquid silicon based poly-Si, since increases in temperature during the process may alter its performance, which would otherwise not occur in a temperature limited process. Potentially, such a process using conventional tools can in some cases be applied to low-cost, low-thermal-budget substrates such PEN or PET.

The implementation of poly-Si created at low temperatures in a conventional IC fabrication environment raises challenges. An alternative to some important steps is needed that would otherwise require higher temperatures. The thermal budget in this process was set to 130 °C, limited by photolithography.

5.1.1. TFT PROCESSING EQUIPMENT

The equipment used in this process is optimized for a 4" wafer. In this work an area of 52 dies of 1 cm^2 each, is defined. After every patterning and implantation step, all wafers are cleaned in 99% HNO_3 to remove organic contaminants. An additional cleaning in 69.5% HNO_3 at 105 °C is utilized to remove metallic contaminants for wafers without metallic patterns.

PHOTOLITHOGRAPHY

Patterning is performed by means of photolithography which is a subtractive process. An EVG 120 Coater-Developer is used to spin-coat positive photoresist (SPR3012) on the sample wafers. Hexamethyldisilazane (HMDS) is predeposited at 130 °C to improve photoresist adhesion. The tool has optimized rotational speed recipes for the desired photoresist thicknesses. In this work, photoresist thicknesses of 1.4 µm and 2.1 µm are typically used for the TFT fabrication process. A soft bake of 95 °C for 90 seconds follows the coating.

For the pattern exposure, an ASML PAS 5500/80 waferstepper is used with reticles suited for 1 by 1 cm dies. For 1.4 µm and 2.1 µm photoresist 130 and 165 mJ/cm^2 exposure energies were used, respectively.

Finally, after a post-exposure bake at 115 °C for 90 seconds, the exposed photoresist is dissolved for 57 seconds by the MF322 developer after which the remaining patterned resist is hard baked for 90 seconds at 100 °C. This concludes the photoresist patterned masking film, ready for etching, or implantation steps.

After etching the desired patterns through the openings of the photoresist mask, the resist is removed either by a 1000 W oxygen plasma ashing process with endpoint detection (PVA TePla 300) or by dissolution in acetone for 1 minute.

EXCIMER LASER: CRYSTALLIZATION AND DOPANT ACTIVATION

In this work, the excimer laser has played a key role in crystallizing liquid silicon directly on top of low thermal budget substrates. Its effects on liquid silicon have been thoroughly investigated in Chapters 3 and 4.

In order to create positive or negative type semiconductors, the silicon has to be doped. For this, the material undergoes a boron and phosphorus ion implantation treatment, respectively. This implantation causes damage to the silicon material, and moreover, the dopant ions are not electrically active since they have not replaced a silicon atom inside the lattice. Excimer laser annealing allows both the restoration of damage from the ion bombardment, as well as the activation of dopant ions.

IMPLANTATION: P AND B IONS

In order to insert dopants in the source and drain regions of the semiconductor, ions are implanted using the Varian Implanter E500HP. This step is conducted after gate deposition and therefore prevents ions from entering the silicon channel under the gate. As a result, self-alignment is induced. For p-type and n-type dopants, boron and phosphorus have been used respectively.

DEPOSITION: OXIDE AND METALS

SiO_2 is used in this process for both the gate-insulator, and as a passivation layer. Since conventionally, the deposition temperatures of these oxides exceed by far the 130 °C temperature budget, low-temperature oxide deposition processes are analyzed in this work. Specifically, two types of tools were used: atomic layer deposition (ALD)(FlexAl2, Oxford Instruments), and radio-frequency plasma-enhanced chemical-vapor-deposition (RF-PECVD)(AMIGO, Elettrorava).

For the gate, source and drain contact metals of the TFT, physical vapor deposition (PVD) has been used. Aluminum is deposited using the SPTS Trikon 204 Sigma Sputter-coater at 50 °C. Silicon spiking is prevented by saturating the Al target with 1% of silicon.

DRY ETCHING: ISLAND, METAL, AND OXIDE PATTERNING

The Trikon Omega 201 plasma etcher has been used to dry etch silicon island patterns from the crystallized liquid silicon film, and Al for the gates and metal contacts. The gases used for etching silicon and Al are Cl_2 and HBr at 500 W.

Oxide is etched using the Drytek Triode 384T plasma etcher for coarse oxide etching treatments at a power of 300 W with a soft landing step of 100 W for a fine etching treatment. C_2F_6 and CHF_3 gases are used in such etching process.

WET ETCHING: OXIDE AND METAL RESIDUE REMOVAL

In most patterning steps plasma etching is used to allow a good anisotropic patterning, although this comes at the cost of poor material selectivity. While wet etching is isotropic, the selectivity is very good. It is therefore used in this work for native oxide and aluminum residue removal.

Native oxide is removed by 4 minutes in 0.55% HF, after which either the gate-oxide or metal contact is deposited. For the Al residues that exist after dry-etching steps, a 30 second treatment of buffered aluminum etchant (65% H_3PO_4, 2% HNO_3, 14% CH_3COOH, and H_2O) also known as PES, is used.

5.1.2. LOW-TEMPERATURE TFT PROCESS STEPS ON A RIGID SUBSTRATE

As a starting substrate, 850 nm of PECVD TEOS SiO_2 is deposited at 350 °C on top of a 4" silicon wafer, to obtain a non-conductive surface, as well as a buffer layer. The maximum processing temperature of 130 °C for the device fabrication, allows the potential usage of low-thermal budget substrates with conventional processing equipment.

A detailed flowchart of this low-temperature TFT fabrication process is presented in Appendix B. The process steps are summarized in Fig. 5.1, and a brief description of these steps is presented below:

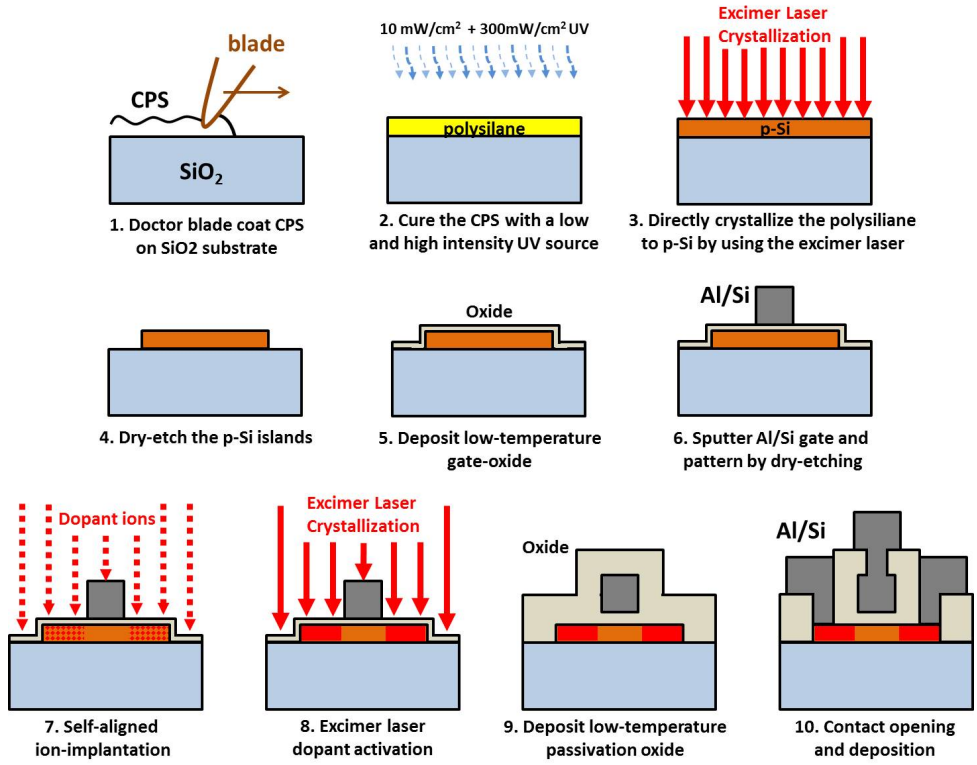

Figure 5.1: Low-temperature rigid TFT process flow.

Step 1: Coating

Using a polyimide doctor blade (as explained in sect. 3.1), 12.5 µL of pure CPS is coated on the wafer substrate, in an area of approximately 30 cm^2.

Step 2: Curing

The coated CPS is photopolymerized for 30 minutes by a UV light with an intensity of 10 mW/cm^2. Subsequently the film is cured for 30 minutes with a UV light with an increased intensity of 300 mW/cm^2 at 80 °C. After the latter curing treatment, the film turns slightly yellow.

Step 3: Crystallization

The KrF excimer laser is used to directly crystallize the polysilane. Various energy fluences and numbers of pulses can be applied.

Step 4: Island etching

T-bone shaped silicon channel patterns are dry-etched in the crystallized film.

Step 5: Gate-oxide deposition

After the removal of native oxide by a 0.55% HF dip, a 50 nm thick gate-oxide is deposited at temperatures around 100 °C using either RF-PECVD or ALD.

Step 6: Gate deposition and patterning

A 675 nm thick Al is deposited by sputtering and subsequently patterned by dry-etching to form the gate electrode.

Step 7: Ion implantation

Self-aligned ion implantation by the gate-metal allows dopant ions to enter the semiconducting film outside of the channel area. For the p-type, boron is used at 17 keV with a dose of $3{\cdot}10^{15}$ at/cm^2. For the n-type, phosphorus is used at 50 keV with a dose of $2{\cdot}10^{15}$ at/cm^2.

Step 8: Dopant activation

The implanted dopants are activated using the excimer laser once again, at an energy fluence below crystallization levels. 20 Pulses of 50 mJ/cm^2 have been used.

Step 9: Passivation

The silicon island and gate patterns are passivated with an 800 nm thick RF-PECVD SiO_2, deposited at 120 °C. This protects the gate from wet etching steps.

Step 10: Contact opening and deposition

Al/Si contacts of 1.4 µm thickness are created after etching the passivation oxide.

5.2. LOW-TEMPERATURE SILICON OXIDES

SiO_2 is used in the TFT process both as a gate insulator as well as the passivation layer. The material is preferred over other oxide types due to favorable interface properties with the silicon island [1].

Generally, high quality oxides are prepared at high temperatures and have good chemical stability as well as electrical passivation. In the case of thermally oxidized silicon wafers, temperatures of around 1000 °C are used to grow SiO_2 on the Si wafer surface by using oxygen or water vapor. Since the speed of this process is depending on the diffusivity of the oxygen or water molecules, growth of oxides of sufficient thicknesses can only be employed at these high temperatures.

On the other hand, oxides can also be deposited, in which case the temperature can be significantly reduced. Low pressure chemical vapor deposition (LPCVD) allows a deposition of SiO_2 at temperatures of around 650 °C. By using a plasma enhancement, the

temperature can be further reduced to approximately 350 °C. The process is known as plasma-enhanced chemical vapor deposition (PECVD).

The electric insulating performance of PECVD SiO_2 deposited at 350 °C was found to be of sufficient quality for the gate insulator for some reported works[2, 3]. In this work however, a temperature of 350 °C is still too high, and an oxide deposition process at temperatures around 100 °C is required.

Atomic Layer Deposition (ALD) is a tool that can deposit at these low temperatures. It is based on the sequential construction of atomic monolayers which, as a result, leads to good conformity on non-smooth surfaces. At temperatures below 300 °C the dielectric performance deteriorates significantly, and must be improved by a post-annealing step [4, 5].

An alternative low-temperature oxide deposition method is the radio-frequency PECVD (RF-PECVD). SiO_2 may be deposited at a temperature of 120 °C. Through optimization of process gases, pressure, power, and temperature, the tool can deposit oxides with good electrical as well as chemical insulation and has been used for solar cell applications [6].

Generally, a deposition of an oxide is followed by an annealing step in a hydrogen ambient to passivate fast surface states [5, 7, 8]. This significantly improves the dielectric performance of the oxides, especially for those that are deposited at low temperatures. However, in this work, such an annealing cannot be performed and the effect of omitting such a step must be evaluated.

5.2.1. OXIDE CHARACTERIZATION

In order to analyze the properties of different low temperature oxides, MOS capacitors have been fabricated and measured. These are devices that are not commonly used in ICs but are powerful tools for extracting the characteristic oxide parameters and judging its performance [9, 10]. The structure of a MOS capacitor is shown in Fig. 5.2 a.

Depending on the voltage applied on the metal, a certain capacitance is formed by this electrode and the charges in the semiconductor. When the applied voltage causes the semiconductor to operate in accumulation (e.g. majority carriers to collect at the Si-SiO_2 interface), two conducting plates are separated by the oxide layer.

For a p-type semiconductor, the majority carriers are holes. Consequently, when the applied voltage is increased, the charge inside the semiconductor is repelled from the oxide interface, and a layer depleted of charge carriers will develop. This depletion layer will form a series connection to the original oxide, and reduce the overall capacitance of the total system.

A further increase in applied voltage may even cause an inversion layer to form at

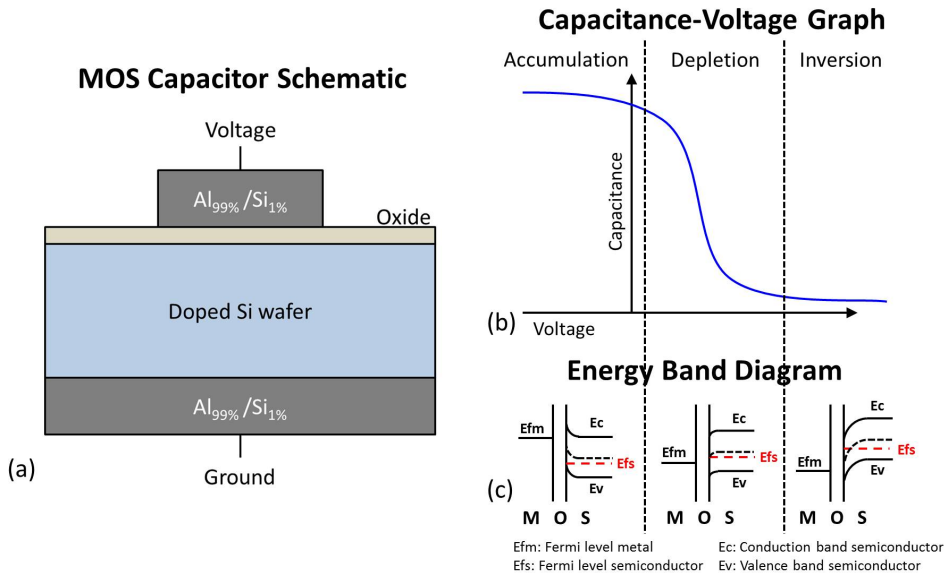

Figure 5.2: Illustration of MOS capacitor structure (a), sample CV curve (b), and the associated band diagram for the capacitance conditions (c).

the Si-SiO_2 interface. This change in capacitance as a function of voltage (CV) can give useful information about the quality of the oxide in terms of fixed and mobile charges. The three conditions are displayed in a CV curve in Fig. 5.2 b, and the respective band diagrams are shown in Fig. 5.2 c.

A number of parameters are extracted from the CV measurements that allow the quality of the oxides to be judged:

Relative Permittivity, ε_r

The relative permittivity for high quality SiO_2 is approximately 3.9. Deviations from this value show imperfections in the produced silicon oxide layer [4, 11]. It can be extracted from the CV curves by applying the following equation:

$$\varepsilon_r = \frac{C_{ox}\, t_{ox}}{\varepsilon_0 A} \tag{5.1}$$

where C_{ox} is the oxide capacitance obtained from the MOS capacitor operation in accumulation, t_{ox} the oxide thickness, ε_0 the vacuum permittivity ($8.85 \cdot 10^{-12}$ F/m), and A the area of the capacitor plate.

Fixed Oxide Charge, Q_f

The fixed oxide charge can be calculated after extracting the flatband voltage from the CV curve. The flatband condition is the result of a certain bias voltage (flatband voltage) applied to the metal, that would allow the energy band at the semiconductor-oxide interface to be flat. This means that the electric field at the semiconductor surface is zero [10].

Ideally, the flatband voltage is the result of the work function difference of the metal and the semiconductor in the MOS capacitor structure. Fixed charges in the oxide however cause a shift of this ideal voltage. The distribution of this fixed charge inside the oxide is unknown, and therefore a quantitative comparison is not possible, only relative. It is however, reasonable to assume that the bulk of the fixed charge is located at the Si-SiO_2 interface.

The flatband voltage can be read out of the CV curve by calculating the ideal flatband capacitance (C_{FB}) based on the series oxide and depletion capacitance and the Debye length [7, 9], by the following equation:

$$C_{FB} = \frac{C_{max}}{1 + \frac{(C_{max}/C_{min})-1}{2\sqrt{ln(|N_A - N_D|/n_i)}}} \tag{5.2}$$

where C_{max} is the maximum capacitance, also known as the oxide capacitance C_{ox}, C_{min} the minimum capacitance which is the series total of the oxide and depletion capacitance, N_A and N_D the acceptor and donor concentrations in the semiconductor, respectively, and n_i is the intrinsic carrier concentration of the semiconductor.

In this work, the acceptor concentration of P-type silicon wafers used are in the order of 10^{15} cm^{-3}. n_i for silicon is $1.5{\cdot}10^{10}$. After extracting the flatband voltage from the CV curve, the amount of fixed charges (Q_f) can be calculated by:

$$Q_f = \frac{C_{ox}}{A}(W_{MS} - V_{FB}) \tag{5.3}$$

where W_{MS} is the difference of the metal and semiconductor work functions. The value of this for aluminum and a p-type silicon wafer, is -0.9 V.

Trapped Charge, Q_t

A hysteresis effect of the CV-curve may be observed when sweeping the voltage in the positive and negative directions. This is due to charges being trapped as a

result of the applied voltage [12]. The amount of trapped charges can be extracted from the shift in flatband voltage by:

$$Q_t = \frac{C_{ox}}{A}(\Delta V_{FB-hyst}) \tag{5.4}$$

where $\Delta V_{FB-hyst}$ is the difference in flatband voltage as a result of the bidirectional sweep.

CV measurements could also be used to extract other important parameters, however these are impractical for the oxides aimed at in this work. Mobile charges for instance can be extracted by a bias stress test, for which a thermal cycle of 200 °C under a gate bias is necessary [7]. This temperature may alter the performance of the low-temperature oxides and will give an inaccurate representation of the mobile charge results since the temperature is never reached in the TFT fabrication process.

Fast surface states and interface trap states require the results of a quasistatic (low-frequency) CV measurement [7, 8]. These cannot be extracted with the silicon wafers used today due to the high quality of the semiconductor material and the requirement of a thermal generation of minority charge carriers. As a result, at low frequencies, the charges cannot respond to the alternating signal. At even lower frequencies, the capacitive current becomes too low to be accurately read out. Low frequency CV measurements today have therefore lost their practical meaning [10].

A final key oxide parameter is the breakdown electric field (E_{BD}). It is measured by observation of the applicable voltage over a certain oxide thickness before the MOS device breaks down. This value needs to be sufficiently high for TFT operation.

5.2.2. OXIDE MEASUREMENT RESULTS

Four different oxides are analyzed. As a reference, PECVD TEOS SiO_2 deposited at 350 °C is used. RF-PECVD and ALD SiO_2 deposited at 120 and 100 °C, respectively, are analyzed as low temperature silicon oxide alternatives. Additionally an ALD stack of 12.5 nm SiO_2 and 30 nm Al_2O_3 deposited at 100 °C is analyzed due to the increase in oxide performance as presented by Dingemans et al. in [5].

For every oxide type, three curves are plotted: a first measurement curve, a curve extracted after repeated measurements, and a curve swept from the opposite voltage direction. These high frequency (1 MHz) CV curves of the respective oxide types are plotted in Fig. 5.3. The repeated measurements give a reproducible result and incorporates charge movement from bias stressing. From the repeated measurements curves, oxide parameters have been extracted and presented in table 5.1.

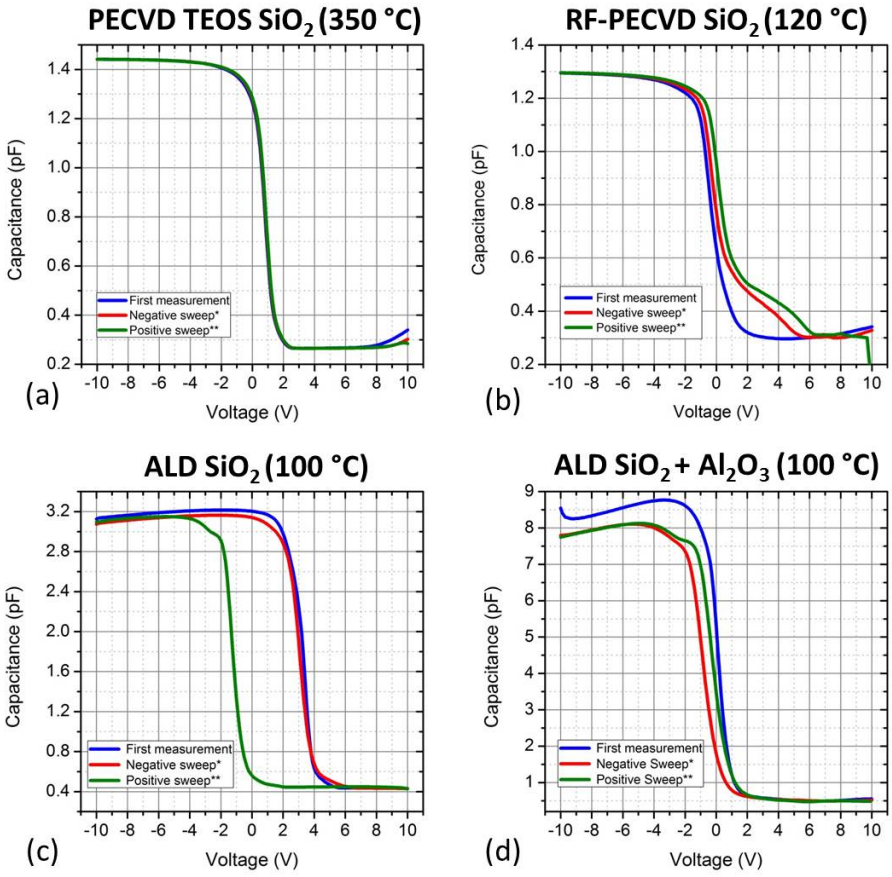

Figure 5.3: Capacitance to voltage measurements for four different types of oxides: PECVD TEOS SiO_2(a), RF-PECVD SiO_2(b), ALD SiO_2(c), ALD SiO_2 + Al_2O_3(d). Each displaying three curves: first measurement (blue), repeated measurements (red), and opposite voltage sweep (green).

Table 5.1: Summary of reference and low temperature oxide performance, with best and worst indications.

	PECVD TEOS SiO_2	RF-PECVD SiO_2	ALD SiO_2	ALD $SiO_2 + Al_2O_3$
ε_r	4.4	3.9	7.1	15.6
ΔV_{FB} (V)	-1.7	-0.7	-4.1	-0.6
Q_f(e/cm^2)	-6.1·10^{11}	-2.3·10^{11}	-1.6·10^{12}	-1.2·10^{12}
$\Delta V_{FB-hyst}$ (V)	0.02	0.37	4.55	0.63
Q_t(e/cm^2)	7.2·10^9	1.2·10^{11}	3.6·10^{12}	1.3·10^{12}
E_{BD} (MV/cm)	10.7	13.1	12.5	4.4

Based on the measurement results, the best performing low temperature oxide was found to be the RF-PECVD SiO_2. In some aspects this oxide outperformed even the PECVD TEOS oxide deposited at 350 °C.

Its relative permittivity of 3.9 is identical to thermally grown, high quality, SiO_2. In addition, the amount of fixed and trapped charge of -2.3·10^{11} e/cm^2 and 1.2·10^{11} e/cm^2 are the lowest compared to other low-temperature deposited oxides. The breakdown field of 13.1 MV/cm was also the highest.

Regarding the other oxides, the relative permittivity of ALD SiO_2 is 7.1, which is much higher than the theoretical value of 3.9. This increase can be attributed to polarizable moieties inside the film (-OH) [4, 11], which generally reduce after an annealing treatment. The relative permittivity of the stacked oxide is even higher due to the Al_2O_3 which has a higher dielectric constant of approximately 10.

Another important observation from the CV-curves are the differences between the first measurement, repeated measurements and the measurement with a change in sweep direction. The PECVD TEOS oxide shows a relatively stable oxide performance, while the low-temperature oxides show deviations. A rather large flatband voltage shift was observed for the ALD SiO_2 of almost 5 V.

Omission of an annealing treatment has strong detrimental effects on the low-temperature ALD oxides when comparing to the work done by Dingemans et al. [5]. For the purposes of this work however an annealing step must be omitted and when comparing the low-temperature oxides with one another, the RF-PECVD oxide is the most promising.

5.3. LOW-TEMPERATURE POLY-SI RESISTORS

Some important parts of the TFT fabrication process are subject to optimization. One area of optimization is regarding the doping of the source and drain regions. A sufficiently high doping is necessary in order to have low enough source and drain resistances, but moreover to have a sufficient supply of charge carriers for the TFT operation. For this purpose, P- and N-type resistors have been fabricated.

In order to avoid the inclusion of contact resistance, a four-point probe (Kelvin method) measurement has been performed. This is done by placing the four probes in a Greek cross arrangement as shown in Fig. 5.4. Current is injected and collected by two probes on one side of the cross, and the differential voltage is measured over the two probes on the opposite side.

For the calculation of the resistivity the following formula is applied:

$$\rho = \frac{\pi}{\ln 2} t \frac{V_1 - V_2}{I} \tag{5.5}$$

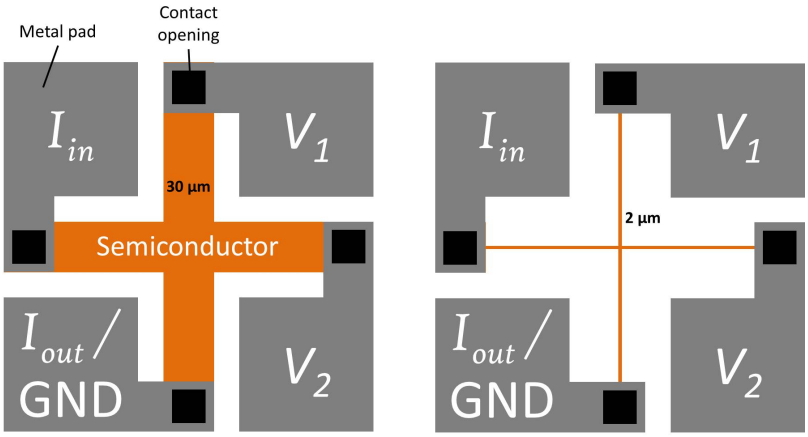

Figure 5.4: Greek-cross resistors used in this work with resistor beam widths of 30 and 2 µm.

where ρ is the resistivity of the material, $\frac{V_1-V_2}{I}$ is the measured resistance, t the film thickness and $\frac{\pi}{\ln 2}$ the correction factor. This factor is used to correct for the radial current flow from the probe tip, the limited sample thickness, lateral dimensions, and the distance from the probe to the edge of the resistor. The reader is referred to [13] for a more detailed explanation of the applicable correction factor.

The doping conditions were the same as described in section 5.1.2: for the p-type, boron is implanted at 17 keV with a dose of $3{\cdot}10^{15}$at/cm^2, and for the n-type, phosphorus is implanted at 50 keV with a dose of $2{\cdot}10^{15}$at/cm^2. These conditions were optimized from simulation results.

From the resistor measurement results, the resistivity can be calculated. Since the exact thickness could not be extracted for the specific samples, a thickness ranging from 50 to 150 nm is assumed. Depending on the thickness the resistivity changes. The lowest values obtained are 10-30 mΩcm and 0.2-0.6 Ωcm for the N- and P-type resistors respectively. The measurement results are shown in Fig. 5.5a and b, respectively.

From the measured resistivities, the doping concentration can be approximated by curve shown in Fig. 5.5. The obtained resistivity values are at least an order of magnitude higher than expected of an ideal poly-Si doping case, where resistivities are in the order of mΩcm. The following are some of the reasons for their lower performance. Optimization can help reduce these effects and give lower doped silicon resistivities.

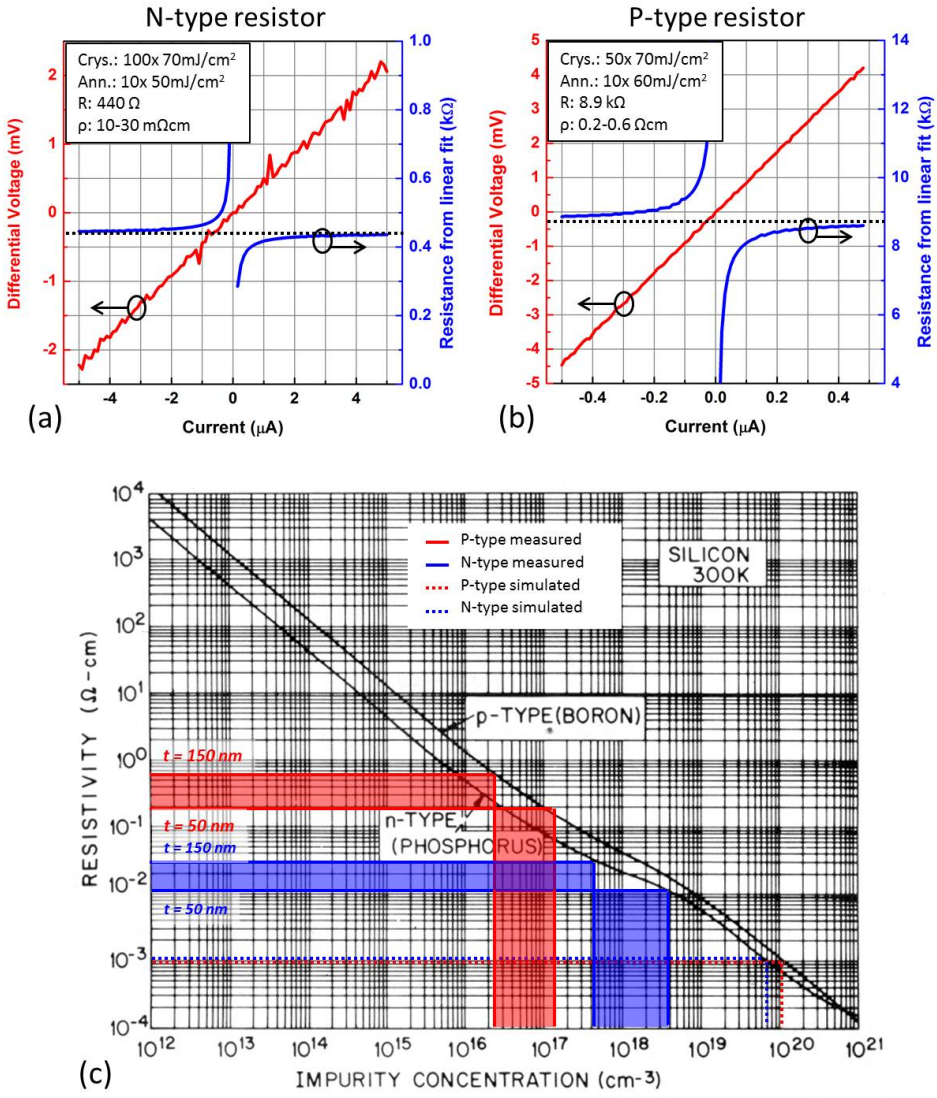

Figure 5.5: Resistivity to doping concentration graph[14], red and blue solid lines indicate the lowest measured resistivities for the p- and n-type resistors. The dotted lines indicate the simulated ideal values.

1. Different material

The indicated black lines in the graph are associated with the doping of high quality crystalline silicon. For the material crystallized in this work the crystal sizes are much smaller (in the order of nanometers). As a result, the position of these lines will differ to some extent.

2. Ion Implantation simulation

Simulation results revealed a proper doping in a system where 50 nm of SiO_2 on top of 150 nm of poly-Si was used. Deviations from these ideal materials are present, therefore the suggested implantation profile will be different.

3. Dopant Activation

The activation laser recipe of 10 pulses of 50 mJ/cm^2 and 10 pulses of 60 mJ/cm^2 may be insufficient to fully activate the implanted dopant ions. Either more pulses, a higher fluence or a combination of the two may improve the level of activation.

4. Laser spot uniformity

Deviations from the aimed laser fluence has an impact on both the crystallization as well as the dopant activation. Depending on the location within the laser spot, different performing devices have been observed.

5. Thickness

Due to the manual doctor blade coating process, uniformity in thickness is an issue. It is also difficult to accurately evaluate the actual thickness of the film. For the resistivity calculation a thickness ranging from 50-150 nm has been evaluated. Variation in this thickness not only has an effect on the calculated values, but also on the crystallinity threshold energy, as well as the dopant activation energy. Optimization in this case can only be performed once a uniform and reproducible thickness can be realized.

5.4. LOW-TEMPERATURE POLY-SI TFTS

Solution processed silicon based poly-Si TFTs have been fabricated at a maximum process temperature of 130 °C on a silicon substrate. As was discussed in the previous chapters, different excimer laser conditions lead to a variety of crystallization results. In order to compare the different device performances, the transistor transfer characteristics were analyzed [15].

To obtain the transfer characteristics, the transistor source is grounded, and the drain is kept at a relatively low absolute voltage of 0.5 V to be able to define the drain current I_{DS} in the linear regime. The voltage at the gate of the transistor is manipulated, as a result the drain current changes and is defined by the following equation:

$$I_{DS} = \mu_{FE} C_{ox} \frac{W}{L}((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}) \tag{5.6}$$

where μ_{FE} is the field effect mobility, C_{ox} the gate oxide capacitance per unit area, $\frac{W}{L}$ the

channel width over length ratio, V_{GS} the voltage applied at the gate, V_{th} the transistor threshold voltage, and V_{DS} the voltage applied at the drain.

Since only the gate is varied, an expression can be given for the transconductance:

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} |_{V_{DS}=0.5V} \tag{5.7}$$

where g_m is the transconductance, taken as the slope of the drain current to gate voltage, having the drain voltage fixed at a value of 0.5 V. The maximum value of transconductance can be used to calculate the maximum field effect mobility. This value indicates the switching speed of the transistor. Combining the two aforementioned equations the mobility can be calculated by:

$$\mu_{FE} = \frac{g_m}{C_{ox}\frac{W}{L}V_{DS}} \tag{5.8}$$

Other parameters that are extracted from the transfer curves are:

Threshold voltage (V_{th})

The threshold voltage value defines the minimum gate voltage necessary to form a well-defined conducting channel under the gate. This value is extracted from the linear transfer curve, in the region that the current increases linearly. An extrapolation of this slope to the voltage axis defines the threshold voltage. A value close to 0 V is generally desired to reduce the power consumption of transistors.

Subthreshold voltage swing (S)

The minimum amount of voltage necessary in order for the current to increase by a factor of 10 is defined as the subthreshold voltage swing. This value is found below the threshold voltage and also indicates the switching speed of the device.

Current range (I_{on}/I_{off})

The range of the drain current is another key transistor parameter. Generally this value is taken from the maximum drain current divided by the minimum drain current and is defined in orders of magnitude. The devices fabricated in this work however have moments where the drain current changes direction (e.g. becomes negative), which makes the on/off current ratio not as accurate as in conventional transistors. Three values are therefore used to be able to compare the devices in this work: maximum drain current (I_{max}), on/off ratio where "off" is defined as $V_{GS} = 0V$, and where "off" is defined as the absolute minimum current readout from the transfer plot.

Crystallization conditions of single and multiple pulses of 50, 60 and 70 mJ/cm^2 were analyzed. The best results were obtained by a laser fluence of 70 mJ/cm^2. The 70 mJ/cm^2 transfer curves of PMOS and NMOS TFTs are plotted for 100 pulses and single pulse crystallization, respectively, in Fig. 5.6. Dopant activation conditions for all devices were 20 pulses of 50 mJ/cm^2.

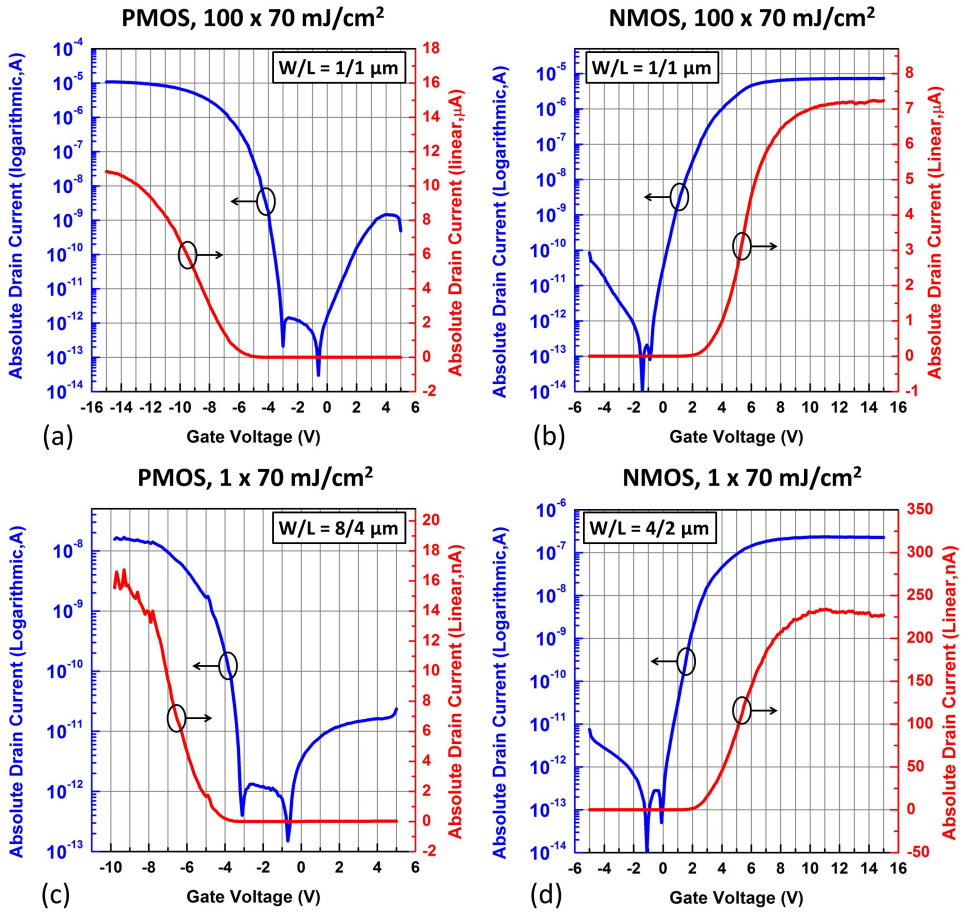

Figure 5.6: Transfer curves in linear (red) and logarithmic (blue) scale of 100 pulses of 70 mJ/cm^2 crystallized PMOS (a), NMOS (b), and single pulse of 70 mJ/cm^2 crystallized PMOS (c) and NMOS (d) TFTs.

The typical output characteristics for a PMOS and NMOS device that have been crystallized by a fluence of 70 mJ/cm^2 is plotted in Fig. 5.7. Short channel effects and current crowding is visible in these plots. These results confirm that the chosen drain voltage of 0.5 V for the transfer curves was low enough for the device to operate in the linear

regime, and therefore for the associated formulas to be applied.

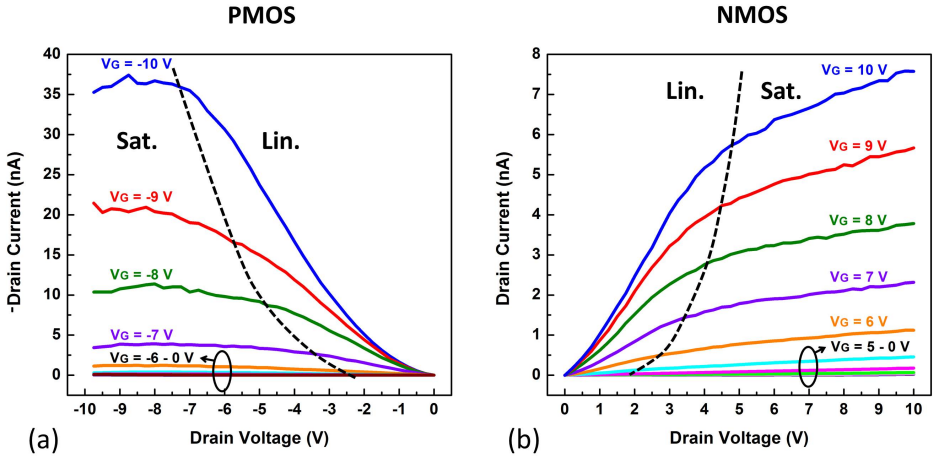

Figure 5.7: Output curves of multiple pulse crystallized poly-Si TFTs: PMOS (a), and NMOS (b).

Table 5.2: Performance summary of liquid silicon based poly-Si TFTs on a silicon substrate.

	Multiple pulse PMOS	Multiple pulse NMOS	Single pulse PMOS	Single pulse NMOS
μ_{FE} (cm^2/Vs)	87.7	91.5	0.21	1.44
V_{th}(V)	-6.5	3.5	-5.0	3.0
S(mV/dec)	177	164	140	190
I_{max} (A)	$1.1{\cdot}10^{-5}$	$7.3{\cdot}10^{-6}$	$1.7{\cdot}10^{-8}$	$2.3{\cdot}10^{-7}$
$\log(I_{on}/I_{0VG})$	6.9	5.4	3.7	6.2
$\log(I_{on}/I_{min})$	8.6	8.9	5.0	7.3

A summary of the device performance is presented in table 5.2. A number of important conclusions can be made from the measurement results:

1. Single and Multiple Pulses

When analyzing the crystallinity a difference is observed for a single pulse and for multiple pulse crystallization. Above the threshold fluence for crystallization, in general, a thicker crystallization thickness was obtained when exposing polysilane to multiple pulses of the same laser fluence. For the TFT performance a clear difference in terms of mobility and yield was observed. The mobility increased by approximately two orders of magnitude, while the difference in yield increased from 40 to 80 percent. As observed by the TEM images, the crystal uniformity was

much better for multiple pulses, while single pulse crystallization also leads to areas where crystal growth is limited or absent.

2. Fluence

From the measurement results when comparing 50, 60, and 70 mJ/cm^2 fluences, the best performing devices were observed for the 70 mJ/cm^2 condition. This is mainly due to the larger grain sizes or overall crystalline film thickness. The crystallization threshold for this batch may have shifted as a result of a thickness variation, compared to what was simulated. Multiple pulses of higher fluences may result in a further increase in TFT performance. Ablation effects however need to be taken into consideration.

3. PMOS and NMOS

Mobilities and levels of current for P- and N-type devices exposed to the same crystallization and dopant activation conditions are similar. The main difference that was observed is the level of threshold voltage. For the P-type device this value was in absolute terms higher. A reduction in the threshold voltage can be achieved by optimization of doping levels, oxide performance, or reduction in thickness of the oxide.

4. Negative I_D

At high negative gate voltages, a portion of the current flows into the gate. At high positive gate voltages, a part of the current flows through to the channel. The drain current has a brief moment where it reverses its direction with a current in the sub-picoampere. This is due to the dominating leakage current entering through the gate.

5. Laser Spot Uniformity

Within every laser spot, a matrix of TFTs were fabricated. Inhomogeneities in the laser spot may cause a variation in crystallization and consequently a variation in device performance. By comparing different TFTs within a laser spot, it was found that the top half of the spot led to better performing TFTs than the bottom half. To prevent this variation, the spot uniformity should be optimized, or a scanning laser recipe may be used.

5.5. CONCLUSIONS

Solution-processed polycrystalline silicon TFTs have been successfully fabricated using a process that is limited to a maximum temperature of 130°C with conventional micro-

electronic processing equipment. A maximum temperature of 130 °C is sufficient for inexpensive substrates such as PET, PEN or paper, showing the potential of this material to be used on such substrates.

In order to achieve the low temperature process with conventional microelectronic fabrication tools one critical process that needed to significantly reduce its production temperature, is the oxide. Three types of low-temperature oxides were analyzed by creating MOS capacitors. These are RF-PECVD SiO_2 deposited at 120 °C, ALD SiO_2 deposited at 100 °C, and a stack of ALD SiO_2 with Al_2O_3 deposited at 100 °C.

The RF-PECVD oxide showed the best performance out of the three: The relative permittivity of 3.9 is theoretically ideal, the fixed and trapped charges of -2.3·10^{11} e/cm^2 and 1.2·10^{11}, respectively, were also found to be the lowest among the low temperature oxides. Finally, the breakdown field of 13.1 MV/cm was the highest.

For the electronic devices, polysilane was crystallized with fluences of 50, 60, and 70 mJ/cm^2 and numbers of pulses ranging from 1 to 100.

Kelvin resistors that have been fabricated by this process performed best when exposed to multiple pulses of 70 mJ/cm^2. The lowest resistivity obtained for the N-type resistor was 10-30 mΩcm, and for the P-type resistor this was 0.2-0.6 Ωcm, depending on the film thickness ranging from 50 to 150 nm. The resistivities were higher than those simulated due to a number of reasons such as: the difference in silicon quality, the mismatch between simulated materials and the materials at hand, insufficient dopant activation, and uniformity issues in laser and material thickness.

The best performing TFTs were observed for a crystallization condition of 100 pulses of 70 mJ/cm^2. Mobilities of 87.7 and 91.1 cm^2/Vs for the PMOS and NMOS TFTs respectively. Single pulse crystallized TFTs, using the same fluence, showed significantly lower mobilities of 0.21 and 1.44 mJ/cm^2, respectively. Yield for a single pulse case was also reduced from 80 to approximately 40 %. The reason behind this lies in the way the film is crystallized, for a single pulse case, the grain formation is scattered, whereas for multiple pulses a fine collection of grains form a relatively uniform film. Fluences above 70 mJ/cm^2 may perform better, although ablation has to be taken into consideration.

PMOS devices have shown a slightly higher absolute threshold voltage, which can be optimized by the doping conditions, improving the oxide performance, or by reducing the oxide thickness. The drain current changed its direction for certain gate voltage conditions at a level of sub-picoampere, due to the dominating gate leakage. Laser spot uniformity was found to play an important role in the reproducibility of the device performance within a single spot area.

The obtained TFT results are far higher than those obtained by solution based al-

ternatives such as organic and metal-oxide semiconductor TFTs. It shows the potential of the liquid silicon material produced at temperatures sufficiently low for low-thermal budget substrates. The next step would be to fabricate these devices on such substrates.

REFERENCES

[1] G. D. Wilk, R. M. Wallace, and J. Anthony, *High-κ gate dielectrics: Current status and materials properties considerations,* Journal of applied physics **89**, 5243 (2001).

[2] J. Zhang, R. Ishihara, H. Tagagishi, R. Kawajiri, T. Shimoda, and C. Beenakker, *Single-grain si tfts using spin-coated liquid-silicon,* in *Electron Devices Meeting (IEDM), 2011 IEEE International* (IEEE, 2011) pp. 14–5.

[3] J. Zhang, M. Trifunovic, M. Van Der Zwan, H. Takagishi, R. Kawajiri, T. Shimoda, C. Beenakker, and R. Ishihara, *Single-grain si thin-film transistors on flexible polyimide substrate fabricated from doctor-blade coated liquid-si,* Applied Physics Letters **102**, 243502 (2013).

[4] D. Hiller, R. Zierold, J. Bachmann, M. Alexe, Y. Yang, J. Gerlach, A. Stesmans, M. Jivanescu, U. Müller, J. Vogt, *et al.*, *Low temperature silicon dioxide by thermal atomic layer deposition: Investigation of material properties,* Journal of Applied Physics **107**, 064314 (2010).

[5] G. Dingemans, C. van Helvoirt, D. Pierreux, W. Keuning, and W. Kessels, *Plasma-assisted ald for the conformal deposition of sio2: Process, material and electronic properties,* Journal of The Electrochemical Society **159**, H277 (2012).

[6] M. van Sebille, R. Vasudevan, R. Lancee, R. van Swaaij, and M. Zeman, *Optical characterization and density of states determination of silicon nanocrystals embedded in amorphous silicon based matrix,* Journal of Physics D: Applied Physics **48**, 325302 (2015).

[7] D. R. E. P. S. University, *Microelectronic device fabrication i: Lecture 8 - cv measurements,* Lecture Notes Online (2016).

[8] N. L. Cohen, *Observation and Characterization of Near-Interface Oxide Traps with C-V Techniques - Chapter 2: C-V Measurement and Techniques*, Master's thesis, Lehigh University (1995).

[9] T. Keithley, *C-V Testing for Components and Semiconductor Devices - Applications Guide, C-V Characterization of MOS Capacitors Using the Model 4200-SCS Parameter Analyzer*.

[10] C. Hu, *Modern semiconductor devices for integrated circuits,* (Prentice Hall, 2010) Chap. Chapter 5: MOS Capacitor, pp. 157–193.

[11] B. Fowler and E. OBrien, *Relationships between the material properties of silicon oxide films deposited by electron cyclotron resonance chemical vapor deposition and their use as an indicator of the dielectric constant,* Journal of Vacuum Science & Technology B **12**, 441 (1994).

[12] J. Lin, S. Monaghan, K. Cherkaoui, I. Povey, E. OConnor, and B. Sheehan, *A study of capacitance-voltage hysteresis in the hfo 2ingaas metal-oxide-semiconductor system,* Microelectronic Engineering **147**, 273 (2015).

[13] A. Doolittle, *Ece4813: Semiconductor device and material characterization, resistivity and sheet resistance,* Online Lecture Slides (2016).

[14] S. M. Sze and K. K. Ng, *Physics of semiconductor devices,* (John wiley & sons, 2006) Chap. 1: Physics and Properties of Semiconductors - a Resume, p. 32, 2nd ed.

[15] J. e. a. Rabaey, *Digital integrated circuits,* (Prentice Hall, 2003) Chap. 3: The Devices, pp. 77–132, 2nd ed.

6

LIQUID SILICON TFTS ON PAPER

In chapter 3, it has been shown that a silicon film itself can be synthesized on top of paper, and in chapter 5 electronic devices, using the same synthesis, have been fabricated on rigid substrates. The next step is to create electronics on low thermal budget substrates. A particularly interesting substrate is paper. Therefore, in this chapter, the low-temperature transformation method of polysilane is used to create electronics directly on top of paper.

Section 6.1 describes the opportunities and challenges of existing research on paper electronics. Section 6.2 presents the experimental procedure of coating and crystallizing liquid silicon on paper. The TFT fabrication method compared to devices on rigid substrates is fundamentally different and is presented in section 6.3. Section 6.4 presents the results of the fabricated paper devices. Finally the chapter concludes with a brief summary of the process and results of the fabricated devices in section 6.5.

6.1. INTRODUCTION

6.1.1. OPPORTUNITIES AND CHALLENGES

Solution-based processes have led to new types of electronics that are impractical or impossible to create with conventional microelectronic fabrication methods. This is due to both the usage of flexible rather than rigid substrates, as well as the simplification of processing methods. A printing process is commonly used to mass-produce arranged patterns over large flexible sheets; improving throughput and reducing the product cost. Bringing this type of processing to electronics however, raises a number of challenges such as the required type of materials, and technologies.

The choice of the flexible substrate is a key element of this cost reducing process. Many of the research on flexible electronics have been focusing on polymer substrates [1–3] due to the relative chemical and mechanical stability, and low surface roughness. Temperature for such substrates is an important processing issue. Those polymers with a relatively high thermal resistivity come at a higher cost than those with a lower thermal resistivity.

Aiming for low-cost by large scale printing of electronics is only practical if the substrate is also low-cost. For example, among flexible substrates, polyimide has excellent upper working temperatures (~400 °C), but has a cost of 8.16 euro/dm^2 [4], which is almost double in price of a rigid (Corning) glass wafer of 4.82 euro/dm^2 [4]. While low-cost polymers such as PET and PEN (Goodfellow[4]) cost 1.14 and 2.58 euro/dm^2. Their thermal budget however, is limited to <150 °C.

In order to optimally use the advantages of a solution-based process, it needs to be engineered in a way to produce on these low-cost substrates. Once the processing temperature is low enough, flexible substrate alternatives to these low-cost polymers may also be used. One particularly interesting alternative is paper.

Paper in everyday life is mainly used in displaying and storing information, and packaging. On one hand, using this material as a substrate for IC fabrication, leads to much more stringent requirements. Substrates in this case need to overcome high porosity, surface roughness, and poor chemical and mechanical barrier properties.

On the other hand, there are a number of advantages in using paper over polymers as a substrate for electronics. The first advantage is the significant lower cost among all flexible substrates. Paper substrates [1] cost approximately 0.13 euros/dm^2, being an order of magnitude lower than the aforementioned low-cost polymers.

In addition, paper is recyclable and biodegradable, which makes the substrate a good

[1] specifically designed for electronic purposes (Powercoat HD[5])

candidate for environmentally friendly, green, or even edible electronics. Finally, paper has a relatively low coefficient of thermal expansion (CTE) compared to polymers (values similar to the CTE of glass($4\ K^{-1}\cdot10^{-6}$)[6])[2].

These advantages of paper when combined with electronics, allow potential applications such as: sensors and actuators (smart paper), displays, and RFID tags, since reducing cost in these applications will play a significant role.

There are three types of approaches that have been investigated in this field which will be discussed in the following subsection:

1. fabricating devices directly on top of paper,

2. fabricating devices using paper as part of the device,

3. fabricating devices separately and transferring these to paper

6.1.2. RESEARCH SO FAR IN THE FIELD OF PAPER ELECTRONICS

Fabrication of devices directly on top of paper has led to a variety of research aiming at low-temperature deposition. One of the first semiconducting materials that was deposited directly on top of paper was in fact silicon, which was done by hot-wire chemical vapor deposition (HW-CVD) at 100 °C[9].

Low-temperature a-Si devices were also obtained by using Si nanoparticles in a liquid mixture and screen printing this directly on top of paper. It has been shown that using this ink, a fully printed (additive) a-Si TFT was possible with mobilities ranging from 0.3 to 0.7 cm^2/Vs.[10]

Today a variety of solution-based materials are used to process on top of paper. Organic and metal-oxide TFTs have not only a strong position in the printed electronics field, but also in the paper electronics field.

In more recent studies, organic TFTs and inverters have been created directly on a banknote,[11] with the aim of having passive security methods for anti-counterfeiting or tracking of these bills. This work showed that directly creating transistors on top of a challenging substrate such as an ordinary banknote was possible. The mobility of the p-type device was limited to 0.2 cm^2/Vs. An image of the printed banknote is shown in Fig. 6.1 a.

[2] The CTE of polymers used in the packaging industry is indeed approximately 1-2 orders of magnitude higher than paper($\sim 70\ K^{-1}\cdot10^{-6}$). However, there are those PET and PEN type polymers specifically designed for the printing of electronics [7, 8]. In those cases the CTE is not too much higher than that of paper($20\ K^{-1}\cdot10^{-6}$). In addition, paper is commonly coated with a polymer to improve surface properties. The CTE will as a result increase.

A different approach is the use of paper itself integrated as a component of the electronic device. It can be used for instance as a gate dielectric, [12, 13] or a sensor[14] or actuator[15, 16] (electroactive paper, smart paper). For sensing and actuating, its typical electric properties such as volume and surface resistivity, dielectric constant, dielectric loss, permittivities, and dielectric breakdown, have a strong dependence on external factors such as humidity. The property of the paper itself in this type can be controlled by changing the thickness, density and paper filler content.

As a gate dielectric [12, 13], because of the foam-like structure of paper, a large gate-capacitance is obtained and therefore device transconductance is improved. In addition, charged species inside the paperlead form electric double-layers, which are a function of the moisture, further increase the paper-dielectric capacitance. Paper integrated metal-oxide TFTs have been created with mobilities of around 23 cm^2/Vs and 1.3 cm^2/Vs, for n- and p-type devices, respectively. An image of this device is shown in Fig. 6.1 b.

Although it forms an efficient use of the paper substrate, the properties of the paper need to be specifically engineered. In addition the substrate is highly sensitive to the external environment. Applications may therefore be limited to sensing, rather than common TFT circuitry.

Truly high performing, complementary and reliable circuitry such as those obtained in conventional processes, can only be achieved at much higher temperatures and harsh processing conditions. The creation of silicon devices on top of paper brings stringent requirements in the silicon fabrication process. Therefore, as a third approach, high performance silicon electronics are created separately and later transferred to arbitrary substrates.

In [17], thin silicon device layers are combined in serpentine mesh geometries and are transferred to a PDMS coated surface. This PDMS enables the strong adhesion of the device areas onto the substrate while having the interconnects only loosely bonded. In addition, this layer provides strain isolation that allows high bending of the final product. Mobilities as high as 530 and 150 cm^2/Vs for NMOS and PMOS devices have been fabricated respectively. Although this method provides a solution by having high performance devices on arbitrary substrates, cost remains an issue since processing is still essentially based on high temperatures, vacuum environments and lithography. An image of this device is shown in Fig. 6.1 c.

Many different methods have been developed over the past years to create electronics using a paper substrate. However, there have been no reports, of silicon electronics directly being fabricated on top of a paper substrate in a solution-based process. This has the potential to lead to a combination of truly low-cost and yet high speed, reliable

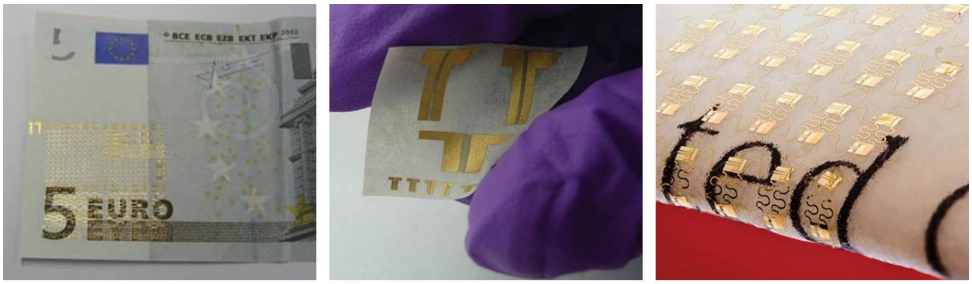

Figure 6.1: Paper electronics with OTFT on banknotes (a), MO-TFTs with integrated paper dielectric (b), and transferred Si devices on a paper substrate (c).

and efficient, electronic applications.

In this chapter a step-by-step approach towards poly-Si TFT fabrication on top of a paper substrate is presented. First, the experimental procedure towards coating and crystallizing liquid silicon on top of paper is discussed. This is followed by the engineered methods that allow fabrication of liquid silicon TFTs on top of the substrate, to finally the measurement results of the produced electronics.

6.2. EXPERIMENTAL PROCEDURE OF LIQUID SI ON PAPER

For the liquid silicon process, the approach of TFT fabrication on top of paper has been chosen. It is important to choose the right type of paper to build the transistor on. Although in some cases the paper can be used directly, device properties have shown to significantly improve when the substrate has a coating which reduces porosity and surface roughness. In this work, PowerCoat HD paper by Arjowiggins has been used which is specifically designed for printed electronics. The RMS roughness of this paper is approximately 20 nm. Additional information on the substrate can be found in the product datasheet[18].

6.2.1. COATING PROCEDURE ON HIGH SURFACE ENERGY SUBSTRATES

Although coating of CPS on rigid substrates such as silicon and glass showed reasonably good wettability, wetting issues arise when coating on paper substrates due to the high surface energy. The unstable film formation of CPS on various substrate surfaces had been investigated by Masuda et al.[19, 20]. They found that liquid silicon is subject to spinodal decomposition, which creates film ruptures as a result of an unstable capillary wave throughout the film. To create a unified film, the material must be solidified before

the ruptures are formed. The growth time of a rupture is defined by:

$$\tau_{max} = \frac{48\pi^2 \gamma_{LA} \eta L^5}{|A_{ALS}|^2} \tag{6.1}$$

where τ_{max} is the maximum growth time of a rupture, γ_{LA} is the surface free energy of the liquid-air boundary, η is the viscosity of the liquid, L is the thickness of the film, and A_{ALS} is the Hamaker constant. In order to maximize the rupture growth time, the viscosity and the amount of liquid deposited on the film have been manipulated.

The amount of liquid has a strong impact on the rupture growth time and may be increased. However, by creating a thick film will cause accumulation of stress during solidification, which leads to film cracking [21]. Therefore the amount of deposited liquid needs to be optimized. In this work 12.5 µL has been used on a paper sheet of approximately 5 by 7 cm.

The viscosity of the CPS is increased by UV-photopolymerization with a light intensity of 10 mW/cm^2. Instead of preparing the liquid in a separate beaker, curing the liquid during coating, allows a manipulation of the polymerization and coating process. In this way rupture formation times gradually increase after a number of blading strokes. Once the film appears to be stable for at least a few seconds, a more intense UV treatment of 300 mW/cm^2 is used for 30 seconds in order to solidify the film. A schematic of the process is shown in Fig. 6.2.

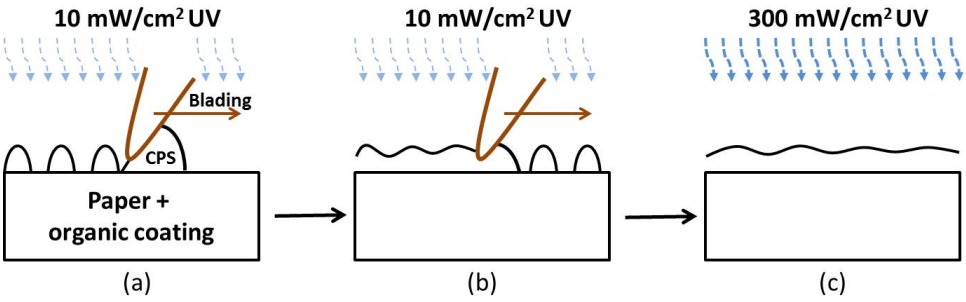

Figure 6.2: Schematic of producing a film on top of paper. Initial blading (a) showing the rupture of the film. Increasing viscosity of the film in (b), and final solidification of the film using a stronger UV source in (c).

Heat was also found to have a strong impact on the wetting properties of the liquid. Since temperature is proportional to the Hamaker constant, a heated environment will cause the rupture growth time to decrease. Film heating by for instance UV radiation must therefore be limited or avoided.

After the coating procedure, the film is further cured for 30 minutes under a UV

intensity of 10 mW/cm^2. In the rigid TFT samples, after this process a flood UV (300 mW/cm^2) treatment is employed for 30 minutes to increase the cross-linking of the film. However, for the fabrication of paper devices, the more intense UV treatment must be avoided for island patterning reasons, as will be explained in section 6.3.

6.2.2. CRYSTALLIZATION USING EXCIMER LASER ON PAPER

Crystallization of liquid silicon on top of a rigid substrate has already been explained in detail in chapters 3 and 4. Because of the change in substrate, coating and polymerization procedure, the effect of excimer laser crystallization has to be reevaluated.

Since a high intensity UV curing step is omitted. A difference is observed in polysilane films that have been laser annealed immediately after coating, and those that have been treated 1 day after coating. The former is more reactive, and shows signs of crystallization at lower energy density levels. For these films crystallization is also observed for a single pulse of the KrF laser.

Films that have been left to stabilize at least overnight inside the glovebox show less reactivity to the excimer laser treatment due to minor oxidation of the film. For these cases, a single pulse is not sufficient to crystallize the film even at fluences as high as 200 mJ/cm^2. For these samples, multiple laser pulses are required for crystallization. The stabilized film can only crystallize when it is sufficiently cross-linked and can absorb enough of the KrF laser energy. In this work, this stabilized sample has been used.

Raman spectroscopy has been used to evaluate the crystallization conditions after the excimer laser treatment of polysilane on paper. The Raman spectra of bare paper shows vibrational modes at 395, 517 and 638 cm^{-1}. As a result, when the laser transformation is limited, the key silicon vibrational modes at around 500 cm^{-1} are overshadowed by the paper baseline.

Raman measurement results of single pulse treatments of stabilized polysilane is shown in Fig. 6.3. Only a limited change in peak intensity is observed. In addition, a color change is observed for these samples, which would indicate an increase in cross-linking which may amplify the absorption of subsequent laser pulses.

Samples that are successfully transformed to polycrystalline silicon however show a relative intensity increase of the peak at 520 cm^{-1}, which overwhelms the baseline of the paper substrate. Multiple pulses at energy densities of 40 mJ/cm^2 generally result in a colorful film. This film shows signs of crystallization, however depending on the area the film may give a higher or lower crystalline silicon peak intensity due to the inhomogeneity of the thickness and laser spot. This is shown in Fig. 6.4 a.

Multiple pulses from a fluence of 50 mJ/cm^2, have led to a strong poly-Si signal in the

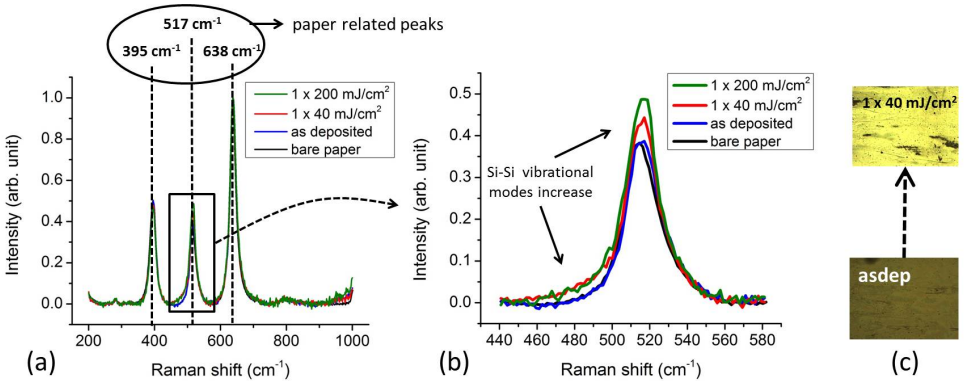

Figure 6.3: Raman spectra of polysilane annealed with single pulse excimer laser energy densities (a), the same spectra focusing on the area for the Si-Si TO mode (b), optical images of the transformation (c).

Raman spectra (see Fig. 6.4 b), accompanied by a significant darkening of the film due to the roughness increase. For higher laser fluences, more intense c-Si Raman peak are observed, although film roughness is also significantly increased, which will deteriorate device performance.

From these experiments it is expected that multiple pulses of 40 or 50 mJ/cm^2 should give the best results in terms of electric device performance.

6.3. FABRICATION METHOD OF DEVICES ON PAPER

Compared to processes on silicon wafers or glass substrates, processing with paper bring important challenges that need to be addressed. Although the final goal is to create fully solution-processed low-cost Si electronics, as a first approach, it is important to keep using many of the conventional fabrication steps to maximize the device performance. For this process, there are three important requirements:

1. The paper must be taped or otherwise fixed to a rigid wafer to allow the processing equipment to handle the substrate as a rigid one.

2. The paper may not be exposed to wet chemical etchants such as HNO_3, acetone, among others, necessary for cleaning steps and photoresist removal.

3. The paper may not be exposed to temperatures above 130 °C.

The solution to requirement 1 is simply taping the paper to a silicon substrate by means of a double-sided tape from the backside of the paper.

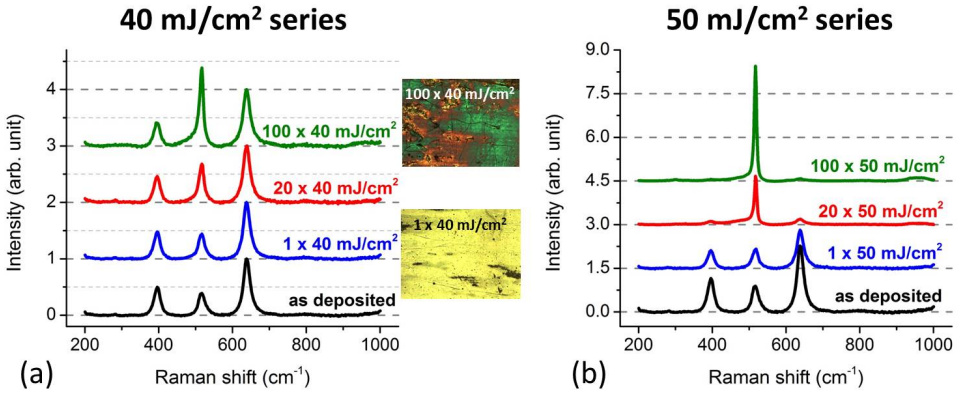

Figure 6.4: Raman spectra of polysilane annealed with multiple pulse excimer laser energy densities of 40 mJ/cm^2 (a), and 50 mJ/cm^2 (b).

The second requirement is more challenging. This requirement would imply that photoresist cannot be used, since the resist cannot be removed without affecting the paper. Processing without lithography means that additive patterning is necessary. In addition, being unable to clean the devices in HNO_3 will also have an impact on the final device performance.

The third requirement has already been met in the rigid device processing explained in chapter 5. The gate oxide deposition is the most critical step, and is deposited at 120 °C. Process steps in general should be performed at as low temperature as possible due to the thermal expansion of the paper which may cause cracking of device patterns.

6.3.1. MICROPATTERNING WITHOUT PHOTOLITHOGRAPHY

In the creation of a TFT there are a number of films that need to be patterned: a crystalline silicon island, gate metal, contact openings, and contact metal. In addition these layers need to be aligned on top of each other.

ISLAND PATTERN CRYSTALLIZATION

Polysilane left in open air will oxidize, unless it is crystallized. Since crystallization is the result of laser exposure, exposing parts of the film will allow both crystalline silicon as well as untreated polysilane to exist in the same film. By preparing a mask with island patterns, poly-Si islands can be formed that are surrounded by the dielectric. In this way, the islands are formed in a process of an additive nature, rather than a subtractive one.

It is important that the polysilane used is therefore not severely cross-linked to allow the oxidation procedure under ambient conditions. Therefore for the curing process

of CPS on paper, the UV source with 10 mW/cm^2 is used without a subsequent curing treatment of the more intense 300 mW/cm^2 UV source, which was needed in chapters 3 to 5.

A quartz wafer with a patterned metal film is used that could block parts of the excimer laser pulse. 100 nm of 99% Al with 1% Si has been sputtered on one side of the quartz wafer. Island patterns in photoresist are exposed by photolithography, and a wet-etching process is used to remove the exposed metal. A phosphoric/acetic/nitric acid mixture (PES) has been used as the wet aluminum etchant. The remaining silicon (approximately 1 nm) has been found to have a negligible impact to the laser fluence, as the difference is overshadowed by the pulse to pulse variation of the excimer laser itself.

The quartz mask is attached with the metal-side onto the target substrate. This is done to ensure a minimum distance between the defined metallic area and the polysilane. Any distance will lead to a diffraction of the laser beam, and as a result, poorly defined poly-Si patterns. In addition, the paper surface needs to be completely flat, otherwise the patterned laser pulse will land on a different location than preassigned by the quartz-mask, making future alignment of the film impossible.

Fig. 6.5 (a) and (b), show the schematic of the patterned crystallization process, and an image of the mask used in this process, respectively. The total design of one die in this mask is shown in Fig. 6.5 (c). This design has three important aspects:

1. A cross in the middle of every die is created in order to facilitate the manual alignment using an optical microscope.

2. A big open area in one quadrant of every die is used to inspect the change of color during crystallization.

3. It is important to have some working space when subsequent layers get misaligned. Device structures are therefore designed to be relatively large (5-100 μm).

The laser annealing will be used for a second time in the process during the dopant activation step. The untreated polysilane that has oxidized however, will not react to an excimer laser treatment. As a result, a following dopant activation treatment can be performed on the unmasked film without the risk of SiO_2 transforming into poly-Si or a-Si.

METAL PATTERN CREATION

Shadow-masking is a common method for patterning metals by additive means. Rigid plates with patterned holes are fixed on a target substrate. Metal is then evaporated onto the substrate under vacuum conditions. After the plate or mask is removed, only

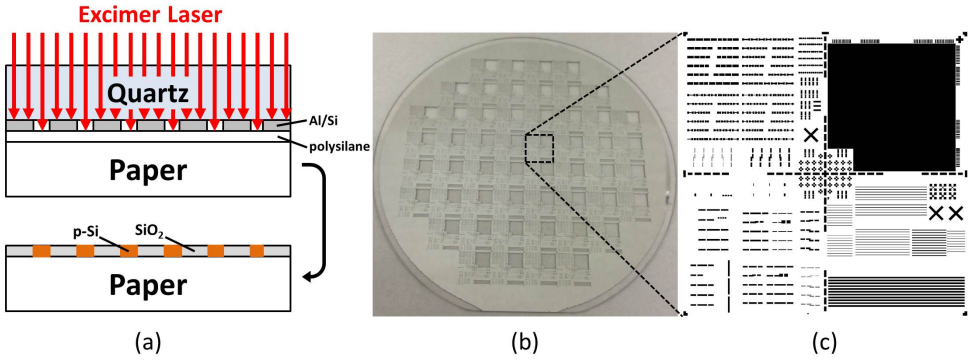

Figure 6.5: Masking process schematic for island patterns (a), optical image of the mask (b), design of one die (c).

the parts of the mask that were exposed allowed metal to be directly deposited on the substrate.

In this process a wafer sized mask is used for two reasons: to simplify alignment and fixation of the mask to the target substrate, and to be able to use equipment used for wafer based processing such as photolithography and etching to create patterns in the mask.

The masking wafers have a thickness of 550 µm, and need to be etched all the way through by using deep reactive ion-etching (DRIE). 4 µm of Al is sputtered on the back-side of the wafer, and this will serve as the stopping layer for the etching process. 6.5 µm of PECVD SiO_2 is deposited and patterned on top of the Si wafer which will form as a masking layer for the DRIE process. Although the machine is meant for straight side-wall etching, in this process this feature is less important, as long as the patterns etch all the way through, and the wafer does not become too brittle in the process. Bigger sized patterns inevitably etch away faster than smaller patterns, so a significant overetching time is needed in order to fully open the smallest patterns. Since the etching time is calculated for the smallest patterns, the bigger holes start to deform at the bottom of the wafer once the silicon is fully etched.

Pattern deformation at the bottom of the wafer is acceptable, as long as the topside is clearly defined, since this topside is placed in contact with the wafer to define the final pattern shapes. Fully etching from 100 µm to 5 µm patterns was possible in this way. The Al stopping layer is later chemically removed. Fig. 6.6 (a) shows a schematic of the shadowmask evaporation process. Fig. 6.6 (b) shows an image of the mask and the top and bottom side view of the patterns. Fig. 6.6 (c)shows the gate-pattern design of a single

die.

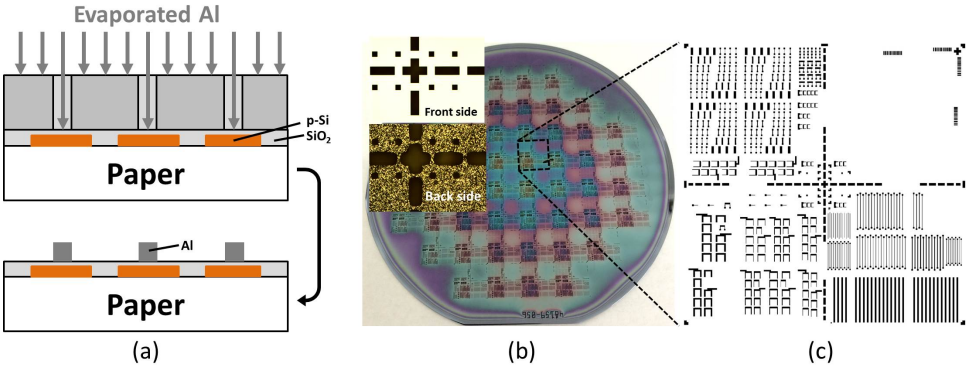

Figure 6.6: Masking process schematic for metal patterns (a), optical image of the mask with comparisons of front to backside (b), and the design of a single die (c).

PATTERN ALIGNMENT

The design of the mask allows alignment to the previously created patterns by using the cross in the middle of every die [3]. After the accurate positioning of the mask to the target substrate, the mask needs to be fixed in a way that it does not move during handling and metal deposition.

Rather than taping or clamping, the mask is fixed by using a type of wax (Crystalbond™590, Ted Pella. Inc.) commonly used in the semiconductor industry for TEM analyses. It is a wax that can melt at 100 °C, and resolidifies below this temperature. It can withstand high vacuum conditions similar to those applied in TEM equipment.

A thin layer of wax is prepared on the edge of both the mask and the carrier wafers. The wafers are then aligned manually using a microscope. Once aligned, the wafers are held in position and heated locally around the edge by using a soldering iron. A schematic is shown in Fig. 6.7 (a).

Since the wafers are fixed with a wax that melts at 100 °C, and softens at 80 °C, it is important that during the evaporation process, the temperature of the sample does not exceed 70 or even 60 °C. The temperature of the evaporation chamber was set to not exceed 60 °C during the 500 nm Al evaporation process.

The mask can be removed by locally heating the edges of the wafers and separating the two by tweezers[4]. Subsequently, the wax residues can be dissolved in methanol. The

[3] It is important to have the cross designed in separated fragments. This slows down the etching rate of the cross, and more importantly, makes the mask less brittle.

[4] Alternatively, the setup can be placed on a hotplate, increasing the temperature to around 110 °C and slowly pulling the mask off the wafer. However, at these temperatures the paper starts to expand and may cause structures on the paper to crack. Therefore, heating only locally is preferred.

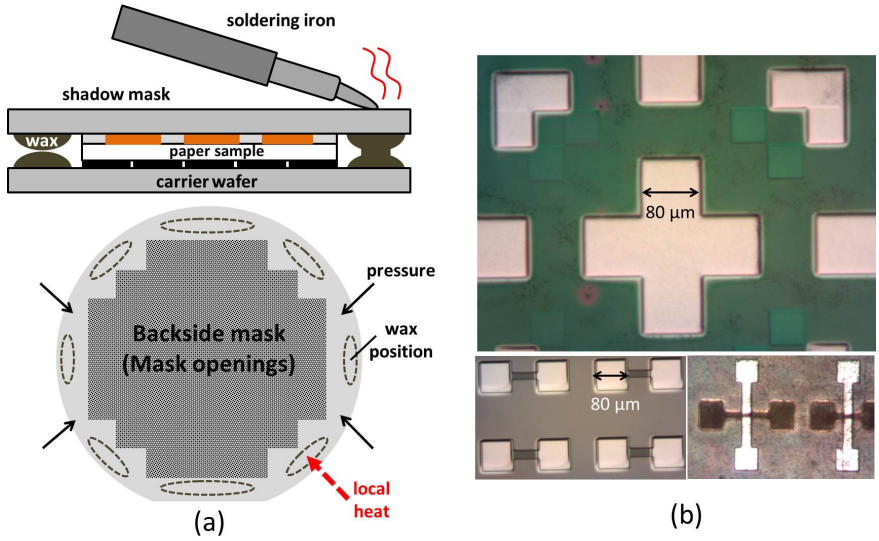

Figure 6.7: Shadow mask alignment process schematic with the wax method (a), cross in the middle of the die and island patterns (b).

result is shown in Fig. 6.7 (b).

6.3.2. TOTAL DEVICE-ON-PAPER PROCESS FLOW

The complete flowchart of the TFT-on-paper process is presented in Appendix C. A summary of the processing steps is displayed in Fig. 6.8, and is briefly described below:

1. PowercoatHD paper is taped with a double-sided tape on a carrier wafer.
2. The paper is coated with 12.5 µL of pure CPS with a doctor blade, while at the same time being cured with a 10 mW/cm^2 UV light source. Once a film is formed, it is rapidly solidified with an intensity of 300 mW/cm^2 UV for 30 seconds.
3. The film is further cured with the intensity of 10 mW/cm^2 for 30 minutes.
4. A quartz mask with metallic patterns is placed metal-side-down onto the sample and is fixed by tape. The excimer laser is used to crystallize the polysilane islands while leaving the parts covered with metal untreated.
5. The sample is exposed to open air for 1 day to oxidize the untreated polysilane.
6. A gate-oxide of 100 nm thick SiO_2 is deposited by RF-PECVD at 120 °C.
7. 500 nm thick Al gate is evaporated using a shadow-mask which is aligned with a microscope and fixed with a wax.

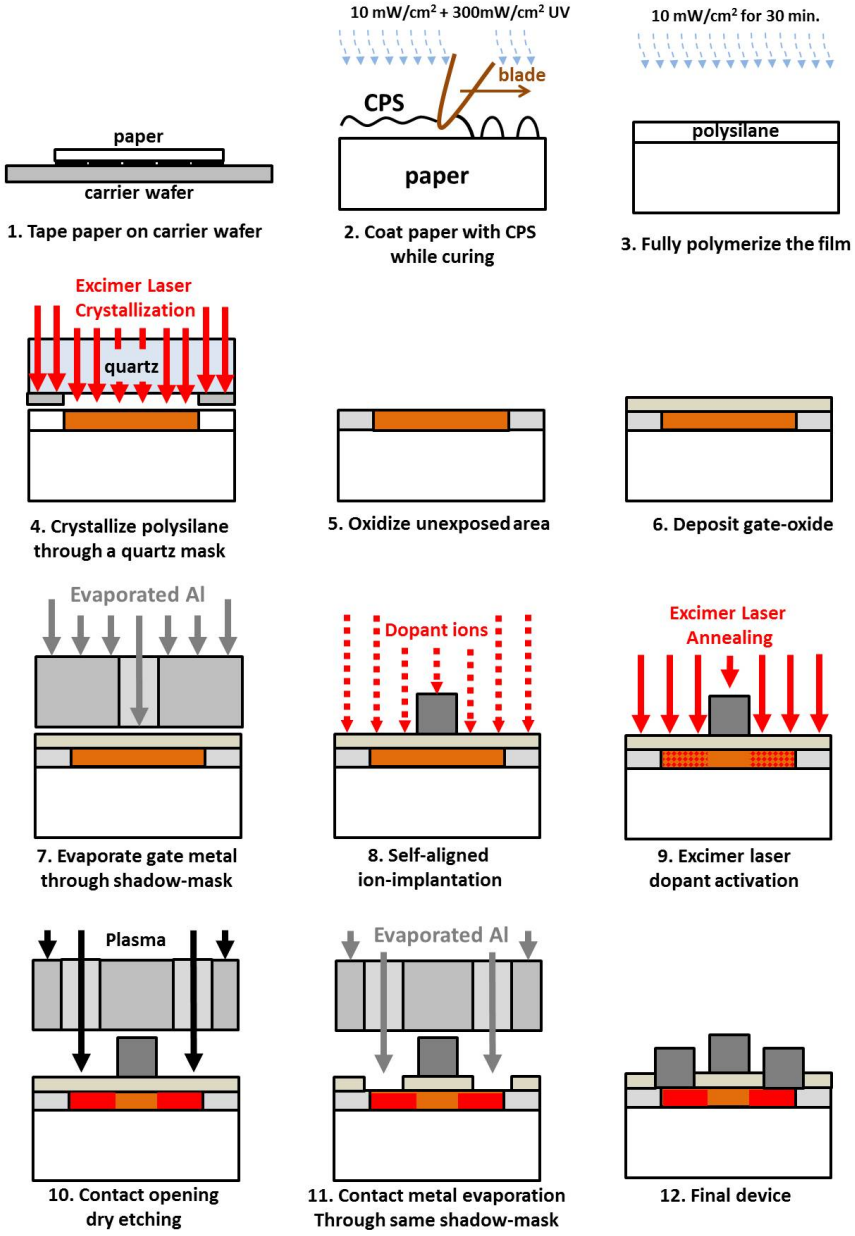

Figure 6.8: Paper process schematic.

8. Self-aligned ion implantation is performed on the sample, by using the Al gate to block the ions from entering the channel region.

9. The excimer laser is used to activate the dopant ions.

10. A shadow mask is used to cover everything except for the contact openings. Using this mask the oxide at the position of the contacts is removed by a plasma etching.

11. Without moving the shadow mask, 500 nm thick Al contacts are evaporated.

An image of the completed full wafer sample and some of its individual transistor elements are shown in Fig. 6.9.

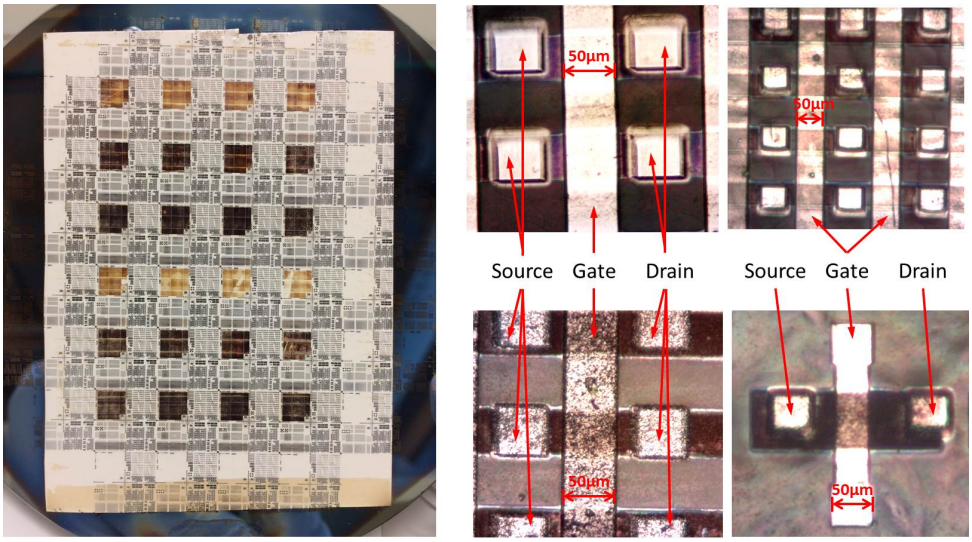

Figure 6.9: Photographic image of the full completed sample (a), and individual TFT elements found on the sample (b).

6.4. PAPER DEVICE CHARACTERISTICS

Similar to the rigid devices, both resistors and TFTs have been fabricated and analyzed. For details about the method of device parameter extraction, the reader is referred to sections 5.3 and 5.4.

6.4.1. RESISTORS ON PAPER

P-type Kelvin resistors were fabricated on top of the paper substrate. Although definite conclusions about the optimal crystallization and activation conditions is difficult to give, it is important to know the highest conductivity obtained given a range of laser conditions.

For the implantation, boron ions were implanted at a dose of $3{\cdot}10^{15}$ at/cm^2 and an energy of 15 keV. Crystallization and dopant activation conditions were analyzed for fluences of 40, 50, 60, and 70 mJ/cm^2 with 1, 10 and 50 pulse conditions.

From the resistor measurement results, the lowest resistivities were obtained for 10 pulses of 50 mJ/cm^2 for both crystallization as well as dopant activation. A resistance of 6.9 kΩ was measured. A plot of the applied voltage to measured current together with the fitted resistance calculation is presented in Fig. 6.10 a.

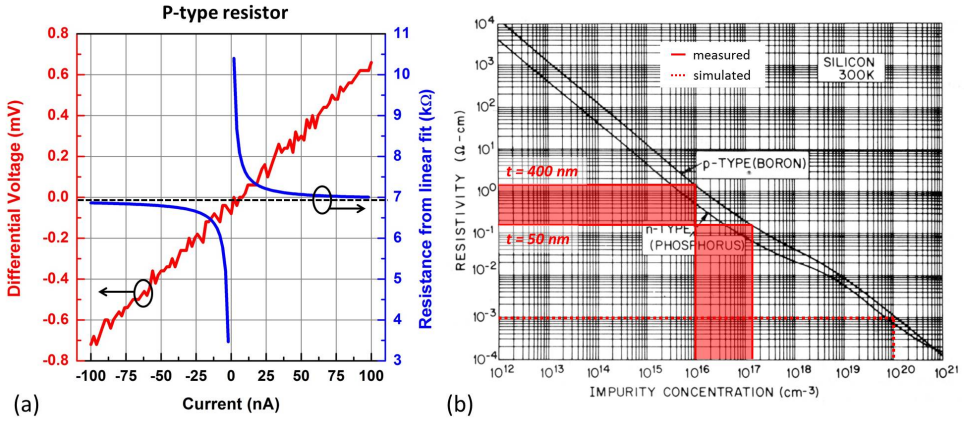

Figure 6.10: VI-curve of the lowest resistivity resistor on paper (a). Resistivity to doping concentration curve[22] with the indicated measured values and the desired value (b).

Since the film thickness is difficult to determine on the paper substrate, only an assumption can be made. The thickness is believed to vary between 50 and 400 nm. Less than 50 nm is unlikely due to the increased liquid viscosity during the blading process. Above 400 nm is unlikely due to the accumulated stress inside the film which would lead to cracking. In this way the resistivity ranged from 0.2 to 1.3 Ωcm for a thickness of 50 and 400 nm, respectively. The resistivity to dopant concentration for the measured condition is presented in Fig. 6.10 (b).

Similar to the resistors created on the rigid wafer, the difference between the measured and desired resistivities are 2 to 3 orders of magnitude. This deviation has similar causes as those listed in section 5.3, the most important reason being the difference in

silicon quality. The black curve in the Fig. 6.10 (b) is related to high quality crystalline silicon, and not nanocrystalline silicon produced on a rough paper substrate.

The observed optimal condition of 10 pulses of 50 mJ/cm^2 for both crystallization and dopant activation may vary for different paper samples. This is again caused by the variation in coated polysilane thickness. An accurate optimization can only be performed once a reproducible thickness can be created. The obtained results is a proof of concept and shows that the created poly-Si on paper has similar properties to those created on a rigid sample which has shown to give relatively good TFT performance.

6.4.2. POLY-SI TFTS ON PAPER

Transfer and output properties of the poly-Si PMOS and NMOS TFTs were measured. For the transfer curves, a drain voltage of -5 and 5 V for the PMOS and NMOS TFTs were applied, respectively. At these drain voltage values, both TFTs operate in the saturation regime ($|V_D| > |V_{GS} - V_{th}|$) for which the following drain current description should be applied:

$$I_{DS} = \frac{1}{2}\mu_{FE}C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \tag{6.2}$$

where μ_{FE} is the field effect mobility, C_{ox} the gate oxide capacitance per unit area, $\frac{W}{L}$ the channel width over length ratio, V_{GS} the voltage applied at the gate, and V_{th} the transistor threshold voltage.

From this current definition the mobility is obtained by the derivative of the square root of the drain current as described by:

$$\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}} = \sqrt{\frac{1}{2}\mu_{FE}C_{ox}\frac{W}{L}} \tag{6.3}$$

Rearranging gives:

$$\mu_{FE} = \frac{(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}})^2}{2\frac{L}{W}C_{ox}} \tag{6.4}$$

All devices that were measured had a channel length and width of 50 µm. From the range of applied laser conditions, the best performing PMOS and NMOS TFTs were obtained for a crystallization treatment of 20 pulses of 50 mJ/cm^2, and activated with 10 pulses of 50 mJ/cm^2.

The transfer properties of typical PMOS and NMOS TFTs are presented in Fig. 6.11. Due to the relatively small difference between gate leakage current and drain current (1 to 2 orders of magnitude) compared to the devices prepared on a rigid sample in chapter 5 (5 to 6 orders of magnitude), measurements were restricted to the voltage ranges of good TFT operation. Gate voltages outside of the presented range either cause the gate current to surpass the drain current, or the drain current tail to rise. Drain currents were significantly limited by the high contact resistance, as a result of omitting the native oxide removal step.

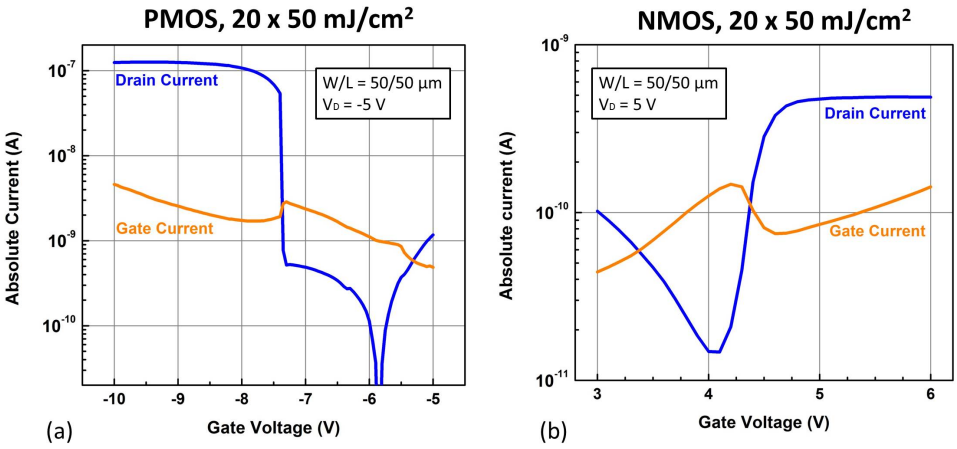

Figure 6.11: Transfer curves of typical PMOS (a) and NMOS (b) TFTs on a paper substrate. Drain current shown in blue and gate current shown in orange.

The output properties of typical PMOS and NMOS TFTs are presented in Fig. 6.12. The output characteristics of the PMOS TFT show relatively standard operation, with a brief moment where the slope becomes negative. This is due to the self-heating effect on the device, since paper is a poor thermal conductor [23]. For the NMOS TFT, good output properties were difficult to obtain. Due to the high gate leakage, higher gate voltages led to an initially larger leakage at 0 V_{DS}. As a result every curve shifts with increasing gate voltages. In order to be able to determine the linear and saturation regimes, the curves need to be offset and rearranged. Self-heating effects are also visible in these curves by the declining drain current for increased drain voltage.

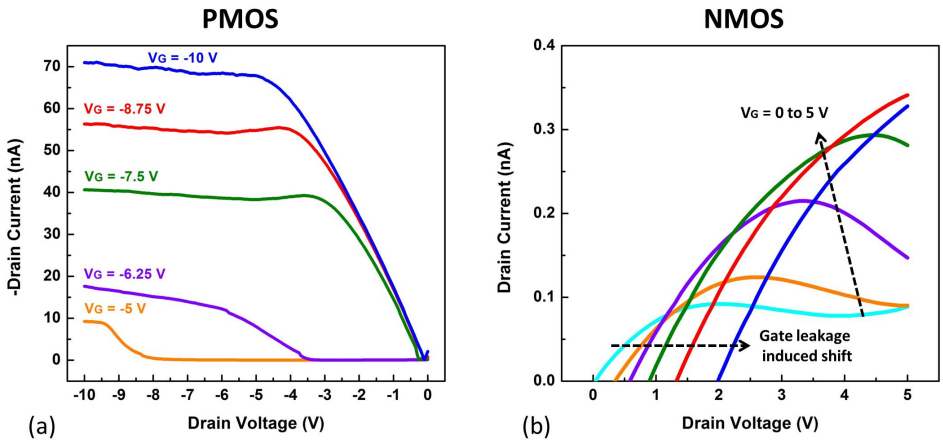

Figure 6.12: Output curves of PMOS (a) and NMOS (b) TFTs on a paper substrate for different gate voltage values.

The TFT properties are summarized in Table 6.1. Two important items need to be addressed regarding the measurement results obtained for the PMOS and NMOS TFTs: gate current leakage, and the difference in performance between PMOS and NMOS samples.

Table 6.1: Performance summary of liquid silicon based TFTs on a paper substrate.

	PMOS	NMOS
Field Effect Mobility (cm^2/Vs)	6.2	0.2
Threshold Voltage (V)	-7.3	4.3
Subthreshold Swing (mV/dec)	27	190
Gate Leakage Current (A)	~ 10e-9	~ 10e-10
I_{on}/I_{off}	1.3e-7/neg.	33

GATE CURRENT LEAKAGE

A gate current for both samples in the order of nanoampere is observed for both samples, which is considered relatively high compared to the rigid device samples (tens of picoampere). This in spite of the fact that a relatively thick gate oxide of 100 nm was used in this process as opposed to 50 nm used in the rigid samples, to avoid such high leakage currents. This can be caused either by its production on top of the paper substrate, or the subsequent process steps that may have harmed the oxide in any way.

During the deposition process, it is likely that the paper may have outgassed in the vacuum environment, due to the high paper porosity that captures moisture and oxy-

gen. This outgassing was also observed for metal evaporation causing the deposited metal to oxidize. Therefore the deposited oxide may not be identical to the one that was constructed on a rigid silicon sample. A solution to this issue was found, for the case of metal evaporation, by allowing the sample to outgas overnight or longer before the deposition.

Another aspect of this deposition is the temperature. The equipment uses radiative heating for the deposition, where the set temperature is 120 °C, and the sample temperature generally rises to around 100 °C. While this is accurate for a silicon wafer, for paper, thermal conductivity and heat capacity properties are different and the sample may heat up in a different way. Experiments indicated however that the temperature did not significantly rise over 100 °C. Besides structural oxide quality deviations due to the difference in temperature, the height of the temperature may have already been too high for the paper sample, causing the substrate to partially expand or even cause cracks in the existing crystalline silicon structures. One solution to this issue is to optimize an oxide deposition process for even lower temperatures that limits the thermal expansion of the substrate.

In addition, for the SiO_2 deposition RF-PECVD was used at a temperature of 120 °C. Prior to the deposition, no native oxide removal has been performed. Native oxide causes detrimental effects on the device performance since it creates a poor interface between the silicon and the gate-oxide, and is a center for charge carrier traps. To remove the native oxide, a wet chemical etching treatment is necessary which is avoided in the work on a paper substrate. As a result, a native oxide layer exists on top of the poly-Si surface, which significantly increases the subthreshold slope.

PERFORMANCE DIFFERENCE PMOS AND NMOS TFTS

In the TFT measurement results PMOS TFTs have shown to outperform the NMOS counterpart in terms of mobility, Ion/Ioff ratio, and subthreshold slope. There are two reasons behind this result.

After contact hole etching by plasma, the samples had to be transported to the evaporator in an open air ambient. It is likely that this ambient caused native oxide to form on the source and drain regions before contact pad evaporation, leading to a high contact resistance. The effect of this native oxide on the conduction band is stronger than the valence band, causing only the NMOS TFTs to limit in performance. Indeed, n-type resistor measurements have mostly resulted in values in the gigaohms range, and an optimization is necessary. To ensure a good passivation, rather than a HF dip, HF vapor etching may be used which would minimally impact both the paper and the existing metallic patterns.

A second reason is the difference in implantation. For the n-type TFTs phosphorus dopants are implanted at an energy of 90 keV, while for the p-type boron dopants the implantation energy was limited to only 30 keV. Although structural amorphization from this high energy ions of the silicon island can be repaired by subsequent excimer laser annealing, the implantation process itself causes the sample to heat up. In order to limit the temperature to 100 °C, the applied current was reduced. This temperature however may still have been enough for the paper to once again expand and break existing silicon islands or oxides. A solution to this is to further reduce the implantation current to a temperature of approximately 80 °C. Alternatively a thinner gate oxide may be deposited that would reduce the required implantation energy and as a result reduce the heat on the sample.

Other areas of improvement besides the items presented for the gate oxide, native oxide prevention and ion implantation, for an increased TFT performance on paper include: using an SiO_2 buffer layer before CPS coating, optimization in dopant activation recipes, automated alignment and specific mask design in such a process, among others.

6.5. CONCLUSIONS

In order to obtain the maximum benefits of a solution-based process, the substrate choice plays an important role. Both in the cost minimizing aspect as well as in the functional aspects of the substrate such as flexibility. For low-cost flexible polymer substrates, the thermal budget is generally limited, which raises challenges for a microelectronic fabrication process. Once this process can be engineered to be built on such low thermal budget substrates, an interesting alternative can be used: paper.

Paper is a challenging substrate to work on for microelectronics fabrication due to the porosity, roughness, and poor chemical and mechanical properties. The substrate however has important advantages over other low-cost flexible substrates such as: significant lower cost (an order of magnitude lower than low-cost polymers), biodegradability/recyclability, and low coefficient of thermal expansion.

Three approaches of integrating electronics on/in paper is being researched: direct device fabrication on top of paper, integrating paper as part of the device, transferring finished device onto a paper substrate. In this work the first approach is used, by using paper with a coating to significantly reduce the roughness and porosity.

CPS has a poor wettability on the paper substrate used in this work. This is due to the spinodal dewetting that a CPS film experiences, which causes ruptures to form. The rupture growth time is improved by increasing the viscosity and the thickness of the film. 12.5 µL of CPS is used for a paper sheet of approximately 5 by 7 cm. The viscosity is

increased gradually by blade-coating the liquid under a 10 mW/cm^2 UV exposure. Once a unified, rupture-less film, stays for a few seconds, the film is solidified by curing with an intensity of 300 mW/cm^2 for 30 seconds.

Crystallization of this film is analyzed by Raman spectroscopy. The threshold fluence for crystallization was found to be approximately 40 mJ/cm^2. A colorful film was observed after multiple pulses of this fluence. As the fluence increases, the film becomes more crystallized, but also increases in roughness, which may harm device performance.

For device fabrication on top of paper, three requirements had to be met: maximum process temperature of approximately 130 °C, using a rigid carrier wafer, and avoid usage of wet chemical etchants. The paper sample is taped onto a rigid wafer to allow the usage of conventional microelectronics equipment. The sample may not be exposed to chemical etchants, which prohibits usage of photolithography for patterning on the paper substrate. Additive patterning by using shadow-masks is a solution to this.

Contrary to the rigid substrates, an improved cross-linking step by the 300 mW/cm^2 UV is omitted to allow untreated polysilane to oxidize in open air. Using a shadow mask, island patterns are directly crystallized by the excimer laser, while leaving the unexposed parts untreated and still reactive to oxygen.

After the oxide deposition at 120 °C by RF-PECVD, the metallic gate is evaporated through a shadow mask, and the contact openings and metals are etched and deposited, respectively, by a single mask. Mask alignment during these steps is conducted manually under a microscope. Fixation of the mask is performed by a wax which has a melting point of 100 °C.

In this way, resistors and TFTs have been fabricated. The lowest device p-type resistivity was observed for a laser treatment of 10 pulses of 50 mJ/cm^2 for both crystallization and activation. Depending on the film thickness this resistivity ranged from 0.16 Ωcm to 1.25 Ωcm for a thickness of 50 nm and 400 nm, respectively. The measured values are 2 to 3 orders of magnitude higher than desired. This deviation comes from the difference in crystalline silicon quality, as well as simulation mismatch, and non-optimization. Increasing the dose may reduce the resistivity.

The device mobilities obtained for the P- and N-MOS device were 6.2 and 0.2 cm^2/Vs, respectively. The device performance is limited due to the high roughness of the paper, and the non-ideal process conditions. The obtained results serve as a proof of concept and is subject to optimization.

This work has shown that silicon devices can be created on top of a paper substrate, which opens the pathway towards new applications such as extreme-low-cost-silicon, RFID tags, displays, sensors and actuators that are also biodegradable.

REFERENCES

[1] M. Kaltenbrunner, T. Sekitani, J. Reeder, T. Yokota, K. Kuribara, T. Tokuhara, M. Drack, R. Schwödiauer, I. Graz, S. Bauer-Gogonea, *et al., An ultra-lightweight design for imperceptible plastic electronics,* Nature **499**, 458 (2013).

[2] S. Chung, S. O. Kim, S.-K. Kwon, C. Lee, and Y. Hong, *All-inkjet-printed organic thin-film transistor inverter on flexible plastic substrate,* Electron Device Letters, IEEE **32**, 1134 (2011).

[3] J. Zhang, M. Trifunovic, M. Van Der Zwan, H. Takagishi, R. Kawajiri, T. Shimoda, C. Beenakker, and R. Ishihara, *Single-grain si thin-film transistors on flexible polyimide substrate fabricated from doctor-blade coated liquid-si,* Applied Physics Letters **102**, 243502 (2013).

[4] Goodfellow, *Alphabetic list of materials,* online (2016).

[5] *Arjowiggins creative papers, powercoat,* online (2016).

[6] C. D. Technologies, *Product information sheet eagle xg slim glass,* (2013).

[7] Goodfellow, *Polyethylene terephthalate material information,* .

[8] D. T. Films, *Teonex q65a star,* .

[9] D. Britton, M. Härting, D. Knoesen, Z. Sigcau, F. Nemalili, T. Ntsoane, P. Sperr, W. Egger, and M. Nippus, *Microstructural defect characterisation of a-si: H deposited by low temperature hw-cvd on paper substrates,* Thin solid films **501**, 79 (2006).

[10] M. Härting, J. Zhang, D. Gamota, and D. Britton, *Fully printed silicon field effect transistors,* Applied Physics Letters **94**, 193509 (2009).

[11] U. Zschieschang, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, and H. Klauk, *Organic electronics on banknotes,* Advanced Materials **23**, 654 (2011).

[12] R. Martins, A. Nathan, R. Barros, L. Pereira, P. Barquinha, N. Correia, R. Costa, A. Ahnood, I. Ferreira, and E. Fortunato, *Complementary metal oxide semiconductor technology with and on paper,* Advanced MAterials **23**, 4491 (2011).

[13] R. F. Martins, A. Ahnood, N. Correia, L. M. Pereira, R. Barros, P. M. Barquinha, R. Costa, I. M. Ferreira, A. Nathan, and E. E. Fortunato, *Recyclable, flexible, low-power oxide electronics,* Advanced Functional Materials **23**, 2153 (2013).

[14] S. Ummartyotin and H. Manuspiya, *a critical review on cellulose: From fundamental to an approach on sensor technology,* renewable and Sustainable Energy Reviews **41**, 402.

[15] J. Kim and Y. B. Seo, *Electro-active paper actuators,* Smart Materials and Structures **11**, 355 (2002).

[16] S. Deshpande, J. Kim, and S.-R. Yun, *Studies on conducting polymer electroactive paper actuators: effect of humidity and electrode thickness,* Smart materials and structures **14**, 876 (2005).

[17] D.-H. Kim, Y.-S. Kim, J. Wu, Z. Liu, J. Song, H.-S. Kim, Y. Y. Huang, K.-C. Hwang, and J. A. Rogers, *Ultrathin silicon circuits with strain-isolation layers and mesh layouts for high-performance electronics on fabric, vinyl, leather, and paper,* Adv. Mater **21**, 3703 (2009).

[18] A. C. Papers, *Powercoat paper hd technical data sheet,* .

[19] T. Masuda, Y. Matsuki, and T. Shimoda, *Spectral parameters and hamaker constants of silicon hydride compounds and organic solvents,* Journal of colloid and interface science **340**, 298 (2009).

[20] T. Masuda, Y. Matsuki, and T. Shimoda, *Stability of polydihydrosilane liquid films on solid substrates,* Thin Solid Films **520**, 5091 (2012).

[21] T. J. Garino, *The cracking of sol-gel films during drying,* in *MRS Proceedings*, Vol. 180 (Cambridge Univ Press, 1990) p. 497.

[22] S. M. Sze and K. K. Ng, *Physics of semiconductor devices,* (John wiley & sons, 2006) Chap. 1: Physics and Properties of Semiconductors - a Resume, p. 32, 2nd ed.

[23] A. Valletta, A. Moroni, L. Mariucci, A. Bonfiglietti, and G. Fortunato, *Self-heating effects in polycrystalline silicon thin film transistors,* Applied physics letters **89**, 093509 (2006).

7

Micro-Contact Printing of Liquid Silicon Patterns

In previous chapters, the primary focus was to develop a method that allows crystalline silicon formation from liquid silicon on low thermal budget substrates. This method has been developed and used in electronic devices in chapters 5 and 6. In the latter chapter, an attempt had been made to move towards a system with additive processing only. The island patterns were constructed inside a polysilane film. Printing individual islands directly allows the substrate to be bent with a reduced risk in device cracking, and uses the liquid more efficiently.

In this chapter, an investigation is made on liquid silicon printing by means of a PDMS stamp. Section 7.1 presents the research that has been done so far on printed electronics in general. The experimental printing procedure and results of the process are then presented in sections 7.2 and 7.3, respectively. Finally, in section 7.4, the chapter is concluded by giving a summary of fabrication process, device characteristics and recommended work.

7.1. INTRODUCTION

Printing is a method of reproducing inks in a certain arrangement by means of a template also known as a master. It has been widely used in the graphics industry as a way of mass producing products such as newspapers, magazines, books, posters, packages, etc. In such a process, large sheets or webs are fed through a system with many ink-applying rolls that transfer patterns at high speeds. As a result, the cost per unit area is extremely low since product throughput is high.

Printing processes could also be applied to the field of microelectronic fabrication by applying electronic elements as inks. Similar to the graphics industry, this would significantly drive the cost for IC fabrication down. However, since high performing electronics require complex equipment and stringent environments, electronics produced by printing in essence cannot be superior to those created by conventional methods.

It is therefore unlikely for this alternative method to replace existing microelectronic fabrication processes. For a broad range of applications however, where the performance of electronics is not a primary requirement, driving the cost down will play a leading role.

7.1.1. IMPACT OF PRINTED ELECTRONICS

ECONOMICAL IMPACT

The main driving force for pursuing a production process based on printing was its potential to significantly decrease processing costs. This can be analyzed in three important aspects comparing to conventional microelectronic fabrication processes.

The first aspect is the initial expenses for having the patterning equipment for printed electronics compared to lithography tools, used in conventional microelectronic processes. Although, the state-of-the-art lithography tools are far more expensive than the state-of-the-art printing system, the comparison is unfairly made since the obtainable resolution in patterning is very different. For the lithography systems these are orders of magnitude higher than for printing systems. A depreciated lithography tool that can produce the same resolution as a printing system, is lower in cost compared to a printing system for a resolution of 1 μm or less.

The second aspect is the overall cost reduction of using a printing process due to less patterning complexity by its additive nature. For a conventional lithography system, a predeposited film is removed by using a photoreactive polymer masking layer. As a result, six steps are necessary to create a pattern of a specific material.

On the other hand, for a printing process, a specific liquid material is directly transferred to a target substrate in the desired arrangement. A subsequent curing or annealing

step solidifies the transferred liquid pattern. Since patterning in a conventional IC is performed at least 30 times [1], the product throughput for printing systems is much higher, and there exists therefore a strong cost advantage in this aspect.

Finally, using printing systems allows mass-production by fabricating on large areas through a roll-to-roll process. Although this advantage exists in the long term when processes are optimized, research is still ongoing for this potential.

As a conclusion, an economical advantage of at least 10X was found to be obtainable, in the cost per unit area. The cost per device however, is much higher compared to conventional processes. Therefore, rather than being a competing technology, the printing process should be an alternative way for applications that are area constrained rather than device density and functionality constrained such as for displays and solar cells among others [2, 3].

TECHNOLOGICAL ADVANTAGES AND DISADVANTAGES

From the technology point of view there are a number of important advantages and disadvantages, or rather challenges, of using solution-based printing over conventional microelectronic fabrication methods:

+1 Vacuum

Solution-based processes in general do not require vacuum, and therefore the size constraint of using a vacuum chamber is removed. Large areas can be coated using different techniques over a large substrate, which is especially advantageous for large area applications. In addition, omitting a vacuum chamber results in the removal of pumping and venting times which leads to an overall increase in throughput.

+2 Additive patterning

Printing involves the direct transfer of patterns onto a substrate. As opposed to subtractive patterning, which is based on the deposition of complete films that is later etched away in specific locations. The number of steps per pattern are reduced, and throughput is significantly increased.

+3 Waste

Photolithography requires the usage of large amounts of photoresist that is later removed after every patterning step. The nature of subtractive processing in general requires the removal of large amounts of predeposited material. In printing processes however, the ink is selectively placed, and the excess is generally reused.

+4 Flexible substrates

Research involving printing of electronics are generally performed at low enough temperatures for flexible substrates to be used. As a result, new application areas arise which were formerly difficult or impossible to do with conventional tools.

-1 Resolution

In general the resolution for printing processes may reach in the order of micrometers[1], while the state-of-the-art lithography equipment achieve resolutions in the order of nanometers. The size of the transistor or rather the channel length is directly influencing the switching speed of the transistor. The switching speed is stated in terms of the transit frequency (f_T):

$$f_T = \frac{1}{2\pi}\frac{\mu_{FE}}{L^2}(V_{GS} - V_T) \tag{7.1}$$

where μ_{FE} is the field-effect mobility, L the channel length of the transistor, V_{GS} and V_T the gate-source voltage and threshold voltage respectively.

-2 Ink

Although solution-processing brings many advantages, not every material can be made into a solution, and not every solution can be used in a printing process. In addition, it is important to control liquid properties such as viscosity, wettability, volatility, etc. A variety of inks are required for different electronic parts: conductor, semiconductor, and insulator. Finding or engineering the right type of ink is essential.

-3 Electronics fabrication

Compared to the graphics industry, much more stringent requirements are needed for printed electronics such as: continuous and homogeneous patterns, layer thickness control, low roughness, alignment for multiple layers, no damage from previously deposited layers, etc.

Significant advantages are to be found when printing electronics. Different printer types exist and an evaluation has to be made which is the most useful for electronics. A combination of multiple types may also be needed for different applications, similar to the graphics industry.

[1] with some exceptions such as microcontact printing and nano-imprinting.

7.1.2. TYPES OF PRINTERS FOR ELECTRONICS

In the graphics industry, different printer types are used for specific applications. An overview of the different printer types and their properties will therefore be presented to analyze which type is most appropriate for which application. Printing processes can in general be divided into two main groups: impact, and non-impact printers.[4–6]

IMPACT PRINTERS

For impact printers, the print master comes into contact with the target substrate. This type of printer generally maintains good reproducibility, since the same master is used for every print. These types of printers are used in highs speed production systems where minimizing the cost is the main driving force.

Fig. 7.1 presents the four main types of impact printers that are commonly used in the graphics industry, and illustrates their method of operation:

1. Flexography is based on ink transfer from raised elements of the print-master.
2. Gravure printing, transfers the ink through the recesses of the print master.
3. Offset printing controls the surface properties of the master and allows transfer through local ink adherence.
4. Screen printing uses a perforated master that allows ink to be squeezed through from the other side of the master.

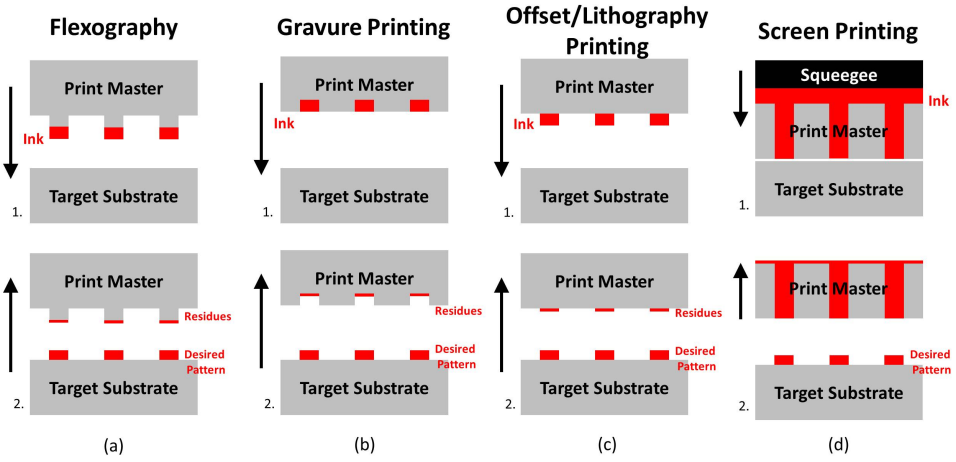

Figure 7.1: Schematic pattern transfer of four different impact-printer types: flexography (a), gravure printing (b), offset/lithography printing (c), and screen-printing (d).

NON-IMPACT PRINTERS

Non-impact printers do not have a physical master. Generally, these have a predefined digital master that is loaded into the printing system. It allows every print to be treated as a new run. Changes in the master can be easily made as opposed to the impact printer types, although the printing speed is much lower.

Although there are different types of non-impact printers such as electrophotography, magnetography and thermography among others, the inkjet printer is the most widely researched type of non-impact printer for electronics. In this process ink is propelled to the substrate either continuously or by drop-on-demand. Fig. 7.2 shows the schematic operation of different inkjet printer types. The inkjet printer is commonly used in research due to their ease in prototyping. Fully printed devices have also been achieved using this method [7, 8].

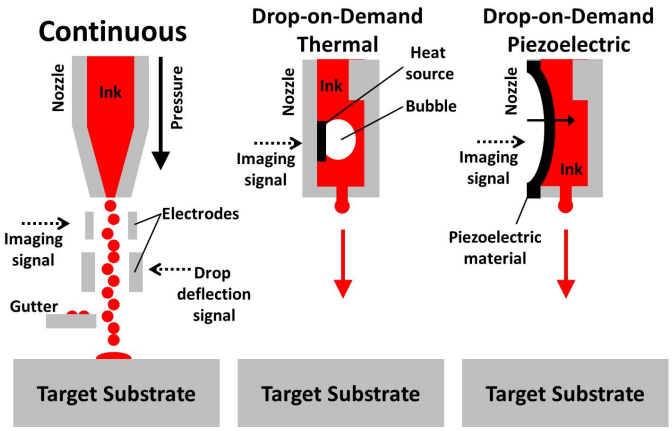

Figure 7.2: Inkjet printer operation schematic. Continuous inkjet (a), drop-on-demand by thermal inkjet (b), drop-on-demand by piezoelectric inkjet (c).

In recent years, alternative printer methods have been developed that are more appropriate for electronic fabrication purposes due to the higher resolution among other properties. Although not yet realized in a roll-to-roll process, these printer types show a high potential.

Microcontact printing is based on a flexible print master created from a lithographically patterned mold. This master can conformally transfer material to irregular surfaces by the raised pattern elements similar to flexography.

Nano-imprinting is a method that uses a master more closely related to gravure printing. The raised elements push away predeposited ink, resulting in patterns only in the recess positions of the print-master. The ink is at the same time treated during the im-

printing to solidify and keep the patterned arrangement. Both methods have shown sub-micron patterning results [9, 10].

A summary of the advantages and disadvantages of the impact and non-impact printer types are listed in Appendix E. Table 7.1 shows the typical resolution, ink viscosity, and pattern thickness for the various printer types.

Table 7.1: Typical resolution, ink viscosity and pattern thickness for various printer types [10, 11].

	Resolution (µm)	Ink Viscosity (Pa.S)	Pattern Thickness (µm)
Flexography	30-80	0.01-0.5	0.17-8
Gravure	50-200	0.01-1.1	0.02-12
Offset	20-50	20-100	0.6-2
Screen	30-100	0.5-50	3-30
Inkjet	15-100	0.001-0.1	0.01-0.5
Microcontact	1-20	~ 0.1	0.18-0.7
Nano-imprint	1-20	~ 0.1	0.18-0.7

7.1.3. PDMS STAMPS FOR PRINTING

In this work, a type of microcontact printing technology [9] has been used. This is due to the high resolution that can be obtained and the ease of preparation of the stamp/print-master. Although using a flexible stamp brings many advantages, there are a number of challenges that are being faced in this research. For the printing of liquid silicon these challenges will also be relevant, and solutions need to be investigated.

Commonly for microcontact printing a polymer stamp is used for transferring the ink. Often, the material used for this stamp is polydimethylsilazane (PDMS). The advantages of this material lies in the ease of preparation and its properties. Due to its flexibility, a conformal contact with irregular surfaces is possible, while at the same time having high mechanical stability. The stamp preparation allows also minor adjustments of the PDMS properties by changing the chemical formulation of the stamp, number of monomer units between junctions, junction functionality, and by curing conditions.

Using PDMS however also brings a number of challenges. Due to its highly hydrophobic nature, only apolar inks can be used on bare PDMS due to chemically inert methyl groups. Oxygen plasma and UV ozone treatment are widely used methods to make the surface of the material more hydrophilic. A top region rich in $SiCH_2OH$ groups are formed when oxidized. These regions are however more brittle and can form cracks in the stamp.

Another disadvantage, is the pattern deformation as a result of the raised element being pressed against the target substrate, which is also observed in flexography. Due to the high PDMS flexibility however, this deformation is more severe. A high aspect ratio leads to buckling and lateral collapse of the PDMS stamp, while for low aspect ratios there is a risk of roof collapse. Deformation can occur during pattern transfer similar to flexography, but also during the production of the stamp, and even during the inking. Patterns may deform from absorption of the ink material, that could lead to swelling.

Other factors that may affect the final printing result in this process are ink related: Adhesion of ink to PDMS, quantity of ink used, the ink viscosity and target surface adhesion of the ink are all factors that significantly impact the final printing result.

7.2. EXPERIMENTAL LIQUID SILICON PRINTING

7.2.1. PDMS STAMP FABRICATION

For a detailed flowchart of the stamp fabrication process, the reader is referred to Appendix D. PDMS stamps with micrometer sized patterns are created by using a lithographically patterned 4" wafer as a mold. The wafer has a PECVD TEOS SiO_2 deposited on top with a thickness of the pattern height. The layer is required to have an equal pattern height for both small and large patterns, since the silicon will serve as an etch-stop.

A commercially available PDMS prepolymer (Sylgard 184A, Sigma-Aldrich) and curing agent (Sylgard 184B) are used. The two materials are mixed in a weight ratio of 10:1, and degassed using a mixer/degasser (ARE-250, Thinky). The lithographically patterned mold was a silicon wafer with oxide patterns. Since PDMS adheres well to both silicon as well as silicon-oxide, a thin layer of hexamethyldisilazane (HMDS) was used to allow the effective removal of PDMS after curing, without damaging the stamp.

An edge is created around the wafer edge with cellular tape, and the PDMS mixture is poured over this mold. Trapped air bubbles from the pouring process are removed in a vacuum chamber (HERAEUS Vacuum Oven) under 500 mBar. Subsequently the setup was thermally annealed at 90 °C for 1 hour.

The cross-linked PDMS contains -$Si(CH_3)_2$-O- as the structural unit. After cooling to room temperature, the PDMS stamp could easily be removed without damaging the micrometer sized patterns. Fig. 7.3. shows the result of this stamp fabrication process. The smallest 1 by 1 μm feature has also successfully been filled and created.

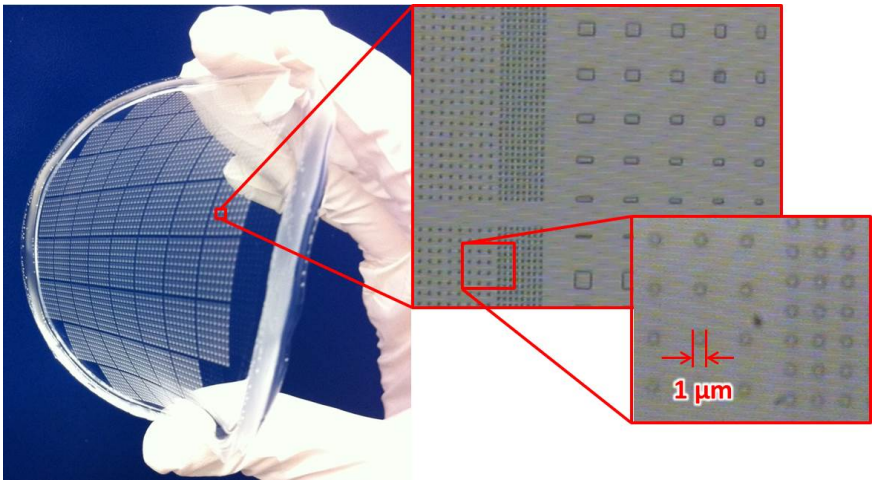

Figure 7.3: PDMS stamp used for flexography with microscope images of features as small as 1 µm.

7.2.2. LIQUID SILICON PRINTING EXPERIMENTS

Because of the poor wetting properties of the PDMS stamp, liquid silicon could not directly be coated on top of the patterned stamp. An alternative way of uniforming distributing liquid silicon, was to coat a dummy wafer by doctor blade coating first. The stamp is placed on top of this dummy wafer, and subsequently lifted and pressed against the target substrate. The schematic of this process is shown in Fig. 7.4.

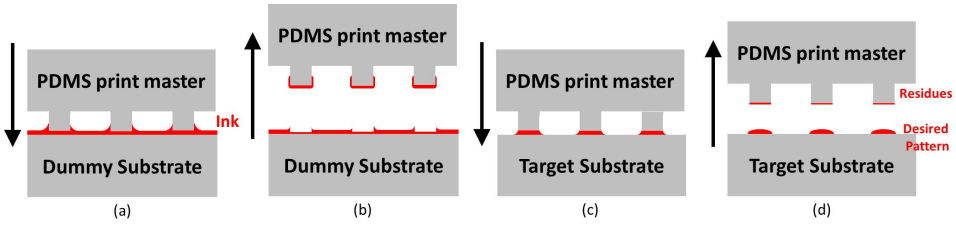

Figure 7.4: Liquid silicon flexography schematic. First the PDMS stamp receives liquid silicon that is precoated on a dummy substrate (a). Then the PDMS stamp is lifted, in this process the dummy wafer is left with the inverted patterns from the PDMS stamp (b). The stamp transfers the patterned liquid to the target substrate (c). Finally, the stamp is released from the target substrate (d).

The physics behind flexography is a bit more involving for microelectronic applications, than when applied to the graphics industry. When it comes down to the micrometer or nanometer feature sizes, fluid dynamics play a more significant role.

When the print master with inked patterns simply touch the target substrate, depending on the adsorption of the ink to the target substrate, ink may be transferred

with minimal deformation. However, in this work, a force is applied to the stamp, which would initially push the excess ink outside of the predefined pattern area. Subsequently when the stamp is lifted, a pressure difference is created underneath the pattern. This would pull the liquid back to the pattern position leaving a direct copy of the desired pattern. This process is illustrated in Fig. 7.5.

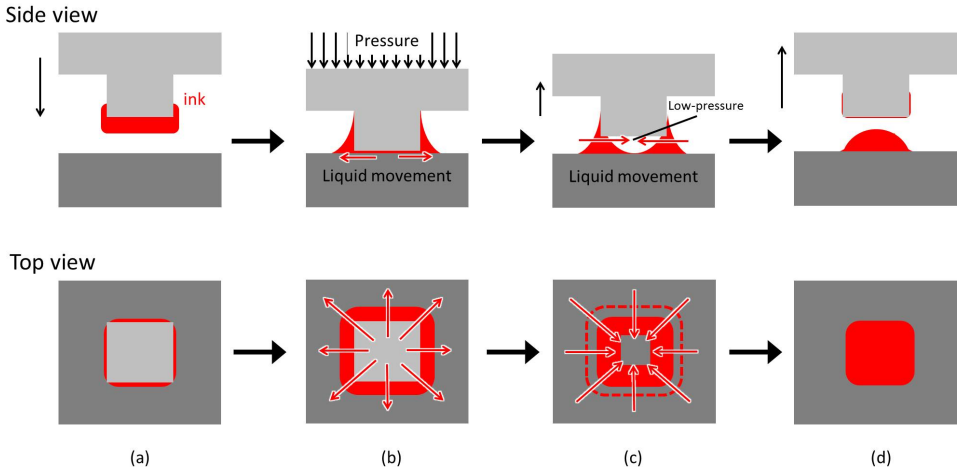

Figure 7.5: Flexographic printed process schematic on the micrometer scale from side view and top view. Inked master is positioned on the desired location (a). During pressure on the print master, the ink is pushed outside of the edge of the pattern (b). When the master is lifted the void under the pattern creates an under-pressure that pulls the previously squeezed out liquid back inside the defined pattern region (c). Finally when the stamp is completely lifted, the desired pattern is left on the target substrate (d).

Depending on various parameters in this process, undesired results may also be created such as the inverted version of the desired patterns. A variation of a number of parameters have been investigated in this work:

1. liquid quantity on the dummy wafer,
2. treatment of the liquid before transfer,
3. pattern density,
4. PDMS stamp pattern aspect ratio,
5. pressure of the PDMS stamp.

7.3. LIQUID SILICON MICROCONTACT PRINTING RESULTS

For the investigation of the printing parameters, the items can be subdivided into ink, stamp, and method properties. The quantity, and viscosity are both controllable parameters of the ink. As for the pattern density and aspect ratio, these can be controlled by stamp design. The pressure applied to the stamp is related to the method used for pattern transfer. In this work the transfer is conducted manually and an accurate control is difficult.

The quantity of liquid silicon on the dummy wafer has a direct influence on the amount of liquid transferred to the stamp and subsequently to the target substrate. When there is too much liquid supplied, the stamp patterns are overflown, and the excess is pushed to the non-patterned areas. This means that during the stamping, the excess liquid will also get transferred. As a result, individual patterns from flexography become indistinguishable. An effect similar to imprinting may be obtained. On the other hand, when too little liquid is supplied, there will be a risk that the stamp is insufficiently coated. Fig. 7.6 shows the effect of both extremes in liquid quantity. In this work, an amount of approximately 10 µL for an area of 5 by 8 cm, was found to give sufficiently good results.

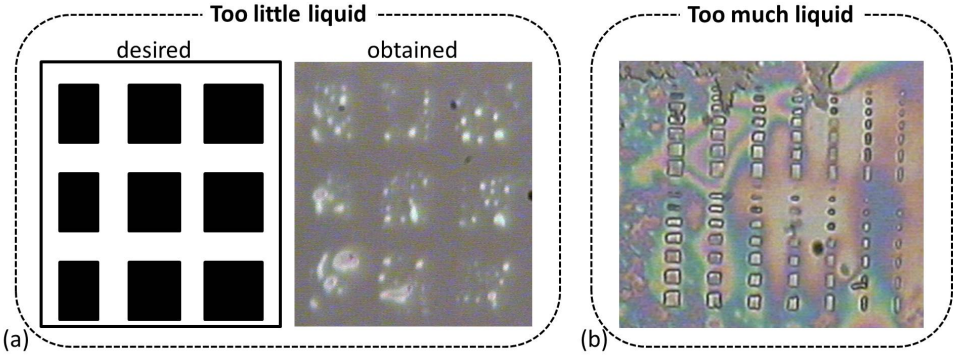

Figure 7.6: Effect of stamping with too little (a) and too much (b) liquid.

Liquid silicon cured before the transfer, increases its viscosity, and has a strong influence on the final printed result. When the ink has a low viscosity, the final stamping result would not show well defined patterns. In the other extreme, for high viscosities, inverted patterns were more likely to be formed. This is because the liquid behaves more gel-like, and does not flow as much as a liquid anymore. As a result, during the stamp placement, the liquid at the tips of the patterns are pushed outside, and the liquid is less likely to flow back. This effect is illustrated in Fig. 7.7.

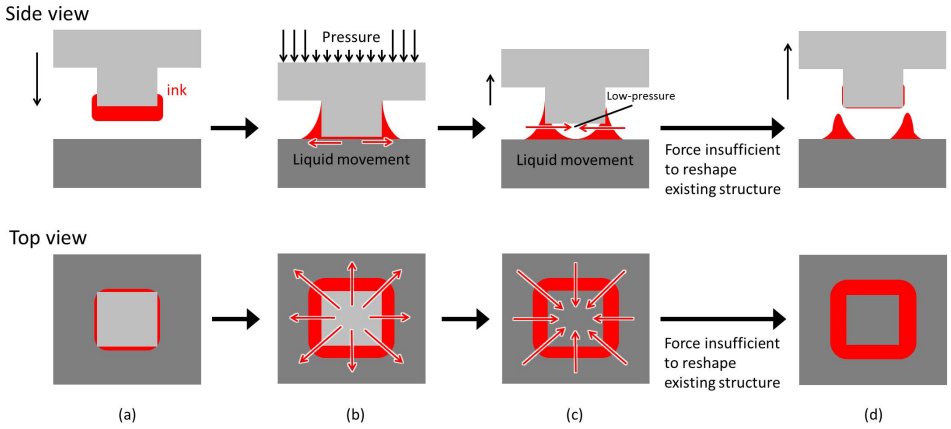

Figure 7.7: Flexographic printing process schematic of high viscosity inks from side and top view. Inked master is positioned on the desired location (a). During pressure on the print master, the ink is pushed outside of the edge of the pattern (b). When the master is lifted the void under the pattern creates an pressure difference which pulls the liquid back inside the defined pattern region. The high viscosity of the ink however, prevents this counter-movement (c). Finally when the stamp is completely lifted, the inverted pattern is left (d).

Depending on the density of the patterns, there is a possibility for inverted patterns to be created. Channeling of the recesses play an important role in this process. The liquid in these recesses unite and form a strong network that prevents movement toward the patterned area. This effect is particularly strong for higher viscosity inks and larger quantity inks, since the potential of neighboring patterns connecting will increase. Fig. 7.8 shows two optical microscope images illustrating the difference in pattern density.

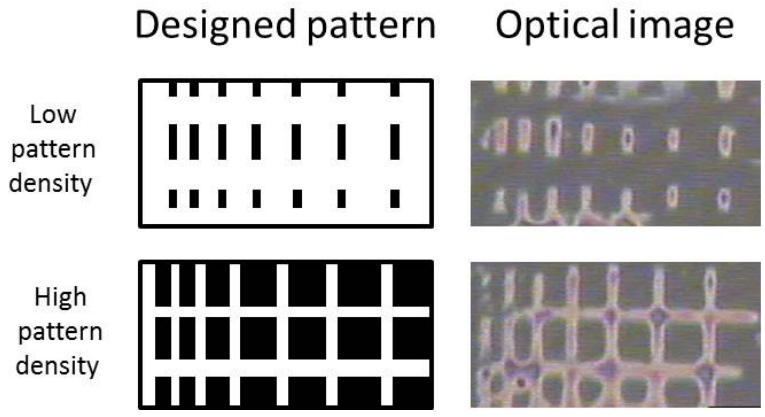

Figure 7.8: Flexographically printed images of high and low pattern density areas.

In flexography, patterns are created by a transfer of ink through the raised patterns. A typical issue for microcontact printing processes is the deformation of the stamp as a result of an applied force and pattern aspect ratio. When the patterns have a high aspect ratio, they are likely to be deformed by the pressure on the PDMS stamp. Decreasing the height too much would bring a risk that the ink contacts the stamp recesses, and subsequently get transferred. As a result, the inverted pattern is again more likely to be produced.

The investigated parameters show that an optimal condition needs to be found for the direct pattern transfer. Alternatively, patterns may be designed for inversion, similar to a gravure- or nano-imprinting process. Table 7.2 shows a summary of the variations and their extreme effects.

Table 7.2: PDMS stamping process variations and their extreme effects.

stamp parameter	effect high	effect low
ink quantity	pattern overflow/ inverted patterning	poor defined patterns
ink viscosity	inverted patterning	poor defined patterns/ poor stamp adherence
pattern density	inverted patterning	direct patterning
pattern height	pattern deformation/ direct patterning	inverted patterning
stamp pressure	pattern deformation/ inverted patterning	poor pattern definition/ direct patterning

As a proof of concept, solid silicon patterns were created after the microcontact printing of liquid silicon. A stamp with a pattern height of 1 µm was used and a dummy wafer was coated with 10 µL of CPS at 80 °C. Similarly, the target wafer was heated to 80 °C during the pattern transfer. This temperature allows a slight increase in viscosity of the liquid, and an improved adhesion was found for the target substrate.

After pattern transfer, the liquid patterns were cured for 30 minutes with a 10 mW/cm^2 intensity UV light, and subsequently thermally annealed at 350 °C for 1 hour. As a result the liquid silicon is transformed into solid amorphous silicon [12]. Raman spectroscopy confirmed the presence of a-Si within the patterned areas, and an absence of a-Si outside these areas. A stronger a-Si signal was found for the patterns compared to when a film of a-Si was created. This is due to the higher local a-Si thickness, confirmed by white-light profilometer to be above 1 µm while the a-Si film was around 250 nm. The profilometer image and height measurements are shown in Fig. 7.9.

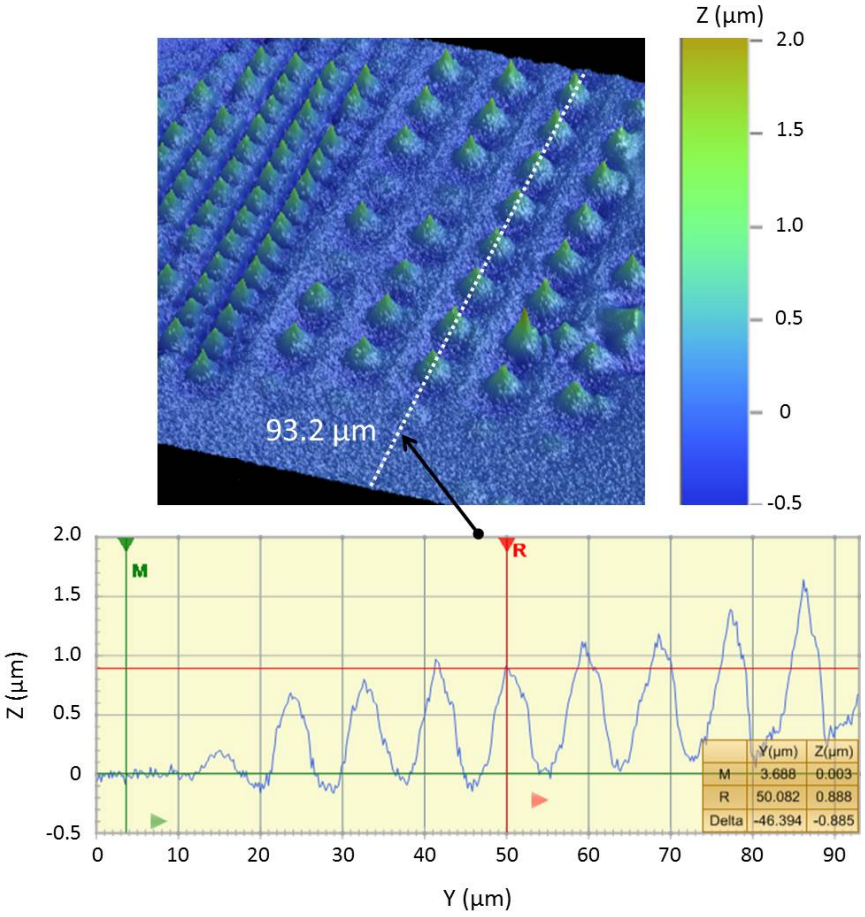

Figure 7.9: 3D optical profilometer images of the flexographically printed patterns annealed at 350 °C.

It had been observed that for a-Si films created from liquid silicon, a thickness of >400 nm would lead to a film cracking due to stresses accumulated during the annealing process[13] (see section 2.3.2). In this case however, 1 µm thick patterns were created without cracking of the patterns since they are isolated, which leads to a substantial stress reduction.

The resulting patterns have been crystallized using a XeCl excimer laser (308 nm, 28 ns), with fluences of 100, 200 and 300 mJ/cm^2. 100 mJ/cm^2 resulted in microcrystalline silicon by showing a mixture of a-Si and crystalline silicon peaks from the Raman spectrum. 200, and 300 mJ/cm^2 resulted in a strong poly-Si peak with no a-Si fraction. The Raman spectra were obtained from the patterned area. For thinner areas such as contin-

uous films, only the 300 mJ/cm^2 showed a small crystalline peak, while for lower energies the a-Si spectrum was dominant. This thickness dependency on crystallization has also been supported in section 4.4.2.

Both inverted patterns as well as direct patterns have shown to crystallize successfully to polycrystalline silicon while the area outside the patterns show no or minimal signs of silicon residues, as shown by the Raman spectra in Fig. 7.10.

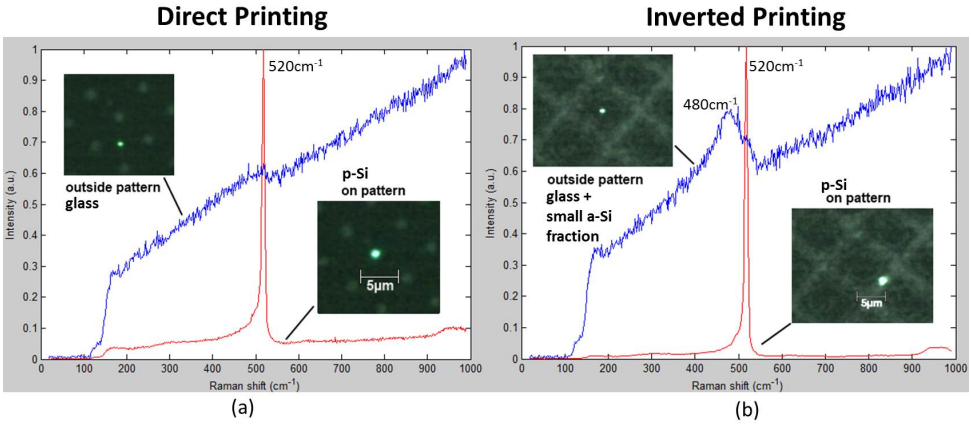

Figure 7.10: Raman spectra of stamped results showing the light pattern to be poly-Si and the dark area to have no silicon. Direct printing (a), and inverted printing (b).

7

7.4. CONCLUSIONS

Printing of electronics has many advantages compared to conventional fabrication processes. The most important one is the cost advantage from the high product throughput, similar to the graphics printing industry. However, it would not serve as a replacement to conventional processes, since the high performance and functionality cannot be matched by a printing process. It would much rather serve as a complementary technology, finding its advantages for large area, and cost dominated electronics.

A wide range of printer types exist, which can be divided into two categories: impact, and non-impact. Although non-impact printers such as inkjet are commonly used in research due to their ease in prototyping, high product throughput in roll-to-roll processes may only be achieved by impact printer types. When printing of electronics, more stringent requirements are needed, therefore, micro-contact printing and nano-imprinting are two new types that are introduced for electronic purposes.

In this work, micro-contact printing of liquid silicon patterns has been investigated,

due to the high resolution that can be obtained and the ease of print master preparation. A PDMS stamp has been used as the master. Since liquid silicon poorly wets on the PDMS surface, a dummy wafer has been used to uniformly distribute the liquid. The stamp is used to transfer the liquid from dummy wafer to a target substrate.

A number of parameters strongly affect the result of this printing process. Ink quantity and viscosity are parameters related to the ink, pattern density and pattern aspect ratio are related the stamp design, and stamp pressure is related to the printing method. Each of these parameters have been investigated.

A low liquid quantity affects the pattern definition, while a higher quantity overflows the stamp patterns. A low viscosity of the ink leads to a distortion of the pattern as a result of wetting properties. A higher viscosity gives a better pattern definition, but a risk of pattern inversion. This is because the ink during stamping is initially squeezed out of the patterned area. When the stamp is lifted, the pressure difference underneath the pattern pulls the liquid back in the desired position. For a highly viscous liquid this effect is weaker, and an inverted pattern may result.

Regarding the stamp design, a high pattern density is more likely to result in an inversion of the desired patterns. This is because during the squeeze-out of the stamping process, the ink forms a network with neighboring squeezed-out inks, which makes it more difficult for the liquid to reposition under the desired locations. Pattern aspect ratio is a common issue for micro-contact printing. A high aspect ratio patterns are prone to deformation, while low aspect ratios may lead to roof collapse (the inking and ink transfer of non-patterned locations). The latter is another cause for inverted patterning.

Finally the force applied to the stamp during transfer must be controlled. In this work, the force is applied manually and an accurate control is difficult to achieve. The effects of a large force is pattern deformation or roof collapse.

With the knowledge of the parameter investigation a proof of concept for the silicon micro-contact printing is presented. On top of a 4" wafer, 10 μL of CPS was coated at 80 °C, which marginally increased the CPS viscosity. The target substrate was also heated to the same temperature to improve the liquid adhesion. 1 μm pattern heights were developed for the stamp. After curing and annealing at 350 °C, a-Si patterns were obtained. The height of these patterns were approximately 1 μm, which is higher than the obtainable silicon film thickness from liquid silicon, due to cracks that occur from annealing above a thickness of approximately 450 nm. The stress is substantially reduced in this case due to pattern isolation.

Patterns, both desired and inverted, were crystallized by XeCl (308 nm, 28 ns) excimer laser at 200 and 300 mJ/cm^2. The crystallization was confirmed by Raman spectroscopy.

Micro-contact printing of liquid silicon has been performed and poly-Si patterns have been created in this additive process. The investigated parameters for printing can be further optimized. This work serves as a proof of concept and shows the potential of this method to be applied for roll-to-roll Si printing systems.

REFERENCES

[1] *Intel corporation, 22nm process technology,* online (2011).

[2] D. Mitzi, *Solution processing of inorganic materials* (John Wiley & Sons, 2008).

[3] V. Subramanian, J. B. Chang, A. de la Fuente Vornbrock, D. C. Huang, L. Jagannathan, F. Liao, B. Mattis, S. Molesa, D. R. Redinger, D. Soltman, *et al.*, *Printed electronics for low-cost electronic systems: Technology status and application development,* in *Solid-State Circuits Conference, 2008. ESSCIRC 2008. 34th European* (IEEE, 2008) pp. 17–24.

[4] H. Kipphan, *Handbook of print media: technologies and production methods* (Springer Science & Business Media, 2001).

[5] H. Yan, Z. Chen, Y. Zheng, C. Newman, J. R. Quinn, F. Dötz, M. Kastler, and A. Facchetti, *A high-mobility electron-transporting polymer for printed transistors,* Nature **457**, 679 (2009).

[6] M. Magliulo, M. Mulla, M. Singh, E. Macchia, A. Tiwari, L. Torsi, and K. Manoli, *Printable and flexible electronics: from tfts to bioelectronic devices,* Journal of Materials Chemistry C **3**, 12347 (2015).

[7] D. Kim, S. H. Lee, S. Jeong, and J. Moon, *All-ink-jet printed flexible organic thin-film transistors on plastic substrates,* Electrochemical and Solid-State Letters **12**, H195 (2009).

[8] S. Chung, S. O. Kim, S.-K. Kwon, C. Lee, and Y. Hong, *All-inkjet-printed organic thin-film transistor inverter on flexible plastic substrate,* Electron Device Letters, IEEE **32**, 1134 (2011).

[9] A. Perl, D. N. Reinhoudt, and J. Huskens, *Microcontact printing: limitations and achievements,* Advanced Materials **21**, 2257 (2009).

[10] S. Khan, L. Lorenzelli, and R. S. Dahiya, *Technologies for printing sensors and electronics over large flexible substrates: A review,* Sensors Journal, IEEE **15**, 3164 (2015).

[11] D. Tobjörk and R. Österbacka, *Paper electronics,* Advanced Materials **23**, 1935 (2011).

[12] T. Shimoda, Y. Matsuki, M. Furusawa, T. Aoki, I. Yudasaka, H. Tanaka, H. Iwasawa, D. Wang, M. Miyasaka, and Y. Takeuchi, *Solution-processed silicon films and transistors,* Nature **440**, 783 (2006).

[13] T. J. Garino, *The cracking of sol-gel films during drying,* in *MRS Proceedings*, Vol. 180 (Cambridge Univ Press, 1990) p. 497.

8

Conclusions and Recommendations

The goal of this work was to find a new method that would allow the fabrication of solution-based silicon transistors directly on top of low-thermal budget substrates. By achieving this goal the path towards extreme low-cost silicon electronics is opened.

Chapter 2 presented the literature work of the liquid silicon material in order to obtain a better understanding before delving into the optimization of its transformation. Chapters 3 and 4 focus on the development of the low-temperature transformation method, while chapters 5, and 6 discuss the implementation of this method for transistors on a silicon wafer and a paper substrate, respectively. Finally in Chapter 7, the potential of the material used in roll-to-roll process compatible additive patterning is investigated.

This concluding chapter is divided into three sections discussing in brief the key conclusions obtained in the respective chapters in section 8.1, giving additional remarks regarding these conclusions in section 8.2, and finally presenting a list of recommendations in section 8.3.

8.1. CONCLUSIONS

GENERAL

Solution-based poly-Si has been created directly on top of low-thermal budget substrates such as paper by excimer laser crystallization of polysilane. The material properties were investigated and a model has been created revealing that the underlying physics behind the liquid to solid laser transformation process is predominantly thermal rather than photochemical.

From this material, NMOS and PMOS TFTs with mobilities of approximately 100 cm^2/Vs, similar to those produced at high temperatures were created, in a process limited by a maximum temperature of 130 °C. These devices outperform solution-based alternatives such as organic and metal-oxide semiconductors. Poly-Si TFTs have also been produced directly on top of paper in a fully additive process with a maximum temperature of approximately 100 °C. Finally, an initial investigation toward micro-contact printing of liquid silicon was demonstrated.

This work presented a method which would open the pathway towards extreme-low-cost silicon electronics, including sensors and actuators, smart packages, and potentially wearable silicon electronics.

Liquid Silicon Ink

Silicon hydride compound precursors are used for solution-based processing that allow the transformation into solid silicon. Cyclopentasilane was found to be one of the stronger candidates for this purpose and has been used in this work.

In the conventional transformation process, a UV photopolymerization followed by a thermal annealing of CPS at 350 °C were required to create solid amorphous silicon. (Chapter 2)

Liquid Silicon TFTs in Other Works

In related works, TFTs have been fabricated using CPS, and high charge carrier mobilities could be obtained by controlling the location of individual large silicon crystal grains. Mobilities of 391 and 111 cm^2/Vs were obtained for NMOS and PMOS TFTs respectively.

While a minimum silicon annealing temperature of 350°C was used in other works, this temperature is too high for low-cost substrates that generally have a low thermal budget, such as PET, PEN or paper. Therefore an alternative material synthesis method is needed. (Chapter 2)

Curing Intensity

Curing of CPS does not only ring-open the molecules but also causes the ring-opened molecules to cross-link with each other. By increasing the curing intensity, properties similar to when the material is thermally annealed at 300°C are achieved.

Curing at an intensity of 300 mW/cm^2 led to a much more air-stable material than when CPS was cured with 10 mW/cm^2. Additionally, the increased intensity led to a bandgap reduction from 6.5 eV to 2.5 eV due to the stronger Si network formed. Increasing the UV curing intensity further shows promise of a stronger liquid silicon transformation.(Chapter 3)

Excimer Laser Crystallization

A high UV intensity tool, such as the excimer laser, was found to be able to crystallize liquid silicon directly without employing an intermediate baking step. Both CPS as well as polysilane could in this way be crystallized. The latter being more favorable due to a less violent reaction.

For a KrF excimer laser with a pulse duration of 20 ns, a trade-off between roughness and crystallinity resulted in a preferred laser irradiation condition of multiple pulses of 50 mJ/cm^2.

The preferred recipe could vary depending on the polysilane conditions, thickness, and laser related variations. (Chapter 3)

Simulations

A transient heat analysis model has been constructed for the investigation of the physics behind excimer laser crystallization of polysilane. Simulation results suggest that the primary physics behind the transformation is crystallization by melting, rather than a photochemical conversion.

Simulation results suggest a threshold fluence of 52 mJ/cm^2 when polysilane is exposed to a single excimer laser pulse, which is in good agreement with the physical data of Raman spectroscopy and SEM images.

A thickness variation was found to play a role in the shift of threshold fluence for a polysilane thickness below 100 nm. Multiple pulse irradiation was approximated by decreasing the density of the material. A similar shift of threshold fluence as for the physical data was observed.

The model used in this work has several limitations such as the parameter data variations, and the absence of outgassing, photochemical effect, and explosive crystallization. (Chapter 4)

Low-Temperature Silicon Oxide

In order to apply the new transformation method that allows low-thermal budget substrate usage, remaining fabrication temperatures for the creation of a TFT were also limited. A particularly important element in the TFT that is hampered by this limitation is the gate-oxide. Different low-temperature deposited oxides, based on ALD and RF-PECVD, were investigated by fabricating MOS capacitors. The best performing oxide was obtained from the RF-PECVD SiO_2 deposited at 120 °C. (Chapter 5)

Low-Temperature Liquid Silicon TFT on a Rigid Substrate

Poly-Si TFTs from crystallized polysilane have been fabricated by using conventional fabrication equipment on top of a rigid wafer. The process temperature has been limited to 130°C. By using a laser crystallization condition of 100 pulses of 70 mJ/cm^2, NMOS and PMOS TFTs have been created with mobilities of 91.5 and 87.7 cm^2/Vs, respectively. (Chapter 5)

Liquid Silicon TFT on a Paper Substrate

Liquid silicon was also crystallized into poly-Si on top of a paper substrate. TFTs has been fabricated using this material through a process limited to a maximum temperature of approximately 100 °C. Avoiding lithography, cleaning, and wet-etching steps, NMOS and PMOS devices have been fabricated with mobilities of 0.2 and 6.2 cm^2/Vs respectively.

Areas of improvement for these devices include: native oxide removal prior to oxide and metal deposition, optimized thickness control, crystallization and dopant activation conditions, improved alignment, and a further reduction in processing temperature. (Chapter 6)

PDMS Stamping of Liquid Silicon Patterns

Roll-to-roll fabrication brings the highest product throughput and will substantially reduce the cost. Different printer types exist, although more stringent requirements have to be taken into account when printing electronics.

Micro-contact printing by a PDMS stamp, was investigated in this work due to its high resolution and ease in print-master fabrication. Various parameters were investigated, both ink and stamp related: High values for ink related parameters such as liquid quantity and ink viscosity, result in pattern overflow and inverted pattern creation. A high stamp pattern density allows neighboring overflown liquids to connect, again leading to inverted patterns. Extremes for the pattern height could lead to pattern deformation or non-patterned areas being inked. Finally, a

high stamp pressure leads to pattern deformation, while a low pressure leads to poor pattern definition.
Using this knowledge, both direct and inverted poly-Si patterns have been successfully created from the printed patterns. (Chapter 7)

8.2. ADDITIONAL REMARKS

8.2.1. REGARDING POLYSILANE CRYSTALLIZATION

Although used as a liquid, the advantages of having CPS as the precursor has not been used to its full potential. Additive patterning processes of liquid silicon have only been investigated by one paper using inkjet printing [1]. Only recently imprinting of the CPS has been researched, although not for TFT applications [2]. It is believed that the lack of research in this field is because of its reactivity to ambient air, and that a printing system should therefore either be inserted inside a contained environment such as the glovebox, or a local nitrogen ambient should be prepared. In addition, CPS is not commercially available and therefore relatively difficult to obtain.

In the process of creating poly-Si from CPS, intensity of the UV curing has been found to play an important role in the cross-linking of the material. The process is photochemical and depending on its intensity could create a strongly cross-linked a-Si. Its results were compared to a sample cured with a low intensity UV light, and thermally annealed at 300°C.

Although Raman and absorption spectra showed similar results of both samples, due to the way that they are created, have significant differences. In the thermal case, the transformed material is uniform throughout the thickness, and in its cross-linking process hydrogen and silicon radicals throughout the film are released. For the photochemical process, the polysilane film consists of a stronger cross-linked part at the surface, and a less cross-linked part at the bottom. This leads to less hydrogen and silicon radical desorption.

For low-thermal budget substrates the photochemical process is preferred. Despite the fact that it does not uniformly cross-link throughout the depth of the film, it is a good precursor for laser crystallization for several reasons:

1. The material exhibits less stress and is therefore much less prone to initial film cracking.

2. The absorption spectrum is the same as for the thermally induced transformation.

3. Poorly cross-linked polysilane is more reactive to the excimer laser pulse, allowing

the film to crystallize at lower laser fluences.

4. Despite the presence of the reactive polysilane, the film shows sufficient stability and a strong decrease in ablation levels.

Increasing the UV curing intensity further will more strongly cross-link the polysilane however, crystallization is impossible using this type of UV source, since only the physical rearrangement of Si atoms defines the crystallization. To facilitate this, the atoms must be able to move either in a liquid state, or in a solid state at increased temperatures over longer periods of time (solid phase crystallization). This is also the reason why excimer laser treatments crystallize polysilane, since high temperatures are reached (T>1440 K), as observed from the simulation results.

In the transient heat simulation of the crystallization process, it was found that the underlying film is subject to temperatures of a few hundred degrees Celsius. For glass or silicon wafer substrates this temperature is not an issue, however for polymer or paper substrates, this increase of temperature above the substrate working temperature could impact the substrate. No significant harm however has been observed by the paper substrate, which is due to the short duration of the increased temperature. A chemical barrier such as a low temperature oxide on top of the paper substrate, could help protect the silicon film from possible harmful contaminants that may enter the silicon film at these increased temperatures.

8.2.2. REGARDING SI ON PAPER ELECTRONICS

Although fabrication of silicon directly on top of a paper substrate was challenging, the applications envisioned by this process requires some additional clarification.

Silicon on paper electronic applications. Some unique advantages for having high performance electronics on top of a paper substrate do exist however. Electronic packaging for instance can be made into smart packages by applying sensors that can measure the freshness of a carton of milk for example. This can be actuated by a change in color of the package, and for more complex operations, a signal can be emitted to inform the owner about the status of the package. This becomes possible due to the low-cost property of paper over polymers.

An additional advantage is that power consumption is low compared to the organic and metal-oxide semiconductor counterparts, due to the applicability of CMOS. As a result, more complex circuitry are able to operate at lower energies. An integration of a liquid silicon based battery, or solar cell may already be sufficient to power such devices.

Besides the advantages in circuit complexity, reliability is also significantly improved

using silicon, as opposed to organic and metal-oxide semiconductors that are sensitive to the open ambient and light. This becomes important when electronics on paper get related to applications concerning health, or monetary applications such as electronics on banknotes.

Finally, using paper as the substrate makes production of sensor nodes in general very attractive due to the low-cost. These sensor nodes may communicate with one another to form an internet-of-things system, which helps to collect data that allows optimization of certain processes such as marketing (by analysis of the distribution of flyers), or networking (by analysis of the routes taken by attendees of a conference through name tags).

8.3. RECOMMENDATIONS

8.3.1. SILICON FILM FORMATION

1. The manual doctor blade coating has been the cause of uniformity issues in this work. A controlled and automatic coating process is therefore advised for the production of uniform films. Spin-coating however has been avoided since it produces a lot of material waste, and is not scalable to a roll-to-roll process. Optimization of the alternative coating process should also be investigated. For instance by changing the wetting properties of target surfaces or the liquid itself.

2. More intense UV light sources can be used to improve the cross-linking of the film. The resulting material will have properties similar to a-Si, with a lower hydrogen content compared to the original polysilane, and a higher air stability.

3. Film roughness has a big impact in the final performance of the TFT. The roughness is caused by the outgassing of the film as well as the agglomeration of parts of the material. A reduction in hydrogen content has been found to greatly improve the ablative properties of the film. For low-thermal budget substrates, it is advised to use excimer laser pre-annealing, where low fluence laser pulses are irradiated on the film surface allowing a reduction of the hydrogen content without causing damage to the film. This effect has also been observed in other works [3, 4], and a deeper investigation is presented in Appendix A. It is important to note however that hydrogen is used as passivation for dangling bonds inside the material. Therefore, material properties could be improved by increasing the hydrogen content after crystallization. This can be done by a hydrogen plasma treatment [5, 6].

4. In this work, the KrF excimer laser has been used to crystallize polysilane. Other

types of excimer lasers would also give similar results. Different types of excimer lasers have different wavelengths that have their respective penetration depths. Longer wavelengths such as the XeBr (282 nm), XeCl (308 nm), or XeF (351 nm) excimer lasers, have deeper penetration depths, and in general result in a higher melting volume and therefore larger crystal grains. The various absorption coefficients and penetration depths of the different laser types are presented in Table 8.1.

Table 8.1: Polysilane absorption coefficient and penetration depths for various excimer laser systems.

	Absorption Coefficient (cm^{-1})	Penetration Depth (nm)
KrF (248 nm)	$2.49 \cdot 10^5$	40.2
XeBr (282 nm)	$2.47 \cdot 10^5$	40.5
XeCl (308 nm)	$2.32 \cdot 10^5$	43.1
XeF (351 nm)	$1.65 \cdot 10^5$	60.6

In addition, pulse duration plays a strong role in the crystallization process. A longer pulse duration generally results in larger crystal grains due to the slower cooling time.

8.3.2. SIMULATIONS

1. COMSOL Multiphysics uses a continuous model that simplifies simulations since a structure is modeled as a uniform component. Molecular behavior however, cannot be analyzed. Molecular simulations are based on the structure of individual molecules. Simulations of these are very time-consuming if large amounts are needed, however, the development of crystallization at the molecular level can be obtained, which can give a new insight on the crystallization process of polysilane.

2. Parameters extracted from polysilane for the simulations need to be supported by alternative measurements. One approach is to thermally anneal samples to 300°C to have a uniform cross-linking throughout the material. Although this sample would be slightly different from the photochemically reacted polysilane, it would give some additional information regarding the material. For the density, TOF-SIMS is recommended, which gives a depth profile of the coated material.

3. Since the high-intensity UV curing treatment causes the formation of a capping layer of highly cross-linked polysilane, the material in the simulation can be separated in a higher and a lower cross-linked portion (see Fig. 8.1). The separated materials then should have their own respective parameters extracted.

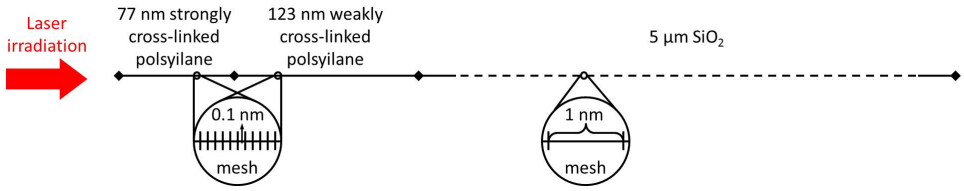

Figure 8.1: 1-Dimensional COMSOL simulation model of a polysilane on top of a glass substrate divided into a strongly and a weakly cross-linked fraction.

4. In this work, the simulation analyzes the phase transition from polysilane to molten silicon. The results suggest that the silicon transforms back to a-Si, although in reality the molten silicon transforms to c-Si. This transition can be incorporated in the simulation software. In addition, explosive crystallization is triggered by a positive net flux of latent heat that raises unmolten a-Si above its melting point. This could also be added to the simulation software, although the complexity could make the simulations time consuming.

5. The use of different substrates calls for different influences on the crystallized silicon film, especially for polysilane films below 100 nm. Simulation of other substrates is also useful, however, in general it is advised create a buffer layer of a sufficiently thick silicon oxide.

8.3.3. LIQUID SI TFT FABRICATION

1. In order to fabricate TFTs at lower temperatures, alternative equipment or tool settings are required. A key element in the TFT besides the semiconductor is the gate-oxide. A very high quality gate oxide is generally created at high temperatures. In this work, lower temperature, vacuum-based, methods have been used to create the gate-oxide such as ALD or plasma CVD at temperatures around 100 °C. These tools need to be further optimized for the TFT process. A reduction in temperature could be advantageous for flexible substrates to limit thermal expansion.

2. In order to scale up to roll-to-roll printing systems, vacuum processes need to be avoided. Therefore solution-based oxide fabrication processes need to be investigated. Potential solution-based oxide materials are: CPS [7], and per-hydro-polysilazane [8].

3. Many of the fabrication processing steps can be optimized to give the best TFT performance. Optimizations include: polysilane crystallization, gate-oxide, im-

plantation and dopant activation conditions. Specifically for the paper process, optimizations include: native oxide removal, maximum process temperature reduction, layer-to-layer alignment, barrier layer deposition on top of the paper substrate, and more controlled environment to ensure device cleanliness.

4. Gate-leakage current was relatively high for the Si TFTs on paper. The source of this leakage is linked to the condition prior, during, and after oxide deposition. Prior to oxide deposition, a native oxide is still present which forms a center for traps and can lead to an increase in the leakage current. This oxide can be removed by HF vapor etching. During the deposition, oxide is deposited in a vacuum ambient. It is likely that the paper is outgassing and that it influenced the quality of the deposited oxide. This can be solved by allowing the paper to degas for longer periods of time before deposition. After sample after deposition should not be increased to high temperatures due to the thermal expansion which can cause cracking of the film. It is therefore advised to further limit the maximum processing temperature.

5. A difference in device performance was observed for the PMOS and NMOS TFTs on paper, revealing the inferiority of the NMOS TFTs. This effect may be linked to the presence of native oxide which impacts the conduction band stronger than the valence band. Another reason may be the difference in implantation energies. Since the N-type semiconductor is created by the larger phosphorus atom, a high energy of 90 keV was necessary to go through the 100 nm gate oxide. The temperature in such a process increases to values close to 100 °C which may be sufficient to cause expansion of the sample. This issue can be solved by either removing the 100 nm gate oxide by HF vapor etching, before implantation, or reduce the temperature generated by the implantation process.

6. Once the fabrication process is optimized, more complex circuitry can be designed that specifically use the advantage of silicon TFTs over other solution-processable materials. It is advised to start with an inverter, followed by ring-oscillator, NAND, NOR and transmission gates.

7. Silicon devices were created directly on top of the paper substrate. Due to the heating of the surface of the paper substrate however, contamination issues may arise. It is therefore advised to use an oxide buffer layer to protect the silicon channel from possible contaminants.

8. In this work, Si TFTs were fabricated on paper. Other substrates also need to be investigated such as PEN or PET since these have favorable properties in terms of

mechanical and chemical stability. Higher performance devices may be fabricated using these substrates.

8.3.4. LIQUID SI PRINTING

1. In printing processes aimed for electronics fabrication, the large feature sizes may form an issue in obtaining high speed electronics, since the switching speed scales with the transistor channel lengths. Decreasing the printable feature sizes therefore requires investigation.

2. Different printing types have their specific advantages and challenges. An analysis has to be made to find out which printing method is the most suitable for liquid silicon, and which for the remaining process steps. It could very well be the case that different layers perform best with different printer types.

3. Further optimization of the stamping procedure can be done by replacing manual labor with automation. The stamping process for instance is currently done manually, and should be replaced with an accurate tool that could create a uniform pressure on the stamp.

4. In this work, the stamped patterns were thermally annealed and subsequently crystallized. A direct crystallization however will allow omission of the thermal annealing step, which in turn allows usage of low thermal budget substrates that generally have a lower cost. The process could for instance be conducted on top of a paper substrate although surface energy physics needs to be optimized.

5. As a first approach, the fabrication of Greek-cross resistors could give useful information on the quality of the produced solid silicon.

6. To create TFTs from stamped liquid silicon, alignment of multiple layers using lithography is an important approach to fully printed TFTs. In the conventional rigid TFT fabrication process (Appendix B) the silicon island formation step can be replaced by the stamping process. Alignment markers need to be created during the liquid silicon stamping process. After the formation of these markers, they can be used in subsequent lithography processes. The contact aligner can be used which requires manual alignment.

7. A next step would be to make an additive process by shadow masking. The process used in section 6.3 can initially be employed. In this process, the alignment is done by using an optical microscope and shadow masks. Step coverage needs to

be considered, since the pattern heights are much larger in this process. A thicker metal deposition is required. By using this process, devices on paper could be fabricated. In a sense, this process is fully additive although it cannot be considered as a fully printed device since vacuum is still required and material is still wasted by depositing on top of the shadow mask.

8. From a rigid substrate to a paper substrate additive patterning replaced the deposition, lithography, and etching process. For a fully scaled printing process additional alternatives have to be devised and optimized. The particular steps that are replaced by printing, are as follows:

Island formation by masked crystallization

Although this step could technically be scaled up, a number of complications are still present that would disappear once a printing process is used. The first complication is the fact that outgassing of the polysilane film causes the quartz mask to get dirty and cannot be reused many times. A second complication is that the non-crystallized area solidifies and may crack during a bending of the film. By producing separate islands this cracking can be prevented.

Gate-oxide

The deposition method used in this work requires vacuum conditions which is impractical in a roll-to-roll process. A solution-based alternative has to be found that can be fabricated at low annealing temperatures. Potentially this can also be created using cyclopentasilane, or other silane-based liquid compounds. In this way, only the channel can be coated by the liquid, while leaving the contact openings exposed for doping purposes, without having to subsequently etch the oxide.

Shadow-masking and metal evaporation

Although shadow-masking could be scaled up similar to the stencil used for a screen printing process, the evaporation process should be replaced due to the required vacuum ambient. The process can be replaced by printing of metallic inks [9].

Doping

Again due to the high vacuum requirement, dopants cannot be implanted into the polysilane material. Alternatively, a doped liquid material can be coated on top of the desired location and then through laser annealing be

diffused inside the silicon material. This has been done by using doped spin-on-glass for instance [10], but this could also be done by depositing doped liquid silicon [5, 11, 12] which can form the source and drains directly after laser crystallization.

The complete process flow is illustrated in Fig. 8.2. First the polysilane island is printed, after which the material is crystallized using the excimer laser. Then the liquid oxide material is printed for the gate-dielectric and treated until solidified. The gate metal is printed on top of the previously deposited oxide layer and also solidified at low temperature. Doped polysilane is printed in the source and drain regions, after which the dopant ions are activated by excimer laser annealing. Finally the contact metals are printed and solidified.

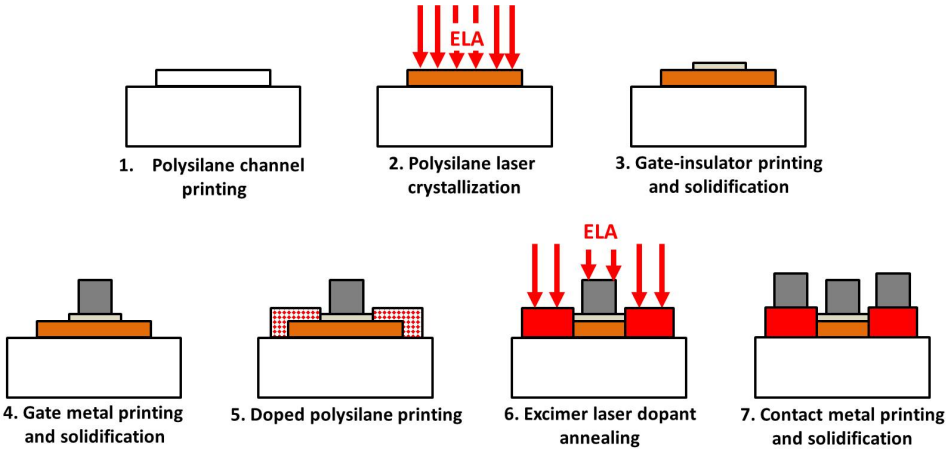

Figure 8.2: Process flow schematic of envisioned fully printed liquid silicon TFT process.

REFERENCES

[1] T. Shimoda, Y. Matsuki, M. Furusawa, T. Aoki, I. Yudasaka, H. Tanaka, H. Iwasawa, D. Wang, M. Miyasaka, and Y. Takeuchi, *Solution-processed silicon films and transistors,* Nature **440**, 783 (2006).

[2] T. Masuda, H. Takagishi, K. Yamazaki, and T. Shimoda, *Direct imprinting of liquid silicon,* ACS applied materials & interfaces **8**, 9969 (2016).

[3] J. Zhang, M. Trifunovic, M. Van Der Zwan, H. Takagishi, R. Kawajiri, T. Shimoda, C. Beenakker, and R. Ishihara, *Single-grain si thin-film transistors on flexible poly-*

imide substrate fabricated from doctor-blade coated liquid-si, Applied Physics Letters **102**, 243502 (2013).

[4] V. Privitera, S. Scalese, A. La Magna, A. Pecora, M. Cuscunà, L. Maiolo, A. Minotti, D. Simeone, L. Mariucci, G. Fortunato, *et al.*, *Low-temperature annealing combined with laser crystallization for polycrystalline silicon tfts on polymeric substrate,* Journal of The Electrochemical Society **155**, H764 (2008).

[5] T. Masuda, N. Sotani, H. Hamada, Y. Matsuki, and T. Shimoda, *Fabrication of solution-processed hydrogenated amorphous silicon single-junction solar cells,* Applied Physics Letters **100**, 253908 (2012).

[6] Y. Sakuma, K. Ohdaira, T. Masuda, H. Takagishi, Z. Shen, and T. Shimoda, *Effect of annealing and hydrogen radical treatment on the structure of solution-processed hydrogenated amorphous silicon films,* Japanese Journal of Applied Physics **53**, 04ER07 (2014).

[7] H. Tanaka, T. Aoki, I. Yudasaka, T. Shimoda, M. Furusawa, H. Iwasawa, D. Wang, and Y. Matsuki, *P-5: Solution-processed sio2 films using hydrogenated polysilane based liquid materials,* in *SID Symposium Digest of Technical Papers*, Vol. 38 (Wiley Online Library, 2007) pp. 188–191.

[8] D. Hishitani, M. Horita, Y. Ishikawa, H. Ikenoue, Y. Watanabe, and Y. Uraoka, *Forming sio 2 thin film by co 2 laser annealing of spin-on glass on polycrystalline silicon thin film,* in *Active-Matrix Flatpanel Displays and Devices (AM-FPD), 2013 Twentieth International Workshop on* (IEEE, 2013) pp. 163–166.

[9] N. Matsuhisa, M. Kaltenbrunner, T. Yokota, H. Jinno, K. Kuribara, T. Sekitani, and T. Someya, *Printable elastic conductors with a high conductivity for electronic textile applications,* Nature communications **6** (2015).

[10] D. Silicon, *Spin-on glass & spin-on dopants application procedure,* Online (2016).

[11] H. Tanaka, H. Iwasawa, D. Wang, N. Toyoda, T. Aoki, I. Yudasaka, Y. Matsuki, T. Shimoda, and M. Furusawa, *Spin-on n-type silicon films using phosphorous-doped polysilanes,* Japanese Journal of Applied Physics **46**, L886 (2007).

[12] T. Masuda, H. Takagishi, Z. Shen, K. Ohdaira, and T. Shimoda, *Phosphorus-and boron-doped hydrogenated amorphous silicon films prepared using vaporized liquid cyclopentasilane,* Thin Solid Films (2015).

A

Excimer Laser Pre-annealing for the Dehydrogenation of Polysilane

Excimer laser annealing was found to be effective in crystallizing polysilane films without harming underlying low thermal budget substrates. Hydrogen inside a silicon film during laser crystallization can eject and destroy the film structure. A hydrogen rich material such as polysilane is especially influenced by this process, and removal of hydrogen on top of low thermal budget substrates is necessary. Excimer laser pre-annealing (ELPA) at low laser fluences was found to be effective in reducing the hydrogen content and therefore reducing the levels of ablation.

In this chapter, ELPA of polysilane is investigated by analyzing the experimental results in section A.2. Subsequently the pre-annealing process was simulated in a transient heat analysis to understand its effect on the polysilane film in section A.3. Finally, this chapter is concluded by summarizing the obtained results and presenting recommendations.

A

A.1. INTRODUCTION

Excimer laser crystallization allows the treatment of thin layers of silicon without the thermal damage of the substrate or underlying layers. This is due to the short pulse duration (few tens of ns), and the high absorption coefficient of silicon (10^{5-6} cm^{-1}). The crystallization is the result of the absorption of the laser light translated to a sharp temperature increase of the material. As a result, the melting point of amorphous silicon (1200 °C) is reached.

Silicon intended to be crystallized, generally has a high hydrogen content. This is due to its synthesis which is meant for low-temperature processes. A PECVD Si deposition process commonly results a hydrogen content of the a-Si film of approximately 10 %.

When the excimer laser fluence is high enough (reaching the Si melting temperature), during the sharp temperature increase, the hydrogen explodes out of the film, known as ablation. This process leaves a very rough and damaged silicon film, which is detrimental to the performance of the final TFT devices.

Reducing the hydrogen content can reduce ablation. It would also allow even higher laser fluences to be irradiated on the film which would result in bigger crystal grains. This can be done by thermally annealing the hydrogenated silicon in a furnace above 400 °C for a few hours [1–3]. This, however, takes away the purpose of using an excimer laser crystallization method on top of low-thermal budget substrates.

An alternative for reducing the hydrogen content is to use the excimer laser itself at low laser fluences, which would avoid damage to the underlying temperature sensitive layers. Hydrogen ablation is only initiated at certain laser energy densities, generally reaching the film melting temperature. Exposing the film to fluences below this energy, does not melt the film, but removes the hydrogen content, especially at the film surface. The laser fluence can then be slowly increased to remove more hydrogen until the crystallization fluence is reached without significant damage from ablation. This has been shown by numerous other groups in the case of PECVD a-Si:H [4–6].

The hydrogen issue exists also in the case of liquid silicon, annealed at 350 °C. Zhang et al. therefore, used a thermal treatment of 650 °C to two orders of magnitude worth of hydrogen from the film[3] (from 10^{21} to 10^{19} [H] cm^{-3}). This allowed higher laser fluences to be irradiated on the sample without ablation. Later, Zhang et al., replaced the thermal dehydrogenation treatment with a laser induced pre-annealing[7].

In this work, experiments have been conducted regarding the laser induced pre-annealing process, since polysilane has much more hydrogen than thermally annealed amorphous silicon, and high temperatures cannot be used.

A.2. EXPERIMENTAL ELPA RESULTS OF POLYSILANE

In Chapter 3, SEM images of various excimer laser annealed polysilane samples have been presented and analyzed. A threshold fluence of 50 mJ/cm^2 was found. Films exposed to higher laser fluences were subject to high surface roughness from ablation and material outgassing.

SEM images have been analyzed from a film that has been pre-annealed with 100 pulses of 20 mJ/cm^2, followed by 100 pulses of 40 mJ/cm^2. After the pre-annealing treatment, the film morphology has not changed at an optically observable level. When exposing the pre-annealed film to a single pulse of 70 mJ/cm^2, the film gets a wavy texture, similar to when the untreated film is exposed to a single pulse of 50 mJ/cm^2. This proves that higher energy density pulses could be irradiated on films that have had a laser pre-annealing treatment. For this particular pre-annealing treatment the film still agglomerates at higher energy densities of 100 mJ/cm^2. The SEM images of the pre-annealed samples are presented in Fig. A.1.

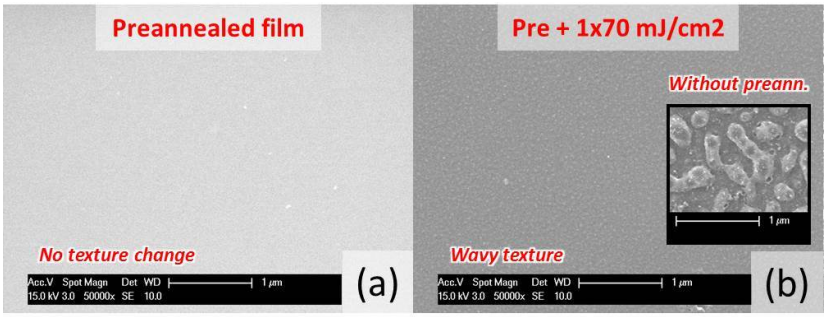

Figure A.1: SEM images of a excimer laser pre-annealed film (a), and a pre-annealed film with a subsequent exposure to 1 pulse of 70 mJ/cm^2 (b).

Pre-annealing can be extended to extreme measures. When exposing the film to sufficient low energy density pulses, and when the step height to the next fluence treatment is low, the maximum fluence that can be irradiated onto such a film can be significantly increased.

When looking at Raman spectra however, that for which a single pulse would have resulted in poly-Si now becomes a-Si. Although higher fluences can be irradiated after a pre-annealing laser treatment, even higher laser fluences are necessary in order to crystallize the film. This is due to the structural change that the material inhibits [8]: The film first turns into a densified a-Si. After this, the crystallization process requires higher fluences, while in the reactive polysilane case the fluence necessary for crystallization is

relatively low. A trade-off has to be made between keeping polysilane as a highly reactive material, and preventing ablation.

A.3. TRANSIENT HEAT SIMULATION OF ELPA OF POLYSILANE

In Chapter 4, single pulse laser annealing treatments have been simulated and matched to the experimental results. In addition, the scenario for multiple pulses was discussed. It was concluded that multiple pulses would lead to a porous silicon material due to the release of silicon hydride radicals and hydrogen. Other effects may have also played a role at the same time, although the dominating effect would be the structural change in material density for a specific, threshold level laser fluence (50 mJ/cm^2).

When the polysilane is treated however at lower laser fluences, although dehydrogenation and material outgassing occurs, since the temperature for crystallization is not reached, material densification occurs. This is also found for processes where the a-Si is dehydrogenated in a furnace [3]. A transition toward strongly cross-linked a-Si is present at these lower fluences. Consequently an a-Si structure requires higher laser energy fluences in order to be rearranged into a crystalline silicon structure.

Transient heat simulations confirm this increase in threshold fluence, since material properties similar to a-Si can be used when considering the pre-annealing process, which have shown to have higher threshold fluences in chapter 4.

A.4. CONCLUSIONS AND RECOMMENDATIONS

For the crystallization of polysilane, ablation plays a large role due to its high concentration inside polysilane films (67%). Exposing the film to laser energy densities below crystallization levels helps remove the hydrogen and silicon hydride radicals. As a result, higher laser fluences can be irradiated on the film without ablation.

Simulation results matching with experimental data, suggest that the material transforms into a-Si rather than becoming porous. This is in contrast to multiple pulse exposures at the threshold fluence of 50 mJ/cm^2. The pre-annealing fluence is low enough to increase the cross-linking of the film. Therefore, the threshold fluence is increased.

Optimization of the excimer laser pre-annealing process is required to obtain a good balance between the removal of hydrogen, while maintaining the high reactivity of polysilane.

REFERENCES

[1] P. Boher, M. Stehle, B. Godard, and J. Stehle, *Single shot excimer laser annealing of amorphous silicon: effect of hydrogen on the properties of the poly silicon,* in *MRS Proceedings*, Vol. 397 (Cambridge Univ Press, 1995) p. 417.

[2] K. Suzuki, M. Takahashi, and M. Saitoh, *Influences of hydrogen contents in precursor si film to excimer laser crystallization,* Applied Physics A **69**, S263 (1999).

[3] J. Zhang, R. Ishihara, H. Tagagishi, R. Kawajiri, T. Shimoda, and C. Beenakker, *Single-grain si tfts using spin-coated liquid-silicon,* in *Electron Devices Meeting (IEDM), 2011 IEEE International* (IEEE, 2011) pp. 14–5.

[4] P. Mei, J. Boyce, M. Hack, R. Lujan, R. Johnson, G. Anderson, D. Fork, and S. Ready, *Laser dehydrogenation/crystallization of plasma-enhanced chemical vapor deposited amorphous silicon for hybrid thin film transistors,* Applied physics letters **64**, 1132 (1994).

[5] D. Toet, P. Smith, T. Sigmon, T. Takehara, C. Tsai, W. Harshbarger, and M. Thompson, *Laser crystallization and structural characterization of hydrogenated amorphous silicon thin films,* Journal of applied physics **85**, 7914 (1999).

[6] V. Privitera, S. Scalese, A. La Magna, A. Pecora, M. Cuscunà, L. Maiolo, A. Minotti, D. Simeone, L. Mariucci, G. Fortunato, *et al.*, *Low-temperature annealing combined with laser crystallization for polycrystalline silicon tfts on polymeric substrate,* Journal of The Electrochemical Society **155**, H764 (2008).

[7] J. Zhang, M. Trifunovic, M. Van Der Zwan, H. Takagishi, R. Kawajiri, T. Shimoda, C. Beenakker, and R. Ishihara, *Single-grain si thin-film transistors on flexible polyimide substrate fabricated from doctor-blade coated liquid-si,* Applied Physics Letters **102**, 243502 (2013).

[8] P. Lengsfeld, N. Nickel, and W. Fuhs, *Step-by-step excimer laser induced crystallization of a-si: H,* Applied Physics Letters **76** (2000).

B

Flowchart of poly-Si TFT on a Silicon Substrate at Temperatures Below 130°C

From CPS ink, poly-Si could be created on top of temperature sensitive substrates. The first approach towards poly-Si TFTs on top of these substrates is to first fabricate these on top of a standard rigid substrate which is the silicon wafer. All processes following the CPS coating were conducted at a temperature below 130 °C.

Substrate

1. Starting substrate

A 4" diameter, 550 µm crystalline silicon wafer is used in this process.

2. Oxide deposition

This is the only step that is done at a temperature above 130 °C, used only for the sample preparation. A 850 nm thick PECVD TEOS based SiO_2 is deposited at 350 °C.

Poly-Si Synthesis

3. CPS coating

Inside the Glovebox, 10 µL of pure CPS is manually coated on top of the substrate by means of a doctor blade.

4. CPS curing

The coated CPS is cured for 30 minutes under a mercury-based UV lamp with an

intensity of 10 mW/cm^2. Subsequently the CPS is cured under a LED based UV light with an intensity of 300 mW/cm^2 on top of a hotplate at a temperature of 80 °C. As a result the CPS will be transformed into polysilane.

5. Polysilane Crystallization

The sample is sealed inside a holder with a quartz window. This allows excimer laser crystallization in a local nitrogen ambient. A KrF excimer laser with pulse duration of 20 ns is used with various laser fluences ranging from 40 to 70 mJ/cm^2 and numbers of pulses ranging from 1 to 100.

POLY-SI TFT

6. Cleaning Si procedure

After crystallization the sample is taken out of the sealed holder and cleaned by exposing it for 10 minutes in 99% HNO_3 at room temperature to dissolve organic contaminants, and subsequently for 10 minutes in 69.5% HNO_3 at 110 °C to dissolve metallic contaminants. After each step the wafer is rinsed for 5 minutes in DI water.

7. Lithography Si Islands

After an HMDS pre-treatment to improve photoresist adhesion, 2.1 µm thick positive photoresist is created on top of the sample by spin-coating (higher than the 1.4 µm standard due to topography created by the blade-coating process). This photoresist is softly baked at 95°C for 90 seconds.

Silicon channel island patterns are exposed using an energy density of 165 mJ/cm^2, after which the exposed photoresist is baked at 115°C for 90 seconds, developed for 57 seconds, rinsed with DI water, and finally hard baked at 100°C for 90 seconds.

8. Dry-etching Si islands

The poly-Si is etched at 20 °C, in a sequence of 10 seconds of oxide breakthrough, and 210 seconds for bulk etching.

9. Dry-etching Photoresist

Photoresist is removed by a plasma oxidation treatment of 1000 W for approximately 5 minutes with end-point detection.

10. Cleaning Si procedure

The sample is cleaned by exposure for 10 minutes of 99% HNO_3 at room temperature, and 10 minutes of 69.5% HNO_3 at 110 °C. 5 minute rinsing in DI water after each step.

11. Native oxide removal

Native oxide is removed just before the gate-oxide deposition step to ensure good interface properties. This is done by dipping the sample for 4 minutes in 0.55% HF. After which it is rinsed with DI water for 5 minutes.

12. Deposition Gate Oxide

50 nm thick silicon oxide is deposited at 120°C by RF-PECVD.

13. Cleaning Si procedure

The sample is cleaned by exposure for 10 minutes of 99% HNO_3 at room temperature, and 10 minutes of 69.5% HNO_3 at 110°C. 5 minute rinsing in DI water after each step.

14. Deposition Gate Metal

900 nm thick 99% Al with 1% Si is sputtered (PVD) on top of the sample at 50 °C.

15. Lithography Gate

2.1 µm thick photoresist is coated, gate patterns were exposed at 165 mJ/cm^2, and were developed for 52 seconds and hard baked.

16. Dry-etching Gate

The Al/Si is etched at 25 °C, in a sequence of 15 seconds of breakthrough, and 1 minute and 5 seconds for bulk etching at 500 W, and 45 seconds for over etching at a lower power of 250 W. As a result patterns the gate patterns were successfully etched without residues around the island patterns.

17. Wet-etching Metallic residues

Metallic residues that have attached to the sidewalls of the photoresist as a result of the dry-etching process, are removed by exposing the sample for 30 seconds to the chemical PES (a combination of phosphoric, nitric, and acetic acid). 75 nm of Al is removed by this process, and a 5 minute rinsing process followed.

18. Dry-etching Photoresist

Photoresist is removed by a plasma oxidation treatment of 1000 W for approximately 5 minutes with end-point detection.

19. Cleaning Metal Procedure

Now that there is metal on the sample, the wafer cannot be cleaned in the 69.5% HNO_3 at 110 °C. A separate bath of 99% HNO_3 for metals is used for 10 minutes to remove organic contaminants, after which the wafer is rinsed for 5 minutes in DI water.

20. Lithography N-dopants Mask

2.1 µm thick photoresist is coated, locations for n-type channels were exposed at 165 mJ/cm^2, and were developed for 52 seconds and hard baked.

21. Implantation N-dopants

Phosphorus ions were used to implant at an energy of 50 keV, with a dose of $2.0{\cdot}10^{15}$ ions/cm^2 at an angle of 7 degrees, and the flat of the wafers rotated at 22 degrees.

22. Dry-etching Photoresist

Photoresist is removed by a plasma oxidation treatment of 1000 W for approximately 5 minutes with end-point detection.

23. Cleaning Metal procedure

10 minutes of 99% HNO_3 at room temperature, designated for wafers with metals. 5 minute rinsing after each step.

24. Lithography P-dopants Mask

2.1 µm thick photoresist is coated, locations for p-type channels were exposed at 165 mJ/cm^2, and were developed for 52 seconds and hard baked.

25. Implantation P-dopants

Boron ions were used to implant at an energy of 17 keV, with a dose of $3.0{\cdot}10^{15}$ ions/cm^2 at an angle of 7 degrees, and the flat of the wafers rotated at 22 degrees.

26. Dry-etching Photoresist

Photoresist is removed by a plasma oxidation treatment of 1000 W for approximately 5 minutes with end-point detection.

27. Cleaning Metal procedure

10 minutes of 99% HNO_3 at room temperature, designated for wafers with metals. 5 minute rinsing after each step.

28. Dopant Activation by Excimer Laser Annealing

A KrF excimer laser with pulse duration of 20 ns is used with various laser fluences ranging from 40 to 70 mJ/cm^2 and numbers of pulses ranging from 1 to 100.

29. Cleaning Metal procedure

10 minutes of 99% HNO_3 at room temperature, designated for wafers with metals. 5 minute rinsing after each step.

30. Deposition Passivation Oxide

800 nm thick silicon oxide is deposited at 120°C by RF-PECVD.

31. Cleaning Metal procedure

The sample is cleaned by exposure for 10 minutes of 99% HNO_3 at room temperature, designated for wafers with metals. This step is followed by a 5 minute rinsing in DI water.

32. Lithography Contact Openings SD

2.1 µm thick resist is coated, contact openings above the silicon island for source and drain contacts, were exposed at 165 mJ/cm^2, and were developed for 52 seconds and hard baked.

33. Dry-etching Contact Openings SD

The 850 nm thick SiO_2 is etched at room temperature, in a sequence of 82 seconds of bulk etching with a power of 300 W to remove 820 nm, and 30 seconds for a soft landing at 100 W to remove 60 nm, which includes over-etching.

34. Dry-etching Photoresist

Photoresist is removed by a plasma oxidation treatment of 1000 W for approximately 5 minutes with end-point detection.

35. Cleaning Metal procedure

The sample is cleaned by exposure for 10 minutes of 99% HNO_3 at room temperature, designated for wafers with metals. This step is followed by a 5 minute rinsing in DI water.

36. Native oxide removal

Native oxide is removed just before the SD metal deposition step to prevent series resistance. This is done by dipping the sample for 4 minutes in 0.55% HF. After which it is rinsed with DI water for 5 minutes.

37. Deposition SD Via Metal

300 nm thick 99% Al with 1% Si is sputtered (PVD) on top of the sample at 50 °C.

38. Lithography Contact Openings SD

2.1 µm thick negative resist is coated, contact openings above the silicon island for source and drain contacts, were exposed at 300 mJ/cm^2, were separately cross-link baked, and were developed for 52 seconds and finally hard baked. The negative resist is only left at the locations where previously the oxide was etched away.

39. Dry-etching SD Via Metal

The Al/Si is etched at 25 °C, in a sequence of 15 seconds of breakthrough, and 25

seconds for bulk etching at 500 W, and 45 seconds for over etching at a lower power of 250 W. As a result patterns the gate patterns were successfully etched without residues around the island patterns.

40. Wet-etching Metallic residues

The sample is exposed for 30 seconds to the chemical PES. 75 nm of Al is removed by this process, and a 5 minute rinsing process followed.

41. Dry-etching Photoresist

Photoresist is removed by a plasma oxidation treatment of 1000 W for approximately 5 minutes with end-point detection.

42. Cleaning Metal procedure

The sample is cleaned by exposure for 10 minutes of 99% HNO_3 at room temperature, designated for wafers with metals. This step is followed by a 5 minute rinsing in DI water.

43. Lithography Contact Openings G

2.1 µm thick photoresist is coated, contact openings above the gate, was exposed at 165 mJ/cm^2, and was developed for 52 seconds and hard baked.

44. Dry-etching Contact Openings G

The 800 nm SiO_2 is etched at room temperature, in a sequence of 78 seconds of bulk etching with a power of 300 W to remove 780 nm, and 30 seconds for a soft landing at 100 W to remove 60 nm, which includes over-etching.

45. Dry-etching Photoresist

Photoresist is removed by a plasma oxidation treatment of 1000 W for approximately 5 minutes with end-point detection.

46. Cleaning Metal procedure

The sample is cleaned by exposure for 10 minutes of 99% HNO_3 at room temperature, designated for wafers with metals. This step is followed by a 5 minute rinsing in DI water.

47. Deposition all contact metals

1475 nm thick 99% Al, 1% Si is sputtered (PVD) on top of the sample at 50 °C, after an initial RF treatment that removed the native oxide of aluminum.

48. Lithography Contact Metals

2.1 µm thick photoresist is coated, the area outside metal contacts was exposed at 165 mJ/cm^2, and was developed for 52 seconds and hard baked.

49. Dry-etching SD Via Metal

The Al/Si is etched at 25 °C, in a sequence of 15 seconds of breakthrough, and 2 minutes for bulk etching at 500 W, and 1 minute 30 seconds for over etching at a lower power of 250 W. As a result the contact patterns were successfully etched without residues around the island patterns.

50. Wet-etching Metallic residues

The sample is exposed for 30 seconds to the chemical PES. 75 nm of Al is removed by this process, and a 5 minute rinsing process followed.

51. Dry-etching Photoresist

Photoresist is removed by a plasma oxidation treatment of 1000 W for approximately 5 minutes with end-point detection.

52. Cleaning Metal procedure

The sample is cleaned by exposure for 10 minutes of 99% HNO_3 at room temperature, designated for wafers with metals. This step is followed by a 5 minute rinsing in DI water.

C

FLOWCHART OF POLY-SI TFT ON A PAPER SUBSTRATE

Many of the steps used in the conventional microelectronic fabrication method have to be avoided when processing on a paper substrate. This concerns steps that use liquids in general, such as cleaning in HNO_3, or photolithography. Therefore, mostly additive patterning has to be used.

SHADOW MASK FABRICATION FOR CRYSTALLIZATION

1. Starting substrate

A 4" diameter quartz substrate is used with a thickness of 700 µm. In principle other transparent substrates can be used, but the laser energy should be adjusted depending on their absorption of the laser light.

2. Deposition of masking metal

100 nm thick 99% Al with 1% Si is sputtered (PVD) on top of the substrate at 50 °C.

3. Lithography Si Islands

After an HMDS pre-treatment to improve photoresist adhesion, 1.4 µm thick positive photoresist (SPR3012) is created on top of the sample by spin-coating. This photoresist is softly baked at 95 °C for 90 seconds.

Silicon channel island patterns are exposed using an energy density of 130 mJ/cm^2, after which the exposed photoresist is baked at 115 °C for 90 seconds, developed (MF322) for 57 seconds, rinsed with DI water, and finally hard baked at 100 °C for 90 seconds.

4. Wet-etching Island patterns

Island patterns of the Al/Si film are etched by exposing the sample for 1 minute to the chemical PES (a combination of phosphoric, nitric, and acetic acid). 100 nm of Al is removed by this process, and a 5 minute rinsing process followed. The remaining Si will oxidize and have insignificant effect to the irradiated laser energy in the crystallization step.

5. Wet-etching Photoresist

Photoresist is removed by using acetone at 40 °C for 1 minute.

6. Cleaning Metal Procedure

The sample is cleaned by exposure for 10 minutes of 99% HNO_3 at room temperature, designated for wafers with metals. This step is followed by a 5 minute rinsing in DI water.

SHADOW MASK FABRICATION FOR METAL PATTERNED DEPOSITION

7. Starting substrate

A 4" diameter, 550 µm thick crystalline silicon wafer is used in this process.

8. Deposition of Etch-stop Metal

4 µm thick 99% Al with 1% Si is sputtered (PVD) on the backside of the wafer at 50 °C.

9. Deposition of Masking Oxide

6.5 µm thick PECVD TEOS based SiO_2 is deposited at 350 °C.

10. Lithography Gate or Contact Metal

4.0 µm thick photoresist is coated, gate or contact metal patterns were exposed at 350 mJ/cm^2, and were developed for 57 seconds and hard baked.

11. Dry-etching Oxide Layer

The 6.5 µm SiO_2 is etched at room temperature, by bulk etching for 13.5 minutes at a power of 300 W, which includes over-etching.

12. Dry-etching Photoresist

Photoresist is removed by a plasma oxidation treatment of 1000 W for 4 minutes with end-point detection.

13. Cleaning Metal Procedure

The sample is cleaned by exposure for 10 minutes of 99% HNO_3 at room temperature, designated for wafers with metals. This step is followed by a 5 minute rinsing in DI water.

14. Deep Reactive Ion Etching (DRIE) through Silicon

The bulk silicon is etched with 1250 etch and redeposition cycles.

15. Dry-etching of DRIE deposited polymer

The polymer deposited during the DRIE process is etched away in an oxygen plasma at 1000 W for 30 minutes.

16. Cleaning Metal Procedure

The sample is cleaned by exposure for 10 minutes of 99% HNO_3 at room temperature, designated for wafers with metals. This step is followed by a 5 minute rinsing in DI water.

17. Wet-Etching Al etch-stop layer

The 4 µm thick Al film used for the DRIE etch stop is removed by wet-etching in PES for approximately 25 minutes, overetching is permitted. After this etching the wafer is rinsed in DI water for 5 minutes. The wafer is subsequently dried by spin-drying and baked at a temperature of 110 °C for 5 minutes, to remove any water residues.

Substrate

18. Starting substrate

A 4" diameter Si substrate of 550 µm thickness is used as a carrier for the paper substrate. Other rigid substrates could be used that are compatible to the fabrication equipment.

19. Paper attachment

A piece of paper of approximately 7 by 5 cm is attached to a silicon wafer by means of double sided, carbon tape.

Poly-Si TFT on Paper

20. CPS coating

Inside the Glovebox, 10 µL of pure CPS is manually coated on top of the substrate by means of a doctor blade. Due to the dewetting of the liquid from the substrate, the CPS is cured by UV light during the blade-coating to increase its viscosity. The intensity of the UV mercury light source was 10 mW/cm^2. When a relatively stable film is formed, a higher intensity UV light is used to freeze the polysilane with an intensity of 300 mW/cm^2 for 10 seconds.

21. CPS curing

The coated CPS is cured for 30 minutes under a mercury-based UV lamp with an intensity of 10 mW/cm^2.

22. Mask preparation - crystallization

The metallic patterned quartz mask is attached by tape with the metal side on the surface of the paper. The sample with the mask is attached to the sample holder. The sample holder is sealed to ensure an oxygen-free ambient during the crystallization process. A quartz mask on the sealed holder allows the irradiation of the laser pulse to the substrate.

23. Polysilane Crystallization

A KrF excimer laser with pulse duration of 20 ns is used with various laser fluences ranging from 40 to 70 mJ/cm^2 and numbers of pulses ranging from 1 to 100.

24. Polysilane oxidation

The sample is taken out of the holder and left in the open air, after removing the quartz mask, for at least a whole day to allow untreated polysilane to oxidize.

25. Deposition Gate Oxide

100 nm thick silicon oxide is deposited at 120 °C by RF-PECVD.

26. Mask preparation - Gate Deposition

A wax (Crystalbond™590) is placed around the edge of the silicon wafer and the edge of the shadow mask. After alignment under the optical microscope, the shadow mask is fixed by heating the wax around the edge using a soldering iron. The alignment should be checked during and after soldering.

27. Deposition Gate Metal

500 nm thick pure Al is deposited by evaporation. The temperature reached by the wafer is approximately 60 °C. The mask is subsequently removed by elevating the temperature of the edges to approximately 100 °C. Residues are removed by manual wiping with methanol.

28. Implantation N- or P-dopants

Depending on the desired dopant type, Phosphorus ions were used to implant at an energy of 90 keV, with a dose of $2.0{\cdot}10^{15}$ ions/cm^2 for n-type devices. Boron ions were used to implant at an energy of 30 keV, with a dose of $3.0{\cdot}10^{15}$ ions/cm^2 for p-type devices. Optionally, shadow masks could be prepared to have both types of dopants on a single wafer.

29. Dopant Activation by Excimer Laser Annealing

A KrF excimer laser with pulse duration of 20 ns is used with various laser fluences ranging from 40 to 70 mJ/cm^2 and numbers of pulses ranging from 1 to 100.

30. Mask preparation - Contact Deposition

A wax (Crystalbond™590) is placed around the edge of the silicon wafer and the edge of the shadow mask. After alignment under the optical microscope, the shadow mask is fixed by heating the wax around the edge using a soldering iron. The alignment should be checked during and after soldering.

31. Dry-etching Contact Openings

Contact openings were created by etching through the mask, 50 nm of SiO_2 in thickness, by using a plasma.

32. Deposition Contact Metal

Using the same shadow mask 500 nm thick pure Al is deposited by evaporation. The temperature reached by the wafer is approximately 60 °C. The mask is subsequently removed by elevating the temperature of the edges to approximately 100 °C. Residues are removed by manual wiping with methanol.

D

Flowchart of Liquid Si PDMS Stamping Process

For developing a stamping process, three elements need to be considered: the fabrication of the stamp mold, the creation of the PDMS stamp, and the creation of the silicon patterns.

Stamp Mold

1. Starting substrate

A 4" diameter, 550 µm crystalline silicon wafer is used in this process.

2. Oxide deposition

A 2 µm thick TEOS based SiO_2 is deposited at 350 °C by PECVD.

3. Lithography Patterns

After an HMDS pre-treatment to improve photoresist adhesion, 2.1 µm thick positive photoresist is created on top of the sample by spin-coating. This photoresist is softly baked at 9 5°C for 90 seconds.

Silicon channel island patterns are exposed using an energy density of 165 mJ/cm^2, after which the exposed photoresist is baked at 115 °C for 90 seconds, developed for 57 seconds, rinsed with DI water, and finally hard baked at 100 °C for 90 seconds.

4. Dry-etching Contact Openings G

The 2 µm thick SiO_2 is etched at room temperature, by dry-etching with a power of 300 W for 210 seconds, including overetching.

5. Dry-etching Photoresist

Photoresist is removed by a plasma oxidation treatment of 1000 W for approximately 5 minutes with end-point detection.

6. Cleaning Si procedure

The sample is cleaned by exposing it for 10 minutes in 99% HNO_3 at room temperature to dissolve organic contaminants, and subsequently for 10 minutes in 69.5% HNO_3 at 110 °C to dissolve metallic contaminants. After each step the wafer is rinsed for 5 minutes in DI water.

PDMS STAMP CREATION

7. Polymer Preparation

A PDMS prepolymer (Sylgard 184A, Dow Corning) is used together with a curing agent (Sylgard 184B) in a ratio of 10:1.

8. Mixing and Defoaming

The two chemicals are mixed and defoamed in a speed-mixer (ARE-250, Thinky).

9. Mold filling

The edge of the silicon wafer mold is taped off which would also create a fence that prevents the poured in PDMS from escaping the mold area. The tape used is a regular cellophane tape. A HMDS pretreatment is used to reduce the adhesion between PDMS and the mold surface. Subsequently the PDMS mixture is poured over the mold.

10. Defoaming and Baking

The mold together with the PDMS is placed inside a furnace which can be brought to vacuum (500 mBar). Repetitive vacuuming of the furnace allows the removal of trapped air formed by the PDMS pouring process. After defoaming, the sample is baked at 90°C for 1 hour.

11. Stamp removal

The cured PDMS stamp is removed from the mold surface after removing the surrounding tape.

LIQUID SILICON PATTERNS

12. Dummy Wafer Coating

10 µL of CPS is coated on a dummy wafer using a doctor blade, at an elevated temperature of 80 °C.

13. Ink Contact

The PDMS stamp is placed on top of the coated dummy wafer. Force is applied to the back of the stamp, to ensure that the whole stamp has contacted the liquid.

14. PDMS stamping

The PDMS with the liquid silicon ink is placed on top of the target wafer at a temperature of 80 °C, and a limited force is applied on the back of the stamp to transfer the ink.

15. Pattern formation and curing

The stamp is carefully removed and the resulting liquid silicon patterns are cured under UV light for 30 minutes. Subsequently either a thermal baking step could be conducted to transform the patterns into a-Si, or the polysilane can be directly crystallized by excimer laser annealing.

E

Advantages and Disadvantages of Printer Types

Flexography

+ Easy and straightforward manufacturing method,
+ no pixelation issues,
+ no cells so not prone to blockage,
- patterns on the print-master are prone to mechanical deformation,
- the physics of the transfer process often lead to a thicker printed pattern edge.

Gravure Printing

+ High image quality since patterns cannot be physically distorted,
+ uniform and low line-edge roughness,
+ good material compatibility,
+ wide range of thicknesses possible by cell design.
- Expensive print-master,
- Separate cells on the cylinder requires special design of cell spacing and size.

Offset Printing

+ No pattern deformation, print-master has only one physical level,
+ high printing quality and resolution,
+ master plates are easy to make and relatively inexpensive.
- Usable ink is limited due to material compatibility and constrained solution properties,
- solvent absorption issues arise.

Screen Printing

+ Not prone to deformed elements of master plate,
+ can deposit thick films, useful for specific applications.
- High viscosity inks are required to prevent bleed-out,
- binders are added to increase the viscosity which can hamper electric performance,
- inks may dry-out on the mask.

Inkjet Printing

+ Uses digital input that allows changes in the design,
+ less prone to wear problems compared to impact printer types,
+ compatible with different materials,
+ minimal waste of the materials.
- Pixelation issues,
- ink droplet position variation,
- complex drying process of droplets.

Microcontact Printing

+ Allows usage of variety of substrates,
+ high resolution due to lithography defined master.
- Polar molecules difficult to print due to stamp hydrophobicity,
- feature deformation,
- polymer swelling.

Nano-imprinting

+ High resolution,
+ high fidelity.
- Difficult alignment,
- high defect density,
- pattern deformation,
- residual layer needs to be removed.

ACKNOWLEDGEMENTS

Four years have passed since I started working on my PhD project. At the time, I knew it wasn't going to be easy. Due to the many challenges that I had to face, I have learned and developed skills that improved me as a person. With this I would like to express my appreciation and gratitude to the people that have helped me in this process.

First of all I would like to thank my supervisor dr. Ryoichi Ishihara. It is he who convinced me to pursue a PhD, and have helped me create the work you are reading today. A proper guidance that challenges me along the way, has made my project inspirational, and kept me motivated throughout the years. Putting the bar higher than I can imagine while showing appreciation to what is achieved. It allowed me to push myself further than my intentions had spanned. I thank you for the guidance, fruitful discussions, and overall support in my work.

My promoter Prof. Lina Sarro was a key person in creating a happy and inspirational environment. Not only focused on work related issues but also the personal problems, someone that is involved in the personal development is what I found her to be. She creates a relaxed atmosphere, but at the same time a sense of urgency. Thank you for your support during the past years.

Behind the scenes it is important to have the proper administrative support. I would like to thank Marjan Roozenburg, Marysia Laagendijk, Bianca Knot, Rosario Salazar, and Xandra Tober for their help. Always being available with a smile on their faces, it was a pleasure to work with you.

Before starting my PhD I have increasingly gained interest in the field of flexible electronics. As a result, I have pursued an internship as a researcher at the Organic Electronics lab in Tokyo University under the supervision of Prof. Takao Someya and Prof. Tsuyoshi Sekitani. It was my first encounter with flexible electronic research and I thank you and my colleagues: Tomoyuki Yokota, Yu Kato, Takeyoshi Tokuhara, Ikue Hirata, Jun Miura, Naoij Matsuhisa, Yuki Terakawa, Shigeyoshi Ito, and Naoya Take, during my stay for an unforgettable experience.

Now going into my project, liquid silicon for flexible electronics, I found, was one of those topics that could revolutionize the industry. Studies done by other groups have helped me gain the insight to this material. Therefore I would like to thank those who

contributed in the prior research in this field, especially the researchers at the Japan Advanced Institute of Science and Technology (JAIST). I have personally experienced in their lab working with the material and have gained new ideas and interesting discussions. I would like to thank Prof. Tatsuya Shimoda, dr. Takashi Masuda, Chikako Yotsuyanagi, and Masahiro Mizoguchi for teaching me their methods.

During my research I worked together with colleagues that have helped me directly in this research. I would like to thank Jin Zhang for her cheerful attitude and interesting discussions regarding liquid silicon. I would like to thank Michiel van der Zwan for his support in my first two PhD years, he was my liquid silicon process buddy, and together we have found the way to create poly-Si from polysilane using the excimer laser. I would like to especially thank Paolo Sberna for his full support and devotion to this topic in the final year of my PhD. As a physicist, he has given me new insight in the research, and I thank him for deep discussions in both work-related and private matters. He brought this work to a new level with his high intelligence in a diverse field. Thank you Jin, Michiel and Paolo, we made a great team together.

In this project I have had the opportunity to supervise master students and spread some of my knowledge in the field. I would like to thank Yuanxing Xu and Xingyu Liu for their enthusiasm and positive attitude in research. I hope that you will do well during your PhD candidacy. I would also like to thank guest researchers that have worked on liquid silicon in our group: Daisuke Hishitani from NAIST, and Akira Iwasaka and Yamazaki Ken from JAIST. Thank you for fruitful discussions regarding liquid silicon.

This work was conducted in a lab that allowed my research to flourish. I am fortunate and privileged to have been able to work in a lab which has led to the results that I have achieved. I know that there aren't many universities in the world that can offer such a wide variety of tools for the student to work on at a high level. I would therefore like to express my gratitude towards the staff members of the Else Kooi Laboratory (EKL), formerly known as DIMES Technology Center (DTC). I would like to thank the directors Carel van der Poel and Casper Juffermans for the organization of the engineering team and functioning of the lab. I would like to thank the members of the facility team: Jan Warmerdam, Robert Verhoeven, Ron van Viersen and Joost Berendse. I would like to thank the engineering team: Alex van den Boogaard, Johan van der Cingel, Koos van Hartingsveldt, Mario Laros, Silvana Milosavljevic, Gregory Pandraud, Tom Scholtes, Cassan Visser, Wim Wien, Johannes van Wingerden, Henk van Zeijl, Gilles Gobreau, Hugo Schellevis, Ruud Klerks, Jan-Cornelis Wolff, Loek Steenweg, and Wim van der Vlist. I would furthermore like to thank the staff members outside of the lab: Paul de Wit and Wim Tiwon. Thank you all for your hard work and open-mindedness for my unconven-

tional research.

Although fabrication of the electronics played a key role in my work, without measurements there is no way to confirm the quality of the conducted work. I would like to thank the staff members that have helped me in my measurements: Peter Swart and Lukasz Pakula.

Collaboration played another important part in this research, due to the unconventional nature of this work. I would first of all like to thank our neighboring PVMD (Photovoltaic Materials and Devices) Lab, more specifically the professors that allowed me to work in their labs: Prof. Miro Zeman and dr. Rene van Swaaij, the technical support staff: Martijn Tijssen and Stefaan Heirman, and the researchers: Guangtao Yang, Fai Tong Si, Martijn van Sebille, Paula Perez Rodriguez, Gianluca Limodio, and Do Yun Kim.

I would also like to thank members of other neighboring labs: Charles de Boer, Marco van der Krogt, Roel Mattern, Ewan Hendriks and Gaurav Nanda from Kavli Nanolab, and Rob Luttjeboer and Patrick van Holst from the Precision and Microsystems Engineering lab.

Outside of academia, I have also collaborated in my project with industry. I would like to thank Rene Sanders and Johan van Eemeren from Philips Innovation Services for the assistance in the KrF Excimer Laser. I would also like to thank ASML and Japan Display, for funding parts of my project.

My fellow members of the Thin-Film Transistors group, I would like to thank for the meetings we had together, sharing our ideas and the social events, both past and current members: Daniel Tajari Mofrad, Sten Vollebregt, Aslihan Arslan, Jin Zhang, Pengfei Sun, Michiel van der Zwan, Benjamin Mimoun, Paolo Sberna, Juan Alfaro Barrentes, Yuanxing Xu, Aniello Franseze, Sourish Banerjee, Ramin Barak, Shinnosuke Kawasaki, and Gautham Rangasamy.

Within the department there are many different groups that all use the cleanroom, and I have had the pleasure of working with these colleagues from many different fields within microelectronics: Jing Zhang, Rene Poelma, Filiberto Ricciardella, Fabio Santagata, Thu Hang Bui, Hong Wah Chan, Zahra Kolahdouz Esfahani, Nikolas Gaio, Yelena Grachova, Shivani Joshi, Aleksandar Jovic, Marta Kluba, Pan Liu, Violeta Prodanovic, Manjunath Ramachandrappa Venkatesh, Cinzia Silvestri, Joost Meerwijk, Robert Sokolovskij, Aleksandar Jovic, William Quiros Solano, Ronald Stoute, Xueming Li, Hengqian Yi, Amir Mirza Gheitaghy, Elina Iervolino, Jiaqi Tang, Bruno Morana, Alessandro Zompanti, Jia Wei, Hugo Perez Garcia, Agata Sakic, Lin Qi, Nie Meng, Gianpaolo Lorito, Theodoros Zoumpoulidis, Guiseppe Fiorentino, Sima Tarashioon, Jaber Derakhshandeh, Negin Golshani, Thomas Moh, Vahid Mohammadi, Fabio Rodrigues, Angela Longo, Berend van

Meer, Amir Sammak, An Tran, Maryam Yazdan Mehr, Caroline Mok, Nishant Lawand, Yinjie Shen, Jian Li, Salvatore Forte, and anybody else that I have forgotten to mention, thank you for all the good times we had.

Besides research, other activities have helped me develop more skills such as social or organizational. I have been a board member of Microelectronic Systems and Technology association for 3 years, and I have been president of the organization for a bit more than 2 years, organizing educational and social activities such as workshops, symposia and lunch lectures. This experience has taught me how to organize, lead, and interact with students, professors and experts in both industry and academia. To express my appreciation for this experience I would like to thank the members of the board during my membership that have helped me in this process: Aslihan Arslan, Sten Vollebregt, Ruimin Wu, Senad Hiseni, Imran Ashraf, Yao Liu, Vishwas Jain, Sourish Banerjee, Sivaramakrishnan Ramesh, Andrei Damian, Joost Meerwijk, Pelin Ayerden, Chockalingam Veerappan, Joost Hoozemans, Hui Jiang, Augusto Carimatto, and Nauman Ahmed.

After my efforts in MEST, I have joined the Faculty PhD Council, discussing matters regarding the PhD process, specifically the graduate school course system. I want to thank my fellow council members and those closely related to the functioning of this group: Martijn van Sebille, Johan Blanker, Violeta Prodanovic, Mingxiao Ma, Chayan Sarkar, Kishor Chandra, Thea Vuik, Tugce Akkaya, Pietro Pasotti, Robin Vismara, Yoeri Dijkstra, and Teun Janssen.

Other organizational activities that I have pursued include the organization of international conferences: ITC2014, and QCIT16 for which I would like to thank my supervisor and fellow Thin-Film Transistor group members with the help of organization. Finally, other organizational activities regarding PhD events, annual department reviews, Master Kickoff events, were made possible by Erica Radelaar, Orsi Toth, Diana Laaij, Lina Sarro, Marian Roozenburg, Anita Coetzee and Laya Zindel, and I would like to thank them for having given me the opportunity to do this.

Teaching courses has taught again improved my communication and connectivity skills, for which I would like to thank Silvana Milosavljevic, and Cassan Visser for having given me the opportunity to do this for the IC Technology course. I would also like to thank Nick van der Meijs and Anita Coetzee for giving me the opportunity to teach the first years bachelor course Begeleide Zelfstudie.

During my PhD I had ample opportunity to meet new people. One additional event that has helped me in this was the Sino-Dutch High Talent Summer School, in China, organized by Kees Beenakker. I would like to thank him, fellow organizers, and participants for this opportunity.

Besides work related activities I have found that sports always played a big part in my life. It has helped me stay healthy and release stress. Therefore I would like to thank Punch Basketball, that has given me this opportunity. Specifically the coaches, Marije van der Laag, Ana Verbanescu, Jurriaan Heuberger, Roel van de Hof, and of course all the fellow players.

Friends have helped me enjoy life. I would therefore like to specifically thank a few, although there are many more that have otherwise deserved to be listed. I would like to specifically thank Marc Sturkenboom, whom I have known since the age of 2, Derryl Lourens, Danny Dirkzwager, Joris Rem, and Gijs Vermeulen with whom I have celebrated life on countless occasions and are my hometown friends. I would also like to thank Jeroen Kruit, a colleague from the beginning of university life, and a fellow basketball player. Paolo Sberna, once again, deserves an additional attention since we see each other so often during the day. Friends from abroad, I would specifically like to thank Youssef Tadrous who was there for me when I started my internship in Japan. Tatsurou Mori, a childhood friend with whom I have met both in Japan and in the Netherlands. Jun Miura, whom I have known as a colleague at Tokyo University. Ogura Takatoshi and Takumi Naganuma, who I meet regularly when I come to Japan and who have also visited me in the Netherlands. Of course all my friends that I haven't mentioned here have helped me in life and I want to thank you for that.

My family are always important to me. Even if I don't openly express it, I truly love them. My parents, Yoshie and Mica, who are going through hard times now, I thank you for raising me into the person I am today. I hope that I make you proud with this, and that I am the kind of person that you had wanted me to be. My sister was the first person I wanted to be a role model for. It is her existence that made me a more responsible person, thank you Reina for this. I would also like to thank my indirect family, my uncles, and aunts, cousins, grandparents. You all know me from the very beginning and it is the fact that you have walked with me in life that I am the person today. Each and every one of you have contributed to my personality. Thank you for this.

Finally, and most importantly, my wife, Feifei. As I mentioned in the preface, she is the star of my show. She supports me through the hardest of times. I am honored to be able to spend the rest of my life with you. I hope that my busy working days for my PhD have not caused you too many troubles or worries, and I will do my best to try and spend more time with you. I feel so blessed that we have a child together, our little ray of light, Lucia. I love you, and hope that you can be proud of me, as I am of you.

List of Publications

Journal Publications

1. **M. Trifunovic**, P.M. Sberna, T. Shimoda, R. Ishihara. *Solution-processed polycrystalline silicon TFTs on paper.*, Advanced Electronic Materials, to be submitted.

2. **M. Trifunovic**, P.M. Sberna, T. Shimoda, R. Ishihara. *Solution-processed polycrystalline silicon CMOS fabricated below 130°C.*, Applied Physics Letters, to be submitted.

3. **M. Trifunovic**, P.M. Sberna, T. Shimoda, R. Ishihara. *Excimer laser annealing of polysilane analysis by transient heat simulations.*, Thin Solid Films, to be submitted.

4. **M. Trifunovic**, T. Shimoda, R. Ishihara. *Solution-processed polycrystalline silicon on paper.*, Applied Physics Letters **106**, 16 (2015), p.163502.

5. R. Ishihara, J. Zhang, **M. Trifunovic**, J. Derakhshandeh, N. Golshani, D.M.R. Tajari Mofrad, T. Chen, C.I.M. Beenakker, T. Shimoda. *Single-Grain Si Thin-Film Transistors for Monolithic 3D-ICs and Flexible Electronics.*, IEICE Transactions on Electronics **97**, 4 (2014), pp.227-237.

6. J. Zhang, **M. Trifunovic**, M. van der Zwan, H. Takagishi, R. Kawajiri, T. Shimoda, C.I.M. Beenakker, R. Ishihara. *Single-grain Si thin-film transistors on flexible polyimide substrate fabricated from doctor-blade coated liquid-Si.*, Applied Physics Letters **102**, 24 (2013), p.243502.

Patents

1. R. Ishihara, M. van der Zwan, **M. Trifunovic**. *Low temperature formation of thin-film structures.*, European Patent Office **WO2016068713 (A1)**,(2016).

2. R. Ishihara, **M. Trifunovic**, M. van der Zwan. *Low temperature formation of silicon and silicon oxide structures.*, European Patent Office **WO2016018144 (A1)**,(2016).

3. R. Ishihara, **M. Trifunovic**, M. van der Zwan. *Method of forming silicon on a substrate.*, European Patent Office **WO2014175740(A1)**,(2016).

4. R. Ishihara, M. van der Zwan **M. Trifunovic**. *Manufacturing a submicron structure using a liquid precursor.*, European Patent Office **CN105264664(A)**,(2016).

Conference Papers

1. **M. Trifunovic**, J. Zhang, M. van der Zwan, T. Shimoda, R. Ishihara. *29.1: Solution-Processed Poly-Si TFTs at Paper Compatible Temperatures.*, SID Symposium Digest of Technical Papers **46**, 1 (2015), pp.415-418.

2. R. Ishihara, J. Zhang, M. van der Zwan, **M. Trifunovic**, H. Takagishi, T. Shimoda. *32.4 Solution processed single-grain Si TFTs on a plastic substrate.*, SID Symposium Digest of Technical Papers **45**, 1 (2014), pp.439-442, (invited).

3. J. Zhang, **M. Trifunovic**, M. van der Zwan, H. Takagishi, T. Shimoda, R. Ishihara. *Single-Grain Si TFTs Fabricated on a Precursor from Doctor-Blade Coated Liquid-Si.*, ECS and SMEQ Joint International Meeting **64**, 10 (2014), pp.31-37, (invited).

4. **M. Trifunovic** J. Zhang, M. van der Zwan, R. Ishihara. *26.5: Solution-Processed Poly-Si TFTs fabricated at a maximum temperature of 150°C.*, Electron Devices Meeting (IEDM) 2014 IEEE International, pp.26-5.

5. R. Ishihara, J. Zhang, **M. Trifunovic**, M. van der Zwan, H. Takagishi, R. Kawajiri, T. Shimoda, C.I.M. Beenakker. *Single-grain Si TFTs fabricated by liquid-Si and long-pulse excimer-laser.*, ECS Transactions **50**, 8 (2013), pp.49-53.

Workshops

1. R. Ishihara, **M. Trifunovic**, P. Sberna, T. Shimoda. *Solution-processed LTPS on paper.*, In Proceeding of IDW'15, The 22nd International Display Workshop (2015).

2. **M. Trifunovic** T. Yokota, Y. Kato, T. Tokuhara, I. Hirata, I. Osaka, K. Takimiya, T. Sekitani, T. Someya, R. Ishihara. *OTFT with PNDT3BT-20 dispersed solution by drop casting method.*, Proc. 2012 19th International Workshop on Active Matrix Flatpanel Displays and Devices (AM-FPD), Kyoto, Japan, Jul 2012, pp. 203-206. ISBN:978-1-4673-0399-6.

About the Author

Miki Trifunović was born in Kyoto, Japan, in 1989. He received his cum laude B.Sc. in Electrical Engineering in 2010 at Delft University of Technology in the Netherlands.

He continued his studies at the university in the field of Microelectronics, and joined the department of Electronic Components, Technology and Materials (ECTM). His interest in the field of flexible electronics grew, which led him to pursue an internship as a guest researcher at the Someya-Sekitani Organic Electronics Lab in Tokyo University in 2011.

His master thesis was on solution-processed silicon transistors on top of a plastic substrate. He obtained a cum laude M.Sc. degree in 2012. In addition he received an honors certificate for which he needed to take an additional half year worth of courses under the topic of Flexible Electronics.

In 2012, he started his PhD in the same group under the supervision of Dr. Ryoichi Ishihara. The topic was a continuation from his research during his Master studies, focusing on solution-processed silicon transistors, this time on top of paper.

He has patented several parts of his work, and has presented his results in reputable scientific conferences such as IEDM14 and SID15. He has published his work in several journals, and has yet to publish his latest findings regarding paper electronics.

During his PhD he had ample opportunity to develop skills outside his research. For 2.5 years he was president of the Micro-Electronic Systems and Technology association. After this, he joined the department PhD council where he discussed with fellow council members about the development of the PhD trajectory. In addition, he helped in the organization of two international conferences (ITC2014, and QCIT16)

Teaching and supervision for both B.Sc. as well as M.Sc. students was another area that he has developed over the past years.

As a new challenge, he currently changed his research direction, and started his Post-doctorate research in Quantum Computing with Qutech and TU Delft, with the goal of bringing qubits and CMOS together through an efficient plan of interconnects.