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DFT Scheme for Hard-to-Detect Faults in FinFET SRAMs

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***Abstract*—Hard-to-detect faults such as weak and random faults in FinFET SRAMs represent an important challenge for manufacturing testing in scaled technologies, as they may lead to test escapes. This paper proposes a Design-for-Testability (DFT) scheme able to detect such faults by monitoring the bitline swing of FinFET memories. Using only five operations per cell, we are able to detect defects that cause deterministic, random, and weak faults. Compared to the state of the art, this leads to an improved detection capability at reduced area overhead.**

***Index Terms*—Hard-to-Detect Faults, DFT, SRAM, FinFET**

I. Introduction

FinFET technology enables the continuous downscaling of *Integrated Circuits* (ICs) as it shows improved short-channel behaviour and overcomes the growing leakage problem of planar CMOS technology [1]. Despite the benefits from FinFET technology, miniaturization of semiconductor circuits is still very challenging. For example, *Static Random-Access Memories* (SRAMs) manufactured at the limits of technology dimensions are statistically more likely to be affected by manufacturing defects [2]. Therefore, they require efficient testing, i.e., tests with a high fault coverage and low cost. This is particularly difficult as dynamic faults are more likely to occur in FinFET SRAMs than in previous technologies [3]. In addition, defects can cause *hard-to-detect* faults such as random and weak faults. Without proper detection schemes, these faults will lead to test escapes.

Many test approaches to detect memory faults have been proposed in literature. Strong, deterministic faults can be detected by schemes that rely on logic faults observation, such as March algorithms [4–8]. Yet, many of these algorithms do not target or have limitations detecting *hard-to-detect* faults. A more efficient way to detect these faults is to perform parametric testing. A well-known approach is to monitor the SRAM cell's current consumption [9]. More recently, the use of on-chip sensors has been proposed for this monitoring [10, 11]. A key advantage of this methodology is the short test time; only a short sequence of operations is required to detect defects. Nevertheless, this methodology also has drawbacks. The addition of new hardware sensors increases the power consumption, area overhead, and routing complexity.

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This paper advances the state of the art by presenting a new *Design-for-Testability* (DFT) scheme for testing FinFET memories. Rather than focusing on power consumption, this scheme identifies faults by using voltage sensors to monitor *bitline* (BL) swing. Results show that the proposed scheme, which requires only 5 operations per word, is able to not only detect strong deterministic faults, but also *hard-to-detect* faults such as random and weak faults. This reduces the number of test escapes and increases the overall product quality. The scheme also has a little area overhead, consuming an area equivalent to only six SRAM cells per memory column.

II. Hard-to-Detect Faults

Manufacturing defects may cause two types of faults in memories [12] :

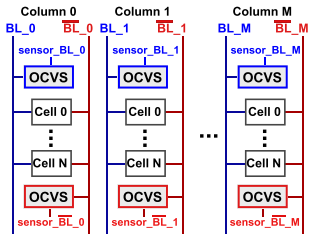
Strong Faults: This type of fault can be fully sensitized by a sequence of operations; i.e., by applying write or read operations. Strong faults can be expressed by fault primitives using the standard <S/F/R> notation [4]. Some of the faults can have a random behavior [13] (i.e., the cell switches to an undefined state or the BL swing at the sense amplifier's input is smaller than the required value).

Weak Faults: A weak fault can only be partially sensitized by an operation; it leads to parametric faults. From a functional point of view, these faults are undetectable as all write and read operations will pass successfully.

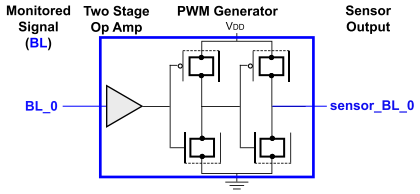
Strong deterministic faults always lead to logical faults and are therefore easily detected by fault observation (e.g., using March tests). This is not the case for strong random faults (as the read value is random), neither for weak faults (as they don't cause any logical faults, only parametric deviation). Therefore, random and weak faults are considered *hard-to-detect* faults – they require additional DFT circuitry that creates special conditions (such as high stress) or performs parametric testing to detect them.

III. DFT for Hard-to-Detect Faults

The DFT technique proposed in this work performs parametric analysis on the bitlines of each memory column. The scheme consists of monitoring the bitline swing using *On-Chip Voltage Sensors* (OCVS) and generating *Pulse-Width-Modulated* (PWM) pulses based on the charging and discharging rate of bitlines. By comparing the PWM signals of neighbouring cells, discrepancies can be observed during the



(a) DFT organization.



(b) On-Chip Voltage Sensor (OCVS).

Fig. 1: Proposed DFT scheme.

operations and defective cells causing *hard-to-detect* faults can be singled out.

The OCVS are integrated into both bitlines (BL and $\overline{BL}$); one sensor is required per bitline (Fig. 1a). The OCVSs operate in parallel by applying the same stimuli to all the cells in the same word. SRAM cells affected by defects will show poor charge and discharge pace and hence, the bitline voltages will differ from their neighbouring cells. This will create skews in the output of sensors, which are later used to identify cells causing *hard-to-detect* faults. It is important to highlight that this scheme monitors voltage levels on both bitlines in parallel and independently in order to detect faults, thus allowing a greater detection capability. Furthermore, the area overhead of each sensor is approximately equivalent to the area of three SRAM memory cells. Therefore, the cost of this scheme is around six cells per memory column.

Each sensor is composed of two functional blocks (Fig. 1b): (1) a Two-Stage Operational Amplifier, and (2) a PWM Generator. The two-stage operational amplifier monitors the BL swing and generates analogue output pulses. Next, the PWM generator converts the analogue pulses to a PWM digital signal that reflects the variations on the bitline swing. The output of the sensors are collected by a *Neighborhood Comparison Logic* (NCL) circuit [10] that processes them and generate a flag signal when a fault is detected.

IV. Validation of the Proposed DFT

In this scheme, all cells in a row must be tested with the same stimuli. To do so, the March algorithm $\Updownarrow(w1)$; $\Updownarrow(w0,r0,w1,r1)$ is adopted. First, the algorithm initializes all cells in '1'. Then, it sequentially applies the sequence write '0', read '0', write '1', read '1' to each row. This way, the DFT monitors the bitline swing during all possible operations.

To validate the proposed DFT, we analyze a representative case in detail, namely a resistive bridge (RB) defect between the two internal nodes of a 6T SRAM cell. Fig. 2 shows the input ($\overline{BL}$) and output waveforms of the OCVS sensor for

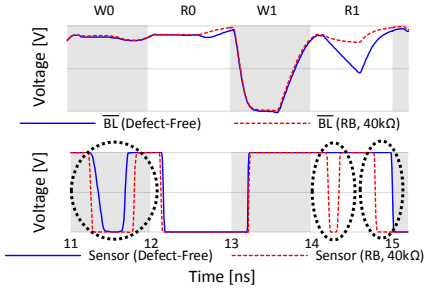


Fig. 2: Impact of RB=40 kΩ on OCVS output.

defect RB=40 kΩ when the March element $\Updownarrow(w0,r0,w1,r1)$ is applied. In the figure, blue lines represent a defect-free cell, while red dashed lines represent the defective cell. Conventional March tests cannot detect this defect, as the resistance of 40 kΩ does not sensitize logical faults. Comparing both bitlines, it is possible to see that the defective cell can't discharge its $\overline{BL}$ as fast as the defect-free cell, generating a *hard-to-detect* fault. This results in sensors outputting signals with a clearly different behavior, which is highlighted by the dashed circles. The NCL circuitry subsequently decides based on this behavior if there is a fault or not.

V. Conclusion

This paper proposed a DFT scheme for detecting weak and random faults in FinFET SRAMs. It compares the bitline swing between neighboring cells by identifying variations in the bitline charge and discharge rate during read/write operations. The proposed approach has a very small test time as it identifies *hard-to-detect* faults by executing only 5 operations per cell, while simultaneously improving the detection capability significantly. This does not only enhance the testing quality, but also reduces the test escapes.

References

[1] Bin Yu *et al.*, "FinFET scaling to 10 nm gate length," in *Digest. International Electron Devices Meeting,*. IEEE, 2002.

[2] P. Girard *et al.*, "Basics on SRAM Testing," in *Advanced Test Methods for SRAMs*. Boston, MA: Springer US, 2010.

[3] G. Harutyunyan *et al.*, "Test and Repair Methodology for FinFET-Based Memories," *IEEE Tran. on Device and Mat. Reliability*, mar 2015.

[4] S. Hamdioui *et al.*, "Testing static and dynamic faults in random access memories," in *VTS*, 2002.

[5] L. Dilillo *et al.*, "Resistive-Open Defects in Embedded-SRAM Core Cells: Analysis and March Test Solution," in *ATS*, 2004.

[6] S. Borri *et al.*, "Analysis of Dynamic Faults in Embedded-SRAMs: Implications for Memory Test," *Journal of Electronic Testing*, apr 2005.

[7] A. Benso *et al.*, "March AB, march AB1: new march tests for unlinked dynamic memory faults," in *ITC*, 2005.

[8] G. Harutyunyan *et al.*, "Memory Physical Aware Multi-Level Fault Diagnosis Flow," *TETC*, 2018.

[9] S. S. Sabade *et al.*, "IDDX-based test methods," *ACM Transactions on Design Automation of Electronic Systems*, apr 2004.

[10] F. Lavratti *et al.*, "Technique based on On-Chip Current Sensors and Neighbourhood Comparison Logic to detect resistive-open defects in SRAMs," in *LATW*, apr 2013.

[11] G. Medeiros *et al.*, "A defect-oriented test approach using on-Chip current sensors for resistive defects in FinFET SRAMs," *Mic. Reliability*, sep 2018.

[12] S. Hamdioui *et al.*, "An experimental analysis of spot defects in SRAMs: realistic fault models and tests," in *ATS*, 2000.

[13] S. Hamdioui, *Testing Static Random Access Memories*, ser. Frontiers in Electronic Testing. Boston, MA: Springer US, 2004, vol. 26.