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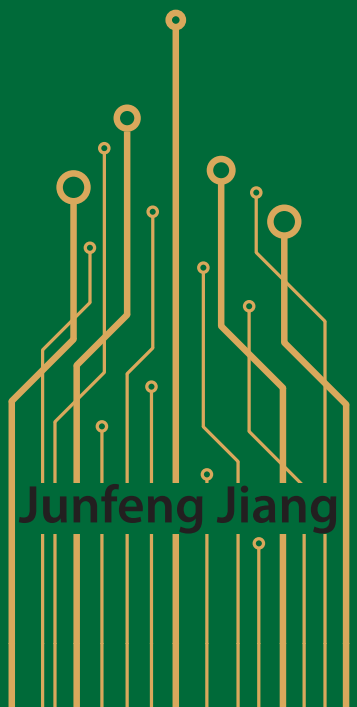

Junfeng Jiang

CMOS Wide-Bandwidth Magnetic Sensors for Contactless Current Measurements

J. JIANG

CMOS Wide-Bandwidth Magnetic Sensors for Contactless Current Measurements

Proefschrift

ter verkrijging van de grad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. dr. ir. T.H.J.J. van der Hagen
voorzitter van het College voor Promoties,

in het openbaar te verdedigen op
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Technische Universiteit Delft, Nederland

geboren te Dalian, China

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To my beloved parents and Xi

致我亲爱的父母和成茜

Table of Contents

Introduction 1

Since 1879, the world has been much brighter thanks to Thomas Edison and his invention of the light bulb [1]. This marked a major milestone in mankind's use of electricity as a bridge between different forms of energy, in this case transforming mechanical energy into electricity and then into light and heat. Since then, the generation, distribution, control and measurement of electricity has become an increasingly important topic and field of research.

1.1 Background

In the course of the 20th century, the use of electricity drastically changed the face of industry by replacing human labor with machines to improve manufacturing and production. However, the safe use of electricity requires the control of current. For instance, excessive current will burn out an incandescent lamp, and for that matter, most other electronic devices. From a macro-economic perspective, the accurate control of current is even more important. In 2015, over 3,000 million GWh electricity was consumed in Europe [2]. This corresponds to a constant current flow of over 1.5 trillion Amperes during the year. The consequences of failing to control such huge amounts of current are unimaginable.

The ability to measure current is an important premise to controlling it. Advances in physics and material science have revealed the relation between current and many other physical quantities such as heat, voltage and magnetic field. These allow current measurements to be made in many different ways. For instance, the flow of current in a conductor will generate heat, resulting in a measurable temperature change. This effect is the basis of a fuse, which will melt due to the temperature increase caused by excessive current flow. However, this approach has limited accuracy, and slow response due to the ambient temperature dependency and the time delay of the temperature change, respectively. These drawback can be addressed by measuring the voltage across a conductor, a so-called shunt resistor [3]. Applications include, but are not limited to multi-meters, battery monitoring systems in mobile devices, and circuit-breakers in distribution boxes. In high power systems, however, the use of shunt resistors is severely limited due to the lack of galvanic isolation. To achieve this, magnetic sensors can be used to measure the current's induced magnetic field (IMF). Such contactless sensors are often used in hybrid and electric vehicles, electric motors, switched-mode power supplies and smart grids [4].

For high volume, cost-sensitive applications, contactless current sensors are preferably implemented in CMOS (complementary metal-oxide-semiconductor) technology. This is because (1) they are based on silicon (Si), which is cheaper than the substrate materials used by other IC processes such as Gallium Arsenide (GaAs) and Indium Arsenide (InAs); and (2) most signal processing ICs are manufactured in CMOS processes. Therefore CMOS compatible sensors can be easily co-integrated into the signal chain with negligible added cost, occupying significantly less space compared to sensors implemented with discrete components.

Presently, contactless current sensor ICs are widely available in both CMOS and non-CMOS processes. They can be classified according to their working principle, namely Hall Effect (Hall) sensors, magnetoresistive (MR) sensors, fluxgates and pick-up coils. Of these, Hall sensors and pick-up coils can be manufactured in standard CMOS processes, while MR sensors and fluxgates require the use of ferromagnetic materials, which can be added with the help of post processing. For this reason, MR sensors and fluxgates will not be considered in this thesis.

Figure 1.1 400kV HVDC line under the English Channel (Copied from http://www.ifa2interconnector.com/the-project/).

Recent industrial and automotive developments has created a large demand for wide bandwidth contactless current sensors. One example is current sensing in high voltage DC (HVDC) transmission lines, shown in Figure 1.1, which are increasingly used for long distance and undersea power transmission. Compared to high voltage AC (HVAC) transmission systems, HVDC transmission systems have many advantages such as low construction costs and power losses, high power density, capability of transmission and stabilization between unsynchronized AC grids, and most importantly, integration of renewable energy sources into the existing power grid [5]. However, HVDC lines are sensitive to overloading, which can lead to catastrophic power failure and hence severe economic losses. Very fast current sensors, with response time in the

order of microseconds, are then required to prevent damage. Such bandwidths are beyond the reach of conventional CMOS magnetic sensors, especially if an adequate resolution for current measurement must be maintained.

Wide bandwidth current sensors are also required in switched-mode power supplies. Current trends towards higher power efficiency require higher switching frequencies and less power loss [6]. Moreover, the general industrial trend toward smaller power-conversion components requires smaller passive components such as inductors. This in turn requires switching currents at a few MHz [7]. To accurately control the resulting output voltages, currents need to be accurately measured in real-time, which is challenging for conventional current sensors.

The trend towards electrical vehicles (EV) and hybrid electric vehicles (HEV) can be expected to dramatically increase the use of electric motors. EV and HEV motors require high currents and voltages to produce enough horsepower and torque to compete with traditional internal combustion engine powertrains. In order to maximize power efficiency, these motors are usually controlled by PWM drivers. This also requires wide bandwidth current sensors so that the associated current transients can be captured.

Prior to this Ph.D. project, the bandwidth of CMOS contactless current sensors was limited to less than 100 kHz [8], which limited their use in many of the applications discussed above. In consequence, high speed contactless current sensors were typically implemented either with discrete components or in non-CMOS processes such as InAs (Indium Arsenide) [9], both of which are associated with higher costs.

1.2 Motivation and Objectives

This dissertation describes research into the realization of wide bandwidth magnetic sensors for current sensing in standard CMOS. The research progressively explores different ways of extending the bandwidth of CMOS magnetic sensors, based on Hall sensors and coils, mainly by improving their readout electronics at the circuit and system levels.

1.2.1 Bandwidth Improvement of CMOS Hall Sensors

A Hall sensor can be realized as a plate with four contacts, as shown in Figure 1.2. When a biasing current is conducted along the x-axis direction, moving charges experience the Lorentz Force (F_L) due to the presence of a magnetic field (B) along the z-axis. As a result, charges accumulated at the contacts along the y-axis will build up an electric field to cancel out F_L such that the net force experienced by the charges is reduced to zero to reach an equilibrium state. The sensor's output is then the voltage difference V_{out} between the two contacts along the y-axis. For a fixed plate dimension and biasing current, V_{out} is linearly proportional to the strength of B.

Hall sensor ICs are widely used due to their easy realization in standard CMOS. They are normally fabricated as n-well plates, and have sensitivities ranging from 100 V/A·T to 400 V/A·T

[10-13]. With proper interface circuitry, CMOS Hall sensor systems can achieve offsets below 10 μT [8, 14], bandwidths up to 1 MHz [15], and sub-μT resolution [16]. Hall sensors can also be realized in GaAs and InAs processes. Compared to CMOS, these have higher electron mobility, resulting in Hall sensors with greater sensitivity [17].

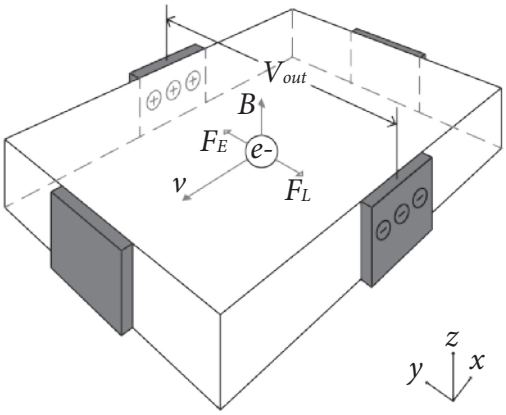

Figure 1.2 Simplified working principle of a Hall sensor.

Hall sensors are essentially resistors, therefore for a given signal-to-noise ratio (SNR), their useful bandwidth is fundamentally limited by thermal noise. A further increase in bandwidth causes a proportional increase in noise power, and thus a less SNR.

Intrinsically, the bandwidth of CMOS Hall sensors is comparable to that of non-CMOS Hall sensors, e.g., InAs Hall sensors. However, due to their lower sensitivities, CMOS Hall sensors suffer more from noise, and hence achieve worse resolution within the same bandwidth. In other words, CMOS Hall sensors require smaller bandwidths, compared to non-CMOS Hall sensors, to achieve the same resolution. Unfortunately, there have been very few means to improve the bandwidth of CMOS Hall sensors except by using more power.

The offset of a typical CMOS Hall sensor can be as large as 10-50 mT, which is often much larger than the maximum signal of interest. This limitation can be overcome by a dynamic offset cancellation technique that was first proposed in 1989 [18]. Known as the "spinning current technique," it is now used in the interface circuits of nearly all of today's CMOS Hall sensors. It involves periodically rotating the direction of the biasing current and the location of the readout terminals, such that the offset and signal can be separated and processed individually. However, it has the drawback that low-pass filters (LPFs) are then required to suppress the offset ripple due to the spinning current operation, which severely limits the system bandwidth, e.g. to below 50 kHz [8].

To overcome the bandwidth limitation associated with the spinning current technique, a first research goal was to obviate the need for LPFs in the signal path. This meant that new methods of suppressing the spinning ripple of Hall sensors had to be found. Inspired by chopper

instrumentation amplifiers, this was achieved with the help of ripple reduction loops (RRL) [19] and multi-path architectures [20].

Despite the new ripple reduction methods, the bandwidth of Hall sensors is ultimately limited by thermal noise for certain resolution specifications, and cannot be improved at the circuit level. A further increase in bandwidth requires innovation at a higher level, i.e. the system level.

1.2.2 Pick-up Coils

Compared to Hall sensors, pick-up coils (Figure 1.3) are better suited for high frequency current sensing due to their differentiating characteristic. In the presence of a changing magnetic field B, a pick-up coil will generate an electromotive force (EMF) ε which is proportional to the time derivative of the magnetic field:

$$\varepsilon = nA\frac{dB}{dt} \tag{1.1}$$

where n is the number of windings of the pick-up coil, and A represents the winding area. For an input magnetic field B at frequency f, B can be expressed as:

$$B = B_0 \cdot \sin(2\pi f \cdot t) \tag{1.2}$$

in which B_0 represents the amplitude of the magnetic field. With Equation (1.2), Equation (1.1) can be rewritten as:

$$\left|\varepsilon\right| = 2\pi f \cdot nA \cdot B_0 \tag{1.3}$$

which suggests that the amplitude and power of the output ε is proportional to f and f^2, respectively. Due to the presence of a source resistance R, thermal noise is expected at the output of a pick-up coil with the power N^2 expressed as:

$$N^2 = 4kTR \cdot f \tag{1.4}$$

Equation (1.3) and (1.4) suggest that the SNR of a pick-up coil is linearly proportional to its input frequency f, making them better suited for measuring high frequency magnetic fields.

Despite the fact that pick-up coils can cover a wide frequency range, e.g. 50 kHz to 1 MHz [21], their sensitivity decreases at low frequencies. This drawback limits their use in wide bandwidth systems that need to cover DC and low frequency signals as well.

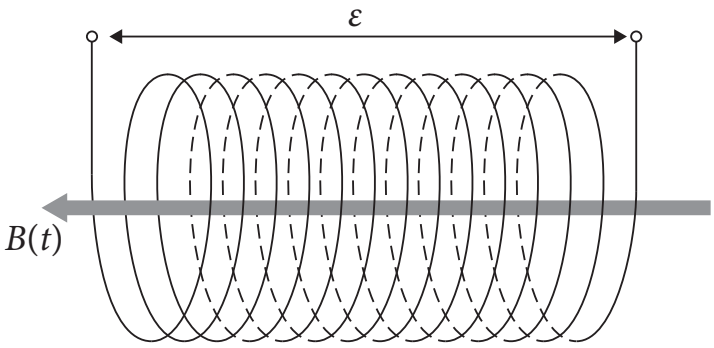

Figure 1.3 Pick-up coil.

Considering the fact that Hall sensors and pick-up coils are suited for measuring low frequency and high frequency magnetic fields respectively, combining Hall sensors and pick-up coils appears to be a promising system innovation. The second research goal of this thesis is to build a hybrid magnetic sensor by combining Hall sensors and pick-up coils on a single die, so that the overall system can cover a wide bandwidth from DC to beyond 1 MHz.

1.2.3 Hybrid Magnetic Sensors

The idea of realizing hybrid magnetic sensors by combining different types of sensors, e.g., Hall sensors and pick-up coils, is not new, and some systems have been reported in the literature [22-24]. These can be divided into closed-loop and open loop-loop systems. In a closed-loop system, an unknown magnetic field is cancelled by driving a feedback coil with a current. The zero-field condition is detected by a Hall sensor and the unknown magnetic field is then proportional to the current in the coil. In an open-loop system, the outputs of a Hall sensor and a coil are simply combined. However, all the hybrid magnetic sensors reported in literature were implemented with discrete components and so did not address the challenges of CMOS integration. The following section gives a brief overview of prior work on hybrid magnetic sensors.

Closed-Loop Hybrid Magnetic Sensors

Due to the fact that magnetic fields can be directly generated by current flow, magnetic sensors can be realized in closed-loop architectures with the help of feedback coils [22]. Figure 1.4 shows an example of a closed-loop magnetic sensor using Hall sensors and coils. The magnetic field B is read out by a Hall sensor. The output of the Hall sensor is then amplified and integrated to drive the feedback coil with a current I_{coil}. The feedback coil then generates a feedback magnetic field which counter balances the input magnetic field B. Any residual magnetic field will be read out by the Hall sensor to adjust the feedback current I_{coil}. At steady state, B will be fully cancelled by I_{coil}, which is read out by $V_{out} = I_{coil} * R$.

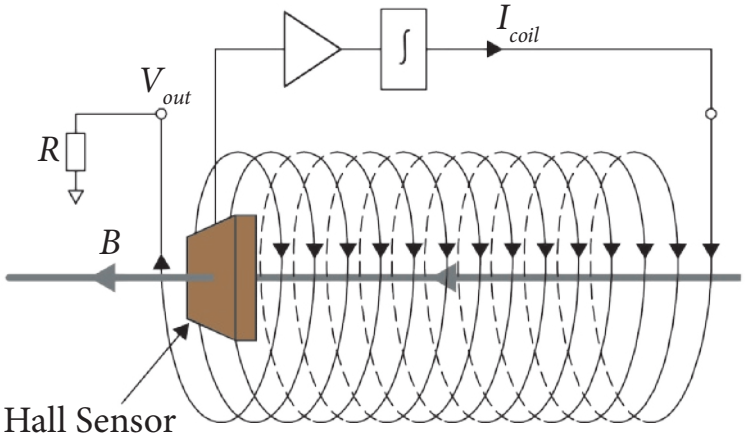

Figure 1.4 Closed-loop magnetic sensor with a Hall sensor and a feedback coil.

The closed-loop architecture can also be used to achieve wide bandwidths since the coil continues to generate an output voltage after the Hall sensor runs out of bandwidth [25, 26]. However, due to the presence of multiple time constants in the system, transfer function matching of the two sensors in the frequency domain can be rather challenging. In addition, only planar coils can be realized in a standard CMOS process, which limits the field strengths that can be generated. Without the use of ferromagnetic material, current-to-magnetic field ratios are usually below 500 mT/A [27, 28]. Moreover, electromigration constraints mean that on-chip coils can only handle currents of a few mA, corresponding to magnetic fields of only a few mT [29]. For these reasons, closed-loop hybrid magnetic sensors are rarely integrated in CMOS.

Open-Loop Hybrid Magnetic Sensors

Hall sensors and pick-up coils can be combined in an open-loop manner such that the Hall sensors measure only the static magnetic field, while the pick-up coils are only used to capture the magnetic field transients. This concept has been demonstrated on PCB with discrete components, and is sometimes referred as the "HOKA" principle [30]. Recent researches extended this concept to combine pick-up coils and other kinds of magnetic sensors, such as AMR (anisotropic magnetoresistive) sensors [31], GMR (giant magnetoresistive) sensors [32] and TMR (tunnel magnetoresistive) sensors [33], which have better sensitivities compared to Hall sensors. To further improve system sensitivity, some work also incorporated ferromagnetic cores into the system, as shown in Figure 1.5. A Hall sensor is placed in the gap of a ferromagnetic core to measure low frequency field. And a pick-up coil, wrapped around the same ferromagnetic core, measures high frequency magnetic field, which is added to the output of the Hall sensor. This has achieved a superior bandwidth of DC – 30 MHz [34].

However promising, robust ways of combining the very different output signals of integrated Hall sensors and pick-up coils must be designed. By taking advantage of digital signal processing (DSP), the outputs of both sensors can be processed and combined in the digital domain. This

approach inevitably requires ADCs to convert the sensor outputs into digital words so that they can be read by a succeeding DSP. However, the differentiating characteristics of pick-up coils pose high requirements on the ADC bandwidth and SNR. Although state-of-the-art ADCs [35-37] are capable of meeting these requirements, they are mostly implemented in advanced technologies such as 40 nm CMOS. Moreover, they usually consume considerable amount power and operate with high speed clocks. These can result in undesired inductive interference between the coil and the ADC, leading to extra work in addition to the ADC design itself. Alternatively, the outputs of both sensors can be combined in the analog domain, which will greatly relax the ADC SNR requirement. An analog crossover network and readout topology in a CMOS process were, however, unknown before this research commenced. In addition, the sensitivity drift of Hall sensors over temperature needs to be minimized to match that of the pick-up coils.

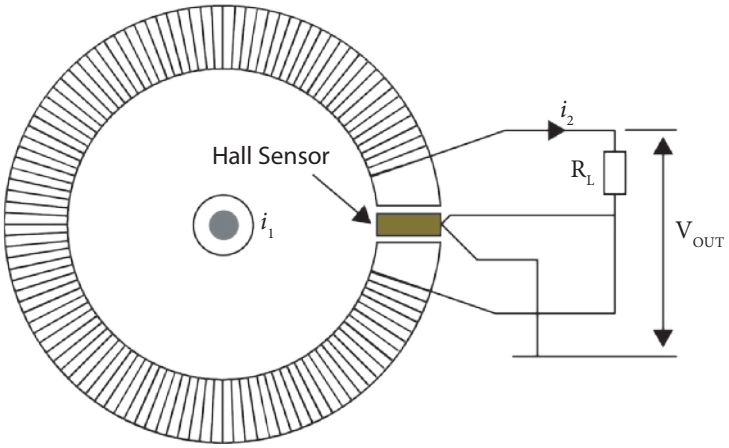

Figure 1.5 Magnetic sensor system combining a Hall sensor and a coil [34].

1.3 Dissertation Organization

The fundamentals of CMOS Hall sensors are first introduced in Chapter 2, including the working principle, fabrication process, and the spinning current technique. This is then followed by a comprehensive review of the prior art in the past decade. The readout techniques of pick-up coils are also reviewed in Chapter 2.

Chapter 3 presents a continuous-time ripple reduction technique for spinning current Hall sensors. It involves the use of three orthogonal ripple reduction loops (triple RRLs) to suppress spinning ripple, thus obviating the need for low-pass filters. Implemented with off-chip components, the triple RRL scheme successfully suppresses the output ripple of a test chip to its noise level, and extends the bandwidth to above 100 kHz, at the expense of two notches in the frequency response. The implementation details and measurement results are discussed in Chapter 3.

To eliminate frequency-response notches, a multi-path CMOS Hall sensor in a 0.18 μm CMOS process is introduced in Chapter 4. The test chip achieves a 400 kHz bandwidth and a 40 μT offset, which at the time of publication was the fastest CMOS magnetic sensor ever reported with less than 50 μT offset. In addition, the triple RRL scheme was also integrated on-chip.

Chapter 5 investigates the possibility of combining Hall sensors and pick-up coils in a multi-path structure. After the discussion of the combination theory, a test chip fabricated in a 0.18 μm standard CMOS process is presented which achieves a 3 MHz bandwidth with an offset of 40 μT and a resolution of 210 μT. This was the fastest CMOS magnetic sensor ever reported by the time of publication [38].

Chapter 6 addresses two unsolved issues from the previous chapters, namely: (1) that the sensitivity of Hall sensors changes over temperature, and is different from that of the pick-up coils, and (2) the complexity and area-inefficiency of triple RRL implementations. The first issue is solved by exploiting the common mode rejection of the differential sensing scheme in current measurements. By introducing a common mode reference field, the Hall sensitivity can be dynamically monitored and thus regulated. Measurement results on a test chip demonstrated that the Hall sensor's sensitivity drift was reduced from 22% to 1% in the temperature range of -45˚C to 105˚C, corresponding to a temperature coefficient of 76 ppm/˚C. The second issue is addressed by revising the triple RRL algorithm such that the hardware required to implement one loop can be multiplexed between the three loops.

Chapter 7 concludes this dissertation and provides an outlook for future work.

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Magnetic Sensors in CMOS Technologies

2

2.1 Introduction

Magnetic sensors are essential parts of current sensing systems that must achieve high galvanic isolation. During the past decades, many efforts have been made to improve their performance. This has led to significant improvements in the performance of CMOS Hall sensors, and pick-up coils.

This chapter reviews the most recent developments in CMOS magnetic sensors, providing the background for later chapters. It is organized as follows. Section 2.2 reviews the basic working principle of Hall sensors, and introduces some readout techniques to improve their performance. The working principle and readout techniques of pick-up coils are then reviewed in Section 2.3, and Section 2.4 concludes this chapter.

2.2 Hall Effect Sensors

The Hall Effect was first discovered by Edwin Hall in 1879 [1]. This section will provide a brief discussion of the Hall Effect for the purposes of circuit design. A more detailed analysis can be found in [2].

In the presence of a out-of-plane magnetic field B, as shown in Figure 2.1, an in-plane charge flow (electrons in this case) is subjected to a certain Lorentz Force in the transverse direction of the charge flow, which is given by:

$$F_L = q \cdot v \cdot B \tag{2.1}$$

where q is the unit charge, v is the charge flow velocity, and B is the vertical magnetic field strength. As a result of the Lorentz Force, the charge flow will bend, and thus more electrons will accumulate on one side of the material, i.e. the electrode V_{out-}. To maintain charge neutrality, positive charges will accumulate on the opposite electrode V_{out+}. Therefore, an electric field is generated within the sample in the transverse direction of the charge follow, which poses an electric force F_E on the charge flow to counterbalance the Lorentz Force. An equilibrium state is

established in the order of 10^{-14} s [3], when the Lorentz Force F_L is fully compensated by the electric force F_E. Therefore, a steady voltage difference can be read out at the transverse electrodes, which is given by:

$$V_{Hall} = G \cdot S_{HS} \cdot I_{bias} \cdot B \tag{2.2}$$

where S_{HS} represents the absolute sensitivity of the Hall Effect in a plate with an infinite length L. G is a geometry factor which depends on the shape and size of the Hall sensor [4]. The Hall sensitivity is sometimes expressed as $S_{HS} \cdot I_{bias}$, which is better suited for a magnetic sensor system.

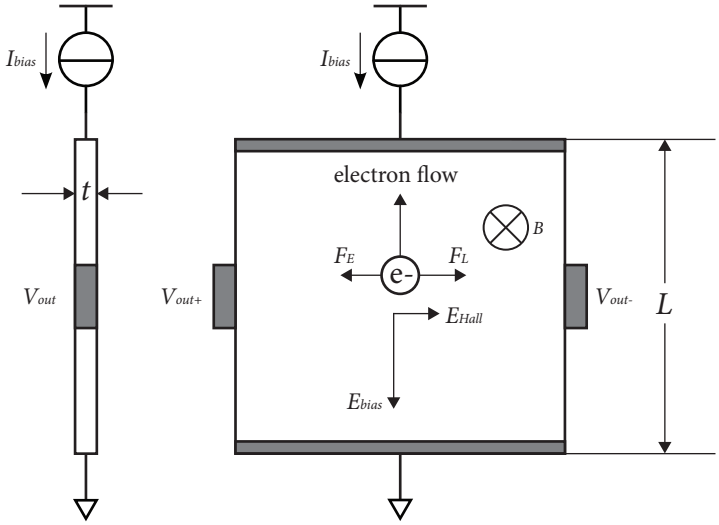

Figure 2.1 Hall Effect.

The absolute Hall sensitivity S_{HS} can be expressed as:

$$S_{HS} = \frac{R_H}{t} \tag{2.3}$$

where R_H is the Hall constant of the material, and t is the thickness of the plate. Instead of being a real constant, R_H is a process-dependent parameter, which can be expressed as:

$$R_H = \frac{r(n\mu_n^2 - p\mu_p^2)}{q(n\mu_n - p\mu_p)^2} \tag{2.4}$$

in which n, p, μ_n and μ_p represent the electron concentration, the hole concentration, the electron mobility, and the hole mobility in the Hall plate, respectively. q is the unit charge, and r is the scattering factor for a given material type. The scattering factor r is related to the relaxation time

constant τ, after which all kinetic energy of the charge carriers is consumed by collisions [2]. It is usually between 1.18 (acoustic phonons) and 1.93 (ionized impurities) for modern CMOS processes [2]. For a single-type doped silicon, e.g. n-doped, Equation (2.4) can be simplified as:

$$R_H = \frac{r}{qn} \tag{2.5}$$

Therefore, Equation (2.2) can be re-written as:

$$V_{Hall} = G \cdot \frac{r}{qnt} \cdot I_{bias} \cdot B \tag{2.6}$$

Although Equation (2.6) is commonly used to express the Hall voltage, it provides information about physical design parameters rather than circuit design parameters. In a given process, Equation (2.5) can be re-written in terms of resistivity ρ as:

$$R_H = \frac{r}{qn} = r \cdot \mu_n \cdot \rho \tag{2.7}$$

By substituting Equation (2.7) in Equation (2.6), the Hall voltage can also be expressed as:

$$V_{Hall} = G \cdot \frac{\rho \cdot \mu_n}{t} \cdot r \cdot I_{bias} \cdot B = G \cdot r \cdot \mu_n \cdot R_S \cdot I_{bias} \cdot B \tag{2.8}$$

where R_S is the sheet resistance of the plate material. In CMOS processes, the mobility of electrons is about 2.5x greater than that of holes. Therefore, CMOS Hall sensors are commonly built with n-well plates instead of p-well plates [2]. In addition to the choice of materials, Equation (2.8) also indicates a limiting factor in system design, namely that the term $R_S \cdot I_{bias}$ is directly related to the power supply rail. This also explains why for a given power supply, the maximum achievable magnetic sensitivity in V/T cannot be significantly improved by using a thinner plate, despite the absolute Hall sensitivity in V/A·T being inversely proportional to the thickness of the plate. However, in order to optimize their offset [5], CMOS Hall sensors are rarely biased at maximum current/voltage. This will be explained later in Section 2.2.2.

Despite the fixed junction depth and doping concentration of the plate in a CMOS process, the Hall sensitivity in V/A·T can still be slightly adjusted and improved by changing the effective thickness of the sensor plate. Figure 2.2 (a) shows the cross-section of a typical Hall sensor built with an n-well plate. A p+ pinch layer, as shown in Figure 2.2 (b), can be created inside the n-well plate to reduce the thickness of the active region, therefore improving the Hall sensitivity. Alternatively, this can be achieved by constructing the Hall sensor in a MOS capacitor structure, as shown in Figure 2.2 (c), where the gate voltage is used to create a depletion region to reduce the thickness of the n-well. Apart from the slightly increased sensitivity, the sensor's flicker noise will

also be reduced since the structures in Figure 2.2 (b) and (c) effectively isolate the sensor from the crystal defects present at the Si/SiO_2 interface [6].

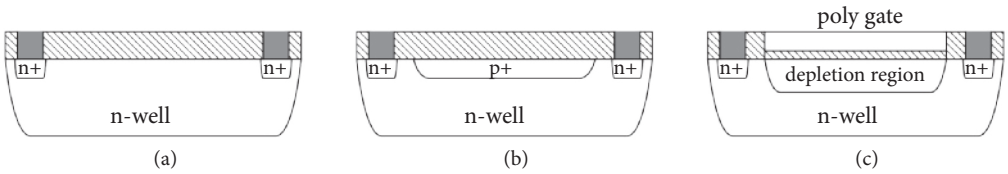

Figure 2.2 Cross-sections of (a) a Hall sensor built with n-well, (b) a Hall sensor built with a pinched n-well by a p+ layer, and (c) a Hall sensor built with the MOS cap structure.

The Hall Effect is considered to be a highly linear effect. However in CMOS technologies, this only holds up to a field strength of about 1 T. In [7], the linearity of an n-type silicon Hall sensor is measured, as shown in Figure 2.3. For most applications, the magnetic field strength of interest is limited to 10^{-2} T, for which the non-linearity of the Hall sensors is quite negligible compared to that of the readout circuits.

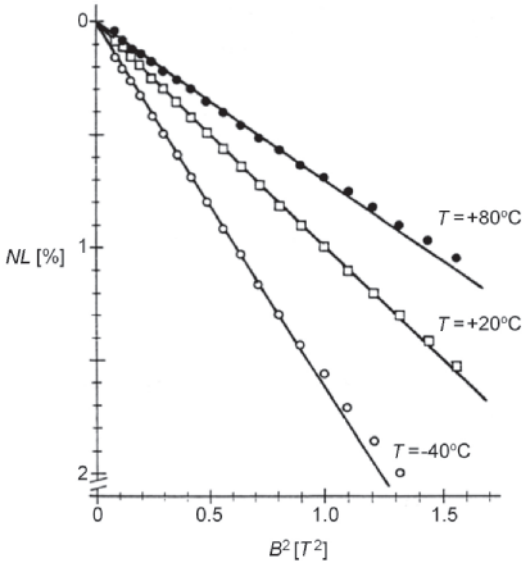

Figure 2.3 Experimental result [7] of the non-linearity (NL) of an n-type silicon Hall sensor versus squared magnetic field strength (B2).

2.2.1 Offsets in Hall Sensors and the Spinning Current Technique

Being four-terminal devices, Hall sensors can be modeled as a Wheatstone bridge, as shown in Figure 2.4. Due to the arm resistance mismatch, an offset V_{offset} appears at the outputs together with the magnetic signal V_{Hall}. This offset is usually in the order of a few milli-Volts, which is too large for precision applications. For instance, a Hall sensor with a nominal source resistance of

1 kΩ could have a mismatch of 1% in one of the arm resistances, e.g. R_3 = 1.01 kΩ. When biased with a current of 1 mA, an offset of 2.5 mV would appear at the outputs. Assuming a sensitivity of 100 V/A·T, this is then equivalent to an offset of 25 mT, which is orders of magnitudes larger than the signal of interest. Offset is mainly caused by three factors: lithographic inaccuracy; cross-sensitivities of resistance to temperature, stress, etc.; and process spread.

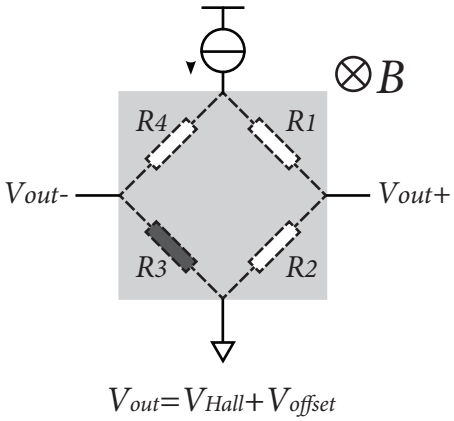

Figure 2.4 Hall sensors modeled as a Wheatstone bridge.

Lithographic Inaccuracy

For a given process, lithographic inaccuracy represents a fundamental limit which itself cannot be improved without moving to a more advanced process node. However, the influence of lithographic accuracy can be minimized by proper sensor design. For instance, instead of using the point contacts shown in Figure 2.4, the wider contacts shown in Figure 2.5 can be used, such that lithography errors become less significant. However, wider contacts form a parasitic conducting path between the biasing and measurement electrodes, and therefore reduce the effective biasing current and hence the sensitivity. This is often referred to as the short-circuit effect, which leads to a slightly reduced Hall sensitivity. The short-circuit effect can then be alleviated by making the sensor larger.

Alternately, the sensor can be designed in a different shape, for instance, in the Greek cross shape shown in Figure 2.6. Thanks to the presence of resistive arms, the voltage gradients around the contacts in Greek-cross-shaped sensors are much lower than that in square-shaped sensors [4]. This makes Greek-cross-shaped Hall sensors less sensitive to lithographic inaccuracies, and therefore can achieve better offset without using large sensors. However, the source resistance of the cross-shaped Hall sensors is inevitably higher. Therefore the maximum biasing current, and hence the highest achievable sensitivity, is then reduced for a given power supply rail. Nevertheless, for various reasons, the biasing voltage of CMOS Hall sensors are usually lower than the power supply, and therefore Greek cross-shaped Hall sensors are often used to minimize offset errors due to lithographic inaccuracies.

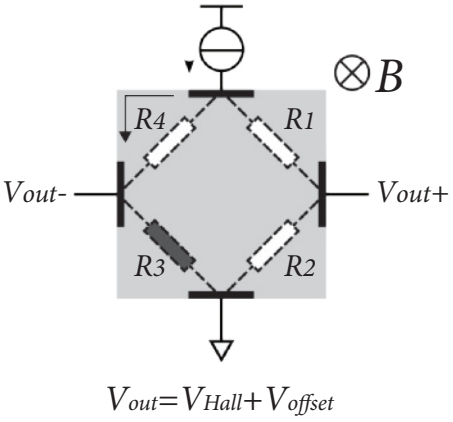

Figure 2.5 Hall sensor with wide contacts to minimize lithography errors.

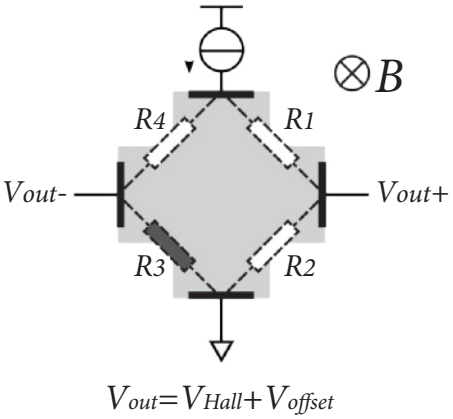

Figure 2.6 Greek cross-shaped Hall sensor with wide contacts.

Cross-Sensitivity

In contrast to lithography-related errors, cross-sensitivity related errors cannot be alleviated by using larger devices. As a matter of fact, smaller devices are usually preferred to minimize the cross-sensitivities of temperature and stress. For instance, with a temperature gradient across the Hall sensor, the temperature difference seen by the diagonal arm resistors in smaller devices will be lower than that of the large devices. In addition to static offset issues, the cross-sensitivity of temperature and stress usually introduces dynamic offset changes, which is a more critical issue in sensor systems. Such errors cannot be effectively removed by simply reducing the sensor dimensions.

In [8], a Hall sensor structure consisting of two orthogonally connected Hall plates, as shown in Figure 2.7, can be used to cancel the 1st order cross-sensitivities. For instance, due to the cross-

sensitivity to temperature and stress, the arm resistance R_3 changes from its original value. However, as the biasing and readout electrodes of the two plates are rotated by 90˚, the ratio between the two parallel arm resistances ($R_3||R_4$ and $R_3||R_2$) remains relatively constant, thus minimizing the offset change due to external stress [9].

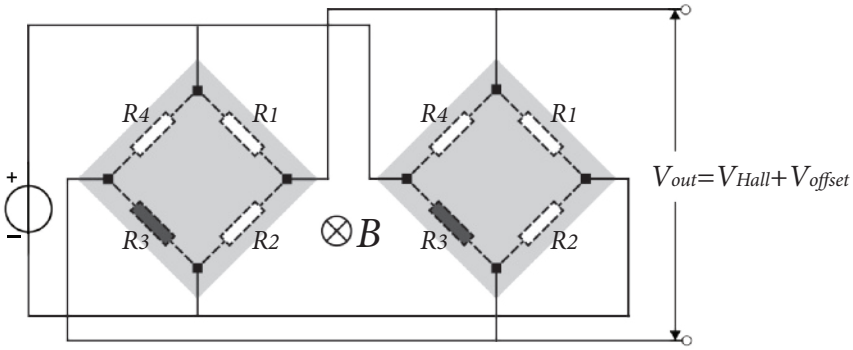

Figure 2.7 Two orthogonally connected Hall plates to stabilize offset change due to cross-sensitivities of temperature and stress (replotted from [8]).

Process Spread

Process spread is usually the dominant source of error in small-sized Hall sensors. The matching properties of a normal resistor can be expressed as:

$$\frac{\sigma_{\Delta R}}{R_0} = \frac{A_R}{\sqrt{area}} \tag{2.9}$$

in which R_0 is the nominal resistance of the resistor, $\sigma_{\Delta R}$ is the relative matching of the designated resistor, and A_R is a process parameter expressed in units of [%·μm]. Even though Equation (2.9) clearly suggests that a large device can potentially reduce the mismatch and thus offset, this improvement is rather limited. For instance, to reduce the offset by 10 times, under the assumption that the offset is linearly related to the relative mismatch, a Hall sensor with 100 times larger area is required.

The sensor structure proposed in Figure 2.7 can also help to reduce the process-spread related offset without using large-size devices. However, the offset reduction factor is limited to about 10 times [8], which means that the resulting offset of a few milli-Tesla is still considerably larger than the signal of interest.

Spinning Current Technique

To suppress Hall sensor offset efficiently, a dynamic offset cancellation technique, known as the spinning current technique, was introduced in 1989 [10]. This technique exploits the reciprocity

of symmetrical Hall plates. By swapping the functions of Hall sensor readout and bias electrodes and thus changing the direction of the bias current through the sensor, the relative polarities of the sensor offset and V_{Hall} can be periodically swapped. Figure 2.8 depicts the operation of a two-phase spinning current Hall sensor [11]. With both the biasing electrodes and readout electrodes rotated by 90˚, the polarity of the offset is flipped, while that of V_{Hall} is not. V_{Hall} can be then extracted by averaging the outputs of the two spinning phases.

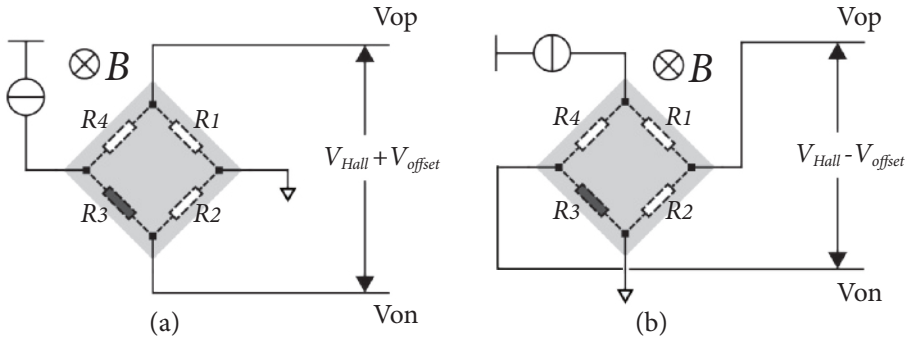

Figure 2.8 Operation of a two-phase spinning current Hall sensor (replotted from [11]).

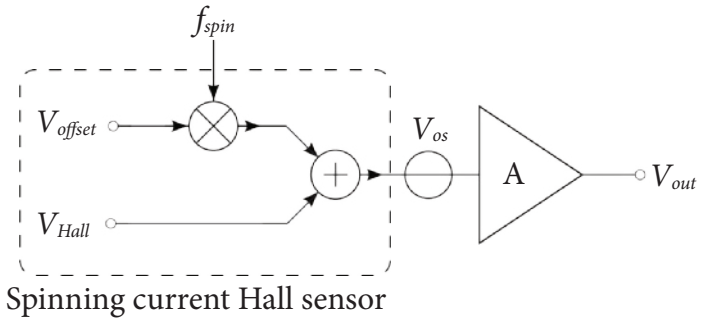

Figure 2.9 Circuit model of a two-phase spinning current Hall sensor with analog front-end.

Periodically switching between two different spinning phases will effectively modulate the offset to the switching frequency, namely the spinning frequency f_{spin}. Therefore the operation of a two-phase spinning current Hall sensor can be modeled as shown in Figure 2.9. A typical Hall sensor will only produce a μV-level V_{Hall}, which therefore requires amplification. However, a typical amplifier A will introduce an extra offset V_{os} which is usually in the order of a few milli-Volts. This is typically reduced by trimming or the use of circuit techniques such as chopping or auto-zeroing [12].

Alternately, the spinning current technique can be re-arranged so that the magnetic signal V_{Hall}, rather than the offset V_{offset}, is modulated to f_{spin} [11], as shown in Figure 2.10. V_{Hall} can then be re-constructed with a demodulator succeeding the amplifier (Figure 2.11), which also modulates

both V_{offset} and V_{os} to the spinning frequency. Although the modified spinning topology greatly relaxes the offset requirement of the amplifier, it does require an amplifier with a sufficiently high bandwidth such that the up-modulated V_{Hall} is not suppressed.

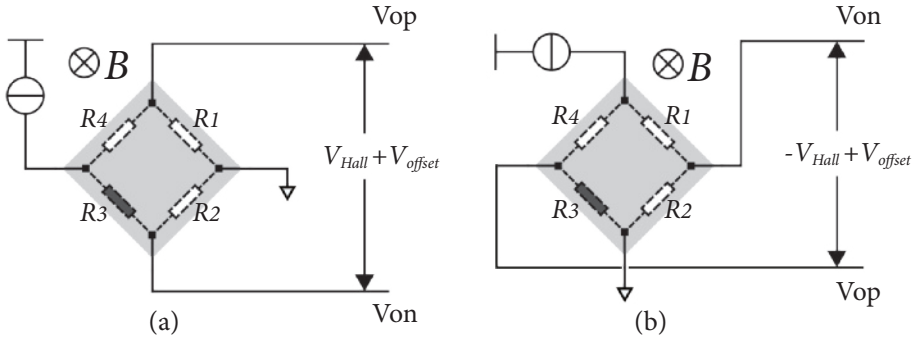

Figure 2.10 Operation of an alternative two-phase spinning current Hall sensor.

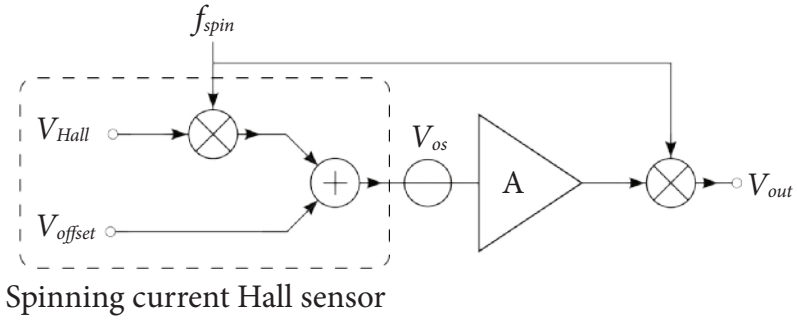

Figure 2.11 Circuit model of a two-phase spinning current Hall sensor with analog front-end.

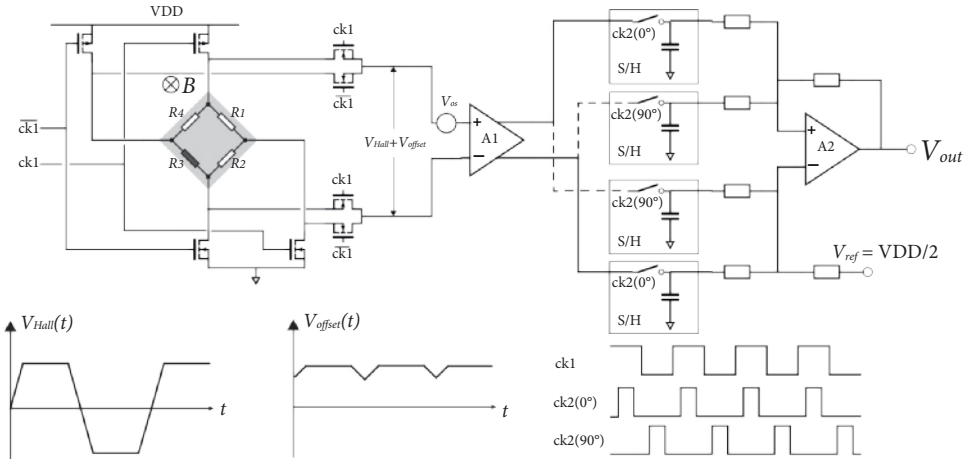

Figure 2.12 Implementation example of a two-phase spinning current sensor (replotted from [11]).

Figure 2.12 shows one of the first on-chip implementations of a two-phase spinning current Hall sensor in a 2 μm BiCMOS process [11]. The spinning current technique is implemented with PMOS and NMOS switches. After the amplification by A1, the Hall sensor outputs are sampled by four sample and hold (S/H) blocks, and then subtracted from each other to retrieve V_{Hall}. This implementation reports a residual offset of 0.5 mT, which is still quite large for precision applications like current sensing. This is limited by several design choices, i.e. the choice of biasing and readout, the number of spinning phases, and the biasing strength. These limiting factors will be discussed in the next section.

2.2.2 Constraints and Improvements in the Spinning Current Technique

With a properly designed analog front-end (AFE), a spinning-current Hall sensor can achieve an offset of less than 50 μT [13, 14]. This section provides a detailed analysis on the choice of biasing and readout, the number of spinning phases, and the biasing strength of spinning Hall sensors, and their influence on residual offsets.

Biasing and Readout

Both voltage and current sources can be used to bias a Hall sensor. It does not make a fundamental difference in a static non-spun Hall sensor, as the voltages and current can be mutually translated via the source resistance of the Hall sensor. Similarly, non-spun Hall sensors can be read out in voltage or current mode, which is independent of the biasing choice.

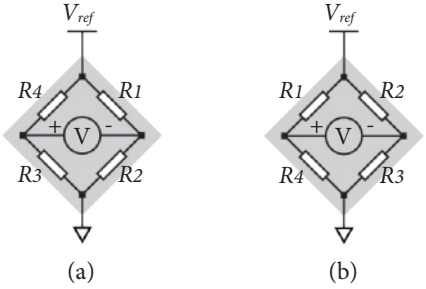

Figure 2.13 Voltage biased spinning current Hall sensor with voltage outputs: (a) the 1st phase and (b) the 2nd phase.

However, these statements about the biasing and readout of non-spun Hall sensors does not apply to spinning Hall sensors. Figure 2.13 shows an arbitrary Hall sensor for analysis; the Hall sensor is voltage-biased and read out by a voltage meter. The output offsets can then be expressed in terms of the biasing voltage V_{ref} and all the arm resistances $R_1 - R_4$:

$$V_{offset1} = V_{ref} \frac{R_1 R_3 - R_2 R_4}{(R_3 + R_4)(R_1 + R_2)} \tag{2.10}$$

$$V_{offset2} = V_{ref} \frac{R_2 R_4 - R_1 R_3}{(R_1 + R_4)(R_2 + R_3)} \tag{2.11}$$

Equations (2.10) and (2.11) suggest that offsets $V_{offset1}$ and $V_{offset2}$ do not cancel each other out unless (R_1+R_4)(R_2+R_3) and (R_1+R_2)(R_3+R_4) are equal. The two denominators are indeed equal in the case that only one arm resistance, e.g. R_3, differs from the other three. Therefore the voltage-biasing and voltage-readout setup works with the simplified analysis shown in Figure 2.12. However, in reality, mismatches exist among all the arm resistances, which inevitably introduces a residual offset error.

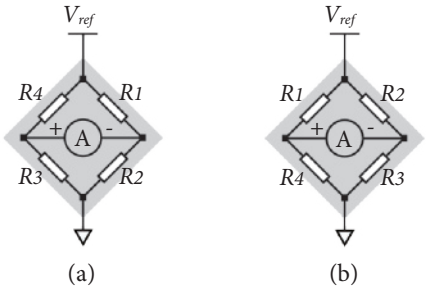

Figure 2.14 Voltage biased spinning current Hall sensor with current outputs: (a) the 1st phase, and (b) the 2nd phase.

On the other hand, if the voltage-biased Hall sensors are read out by a current meter (Figure 2.14), then the offset current in the different spinning phases can be written as:

$$I_{offset1} = V_{ref} \frac{(R_1 R_3 - R_2 R_4)(R_1 + R_2 + R_3 + R_4)}{(R_3 + R_4)(R_1 + R_2)(R_1 + R_4)(R_2 + R_3)} \tag{2.12}$$

$$I_{offset2} = V_{ref} \frac{(R_2 R_4 - R_1 R_3)(R_1 + R_2 + R_3 + R_4)}{(R_1 + R_4)(R_2 + R_3)(R_1 + R_2)(R_3 + R_4)} \tag{2.13}$$

Equations (2.12) and (2.13) suggest that the offsets in current readout mode are completely cancelled out, and so current readout should be used in voltage-biased spinning Hall sensors to achieve minimum offset.

Alternately, Hall sensors can be biased with current sources, and read out in either the voltage or current mode (Figure 2.15). Equations (2.14 – 2.17) express the current offsets and the voltage offsets in their corresponding readout modes.

$$V_{offset1} = I_0 \frac{R_1 R_3 - R_2 R_4}{R_1 + R_2 + R_3 + R_4} \tag{2.14}$$

$$V_{offset2} = I_0 \frac{R_2R_4 - R_1R_3}{R_1 + R_2 + R_3 + R_4} \tag{2.15}$$

$$I_{offset1} = I_0 \frac{R_1R_3 - R_2R_4}{(R_1 + R_4)(R_2 + R_3)} \tag{2.16}$$

$$I_{offset2} = I_0 \frac{R_2R_4 - R_1R_3}{(R_3 + R_4)(R_1 + R_2)} \tag{2.17}$$

Like voltage-biased, voltage-readout spinning Hall sensors, the offset of current-biased, current-readout spinning Hall sensors will not be fully cancelled due to arm resistance mismatches. In conclusion, to optimize their offsets, spinning Hall sensors should either employ voltage biasing and current readout, or current biasing and voltage readout.

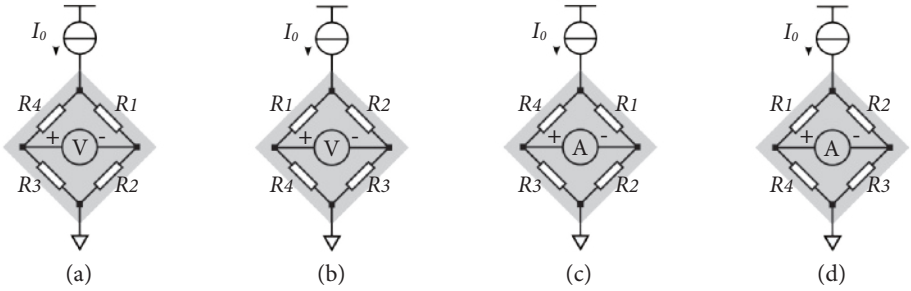

Figure 2.15 Current biased spinning current Hall sensor: (a) the 1st phase and (b) the 2nd phase offset in the voltage readout mode; (c) the 1st phase and (d) the 2nd phase offset in the current readout mode.

Biasing Strength: Sensitivity vs. Offset

To maximize their output signal-to-noise ratio (SNR), CMOS Hall sensors are preferably biased at high current/voltage levels, i.e. close to the power supply rail as in [11]. To a first approximation, this does not change the magnetic referred offset of a spinning Hall sensor since both offsets and sensitivities are linearly proportional to the biasing current/voltage. However, this statement regarding biasing strength overlooks the fact that n-well resistors exhibit a certain voltage coefficient due to the presence of a depletion region between the n-well and the p-substrate, as shown in Figure 2.16. An increase in the biasing strength will increase the reverse biasing of the p-n junction, and therefore increase the resistance of the n-well. This is usually referred to as the JFET effect or the back-biasing effect.

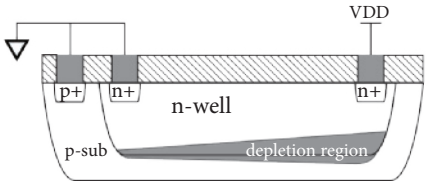

Figure 2.16 JFET effect due to the depletion region between the n-well and the p-substrate.

The JFET effect significantly limits the effectiveness of the spinning current technique, as the arm resistances will now be dependent on their position relative to the biasing electrode. This can be better understood by analyzing an example of a two-phase spinning current Hall sensor, as shown in Figure 2.17.

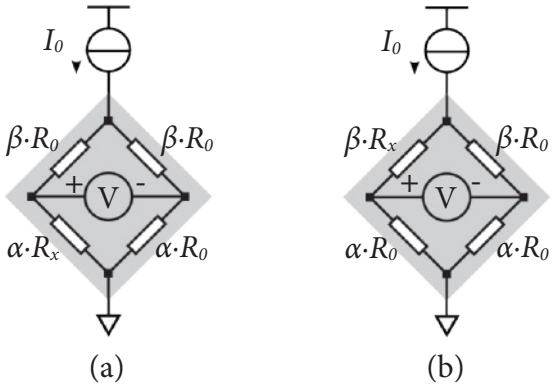

Figure 2.17 Arm resistance change due to different biasing conditions: (a) the 1st spinning phase and (b) the 2nd spinning phase.

Due to the JFET effect, each arm resistor experiences an amplification factor of α or β ($\beta > \alpha > 1$) depending on the biasing position. To simplify the analysis, we assume that only one resistor has a larger resistance of R_x compared to the others. In the 1st spinning phase, as shown in Figure 2.17 (a), R_x is only amplified by α ($< \beta$). Therefore the resistance mismatch between R_x (lower left) and R_0 (top left) is alleviated. However, in the 2nd phase, R_x is amplified by β ($>\alpha$), which agitates the resistance mismatch between R_x and R_0. As a result, the offsets in these two phases $V_{offset1}$ and $V_{offset2}$ cannot fully compensate each other, but lead to a residual offset error. The offsets in the two spinning phases can be expressed by using Equations (2.14) and (2.15):

$$V_{offset1} = I_0 \frac{\beta R_0 \cdot \alpha R_x - \beta R_0 \cdot \alpha R_0}{2(\alpha+\beta)R_0 + \alpha(R_x - R_0)} \tag{2.18}$$

$$V_{offset2} = I_0 \frac{\beta R_0 \cdot \alpha R_0 - \beta R_x \cdot \alpha R_0}{2(\alpha+\beta)R_0 + \beta(R_x - R_0)} \tag{2.19}$$

The exact influence of the JFET effect can then be identified in the denominators of Equations (2.18) and (2.19), showing that the resistance mismatch (R_x – R_0) has different coefficients in different spinning phases. Moreover, since the amplification factor is bias-dependent, the residual offset of a spinning Hall sensor will be dependent on the biasing strength. This effect has been explicitly studied [5], and is shown in Figure 2.18. In modern CMOS processes, the optimum biasing points of Hall sensors highly depend on the target application, as well as on the process parameters, device dimensions, and sensor structures.

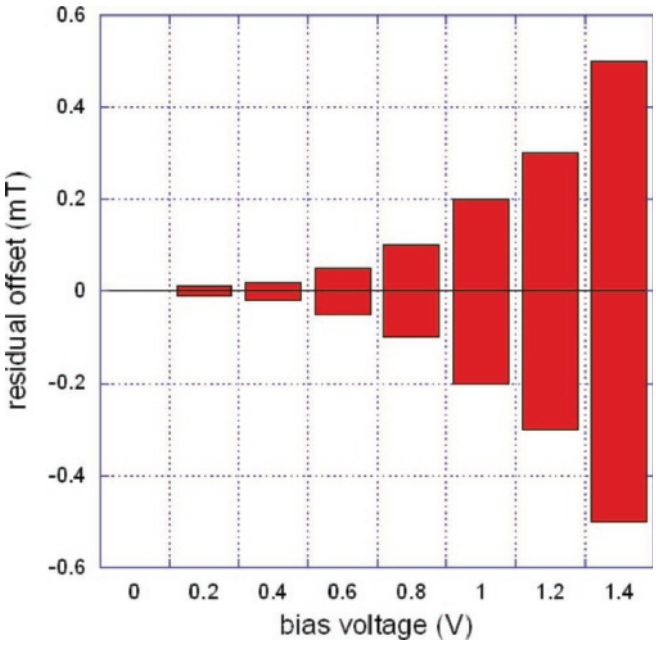

Figure 2.18 Relation between the biasing voltage and residual offset of a traditional spinning Hall sensor (reprinted from [5]).

Multi-Phase Spinning Current Hall Sensors

The readout and biasing topologies discussed in the previous sections are based on the assumption that the arm resistances remain constant over the spinning phases. However, due to the JFET effect, two-phase spinning is rather ineffective as the original resistance mismatches change in the different spinning phases. In addition, this effect is exacerbated by the fact that silicon has a tri-directional lattice structure, so that n-well resistors exhibit anisotropic behavior [15], i.e. that their intrinsic resistances change as a function of the biasing direction. These effects lead to incomplete compensation of Hall sensor offsets, which are considered to be the major error sources in two-phase spinning Hall sensors [16, 17].

The residual offset due to the anisotropic resistances and the JFET effect can be alleviated by using a four-phase spinning technique to exploit all four possible operations of a four-contact

Hall sensor. The improvement achieved by using a four-phase spinning Hall sensor has been specifically studied in [13], and the results are shown in Figure 2.19. Mathematical analysis suggests that the offset of a 4-phase spinning current Hall sensor can be as low as 10 μT [13], which is 10 times smaller than that of a 2-phase spinning current Hall sensor.

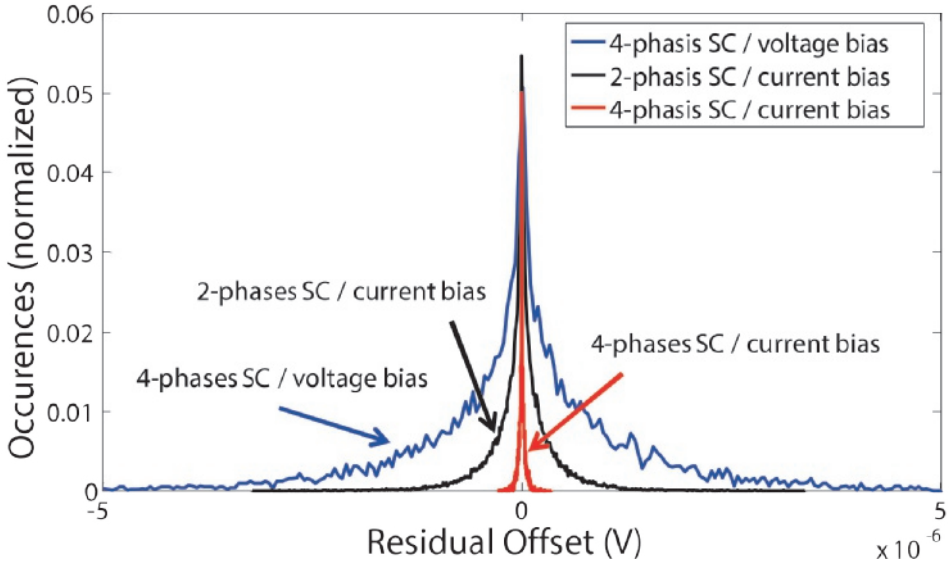

Figure 2.19 Residual offsets of a two-phase spinning Hall sensor and a four-phase spinning Hall sensor (reprinted from [13]).

Nevertheless, in [18] an offset of 50 μT has been achieved by configuring two four-contact Hall plates in current-mode, as shown in Figure 2.20. The presence of a vertical magnetic field forces the current flow to be unevenly split between the two Hall plates, which results in an improved sensitivity. In addition, the use of two sensors helps to reduce intrinsic offset and thus alleviate the JFET effect. Therefore, the sensor could achieve a low offset (50 μT) with only two spinning phases and a proper analog front-end, as shown in Figure 2.21. The current signals from the Hall plates are integrated into a chopped active integrator. During the integration phase, the intrinsic offset errors of the sensor are cancelled out by the two-phase spinning operation. A switched-capacitor (SC) filter is then used for further processing after the integration phase.

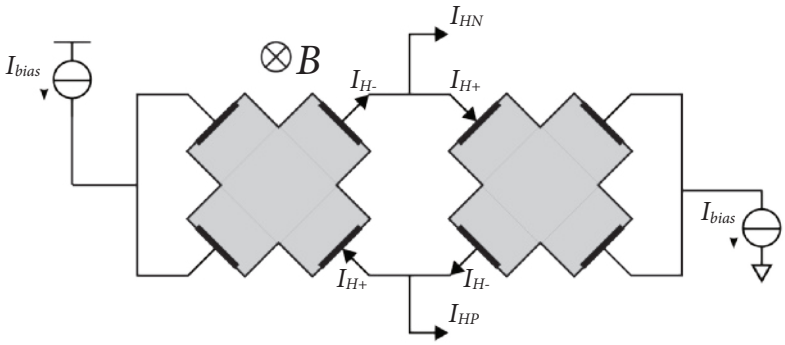

Figure 2.20 Two Hall plates used in current-mode (replotted from [18]).

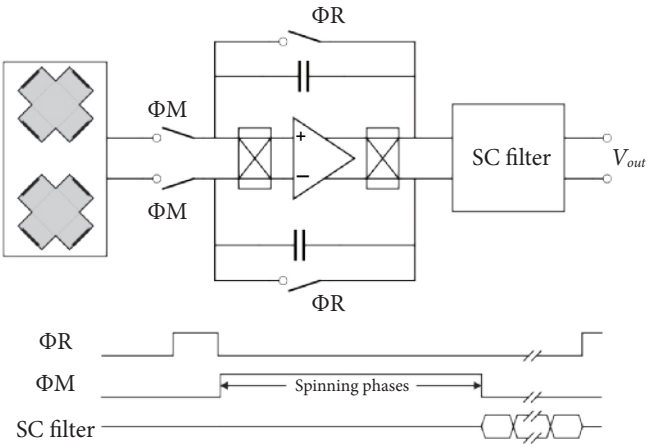

Figure 2.21 Analog front-end of the current-mode Hall sensor (replotted from [18]).

A state-of-the-art four-phase spinning Hall sensor [14] can achieve an offset of as low as 10 μT, as shown in Figure 2.22. The analog front-end consists of a 2nd order continuous-time sigma-delta modulator with an offset pre-compensation scheme. To minimize the offset errors due to the readout circuitry, both integrators inside the sigma-delta modulator are chopped. In addition, the first integrator has a resistively-degenerated input stage which maximizes the input linear range of the g_m-C integrator. The offset pre-compensation scheme estimates the raw offset of the Hall sensor, and cancels it by injecting a compensation signal in the 1st integrator of the sigma-delta modulator. This approach dramatically reduces the signal swing at the output of the 1st integrator, and thus relaxes the dynamic range of the g_m-C integrators. The further development of this technique will be discussed in Chapter 3.

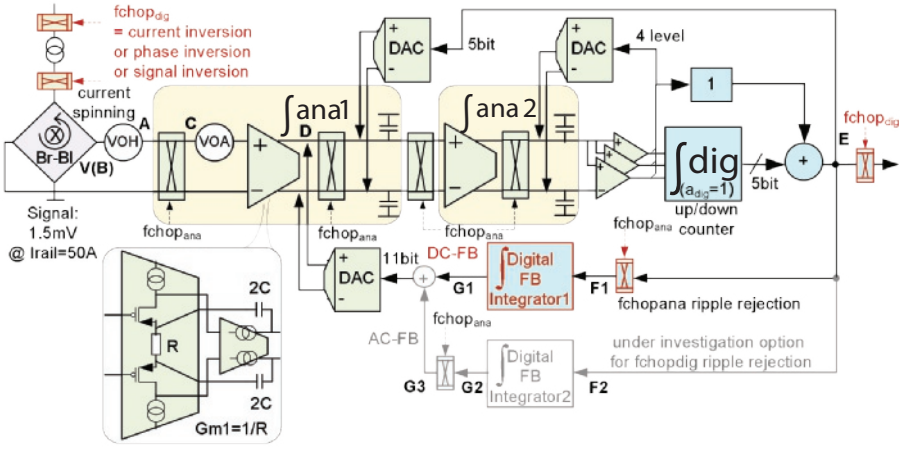

Figure 2.22 System block diagram of a four-phase spinning Hall sensor with 10 µT offset (reprinted from [14]).

A further improvement in offset can be achieved by using even more spinning phases and an improved spinning implementation [19]. Instead of switching a DC biasing current rapidly from one direction to another direction, [19] proposes a continuous spinning topology by combining two harmonic biasing currents with a 90˚ phase shift:

$$I_{AC} = I_0 \cdot \sin\varphi \tag{2.20}$$

$$I_{BD} = I_0 \cdot \cos\varphi \tag{2.21}$$

The combination of I_{AC} and I_{BD} can generate an effective biasing current with an arbitrary angle, as shown in Figure 2.23. However, since φ is not at 0˚, 90˚, 180˚ or 270˚, the output signals are not directly available, but require additional signal processing in both the AC and BD directions.

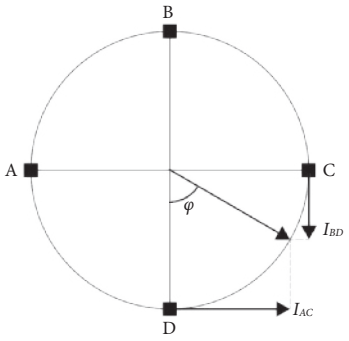

Figure 2.23 Diagram of the two harmonic biasing currents I_{AC} and I_{BD} and the effective biasing current direction (replotted from [19]).

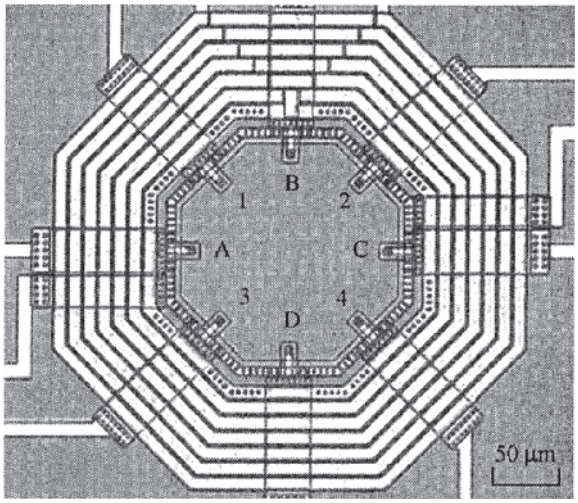

Figure 2.24 Layout of an octagonal shaped Hall plate (reprinted from [19]).

The proposed continuous spinning topology has been implemented on an octagonal shaped Hall plate, as shown in Figure 2.24. With off-chip equipment, [19] experimentally shows the difference between conventional rapid spinning and the proposed continuous spinning; with eight spinning phases, the continuous spinning topology can further reduce the offset by another factor of 2, to below 10 µT. In addition, experiments with a different number of spinning phases have been conducted, the measurement results of which are shown in Figure 2.25. With eight spinning phases, the offset improves dramatically in packages with high pressure. This is due to the anisotropic characteristic of the n-well as described in [15].

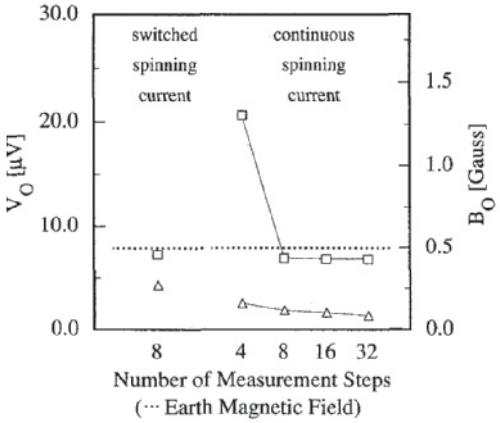

Figure 2.25 Measurement results of switched spinning current and continuous spinning current with a different number of spinning phases. □ are measured with high package stress, and Δ are measured with low package stress (reprinted from [19]).

The idea of an eight-phase spinning Hall sensor is implemented in [20] with complete signal conditioning circuits, as shown in Figure 2.26. To preserve the low offset of the sensor (200 nV), the analog front-end employs nested-chopping and dead banding [21] to further minimize the residual offset of a traditional chopper amplifier. In order to accurately process the spinning ripple, the V-to-I converter requires a linear dynamic range of 120 dB, which is achieved with the help of two opamps and a resistor, as shown in Figure 2.27 [20]. Furthermore, this design uses four Hall sensors in parallel to reduce dynamic stress effects and make the residual offset stable. The measurement results confirm the effectiveness of the eight-phase spinning technique with a stable offset of only 3.65 μT (3σ).

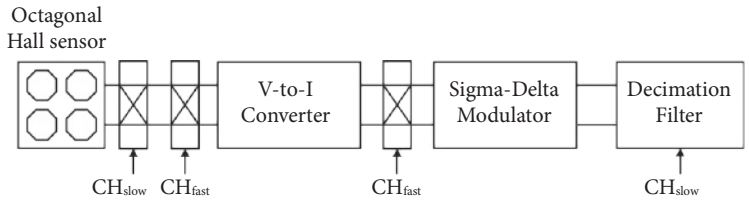

Figure 2.26 Block diagram of an eight-phase spinning Hall sensor system (replotted from [20]).

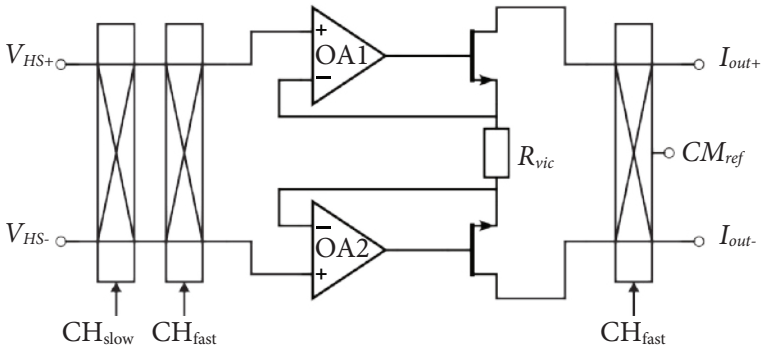

Figure 2.27 Implementation of the V-to-I converter with a 120 dB linear dynamic range (replotted from [20]).

2.2.3 Bandwidth and Ripple Reduction

Intrinsically, the bandwidth of a CMOS Hall sensor is limited by its source resistance and parasitic capacitance. With a source resistance of 10 kΩ and a parasitic capacitance of 0.1 pF, a Hall sensor can achieve a signal bandwidth as high as 159 MHz. However, the total integrated noise over the entire bandwidth is 200 μV_{rms}. Assuming the Hall sensors has a sensitivity of 50 mV/T, the system will have a resolution of no better than 4 mT_{rms}, which is unacceptable in most applications. Therefore, for a given resolution specification, the bandwidth of a Hall sensor needs to be reduced to suppress its noise power.

Apart from noise concerns, the bandwidth of CMOS Hall sensors is usually further limited to suppress the spinning ripple due to the various sources of offset, as shown in Figure 2.28. Due to their relatively large amplitude and the fact that typical spinning frequencies are in the kHz range, this requires continuous-time analog filters with kHz cut-off frequencies that then occupy a large chip area. For instance, the four-phase spinning current technique is used on a Hall sensor with an initial offset of 10 mT. With f_{spin} = 50 kHz, the bandwidth must be limited to 1 kHz by a 1st order low-pass filter (LPF) to ensure that the spinning ripple is lower than 100 μT.

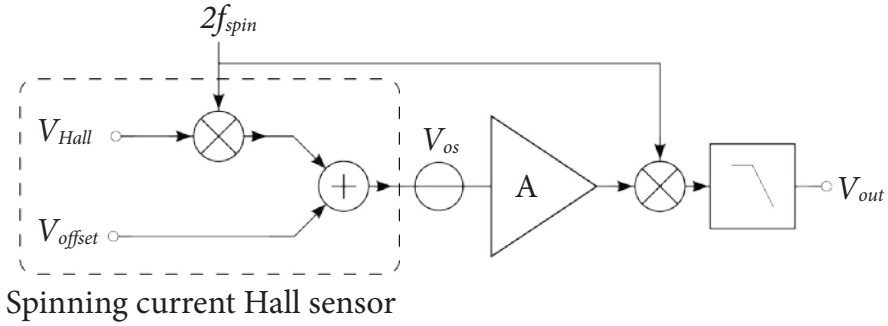

Figure 2.28 Use of a low-pass filter (LPF) to suppress spinning ripple.

A more area-efficient approach is to use discrete-time LPFs, which avoids the implementation of large time constants. For instance, a four-phase switched-capacitor integrator can be used to average out the spinning ripple. As an alternative, the outputs of a spinning Hall sensor can be directly digitized by an ADC and filtered by a digital filter. This is especially convenient in sigma-delta ADCs, as the digital filter can be implemented as part of the decimation filter, as in [20]. With discrete filters, the bandwidth of spinning Hall sensors can be theoretically extended to the Nyquist bandwidth $f_{spin}/2$. However, due to the sampling actions involved in discrete-time filters, this approach will suffer from noise aliasing, resulting in a higher noise density at the output. Moreover, as there is no anti-aliasing filters available in the magnetic field domain, the discrete filters will also be vulnerable to signal aliasing, which makes the system sensitive to nearby high frequency disturbances.

Increasing the spinning frequency can potentially alleviate the bandwidth limits of both the continuous-time and discrete-time approaches. However, as has been experimentally shown in [22], a high spinning frequency will result in a dramatically increased offset. This is because the spinning current technique is a continuous-time modulation process, and therefore any switching transients will count as extra offsets. A similar result is measured in one of the test chips [23] of this thesis, which will be discussed extensively in Chapter 3.

For all the above-mentioned reasons, the bandwidth of precision CMOS Hall sensors (100 μT offset) is usually limited to below 50 kHz. A benchmark plot of offset vs. bandwidth for CMOS

Hall sensors is shown in Figure 2.29. More details of this plot can be found in the Appendix at the end of this thesis.

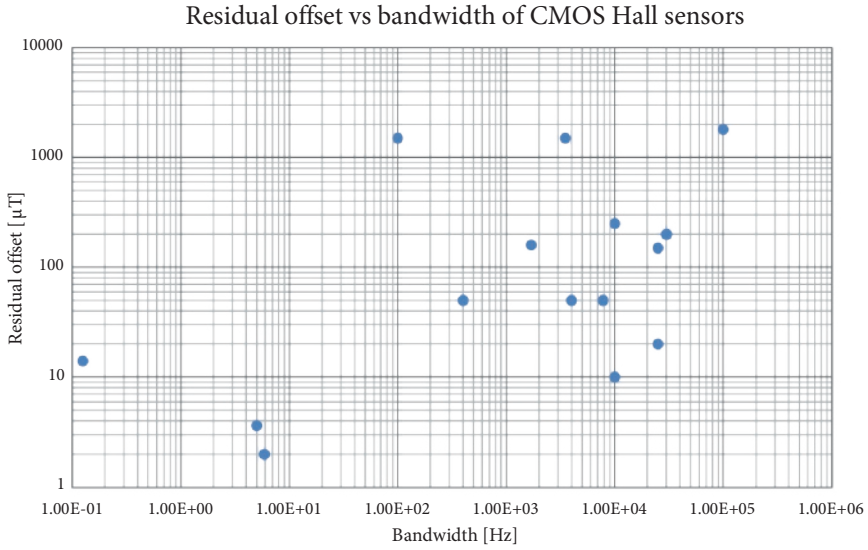

Figure 2.29 CMOS Hall sensor survey of residual offset vs. bandwidth. Papers have been selected from IEEE SSCS and Sensors publications from 2001 to 2015 (see Appendix for more details).

2.3 Pick-up Coils

Pick-up coils, can also be used as magnetic sensors. Unlike Hall sensors, pick-up coils are only sensitive to changes in magnetic field. An electromotive force (EMF) is generated between the two terminals of a pick-up coil in the presence of a varying magnetic field:

$$\varepsilon = nA\frac{dB}{dt} \tag{2.22}$$

where A is the flux area and n is the number of windings. This differentiating characteristic makes pick-up coils very suitable for capturing high frequency magnetic field transients. The output of a pick-up coil placed in a sinusoid magnetic field is expressed as:

$$B = B_0 \sin(2\pi f \cdot t) \tag{2.23}$$

with the pick-up coil unloaded, a voltage output is produced between the two terminals:

$$V_{coil} = 2\pi f \cdot nA \cdot B_0 \cos(2\pi f \cdot t) \tag{2.24}$$

Equation (2.24) explicitly states that a pick-up coil produces an output, the amplitude of which is proportional to the frequency of the magnetic field. This unique property makes pick-up coils immensely suitable for high frequency magnetic field measurements.

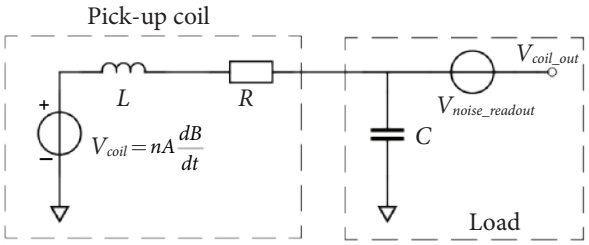

Figure 2.30 Simplified model of a pick-up coil.

The source impedance of a pick-up coil contains an inductive component, as shown in Figure 2.30. In the voltage readout mode, the two terminals of the pick-up coil are left open, and will be effectively loaded by a parasitic capacitor. With the source resistance $R = 0\ \Omega$, the coil will oscillate at the resonating frequency:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{2.25}$$

This resonant behavior is desirable in frequency references, but not in magnetic sensors. It can be suppressed by using a large source resistance R, as shown in Figure 2.31. For magnetic field measurement, pick-up coils can work with three different mechanisms. (1) At low frequencies (up to $0.1f_0$ in Figure 2.31), the source impedances of the pick-up coils are negligible compared to the load impedance, therefore the output V_{coil_out} is linearly proportional to the input frequency. In this region, the magnetic signal needs to be reconstructed by an integrator. (2) In the frequency region defined by the two time constants RC and L/R, the capacitive load impedance become negligible to the source resistance R, thus the magnetic signal is directly integrated, resulting in a flat frequency response in that region. In this region, no integration is required to reconstruct the magnetic signal. (3) At even higher frequencies, the source inductance starts to dominate the source impedance, therefore the output voltage starts to decrease with the magnetic field frequencies.

Due to the presence of a source resistance R, thermal noise is expected at the outputs of a pick-up coil. This noise is then filtered by the RC time constant. However, to read out the pick-up coil, additional noise will be generated by the readout electronics, which is unfortunately unfiltered. For the sake of noise analysis at the system level, the input referred thermal noise $V_{noise\_readout}$ of the readout circuitry is assumed to dominate the overall performance, as shown in Figure 2.30. When further referred to the magnetic field domain, the readout noise behaves differently in different frequency ranges, as shown in Figure 2.32. At low frequencies, the input referred noise density

exhibits a $1/f^2$ characteristic due to the differentiating characteristic of the pick-up coils, as explained in Figure 2.31. In region 2, a flat noise floor is expected due to the frequency-independent sensitivity. At high frequencies, the noise density starts to increase again due to the reduced sensitivity.

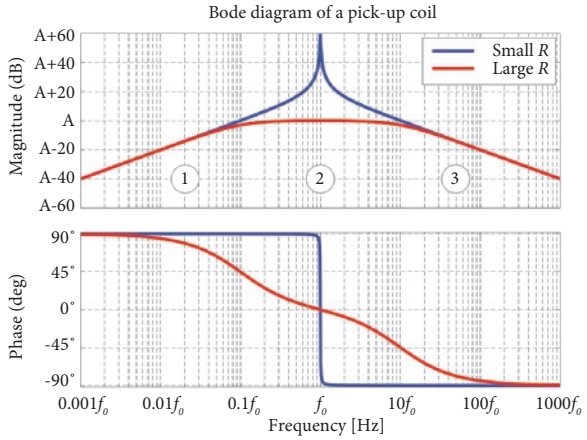

Figure 2.31 Bode diagram of the magnetic-to-voltage transfer function of a pick-up coil with different source resistances.

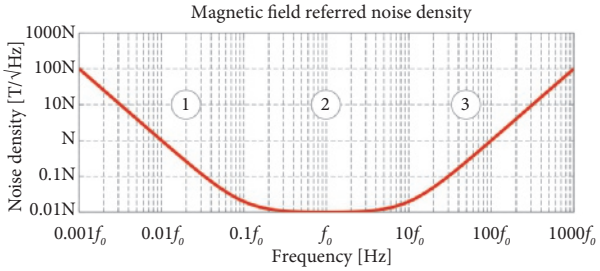

Figure 2.32 Magnetic referred noise density of a pick-up coil, with noise dominated by the thermal noise of the readout circuitry.

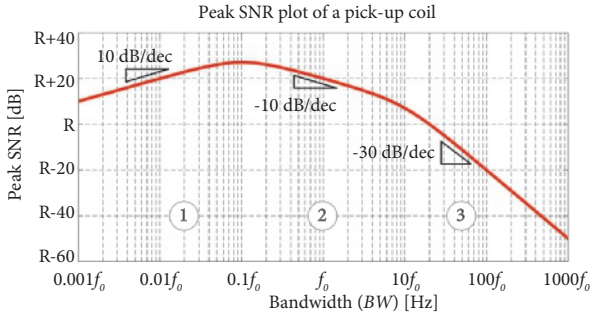

Figure 2.33 Peak SNR plot of a pick-up coil.

For optimum noise performance, pick-up coils are usually designed to work in the first two frequency regions. This is more pronounced in the resulting peak signal-to-noise ratio (SNR) plot of pick-up coils, as shown in Figure 2.33. In frequency region 1, the differentiating characteristic of the pick-up coils produces a signal power proportional to the squared maximum signal frequency (BW^2), while the noise power is linearly proportional to the signal bandwidth (BW). Therefore the peak SNR increases 10 dB/decade. When entering the linear frequency range (region 2), the signal power remains constant, so that the peak SNR starts to drop by -10 dB/decade. At high frequencies in region 3, the SNR decreases even faster (-30 dB/decade) due to the decreased signal power.

Unlike Hall sensors, pick-up coils produce output signals with large amplitudes, and therefore require different readouts. In the differentiating regions, the output signals need to be reconstructed by an integrator. Thanks to their frequency-dependent impedance, the integration process can be performed by the coils themselves once their impedance exceeds that of the load, i.e. a resistor R_L [24], as shown in Figure 2.34. To preserve the voltage readout topology, the load resistance R_L is made large enough such that the source resistance of the pick-up coils R can be neglected. Together with the source inductance L, a time constant is formed by R_L, which integrates the signals the frequencies of which are greater than:

$$f_c = \frac{R_L}{2\pi L} \tag{2.26}$$

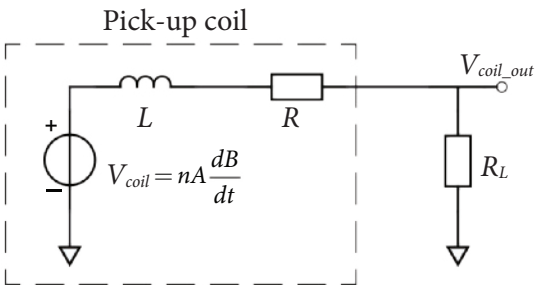

Figure 2.34 Integrator built by a resistor.

However, this approach has no driving capability, which is solved by adding another buffer. As the noise is dominated by the thermal noise of the load resistor, the increase in bandwidth will decrease the peak SNR by -10 dB/decade as explained in Figure 2.33.

Alternately, active integrators can be used to read out pick-up coils as magnetic sensors. Taking advantage of the source resistance of the pick-up coils, an active RC integrator can be built, as shown in Figure 2.35. The voltage output of the pick-up coil is converted into a current signal through its own source resistance R, and integrated on the feedback capacitor C_0. To set the DC

biasing point of the opamp, a feedback resistor R_0 is placed in parallel with C_0, which effectively creates a pole at:

$$f_c = \frac{1}{2\pi R_0 C_0} \tag{2.27}$$

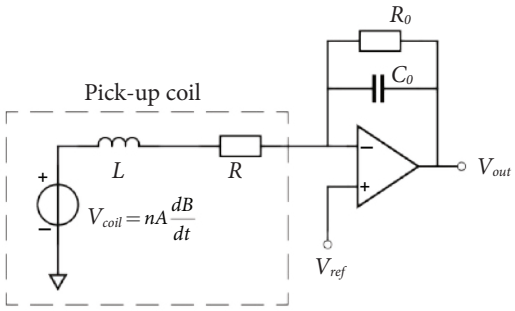

Figure 2.35 Active RC integrator to read out a pick-up coil.

In this approach, thermal noise at the input of the integrator will be effectively filtered by the 1st order LPF with a corner frequency of f_c. At the final outputs, f_c becomes the bandwidth of the noise transfer function, as shown in Figure 2.36. This suggests that irrespective of the signal bandwidth, the total output noise power is always fixed. As a result, the increase in bandwidth from f_c does not affect the overall SNR.

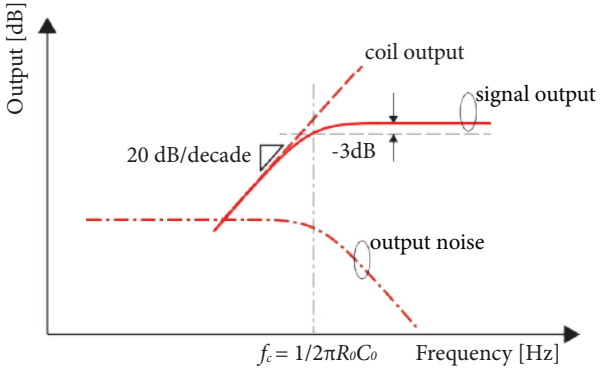

Figure 2.36 Signal and noise transfer functions of a pick-up coil-based system with active integrator readout.

However, the RC integrator exploits the source resistance of the pick-up coil. A relatively high temperature coefficient can be expected in CMOS processes. For instance, when built with copper, the resistance temperature coefficient is about 0.4%/˚C. Over a temperature range of 100˚C, the total source resistance will change over 40%. Therefore, additional temperature compensation is required.

To circumvent the use of temperature compensation, the integrator can be built in a different way so that the pick-up coil is directly read out in the voltage domain, as shown in Figure 2.37. A transconductance amplifier g_m turns the coil's voltage into a current, which is then integrated on C_0. To set the DC biasing point of the g_m stage, a load resistor is added in parallel with C_0. The resulting signal and noise transfer function is exactly the same as shown in Figure 2.36. Due to the absence of feedback, the achievable bandwidth of g_m-C integrators are usually larger than that of active RC integrators. In [24], a 75 MHz integration bandwidth has been achieved with g_m-C integrators.

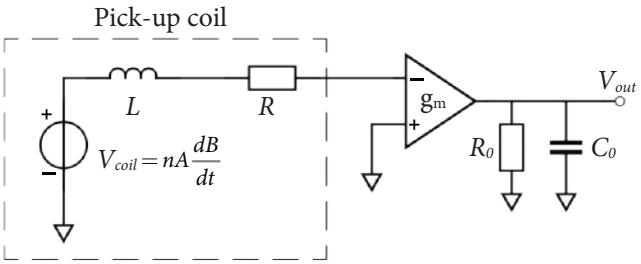

Figure 2.37 g_m-C integrator to read out a pick-up coil.

However, as the pick-up coil can produce large voltage swings to the input of the g_m stage, it places tough requirements on the linear input range of the g_m stage. This is even more profound at higher frequencies as the voltage swing is proportional to the signal frequency. This is usually solved by using different circuit design techniques, e.g. those presented in [20]. Moreover, due to the absence of feedback, the output swings need to be limited to preserve linearity. To limit the output swing of the g_m stage, an integrator combining g_m and active C can be used, as shown in Figure 2.38. As the output current of the g_m stage is fed into the virtual ground of the opamp, practically no voltage swing is required.

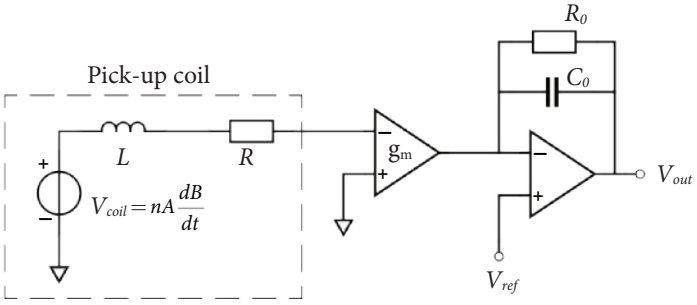

Figure 2.38 g_m- active C integrator to read out a pick-up coil.

Due to the two-dimensional limitations of CMOS processes, on-chip pick-up coils with a large number of windings are usually difficult to realize. With a small flux area and few windings, on-chip pick-up coils are usually used in the RF frequency ranges for communications systems. At

the cost of chip area, the flux area can be increased so that the pick-up coils can work down to 100 kHz. For even lower frequencies, off-chip coils are usually a better choice in terms of cost. To the author's best knowledge, the only commercially available magnetic sensors based on on-chip pick-up coils are the Si850x/1x family from Silicon Labs [25], which can work in the frequency range from 50 kHz to 1 MHz.

2.4 Conclusions

This chapter reviews magnetic sensor technologies in CMOS processes, namely Hall Effect sensors and pick-up coils. Hall sensors are preferably used for low frequency magnetic field measurements, while pick-up coils are well suited for high frequency measurements. Some of the unsolved challenges associated with interfacing those sensors will be addressed in the following chapters: the offset-associated bandwidth limitation of Hall sensors (Chapter 3 and 4), and the noise-associated bandwidth limitations of both Hall sensors (at high frequencies) and pick-up coils (at low frequencies) (Chapters 5 and 6).

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A Continuous-Time Ripple Reduction Technique for Spinning Current Hall Sensors

3

3.1 Introduction

The spinning current technique is commonly used to suppress the offset of CMOS Hall sensors. It involves up-modulating the Hall sensor offset to a spinning frequency f_{spin}, thus converting it into square-wave ripple. This ripple is usually filtered out by a low-pass filter (LPF). However, this filter also limits the signal bandwidth. This is because f_{spin} is typically rather low (a few kilohertz), in order to allow the sensor to settle sufficiently after each change in bias current direction. As a result, the resulting analog filter requires large time constants, and thus occupies considerable area. Since increasing the spinning frequency leads to greater residual offset [1], the use of analog filters results in a tradeoff between filter area and offset. An alternative is to digitize the sensor outputs and then implement the LPF in the digital domain. This approach is particularly effective when a sigma-delta ADC is used, since the notches of the decimation filter can be reused for ripple suppression [2]. However, the bandwidth of the resulting digital LPF will still be less than $1/2f_{spin}$. For these reasons, the bandwidth of CMOS Hall sensors is typically limited to less than 100 kHz [1], even though the sensor's intrinsic bandwidth can be in the gigahertz range [3].

In this chapter, a ripple reduction technique is presented that continuously measures and cancels the spinning ripple, and thus eliminates the need for any low-pass filtering. The rest of the chapter is organized as follows: Section 3.2 introduces the basic ripple reduction loop (RRL) scheme which has been used in chopper instrumentation amplifiers and two-phase spinning current Hall sensors. The proposed ripple reduction technique for four-phase spinning current Hall sensors is then presented in Section 3.3. Section 3.4 describes a prototype sensor that verifies the proposed technique. The experimental results are shown and discussed in Section 3.5. Finally, Section 3.6 concludes the chapter.

3.2 Ripple Reduction Loop

Ripple reduction loops (RRL) have been used to solve a similar ripple problem in chopper amplifiers [4], where the offset of the amplifier is up-modulated to the chopping frequency, as

This chapter is derived from a journal publication of the authors: J. Jiang, W. J. Kindt, and K. A. A. Makinwa, "A Continuous-Time Ripple Reduction Technique for Spinning-Current Hall Sensors," IEEE Journal of Solid-State Circuits, vol. 49, no. 7, pp. 1525-1534, 2014.

shown in Figure 3.1. The amplitude of the offset ripple is extracted by a ripple detector, and then integrated. The output of the integrator can be used to cancel the offset V_{os}, thus reducing the offset ripple at the output of the amplifier. At steady state, V_{os} should be fully cancelled by the integrator's output, so that no ripple appears at the output of the amplifier. The use of a RRL eliminates the need for any low-pass filtering, thus preserving the full bandwidth of the system. However, it will introduce a narrow notch at the ripple frequency. Apart from the bandwidth benefit, the dynamic range requirement for the amplifier is significantly relaxed because the offset is cancelled before amplification.

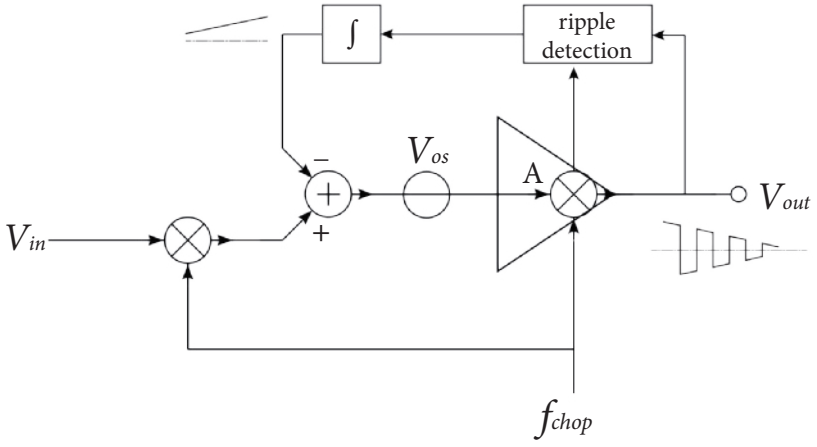

Figure 3.1 RRL in a chopper instrumentation amplifier.

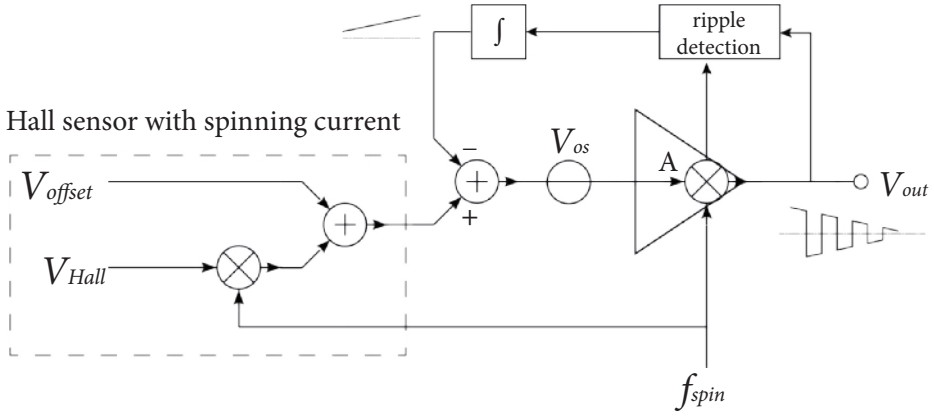

Figure 3.2 RRL in a two-phase spinning current Hall sensor.

The same principle can be applied to a two-phase spinning current Hall sensor [5], as shown in Figure 3.2. The spinning currents are applied in such a way that the signal V_{Hall} due to the magnetic field is first up-modulated and then de-modulated after amplification, while the Hall sensor offset V_{offset} is kept at DC, merged with the readout offset V_{OS}, and converted into spinning ripple at the output of the amplifier. The ripple amplitude is then extracted and integrated. The

output of the integrator is used to cancel both V_{offset} and V_{os}, thus preventing any ripple from appearing at the output of the amplifier. Since no further low-pass filtering is required, the system's useful bandwidth extends beyond the spinning frequency. Moreover, because the offset of the Hall sensor V_{offset} is usually orders of magnitude larger than the signal V_{Hall}, the reduction in the amplifier's dynamic range requirement can be even more profound.

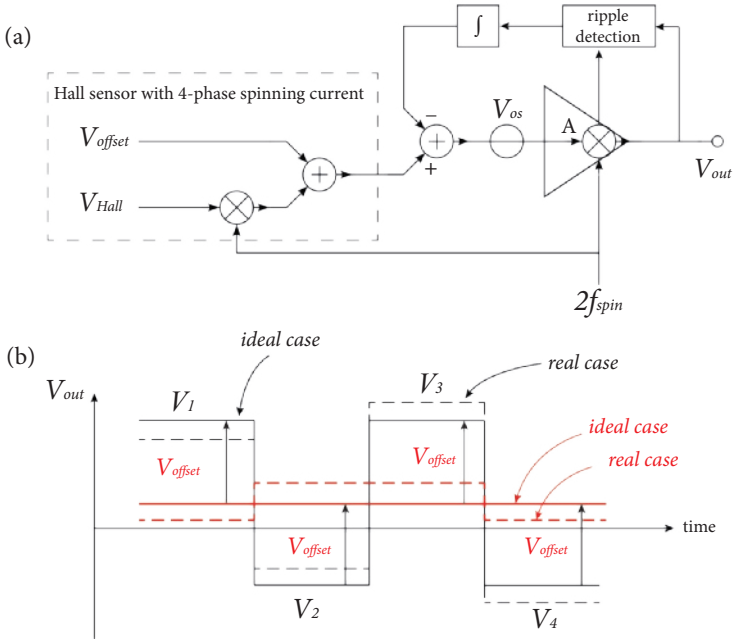

Figure 3.3 (a) RRL used in a four-phase spinning current Hall sensor, and (b) a time domain sketch of V_{out}.

However, due to the anisotropy and JFET effect of the n-well, a two-phase spinning current Hall sensor exhibits considerable residual offset, and so for precision applications four- or even eight-phase [6, 7] spinning current Hall sensors are used. When applying the RRL scheme to a four-phase spinning current, the ripple detector must be modified to extract the average ripple amplitude over four spinning phases, as shown in Figure 3.3 (a). However, the RRL scheme only works under the assumption that the offset of the Hall sensor is constant over all spinning phases. In Figure 3.3 (b), an ideal offset ripple is indicated by the black solid line. By extracting the average ripple amplitude, the ripple can be reduced to the red solid line, which corresponds to the amplified signal V_{Hall}.

In reality, the RRL scheme does not work optimally, mainly because the offset of the Hall sensor changes over different spinning phases due to the n-well anisotropy and JFET effect. As shown in Figure 3.3 (b), an offset ripple with visible non-ideality is indicated by the black dotted line, the amplitude of which changes over the 1st/2nd and 3rd/4th spinning phases. Applying the same RRL scheme leads to a considerable residual ripple (indicated by the red dotted line)[8], which in most

cases still requires low-pass filtering. However, the use of this RRL scheme still substantially reduces the sensor offset and thus facilitates the use of a high gain front-end, as in [9].

3.3 Triple RRL Scheme

For most precision applications that employ at least a four-phase spinning current Hall sensor, the use of a single RRL leads to considerable residual ripple, which still requires some low-pass filtering to remove. A sketch of the output of a four-phase spinning current Hall sensor is shown in Figure 3.4. The offset has been up-modulated to square-wave ripple, where $V_{1\text{-}4}$ represents the output in the 1st to 4th spinning phases, respectively. The magnetic signal V_{Hall} can be extracted by averaging all four phase outputs:

$$V_{Hall} = \frac{V_1 + V_2 + V_3 + V_4}{4} \tag{3.1}$$

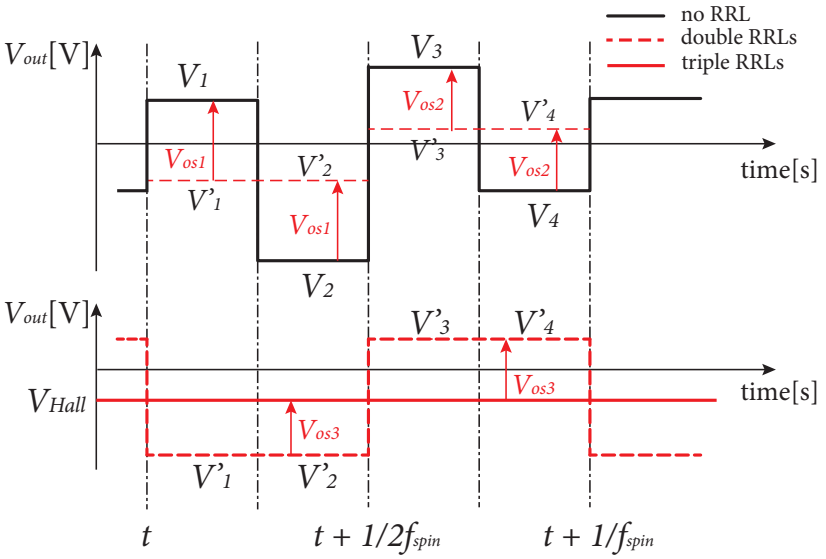

Figure 3.4 Algorithm of tripe RRLs for four-phase spinning current Hall sensors.

The proposed ripple reduction technique can be explained in three parts as follows:

1) A simple RRL scheme is applied to only the 1st and 2nd spinning phases. The RRL detects the difference between V_1 and V_2 and extracts a ripple component of V_{os1}, which is then integrated to compensate for the Hall sensor offset in the 1st and 2nd phases. As shown in Figure 3.4, any ripple associated with these phases is therefore cancelled, resulting in the red dotted line representing:

$$V_1' = V_1 - V_{os1} = V_2' = V_2 + V_{os1} \tag{3.2}$$

in which:

$$V_{os1} = \frac{V_1 - V_2}{2} \tag{3.3}$$

2) A similar scheme can be used in the 3rd and 4th spinning phases, which eliminates any ripple associated with the 3rd and 4th phases, resulting in the red dotted line representing:

$$V_3' = V_3 - V_{os2} = V_4' = V_4 + V_{os2} \tag{3.4}$$

where:

$$V_{os2} = \frac{V_3 - V_4}{2} \tag{3.5}$$

After completing the first two steps, this double RRL scheme will orthogonally suppresses the offset ripple in the 1st/2nd phases and 3rd/4th phases. As a result, any ripple at $2f_{spin}$ is then removed. However, as shown in Figure 3.4, a residual ripple (red dotted line) may still remain between V_1'/V_2' and V_3'/V_4' at f_{spin}.

3) A third RRL is applied at the frequency of f_{spin} extracting any ripple components between the 1st/2nd phases and 3rd/4th phases, thus compensating the residual ripple. The extracted residual ripple component can be expressed as:

$$V_{os3} = \frac{(V_1 + V_2) - (V_3 + V_4)}{4} \tag{3.6}$$

This triple RRL scheme continuously measures and cancels the ripple, and hence the offset, associated with the four-phase spinning current operation. Moreover, the three loops involved in the scheme are orthogonal and thus can be operated in parallel. With Equations (3.1) (3.3) (3.5) and (3.6), we can rewrite $V_{1\text{-}4}$ as:

$$V_1 = V_{Hall} + V_{os1} + V_{os3} \tag{3.7}$$

$$V_2 = V_{Hall} - V_{os1} + V_{os3} \tag{3.8}$$

$$V_3 = V_{Hall} + V_{os2} - V_{os3} \tag{3.9}$$

$$V_4 = V_{Hall} - V_{os2} - V_{os3} \tag{3.10}$$

3.4 Triple RRL Implementation

In this section, a proof-of-the-concept implementation in a 0.18 μm CMOS process is presented to validate the triple RRL scheme. With the help of off-chip components, the proposed system achieves an offset of 25 μT and a bandwidth of over 100 kHz with a spinning frequency of only 1 kHz.

3.4.1 Capacitively Coupled Pre-Amplifier

As discussed previously in Chapter 2, CMOS Hall sensors usually produce a weak signal which requires amplification for robust readout. As the common mode output of a Hall sensor will depend on the biasing current, the readout needs to have a wide common mode input range. For this reason, differential difference amplifiers (DDAs) are often used as the first amplifiers in a Hall sensor interface. However, since a DDA requires two low noise input pairs, this topology is usually not very power efficient. Furthermore, the mismatch between the input pairs will inevitably degrade the gain accuracy.

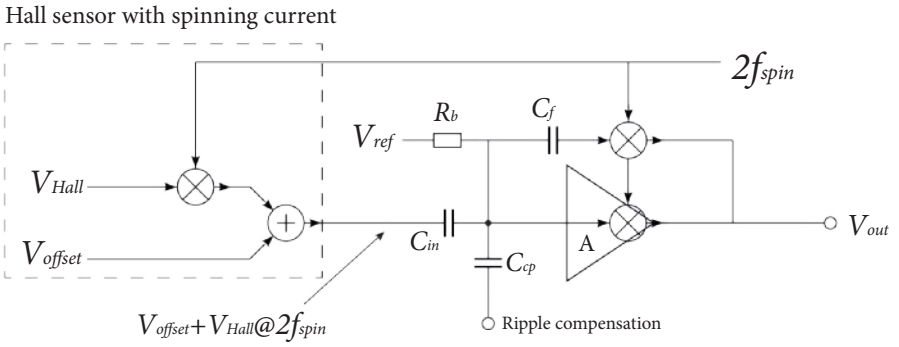

Figure 3.5 Capacitively coupled instrumentation amplifier which can be used to read out a spinning current Hall sensor. The input capacitor C_{in} reduces the offset amplitude and automatically adjusts the common mode voltage.

To improve the power efficiency and the gain accuracy, a capacitively coupled chopper instrumentation amplifier (CCIA) is used [4], as shown in Figure 3.5. The gain of the CCIA is set by C_{in}/C_f. The spinning current scheme is arranged in such a way that the offset V_{offset} is kept at DC while the signal V_{Hall} is up-modulated. The input chopper of the CCIA in this case is actually combined with the spinning current switches, which helps to reduce system complexity and charge injection effect. The magnetic signal is then demodulated within the CCIA. The presence of an input capacitor C_{in} blocks DC offset from the Hall sensor, while passing the up-modulated V_{Hall} at $2f_{spin}$. The common mode voltage at the output of the amplifier will be controlled by its own common mode feedback, which is irrespective of the biasing current of the Hall sensor. The resistor R_b is used to set the DC biasing point of the virtual ground. To minimize the noise penalty introduced by R_b, the resistor is implemented with MOS transistors biased in the sub-threshold region. The resulting equivalent resistance is about 10 GΩ, which hardly introduces any extra noise.

The input referred noise of the CCIA is dominated by that of the opamp, which can be expressed as:

$$V_n = \left(\frac{C_{in} + C_f + C_g}{C_{in}}\right) \cdot V_{nopamp} \tag{3.11}$$

where V_n and V_{nopamp} represent the input referred noise of the CCIA and the input referred noise of the opamp, respectively. Here, C_g is the input capacitance of the opamp. The CCIA's noise should be low enough to ensure that the system's noise performance is dominated by the Hall sensor. Achieving low noise requires a large g_m, which in turn requires large input transistors with a large C_g. Therefore, C_{in} must be made large enough to minimize the effect of V_{nopamp} on the overall performance. In this design, C_{in} is 48 pF, which results in an input impedance of over 5 MΩ at f_{spin} = 1 kHz, and an input referred noise of about 10 nV/√Hz. Since the sensitivity of the Hall sensor was not characterized a *priori*, the CCIA gain can be flexibly switched between 50 and 800 by changing the feedback capacitor C_f between 960 fF and 60 fF. An auxiliary capacitor C_{cp} (= 240 fF) connected to the CCIA's virtual ground provides an input for the RRLs.

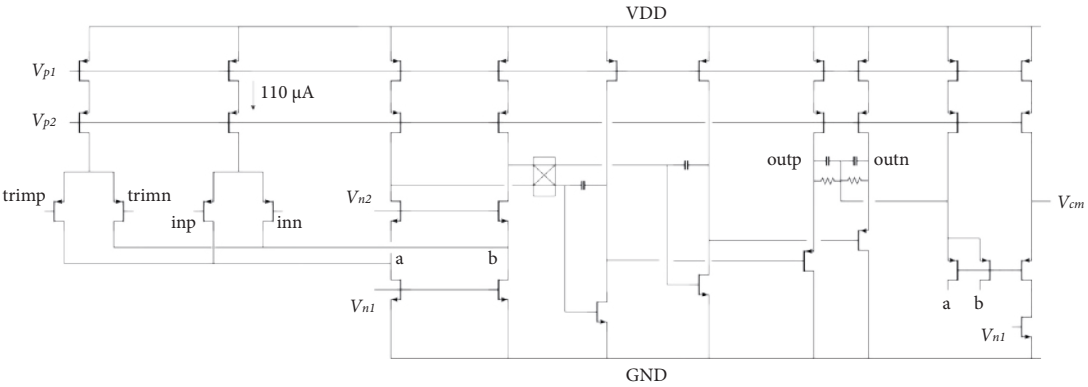

Figure 3.6 Opamp implementation in a CCIA.

The opamp used in the CCIA is shown in Figure 3.6. In order to drive external loads, a two-stage opamp was implemented. It consists of a folded cascode amplifier followed by a class-A gain stage whose outputs are buffered by source followers. Each transistor of the input pair is biased in weak inversion at 55 µA, resulting in a g_m of about 1 mS. The opamp has a DC gain of 96 dB and a GBW of about 10 MHz with a 50 pF load. The source followers relax the need for large resistors in the common mode feedback and can also drive the bond pads. The opamp offset can be trimmed by applying an external voltage to an auxiliary input pair with a g_m of about 10 µS.

3.4.2 Spinning Current with Four-Phase Non-Overlapping Clock

The implementation of the spinning current Hall sensor is shown in Figure 3.7, where clocks $ph_{1\text{-}4}$ control the direction of the biasing current, while signals $out_{1\text{-}4}$ control the location of the output ports. As the biasing current and the location of the output ports of the Hall sensor are

periodically switched, transient spikes will be present in the output signal of the sensor. Therefore the timing of the signals $out_{1\text{-}4}$ implements a short deadband, during which the CCIA is briefly disconnected from the Hall sensor while the bias currents are allowed to settle.

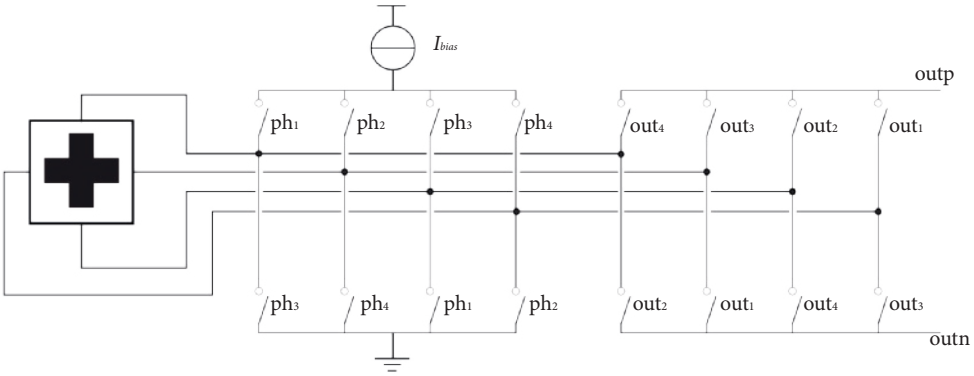

Figure 3.7 Implementation of the four-phase spinning current Hall sensor.

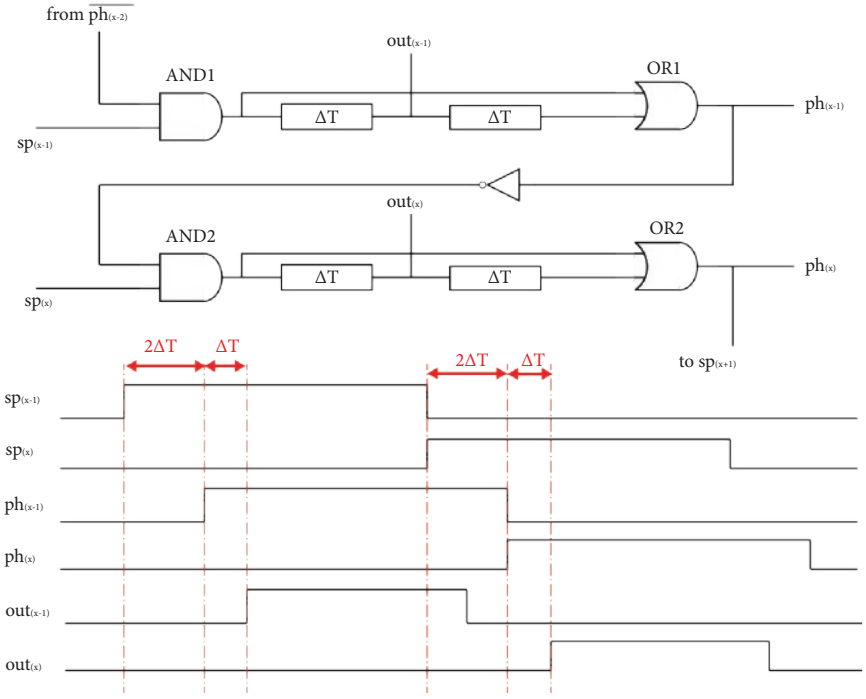

Figure 3.8 Implementation of the four-phase non-overlapping clocks.

The implementation of the four-phase non-overlapping clock is shown in Figure 3.8. Signals $sp_{(x)}$ (x=1-4, and when x=1, x-1=4) are generated by a synchronized four-phase counter. Assuming at certain moments that $sp_{(x-1)}$ has a stable logic value of 1, then all other $sp_{(x)}$ signals should have a logic value 0. When the spinning current Hall sensor is switching from one phase to another, i.e.

when the falling edge of $sp_{(x-1)}$ and the rising edge of $sp_{(x)}$ occur as a result of the counter operation, the falling edge of $ph_{(x-1)}$ will be delayed for 2ΔT, which de-freezes the output of AND2 and instantaneously triggers the rising edge of $ph_{(x)}$. In other words, all clock transients of the $ph_{(x)}$ clocks are delayed by 2ΔT from $sp_{(x)}$ clocks. The rising edge of $out_{(x)}$, however, features an extra ΔT delay from the falling edge of $ph_{(x-1)}$, while its falling edge happens ΔT in advance before the falling edge of $ph_{(x)}$. In conclusion, $ph_{(x)}$ features a 2ΔT delay of corresponding $sp_{(x)}$, and the rising edge of $out_{(x)}$ features a 3ΔT delay of $sp_{(x)}$, while its falling edge is only delayed by 1ΔT. Therefore, the non-overlapping operation of $out_{(x)}$ is realized with a dead-band time of 2ΔT. In this design, ΔT is about 2 ns, thus the switching dead-band is about 4 ns.

It is important to notice that the deadband time in this design is only intended to prevent the spinning spikes from reaching the CCIA. When other issues, i.e. thermal settling of the Hall sensor, are a concern, the dead-band time should be adjusted accordingly.

3.4.3 Triple RRL Implementation

To verify the triple RRL scheme flexibly, it was implemented with off-chip components, as shown in Figure 3.9. The output of the CCIA is first digitized by an ADC, and then processed in a CPLD to extract the three offset components mentioned in Section 3.3. With the proper combination of the three offset components, the CPLD drives a DAC that cancels the offset of the Hall sensor in all four spinning phases.

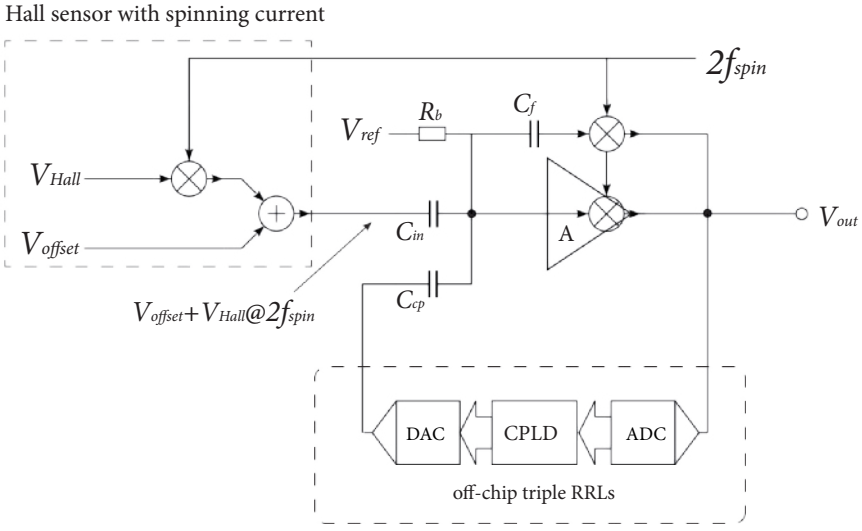

Figure 3.9 Hall sensor system with a CCIA and off-chip digital triple RRLs.

The off-chip ADC and DAC both have a resolution of 16 bits, which corresponds to a magnetic field resolution of 7.6 μT when a reference of 2.5 V is used. Another important requirement is that the DAC needs to be monotonic, otherwise the loop may start oscillating under certain

circumstances. The auxiliary capacitor C_{cp} in this design is 240 fF, which is much smaller than C_{in} (48 pF) and thus helps to minimize the noise contribution of the triple RRLs.

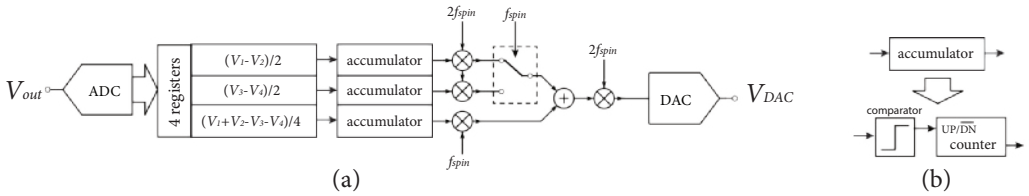

Figure 3.10 Implementation of the triple RRL scheme in CPLD: (a) accumulator-based implementation, and (b) comparator and counter-based implementation.

The triple RRL scheme was first implemented with a CPLD, as shown in Figure 3.10. The output of the voltages $V_{1\text{-}4}$ by the CCIA during the four spinning phases are sampled by the 16-bit ADC. The digital results are then stored and processed in CPLD to extract the three residual offsets (V_{os1}, V_{os2} and V_{os3}). These signals are then integrated by two 17-bit (V_{os12}) and one 18-bit (V_{os3}) accumulators, the 16 MSBs of which are then combined and applied to the 16-bit DAC to generate the appropriate compensation signal V_{DAC} for each spinning phase.

As the ADC under-samples the CCIA's wide-band noise, the computed offsets are rather noisy. This problem can be mitigated by increasing the length of the accumulators to slow it down. However, this approach leads to an increase in the number of logic gates required to implement the adder of the accumulator.

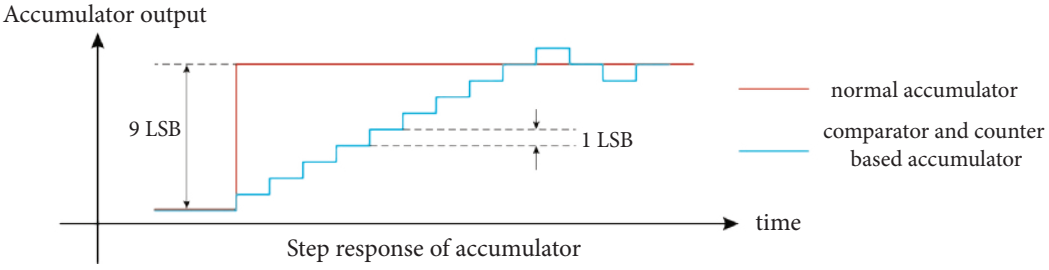

Figure 3.11 Example of a step response for both a normal accumulator and a comparator and counter-based accumulator.

An easy way to alleviate this issue is to replace the normal accumulators with comparators and up/down counters [10] to create an accumulator with a larger time constant, as shown in Figure 3.10 (b). The comparators measure only the polarity of the offset components, and increment or decrement the counters by 1 LSB. Figure 3.11 shows a sketch of the step response of both the normal accumulator and the comparator and counter-based accumulator. For an input step of 9 LSB, the comparator and counter-based accumulator takes nine steps to reach the desired state, which is nine times slower than the normal accumulator. At steady state, the counter toggles within ±1 LSB, which in this case corresponds to a residual offset ripple of 7.6 μT.

3.5 Experimental Results

The Hall sensor and CCIA were implemented in a 0.18 μm 5V CMOS process. The chip photo is shown in Figure 3.12. Four orthogonal Hall plates are connected in parallel to further reduce the raw offset of the Hall sensor. As shown in Figure 3.13, the Hall plates were fabricated as an n-well plate with a p+ pinch layer, which somewhat reduces the thickness and thus increases the sensitivity [11] of the Hall plate. Moreover, the reverse-biased p+/n junction creates a depletion region which effectively isolates the sensor from the crystal defects present at the Si/SiO_2 interface, and therefore reduces the sensor's flicker noise [12]. Furthermore, the presence of the p+ layer keeps the Hall sensor away from the shallow trench isolation (STI) oxide, which reduces the stress-related offset.

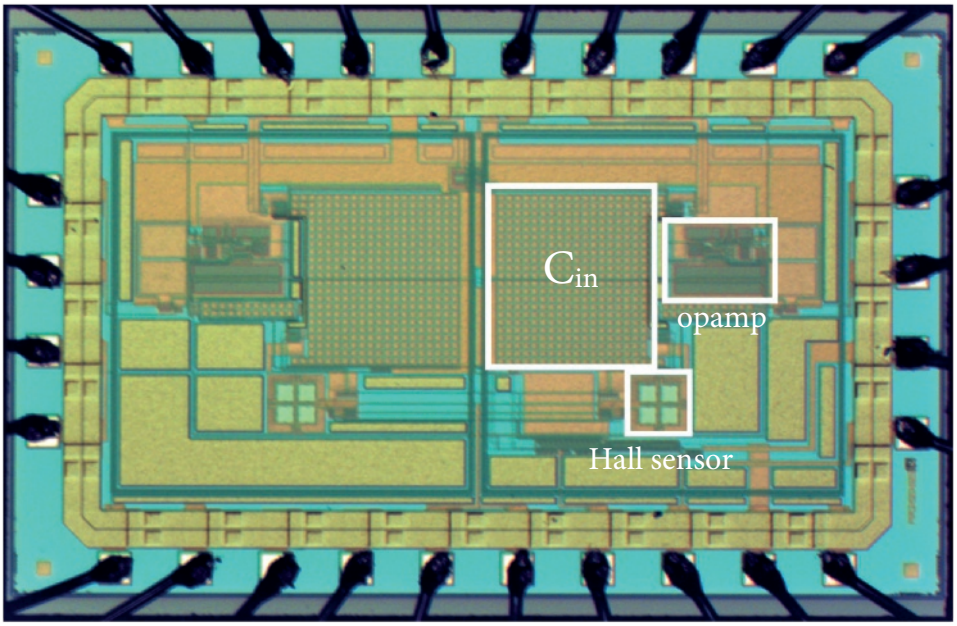

Figure 3.12 Micro photo of the test chip.

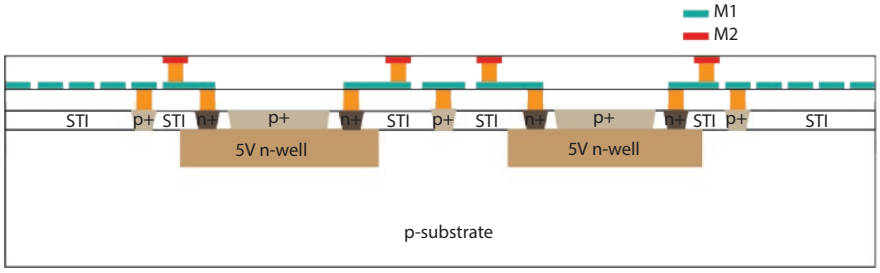

Figure 3.13 Cross-section of the composite Hall sensor. The p+ layer and n-well create a depletion region to reduce the thickness of the n-well and isolate the n-well from the Si/SiO_2 interface.

The composite Hall sensor has a measured sensitivity of 50 mV/T when biased with 0.35 mA per Hall plate, which varies about 3% among the eight samples measured. With f_{spin} = 1 kHz, the measured offsets of the eight samples have a mean value of 3 μT, with a standard deviation of 16 μT. The maximum measured offset was less than 25 μT. The measured noise of Hall sensor and CCIA corresponds to an input referred noise of 0.28 μT/√Hz.

The measured residual offsets of the sensors show strong correlations with the spinning frequency f_{spin}, as shown in Figure 3.14. It can be seen that the sensor's residual offset increases dramatically when the spinning frequency f_{spin} exceeds 10 kHz, which is in line with [1]. This can be caused by insufficient thermal settling of the Hall sensor, unbalanced charge injection associated with the spinning current switches and the CCIA, and the finite linearity and dynamic range of the CCIA. To minimize the offset, the remaining measurements were carried out with the spinning frequency f_{spin} fixed at 1 kHz.

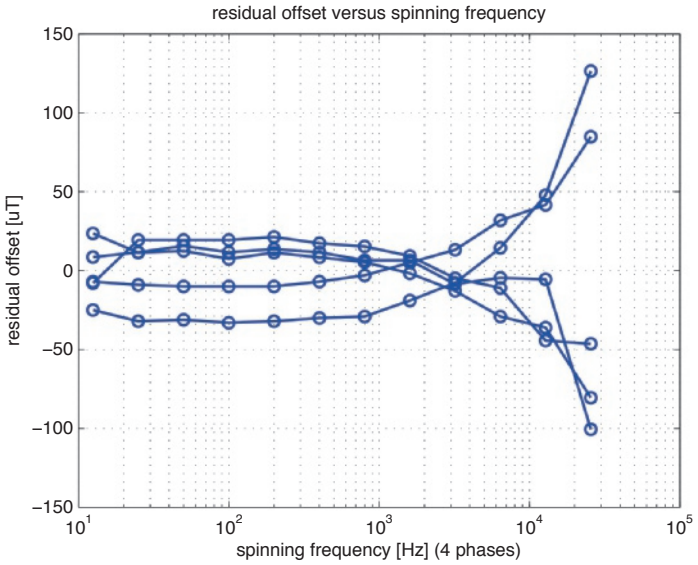

Figure 3.14 Residual offset versus spinning frequency. The residual offset is stable when f_{spin} < 1 kHz, and increases dramatically when f_{sipn} > 10 kHz.

3.5.1 Residual Ripple Measurement

To properly measure the ripple caused by the spinning current Hall sensor, the CCIA offset was first trimmed by placing the test chip inside a zero-Gauss chamber, disabling the spinning clocks and then applying a fixed voltage at the auxiliary diff-pair (Figure 3.6), which drives the output of the CCIA to zero. The outputs of the test chip was digitized by a data acquisition (DAQ) card with a 16-bit ADC. The results were stored and then processed in MATLAB to make the FFT plot, where spinning ripple can be clearly observed in the frequency domain.

The CPLD was first configured with a single RRL scheme, as shown in Figure 3.3. The CPLD extracted only one offset component by averaging the outputs of all four phases, which was then applied to cancel the Hall sensor offset. The resulting FFT plot of the CCIA output is shown in Figure 3.15, where the ripple at $2f_{spin}$ (= 2 kHz) is effectively suppressed to -90 dB. However, by looking at the spectrum component at f_{spin} (= 1 kHz) and its odd-order harmonics, we can conclude that a square-wave residual ripple at f_{spin} remains un-compensated, which is more than two orders of magnitude higher than the noise level. To low-pass filter this amount of residual ripple, what is required is either a 2nd order analog filter with a cut-off frequency of 100 Hz or a digital averaging circuit, resulting in a usable bandwidth of either 100 Hz or 500 Hz, respectively.

The logic of the triple RRL scheme shown in Figure 3.10 (a) was then implemented with CPLD. The resulting FFT plot of the CCIA output is shown in Figure 3.16. The residual ripple in Figure 3.15 is now effectively suppressed. However, as the ADC under-samples the CCIA output, the aliasing effect makes the calculated offset value rather noisy, which leads to an increased noise floor around the ripple reduction frequencies.

This problem is solved by replacing accumulators with comparators and up/down counters as shown in Figure 3.10 (b). The operation of a comparator and counter-based accumulator effectively increases the associated time constant. The resulting FFT plot of the CCIA output is shown in Figure 3.17, where all offset ripple is effectively suppressed, and the noise floor is quite flat. The residual ripple is about 10 μT, which is commensurate with the sensor's noise into a bandwidth of 1.2 kHz. However, the comparators and up/down counters inevitably increase the start-up time of the triple RRLs. In this design, the maximum start-up time is 6 s.

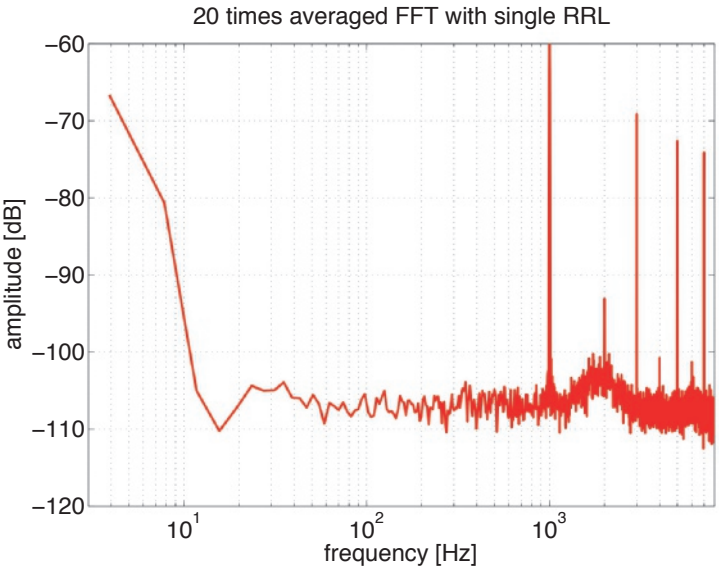

Figure 3.15 FFT plot of the output of the CCIA with a single RRL scheme. The ripple at $2f_{spin}$ is effectively suppressed, however, the spectrum component at f_{spin} and the higher odd-order harmonics suggest a residual square-wave ripple at f_{spin} remains uncompensated.

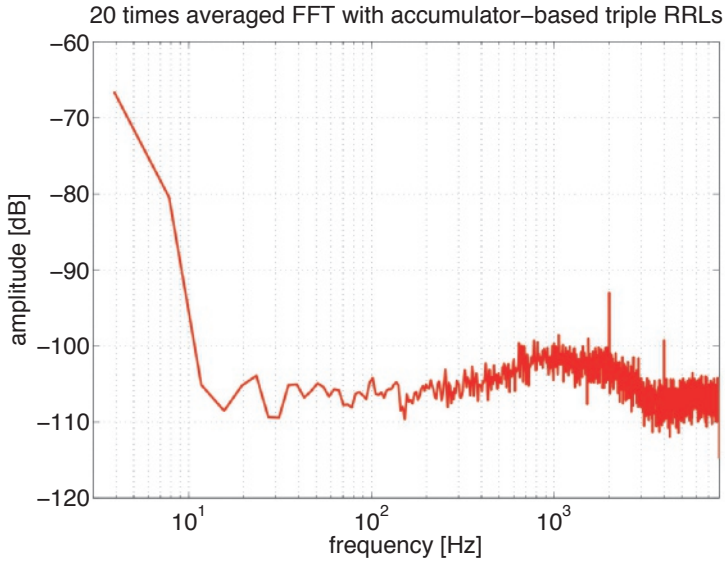

Figure 3.16 FFT plot of the output of the CCIA with the triple RRL scheme. The ripple at both f_{spin} and $2f_{spin}$ is effectively suppressed. The increased noise floor is due to the under-sampled CCIA output in the triple RRLs.

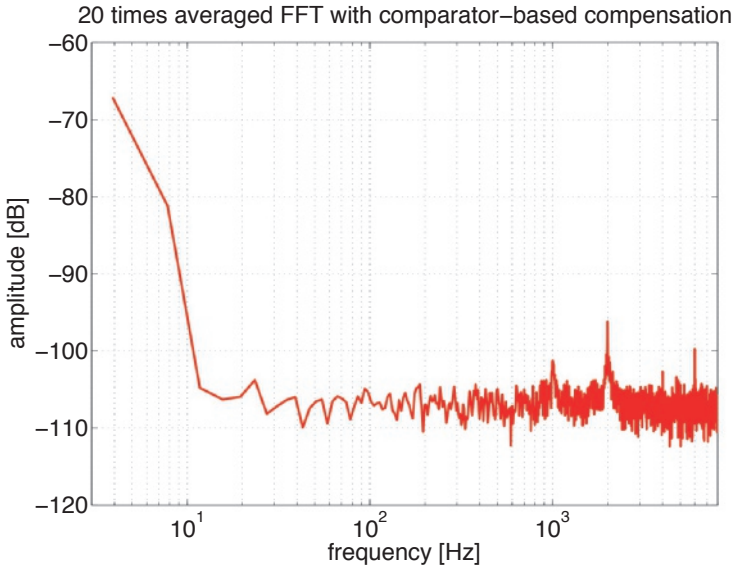

Figure 3.17 FFT plot of the output of the CCIA with comparators and up/down counters in triple RRLs. All offset ripple at f_{spin} and $2f_{spin}$ is effectively suppressed. The noise floor is also flat due to the comparators and up/down counters.

3.5.2 Bandwidth Measurement

To demonstrate the effectiveness of the triple RRL scheme, the bandwidth of the test chip was also measured by a HP3562A spectrum analyzer. The measurement setup is shown in Figure 3.18. To measure the frequency response of the test chip, a spectrum analyzer was used to sweep a sine wave signal from DC to 100 kHz. The generated voltage sine wave drove a voltage-to-current converter to produce a sine wave current through a PCB trace under the test chip, thus generating an AC magnetic field at known frequencies. With the comparator and up/down counter-based triple RRLs, the output of the test chip was buffered by a low noise amplifier with variable gains. The amplified output was then measured by the spectrum analyzer (HP3562A) to calculate the transfer function at specific frequencies.

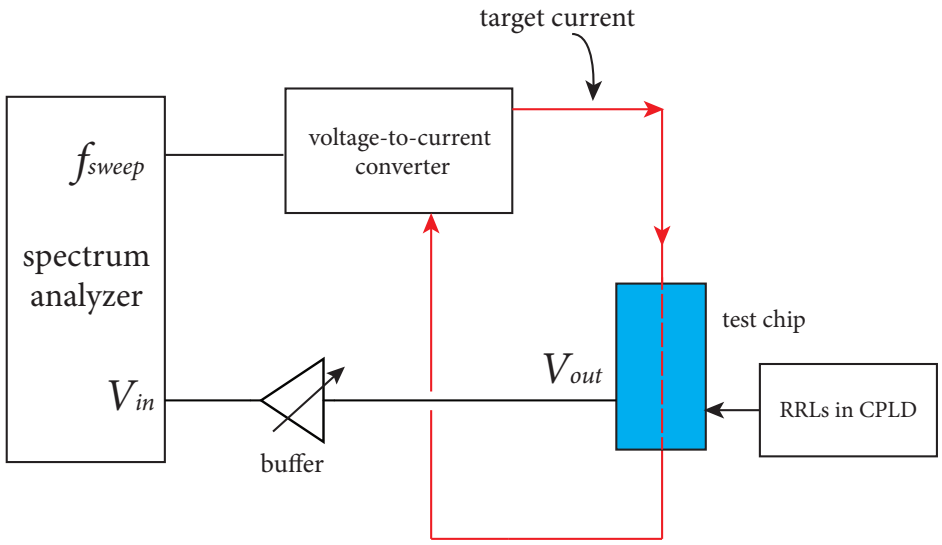

Figure 3.18 Bandwidth measurement setup. The primary current is generated by a spectrum analyzer followed by a voltage-to-current converter.

The CCIA was first configured with a gain of 800. The resulting Bode plot of the transfer function of the test chip is shown in Figure 3.19, which exhibits a -3 dB bandwidth of 12.5 kHz, which is determined only by the bandwidth of the CCIA. The triple RRLs also detect and cancel any signal located at f_{spin} and $2f_{spin}$, resulting in two narrow notches in the system frequency response. When the gain of the CCIA is switched to 50, the bandwidth of the system can be extended to above 100 kHz, which is the upper limit of the spectrum analyzer HP3562A, as shown in Figure 3.20.

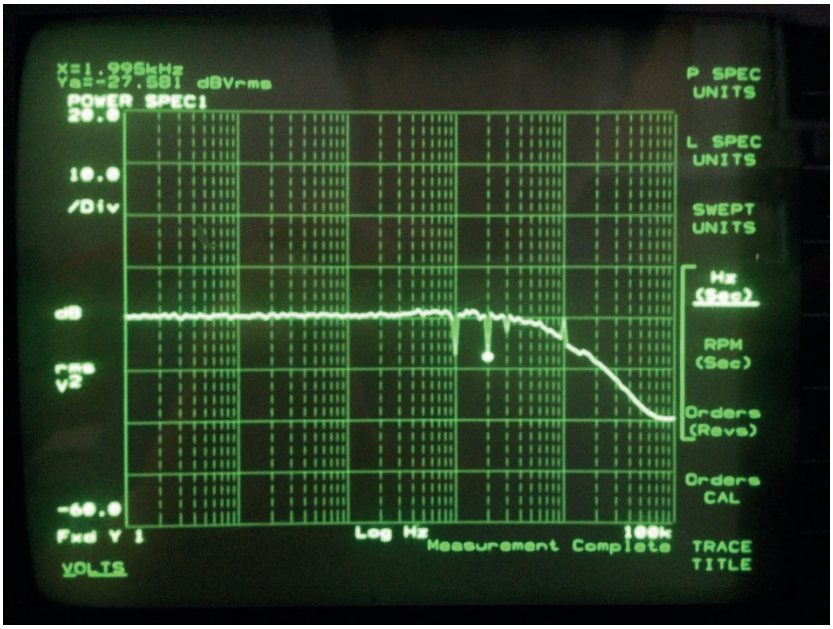

Figure 3.19 Bode plot from the bandwidth measurement with a CCIA gain of 800.

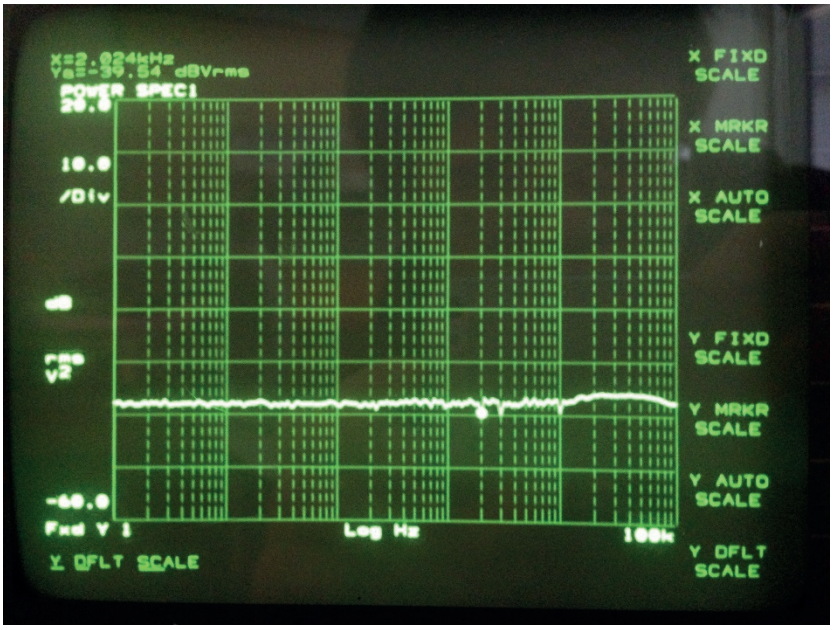

Figure 3.20 Bode plot from the bandwidth measurement with a CCIA gain of 50.

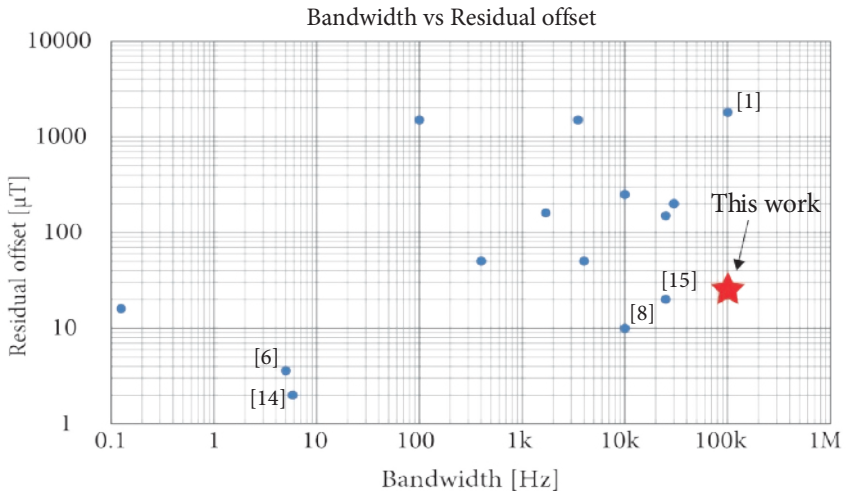

Figure 3.21 Offset versus bandwidth plot of the state-of-the-art Hall sensors until 2015 (see Appendix for more detail).

To compare the work of this chapter with other state-of-the-art Hall sensors, a plot of their offset versus bandwidth (see Appendix for more detail) is shown in Figure 3.21. In [13], a minimum offset of only 2 μT is achieved with help of digital calibration and magnetic concentrator. In [6], a 3σ offset of only 3.65 μT is achieved with eight-phase octagonal spinning current Hall sensors. However, both works have a bandwidth of less than 10 Hz, which is only intended for compass applications. For four-phase spinning current Hall sensors, the work presented in this chapter exhibits a similar offset value compared to [8] [14], with a bandwidth at least four times wider. Compared to other high speed Hall sensors such as [1], this work has improved the offset performance by about 100 times.

3.6 Conclusions

This chapter describes a continuous-time ripple reduction technique for spinning current Hall sensors. Three RRLs continuously measure and compensate the offset ripple associated with spinning current operation, which eliminates any need for further low-pass filtering. As a result, the achievable bandwidth can be further improved, in this case to above 100 kHz, which is no longer limited by the spinning frequency f_{spin}. With the proposed scheme, the test chip simultaneously exhibits a continuous-time analog output with low offset (25 μT), high bandwidth (100 kHz) and low ripple (10 μT), thus solving a problem that has existed for the last three decades. Furthermore, since the offset of Hall sensor is cancelled before amplification, the dynamic range of the readout circuits can be relaxed considerably.

However, the triple RRLs also measure and cancel any signal at f_{spin} and $2f_{spin}$, which creates two narrow notches in the frequency response of the sensor. Again borrowing from the literature on chopper amplifier [15], these notches can be "filled up" with the help of a multi-path architecture, which will be discussed in the next chapters.

3.7 Bibliography

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A Wide-Bandwidth Multi-Path CMOS Hall Sensor with Integrated Ripple Reduction Loops

4

4.1 Introduction

As discussed and demonstrated in Chapter 3, the use of a triple ripple reduction loop (triple RRL) scheme implemented with off-chip components can effectively suppress the offset ripple of spinning current Hall sensors without any low-pass filters (LPFs).

However, the system presented in Chapter 3 built with ADC, CPLD and DAC is quite complex and employs near-ideal off-chip components (ADC, CPLD and DAC). Even though such a system can be integrated on a single die, it may occupy considerable area, thus providing no significant advantages compared to the use of LPFs.

Another limitation of the triple RRLs scheme is that any input signals at f_{spin} and $2f_{spin}$ will be mistaken as spinning ripple, and thus will be suppressed. This translates into two notches in the frequency domain, which are undesirable.

To address the above-mentioned drawbacks, this chapter presents a multi-path Hall sensor system with integrated triple RRLs. The rest of the chapter is organized as follows: Section 4.2 describes the multi-path Hall sensor structure and the analog implementation of the triple RRLs; Section 4.3 shows experimental results which verifies the proposed system; and the conclusions are drawn in Section 4.4.

4.2 Multi-Path Hall Sensor System

The multi-path concept has been used in chopper instrumentation amplifiers to overcome the frequency response notch caused by a ripple reduction loop (RRL) [1]. In a chopper instrumentation amplifier, the use of chopping and a RRL not only suppresses offset and chopping ripple, but also cancels out signals at the chopping frequency f_{chop}. To prevent this, an un-chopped high frequency path can be used to fill up the notch and obtain a flat frequency response. However, this approach cannot be directly applied to a Hall sensor system. This is due

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to the fact that Hall sensors are usually not in any feedback loops. The gain mismatch of the different Hall sensors and their readout paths in a Halls sensor system will appear at the final outputs, resulting in in-band gain variations. As a result, the gain of different paths needs to be carefully designed to match up with each other.

4.2.1 Multi-Path Hall Sensor Structure

To bypass the notches caused by the triple RRL scheme and to achieve higher bandwidth, a multi-path Hall sensor system is proposed as shown in Figure 4.1. The low frequency (LF) path employs the spinning current technique and triple RRLs to suppress offsets and spinning ripple. The LF path signal V_{oL} is then low-pass filtered by the output stage with the crossover frequency f_{cross} defined by the time constant of R_0C_0 and the gain of R_0/R_3. This prevents the notches from reaching the final output V_{out} by making $f_{cross} < f_{spin}$, as shown in Figure 4.2. The high frequency (HF) path uses an identical Hall sensor and readout without the spinning current technique and triple RRLs so that its gain is the same as that of the LF path, i.e. $V_{oH} = V_{oL}$. By replacing R_3 with a capacitor C_3, the output stage effectively acts as a high-pass filter with a cut-off frequency of f_{cross}. This blocks the offset of V_{oH}, but passes its high frequency content, thus filling the notches and extending the system bandwidth.

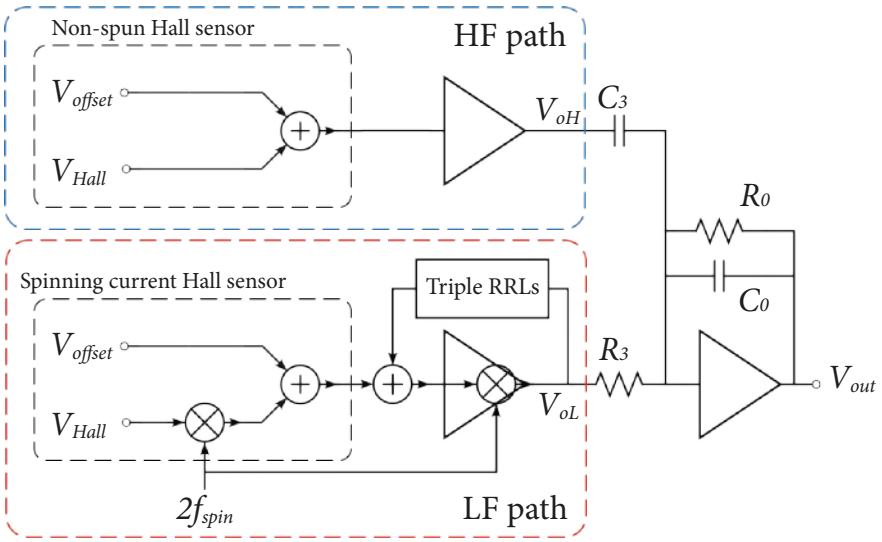

Figure 4.1 System architecture of a multi-path Hall sensor.

To ensure a smooth gain transition, LF and HF path gain can be matched by making $R_0/R_3 = C_3/C_0$, or $R_3C_3 = R_0C_0$. With careful layout in modern CMOS processes, the matching of the two time constants can be better than 1%, which is adequate for contactless current measurements.

A good feature of this architecture is that there is only one time constant involved in the output stage to process both LF and HF path signals. This ensures *perfect* frequency transition between

the two signal paths. The gain matching of the two signal paths is then solely determined by the ratio of passive components R_0/R_3 and C_3/C_0. Should any changes in the environment occur, the gain drifts of both paths will track with each other, ensuring a smooth gain transition.

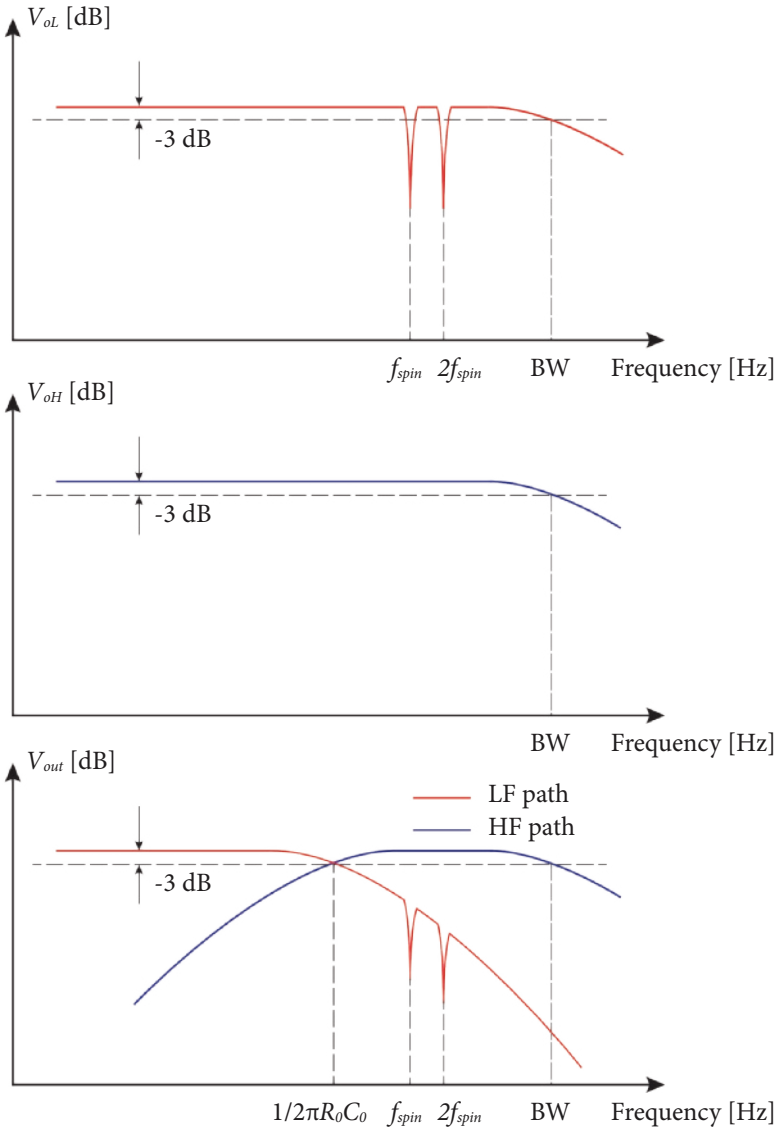

Figure 4.2 Bode plot of the LF path, HF path and the overall system.

4.2.2 System Implementation

A detailed implementation block diagram is shown in Figure 4.3. To ensure good gain matching, both paths use identical Hall sensors and signal paths consisting of two amplifiers: a capacitively

coupled amplifier with a gain of 100, and an inverting amplifier with a gain of 20. Both amplifiers have the same bandwidth of 400 kHz, so that the over frequency response will be flat.

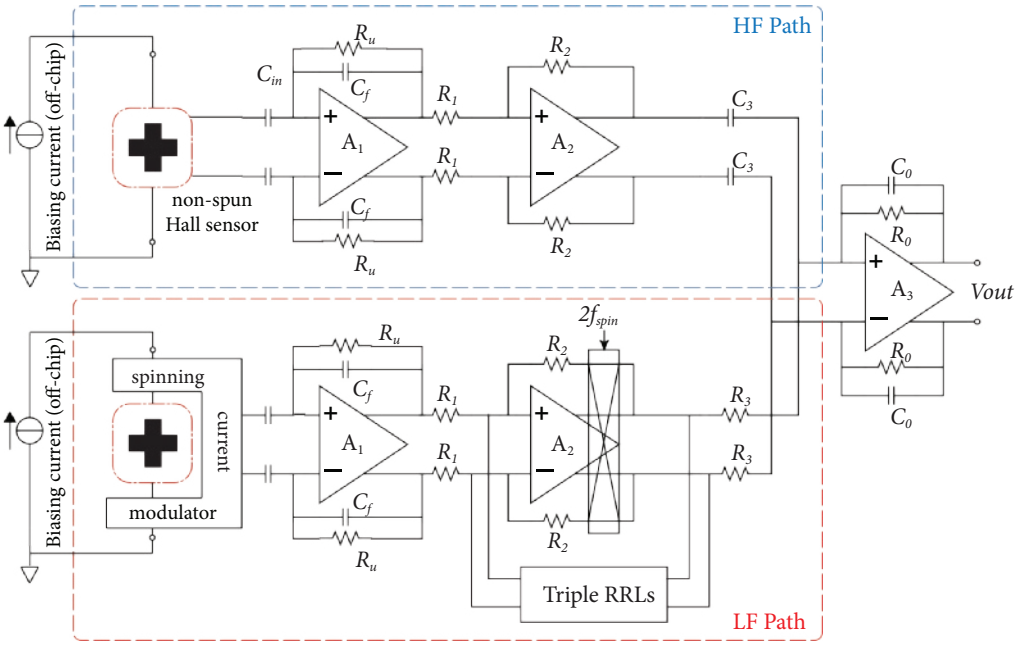

Figure 4.3 Block diagram of the multi-path Hall sensor system.

The spinning ripple in the LF path is suppressed by the integrated RRLs, which inject compensation currents at the virtual ground of A_2. This arrangement greatly relaxes the noise requirement of the triple RRLs thanks to the gain of the preceding stage. Any residual ripple will be further suppressed by the 1st-order low-pass filtering action of the output stage. In this design, the crossover frequency f_{cross} = 2 kHz, and is set by the time constant of R_0C_0 in the feedback of the output stage. This f_{cross} is a compromise between the area, low f_{spin} to ensure good offset, and the need to ensure that the notches will be sufficiently filled by the HF path, i.e., $f_{cross} << f_{spin}$ (10 kHz).

Capacitively Coupled First Stage

The use of a capacitively coupled 1st stage [2] has three advantages: 1) it has better power efficiency than current feedback instrumentation amplifiers or three-opamp instrumentation amplifiers; 2) its capacitively coupled input can handle a wide common mode input range, so that the biasing current of the Hall sensors can be adjusted freely; and 3) a differential sensing structure can be easily implemented by connecting another set of input capacitors to the virtual ground, as shown in Figure 4.4. The DC biasing point of the virtual ground can be defined by a set of high-ohmic resistors. This effectively creates a high-pass filter and configures the opamp in unity gain for offset, which highly relaxes the dynamic range of the succeeding stages.

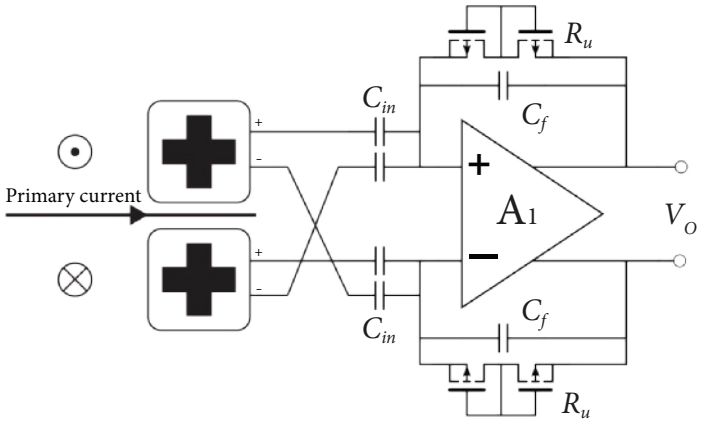

Figure 4.4 Capacitively coupled first stage with a differential sensor arrangement.

At the final output, the LF path only contributes signals ranging from DC to f_{cross} (2 kHz). With f_{spin} = 10 kHz, the Hall signal will be modulated to 20 kHz and so the 1st stage requires a flat frequency response from 18 kHz to 22 kHz, as shown in Figure 4.5. To assure maximum signal attenuation of less than 1% due to the high-pass filtering action, the feedback resistors need to be greater than 370 MΩ with C_f = 240 fF. Considering the output swing of the 1st stage is relatively low (<< 500mV), R_u is implemented as a pseudo resistor with two back-to-back connected PMOS transistors [3]. One of the PMOS transistors is operating in deep subthreshold region, while the other PMOS transistor is turned off with a parasitic diode between drain (P) and body (N) to conduct current. As a result, they can achieve a resistance of several GΩ in a small area as long as the voltage across the devices is well below the threshold voltage of the PMOS transistors.

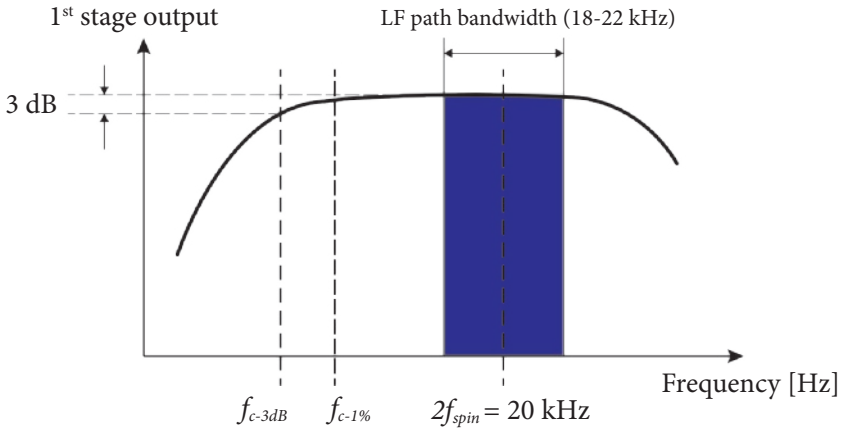

Figure 4.5 Frequency response of the 1st stage.

Since most of the Hall sensor offset will be blocked by the input capacitors, the 1st stage only needs to process the magnetic signal and the offset of the first opamp A_1. Therefore, the input stage of A_1 is implemented as a telescopic amplifier. The input differential pair transistors are biased in weak inversion at 55 µA, to achieve a g_m of 1.2 mS, which is commensurate with the Hall sensor resistance. To drive the load R_l = 50 kΩ (Figure 4.3), A_1 employs a class-A output stage with a biasing current of 20 µA. The common-mode voltage is sensed by M_0 and M_1 through their gate-source voltage V_{gs}, which controls a feedback current to stabilize the output common-mode level. Due to the fact that the common-mode feedback (CMFB) has only one gain stage, the stability and speed of the CMFB can be guaranteed.

The total current consumption of A_1 is 175 µA. Together with input and feedback capacitors of 24 pF and 240 fF, respectively, the 1st stage achieves a gain of 100 in a bandwidth of about 400 kHz, and an input referred noise of about 8 nV/√Hz.

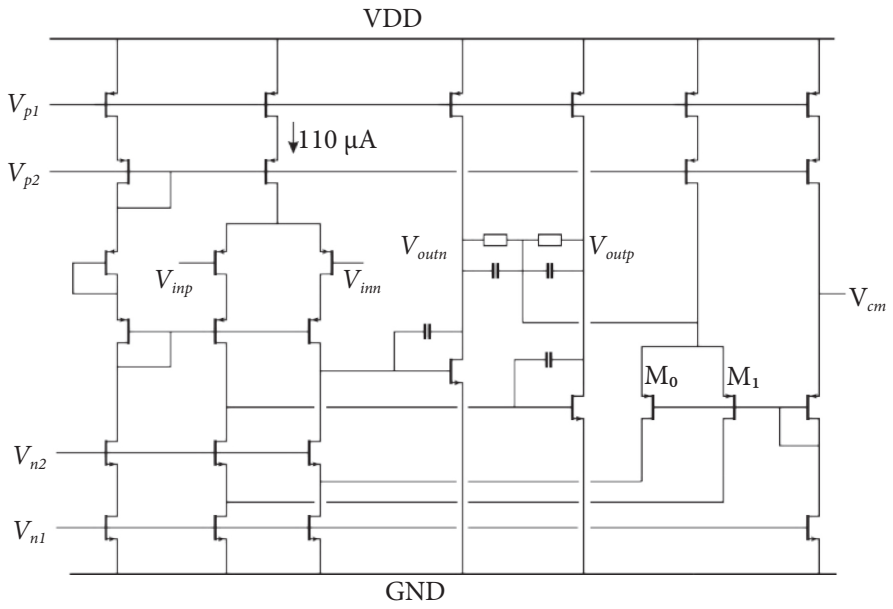

Figure 4.6 Circuit diagram of A_1.

The opamp A_2 is a scaled-down version of A_1, which consumes 75 µA. With an input resistor R_l = 50 kΩ and a feedback resistor R_2 = 1 MΩ, the 2nd stage achieves a gain of 20 in a bandwidth of about 400 kHz, and an input referred noise of about 50 nV/√Hz .

Implementation of Triple RRLs

Primarily due to the anisotropic resistance of the n-well and the JFET effect discussed in Chapter 2, the Hall sensor offset changes in different spinning phases. Together with the offset of the 1st and 2nd stages, it appears as a square-wave ripple at the output of the 2nd stage, which cannot be

fully filtered by the output stage. This ripple can be decomposed into three components, as shown in Figure 4.7, and compensated by the triple RRL scheme from Chapter 3. Two out of three RRLs are working in a ping (1st and 2nd phases) – pong (3rd and 4th phases) sequence to fully compensate any ripple at $2f_{spin}$. The residual ripple at f_{spin} will be compensated by the third RRL.

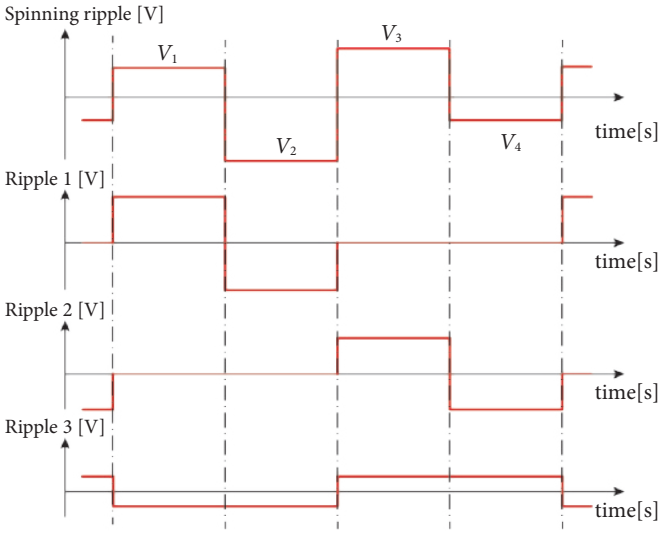

Figure 4.7 Decomposition of the spinning ripple into three orthogonal ripple components.

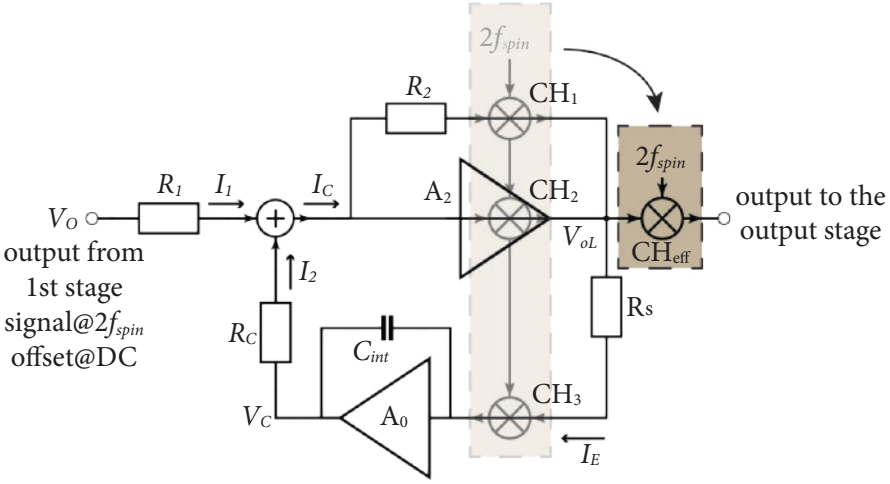

Figure 4.8 Implementation model of a single RRL.

In this design, the RRL implementation is adapted and modified from that in [2], as shown in Figure 4.8. The specific spinning ripple component is converted into current ripple by a resistor R_S. The resulting current is integrated into a capacitor C_{int} after synchronous demodulation. The compensation is done by injecting a current into the virtual ground of A_2 via R_C. For the sake of

parameter analysis, choppers CH_1, CH_2 and CH_3 can be combined to create CH_{eff}. This effectively converts the RRL into an active DC servo loop. Assuming A_2 is ideal, then V_{oL} can be expressed as:

$$V_{oL} = (I_1 - I_2)R_2 \tag{4.1}$$

In the feedback path, the transfer function from V_{oL} to V_C can be expressed as:

$$\frac{V_C}{V_{oL}} = \frac{A_0}{1+(1+A_0)sR_SC_{\text{int}}} \tag{4.2}$$

with which Equation (4.1) can be re-written as:

$$\left[\frac{V_{in}}{R_1} - \frac{A_0 V_{oL}}{[1+(1+A_0)sR_SC_{\text{int}}]\cdot R_C}\right]\cdot R_2 = V_{oL} \tag{4.3}$$

Therefore, the transfer function $H(s)$ from V_{in} to V_{oL} can be expressed as:

$$H(s) = \frac{V_{oL}}{V_{in}} = \frac{\frac{R_2}{R_1}}{1+\frac{A_0R_2}{R_C\left[1+(1+A_0)sR_SC_{\text{int}}\right]}} \tag{4.4}$$

Equation (4.4) can be mapped into the classical feedback theory, of which the corresponding Bode plot is shown in Figure 4.9. The loop gain $A\beta$ can be expressed as:

$$A\beta = \frac{A_0R_2}{R_C\left[1+(1+A_0)sR_SC_{\text{int}}\right]} \tag{4.5}$$

Based on Equation (4.5), the high pass corner frequency f_0 can be calculated by making $A\beta$ to 1:

$$f_0\big|_{A\beta=1} = \frac{R_2}{2\pi C_{\text{int}}R_SR_C} \tag{4.6}$$

Furthermore, the DC transfer function can be expressed as:

$$H(0) = \frac{R_C}{A_0\cdot R_1} \tag{4.7}$$

The action of chopper CH_{eff} will translate this high pass filter into a notch filter around the chopping frequency. In this design, R_1 = 50 kΩ, R_2 = 1 MΩ, R_S = 10 MΩ, C_{int} = 20 pF, R_C = 2.5 MΩ, and A_0 = 100 dB, which results in 66 dB of DC ripple reduction, and a notch width of $2f_0$ = 640 Hz.

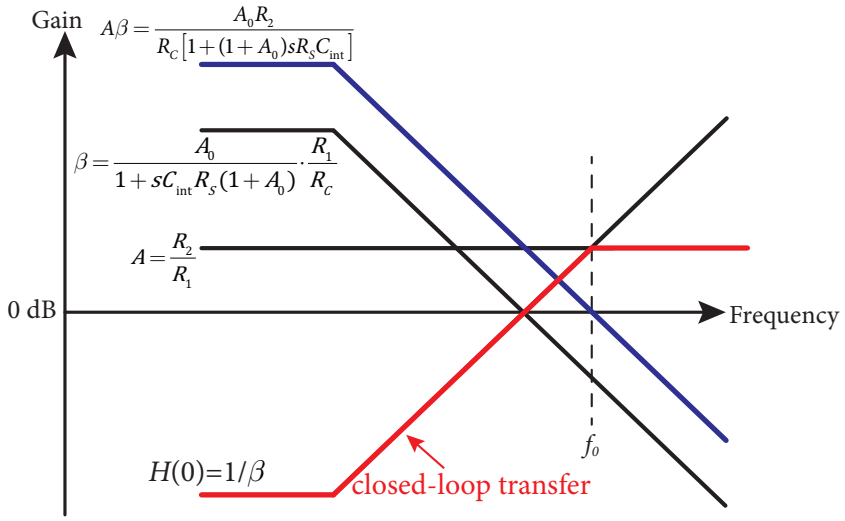

Figure 4.9 Bode plot of the DC servo loop used in the RRL.

The complete implementation of the triple RRLs is shown in Figure 4.10. As the residual ripple will be limited by the offset of A_0, all three integrators are auto-zeroed by storing their offsets on capacitor C_{az}. RRL1 and RRL2 are arranged in a ping-pong sequence: in Φ_1 RRL1 extracts the ripple associated with the 1st and 2nd phases, while RRL2 is in auto-zeroing mode; and in Φ_2, RRL1 is auto-zeroed, while the ripple associated with 3rd and 4th phases is extracted by RRL2. The residual ripple is extracted and compensated by RRL3, which is auto-zeroed once every spinning cycle. Since the integration period of RRL3 is twice as long as that of RRL1 and 2, its integration capacitor is doubled to keep the residual ripple at f_{spin} and $2f_{spin}$ comparable. To ensure a large voltage swing, all opamps A_0 in the integrators are based on a folded-cascode structure. This mitigates the non-idealities of the g_m stages that provide the feedback currents $(V_{os1} + V_{os3})/R_C$, $(V_{os1} - V_{os3})/R_C$, $(V_{os2} - V_{os3})/R_C$, and $(V_{os2} + V_{os3})/R_C$ in spinning phases 1-4, respectively.

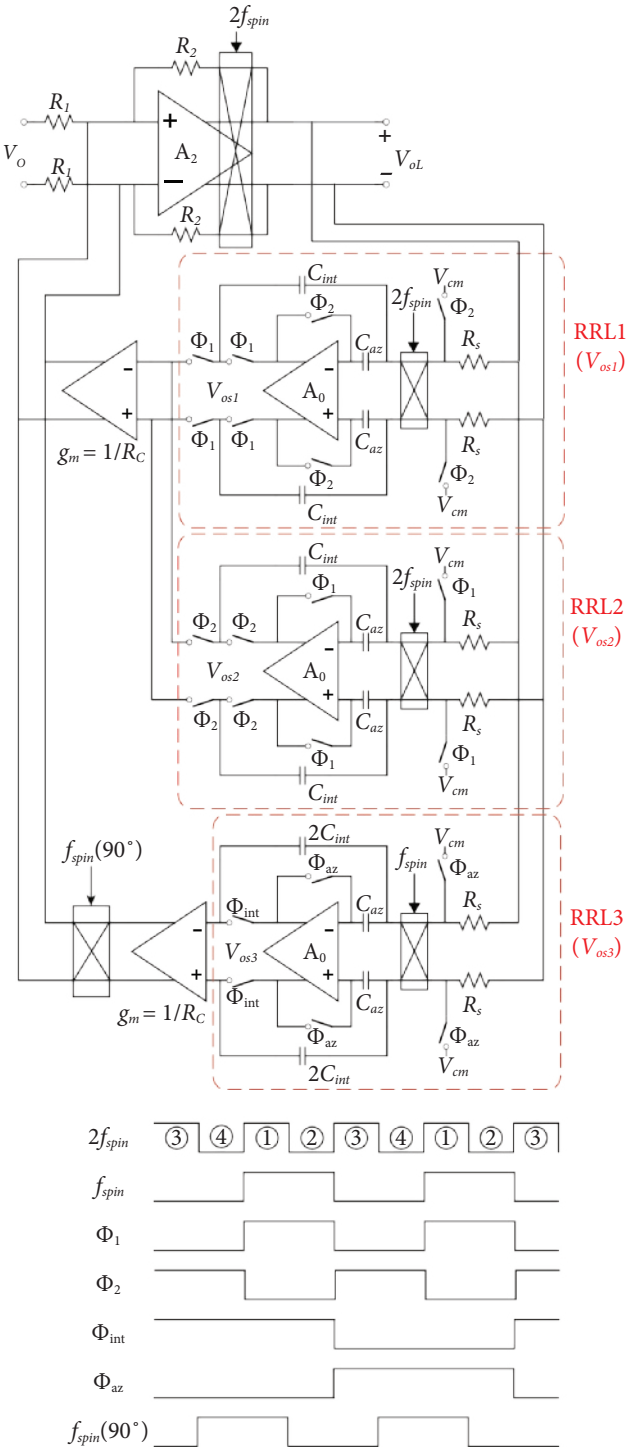

Figure 4.10 Detailed implementation of the triple RRLs.

In order to maximize the dynamic range of the system, the opamp A_3 used in the output stage is designed with a class-AB output, as shown in Figure 4.11. With a 5 V power supply and a combined Hall sensitivity of 100 mV/T (differential), the overall system is able to measure up to ± 12.5 mT.

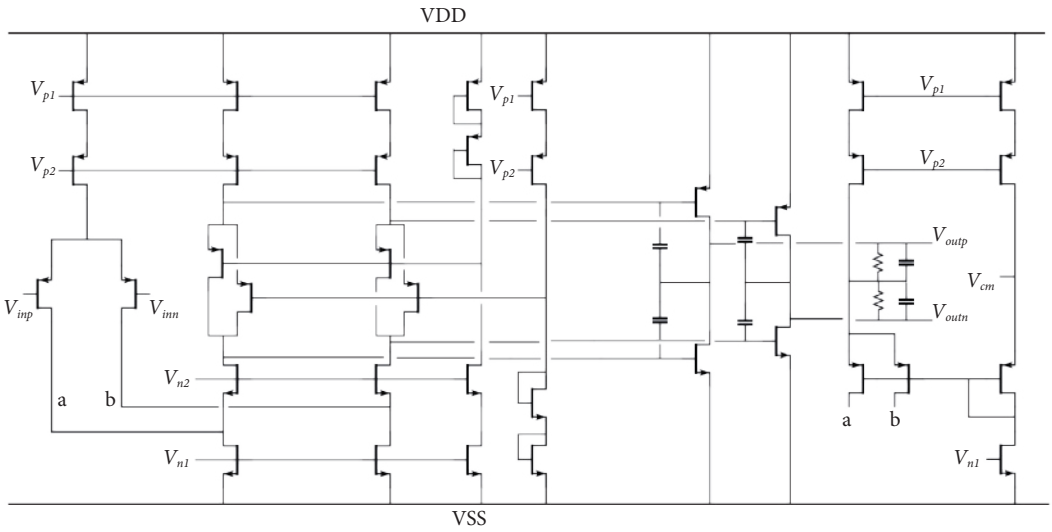

Figure 4.11 Circuit diagram of the opamp A_3.

4.3 Experimental Results

The proposed system is fabricated in a 0.18 μm CMOS process. The chip occupies a total area of 8.75 mm^2, as shown in Figure 4.12. In this implementation, each Hall sensor consists of four orthogonally coupled Hall plates, and each Hall plate is covered by a p+ layer to reduce 1/*f* noise by insulating the Si/SiO_2 interface. When biased with a total current of 1.4 mA (0.35 mA for each plate), the Hall sensors have a sensitivity of 50 mV/T. Therefore the overall system exhibits a differential sensitivity of 100 mV/T. Measurements on six samples show a maximum offset of less than 40 μT.

The chip is packed in a ceramic SOIC package, and mounted on top of a current-carrying PCB trace, such that its magnetic field could be differentially sensed, as shown in Figure 4.13. The use of a SOIC package can reduce the vertical distance between the current carrying PCB trace and the Hall sensors to about 1 mm, which results in an overall system sensitivity of about 0.08 V/A.

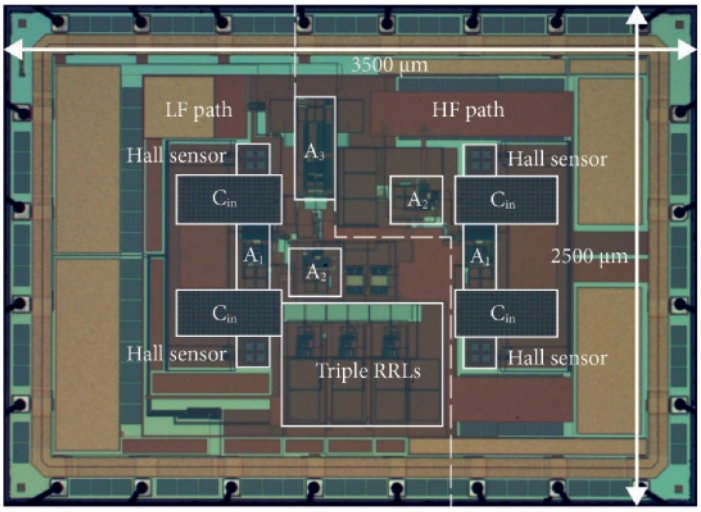

Figure 4.12 Micro photo of the chip.

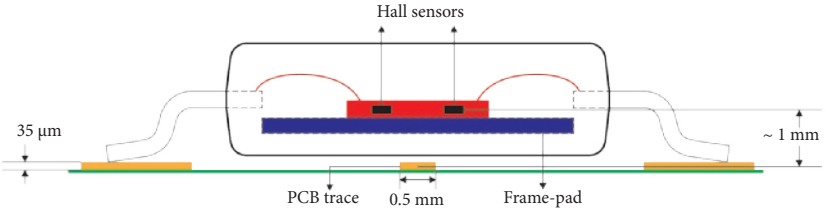

Figure 4.13 Cross-section of the chip packed in a SOIC package.

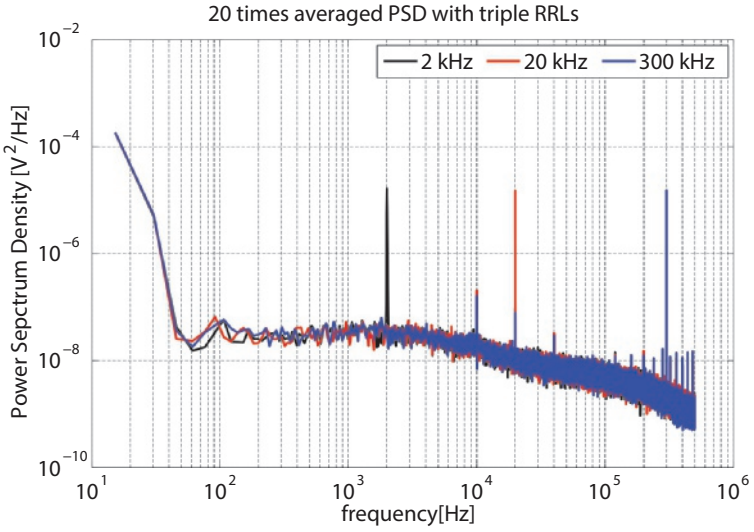

Figure 4.14 Output FFT of the overall system.

Figure 4.14 shows three FFT plots of the overall system with a 1 Ampere sinusoid primary current at different frequencies: the crossover frequency of 2 kHz, the ripple reduction frequency of 20 kHz ($2f_{spin}$), and a higher frequency of 300 kHz. The use of triple RRLs successfully suppresses the spinning ripple to 7.3 μT_{rms} (10 kHz ± 84 Hz), which is roughly equal to the noise of the sensor in a 300 Hz bandwidth, In this design, the residual ripple is ultimately limited by thermal noise and the bandwidth of the RRLs. Without the RRLs, this ripple can be as large as 1.1 mT.

The bandwidth of the overall system is measured with a spectrum analyzer, as shown in Figure 4.15. The system can cover a bandwidth of about 400 kHz without any notches. However, measurements show a gain reduction at frequencies higher than 50 kHz. This is caused by the effect of eddy currents within the lead frame pad inside the package which counterbalances the magnetic field produced by the primary current.

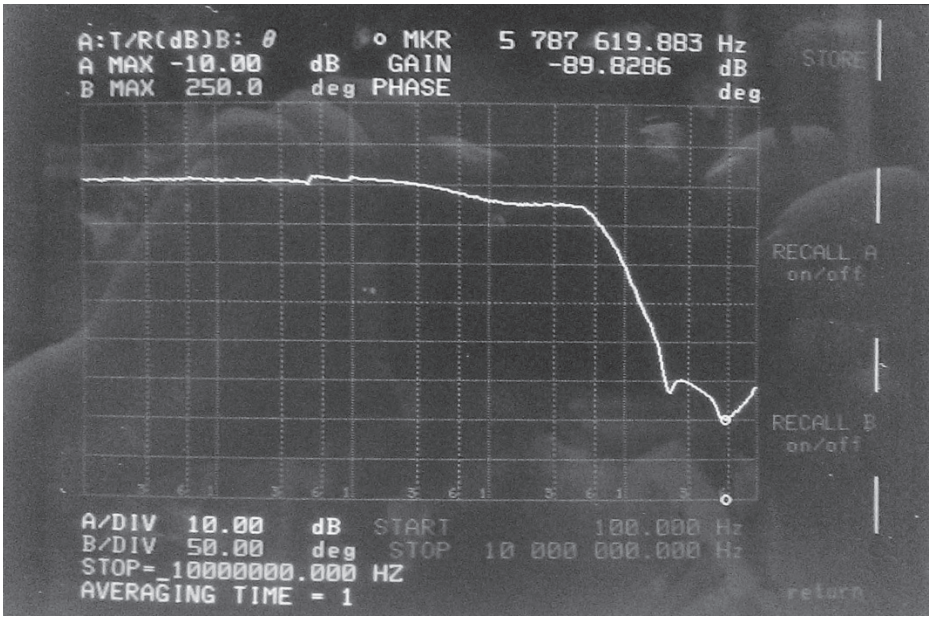

Figure 4.15 Bandwidth measurement result from a spectrum analyzer.

To verify the effect of eddy current, a simplified package model consisting of a primary current trace and a lead frame pad, as shown in Figure 4.16 and 4.17, is simulated in the finite element analysis (FEA) software Femm. With a DC primary current, the magnetic field distribution is nicely symmetrical forming a circle at the sensor spot, as shown in Figure 4.16. However, with an AC primary current, i.e. at 100 kHz, the eddy current effect substantially affects the magnetic field distribution, as shown in Figure 4.17. The magnetic field at the sensor spots is counterbalanced by the eddy current in the frame pad. This issue can be solved with a package which does not have a frame pad. However, such packages are usually not available in small quantities.

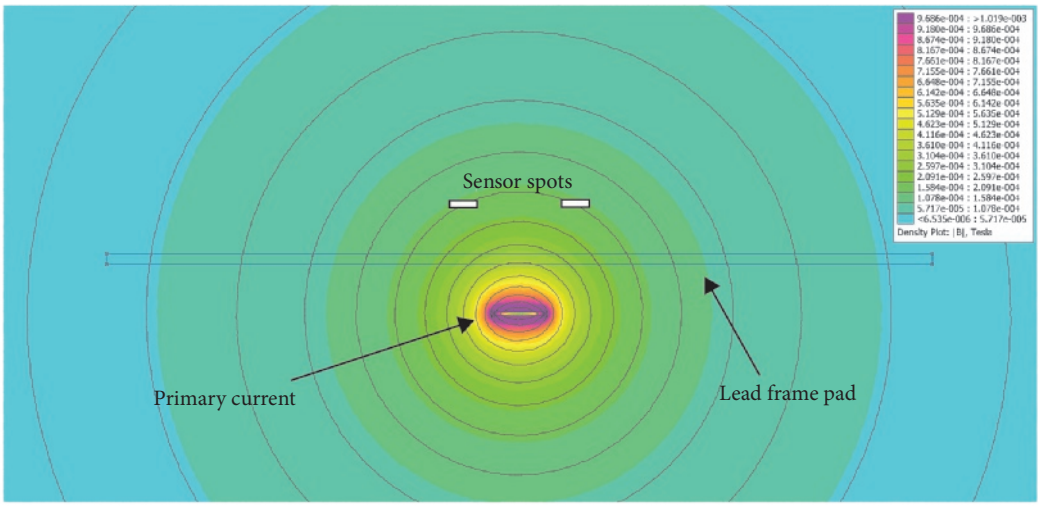

Figure 4.16 FEA simulation result of the magnetic field distribution of a DC primary current.

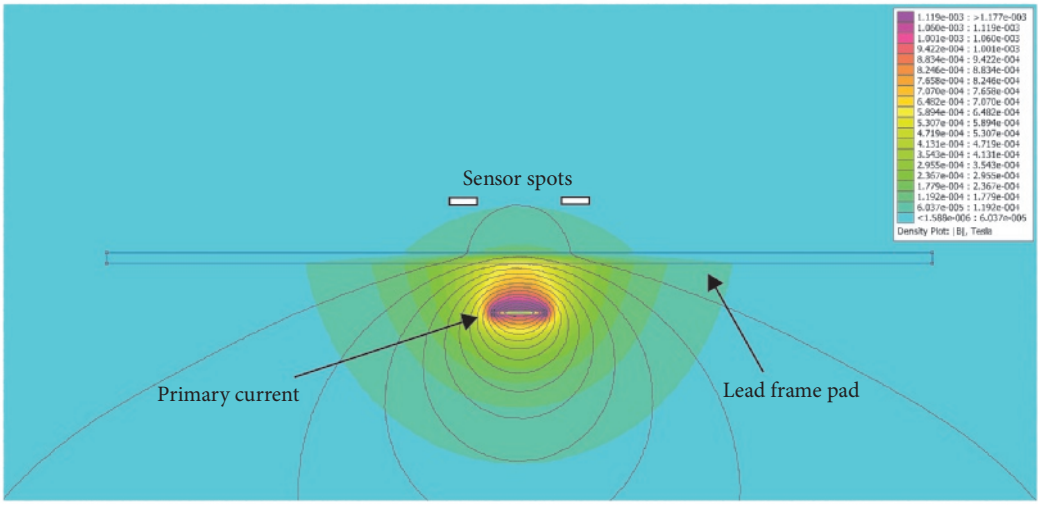

Figure 4.17 FEA simulation result of the magnetic field distribution of a 100 kHz primary current.

Table I compares this design to the other CMOS Hall sensors available at the time of publication (Nov. 2015). Compared to [4], this work achieves a comparable offset of 40 μT, yet with a bandwidth of 400 kHz, which is an improvement of 40x. The offset reported in [5] is even lower, although this was achieved with an eight-phase spinning technique at the expense of a significantly reduced bandwidth. Other wide bandwidth Hall sensors, as in [6], use rather high spinning frequencies, which results in an exponentially increased offset to 1800 μT. However, due to the presence of multiple Hall sensors, the current consumption of this work is inevitably higher.

Table 4.1 Comparison table with summarized performance.

Source	This work	[7]	[5]	[6]	[4]
Technology	0.18 µm	0.35 µm	0.5 µm	0.35 µm	0.35 µm
Maximum offset [µT]	40	10	3.65 (3σ)	1800	10
Area [mm^2]	8.75	5.7	N/A	9	6.5
Resolution [μT_{rms}]	274	0.6	0.33	200	N/A
Input range	±12.5 mT (diff)	±0.5 mT	±10.8 mT	500 mT	N/A
Bandwidth	400 kHz	100 Hz	5 Hz	100 kHz	10 kHz
Output	Analog	Digital	Digital	Analog	Digital
Supply current [mA]	8	5	4.2	N/A	N/A

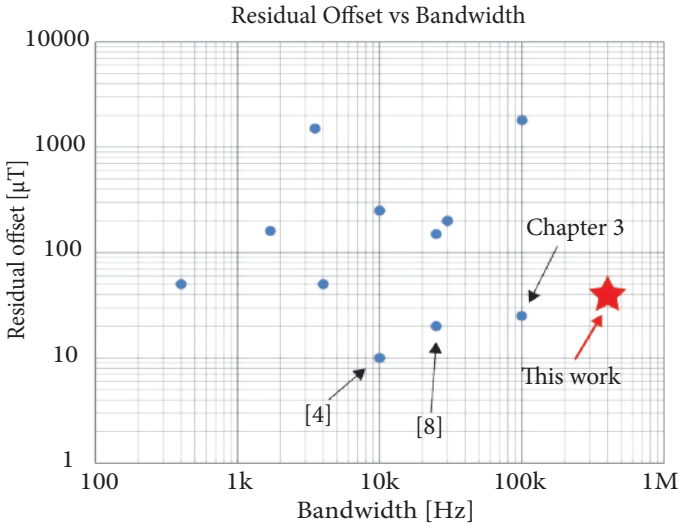

Figure 4.18 Benchmark plot of offset versus bandwidth (as of Nov. 2015).

Figure 4.18 depicts a benchmark plot which summarizes the offset and bandwidth performances of CMOS Hall sensors (as of Nov. 2015). Among all the sensors with a bandwidth greater than 100 Hz, the work in [4] stablishes the state-of-the-art offset-to-bandwidth ratio of Hall sensors in standard CMOS. This ratio is somewhat better in [8], which is achieved with the help of ferromagnetic material as a magnetic concentrator. The work described in Chapter 3 achieves similar offset and bandwidth, but exhibits frequency response notches due to the RRLs, which, moreover, are implemented with off-chip circuitry.

4.4 Conclusions

Throughout this chapter, a multi-path technique is proposed to realize wide-bandwidth, low-offset CMOS Hall sensor systems. A test chip utilizing the proposed technique and the triple RRLs (Chapter 3) is fabricated in a 0.18 μm CMOS process. It achieves an offset of 40 μT and a bandwidth of 400 kHz without any notches. This represents an improvement of 40x on the state-of-the-art.

The use of the multi-path technique and triple RRLs effectively breaks the bandwidth-offset design trade-off in conventional CMOS Hall sensor systems. Nevertheless, the increase in bandwidth is achieved at the expense of greater noise power and thus diminished resolution. Therefore, for a given resolution and power consumption, the maximum bandwidth of a CMOS Hall sensor is still limited. This limitation cannot be solved at the circuit level, and requires further work at a higher level, i.e. the system level. A solution for this issue will be discussed in the next chapter.

4.5 Bibliography

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A Hybrid Multi-Path Magnetic Sensor Combining Hall Sensors and Pick-up Coils

5

5.1 Introduction

Traditional Hall sensor systems can be designed to attain wide bandwidth and low offset by using a multi-path system structure, as discussed in Chapter 4. However, being essentially resistors, the noise power of Hall sensors increases linearly as the bandwidth extends to higher frequencies. For a certain SNR with finite power consumption, the bandwidth of a Hall sensor system is fundamentally limited by noise.

In contrast to Hall sensors, pick-up coils are sensitive to the time derivative of the magnetic field. Their maximum SNR actually increases with bandwidth. This differentiating characteristic makes them very suitable for high frequency AC measurement, while suffering from zero sensitivity at DC.

Theoretically, the combination of a bandwidth-limited Hall sensor and a pick-up coil should result in a system whose bandwidth can be extended without an SNR penalty. This concept has been demonstrated at the PCB level achieving a bandwidth of 30 MHz [1], but has never been built in a standard CMOS process.

This chapter will present a multi-path hybrid magnetic sensor in a 0.18 μm CMOS process which combines a set of Hall sensors and a set of pick-up coils. The rest of this chapter is organized as follows: Section 5.2 refreshes the SNR analysis of Hall sensors and pick-up coils with respect to their system bandwidths, derives the theoretical crossover frequency f_{cross} at which the system needs to switch from one sensor to the other, and finally introduces the basic crossover network. The detailed implementation of the system is then discussed in Section 5.3. The measurement results of the test chips are shown in Section 5.4. A refined noise analysis is given in Section 5.5, which takes the readout circuitry into account. Lastly, Section 5.6 will conclude this chapter.

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5.2 Combination of Hall Sensors and Pick-up Coils

As the sensitivity of linear sensors is frequency-independent, the maximum signal power produced by Hall sensors is independent of bandwidth. However, their thermal noise power increases linearly with bandwidth. For a given bandwidth f_{BW}, the noise n_{HS} [V_{rms}] of a Hall sensor can be expressed as:

$$n_{HS} = \sqrt{4kTR_{HS} \cdot f_{BW}} \tag{5.1}$$

where R_{HS} and S_{HS} represent the resistance and the sensitivity of the Hall sensor, respectively. The SNR of the sensor can be then expressed as:

$$SNR_{HS} = \frac{(B_{RMS} \cdot S_{HS})^2}{4kTR_{HS} \cdot f_{BW}} \tag{5.2}$$

where B_{RMS} represents the root mean square (RMS) of the magnetic field signal. Equation (5.2) suggests a decreasing SNR with a slope of -10 dB/dec, as shown in Figure 5.1.

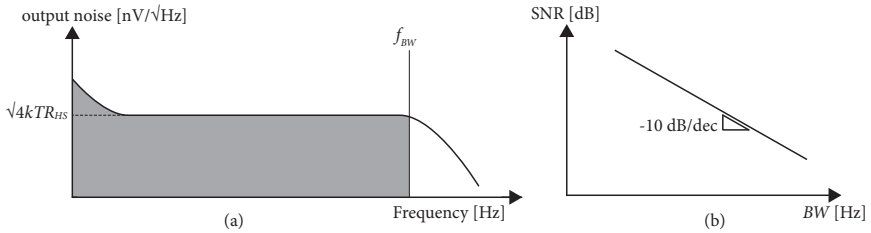

Figure 5.1 (a) Output noise of a Hall sensor, and (b) decreasing SNR with a slope of -10 dB/dec.

Conversely, pick-up coils have a frequency-dependent sensitivity which makes the noise analysis slightly different. Assuming a magnetic signal B_{RMS} at the bandwidth boundary of the system f_{BW}, the time domain magnetic signal can be then expressed as:

$$B = \sqrt{2} \cdot B_{RMS} \sin\left(2\pi f_{BW} \cdot t\right) \tag{5.3}$$

A pick-up coil will then generate a voltage output signal:

$$V_{coil} = n \cdot A \cdot \sqrt{2} \cdot B_{RMS} \cdot 2\pi f_{BW} \cdot \cos(2\pi f_{BW} \cdot t) \tag{5.4}$$

where n and A represent the number and area of the coil windings. Similar to that of a Hall sensor, the noise n_{coil} [V_{rms}] of a pick-up coil can be expressed as:

$$n_{coil} = \sqrt{4kTR_{coil} \cdot f_{BW}} \tag{5.5}$$

Equation (5.4) and (5.5) indicate that doubling the bandwidth of a pick-up coil will double its noise power (10 dB/dec), and quadruple its peak signal power (20 dB/dec). This suggests that the peak SNR of a pick-up coil, expressed as Equation (5.6) and plotted in Figure 5.2, will increase by 3 dB for every doubling of the bandwidth (10 dB/dec).

$$SNR_{coil} = \frac{B_{RMS}^2 \cdot (nA)^2 \cdot 4\pi^2 \cdot f_{BW}^2}{4kTR_{coil} \cdot f_{BW}} \tag{5.6}$$

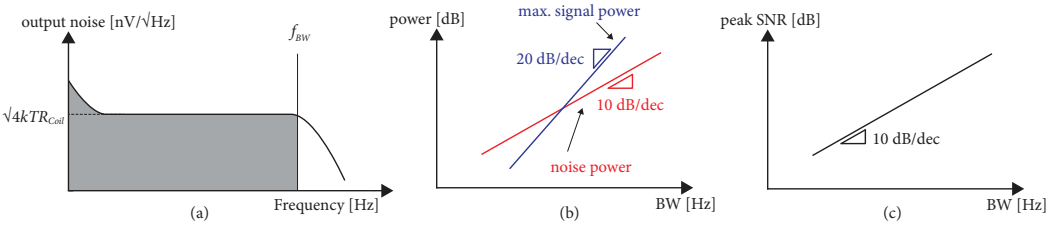

Figure 5.2 (a) Output noise of a pick-up coil, (b) the increasing noise power with a slope of 10 dB/dec and the increasing signal power with a slope of 20 dB/dec, and (c) the increasing peak SNR with a slope of 10 dB/dec.

Considering the fact that the SNRs of Hall sensors and pick-up coils exhibit opposite trends, one can conclude that at certain a frequency the SNRs of the Hall sensor and the pick-up coil will cross each other. This frequency is defined as the optimal crossover frequency f_{cross}, at which a system should switch from one sensor to the other for the sake of the SNR, as shown in Figure 5.3.

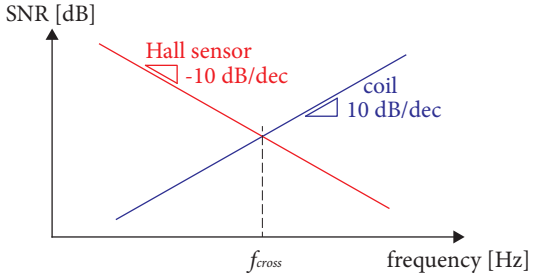

Figure 5.3 SNR plot of a Hall sensor and a pick-up coil.

For a given Hall sensor and a coil, the exact f_{cross} can be calculated by making Equation (5.2) and Equation (5.6) equal:

$$f_{cross} = \frac{S_{HS}}{2\pi nA}\sqrt{\frac{R_{coil}}{R_{HS}}} \tag{5.7}$$

It is worthwhile to point out that the f_{cross} defined in Equation (5.7) is also the frequency at which the input referred noise densities [T/√Hz] of the Hall sensor and coil are equal, as shown in Figure 5.4.

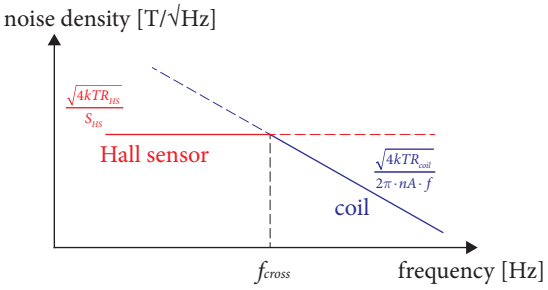

Figure 5.4 Input referred noise of a Hall sensor and a pick-up coil in relation to the crossover frequency f_{cross}.

In the case of an abrupt switching at optimal f_{cross} between the two sensors, the optimal resolution (in Tesla) of the overall system can be already calculated as:

$$n_{B\_overall} = \frac{n_{HS}}{S_{HS}} \cdot \sqrt{\frac{\pi}{2} f_{cross}} = \sqrt{\frac{kT\sqrt{R_{HS} \cdot R_{coil}}}{nA \cdot S_{HS}}} \tag{5.8}$$

An important conclusion can be drawn from Equation (5.8). The optimal resolution of the overall system with Hall sensors and pick-up coils is bandwidth-independent, and relies only on the sensor parameters.

However, the derivation of the optimal f_{cross} assumes that one of the sensors will be shut down at any given time, and therefore will not contribute any signal or noise. This is, however, impractical as in general a magnetic signal will usually consist of multiple frequency components spread over the spectrum. In a practical system, a crossover network ensuring smooth frequency transition is crucial. However, a crossover network will inevitably introduce extra noise, therefore the end results may differ from the optimality expressed in Equations (5.1 - 5.8). A refined noise model which takes the readout circuitry into account will be discussed in Section 5.5 with the measurement results of an implemented system.

Figure 5.5 depicts the proposed crossover network to ensure smooth frequency transition. The Hall sensor in the low frequency (LF) path and the pick-up coil in the high frequency (HF) path are read out by g_{m_HS} and g_{m_coil}, respectively, and then combined by a trans-impedance amplifier with a time constant of *RC*. The low-pass filtering action of the trans-impedance amplifier also limits the noise bandwidth of both Hall sensors and coils, so that both wide bandwidth and high resolution can be achieved. In addition, the proposed crossover network ensures that the crossover frequencies seen by both paths are always identical, even if *R* and *C* spread or drift.

However, the sensitivities of both paths still need to be adjusted to match each other. This can be done by adjusting the biasing current of the Hall sensor.

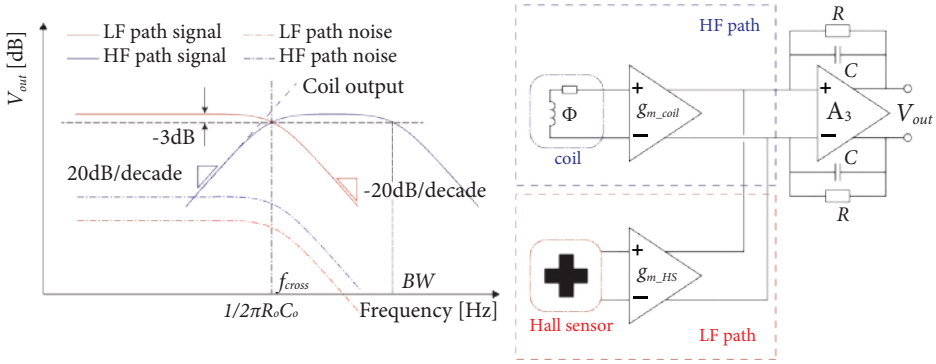

Figure 5.5 Proposed crossover network, which ensures smooth frequency transition.

To demonstrate this theory in a complete system, consider an on-chip realization in which two Hall sensors with S_{HS} = 50 mV/T and $R_{HS} \approx 1$ kΩ, and a pick-up coil with n = 32, $A \approx 1$ mm^2 and R_{coil} = 20 kΩ are used as transducers. These result in an optimal $f_{cross} \approx 1.57$ kHz, which is intentionally set to 2 kHz to accommodate extra readout noise and to save chip area. To balance the chip area occupied by the RC time constant, R = 4 MΩ and C = 20 pF are used in the implementation. g_{m_coil} and g_{m_HS} are then set to 0.25 mS and 1 mS to match the sensitivities of the HF and LF paths, respectively. Based on the simplified noise analysis in Equation (5.8), the Hall sensors and pick-up coil should only produce a noise of 6.3 μT_{rms} (differential). This is, nonetheless, not accurate considering the fact that the proposed crossover network outputs contain thermal noise of both the LF and the HF paths. Taking this into account, the sensors will have an input referred noise of 8.1 μT_{rms} (differential). However, this result still underestimates the readout noise, which, as later shown in experimental results, dominates the system performance in this implementation.

5.3 System Implementation

Due to the presence of the 1st order frequency transition, the bandwidth of the LF path needs to be substantially higher than f_{cross} to prevent any overall gain reduction around the LF path bandwidth. For instance, to ensure a gain flatness of 0.1 dB (~1%), the LF path bandwidth needs to be 100 times higher than f_{cross}, namely 200 kHz, as shown in Figure 5.6.

The implementation of the LF path is shown in Figure 5.7. It employs spinning current Hall sensors and triple RRLs to ensure low offset. This approach guarantees enough bandwidth to ensure a flat frequency response at overall outputs. In order to sufficiently fill up the notches associated with the triple RRLs, the spinning frequency f_{spin} needs to be sufficiently higher than f_{cross}, e.g. 10 kHz.

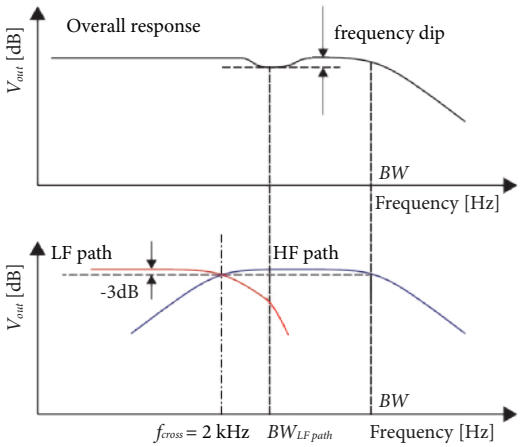

Figure 5.6 Influence of LF path bandwidth on the overall frequency response.

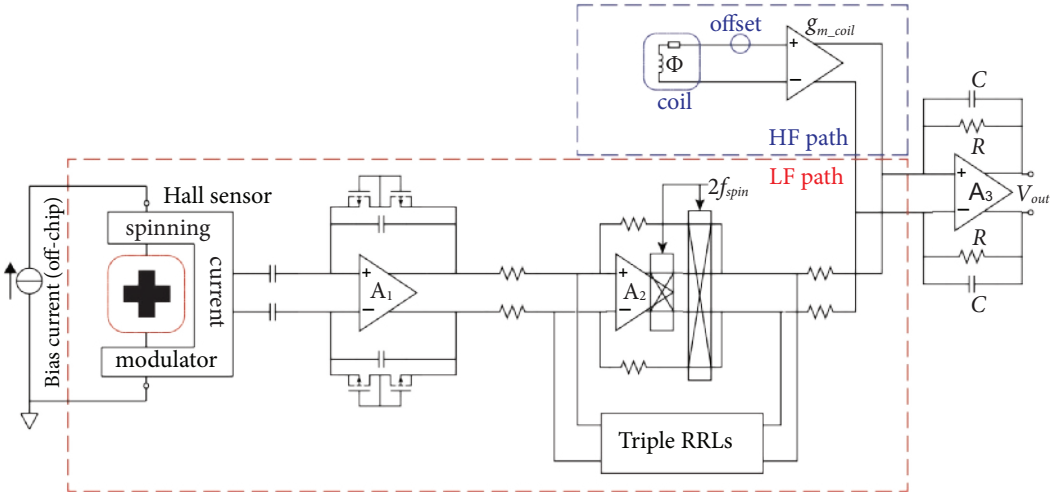

Figure 5.7 Detailed implementation of the low frequency (LF) path.

Since the LF path implementation is exactly the same as the LF path in the multi-path Hall sensor system discussed in Chapter 4, similar low frequency accuracy is expected, i.e. a 40 μT offset, which is equivalent to an output referred offset of only 16 mV.

HF Path Implementation

Due to the nature of the proposed crossover network, the HF path also contributes offset to the final output due to the presence of a DC signal path of $g_{m\_coil} \cdot R$. To preserve the offset performance from the LF path, the offset of g_{m_coil} needs to be lower than 16 μV, which is quite challenging.

Using dynamic offset cancellation techniques such as chopping and auto-zeroing can achieve that level of offset. However in view of the megahertz level bandwidth, an even higher chopping frequency or auto-zeroing frequency is required, which makes the offset reduction efficiency offered by these techniques quite low due to charge injections. Using a lower chopping frequency inside the signal bandwidth can achieve a better offset reduction, although this inevitably introduces extra chopping ripple inside the signal band. An extra ripple reduction loop can suppress the ripple, and any signal at the chopping frequency as well, leaving an uncompensated notch in the frequency response. Reducing the auto-zeroing frequency will break the continuous-time operation of the system, and introduce signal and noise aliasing issues.

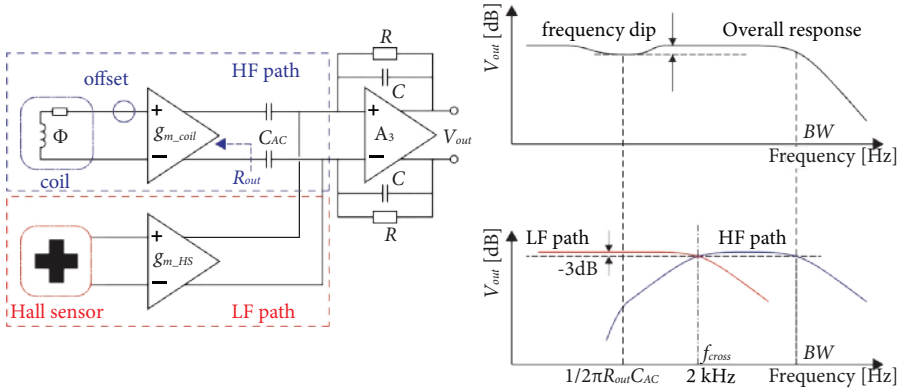

Figure 5.8 High frequency path with AC coupling to block the offset of g_{m_coil}.

To tackle the offset of g_{m_coil}, a set of capacitors C_{AC} are inserted between g_{m_coil} and the output stage, which block the offset current and pass through the AC signals, as shown in Figure 5.8. The output impedance of g_{m_coil} and C_{AC} effectively creates a pole at low frequencies, which can potentially affect the overall frequency response. Similar to the LF bandwidth, to ensure a gain flatness of 0.1 dB (0.1%), this pole needs to be 100x lower than f_{cross} = 2 kHz, namely 20 Hz. With a reasonably sized C_{AC}, i.e. 20 pF, R_{out} needs to be as large as 400 MΩ.

g_{m_coil} Implementation

Figure 5.9 shows a circuit diagram of a traditional g_m stage. The sources of the input pair are degenerated by a resistor to maximize the linear input range. Currents I_{left} and I_{right} are amplified by current mirrors by a factor of 10 to generate the actual outputs. The output impedance of the stage is limited since the drain current of MN2 is dependent on its drain voltage V_d. This effect can be suppressed by using a cascode transistor MN3 to stabilize V_d, which makes the drain current of MN2 less dependent on the output swing, thus boosting the output impedance. However, the gate-source voltage V_{gs} of MN3 is also a function of the drain current of MN2. With a fixed gate voltage V_{bias} of MN3, the swing of V_d cannot be completely suppressed, leading to limited output impedance.

To further improve the output impedance, gain boosting can be used to further minimize the voltage swing of V_d, as shown in Figure 5.10. The voltage swing of V_d is sensed by the gain boosting transistor MN4, the drain of which regulates the gate of MN3 to ensure that V_d becomes signal-independent. In small signal applications where V_g does not swing much, the improvement of the output impedance depends on the gain of MN4. Further improvement can be achieved by replacing MN4 with a high gain opamp. However from a system point of view, the g_m stage in an open loop configuration needs to accommodate a larger swing of V_g and accurately mirror the current signal from MN1 to MN2. With large dynamics, the drain voltages of MN1 V_g and MN2 V_d will be different. This makes the accuracy of the current mirror signal-dependent, leading to gain errors at the output branch.

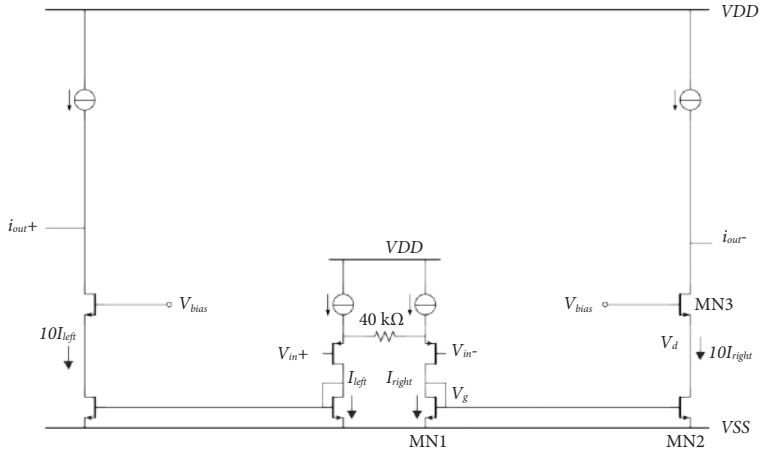

Figure 5.9 Traditional g_m implementation with source degeneration and output cascode.

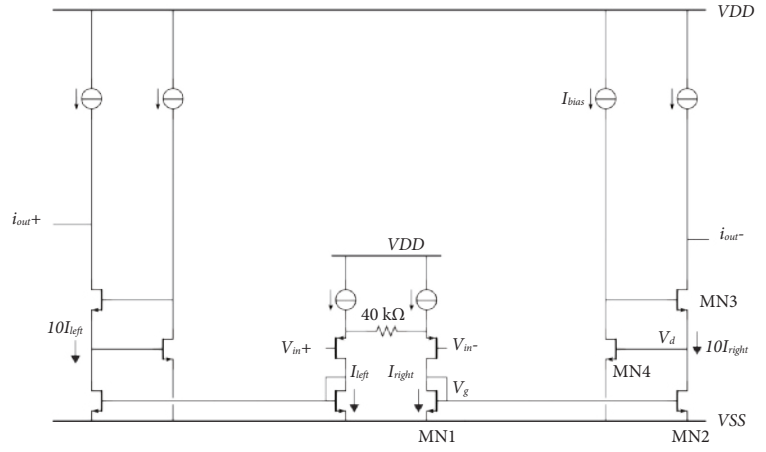

Figure 5.10 Implementation of g_{m_coil} with gain boosting to improve output impedance.

A further improvement can be achieved by replacing the DC biasing current of MN4 with a replica of I_{right}, as shown in Figure 5.11. Since the drain current of MN4 is a replica of the drain current of MN1, the gate voltage of MN4 V_d will track the swing of V_g, which guarantees the matching of the drain voltages of MN1 and MN2. With identical biasing voltages for the gate, source and drain, the drain currents of MN1 and MN2 become identical, producing high output impedance at final outputs. However, due to limited current mirror accuracy between MN1 and MN5, a small signal-dependent error is expected between V_g and V_d, which can be tackled by adding MN6 and MN7 to accurately regulate the drain voltage of MN5.

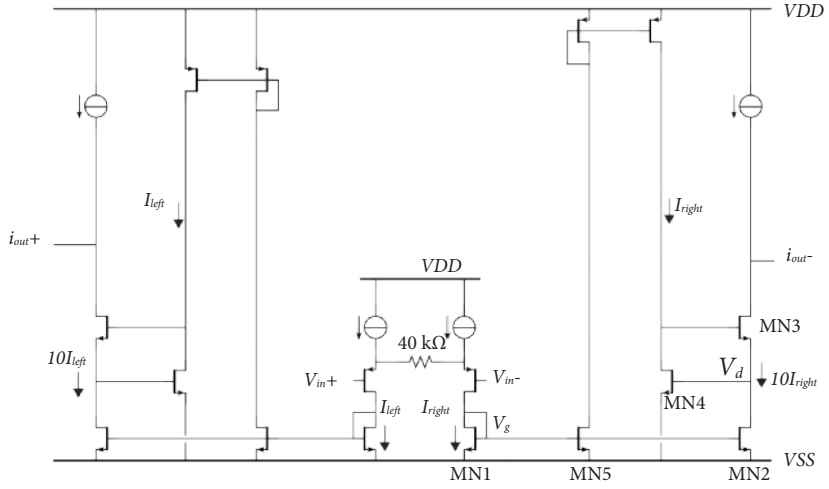

Figure 5.11 Implementation of g_{m_coil} with adaptive gain boosting.

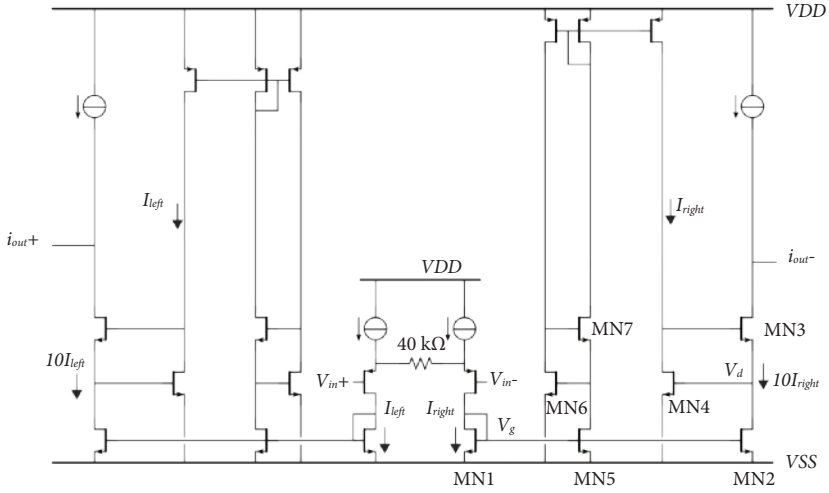

Figure 5.12 Implementation of g_{m_coil} with enhanced adaptive gain boosting.

With a transconductance of 0.25 mS, g_{m_coil} needs to produce a 250 µA output current in response to a 1 V signal at V_{in}. Therefore the current sources at the output branches need to be significantly larger than 250 µA. To minimize unnecessary current consumption, the current sources are replaced with the differential current signal to form a push-pull output stage [2], as shown in Figure 5.12. For the same transconductance, the current mirror ratio can be now reduced from 10 to 5, which saves chip area. The output common-mode voltage is controlled by injecting correction currents (MP1 and MP2) into the output branches before the cascode transistors.

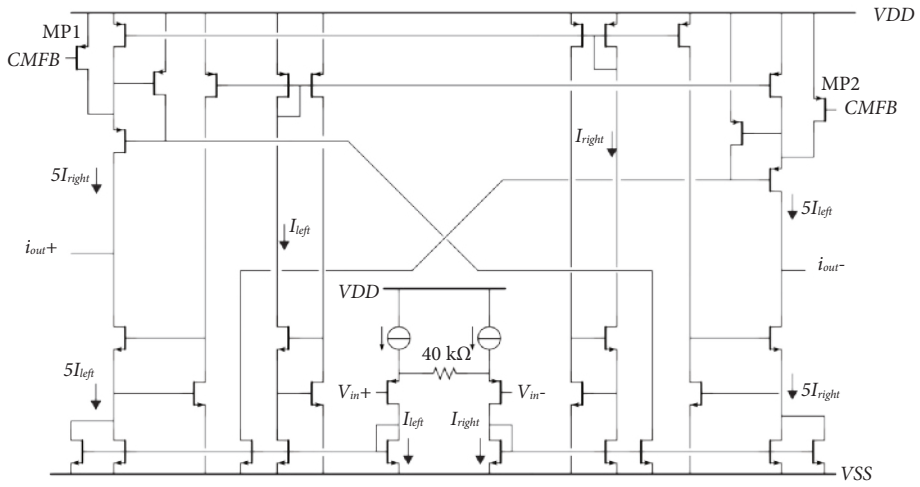

Figure 5.13 Implementation of g_{m_coil} with enhanced adaptive gain boosting and push-pull outputs.

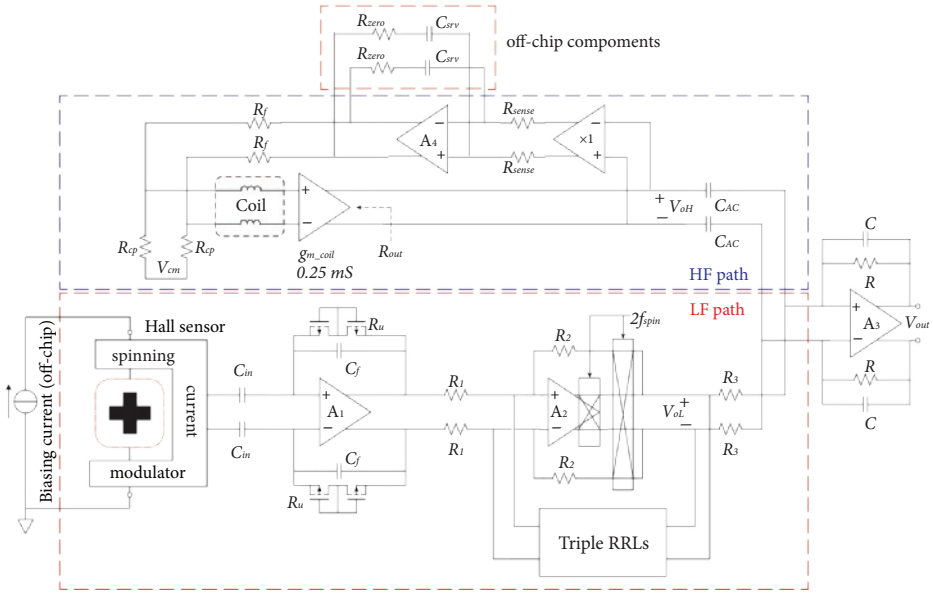

Figure 5.14 Complete implementation of the hybrid magnetic sensor system.

It is important to point out that this implementation of g_{m_coil} is not optimized for noise. It overlooks the fact that all current mirrors used in this circuit will generate significant amount of extra noise in addition to the current noise of the 40 kΩ degeneration resistor. The noise performance of the entire system is dominated by this stage.

HF Path DC Servo Loop and Output Stage

With a large output impedance (about 2 GΩ in simulation over PVT), a tiny offset of a few μV can clip the outputs of g_{m_coil} (V_{oH}). To regulate the DC output of g_{m_coil}, a DC servo loop is built around g_{m_coil}, as shown in Figure 5.14. To preserve the output impedance, V_{oH} is first buffered by a pair of source followers, then converted into current via resistor R_{sense} (5 MΩ) and integrated into C_{srv} (10 μF). Due to the presence of two poles $R_{sense}C_{srv}/A_4$ and $R_{out}C_{AC}$, a zero is created by inserting R_{zero} (2 kΩ) in series with C_{srv} to ensure that the effect of the non-dominant pole $R_{out}C_{AC}$ is cancelled. The compensation voltage is generated by the resistive voltage divider at the convergence of the pick-up coils.

To accurately handle the large output current from g_{m_coil} at high frequencies, i.e. ±100 μA at 2 MHz, and to maximize the output range, the output stage is implemented with a class-AB output stage. The circuit diagram is shown in Figure 5.15.

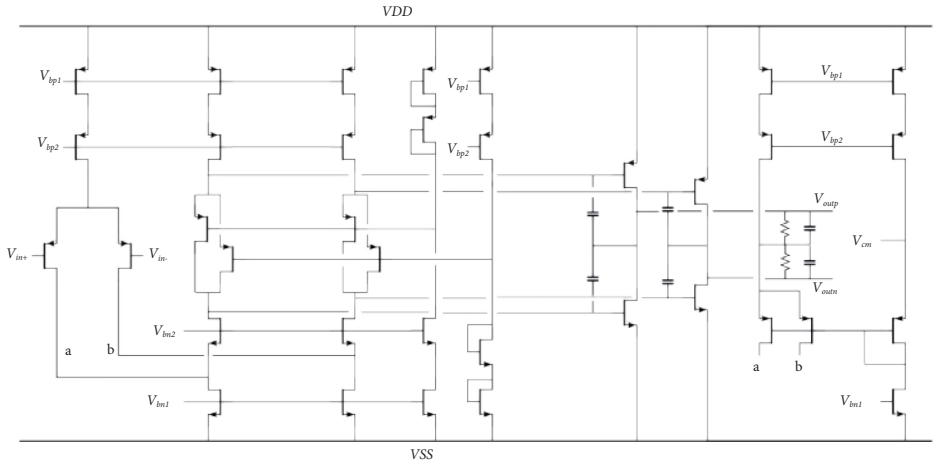

Figure 5.15 Circuit diagram of the output stage with a class-AB output.

5.4 Experimental Results

The proposed hybrid wide-bandwidth current sensor is fabricated in a standard 0.18 μm CMOS process, occupying a total area of 8.75 mm^2, as shown in Figure 5.16. Similar to the system discussed in Chapter 4, each Hall sensor consists of four orthogonally coupled Hall plates; each Hall plate is covered by a p+ layer to reduce 1/*f* noise by isolating the Si/SiO_2 interface. The

biasing current of the Hall sensors is adjusted to 2 mA (0.5 mA for each plate), resulting in a sensitivity of 71.4 mV/T (142.8 mV/T differential sensitivity) to match that of the pick-up coils. Measurement on four samples shows a maximum offset of less than 40 µT.

To minimize the parasitic capacitance and thus the crosstalk between the pick-up coils and readouts, the pick-up coils are moved away from the readout circuitry, and are shielded by two metal plates connected to ground.

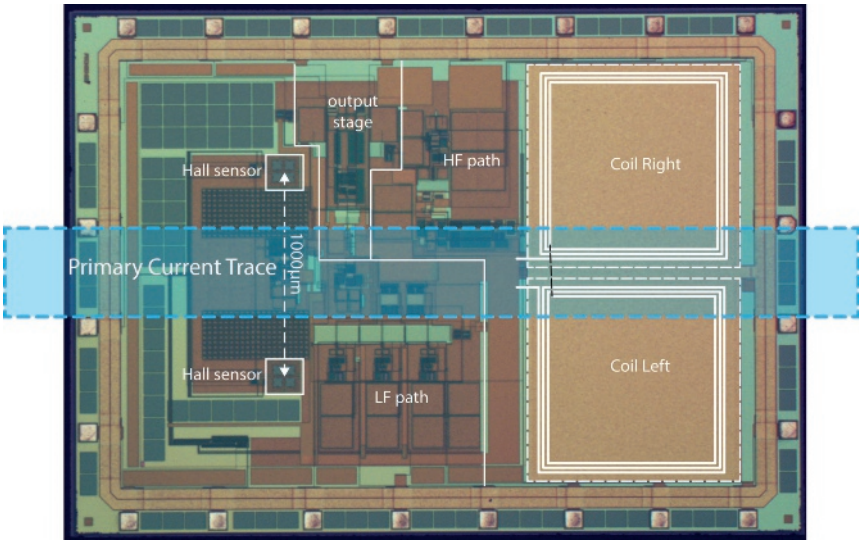

Figure 5.16 Die photo of the hybrid wide-bandwidth current sensor.

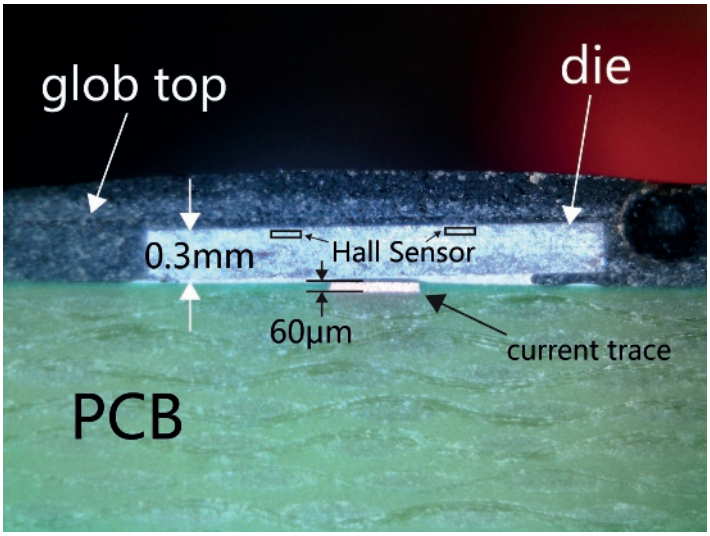

Figure 5.17 Cross-section of a CoB sample.

To prevent eddy current from distorting the high frequency response, as discussed in Chapter 4, the chip is glued directly on top of a PCB current trace using the chip-on-board (CoB) technique, with the added benefit of a small distance between the primary current and the sensors. The cross-section of a CoB sample is shown in Figure 5.17. The resulting primary current-to-magnetic field transfer is about 0.43 mT/A.

To verify the noise performance of the overall system, the outputs are sampled by a 16-bit ADC at 2 MS/s. Figure 5.18 shows the FFT result of the sampled results with a single tone signal at 199 kHz. Thanks to the 1st order low-pass filtering action of the output stage, the noise spectrum density starts to roll off at -20 dB/dec from f_{cross} = 2 kHz, resulting in a total integrated noise of 210 μT_{rms}. This result however does not agree with the noise model predicted by Equation (5.8). This difference is due to the extra noise of readout circuitry as well as the pick-up coils below f_{cross}. These extra noise sources will be analyzed in further detail in the next section.

The residual ripple is suppressed to about 8 μT_{rms} (at 10 kHz) thanks to the RRLs in the LF path as discussed in Chapter 4. Due to the limited linearity of g_{m_coil} in an open loop structure, the 2nd order harmonic is visible at 398 kHz, with an amplitude of about -40 dB with respect to the main signal amplitude, limiting the overall system linearity to about 1%.

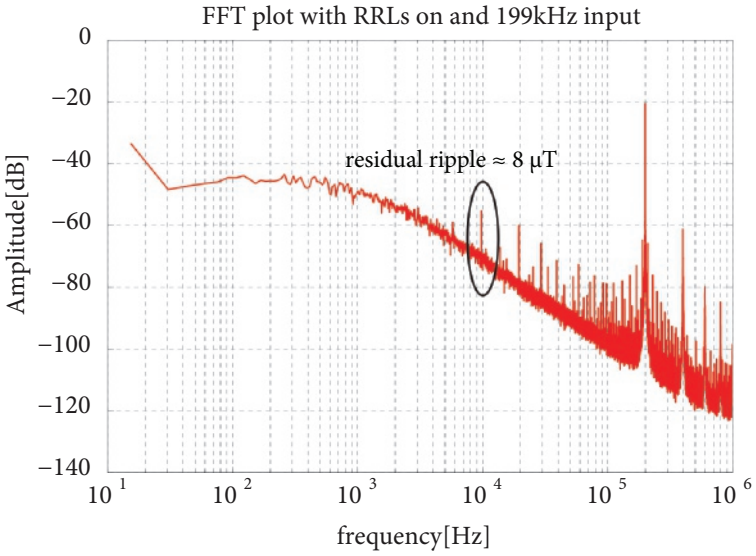

Figure 5.18 FFT plot of the overall system with a single tone input at 199 kHz.

With the help of a spectrum analyzer, the bandwidth of the system is verified from 10 Hz to 100 MHz, as shown in Figure 5.19. With only the LF path active, the system bandwidth is limited to f_{cross} = 2kHz by the *RC* time constant in the feedback of the output stage. Two notches at 10 kHz and 20 kHz can be clearly observed. With both paths active, the -3 dB bandwidth is extended to 3 MHz, after which the system rolls off in a 2nd order fashion, with a slope of -40 dB/dec resulting

from the bandwidth of both g_{m_coil} and the output stage. The notches in the LF path are also filled up by the HF path signal, ensuring a flat frequency response over the entire bandwidth.

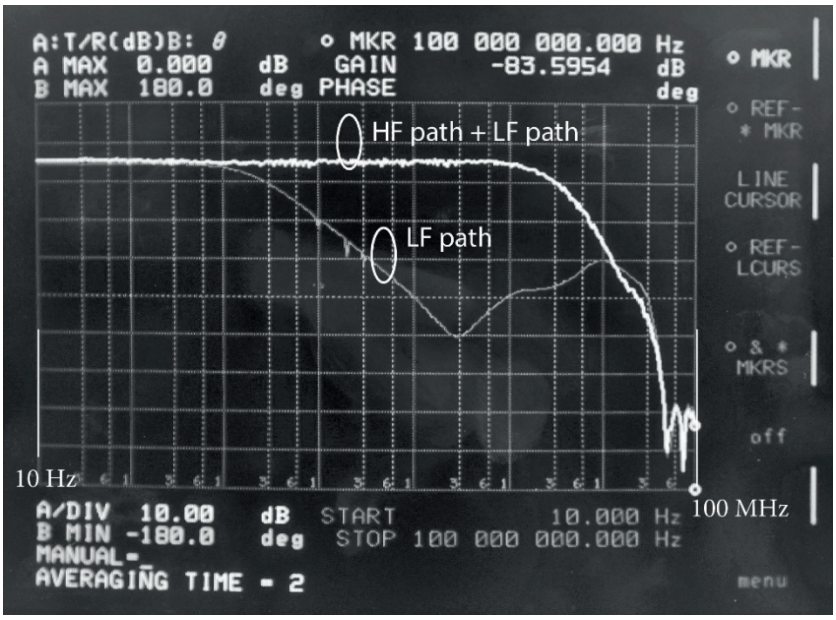

Figure 5.19 Amplitude versus frequency response with only the LF path active and with both the LF and HF paths active.

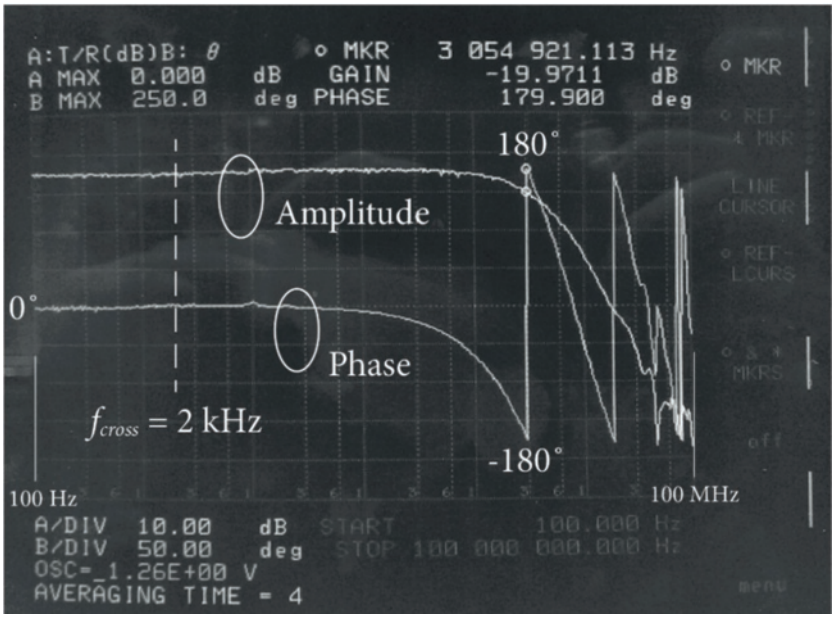

Figure 5.20 Amplitude and phase versus frequency responses of the complete system.

To further explore the performance of the proposed sensor structure, the phase response from 100 Hz to 100 MHz is also verified, as shown in Figure 5.20. A flat phase response of 0˚ is obtained over the entire bandwidth. At high frequencies (>1 MHz), the rolling off of the phase response is due the fact that the proposed system is a 2nd order system.

The achieved system bandwidth can also be demonstrated by examining its step response, as shown in Figure 5.21. The test is done with a 3.3 A_{pp} square-wave primary current at 100 kHz. The settling of both the rising and falling edges is quite symmetrical, with a settling (>90%) time of less than 400 ns.

The system is theoretically capable of measuring a low frequency (<2 kHz) current up to ±18 A (±7.8 mT), which causes the output to clip to the 5 V supply rail. The maximum detectable slew rate is 314 A/μs (135 mT/μs), which is equivalent to about ±12A_{rms} at 3 MHz. Further increasing in slew rate will cause g_{m_coil} to clip.

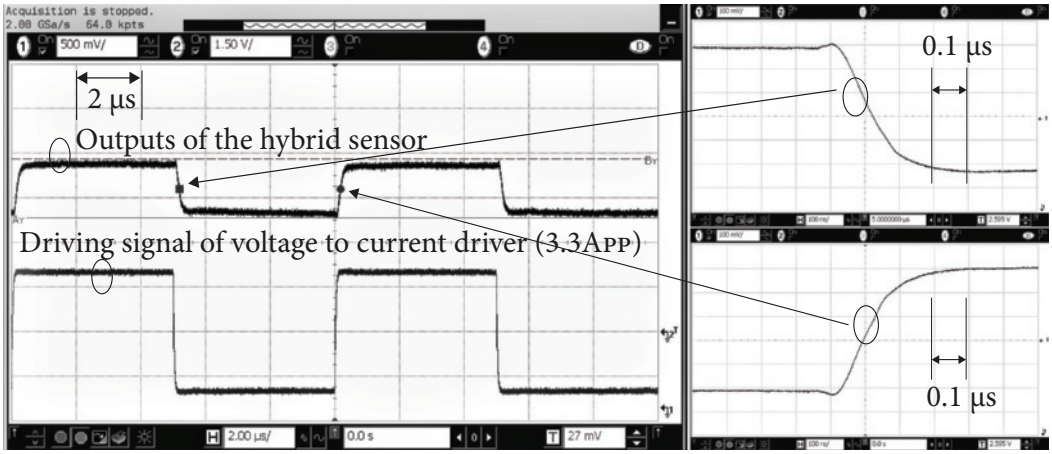

Figure 5.21 Step response of the overall system.

The performance of the proposed hybrid sensor system is summarized in Table 5.1 with other state-of-the-art magnetic sensors. Compared to the system discussed in Chapter 4, the bandwidth is further improved by another order of magnitude with an even slightly better resolution at a similar supply current. The offset achieved in this work is compatible to other low offset CMOS magnetic Hall sensors [3-5], and can still be improved with a better LF path design. However, the bandwidth achieved in this design is 300 times larger than that in [5], and 10^5 – 10^6 times larger than that in [3, 4]. The advantages of the multi-path hybrid sensor structure can be clearly observed in the offset – bandwidth and resolution – bandwidth survey plots of recently published (as of Feb. 2016) high speed CMOS magnetic sensors, as shown in Figure 5.22.

Table 5.1 Comparison table.

Source	This work	Chapter 4	[3]	[4]	[5]
Sensor type	Hall + coil	Hall + Hall	Hall	Hall	Hall
Technology	0.18 µm	0.18 µm	0.35 µm	0.5 µm	0.35 µm
Maximum offset [µT]	40	40	10	3.65 (3σ)	10
Area [mm^2]	8.75	8.75	5.7	N/A	6.5
Resolution [µT$_{rms}$]	210 (diff)	274 (diff)	0.6	0.33	N/A
Input range	±7.8 mT (diff)	±12.5 mT (diff)	±0.5 mT	±10.8 mT	N/A
Bandwidth	3 MHz	400 kHz	100 Hz	5 Hz	10 kHz
Output	Analog	Analog	Digital	Digital	Digital
Supply current [mA]	7.7	8	5	4.2	N/A

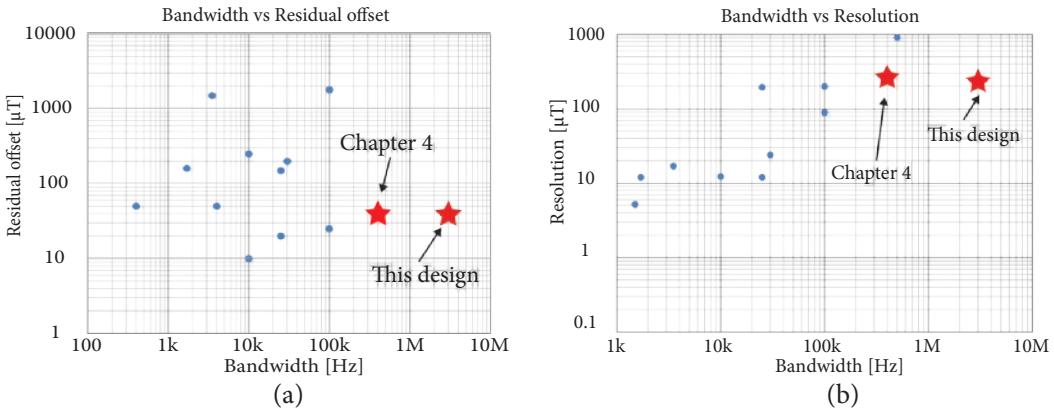

Figure 5.22 CMOS high speed magnetic sensor servo plots (as of Feb. 2016) of (a) residual offset versus bandwidth and (b) resolution versus bandwidth.

5.5 Refined Analysis on Optimal Noise

As mentioned in the experimental results section, the resulting resolution of the overall system does not agree with the noise model of Equation (5.8). This is mainly due to one assumption in Equation (5.8) that the pick-up coils do not contribute any noise in the low frequency band, and vice versa for Hall sensor noise in the high frequency band. This is however not the case in the implementation example discussed in this chapter.

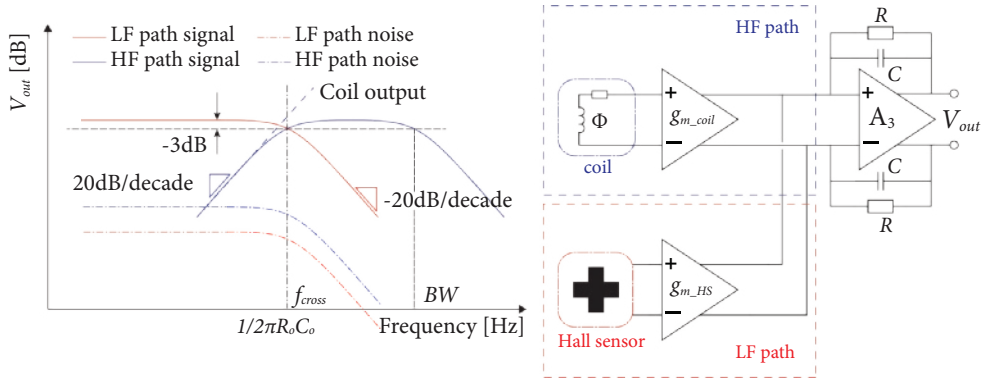

Figure 5.23 Proposed crossover network with 1st order frequency transition.

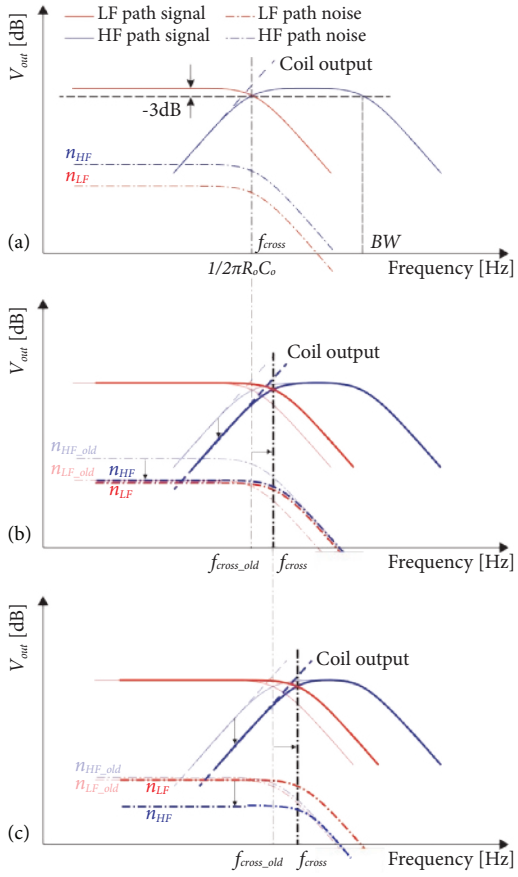

Figure 5.24 Noise changes with different crossover frequencies f_{cross}.

The crossover network used in this implementation, as shown in Figure 5.23, relies on the 1st order frequency transition which requires both sensors to remain on at all times. Considering that

the DC gain of both the LF (4000) and HF (0.25 mS * 4 MΩ = 1000) paths are in the same order of magnitude, the output voltage noise is dominated by the source impedance of the pick-up coils (20 kΩ) and the degeneration resistor (40 kΩ) in g_{m_coil}. Due to the above-mentioned factors, the optimal f_{cross} shifts away.

To maintain a constant relation between the input and output referred noises, the following noise analysis treats the LF path as a reference, namely in which all parameters in the LF path, i.e. the noise and gain of Hall sensor, g_{m_HS} and R will not be changed.

Starting from the scenario of the implementation example as shown in Figure 5.24 (a), the output noise is dominated by the HF path noise n_{HF}. f_{cross} can be shifted to higher frequencies by lowering the feedback capacitor C in the output stage. In order to scale f_{cross} by x from its original value f_{cross_old}:

$$f_{cross} = f_{cross\_old} \cdot x \tag{5.9}$$

The capacitor C needs to be scaled from its original value C_{old} to:

$$C = \frac{C_{old}}{x} \tag{5.10}$$

To maintain the gain matching between both paths, the transconductance of g_{m_coil} needs to be scaled from its original value $g_{m\_coil\_old}$ to:

$$g_{m\_coil} = \frac{g_{m\_coil\_old}}{x} \tag{5.11}$$

This results in a scaled HF path noise density n_{HF} [V/√Hz] with respect to its original value n_{HF_old} at the outputs:

$$n_{HF} = \frac{n_{HF\_old}}{x} \tag{5.12}$$

With Equations (5.9 - 5.12), the output referred noise N_{HF} in V_{rms} can be expressed in terms of its original value N_{HF_old} as:

$$N_{HF} = \sqrt{\frac{n_{HF\_old}^{\ 2} \cdot f_{cross\_old}}{x}} = \frac{N_{HF\_old}}{\sqrt{x}} \tag{5.13}$$

For a scaling factor $x > 1$, the crossover frequency f_{cross} is shifted to higher frequencies, which results in a reduced total integrated noise. With unchanged system sensitivity, the magnetic field referred resolution is thus improved as well. On the other hand, a scaling factor $x < 1$ will worsen

the resolution. The resulting changes with $x > 1$ in signal and noise transfer with respect to their old states are illustrated in Figure 5.22 (b).

Increasing f_{cross} by adjusting C and g_{m_coil} results in a better resolution as the total noise from the HF path is reduced. This is valid as long as the total output noise is dominated by the HF path noise. With a further increased f_{cross}, the output noise density of the HF path will become lower than that of the LF path. The system noise will then be dominated by the LF path. This will then lead to an increase in the total integrated noise, as the noise density of the LF path remains constant over changes in f_{cross}, as shown in Figure 5.22 (c). The LF path output noise N_{LF} in V_{rms} can be expressed in terms of its original value N_{LF_old} with the scaling factor x as:

$$N_{LF} = N_{LF\_old} \cdot \sqrt{x} \tag{5.14}$$

The total output noise N_{total} combining both paths can be written as:

$$N_{total} = \sqrt{\frac{N_{HF\_old}^{\ 2}}{x} + N_{LF\_old}^{\ 2} \cdot x} \tag{5.15}$$

Equation (5.15) will reach its minimum value when:

$$x = \frac{N_{HF\_old}}{N_{LF\_old}} \tag{5.16}$$

The result of Equation (5.16) suggests that the optimal output noise can be achieved when both LF and HF paths contribute an equal amount of noise. In this implementation, the noise floor of the HF path is estimated about 10 times larger than that of the LF path. By applying the refined model to the implementation in this chapter, the crossover frequency should be moved to about 20 kHz, resulting in a 50% improvement in resolution, which is below 100 μT_{rms}.

5.6 Conclusions

The theory and implementation of a hybrid multi-path magnetic sensor system is discussed in this chapter. Thanks to the differentiating characteristic of the pick-up coils, the system signal bandwidth can be extended beyond its noise bandwidth. At the time of publication, the test chip achieved a 3MHz bandwidth, which is an order of magnitude larger than the system introduced in Chapter 4, and 300 times larger than the prior art [5]. A refined noise model is also presented, which takes into account the readout noise in the actual crossover network. A 50% improvement in resolution is expected by adjusting the crossover frequency f_{cross}.

In conclusion, the two examples from Chapter 4 and this chapter demonstrate that the use of multi-path architectures effectively breaks the usual design tradeoff between sensor bandwidth on the one hand, and sensor offset and resolution on the other.

5.7 Bibliography

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A Low Drift Hybrid Multi-Path CMOS Magnetic Sensor with Discrete-Time RRLs

6

6.1 Introduction

Chapter 5 demonstrates that hybrid magnetic sensors combining Hall sensors and pick-up coils can effectively extend system bandwidth with, in principle, no added noise. This unique property makes them immensely suitable for wide-bandwidth precision systems.

However, since Hall sensors and pick-up coils are different by nature, their sensitivities need to be adjusted to match each other. Of the two sensors, the sensitivity of pick-up coils in the voltage mode is geometrically defined, and independent of process and temperature. However, primarily due to changes in carrier concentration, the sensitivity of Hall sensors, on the other hand, is quite dependent on process variations and temperature changes. For this reason, it is more convenient to trim the Hall sensors to the pick-up coils by adjusting their biasing currents.

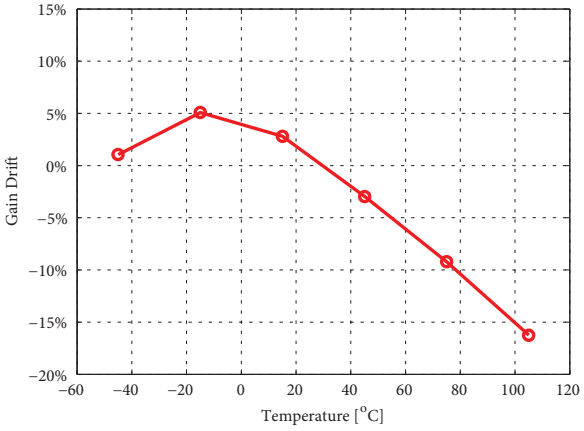

Figure 6.1 Sensitivity drift of an uncompensated Hall sensor system from -45˚C to 105 ˚C.

Taking into account the drift of both the sensor and its readout, the sensitivity of an uncompensated Hall sensor system can drift by as much as 20% over temperature, as shown in

This chapter is derived from a journal publication of the authors: J. Jiang and K. A. A. Makinwa, " A Hybrid Multi-Path CMOS Magnetic Sensor With 76 ppm/°C Sensitivity Drift and Discrete-Time Ripple Reduction Loops," IEEE Journal of Solid-State Circuits, vol. 52, no. 7, pp. 1876-1884, 2017.

Figure 6.1. Furthermore, it has a non-linear temperature dependence which makes it quite difficult to trim. As a result, the sensitivity of Hall sensors needs to be continuously calibrated to withstand temperature change and ensure an overall flat frequency response of the hybrid system.

Another drawback of the triple RRLs presented in Chapters 4 and 5 is that they occupy significant chip area, mainly because they are based on three orthogonal active RC integrators.

This chapter proposes a continuous-time sensitivity calibration scheme which is suitable for Hall sensors in combination with pick-up coils as current sensors. In addition, an area-efficient discrete-time implementation of the RRLs is also proposed. The rest of this chapter is organized as follows: Section 6.2 briefly discusses the existing solutions for low-drift Hall sensors along with their pros and cons; the proposed calibration scheme and its implementation, including the discrete-time RRLs, are described in Section 6.3; the measurement results are shown and discussed in Section 6.4; and Section 6.5 concludes this chapter.

6.2 Low Drift CMOS Hall Sensors

Conventionally, the temperature-related sensitivity drift of any sensor can be corrected if: 1) the temperature is known, and 2) the sensor's temperature dependence is also well known. The resulting drift can then be corrected by an open-loop temperature compensation scheme, which employs an on-chip temperature sensor to continously monitor the die temperature and compensate the gain drift. With carefully designed temperature sensors such as [1, 2], the temperature coefficient of Hall sensors can be reduced to as low as 30 ppm/C˚ [3]. However, accurate characterization of both the Hall and temperature sensors over the entire temperature range takes considerable time. In addition, most temperature sensors require at least a one-point trim to ensure a good accuracy, making this approach rather complex and expensive.

Alternatively as proposed in [4], an on-chip AC magnetic field reference can be generated through on-chip coils. The output signal V_{ref} due to this reference, and hence the system sensitivity, can then be extracted by a dedicated readout channel with synchronous demodulation, as shown in Figure 6.2. With the help of feedback, V_{ref} can be locked to a constant set-point which effectively sets the sensitivity of the overall system as a closed-loop approach. Without any temperature sensors, a gain drift of 50 ppm/ºC can be achieved [4]. To avoid crosstalk, the frequency of the magnetic reference signal should be located outside the desired signal bandwidth. However, this is impractical in the case of a wide bandwidth system. Moreover, since magnetic signals cannot be as easily band-limited as electrical signals, there will always be some residual crosstalk, leading to extra gain error.

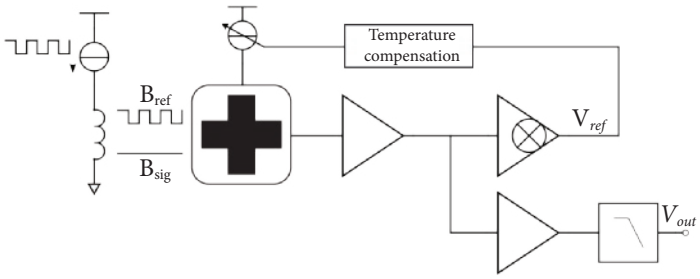

Figure 6.2 Close loop temperature control using on-chip coils [4].

6.3 Low Drift Current Sensor with On-Chip Common-Mode References

In contactless current measurement, two magnetic sensors are typically used in a differential way to naturally reject common-mode interference such as the earth's magnetic field. This feature can be further exploited by introducing a common-mode AC reference which is superimposed on the differential signal introduced by the current flowing through a primary trace, as shown in Figure 6.3. Both these fields are picked up by two sets of Hall sensors, and then amplified. The output results of the amplifiers are subtracted in a differential channel, whose output is proportional to the differential magnetic field, and in which the contribution of the common-mode field is canceled. Conversely, summing their outputs results in a common-mode channel whose output is proportional to the common-mode field, and in which the contribution of the differential field is canceled. The output of the common-mode channel V_{ref} can then be used to monitor and stabilize the sensitivity of the Hall sensor. The frequency of the common-mode field can now be safely located within the sensor's bandwidth, since it will be strongly attenuated by the differential channel.

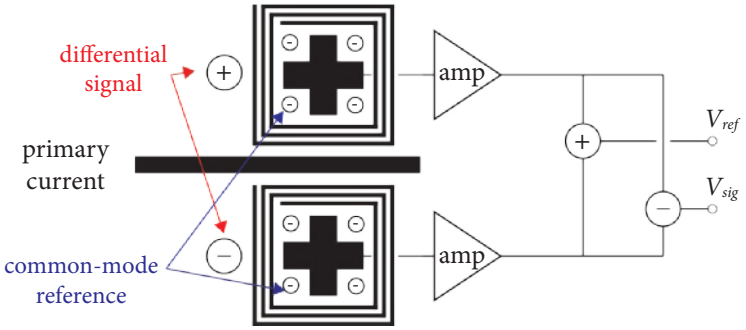

Figure 6.3 Sensitivity extraction by an on-chip common-mode AC reference field.

6.3.1 g_m-Based Hall Sensor Readout

The block diagram of the overall system is shown in Figure 6.4. The design of the HF path is derived from Chapter 5. A transconductance g_{m_coil} converts the outputs of a pick-up coil into currents which are integrated by the transimpedance amplifier (TIA). To preserve the offset performance of the LF path, a coupling capacitor C_{AC} is used to block the offset of g_{m_coil}. A DC servo loop then prevents the output of g_{m_coil} from clipping.

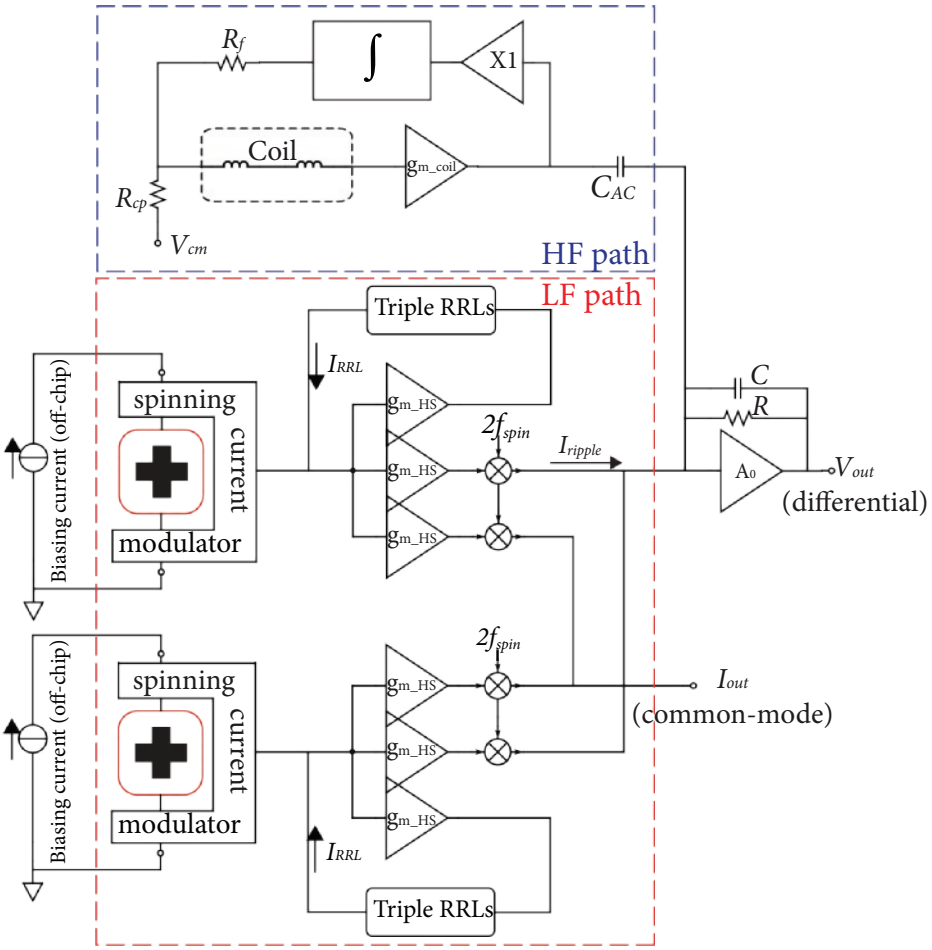

Figure 6.4 Block diagram of the complete system.

In the LF path, each Hall sensor consists of four orthogonally coupled Hall plates to minimize their initial offset. The spinning current technique is then used to further reduce this offset. To realize the differential channel, two g_m stages (g_{m_HS}) convert the outputs of the two Hall sensors into currents, which are demodulated and subtracted to extract the differential signal. The TIA then combines this signal with the output of the HF path. In a similar manner, the common-

mode channel is realized by summing up the two g_{m_HS} outputs. The combined sensitivity of the Hall sensors and g_{m_HS} can be regulated by locking this output current to a set-point. For flexibility, the temperature control loop is implemented off-chip, which is discussed in more detail in Section 6.4.

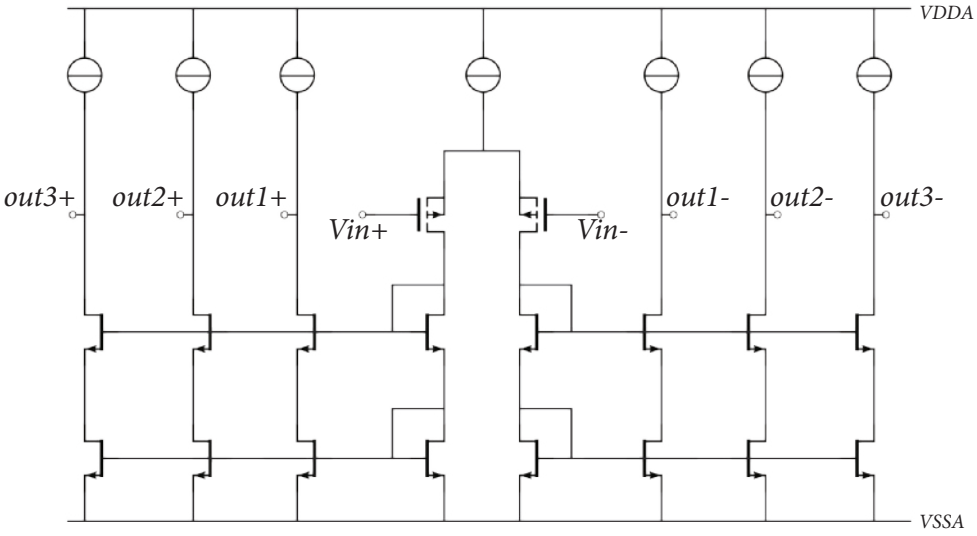

Figure 6.5 Circuit diagram of g_{m_HS} with three output branches.

To suppress the spinning ripple, two sets of triple RRLs feed offset compensation currents directly into the two Hall sensors. This is in contrast to the implementation in Chapter 4, in which the RRLs acted on the output of a pre-amplifier. Since their offset is canceled by the RRLs, the Hall sensors produce relatively small output signals (in the order of 100 μV), which greatly simplifies the design of g_{m_HS}. The residual ripple will then be limited by the mismatch between the three g_{m_HS} stages. To minimize this, they are implemented as a single g_m stage with three output branches, as shown in Figure 6.5.

6.3.2 Discrete-Time Triple RRLs

In this design, the outputs of the two Hall sensors are individually processed to simultaneously extract differential and common-mode signals. The continuous-time implementation of the triple RRLs, as in Chapters 4 and 5, would then occupy considerable chip area, mainly due to the need to realize three independent analog integrators. In this chapter, the integrators are implemented as up/down counters in an area-efficient, discrete-time manner.

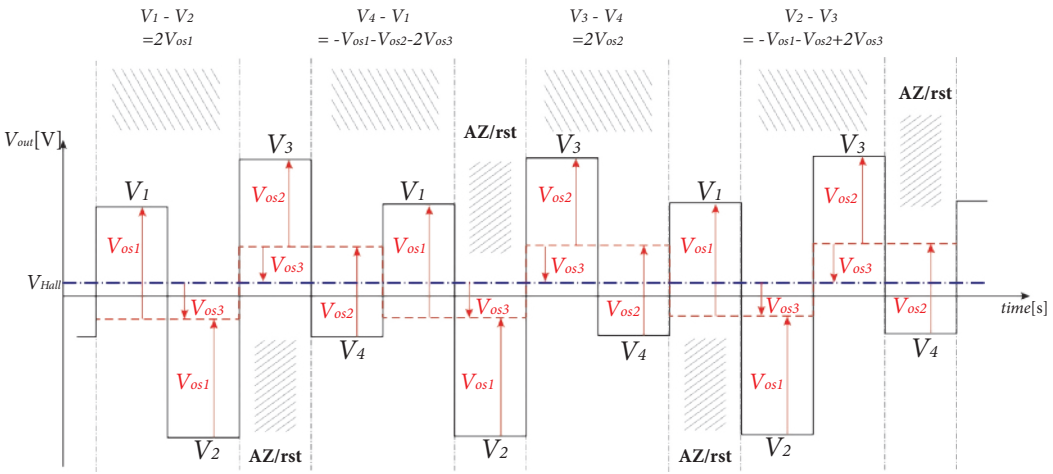

Figure 6.6 Triple RRLs algorithm for discrete-time implementation.

Figure 6.6 shows the output waveform of a typical 4-phase spinning-current Hall sensor. The output during each of the four spinning phases $V_{1\text{-}4}$ can then be expressed in terms of the magnetic signal V_{Hall} and three offset components V_{os1}, V_{os2} and V_{os3} as follows:

$$V_1 = V_{Hall} + V_{os1} - V_{os3} \tag{1}$$

$$V_2 = V_{Hall} - V_{os1} - V_{os3} \tag{2}$$

$$V_3 = V_{Hall} + V_{os2} + V_{os3} \tag{3}$$

$$V_4 = V_{Hall} - V_{os2} + V_{os3} \tag{4}$$

Offsets V_{os1} and V_{os2} can be directly extracted by computing $V_1 - V_2$ and $V_3 - V_4$, respectively. Information about V_{os3} is, however, contained in $V_4 - V_1$ and $V_2 - V_3$:

$$V_4 - V_1 = -V_{os1} - V_{os2} + 2V_{os3} \tag{5}$$

$$V_2 - V_3 = -V_{os1} - V_{os2} - 2V_{os3} \tag{6}$$

Equation (5) and (6) suggest that V_{os3} can be extracted from these signals, provided that V_{os1} and V_{os2} become sufficiently small, i.e. after the other RRLs have settled. This means that a different offset component can be extracted from the output of every two adjacent spinning phases, allowing for the reuse of hardware and, hence, saving chip area.

The implementation of the RRLs is shown in Figure 6.7. The difference in the output current of g_{m_HS} during two spinning phases is directly integrated by an auto-zeroed integrator. A

comparator senses the polarity of the integrator's output, and increments or decrements the appropriate up/down counter (one for each RRL). The digital outputs of the three counters are then combined and applied to three DACs which generate the appropriate compensation currents via g_m stages. According to the algorithm shown in Figure 6.6, the offset components V_{os1} and V_{os2} are updated once every three spinning cycles. V_{os3} is updated twice every three spinning cycles, and will settle after V_{os1} and V_{os2} become sufficiently small. From (5) and (6) it should be noted that the contribution of V_{os1} and V_{os2} to the V_{os3} error signal appears with alternating polarity, and so V_{os3} will, on average, remain stable until the other two loops settle. At steady state, the residual offset $V_{os1\text{-}3}$ will be limited to ± 1 LSB.

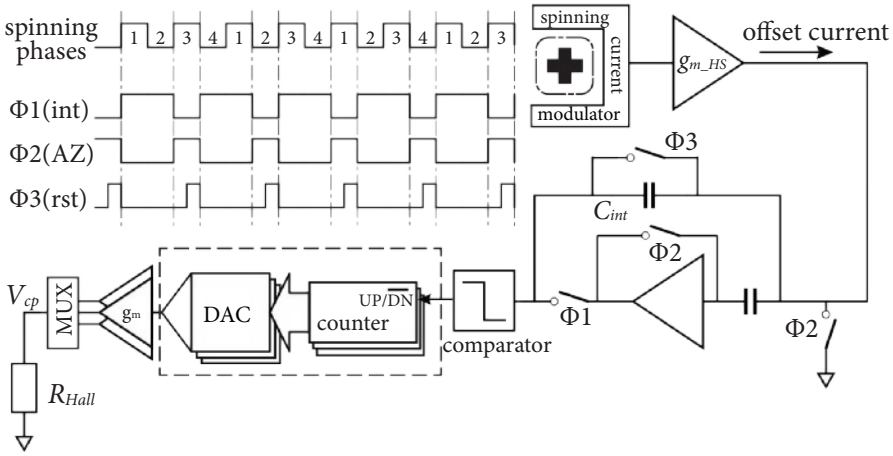

Figure 6.7 Discrete-time implementation of the RRLs.

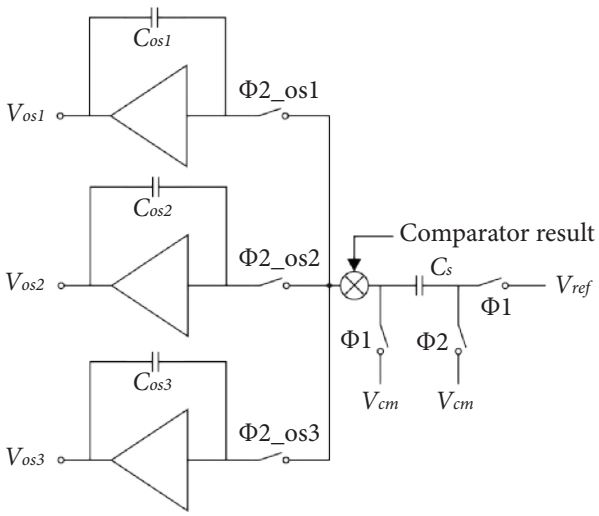

Figure 6.8 Area-efficient implementation of the up/down counters and DACs.

To prevent the sensor from becoming stuck in local limit cycles, the DACs used in the RRLs need to be monotonic. For area-efficiency and simplicity, the operation of the up/down counters and DACs is emulated by a multiplexed switch-cap integrator, as shown in Figure 6.8. In Φ1, a reference voltage V_{ref} is sampled on a sampling capacitor C_s. During Φ2, depending on the comparator outputs, the charge stored on C_s is either added to or subtracted from one of three integration capacitors $C_{os1\text{-}3}$. In this design, C_s = 150 fF and $C_{os1\text{-}3}$ = 10 pF, which with V_{ref} = 50 mV results in a step size of 0.75 mV. With a compensation g_m = 4 μS and R_{Hall} = 1 kΩ, the residual ripple at the input of g_{m_HS} can be reduced to 3 μV.

6.4 Experimental Results

The proposed system was fabricated in a 0.18 μm CMOS process; the chip photo is shown in Figure 6.9. The total area is 2.8 mm × 2.9 mm = 8.12 mm^2. The pick-up coils in the HF path, similar to Chapter 5, are placed away from the readout circuitry and shielded by metal plates to avoid high frequency crosstalk. The common-mode coils for temperature calibration are placed right on top of the Hall sensors, and have a measured resistance of 220 Ω. The triple RRL region for the left Hall sensor (highlighted in blue), occupies an area of about 0.5 mm^2, which is about 20% smaller than the previous continuous-time implementation in Chapter 4.

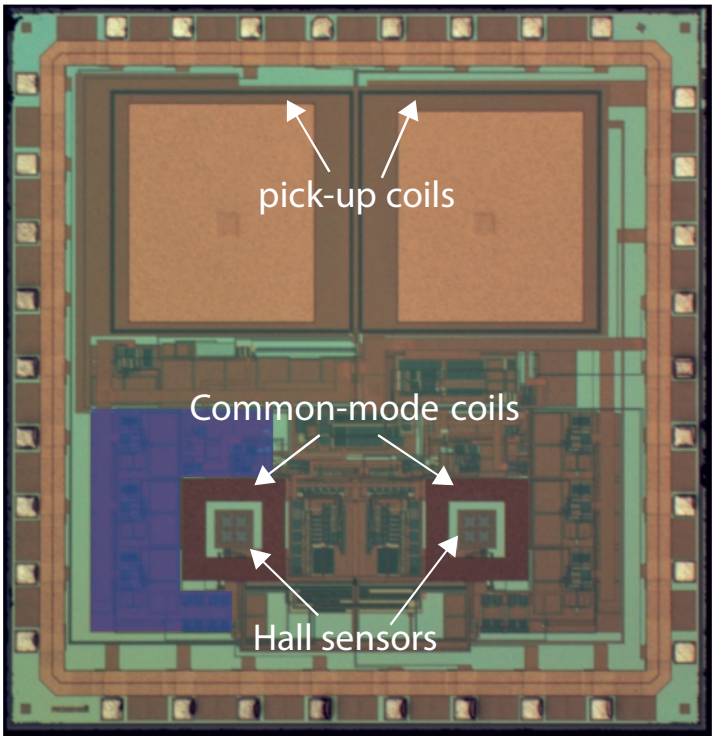

Figure 6.9 Micro photo of the chip.

To verify the performance of the triple RRLs, Figure 6.10 shows the FFT of the system output when the HF path is disabled. With f_{spin} = 41.65 kHz and a zero magnetic field, the RRLs can reduce the spinning ripple from over 1 mT down to 21 μT at 83.3 kHz ($2f_{spin}$). This residual ripple is limited by the mismatch between the current mirrors in the g_{m_HS} stage. At f_{spin} = 41.65 kHz, the residual ripple is reduced to 2.9 μT, which is solely limited by the step size of the switched capacitor integrator in the RRLs. The sub-harmonics in the FFT plot are due to the fact that the modified RRL scheme is multiplexed between three ripple components, and therefore the spinning ripple is undersampled.

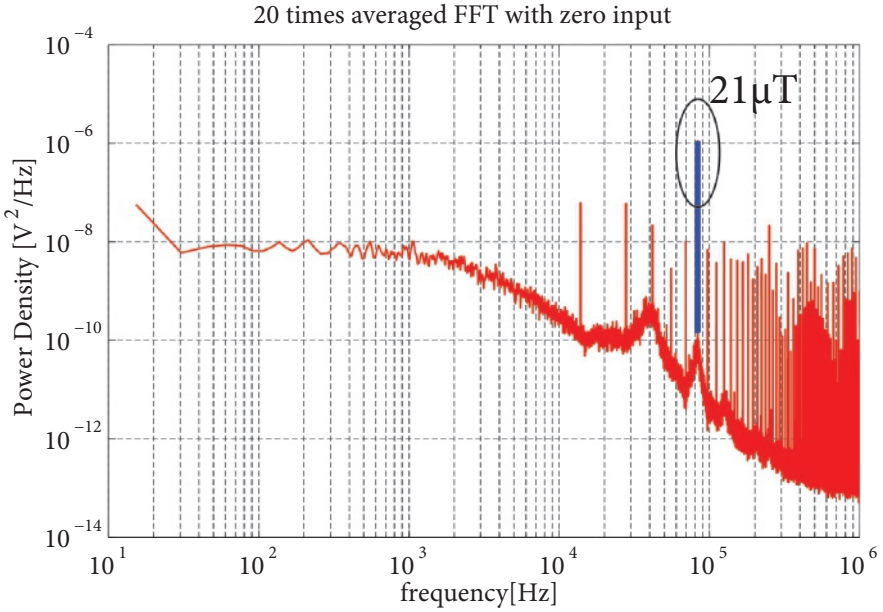

Figure 6.10 FFT plot of the system output with the HF path disabled and a zero magnetic field.

To avoid high frequency distortion due to the eddy current effect associated with the frame pad in normal packages (explained in Chapters 4 and 5), the test chip is mounted directly on top of a PCB trace using the chip-on-board (CoB) technique. After trimming at 30˚C, each Hall sensor is biased by a 2 mA (0.5 mA/plate) current, resulting in a sensitivity of about 71.4 mV/T. With both LF and HF paths active, the system achieves a flat frequency response with the same bandwidth, as in Chapter 5, of 3 MHz (Figure 6.11).

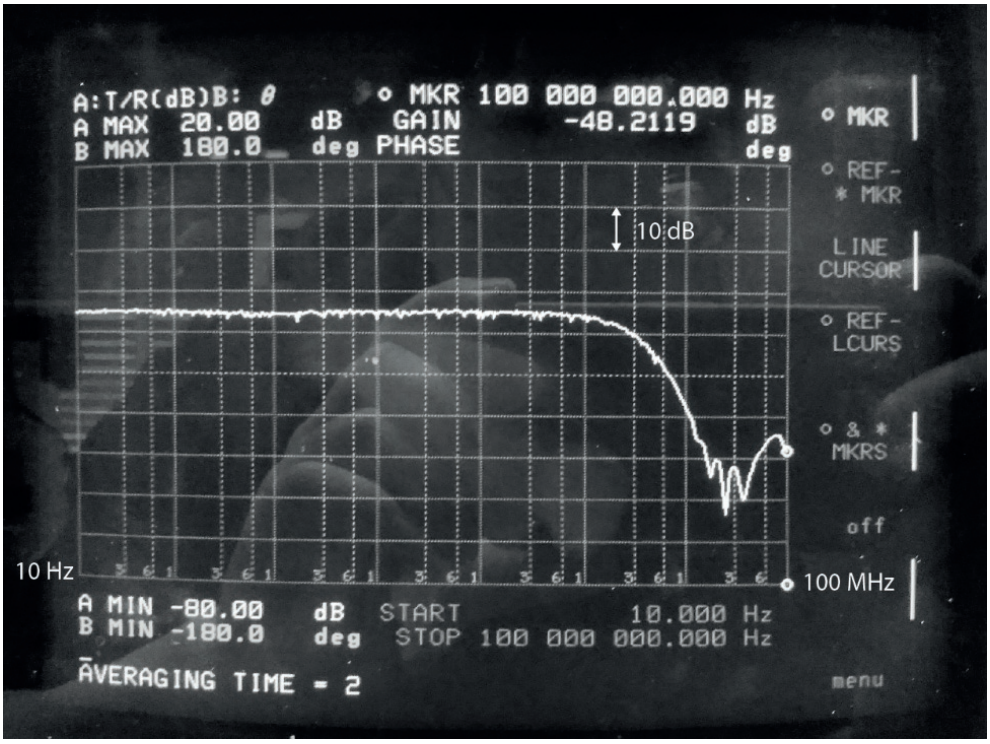

Figure 6.11 Measurement frequency response from 10 Hz to 100 MHz.

To generate a temperature-independent common-mode field for gain calibration, the on-chip common-mode coils are driven by a square-wave current with a constant amplitude (±10 mA) at 80 Hz. This is guaranteed by embedding the coils in the feedback of an off-chip inverting amplifier, as shown in Figure 6.12. The output currents of the common-mode channel are synchronously demodulated and read out by an off-chip current-to-voltage converter, the averaged output voltages V_{out} of which are compared to a set-point by a comparator. The comparison results then increment or decrement a DAC by 1 LSB, which adjusts the biasing current of the Hall sensors by 5 μA.

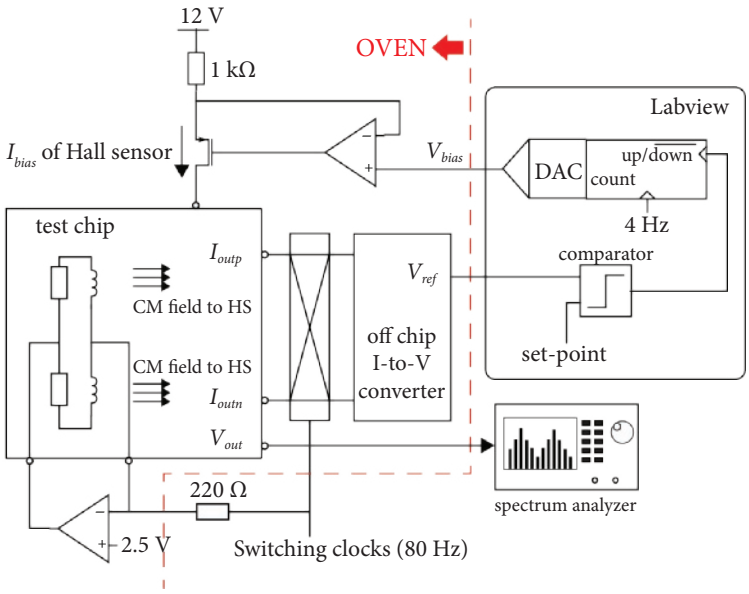

Figure 6.12 Temperature stabilization setup.

Figure 6.12 shows the measured frequency response of the system at 105˚C from 100 Hz to 12 kHz (f_{cross} = 2 kHz). Without the temperature calibration scheme, a 2 dB gain mismatch can be observed across the frequency range. This can then be corrected by activating the proposed calibration scheme. Up till 12 kHz, no gain mismatch can be observed between the HF and the calibrated LF paths.

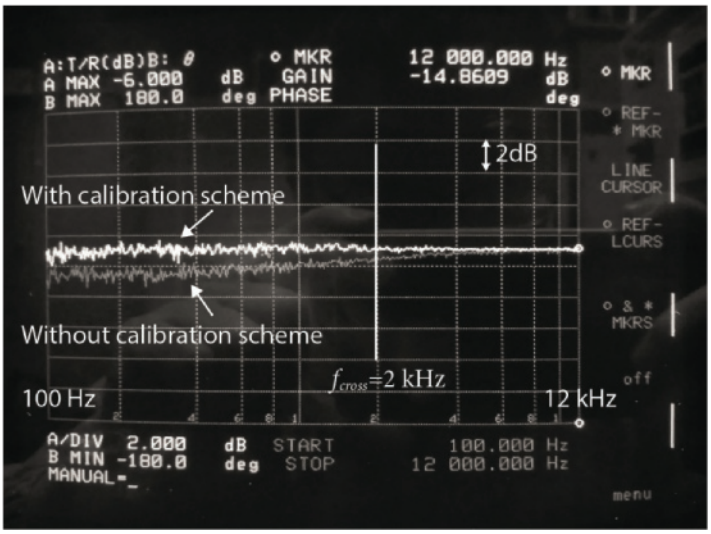

Figure 6.13 Measured frequency response from 100 Hz to 12 kHz with and without temperature calibration.

The gain drift of the system is quantitatively characterized in an oven from -45˚C to 105˚C. Driven by a spectrum analyzer, a primary current is generated outside the oven. The system outputs are directly analyzed by the same spectrum analyzer to extract the gains at the excitation frequencies. The measurement results are summarized in Figure 6.14. Without gain calibration, the LF path gain at 800 Hz drifts as high as 22%, which is caused by the sensitivity drifts of both the Hall sensors and g_{m_HS}. With the proposed gain calibration scheme, the gain drift can be reduced to 1%, corresponding to a maximum temperature coefficient of 76 ppm/˚C, which is comparable to the state-of-the-art [3, 4].

Similarly, the sensitivity of the HF path is characterized at 86.22 kHz. The HF path gain drifts from -10% to 7%, which was not observed in the previous test up to 12 kHz (Fig. 18). This is because at high frequencies, the skin-effect in the current-conducting trace starts to influence the trace impedance and change the geometry profile of the resulting magnetic field. Together with the non-linearity of g_{m_coil}, this results in additional sensitivity drift. Nevertheless, this result is still comparable to the performance of other coil-based magnetic sensors [5].

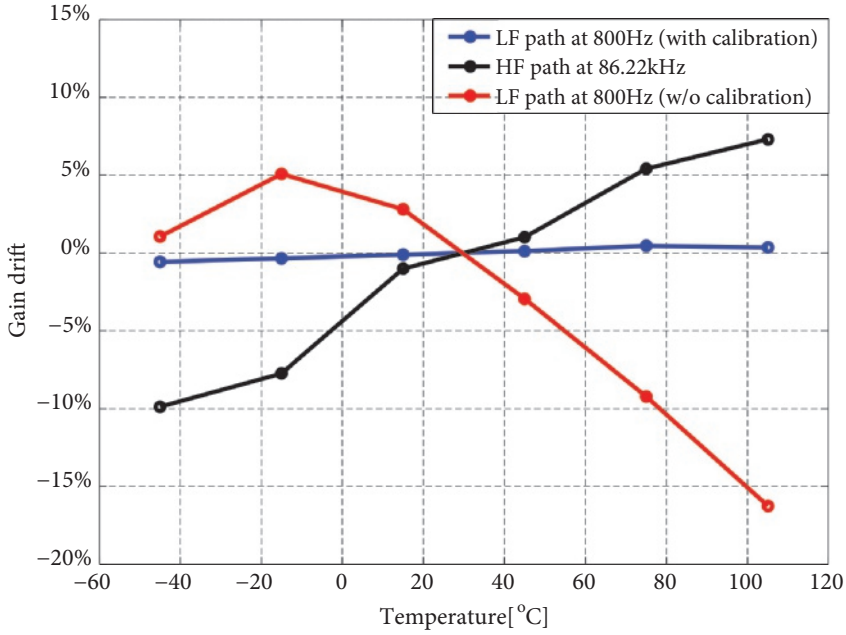

Figure 6.14 Measured temperature coefficient of the system at 800 Hz and 86.22 kHz.

Table I summarizes the performance of this design in comparison to other state-of-the-art CMOS low drift magnetic sensors. Compared to low drift Hall sensors with other temperature calibration schemes, the proposed scheme achieves a gain accuracy comparable to [3] and [4], while the bandwidth is at least 6× higher. Compared to other coil-based magnetic sensors such as [5], the proposed system can cover the full bandwidth including DC while achieving a similar gain accuracy.

Table 6.1 Comparison table.

Source	This work		[3]	[4]	[5]
Technology	0.18 µm		0.35 µm	0.8 µm	N/A
Power supply	5 V		5 V	5 V	2.7 – 5.5 V
Temperature compensation	Close loop		Open loop	Close loop	N/A
Sensitivity drift [ppm/˚C]	76 (LF)	1100 (HF)	30	50	800**
Area [mm^2]	8.75		3.5	11.5	N/A
Input range	± 7.8 mT		± 400-2.2 mT	± 50 mT	N/A
Bandwidth	3 MHz		125 kHz*	500 kHz***	50 kHz–1 MHz

* Calculated based on spinning frequency
** >20% full scale input
*** Theoretical value

6.5 Conclusions

In this chapter, a self-calibration scheme is proposed to continuously regulate the temperature drift of Hall sensors in a hybrid multi-path magnetic sensor. Exploiting the common-mode rejection feature of differential current sensing systems, common-mode coils are integrated to generate a common-mode AC reference magnetic field, through which the system's sensitivity can be actively monitored and, hence, regulated. With this approach, the overall sensitivity drift of the Hall sensors can be reduced from 22% to 1% in the temperature range from -45˚C to 105˚C, corresponding to a temperature coefficient of 76 ppm/˚C. Furthermore, the triple RRLs for spinning current Hall sensors are implemented in a discrete-time manner, which occupies 20% less chip area compared to the previous continuous-time implementation. When combined with temperature-independent pick-up coils, the system achieves a flat frequency response with a bandwidth of DC to 3 MHz.

6.6 Bibliography

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Conclusions and Future Work 7

In the previous chapters, several prototypes of CMOS wide-bandwidth magnetic sensors have been presented. In this chapter, conclusions will be drawn based on the experimental results obtained from these prototypes. In addition, some suggestions for future work will be proposed. Finally, the original contributions of this Ph.D. thesis will be listed.

7.1 Conclusions

Despite the fact that the Hall Effect is a fast physical phenomenon capable of achieving GHz bandwidths, the bandwidth of low-offset spinning-current Hall sensors has been limited to a few tens of kHz due to the need for low-pass filters to suppress their spinning ripple. This constraint in 4-phase spinning current Hall sensors is addressed by the use of three orthogonal ripple reduction loops (RRLs), which is proposed in Chapter 3. Since this technique cancels the Hall sensor offset before amplification, the dynamic range of the analog front-end (AFE) is also greatly relaxed.

However, the proposed triple RRLs cannot distinguish between spinning ripple and magnetic signals at the spinning frequencies. This effectively creates two notches in the frequency response, resulting in slow settling issues. This problem is addressed by a multi-path circuit technique which is covered in Chapter 4. The prototype presented in Chapter 4 combines a spinning current Hall sensor with triple RRLs in its low frequency (LF) path and a non-spun Hall sensor in its high frequency (HF) path. The overall system achieves a 400 kHz bandwidth with an offset of 40 μT.

Being essentially resistors, increasing the bandwidth of a Hall sensor increases its noise, and hence decreases its signal-to-noise ratio (SNR). To break this relationship, pick-up coils are used to replace non-spun Hall sensors to combine with spinning current Hall sensors. The mathematical proof and prototype implementation of this hybrid concept are presented in Chapter 5, which, to the author's best knowledge is the world's first on-chip realization of this concept. With a one-point sensitivity calibration, the hybrid system achieves a signal bandwidth

of 3 MHz with a resolution of 210 μT, which is even better than that of the multi-path Hall sensor system (272 μT) in Chapter 4.

The gain of Hall sensors, unlike that of pick-up coils, exhibits significant temperature drift. Therefore, the Hall sensors in a hybrid system will require continuous-time gain calibration. Conventional approaches with on-chip temperature sensors and single on-chip coils are either too complex or impractical for wide-bandwidth systems. This challenge is addressed in Chapter 6, which exploits the differential structure of current sensors by introducing a common-mode AC magnetic reference through two on-chip coils. This reference is naturally rejected at the main outputs, but is processed in a separate channel to extract the system sensitivity, so that the Hall sensors can be continuously calibrated. With this scheme, a prototype reduces the Hall sensor drift from 22% to 1% from -45˚C to 105˚C, corresponding to a temperature coefficient of 76 ppm/˚C. In addition to system innovations, Chapter 6 also presents a discrete-time implementation of triple RRLs for a spinning Hall sensor, which is about 20% smaller than the continuous-time implementation in Chapter 4.

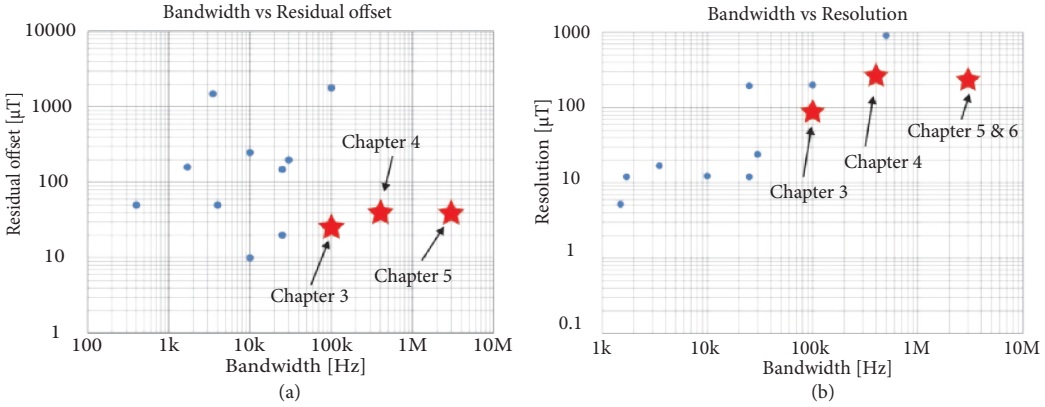


Figure 7.1 CMOS high speed magnetic sensor servo plots (as of Feb. 2016) of (a) residual offset versus bandwidth and (b) resolution versus bandwidth.

Figure 7.1 (a) and (b) depict plots of bandwidth versus offset and noise for several CMOS magnetic sensors reported in IEEE publications from 2000–2015 (see Appendix for more detail). From these plots, a clear trade-off can be seen between bandwidth and offset, on the one hand, and between bandwidth and resolution on the other. Thanks to their multi-path architecture, the prototypes presented in Chapters 4 and 5 break the bandwidth-offset tradeoff. In addition, the prototypes reported in Chapters 5 and 6 break the bandwidth-resolution trade-off by exploiting the differentiating characteristics of pick-up coils.

7.2 Future Work

The main focus of this dissertation has been on the application of multi-path and multi-sensor techniques to CMOS magnetic sensors. By using these techniques, such sensors can achieve wide bandwidth together with low-offset and noise. However, the designs presented in this dissertation are proof-of-concept prototypes. In other words, they have not been optimized in terms of their noise, offset, dynamic range, power consumption and area. For instance, the pick-up coil readout presented in Chapter 5 and 6 needs to be optimized to reduce its noise. Moreover, the pick-up coils used in these prototypes occupy quite a large chip area, and are not well optimized for current sensing. In short, the performance of the prototypes in this dissertation still has a lot room for improvement.

Another important point to note is that although the hybrid magnetic sensors presented in this dissertation used Hall sensors to sense low frequencies, other magnetic sensors could have been used for this purpose, such as GMR (giant magnetoresistive) sensors and fluxgates, to achieve even better performance.

It is also worthwhile to point out that the multi-sensor technique could be used to realize magnetic sensors with high resolution and high dynamic range. This thought was inspired by the fact that most precision magnetic sensors, such as GMR sensors and fluxgates, have superior sensitivities compared to Hall sensors, but are subject to limited dynamic range due to the use of ferromagnetic materials in their sensor structures. A hybrid magnetic sensor can be built in such a way that strong magnetic field signals are read out by Hall sensors, while weak magnetic field signals are read out by GMR sensors or fluxgates.

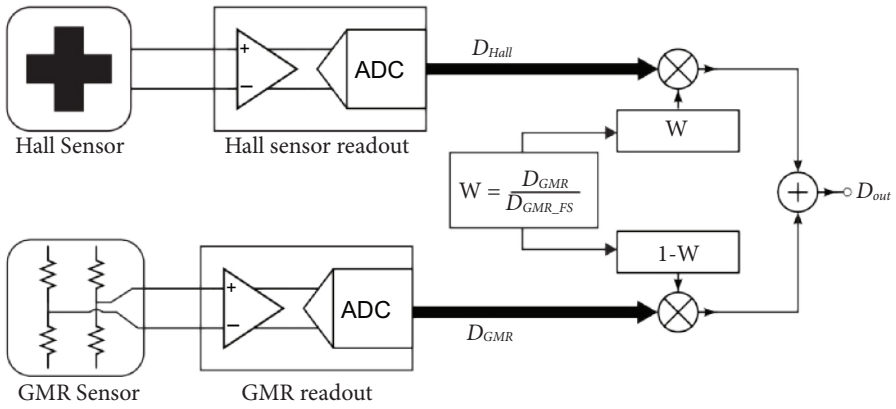


Figure 7.2 System block diagram of combining Hall sensors and GMR sensors.

A possible architecture combining Hall sensors and GMR sensors is shown in Figure 7.2. The GMR sensor and the Hall sensor are read out by their customized readout circuitry, and two ADCs will convert their outputs into digital words D_{Hall} and D_{GMR}. The GMR sensor outputs D_{GMR}

are then compared to its full scale D_{GMR_FS} to calculate a weight distribution factor W, which will be directly used to multiply D_{Hall} and added up to D_{GMR} * (1-W). The final output can be then expressed as:

$$D_{out} = D_{Hall} \cdot W + D_{GMR} \cdot (1 - W) \tag{5.1}$$

which provides a smooth output transition from the GMR sensor to the Hall sensor before the GMR sensor runs out of its dynamic range.

The system shown in Figure 7.2 is still very conceptual, and requires further research in many aspects. One obvious drawback is that the system is not very compact, as it uses two separate readouts and ADCs. The weight distribution circuit is implemented in the digital domain which will cause extra delay when updating W. This can probably be addressed by an analog implementation, which at this stage, remains unclear.

7.3 Original Contributions

In this Ph.D. research, a few original contributions are made to the field of CMOS magnetic sensors:

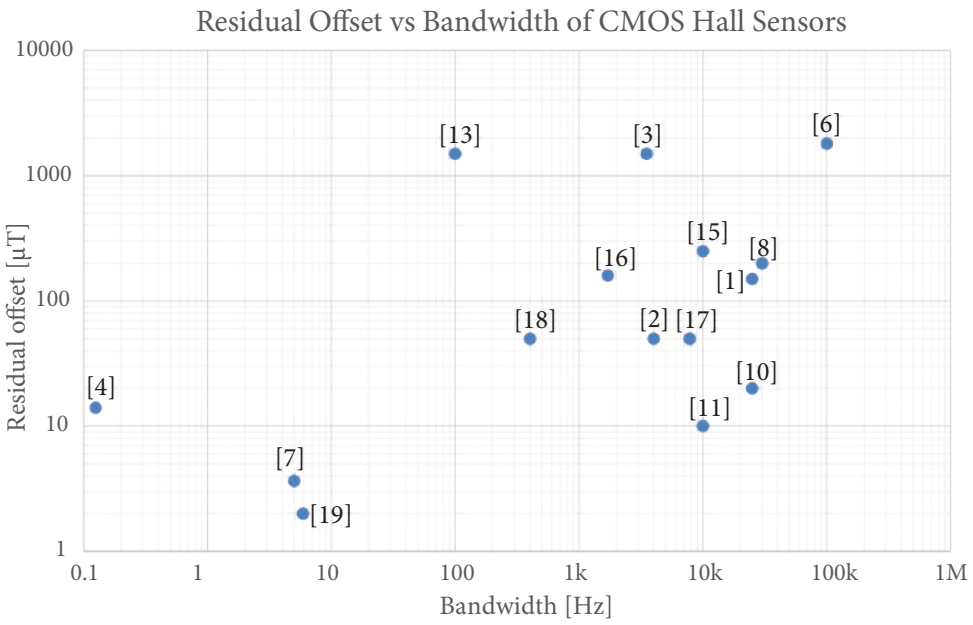
- The invention of triple RRLs for 4-phase spinning current Hall sensors (Chapter 3) and their continuous-time (Chapter 4) and discrete-time (Chapter 6) realization;
- The invention and realization of a multi-path Hall sensor system (Chapter 4);
- The mathematical analysis of a hybrid concept of combining Hall sensors and pick-up coils (Chapter 5);
- The invention and realization of an integrated hybrid wide-bandwidth magnetic sensor with Hall sensors and pick-up coils (Chapter 5);
- The invention and realization of continuous-time Hall sensor gain calibration in hybrid magnetic sensors for differential current measurements (Chapter 6);

Appendix

In this Ph.D. dissertation, two survey plots based on existing publications are used for referencing and comparison purposes. Due to practicality, the publications used in the survey were selected based on criteria concerning the main subject of this dissertation:

- CMOS-based design
- Bandwidth and offset (untrimmed) or noise measured, or can be calculated
- Originally published between 2000 January – 2016 February in
    - Conferences:
        - IEEE International Solid-State Circuits Conference (ISSCC)
        - IEEE Symposium on VLSI Circuits (VLSI)
        - IEEE European Solid-State Circuits Conference (ESSCIRC)
        - IEEE Asian Solid-State Circuits Conference (A-SSCC)
        - IEEE Custom Integrated Circuits Conference (CICC)
        - IEEE Sensors
    - Journals:
        - IEEE Journal of Solid-State Circuits (JSSC)
        - IEEE Sensors Journal

The survey results (excluding the publications related to this dissertation) are shown on the next page followed by a list of the source publications.


Residual Offset vs Bandwidth of CMOS Hall Sensors
Residual offset [µT]
10000
1000
100
10
1
0.1
1
10
100
1k
10k
100k
1M
Bandwidth [Hz]
[13]
[3]
[6]
[15]
[8]
[16]
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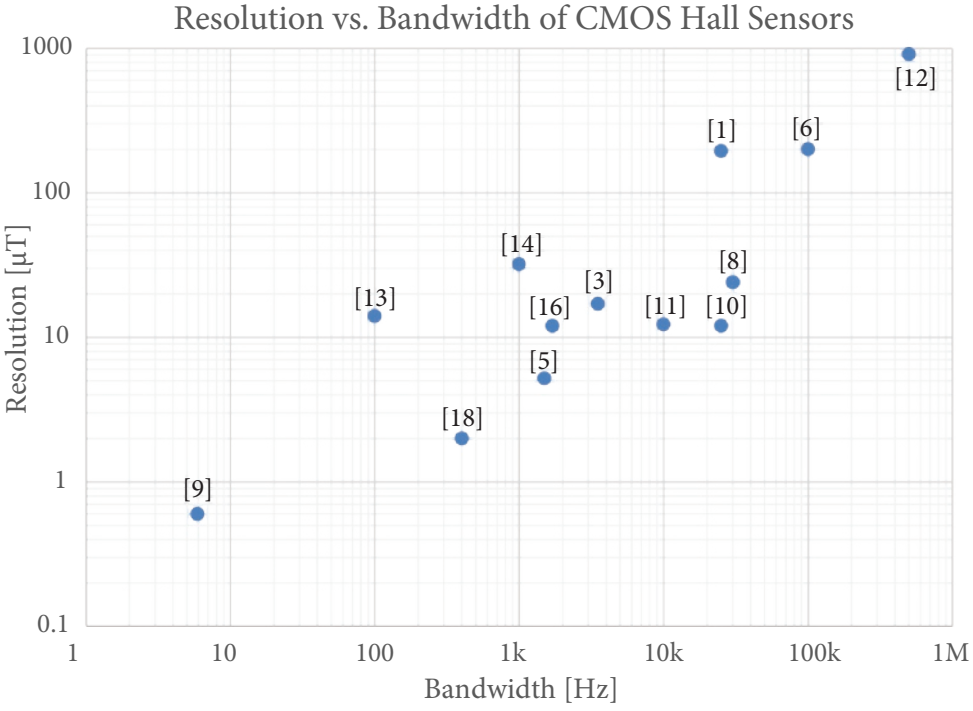
Resolution vs. Bandwidth of CMOS Hall Sensors
Resolution [µT]
1000
100
10
1
0.1
1
10
100
1k
10k
100k
1M
Bandwidth [Hz]
[12]
[1]
[6]
[14]
[8]
[3]
[13]
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[11]
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Summary

This Ph.D. dissertation describes the theory and realization of wide-bandwidth magnetic sensors for current measurements which breach the conventional offset and noise constraints in CMOS processes. These are achieved by several circuit-level and system-level innovations, including the use of three orthogonal ripple reduction loops (RRLs) in spinning-current Hall sensors, a multi-path architecture with double Hall sensors, and a hybrid magnetic sensor system combining Hall sensors and pick-up coils. The prototypes with these techniques have advanced the bandwidth of state-of-the-art CMOS magnetic sensors by more than two orders of magnitude.

Chapter 1

Current sensors are widely employed in electronic systems for measurement, control and protection purposes. For safety concerns in high voltage systems, they are commonly implemented with magnetic sensors so that direct contact can be avoided. Current industrial trends towards better safety and efficiency have posed a high demand on sensor bandwidth. For instance in high power systems, protection modules need to detect an overload event within a short time, e.g. 1 μs, to prevent catastrophic damage. In addition, the trend in state-of-the-art switch mode power supplies is moving towards size reduction to reduce cost, which is realized by using smaller passive components, i.e. inductors. To maintain high efficiency, these power supplies operate at over 1 MHz, which in turn requires that the current sensors are high speed.

Among all magnetic sensors, Hall sensors and pick-up coils can be fabricated in CMOS processes with zero added cost. However, the achievable bandwidth of both is highly determined by their noise. Since Hall sensors are essentially resistors, their noise power increases linearly as their bandwidth expands, resulting in a decreasing signal-to-noise ratio (SNR); a decrease in the pick-up coil SNR is also expected at low frequencies due to their sensitivity decrease. State-of-the-art Hall sensors and pick-up coils can only cover bandwidths of DC to 100 kHz and 50 kHz to 1 MHz, respectively.

Hall sensors and pick-up coils can be combined to achieve high bandwidth. This concept has been demonstrated on PCB with discrete components. However, the challenges of CMOS integration have never been addressed.

Chapter 2

Hall sensors and pick-up coils are reviewed in this chapter to provide the background of this Ph.D. research. In CMOS Hall sensors, achieving both high accuracy and bandwidth is quite challenging. This is primarily due to their relatively large offset, which can range from 10 mT to 50 mT. Presently this offset is suppressed by means of a dynamic offset cancellation technique, namely the spinning current technique. By periodically alternating the biasing and sensing direction of a Hall sensor, offset can be up-modulated appearing as a square-wave ripple at the final outputs. With proper biasing and readout approaches, an offset of less than 50 μT can be achieved. This is however at considerable expense of bandwidth due to the need of ripple reduction, which was conventionally addressed by limiting system bandwidth with low-pass filters (LPFs). Increasing the spinning frequency can alleviate this issue, but usually results in higher offsets due to charge injections and switching transients. For these reasons, precision CMOS Hall sensors usually have a bandwidth of less than 100 kHz.

Conversely, pick-up coils are preferably used for high frequency AC magnetic field measurements due to their differential characteristic. For this purpose, low quality coils with relatively large source resistances are preferred to prevent potential oscillation and their outputs are commonly interfaced with integrators. The state-of-the-art coil-based magnetic sensor can achieve a bandwidth from 50 kHz to 1 MHz.

Chapter 3

To solve the offset constraint in wide bandwidth CMOS Hall sensors, Chapter 3 proposes a readout technique which uses three orthogonal ripple reduction loops (triple RRLs) to continuously measure the spinning ripple of a 4-phase spinning current Hall sensor and compensate its offset before amplification. Thanks to the continuous-time ripple compensation before amplification, this technique facilitates a spinning frequency inside the signal bandwidth, and highly relaxes the dynamic range requirement of the readout circuitry. Implemented and verified with off-chip digital loops, the prototype achieved over 100 kHz bandwidth with a spinning frequency of 1 kHz and an offset of only 25 μT. However, as the RRLs cannot distinguish spinning ripple from real magnetic signals at spinning frequencies, this approach results in two notches in the frequency response, which may lead to a slow settling issue.

Chapter 4

To address the notch issues associated with triple RRLs in spinning current Hall sensors, Chapter 4 proposes the first multi-path readout architecture for CMOS Hall sensors. It employs a spinning current Hall sensor with triple RRLs in its low frequency (LF) path to ensure a low offset, and a non-spun Hall sensor in its high frequency (HF) path to extend the system bandwidth and fill up the notches from the LF path. In addition, the triple RRL concept is fully integrated on-

chip with continuous-time integrators. The overall system achieves a bandwidth of 400 kHz and an offset of 40 μT. The on-chip RRLs reduce the spinning ripple from over 1.1 mT down to 7.3 μT, which is commensurate with the sensor's noise into a bandwidth of 300 Hz. At the time of publication, this prototype is 40 times faster than the state-of-the-art CMOS precision magnetic sensors. The bandwidth achieved in this prototype can be further improved by increasing the bandwidth of its readout, but this will inevitably result in more noise than the current 272 μT_{rms}.

Chapter 5

To address the noise constraint in wide-bandwidth magnetic sensors, Chapter 5 studies the possibility as well as the design theories of hybrid magnetic sensor systems which combine Hall sensors and pick-up coils. Hall sensors and pick-up coils have quite distinct SNR trends in terms of bandwidth. In Hall sensors, the SNR decreases as the bandwidth expands, while in pick-up coils, the SNR increases as the bandwidth expands to higher frequencies. Above certain frequencies, pick-up coils produce a superior SNR compared to Hall sensors. This frequency is the so-called cross-over frequency, from which a system should switch from Hall sensors to pick-up coils for the sake of the SNR.

To verify this theory, a prototype chip was fabricated with an identical LF path design of the spinning Hall sensor with triple RRLs in Chapter 4 and a newly designed HF path with pick-up coils. With a sensitivity trim, the prototype hybrid system achieves not only a bandwidth of 3 MHz, which is an order of magnitude higher than that achieved in Chapter 4, but also even lower noise of 210 μT_{rms}. In the presence of a large signal step, the system settles within 400 ns (>90%), which to the author's best knowledge is the fastest CMOS magnetic sensor ever published. With identical chip area, offset, and comparable current consumption to the multi-path Hall sensor system in Chapter 4, this hybrid system effectively breaks the design trade-off of bandwidth and resolution.

From a system perspective, the optimal cross-over frequency varies from that of the sensor perspective due to excess noise from the readout circuitry. This effect was also analyzed based on the measurement results of the hybrid prototype.

Chapter 6

The hybrid sensor system demonstrated in Chapter 5 requires a sensitivity trim to ensure a flat frequency response. However, primarily due to changes in the carrier concentration, the sensitivity of a Hall sensor is quite temperature-dependent, and will drift significantly over changes in temperature. In contrast, the sensitivity of the voltage-output pick-up coils is temperature-independent. This means that the sensitivity of Hall sensors needs to be continuously calibrated to withstand temperature changes.

Exploiting the fact that the differential sensing scheme typically used for current sensing naturally rejects common-mode fields, Chapter 6 proposes a closed-loop sensitivity regulation scheme based on a common-mode reference field generated by on-chip coils. This scheme eliminates the need for temperature sensors and preserves full system bandwidth thanks to the natural common-mode rejection of the differential sensing structure.

An area-efficient implementation of the triple RRLs is also proposed in Chapter 6. This is achieved by replacing continuous-time integrators with discrete-time integrators, such that the hardware can be multiplexed between different ripple components.

A prototype chip was designed with the proposed Hall sensor readout in its LF path, and the HF path design inherited from the hybrid system in Chapter 5. The complete system achieves a similar bandwidth of 3 MHz which can withstand temperature changes. The proposed temperature calibration scheme reduces the Hall sensor drift from 22% to 1% in the temperature range from -55 ˚C to 105 ˚C, corresponding to a temperature coefficient of 76 ppm/˚C. At higher frequencies, i.e. 86.22 kHz, the temperature coefficient drops to 1100 ppm/˚C due to the surface effect of the conductor and the non-linearity of the HF path readout.

Chapter 7

This thesis describes the theory and design of high speed precision magnetic sensors in CMOS processes. With multi-path and multi-sensor techniques, the prototypes presented in this research have advanced the bandwidth of state-of-the-art CMOS precision magnetic sensors by more than two orders of magnitudes.

However, all designs presented in this dissertation are proof-of concept prototypes, which still have a lot room for improvement.

In addition, the multi-sensor technique could be used to realize magnetic sensors with high resolution and high dynamic range. A conceptual system combining Hall sensors and GMR sensors is proposed to inspire future work.

Finally, this thesis is concluded with its original contributions.

Samenvatting

Deze Ph.D. dissertatie beschrijft de theorie en realisatie van breedbandige magnetische sensoren voor het gebruik in stroommetingen, die de conventionele offset- en ruisbeperkingen in CMOS processen doorbreken. Deze doorbraken worden bereikt door meerdere circuit- en systeemniveau innovaties, waaronder het gebruik van drie orthogonale rimpel reductie lussen (RRLen) in spinning-current Hall sensoren, een meerdere paden architectuur met dubbele Hall sensoren en een hybride magnetische sensorsysteem die Hall sensoren met pick-up spoelen combineert. De prototypes met deze technieken hebben de bandbreedte van state-of-the-art CMOS magnetische sensoren verbeterd met meer dan twee ordes van grootte.

Hoofdstuk 1

Stroomsensoren worden veel gebruikt in elektronische meet-, controle- en beschermingssystemen. Vanwege veiligheidsredenen in hoogspanningssystemen, worden deze vaak als magnetische sensoren geïmplementeerd, om direct contact te vermijden. De huidige industriële trends richting verbeterde veiligheid en efficiëntie zorgen voor een grotere vraag naar breedbandige sensoren. Bijvoorbeeld in hoge vermogenssystemen, waar protectiemodules een overbelasting conditie in een korte tijd, bijv. 1 μs, moeten detecteren om catastrofale schade te voorkomen. Daarnaast is de trend in state-of-the-art schakelvoedingen om de kosten te drukken door de fysieke grootte te verkleinen. Deze verkleining wordt gerealiseerd door het gebruik van kleinere passieve componenten, zoals spoelen. Om een hoge efficiëntie te behouden, moeten deze voedingen opereren boven de 1 MHz, wat weer leidt tot een behoefte aan snelle stroomsensoren.

Van alle mogelijke magnetische sensoren kunnen Hall sensoren en pick-up spoelen gefabriceerd worden in CMOS processen zonder additionele kosten. Voor beide is de bandbreedte die bereikt kan worden echter sterk afhankelijk van de ruis. Aangezien Hall sensoren in essentie weerstanden zijn, neemt hun ruisvermogen lineair toe met de bandbreedte, wat resulteert in een gedegradeerde signaalruisverhouding (SNR). Pick-up spoelen hebben een lagere gevoeligheid bij lage frequenties wat de SNR degradeert. State-of-the-art Hall sensoren en pick-up spoelen kunnen slechts een bandbreedte van respectievelijk DC tot 100 kHz en 50 kHz tot 1 MHz bereiken.

Hall sensoren en pick-up spoelen kunnen gecombineerd worden om een hoge bandbreedte te bereiken. Dit concept is gedemonstreerd op een PCB met discrete componenten. De uitdaging van CMOS integratie is echter nog niet eerder aangepakt.

Hoofdstuk 2

Als achtergrond voor dit Ph.D. onderzoek, worden in dit hoofdstuk enkele Hall sensoren en pick-up spoelen besproken. Met CMOS hall sensoren is het een uitdaging om zowel een hoge nauwkeurigheid als een hoge bandbreedte te bereiken. Dit komt primair door hun relatief hoge offset, die kan variëren van 10 mT tot 50 mT. In huidige ontwerpen wordt de offset onderdrukt door een dynamische offset reductie techniek, genaamd spinning current. Door periodiek te wisselen tussen de bias- en het uitleesrichting van een Hall sensor, kan de offset omhooggemoduleerd worden en als blokgolfrimpel op de uitgang verschijnen. Met een goede bias en uitlees strategie, kan een offset van minder dan 50 µT bereikt worden. Dit gaat echter ten kosten van de bandbreedte door de noodzaak van rimpel reductie, wat in conventioneel ontwerpen gedaan wordt met laagdoorlaatfilter (LPFs). Een hogere spinfrequentie kan dit probleem verhelpen, maar dit zorgt normaalgesproken ook voor een hogere offset door ladingsinjecties en schakeltransiënten. Om deze redenen hebben precisie CMOS Hall sensoren vaak een bandbreedte van minder dan 100 kHz.

Daarentegen worden pick-up spoelen voornamelijk gebruikt voor hoogfrequente AC magnetische veld metingen door hun differentiële karakteristiek. Voor deze toepassing worden lage kwaliteit spoelen met relatief grote bronweerstanden geprefereerd om potentiele oscillatie te voorkomen en hun uitgang wordt normaalgesproeken uitgelezen door een integrator. De state-of-the-art op spoelen gebaseerde magnetische sensoren kunnen een bandbreedte van 50 kHz tot 1 MHz bereiken.

Hoofdstuk 3

Om de offsetbeperking in breedbandige CMOS Hall sensoren op te lossen, wordt in Hoofdstuk 3 een uitleestechniek voorgesteld met drie orthogonale rimpel reductie lussen (driedubbele RRLen). Deze driedubbele RRLen meten continu de spinningrimpel van de 4-fasige spining current Hall sensor en compenseren de offset voor de versterking. Dankzij deze continue-tijd rimpelcompensatie voordat de versterking plaats vindt, staat deze techniek een spinfrequentie binnen de signaalbandbreedte toe en versoepelt het de dynamisch bereik specificaties van het uitleescircuit. Een prototype met off-chip digitale lussen bereikt een 100 kHz bandbreedte met een spinfrequentie van 1 kHz en een offset van 25 µT. De RRLen kunnen de spinningrimpel echter niet onderscheiden van een echte magnetisch signaal op de spinningfrequentie. Dit leidt tot een bandstop in de frequentieoverdracht op twee frequenties, wat kan leiden tot langzaam settle gedrag.

Hoofdstuk 4

Om het probleem van de bandstopkarakteristiek veroorzaakt door de driedubbele RRLen in de spinning current Hall sensoren op te lossen, wordt in hoofdstuk 4 de eerste meerdere-paden architectuur voor CMOS Hall sensoren voorgesteld. Hierin worden een spinning current Hall sensor met driedubbele RRLen in het laagfrequente (LF) pad gebruikt om een lage offset te bereiken. In het hoogfrequente (HF) pad wordt een non-spun Hall sensor gebruikt om de systeembandbreedte te verhogen en de bandstop frequentiekarakteristiek op te vullen. Daarnaast is het driedubbele RRL concept volledig geïntegreerd op de chip met continue-tijd integratoren. Het complete systeem heeft een bandbreedte van 400 kHz en een offset van 40 μT. De op chip RRLen verlagen de spinning rimpel van boven de 1.1 mT naar 7.3 μT, wat in lijn is met de ruis van de sensor in een bandbreedte van 300 Hz. Op het moment van publicatie is dit prototype 40 keer sneller dan de state-of-the-art CMOS precisie magnetische sensoren. De bandbreedte die dit prototype bereikt kan verder verbeterd worden door de bandbreedte van het uitleescircuit te verhogen. Dit leidt echter onherroepelijk tot meer ruis dan de huidige 272 μT_{rms}.

Hoofdstuk 5

Om de ruisbeperking in breedbandige magnetische sensoren aan te pakken, onderzoekt Hoofdstuk 5 de mogelijkheid en het ontwerp van hybride magnetische sensorsystemen, die Hall sensoren combineren met pick-up spoelen. Hall sensoren en pick-up spoelen hebben beide duidelijke SNR trends in termen van bandbreedte. In Hall sensoren neemt de SNR af als de bandbreedte toeneemt, terwijl in pick-up spoelen de SNR toeneemt als de bandbreedte toeneemt. Boven bepaalde frequenties kunnen pick-up spoelen een superieure SNR bereiken ten op zichtte van Hall sensoren. Deze frequenties is de zogenaamde crossover-frequentie, vanaf waar het systeem moet overschakelen van Hall sensoren naar pick-up spoelen voor optimale SNR.

Om deze theorie te verifiëren is een prototype chip gefabriceerd met een identieke LF pad ontwerp met spinning Hall sensor met driedubbele RRLen als in Hoofdstuk 4 en een nieuw ontworpen HF pad met pick-up spoelen. Met een gevoeligheids-trim, bereikt dit prototype hybridesysteem niet alleen een bandbreedte van 3 MHz, wat een ordergrootte beter is dan Hoofdstuk 4, maar ook een nog lagere ruis van 210 μT_{rms}. Het systeem settled binnen 400 ns (>90%) na een stapresponsie, wat naar het beste geweten van de auteur de snelst gepubliceerde CMOS magnetische sensor is. Met identieke chip oppervlak, offset en een vergelijkbaar stroomverbruik als het meerdere-paden Hall sensorsysteem in Hoofdstuk 4, doorbreekt dit hybridesysteem effectief het ontwerpcompromis tussen bandbreedte en resolutie.

De optimale crossover-frequentie vanuit een systeemperspectief varieert van het optimum vanuit sensorperspectief door de extra ruis van het uitleescircuit. Dit effect is ook geanalyseerd, door de meetresultaten van het hybrideprototype te analyseren.

Hoofdstuk 6

Het hybridesensorsysteem gedemonstreerd in Hoofdstuk 5 heeft een gevoeligheidstrim nodig om een vlakke frequentieoverdracht te bereiken. De gevoeligheid van een Hall sensor is echter behoorlijk temperatuurafhankelijk, primair door de verandering in de concentratie van de landingsdrager, en zal behoorlijk verschuiven met temperatuurveranderingen. De spanningsgevoeligheid van pick-up spoelen is daarentegen temperatuuronafhankelijk. Dit betekend dat de gevoeligheid van Hall sensoren continu gekalibreerd moeten worden om temperatuurveranderingen tegen te gaan.

In Hoofdstuk 6 wordt een gesloten lus gevoeligheidsregulatiemethode voorgesteld, gebaseerd op een common-mode referentieveld gegenereerd door op-chip spoelen. Dit maakt gebruik van het feit dat de differentiële uitleesmethode, die typisch gebruikt wordt voor stroommetingen, common-mode velden onderdrukt. Deze regeling heeft geen temperatuursensoren nodig en behoud de volledige systeem bandbreedte door de common-mode rejectie van het differentiële uitleessysteem.

Een oppervlakefficiënte implementatie van de driedubbele RRLen wordt ook voorgesteld in Hoofdstuk 6. Dit wordt bereikt door de continue-tijd integratoren te vervangen door discrete-tijd integratoren. Hierdoor kan de hardware gedeeld worden tussen de verschillende rimpel componenten.

Een prototype chip is ontworpen met het voorgestelde Hall sensor uitleescircuit in het LF pad en het ontwerp van het HF pad is overgenomen van het hybridesysteem uit Hoofdstuk 5. Het complete systeem heeft een vergelijkbare bandbreedte van 3 MHz en is bestand tegen temperatuurveranderingen. De voorgestelde temperatuurkalibratieregeling reduceert de Hall sensors uitgangverschuiving van 22% naar 1% in een temperatuurbereik van -55 ˚C tot 105 ˚C, wat overeenkomt met een temperatuurcoëfficiënt van 76 ppm/˚C. Voor hoge frequenties, bijv. 86.22 kHz, neemt de temperatuurcoëfficiënt toe tot 1100 ppm/˚C door de oppervlakte effecten van de geleider en de niet-lineariteit van het HF pad uitleescircuit.

Hoofdstuk 7

Dit proefschrift beschrijft de theorie en het ontwerp van snelle en precisie magnetische sensoren in CMOS processen. De prototypes gepresenteerd in dit onderzoek hebben de bandbreedte van state-of-the-art CMOS precisie magnetische sensoren vergroot met meer dan twee orde groottes door het gebruik va meerdere paden en meerdere sensor technieken.

Alle ontwerpen gepresenteerd in deze dissertatie zijn prototypes die het nut van de gebruikte concepten aantoont, maar nog steeds een hoop ruimte voor verbetering overhouden.

Daarnaast kunnen meerdere sensor technieken gebruikt worden om magnetische sensoren te realiseren met een hoge resolutie en een hoog dynamisch bereik. Een concept systeem dat Hall sensor en GMR sensoren combineert wordt voorgesteld voor toekomstig werk.

Tenslotte concludeert deze thesis met de originele bijdrages.

List of Publications

Journal Papers

- **J. Jiang** and K. Makinwa, "A Hybrid Multi-Path CMOS Magnetic Sensor with 76 ppm/°C Sensitivity Drift and Discrete-Time Ripple Reduction Loops," *IEEE Journal of Solid-State Circuits*, ***JSSC***, vol. 52, no. 7, pp. 1876-1884, 2017.
- **J. Jiang** and K. Makinwa, "Multi-path wide-bandwidth CMOS magnetic sensors," *IEEE Journal of Solid-State Circuits*, ***JSSC***, vol. 52, no. 1, pp. 198-209, 2017.
- **J. Jiang**, W. J. Kindt, and K. A. A. Makinwa, "A continuous-time ripple reduction technique for spinning-current Hall sensors," *IEEE Journal of Solid-State Circuits*, ***JSSC***, vol. 49, no. 7, pp. 1525-1534, 2014.

Conference Papers

- **J. Jiang** and K. Makinwa, "A hybrid multi-path CMOS magnetic sensor with 76 ppm/˚C sensitivity drift," in Proceedings of *European Solid-State Circuits Conference, **ESSCIRC**,* pp. 397-400, 2016.
- **J. Jiang** and K. Makinwa, "A hybrid multipath CMOS magnetic sensor with 210μT_{rms} resolution and 3MHz bandwidth for contactless current sensing," in the digest of technical papers, *IEEE International Solid-State Circuits Conference, **ISSCC**,* pp. 204-205, 2016.
- **J. Jiang** and K. A. A. Makinwa, "A multi-path CMOS Hall sensor with integrated ripple reduction loops," in Proceedings of *Asian Solid-State Circuits Conference, **A-SSCC***, pp. 53-56, 2015.
- **J. Jiang**, K. A. A. Makinwa and W. J. Kindt, "A continuous-time ripple reduction technique for spinning-current Hall sensors," in Proceedings of *European Solid-State Circuits Conference, **ESSCIRC,*** pp. 217-220, 2013.

About the Author

Junfeng Jiang was born in 1986 in Dalian, China. He received his B.Sc. degree in electrical engineering from Dalian University of Technology, Dalian, China, in 2009, and his M.Sc. degree in microelectronics from Delft University of Technology, Delft, the Netherlands in 2011. He expects to receive his Ph.D. degree from the same university in 2019, for his work on CMOS wide-bandwidth magnetic sensors for contactless current measurements. From 2010 to 2016, he was a visiting scholar at Texas Instruments (Formerly National Semiconductor Corporation), Delft, where he worked on CMOS wide-bandwidth magnetic sensors. From 2016 to 2017, he was with Texas Instruments Deutschland GmbH, Freising, Germany. Since November 2017, he has been with the sensing group of Texas Instruments, Dallas, USA. His interests include the design of precision analog systems, magnetic sensors and mixed-signal integrated circuits.

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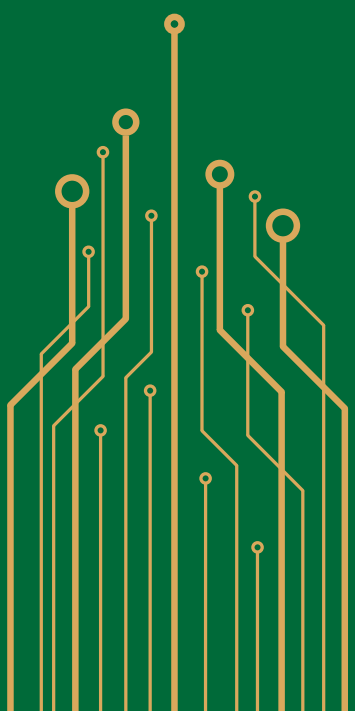
Plano, Texas, USA



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