A Hybrid-Hysteresis-CFM Control Method Recursive Switched-Capacitor DC-DC Converter with ripple reduction and load transition enhancement

By
Shuangmu Li

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Author

ShuangmuLi

Student Number

5530512

Thesis Committee Members

prof.dr. Klaas Bult
prof.dr. Kofi Makinwa
dr. Sijun Du

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Abstract

Switched-capacitor power converters (SCPCs) have emerged as promising alternatives to traditional inductive power converters due to their CMOS integration capability and configurable conversion ratios. However, challenges such as output ripple, power efficiency, and transient response have hindered their widespread adoption. This article presents a novel Hybrid Hysteresis-CFM (HHC) control strategy that effectively addresses these issues.

The HHC strategy combines the best of both worlds, integrating hysteresis control and Continuous Frequency Modulation (CFM) control. During transient moments, the system utilizes a coarse/fine frequency tuning approach to rapidly reach the target frequency. Simultaneously, hysteresis control ensures that overshoot and undershoot are kept within predefined limits, significantly reducing output ripple during load transitions.

To enhance performance and versatility, the proposed system employs a Recursive Switched Capacitor (RSC) topology with adaptive capacitor sizing and 10-phase time-interleaving. This configuration enables configurable voltage-conversion ratios (VCRs) and high power conversion efficiency (PCE) across a wide input-output range.

Experimental results validate the effectiveness of the HHC SCPC. It demonstrates minimal overshoot and undershoot during load transition, maintains a low output voltage ripple during steady-state operation, and achieves high PCE. Comparative analysis with state-of-the-art DC-DC converters underscores the superior performance of the proposed system.

In summary, the Hybrid Hysteresis-CFM (HHC) control strategy offers a promising solution to enhance the capabilities of switched-capacitor power converters. Its ability to address output ripple, power efficiency, and transient response challenges makes it a valuable innovation for diverse applications requiring efficient power conversion.

1 Introduction

In the present era of rapid advancements in electronic technology, achieving an efficient conversion from a direct current (DC) input voltage to a stable DC output voltage is a pivotal objective for electronic systems. DC-DC converters, often referred to as voltage regulators or voltage converters, assume a pivotal role in realizing these objectives. They play a crucial and indispensable role in attaining these goals and are extensively embraced within the modern electronic industrial sector. This widespread adoption stems from their ability to facilitate flexible and efficient voltage conversion, ensuring a stable and reliable power supply for electronic systems.

1.1 DC-DC converter category

Within the expansive realm of DC-DC converters, a diverse array of converter types exists. These types are differentiated based on the types of devices employed, and among them, the most frequently utilized ones can be categorized as follows: linear regulators, inductor-based switched-mode power converters (SMPC) and switched-capacitor power converters (SCPC). Each of these converter categories will be individually introduced in the subsequent sub-sections.

1.1.1 Linear regulator

Linear regulator is an essential part of the power management system that provides constant voltage supply for electronic devices. It regulates the output voltage by utilizing elements such as voltage regulators, feedback circuits and stabilizers to maintain the output voltage at a stable value and dissipating the difference between the input and regulated voltages as waste heat.

In contrast to switching mode DC-DC regulators, linear regulators offer distinct advantages, one noteworthy benefit is the absence of switching noise as no switching activity in the system. Consequently, linear regulators provide a relatively clean power source for the electronic devices, however, as illustrated previously, the linear regulator dissipates

the voltage difference between input and output thus limit the efficiency and always need a higher voltage level as input.

A subset of linear regulators, the Low Dropout Regulator (LDO), offers specific advantages. It requires a lower voltage difference between the input voltage and output voltage in comparison to standard linear regulators, thus can regulate the output voltage even when the supply voltage is very close to the output voltage. The LDO configuration comprises a power MOSFET and an error amplifier, as depicted in Fig .1. This distinct attribute of LDOs makes them particularly advantageous in scenarios where precise and stable voltage regulation is required, even under conditions of minimal voltage discrepancy. The regulation is achieved through a feedback circuit that the error amplifier

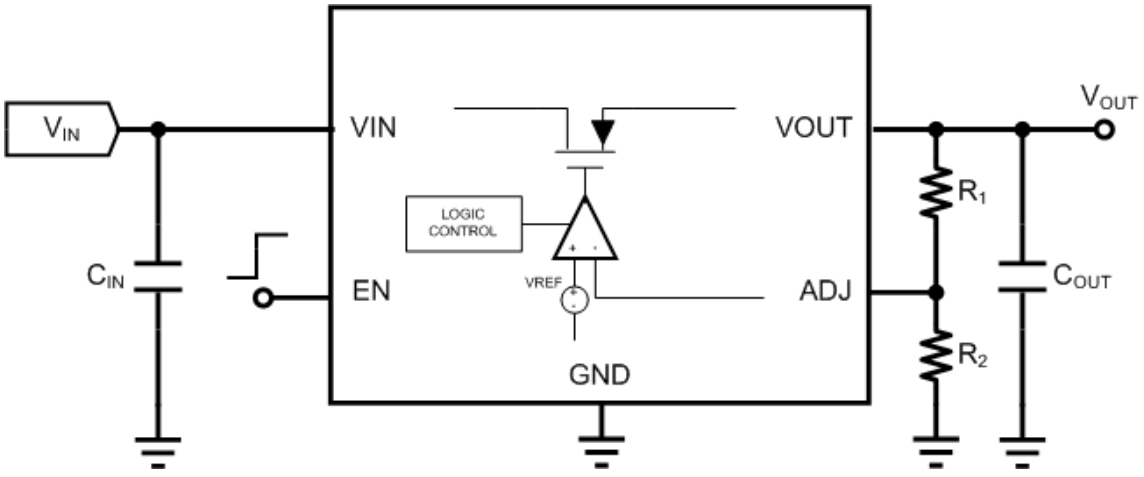

Figure 1: Linear regulator

controls the voltage drop across the power MOSFET in saturation regions through comparison between the difference of the reference voltage and fraction of the output voltage. For the circuit illustrated in Fig.1, the regulated output can be mathematically expressed as:

$$V_{out} = (1 + \frac{R_1}{R_2})V_{ref} \tag{1}$$

The LDO shares similarities with the linear regulator, benefits from easy integration. However, it also encounters a common challenge that the energy efficiency is quantified by $\eta = V_{out}/V_{in}$. This characteristic may not align with the demands of applications

for System on Chip (SoC), Internet of Things (IoT) and wireless scenarios which have strict requirements for battery life and power consumption. Moreover, this feature may be unsuited for implementations involving Dynamic Voltage Scaling (DVS) techniques which is a prevalent strategy embraced within SoC, IoT and wireless applications that reduce power consumption by adjusting voltage levels in correspondence with different operating modes.

1.1.2 Inductor-based DC-DC converter

Given the important role of power efficiency in DC-DC converters, addressing the efficiency concerns of the linear regulator led to the utilization of switching mode DC-DC regulators which use energy storage components to achieve efficient conversion. Inductor, as one of the most common energy storage element paved the way for the design of inductor-based DC-DC converters, which is implemented with switch (Power MOSFET), inductor, and control circuit as shown in Fig.2. The inductor-based DC-DC converter control the flow of energy through the inductor by manipulating the switch and regulate the output voltage by finely tuning the duty cycle of the switch's on-state, which can be mathematically expressed as:

$$V_{out} = DV_{in} \tag{2}$$

Where D represent the duty cycle of the switch's on-stat. The inductor-based DC-DC converter presents an efficient energy conversion approach by controlling energy storage and release through the inductor rather than heat dissipation. Meanwhile, this type of converter offers easy control which ensure a stable output voltage even during load transitions, the output voltage can be always maintained within acceptable range to offer a stable power rail for electronic devices. Nevertheless, the integration of inductor-based DC-DC converters faces limitations due to the utilization of inductor component. This restriction becomes particularly significant in applications in IoT, SoC and wireless scenario with the demands on volume and weight. Moreover, further increasing conversion efficiency can lead to challenges in terms of manufacturing costs since employing high-quality factor inductors may be necessary which will further increase the manufacturing

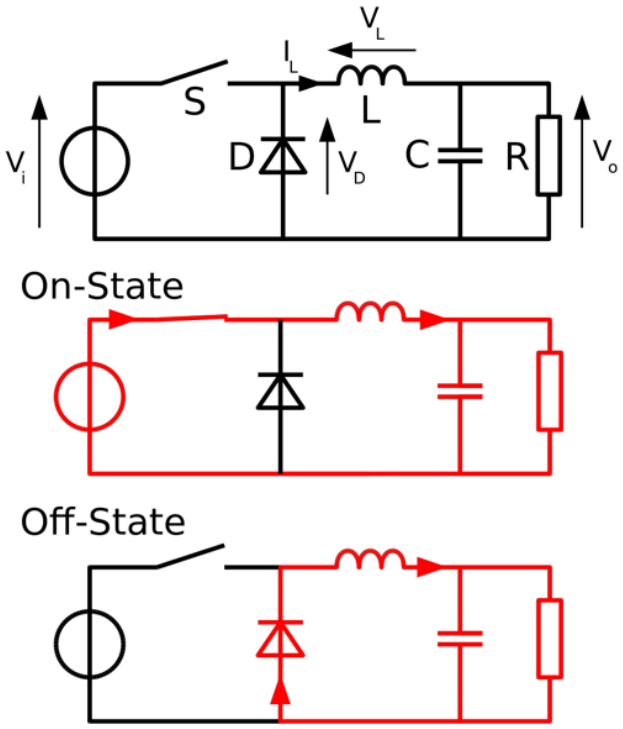

Figure 2: Inductor-based DC-DC converter

expense and be unsuited for integrated circuit application [3] .

1.1.3 Switched-capacitor DC-DC converter

As another energy storage component, capacitor is used in Switched-Capacitor (SC) DC-DC converters to achieve efficient energy conversion. This type of converter offers unique advantages in terms of simplicity, versatility and high-frequency operation.

Fundamentally, the SC DC-DC converters transfer and store the electrical energy by controlling the alternate connection and disconnection of capacitors from input and output voltage. A straightforward example of this principle is shown through a Dickson-type 2:1 step-down converter, depicted in Fig.3. Through manipulation of capacitor configurations, this converter can effectively attain the desired output voltage level.

SC DC-DC converters leverage a network of switches and capacitors to redistribute the electric charge across distinct nodes. This dynamic process enables a configurable conversion ratio based on different SC topology. This feature can be suitable for applications

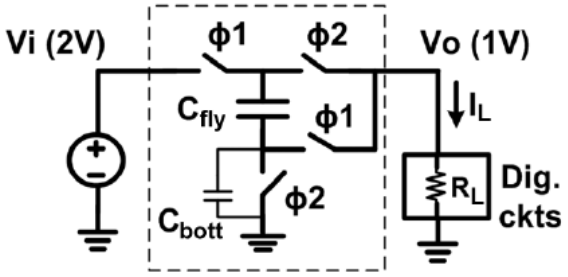

Figure 3: Dickson 2:1 step-down converter [12].

in IoT, SoC and wireless scenario which demands on versatile conversion capabilities by reconstructing different networks of SC DC-DC converters.

Moreover, the inherent characteristics of SC DC-DC converters make them remarkably well-suited for application with space constraints due to its high level of integration, at the same time, SC converters can handle a wide range of input and output voltage levels, making them versatile for various voltage conversion requirements. Furthermore, the control method of SC converters is straight forward due to their inherent first-order system behavior within the power stage. This feature contribute to ease of implementation and management. Thus, these advantages make SC converters one of top choices for on-chip DC-DC converters in IoT, SoC and wireless systems.

1.2 SC DC-DC converter topology

As previously discussed, SC DC-DC converters employ a dedicated arrangement of capacitors and switches to realize voltage conversion. Thus, the topology of SC converters is an important aspect which define the configuration of these components to achieve desired output voltage level from a given input voltage. In the subsequent section, several prevalent SC converter topology will be introduced, each designed for specific voltage conversion applications.

1.2.1 Series Parallel SC converter

The Series Parallel SC converter stands as one of the prevailing topologies in SC DC-DC converter. This topology has a straightforward configuration. An example for step-down conversion is shown in Fig.4. During the charging phase, capacitors are arranged in a series connection between the input voltage V_{in} and output voltage V_{out}. In discharging phase, these capacitors are reconfigured into a parallel connection with V_{out}.

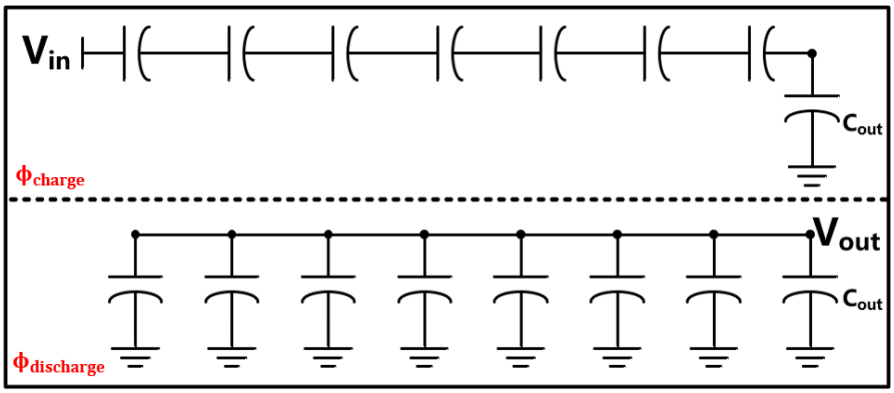

Figure 4: Series Parallel SC converter

This topology minimize the voltage drop across capacitors and alleviate current stress. However, one of the notable drawback of this topology is that it requires a large number of capacitors, furthermore, it is applicable only for conversion ratios of the form M=1/Q or M=P/1, where M represents the conversion ratio. Despite these limitations, the Series-Parallel SC converter continues to be a good choice due to its simple structure and its efficacy in managing voltage and current stresses. It is suitable for scenarios necessitating specific conversion ratios.

1.2.2 Dickson SC converter

The Dickson SC DC-DC converter achieve the desired conversion ratio through transfer of charge between distinct components. A step-down conversion example is shown in Fig.5. During operation cycle, charges are successively moved from the input voltage

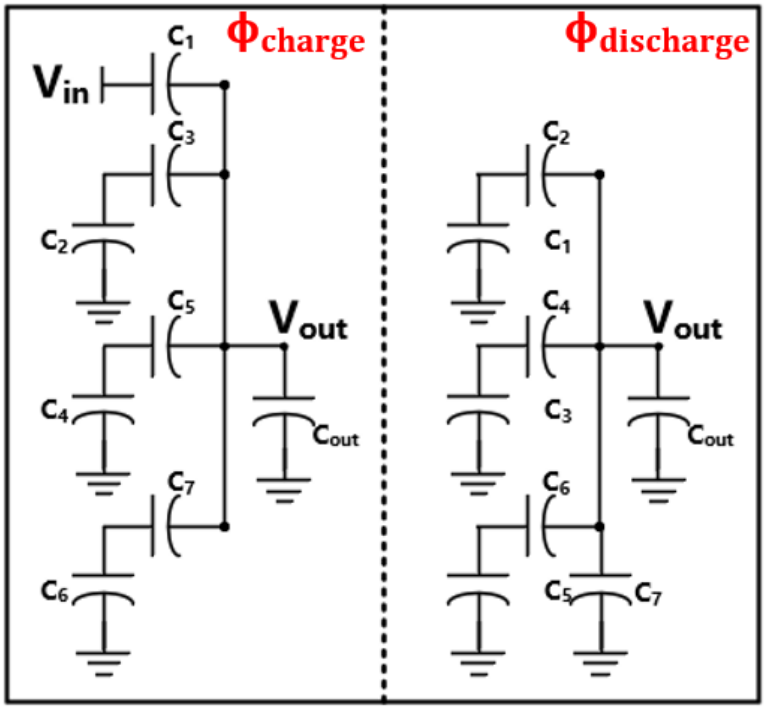

Figure 5: Dickson SC converter

V_{in} to C_1, followed by a transfer from C_1 to C_2, and so forth. This sequence is repeated through the remaining components.

In comparison to the Series-Parallel topology, Dickson topology stands out for its versatility in achieving a wide range of conversion ratios. This flexibility arises from the fact that the normalized voltage across capacitors in Dickson converters assumes values of 1, 2, ..., (Q-1)/Q, thereby accommodating various conversion scenarios. Additionally, this topology can minimize voltage stress on power switches.

Nevertheless, it is important to acknowledge that the Dickson SC DC-DC converter shares the requirement for a significant number of capacitors, similar to the Series-Parallel configuration. While offering advantages in terms of flexibility and reduced voltage stress, the Dickson topology may not align seamlessly with applications prioritizing power density due to the substantial capacitor count involved.

Despite this limitation, the Dickson-type SC DC-DC converter persists as an attractive choice for its capacity to achieve diverse conversion ratios while mitigating voltage stress,

albeit necessitating careful consideration within the context of specific power density requirements.

1.2.3 Recursive SC converter

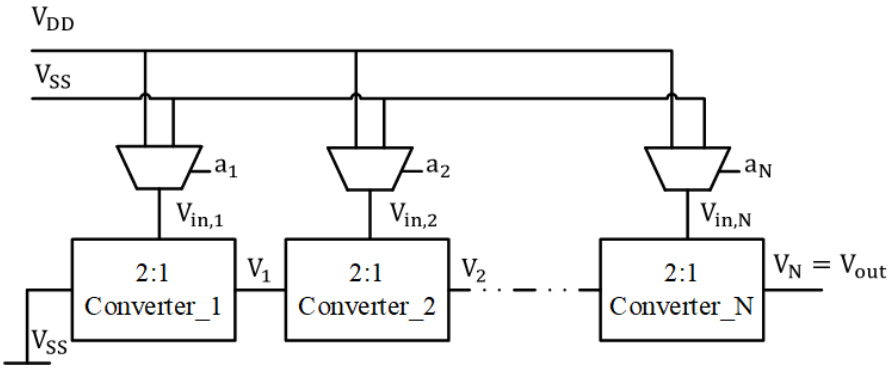

Figure 6: Recursive SC [17]

The recursive SC DC-DC converter presents a modular approach achieve through the series connection of identical power cells with conversion ratio M_{cell}. In 2014, Loai et al. [17] introduced a novel RSC topology as depicted in Fig.6 that enables reconfiguration among $(2^N - 1)$ conversion ratios through a cascaded N stages 2:1 SC cells. This innovative design offers the advantage of reducing the number of required capacitors and enables straightforward implementation due to its practical modular structure. In the RSC DC-DC converter, each 2:1 SC stage is supplied with one input from preceding stage and another input from either V_{DD} or V_{SS}, thus, this configuration results in a binary conversion ratio, expresses as:

$$\frac{V_{out}}{V_{in}} = \frac{A}{2^N} \tag{3}$$

The RSC DC-DC converter offers the distinct advantage of minimizing hardware overhead and facilitating straightforward tuning to attain various conversion ratios. Although it is limited to providing binary conversion ratios rather than arbitrary ones, it remains a viable and uncomplicated choice for expanding the input and output voltage ranges. Meanwhile, it provide a much simpler design method.

1.3 SC DC-DC converter control strategy

To a certain extent, the study of the SC DC-DC converter topology structure is an optimization of SC efficiency for different conversion ratio which will be further discussed in chapter 2. However, in the research area of DC-DC converters, considerations extend beyond conversion efficiency. Control methodologies play an important role in shaping performance metrics, including output voltage ripple, load regulation, startup time, transient response time, overshoot, and undershoot. In the following section, several conventional control method will be introduced, along with some states of art control method that optimize the transient behavior of DC-DC converters.

1.3.1 Hysteresis control method

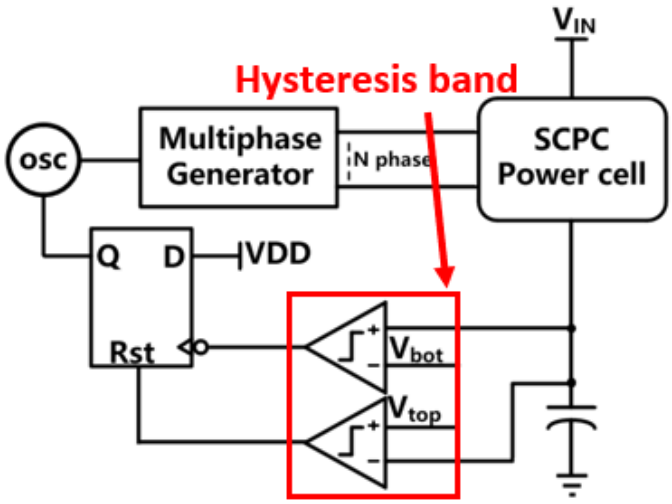

Figure 7: Hysteresis control loop

Hysteresis control often referred to as double boundary hysteresis control, serves as a dynamic regulation technique employed in SC converters to enhance their overall performance, stability, and transient response [14]. It is one of the most widely employed control methods due to its inherent stability and rapid transient response. The simplified structural block diagram of hysteresis control method is illustrated in Fig.7, which is straightforward, consisting of two comparators and an oscillator (OSC). The waveform

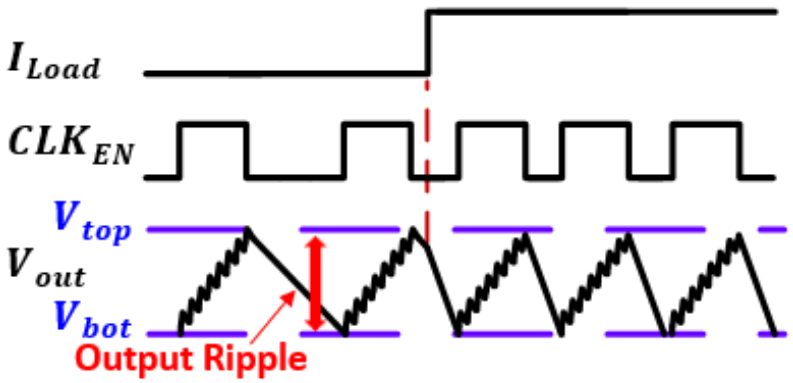

Figure 8: Hysteresis control transient waveform

for hysteresis control is depicted in Fig.8.

Hysteresis control introduces a predefined hysteresis band around the desired output voltage through two comparator which defines V_{top} and V_{bot} respectively. When the output voltage crosses the upper or lower threshold of this hysteresis band, the control circuit responds by initiating the appropriate switching action to bring the output voltage back within the desired range. Through the waveform analysis, this method has no transient state during load transition, however, the output ripple is determined by the hysteresis window and is closely related to the output capacitor [7]. The lower output ripple will necessitate increased capacitance thus leads to power density degradation, otherwise, it will leads to performance degradation of the sensitive system. Consequently, this control method may not be suitable for applications in IoT, SoC and wireless systems.

1.3.2 Pulse skipping control method

The pulse skipping control method, also referred to as single boundary hysteresis control [21], compared with double boundary hysteresis control, it regulated the output voltage with only one voltage boundary. The simplified structural block diagram of pulse skipping control method is depicted in Fig.9, while the waveform which illustrate the performance in transient state and steady state is presented in Fig.10. Similar to double boundary hystersis control, this approach also has inherent stability and fast transient response, and it has less output ripple compared with double boundary hystersis control.

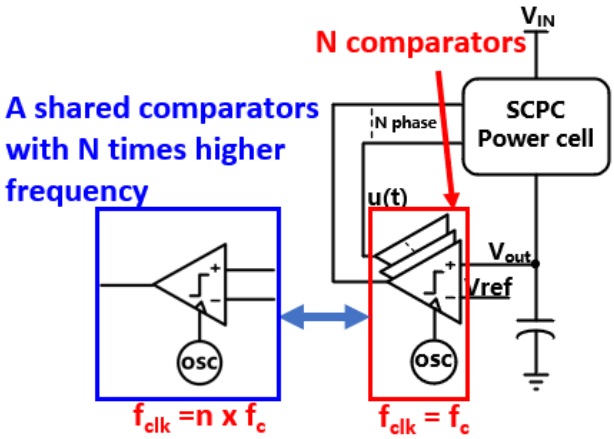

Figure 9: Pulse skipping control loop

However, the pulse skipping control method requires either N comparators for N phase channels or a comparator with a clock speed N times faster for N phase channels [6], if the SCPC employs a multi-phase time-interleaving technique, which will be further discussed in Chapter 2. This will further increase the hardware overhead as well as the power consumption which is not suitable for energy restricted system.

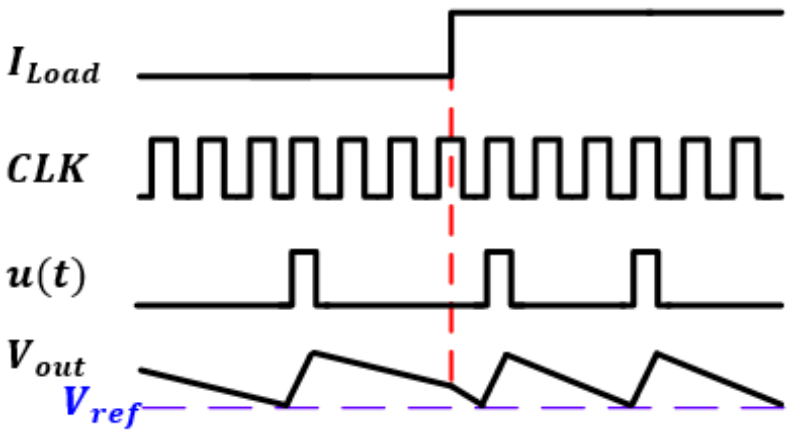

Figure 10: Pulse skipping control transient waveform

1.3.3 Continuous frequency modulation

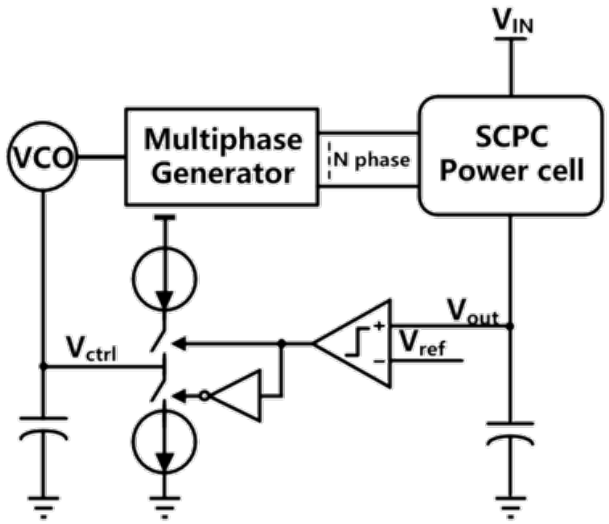

Figure 11: CFM control loop

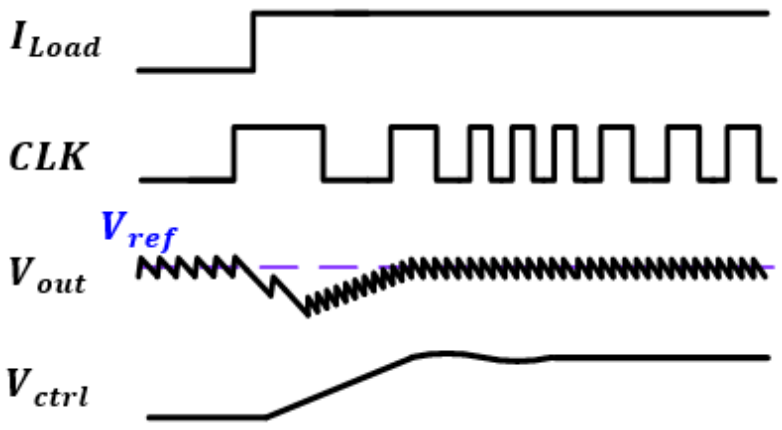

Figure 12: CFM transient waveform

Continuous frequency modulation (CFM) is another dynamic control techniques employed in SC converters. It is designed to optimize the regulation performance and efficiency under varying load conditions. This control method regulates the switching

frequency of the converter in real time to achieve voltage regulation and reduce output voltage ripple. It also can enhance overall efficiency due to its simple structure.

Notably, CFM control has tremendous superiority in minimal output voltage ripple among the control methods. Meanwhile, the use of VCO which typically based on ring oscillator architecture makes the CFM control aligns well with multi-phase time-interleaving technique which will further reduce the output ripple.

A typical CFM control loop structure is depicted in Fig.11, while the waveform illustrate CFM control in steady state and transient state is depicted in Fig.12. The switching frequency is regulated based on the feedback from the output voltage through a charge pump-based integrator. This ensures optimal performance across varying condition. At the same time, by combining with multi-phase time-interleaving, the CFM can achieve faster load transient response as the control loop respond at every phase that is a fraction of the switching period. However, the response speed of the CFM control is still limited by gain bandwidth product of the control loop, thus, it may relatively slower compared to preceding control methods. This will leads to problems with overshoot, undershoot and long response time during load transition [6] [11] [20]. In applications for IoT, SoC and wireless scenarios, multi-core systems will cause large and frequently varying current which will lead to crucial requirements for the transient behavior of DC-DC converters. Thus, CFM control still requires refinement to address these concerns.

1.3.4 State of Art: CFM control with bypass path speed up

Despite its transient response limitations, CFM control maintains a relatively advantageous position among control methods due to its overall efficiency enhancement and minimal output voltage ripple. In 2013, Le et al. [11] proposed an extra bypass path to speed up the load transition recovery as illustrated in Fig.13. This bypass path use an extra comparator, detecting a lower voltage boundary and activating when a load current transition occurs from light to heavy loads, then the VCO is set to its maximum frequency to expedite the transition from light to heavy loads.

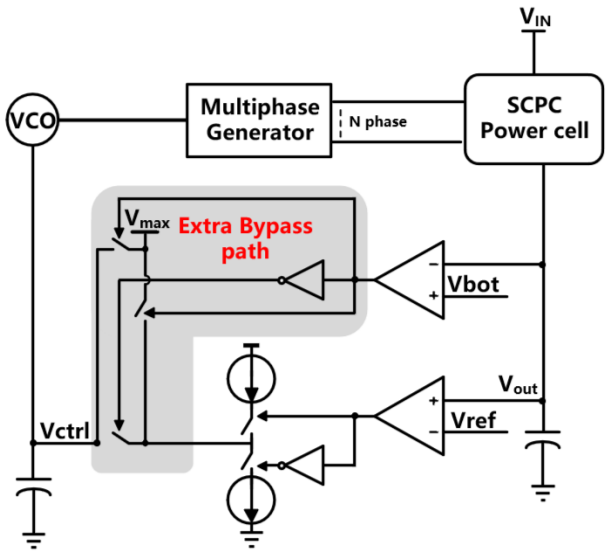

Figure 13: CFM control with bypass path speed up

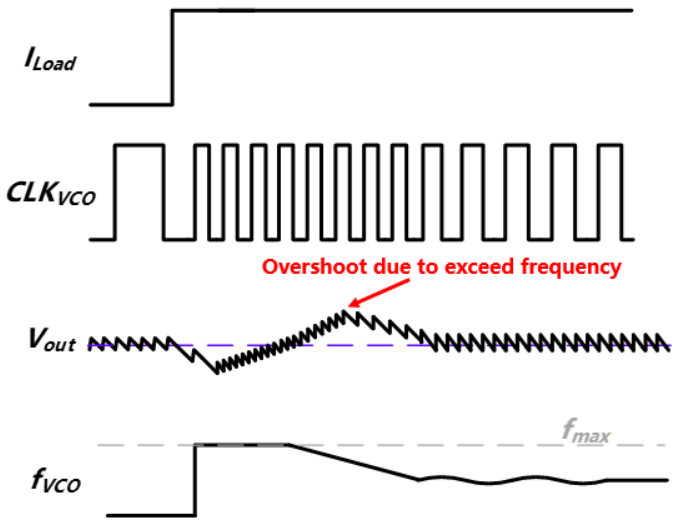

Figure 14: waveform of CFM control with bypass path speed up

However, this bypass path approach has limitations. It is incapable of addressing transitions from heavy to light loads. Furthermore, it introduces the potential for new overshoot issues during transitions from light to moderate loads, as depicted in Fig.14. This suggests that while the bypass path does accelerate specific load transitions, it doesn't offer a

comprehensive solution and may introduce new challenges.

1.3.5 State of Art: CFM control with segmented frequency modulation and multi-phase co-work

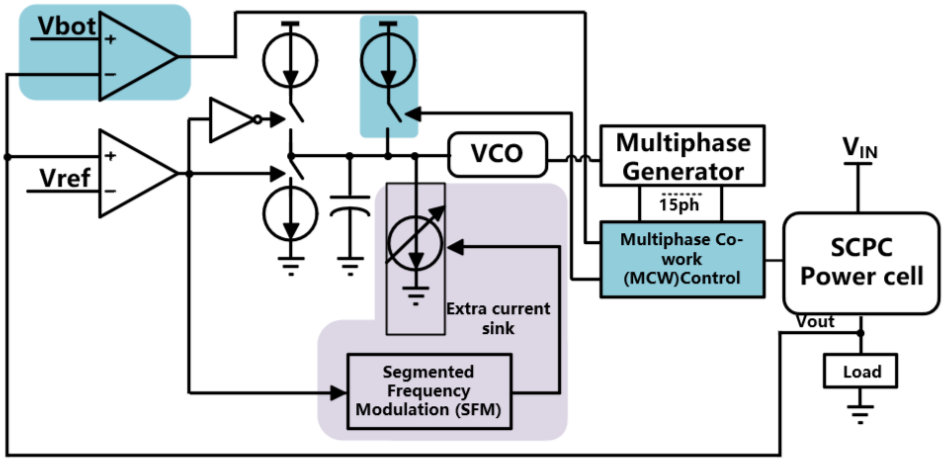

Figure 15: Circuitry of SC DC-DC converter in [6]

To overcome the limitations of the previous state of art control method. A new CFM control system was proposed by Chio et al. in 2019 [6], as depicted in Fig.15. This innovative approach employs different strategies for load transitions. When heavy load to light load transition occurs, the comparator will trigger the segmented frequency modulation loop, with extra current sink to speed up the integration, the response time can be decreased. This mechanism effectively shortens the transient response time.

When light load to heavy load transition occurs, the system will synchronize the selected interleaving multi-phase SC channels to provide a larger pumped charge per time which can be also seen as a larger energy step to speed up the voltage recovery.

Despite these improvements leads to a faster recovery time for the CFM loop, the issue of overshoot and undershoot remains. These still exceed permissible levels, reaching around 200mV. This can potentially impact the lifespan of the electronic devices as the maximum allowed overshoot duration for device is limited, thus, further improvement is

still required.

1.4 Research Question

SC DC-DC converter stands out as a strong competitor among the DC-DC converters, at the same time, Adopting a suitable SC topology, Multi-VCR can be achieved to effectively addressing multi-power supply requirements, mitigating battery degradation issues, and extending batter lifespan, thus can be suitable for IoT, SoC and wireless systems. However, for DC-DC converters, the transient behaviour is also a crucial characteristic that requires further research.

Conventional control methods each possess distinct strengths and limitations. Due to the advantages in enhanced overall efficiency and lowest output voltage ripple, CFM control is a good option however suffers from the transient behaviour. To address these concerns, this thesis proposed a Hybrid-Hysteresis-CFM (HHC) control approach, by combining the advantages of hysteresis control and CFM control, the proposed method aims to achieve minimal votlage undershoot or overshoot during transients, which also maintaining the lowest output voltage ripple during steady-state operation.

Furthermore, this thesis adopted the RSC topology to enable configurable conversion ratio. The RSC topology not only excels in power density and hardware overhead but also enables multiple conversion ratios, at the same time, it increases the input and output range. Therefore, the universality of the proposed control strategy is concurrently substantiated.

The proposed DC-DC converter has been meticulously designed and fabricated using a 180nm BCD TSMC process, occupying a compact $2.89mm^2$ active area. The measurement results underscore the superiority of the proposed control strategy. It achieves a lowest overshoot and undershoot with a large load transition among the comparison table, furthermore, it achieve a minimum steady state output ripple due to CFM control.

1.5 Thesis Outline

This article is organized as follows:

Chapter 2 explains the operation principle of the proposed system, the energy loss mechanism, and the power transfer efficiency.

Chapter 3 illustrates the proposed HHC control system and the implementation of the RSC power core.

Chapter 4 introduces several key blocks of circuit implementation and power cell implementation.

Chapter 5 provides measurement results for the implemented design with emphasis on the load transient, efficiency, and system performance. The performance of this design is also compared with state-of-the-art DC-DC converters.

Chapter 6 illustrates the conclusions and gives some valuable ideas of this design to get futher improved in the future

2 Operation Principle

2.1 2:1 SC DC-DC power stage analysis

In this section, a 2:1 SC DC-DC power stage, as depicted in Fig.16, is utilized for the analysis of the SCPC power stage. It consists of a flying capacitor C_{fly} and four power switches with on resistances R_{on} [1]. Theoretically, the output will include an output capacitor acting as a buffer capacitor, which functions as a low-pass filter to reduce voltage ripple and stabilize the output voltage.

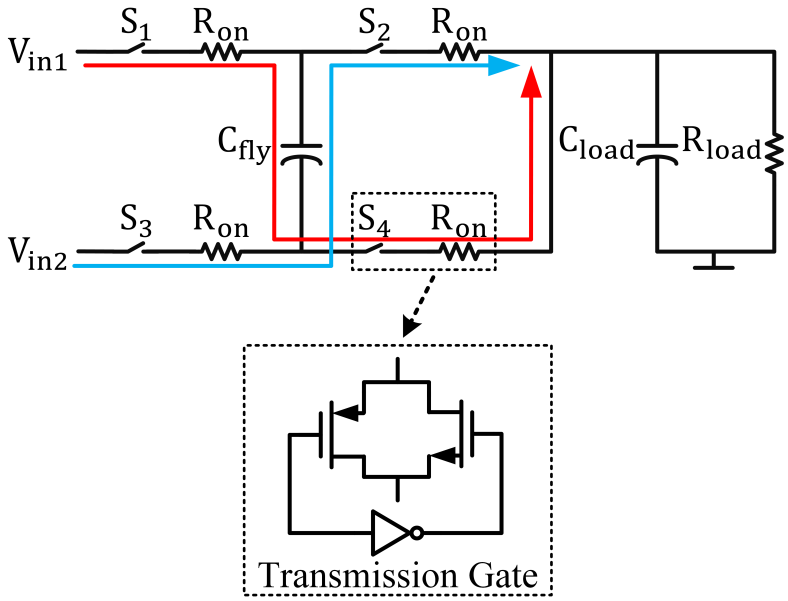

Figure 16: One 2:1 converter cell.

2.1.1 2:1 SC DC-DC power stage working principle analysis

The flying capacitor depicted in Fig.16 dynamically alternates between two operational phases: the charge phase and the discharge phase [3].

During the charging phase, the current flows through the red path in Fig.16. In this configuration, the flying capacitor, denoted as C_{fly}, is in series connection with the output

capacitor, and C_{fly} will be charged up. This process can be expressed as:

$$V_{C1} = V_{in1} - V_{out} \tag{4}$$

During the discharging phase, the current flows through the blue path in Fig.16. The flying capacitor will be in parallel connection with the output capacitor, and then the flying capacitor will be discharged down. This process can be expressed as:

$$V_{C2} = V_{out} - V_{in2} \tag{5}$$

Ideally, if there is no load current (meaning no charge flows through C_{fly}), V_{C1} should be equal to V_{C2}, resulting in an ideal conversion ratio. This can be derived by combining Eq.4 and Eq.5, expressed as:

$$V_{out} = \frac{1}{2}(V_{in1} + V_{in2}) \tag{6}$$

2.1.2 Average model

In practical, the energy stored in C_{fly} will be dissipated due to the on resistance of the power switch and the charge sharing loss during the charging and discharging process. To provide a more realistic representation of the system's behavior, accounting for the aforementioned energy losses, the average model for SC DC-DC converter is proposed as shown in Fig.17 The average model contains an ideal transformer with fixed-conversion

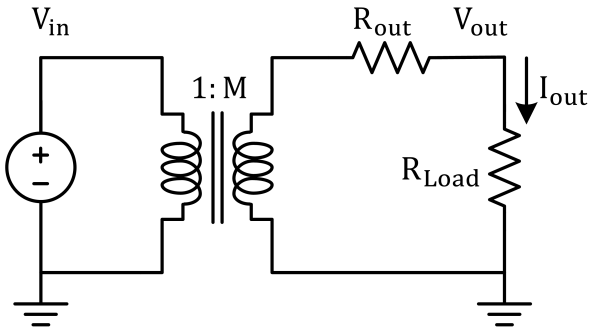

Figure 17: Average Model

ratio along with an equivalent output resistance. Mathematically, the average model can be expressed as

$$V_{out} = MV_{in} - R_{out}I_{load} \tag{7}$$

Where M is the ideal conversion ratio and is determined by the circuit configuration. The equivalent output impedance directly reflects the efficiency of the converter [13] [15] which includes the conduction loss and the charge sharing loss and will be analysed in detail as following.

2.1.3 Analysis of Output Impedance

Fundamentally, the SC converter perform voltage conversion by charging and discharging capacitors. Therefore, the charging process and discharging process are intricately tied to the circuit's time constant. Depending on the switching frequency of the circuit, the converter can be divided into two asymptotic operating regions: the fast switching limit region (FSL) and slow switching limit region (SSL) [18] [19]. These regions describe the converter's behavior under distinct switching frequency regimes.

To analyze the output impedance, a charge flow analysis can be conducted to gain insight into the average model, which is illustrated as Fig.18.

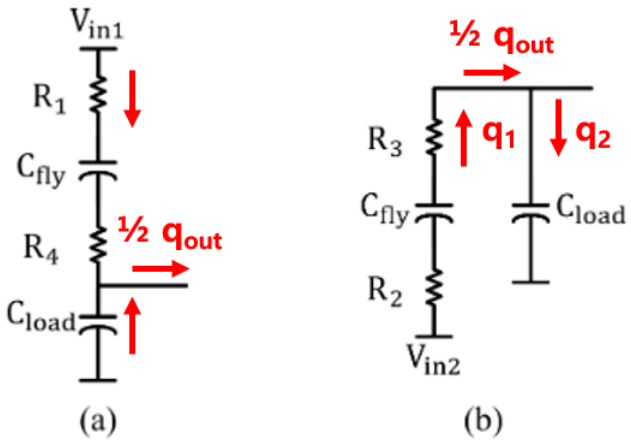

Figure 18: (a) Charge Flow of Charging Phase, (b) Charge Flow of Discharging Phase.

In a conventional 2:1 SC DC-DC converter, the charge flowing to the output during both the charging and discharging phases is equal to $0.5q_{out}$.The charge flowing through flying capacitor C_{fly} and the load capacitor C_{load} is q_1 and q_2 respectively. In the charging phase plotted in Fig.18(a), the input V_{in1} charges these two capacitors and also contributes

some charge to the output. This relationship can be expressed as Eq.(8).

$$q_{in} = q_1 = \frac{1}{2} q_{out} - q_2 \tag{8}$$

In steady state, the charge flowing through each of the capacitors must be of equal magnitude but opposite directions in different clock phase. That means in discharging phase as shown in Fig.18(b), both C_{fly} and C_{load} will contribute charge to the output. The relationship can be expressed as Eq.(9).

$$\frac{1}{2} q_{out} = q_1 - q_2 \tag{9}$$

As a result, the charge stored and released in the flying capcitor can be easily obtained as Eq.(10).

$$q_1 = \frac{1}{2} q_{out} = q_{in} \tag{10}$$

When the switching frequency f_s is sufficiently high that the phase time is much smaller than the time constant τ, the circuit operates in fast switching limit. In this case, the conduction loss predominantly contributes to energy loss as the voltage across C_{fly} can be considered as a constant value. The condition for FSL operation can be expressed as Eq.11

$$\phi_1 = \phi_2 = \frac{1}{2} T = \frac{1}{2} \frac{1}{f_s} \ll \tau \tag{11}$$

The time constant τ can be calculated as the product of the effective resistance R_{eff} and the effective capacitance C_{eff}:

$$\begin{aligned} \tau &= R_{eff} C_{eff} \\ &= (R_1 + R_4) C_{fly} \\ or &= (R_2 + R_3) C_{fly} \end{aligned} \tag{12}$$

The energy consumption of each on resistor of the power switch can be represented as Eq.(13), and the total energy loss $E_{T,FSL}$ caused by the conduction loss is calculated as Eq.(14).

$$E_{FSL} = I_i^2 R_i T_i = R_i \frac{q_i^2}{T_i} \tag{13}$$

$$\begin{aligned} E_{T,FSL} &= \sum_{i=1}^{n} E_{FSL} \\ &= \sum_{i=1}^{4} R_i \frac{q_i^2}{T_i} \\ &= \frac{q_{out}^2}{2T}(R_1+R_2+R_3+R_4) \end{aligned} \tag{14}$$

$$\begin{aligned} P_{R_{SW}} &= \frac{E_{T,FSL}}{T} \\ &= \frac{q_{out}^2}{2T^2}(R_1+R_2+R_3+R_4) \\ &= \frac{1}{2}(R_1+R_2+R_3+R_4)I_{out}^2 \\ &= R_{FSL}I_{out}^2 \end{aligned} \tag{15}$$

Thus, the equivalent output impedance during FSL operation can be expressed as

$$R_{FSL} = 1/2(R_1+R_2+R_3+R_4) = 2R_{on} \tag{16}$$

When the switching frequency is sufficiently low that the flying capacitor is fully charged and discharged, the converter works in SSL region. In this case, the predominant power loss arises from charging sharing loss. To elucidate this phenomenon, assuming charging a capacitor from a initial voltage V_0 to V_1, the voltage expression of the capacitor V_C can be defined as Eq.(17). [9] [16]

$$V_C(t) = V_0 + (V_1 - V_0)(1 - e^{\frac{-t}{R_{ESR}C}}) \tag{17}$$

The corresponding current $I(t)$, through the capacitor during this process is given by:

$$I(t) = C\frac{dV_C(t)}{dt} = (V_1 - V_0)\frac{1}{R_{ESR}}e^{\frac{-t}{R_{ESR}C}} \tag{18}$$

Where the R_{ESR} is the equivalent series resistance including the on resistance of the power switch as shown in Fig.19. The resulting power loss P_{cap} during both charging and discharging phase emerges due to the conduction loss of the equivalent series resistance R_{ESR} which can be calculated as Eq.(19).

$$P_{Cap} = I^2(t)R = (V_1 - V_0)^2\frac{1}{R_{ESR}}e^{\frac{-2t}{R_{ESR}C}} \tag{19}$$

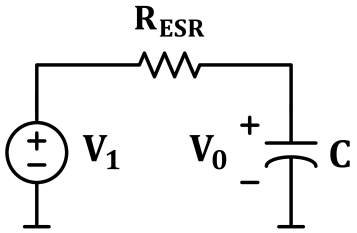

Figure 19: Equivalent series resistance of the capacitor.

The energy loss, E_{Cap}, incurred during these processes can be determined by integrating the power over time, yielding:

$$E_{Cap} = \int_0^{\infty} Pdt = \frac{1}{2}C(V_1 - V_0)^2 = \frac{1}{2}C\Delta V^2 \tag{20}$$

As discussed previously, the charge flowing through the capacitor in two phases are same magnitude but opposite direction, the charge flowing through the capacitor q_i results in the voltage change of the capacitor ΔV as $q_i = C_i\Delta V$. If substituting the relationship equation between q_i and ΔV to the expression of $E_{C_{fly}}$, the energy loss during a half-cycle $E_{C_{fly},\phi}$ can be simplified as Eq.(21).

$$E_{Cap,\phi} = \frac{q_i^2}{2C_i} \tag{21}$$

With this analysis, the energy loss of each capacitor during 2 phases can be expressed as Eq.(22). Because there is only one flying capacitor in this 2:1 converter topology, so the total energy loss $E_{T,SSL}$ can be calculated as Eq.(23).

$$E_{SSL} = E_{Cap,\phi 1} + E_{Cap,\phi 2} = \frac{q_i^2}{C_i} \tag{22}$$

$$E_{T,SSL} = \sum_{i=1}^{n} E_{SSL} = \sum_{i=1}^{1} \frac{q_i^2}{C_i} = \frac{q_{out}^2}{4C_{fly}} \tag{23}$$

$$P_{C_{fly}} = \frac{E_{T,SSL}}{T} = \frac{1}{4f_sC_{fly}}I_{out}^2 = R_{SSL}I_{out}^2 \tag{24}$$

Therefore, the equivalent output impedance of SSL mode can be calculated as R_{SSL} in Eq.(25), which depends on the switching frequency f_s and fly capacitance C_{fly}.

$$R_{SSL} = \frac{1}{4 f_s C_{fly}} \tag{25}$$

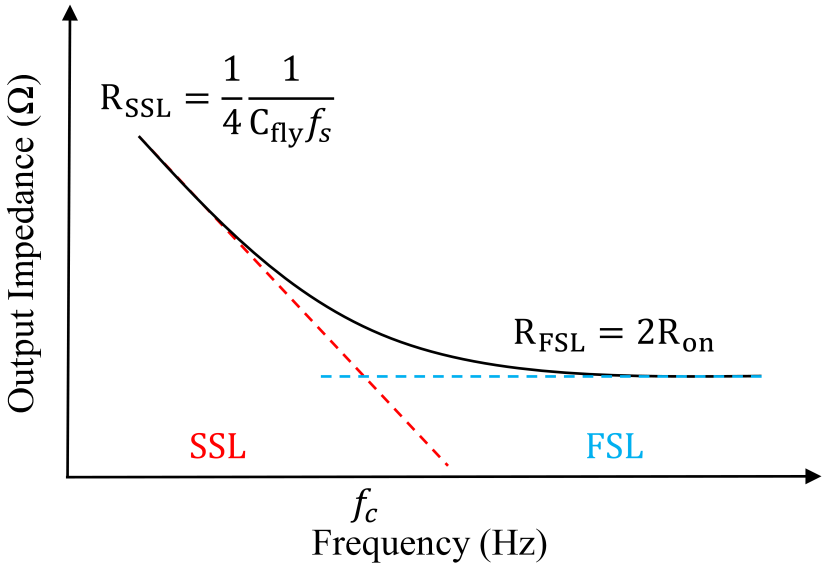

Figure 20: Output Impedance vs Switching Frequency f_s.

The Fig.20, illustrates the relationship between the equivalent output impedance R_{out} and the switching frequency f_s. Conventionally, when designing SC converters, the power switch size is set to make the FSL impedance equal to the SSL impedance at the maximum switching frequency, often referred to as the corner frequency f_c. This design approach ensures optimal performance across the entire frequency range.

$$f_c = \frac{1}{8 C_{fly} R_{on}} \tag{26}$$

The total equivalent output impedance of the converter thus can be expressed as:

$$R_{eq} = \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{27}$$

2.1.4 Switching Loss

In practical circuit implementations, in addition to the conduction loss and charge sharing loss discussed previously, another significant source of power loss is switching loss which includes both bottom plate loss $P_{bot-cap}$ and gate-driving loss P_{driver}.

$$P_{Switching} = P_{bott,cap} + P_{driver} \tag{28}$$

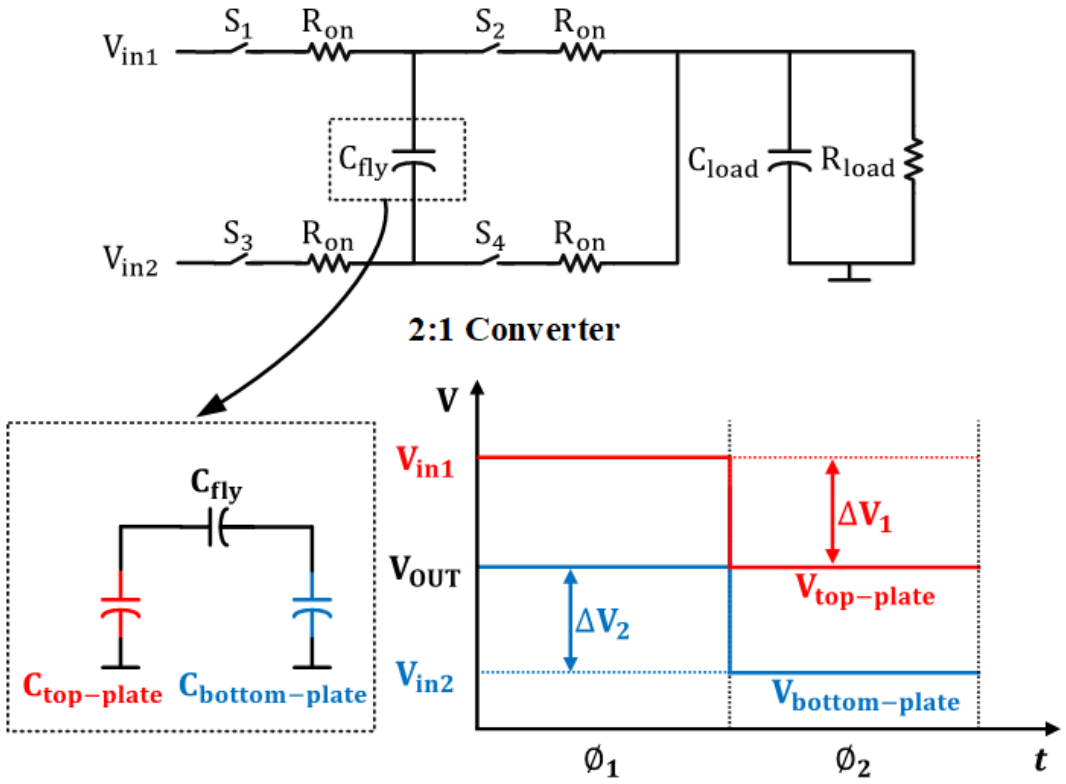

Figure 21: Parasitic Capacitance.

In the design of on-chip SC DC-DC converters, integrated floating capacitors suffer from parasitic capacitance from their terminals to ground. To mitigate this issue, Metal-Insulator-Metal (MIM) capacitors are often employed as flying capacitors due to their relatively lower bottom plate parasitic capacitance compared to Metal-Oxide-Metal (MOM) capacitors and Metal-Oxide-Semiconductor (MOS) capacitors. In the construction of MIM capacitor, parasitic capacitors $C_{top-plate}$ and $C_{bottom-plate}$ exist between each metal layer and the substrate, colored in red and blue respectively in Fig.21. During switching operation, the parasitic capacitances are charged and discharged at switching frequency f_s, and the voltage change across the parasitic capacitors of $V_{top-plate}$ and $V_{bottom-plate}$ are presented in Fig.21, where ΔV_1=ΔV_2=ΔV. In MIM capacitors, the parasitic capacitance of the bottom plate ($C_{bottom-plate}$) is typically larger than the parasitic capacitance from the

top plate ($C_{top-plate}$). Therefore, the energy loss due to the parasitic capacitance of the bottom plate can be expressed as:

$$P_{bot-cap} = f_s C_{bot} \Delta V^2 \tag{29}$$

Another source of the switching loss comes from the gate driver of the power switch. In control circuitry, the output impedance might be too high to directly drive the large gate capacitance of the power switch and achieve a quick on-off transition. To address this, tapered buffers are commonly used to amplify the power of the control signal to be able to drive the gates of the large power switches. For a single power switch, the power loss can be determined as Eq.(30):

$$P_{gate-cap} = f_s (C_{SW} + C_{buffer}) V_{SW}^2 \tag{30}$$

Where C_{buffer} is the sum of the gate parasitic capacitance of each buffer stage, and C_{SW} is the gate parasitic capacitance of the power switch. Then V_{SW} is the voltage swing of the clock driver.

$$\begin{aligned} P_{driver} &= M_{driver} P_{gate-cap} \\ &= M_{driver} f_s (C_{SW} + C_{buffer}) V_{SW}^2 \end{aligned} \tag{31}$$

Eq.(31) expresses the total power loss for gate driver loss.

2.1.5 Advanced multi-phase time-interleaving technique

In advanced SC DC-DC converter designs, the multi-phase time-interleaving technique is a widely employed strategy to reduce the ripple in the output voltage and enhance overall performance by partitioning the converter into smaller units and switching each unit on a different clock phase. As discussed previously, apart from its ability to decrease output voltage ripple, the multi-phase time-interleaving technique also offers the advantage of improving transient response. This enhancement is achieved by allowing the control loop to respond at every phase, which is a fraction of the switching period.

One of the primary motivations behind adopting the multi-phase time-interleaving technique is its potential to enhance converter efficiency. This is achieved through two key mechanisms:

1. Soft-charge Transfer [4]: By distributing the charge transfer among multiple phases, the charge sharing loss (which contributes to power loss) can be mitigated. In a single-phase converter, the charge sharing loss occurs when charge is transferred from one capacitor to another during switching. Multi-phase interleaving spreads out this charge transfer over different phases, reducing the impact on individual capacitors and minimizing energy losses.

2. Bottom-Plate Charge Redistribution [5]: Similar to charge sharing loss, bottom-plate loss (associated with parasitic capacitances) can also be reduced through multi-phase interleaving. The voltage redistribution across parasitic capacitances is distributed over different phases, leading to lower energy losses.

Given the potential benefits of multi-phase time-interleaving, it is crucial to develop control methods that effectively harness this technique. The control strategy must be designed to coordinate the switching of different phases, ensuring optimal charge transfer, minimal energy losses, and improved transient response. This requires careful consideration of the control signals, timing, and synchronization among the different phases.

2.2 CFM loop analysis – charge accumulation analysis

In the context of the CFM control loop, it's evident that its transient response speed is relatively slow due to the use of a Proportional-Integral-Derivative (PID) control mechanism. As previously discussed, the extra bypass path can speed up the transient process, but this presents limitations when dealing with certain load transitions, as illustrated in Fig.14. Specifically, it cannot effectively manage transitions from heavy to light loads, and it can lead to new overshoot problems during transitions from light to moderate loads.

In this section, a more in-depth analysis of the CFM loop will be conducted, and a charge accumulation analysis will be introduced to propose a simplified mathematical model for the proposed control strategy.

As shown in Fig.13, when bypass path's comparator detects a voltage undershoot resulting from the load transition from light to heavy, the bypass loop will take over the system by setting the VCO frequency to its maximum value through the control voltage set to V_{max}. When the load transient from light to moderate happens, the f_{max} exceeds the dedicated frequency f_s determined by load current, which leads to new overshoot. This behavior is similar to the transient response observed during system startup by the maximum frequency f_{max}, where the system operates in the SSL region. In this region, the flying capacitors are fully charged or discharged, allowing the process to be divided into discrete, unrelated points.

Additionally, it's important to note that the charge pump-based integrator in the CFM loop is only activated when the comparator in the CFM loop, detects that the output voltage exceeds the reference voltage V_{ref}. A simulations for start-up process shows, very interestingly, the output voltage trace bears a resemblance to the step response of a second-order system. The overshoot of this latter system is determined by the damping factor. For the former system, the overshoot is influenced by the combination of f_s, the dedicated frequency, and the exceed frequency Δf (the difference between f_s and the initial frequency f_{max}).

The term Δf can be viewed as a disturbance acting on a stable second order system as illustrated in Fig.22, which subsequently cause ringing to the output. A charge accumulation analysis is proposed to quantitatively evaluate this process. When the system is in a stable state, the charging current from the SC power converter to the output capacitor equals the discharging current from the output capacitor to the load. In this scenario, the current can be approximated as a constant current source. Mathematically, this process can be represented as:

$$\frac{dV_{out}}{dt} = \frac{I_{out} - I_{in}}{C_{out}} \tag{32}$$

$$I_{in} = I_{out} \tag{33}$$

, where

$$I_{in} = C_{fly}(MV_{in} - V_{out})f_s \tag{34}$$

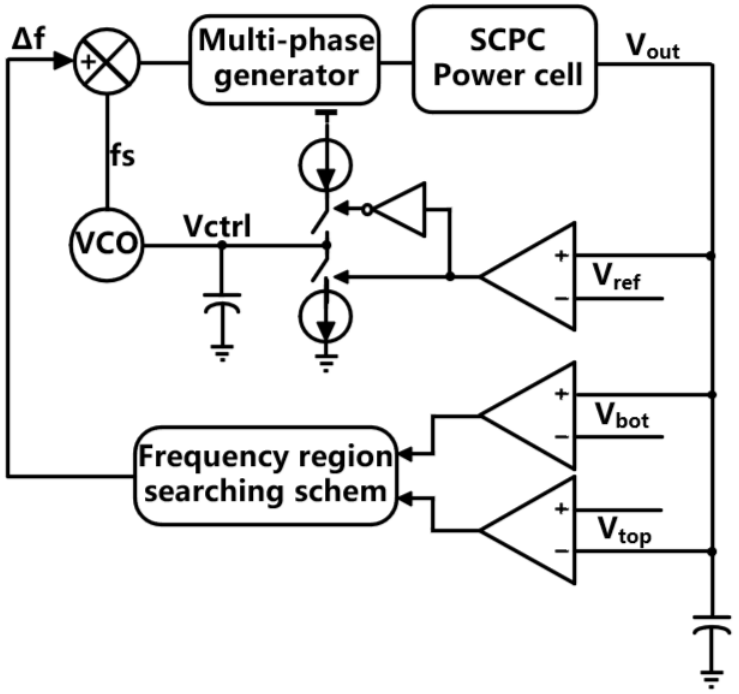

Figure 22: equivalent model of proposed system.

Where I_{out} is the load current, C_{fly} is the capacitance of the flying capacitor,$(MV_{in}-V_{out})$ represents the voltage difference between different phases of flying capacitor as well as the voltage difference between ideal convention ration and the wanted output voltage. The product of C_{fly} and $(MV_{in}-V_{out})$ represents the amount of charge pumped out by the SC converter per switching period. f_s is the steady-state frequency decided by the load current representing the number of pumping per time unit.

Consider now a disturbance $\Delta f(\Delta f > 0)$ is applied to the stable system; this would increase the charging current and causes an increase in output voltage, breaking the steady-state and causing the charge pump to continuously discharge the V_{ctrl} which reduce the VCO frequency. In short, the difference between charging and discharging current will cause a change in output voltage and can be expressed as

$$\frac{I_{in}-C_{fly}(\frac{V_{in}}{2}-V_{out})f_{VCO}}{C_{out}}=\Delta V_1 \tag{35}$$

, where

$$f_{VCO} = f_s + \Delta f - K_{VCO}\frac{I_{cp}}{C_{cp}}t \tag{36}$$

Where K_{VCO} is the voltage-frequency gain of the VCO, I_{cp} and C_{cp} is the charging and discharging current and capacitor at the V_{ctrl} node which would determine the second pole of the system. ΔV_1 is the voltage changing after a unit time period. Consider equation 34 and equation 35, it is clear that the voltage change after the first unit time is dependent of Δf and independent of steady-state frequency f_s. However, for the second unit time, the output voltage varying due to the exceeded frequency will be different and can be expressed as

$$\frac{I_{in} - C_{fly}(\frac{V_{in}}{2} - V_{out} - \Delta V_1)f_{VCO}}{C_{out}} = \Delta V_2 \tag{37}$$

Where ΔV_2 is the voltage changing after the second unit time period. From the formula, it is clear that the larger the steady-state frequency f_s is, the less overshot voltage will be. The voltage variation curve can be considered as the sum of multiple unit time voltage changes which can be expressed as

$$\int \frac{I_{in} - C_{fly}(\frac{V_{in}}{2} - V_{out} - \Delta V(t))f_{VCO}}{C_{out}}dt = \Delta V(t) \tag{38}$$

By simplifying, a first-order non-homogeneous differential equation can be obtained. By analyzing the extreme point of the curve, the relationship between overshoot and Δf and f_s can be obtained and is shown as Fig.23. System model simulation results shown as Fig.24 are consistent with the simplified model by charge accumulation analysis method. Furthermore, the start up process of the system model, depicted in Fig.25, demonstrates a similar trend to that of the simplified model.

From the above results, the exceed frequency has a strong correlation with overshoot, less exceed frequency causes lower overshoot and vice versa. Thus, the feedback loop of the system can limit overshoot to an acceptable voltage range by limiting the value of exceeded frequency Δf, and the proposed system architecture arises from this.

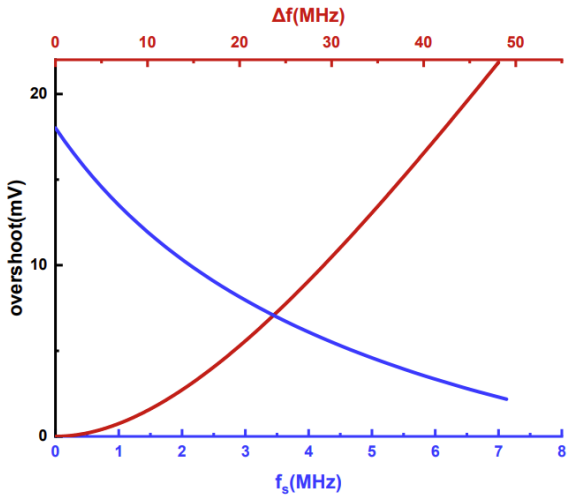

Figure 23: relationship between overshoot and Δf and f_s of proposed analysis method.

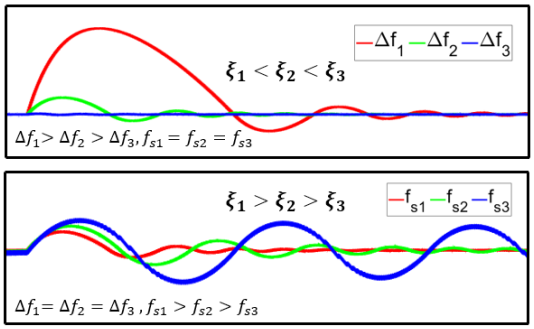

Figure 24: Simulation result of the equivalent system.

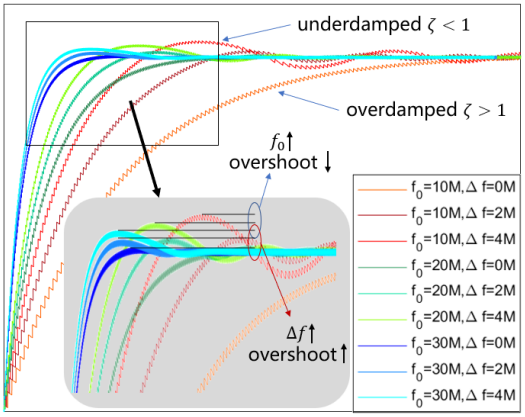

Figure 25: Simulation result of the start up process.

3 Proposed system architecture

As previously discussed, to maintain the output voltage within an acceptable range, it is crucial to limit the extent to which the frequency is exceeded. In this section, we present a novel Hybrid-Hysteresis-CFM control strategy that combines the benefits of CFM and hysteresis control method which minimize the output voltage ripple during steady-state operation and mitigating the voltage undershoot or overshoot during transient state. By seamlessly integrating the strengths of these two control strategies, the proposed architecture offers enhanced protection for electronic devices while ensuring optimal performance.

3.1 proposed system diagram

The HHC RSC system architecture is depicted in Fig.26, which consists of a power core, a hysteresis feedback loop, a CFM feedback loop, and clock generation blocks. The power core of the architecture employs a RSC topology, chosen to expand both input and output ranges while also validating the universality of the proposed theory. The power core comprises 4 power stages, implemented with capacitor sizing technique which is adopted to achieve minimal equivalent output impedance and enhanced load performance for varying conversion ratios, a topic that will be explored comprehensively later on.

Additionally, the architecture incorporates a multi-phase time-interleaving technique. In each power stages, 10 standard 2:1 SC power cells are utilized, driven by a 10-phase clock generated inherently by the on-chip VCO. The utilization of time-interleaving allows the removal of buffer capacitors from the output of each cascade stage. Thus, leads to higher power density, reduced voltage ripple, faster transient response, and further enhance the overall efficiency and performance of the system.

In this system architecture, two comparators are employed to establish a coarse control loop which refer to the hysteresis control loop. This loop serves a dual purpose: first, it restricts the voltage between V_{top} and V_{bot}, thereby creating an acceptable voltage boundary. Second, these comparators are responsible for detecting voltage fluctuations resulting from load transitions, enabling the activation of the hysteresis control loop. This hystere-

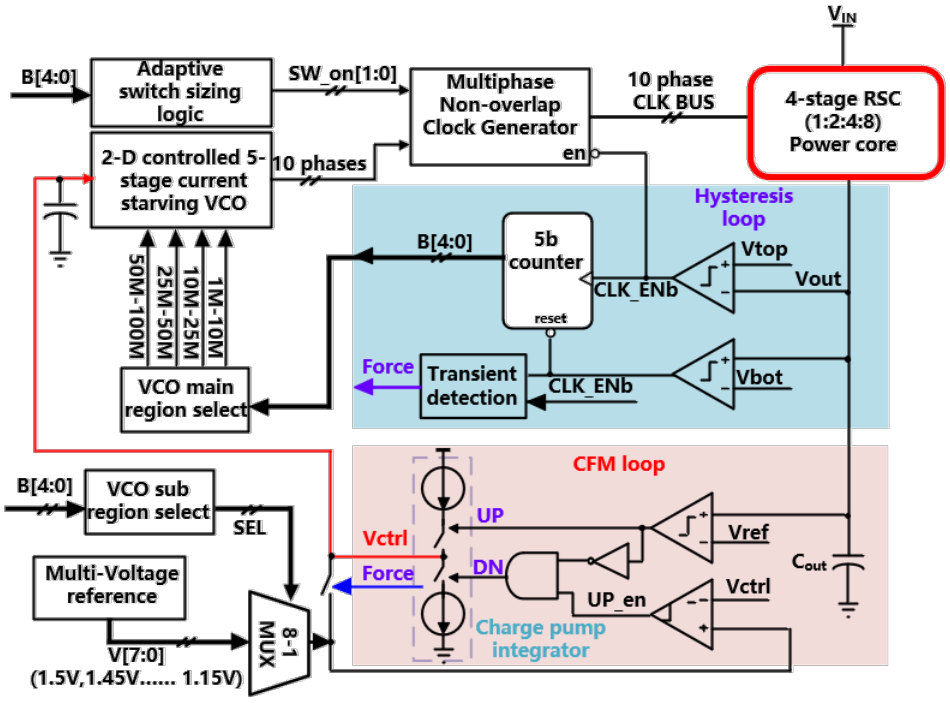

Figure 26: Proposed system architecture.

sis control loop serves to maintain voltage within acceptable boundaries during transient periods.

In CFM control loop, there are two comparators, one of the comparators contributes to the fine CFM control loop. This loop operates during steady-state, determining the optimal frequency that minimizes voltage ripple. Simultaneously, another comparator plays a crucial role during transient. It works by restricting the maximum frequency, effectively capping the value of V_{ctrl} to prevent excessive voltage overshoot.

Integral to this system is a two-dimensional controlled VCO. This VCO acts as a cornerstone in implementing the proposed control strategy. Its unique design allows for the establishment of 32 distinct frequency regions. This feature provides a finely-tuned range for Δf, offering precise control over overshoot voltage limitations. Further insight and a comprehensive explanation of the intricacies of the two-dimensional controlled VCO will be provided in Chapter 4 of this study.

3.2 working flow chart and ideal working waveform

The chart depicting the ideal workflow is presented in Fig.27, and its analysis is detailed as following. Three external reference voltage levels, namely V_{top}, V_{ref}, and V_{bot}, are employed as previously specified.

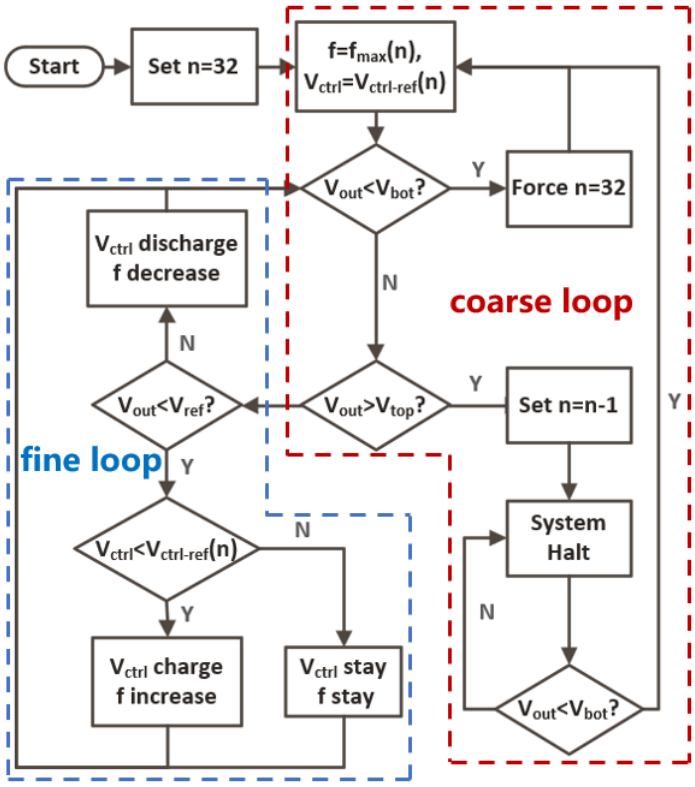

Figure 27: Proposed system work flow chart.

During steady-state operation, the system's output voltage is regulated towards V_{ref} through charge pump-based integrator, controlled by the CFM control loop, which minimizes output voltage ripple. In the event of a sudden increase in load current causing the output voltage to drop and reach the lower boundary, the hysteresis control loop of the HHC control system is engaged. This prompts the system to maximize the VCO frequency to f_{max}, which corresponds to the highest frequency region. This action elevates the output voltage by restricting the maximum control voltage of the VCO, denoted as V_{ctrl}, with the aid of a comparator whose reference originates from a selectable multi-

voltage reference.

For loads closely aligned with the dedicated frequency of f_{max}, the range of Δf remains appropriate. Consequently, the CFM control loop resumes regulating the output voltage to the desired V_{ref} without invoking V_{top}. Subsequently, the fine control loop takes charge once more, and the system achieves a steady state.

However, if the maximum frequency exceeds the appropriate limit for the load current, leading to an excessive Δf, the output voltage undergoes a significant overshoot, prompting the activation of the upper boundary. As a result, the system comes to a halt, and V_{out} gradually decreases due to capacitor discharge. Upon triggering V_{bot}, the system reboots within the subsequent VCO region, characterized by a lower maximum frequency. This cyclic process persists until a suitable Δf is identified. The system seamlessly transitions to the target frequency through a coarse/fine frequency tuning schedule, all the while implementing hysteresis control to maintain the overshoot/undershoot within the specified hysteresis window. The pursuit of an appropriate frequency region through this process is denoted as the ”pseudo startup” process within this system.

In the scenario of a sudden decrease in load current, the output voltage surges and triggers V_{top}. The ensuing process mirrors the aforementioned pseudo startup process. The waveform illustrating the system's behavior during load transitions, specifically from light to heavy and from heavy to light, are demonstrated in Figures 28 and 29, respectively, aligning with the discussed working process.

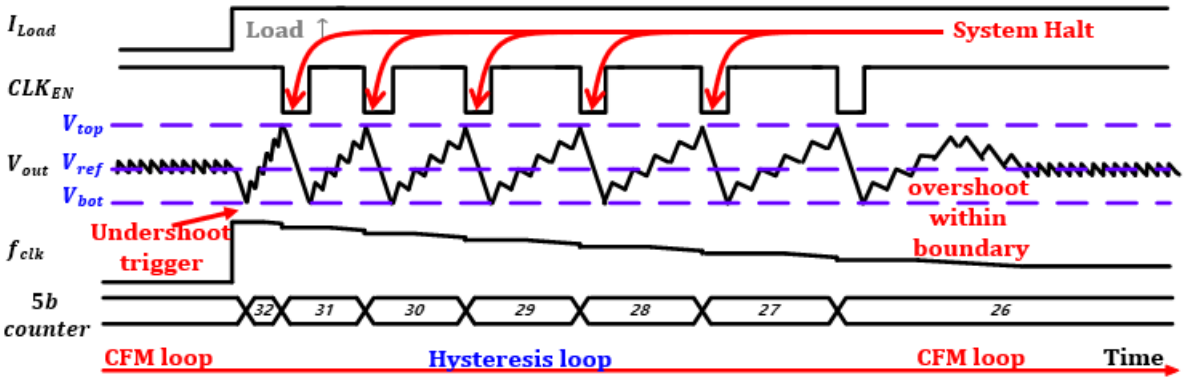

Figure 28: operation timing diagram for load transient from light to heavy.

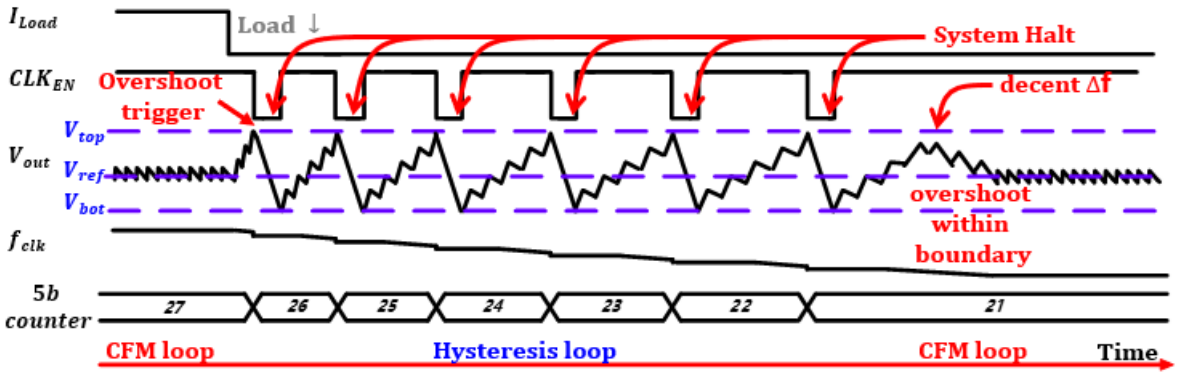

Figure 29: operation timing diagram for load transient from heavy to light.

3.3 Power core implementation

This system adopts the RSC topology to increase the input and output voltage range and provide multiple conversion ratios to improve efficiency. By verifying the proposed control strategy in different conversion ratios, the universality of this method can be confirmed. The RSC topology is shown in Fig.30, where the conversion ratio is selected using a 4-bit binary code out of the chip. All the switches are implemented with transmission gates to handle different voltage situations. Additionally, the four power stages adopt adaptive capacitor sizing which have a ratio of 1:2:4:8 at capacitor to decrease the output equivalent impedance for different conversion ratios and parallelisms the power stage to enhance load capacity. Fig.31 provides simplified examples of the capacitor sizing technique for different conversion ratios.

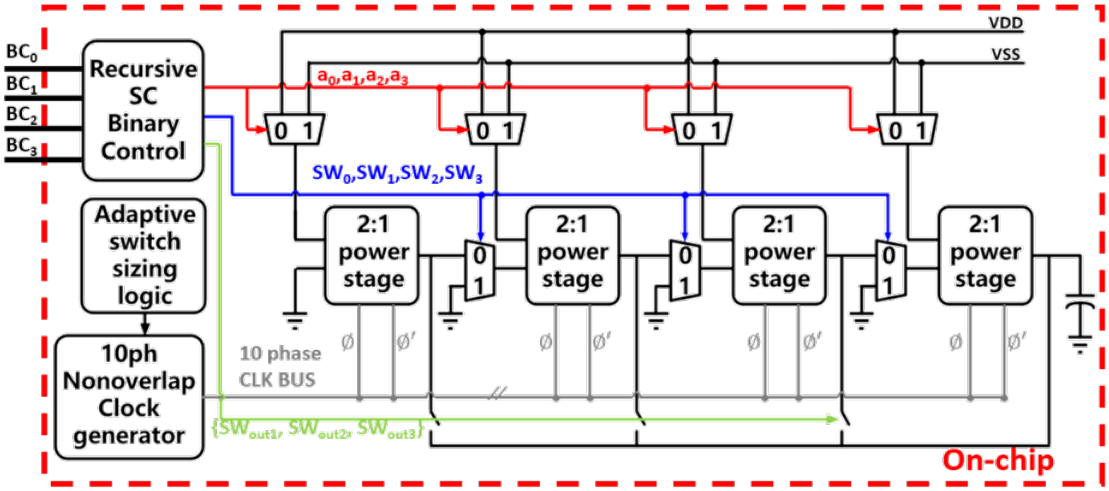

Figure 30: Circuit topology of the RSC topology.

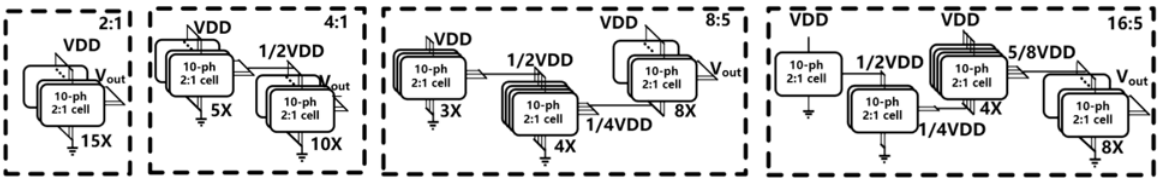

Figure 31: Simplified examples for capacitor sizing RSC topology.

4 Circuit Implementation

In this section, several key circuit blocks that constitute the foundation of the proposed system will be explained in detail. These components play a pivotal role in elucidating the intricacies and functionality of the system architecture.

4.1 Voltage Control Oscillator

The cornerstone component of the HHC control system architecture is the two-dimensional controlled VCO. The VCO serves a dual purpose by generating the necessary clock signal and offering distinct frequency regions for the system to search a decent Δf during transient state. For this purpose, a 5-stage current-starved VCO based on a ring oscillator configuration has been chosen to achieve easy integration, low power consumption, ease of tuning, and inherent generation of a 10-phase clock signal, thereby, its compatibility with multi-phase technology makes it a fitting choice for the system implementation, as illustrated in Fig.32. The oscillation frequency (f_{osc}) of this VCO is determined by the bias current(I_d), the number of stages(N) and the total capacitance(C_{total}), which can be expressed as

$$f_{osc} = \frac{I_d}{2NC_{total}} \tag{39}$$

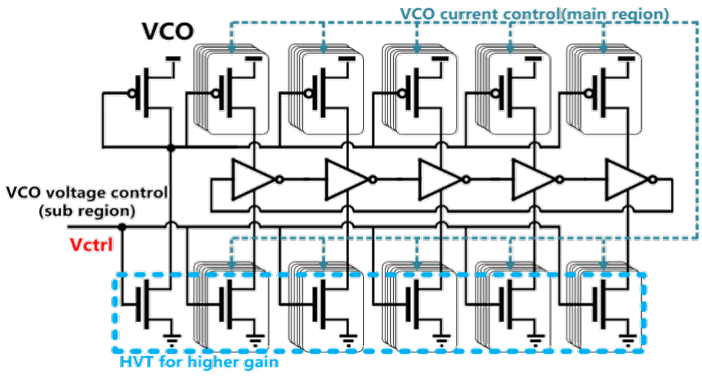

Figure 32: Two-dimensional controlled ring osc based 5-stage VCO.

Conventionally, the bias current of each inverter is only controlled by the control voltage (V_{ctrl}). However, in this design, an innovative approach is introduced wherein the

bias current can also be modulated through the the manipulation of the number of voltage controlled current source. The enhancement results in a continuous two-dimensional control, which defines finely partitioned output frequency regions as depicted in Fig.33. By controlling number of active current sources, the VCO frequency were divided into four main frequency regions, while voltage control further divides each main region into 8 sub-regions, resulting in thirty-two fine clock frequency regions in total.

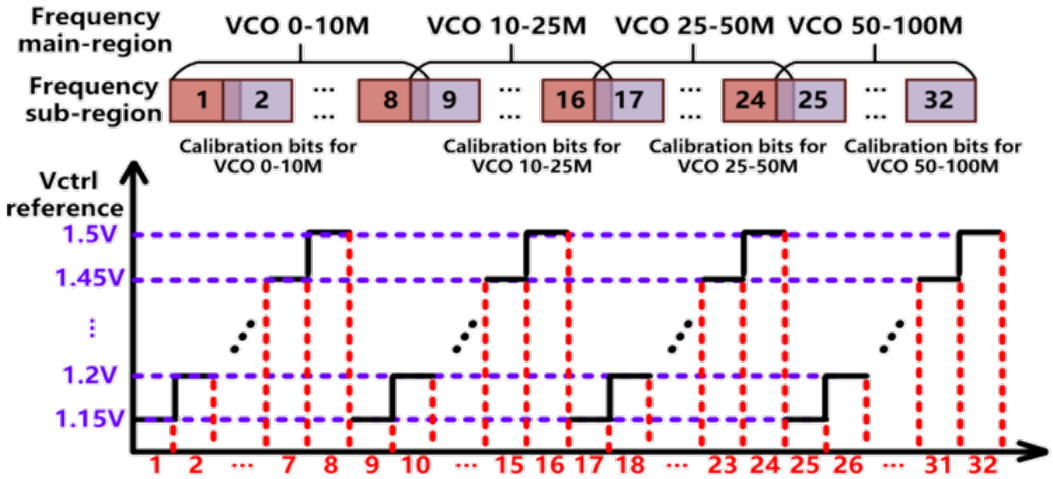

Figure 33: Frequency region relationship for 2-D VCO.

The delineation of these sub-frequency regions adheres to a specific criterion: the maximum frequency of the current region and the subsequent smaller region must maintain a difference which not exceeding Δf requirements. This consideration ensures that the overshoot voltage for load current determined by the maximum frequency of the subsequent smaller region remains within the designated voltage boundaries. Consequently, this approach guarantees the accommodation of varying load conditions, thus constraining overshoot voltage during all load transitions. Furthermore, to safeguard continuity against Process, Voltage, and Temperature (PVT) variations, each sub-region overlaps with its adjacent regions, as illustrated in Fig.33.

Furthermore, calibration for the number of current sources is undertaken for the four main frequency regions, thereby effectively mitigating any potential impact from PVT variations. This comprehensive strategy facilitates robust performance across diverse op-

erational conditions.

4.2 Dynamic Comparator

In this design, a fully dynamic latch-type voltage sense amplifier is chosen to be implemented as comparators, as shown in Figure 34. The clock frequency of the comparators is set to 1GHz to minimize response time and loop delay, which in turn reduces the impact on overshoot and undershoot. The dynamic nature of the comparator enables a balance between low power consumption and faster response time, contributing to the overall efficiency of the HHC system.

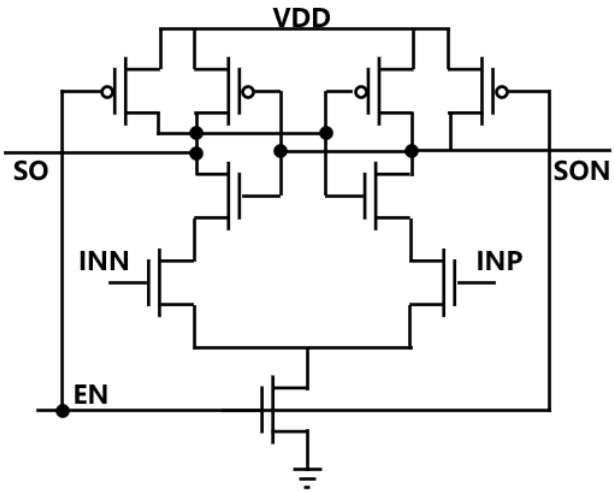

Figure 34: Fully dynamic comparator.

4.3 Constant-gm based charge pump

In a conventional integrator-based CFM loop, the location of the second pole is determined by the V_{ctrl} point and is associated with the ratio I_{ch}/C_{ch}, where I_{ch} represents the charging and discharging current of the charge pump, and C_{ch} denotes the capacitance at the integration point V_{ctrl}. The integrator-based SCPC system faces a trade-off between stability and response speed, necessitating careful design of the second pole.

In this particular design, a MOS capacitor is selected for C_{ch} to optimize area utilization, while a constant-gm based current source is employed for the charge pump, as depicted in Figure 35. The cascode structure ensures reduced variation in current with changes in voltage at the V_{ctrl} node, thereby providing a stable and consistent current for the charge pump. Moreover, this charge pump configuration facilitates calibration to address PVT variations. Calibration can be achieved by adjusting the resistance value, as the relationship between charge pump current and resistance is expressed by:

$$g_m = \frac{1}{R} \tag{40}$$

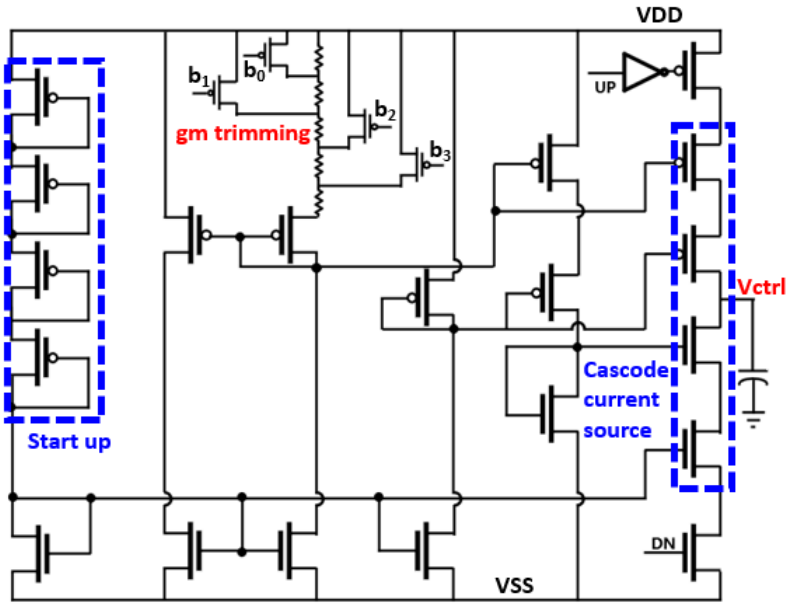

Figure 35: Schematic of the constant-gm based charge pump.

4.4 Power Stage

The circuit implementation of the SC unit and its driver is depicted in Fig.36. The 2:1 power stage consists of four switches and one flying capacitor. Due to the multiple conversion ratios achieved by the RSC topology, the transmission gate is implemented as switches to handle different voltage situations. However, for specific conversion ratios

such as 2:1, the transmission gate will increase the switching loss, leading to efficiency degradation. In this design, the power stage adopts the voltage domain stacking technique to increase efficiency for the 2:1 conversion ratio, as shown in Fig.37. In this situation, only one transistor will operate as the switch to eliminate the switching loss caused by redundant transmission gates. Furthermore, due to the switching loss expressed in Eq.41 below, by halving the switch voltage and doubling the width of the switch, the switching loss will be further decreased.

$$P_{SWLOSS} = CV^2 f \tag{41}$$

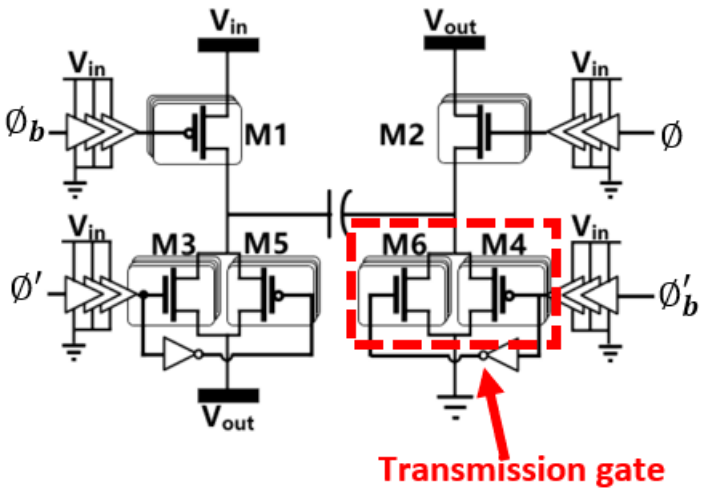

Figure 36: Circuit implementation of SC power stage.

Additionally, the voltage stacking technique can prevent all switches from being exposed to a voltage higher than the breakdown voltage by separating M1 and M3 in a higher voltage domain and M2 and M4 in a lower voltage domain. The gate driver also operates in the corresponding voltage region to protect the switch and decrease switching loss.

For SC power cell design, as mentioned previously, the equivalent output impedance is determined by the slow switching limit resistance and fast switching limit resistance. The relationship between output equivalent impedance and frequency is shown in Fig.38.

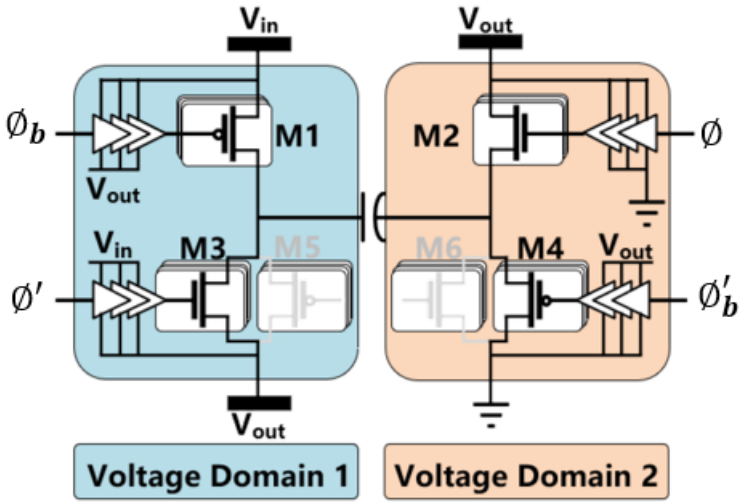

Figure 37: Voltage domain stacking technique.

Conventionally, the size of a switch is determined by setting the FSL impedance equal to the SSL impedance at maximum switching frequency. However, by doing so, switching loss will become larger for lighter load conditions and will degrade power efficiency. In this design, an adaptive switch sizing is proposed to overcome this problem with the help of the proposed HHC system, as shown in Fig.39. The four regions correspond to the 4 main regions of the VCO described in the previous subsection. For different clock regions, the width of the switches can be modulated to reduce switching loss. When the system operates with a heavy load where the VCO operates in the 50M-100M region, the parallel switches will all be on to meet the on-resistance requirement of the corner frequency. When the system operates in a moderate load situation, and the VCO operates in the 25-50MHz region, the on-resistance of the switch does not need to be as low as the on-resistance in the heavy-load region, thus some parallel switches can be turned off to reduce switching loss. By doing so, switching losses can be reduced, especially for light load situations.

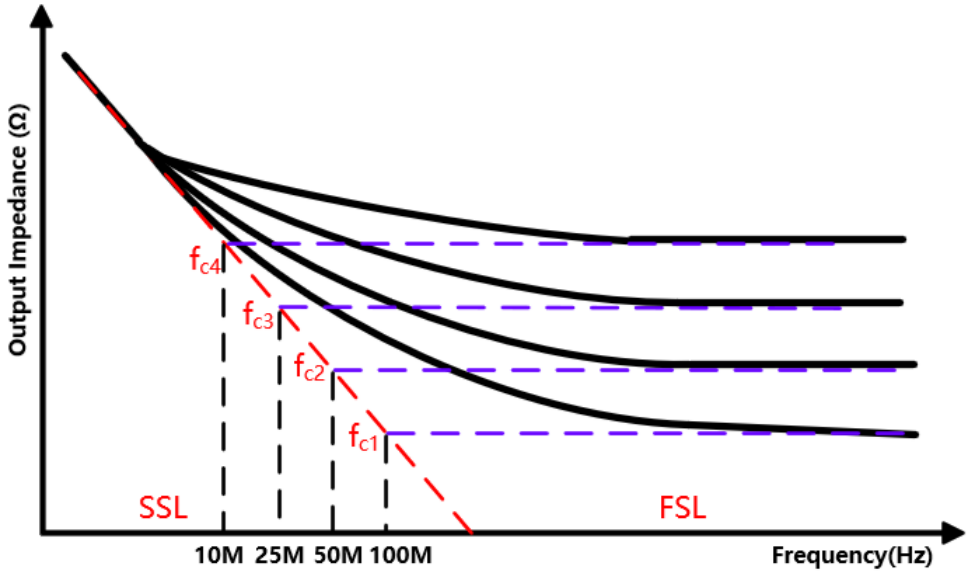

Figure 38: Relationship between equivalent output impedance and frequency.

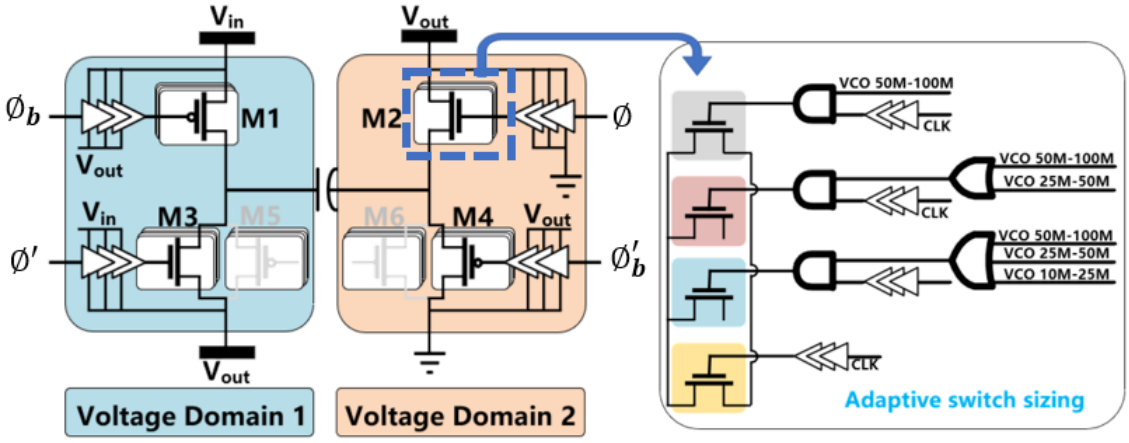

Figure 39: Proposed adaptive switch sizing.

5 Measurement Results

The proposed Hybrid Control DC-DC converter was realized using a 180nm BCD CMOS process, occupying an effective active area of $2.89mm^2$, as depicted in Figure.40.

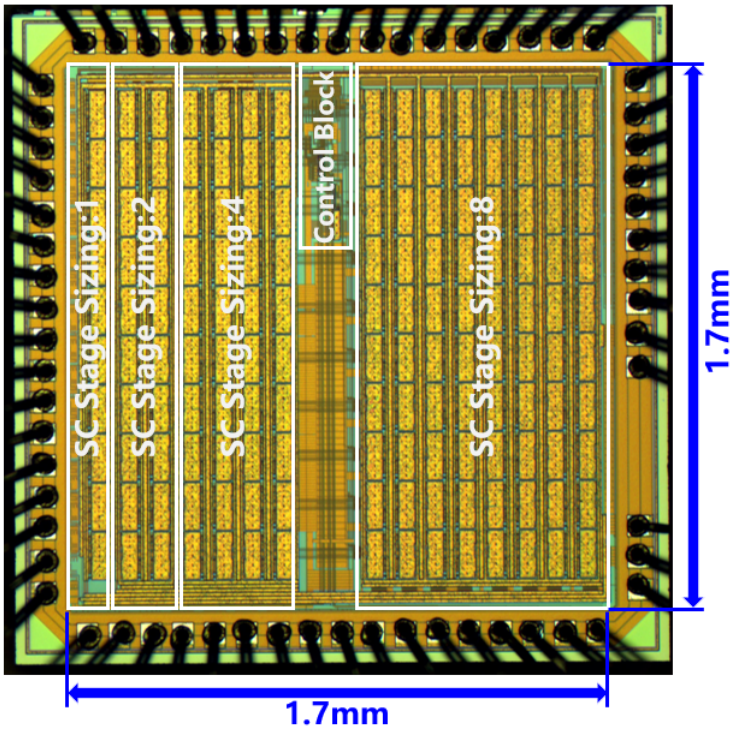

Figure 40: Chip Photo.

The power stage was implemented utilizing MIM capacitors to mitigate bottom plate losses due to their lower parasitic capacitance. Additionally, the output capacitor was constructed using MOS capacitors and stacked with MIM capacitors to achieve higher power density. This section will present measurement results from the fabricated chip, demonstrating the performance of the proposed system.

5.1 Measurement setup

The measurement setup is shown in Fig.41 theoretically and Fig.42 in reality.

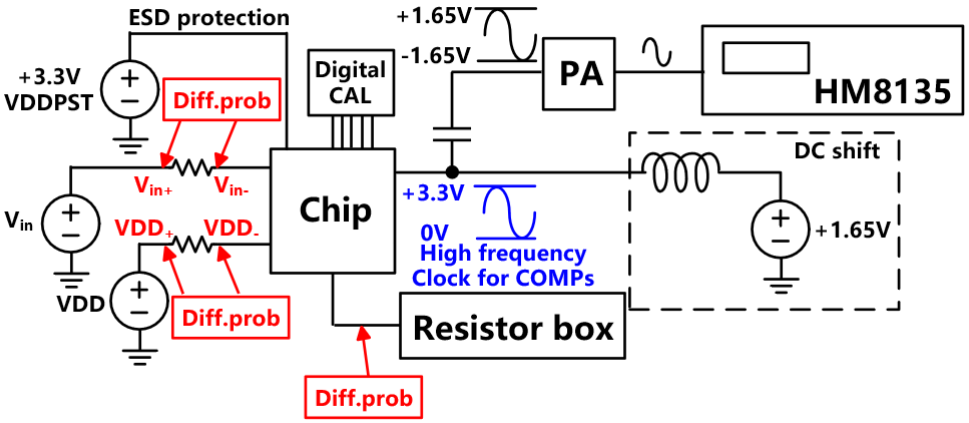

Figure 41: measurement setup in theory.

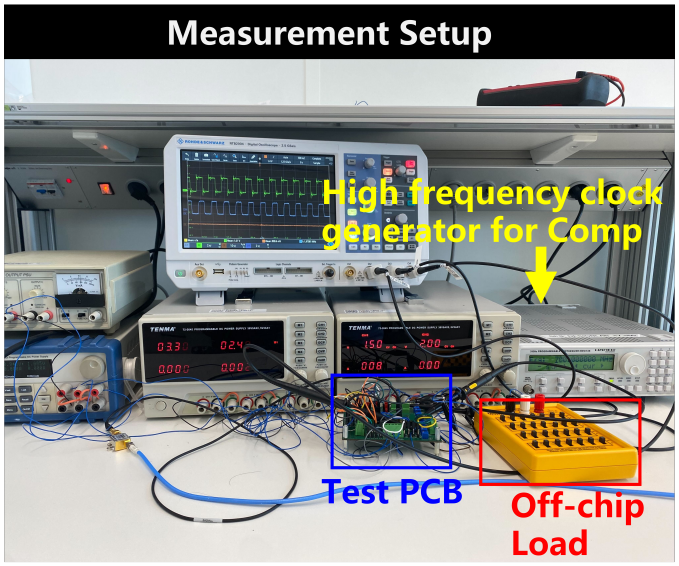

Figure 42: measurement setup in reality.

Since a high frequency clock for comparators is needed in this project, a HM8135 high frequency synthesizer together with power amplifier and DC shift circuit is adopted to provide a high frequency input clock for the circuit. The efficiency of the converter is

expressed as:

$$eff = \frac{P_{out}}{P_{in}} = \frac{\frac{V_{out}^2}{R_{out}}}{\frac{VDD_+ - VDD_-}{R_{VDD}} \times VDD_- + \frac{V_{in+} - V_{in-}}{R_{Vin}} \times V_{in-}} \times 100\% \quad (42)$$

5.2 System behavior measured waveform

The transient waveform from heavy load to light load and from light load to heavy load are shown in Fig.43 and Fig.44.

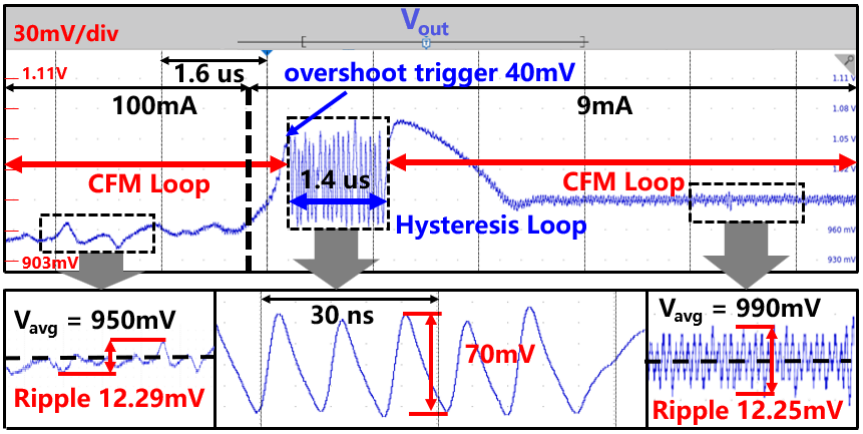

Figure 43: Transient Waveform from heavy load to light load.

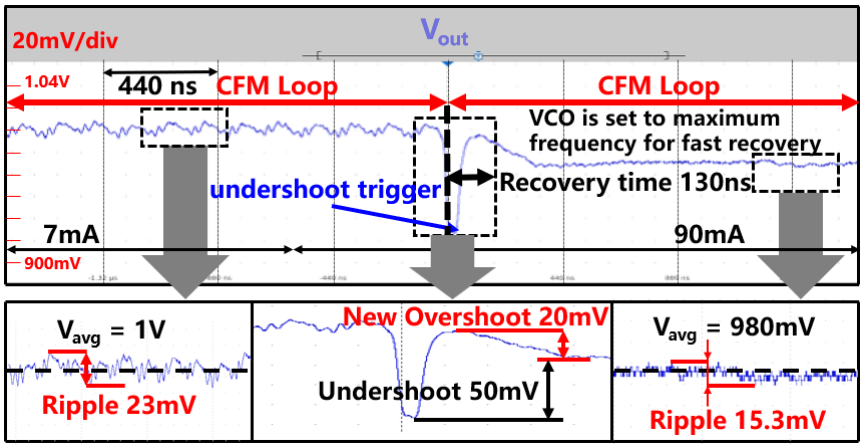

Figure 44: Transient Waveform from light load to heavy load.

From the measured transient waveform, the proposed system achieves significantly lower overshoot and undershoot, with values of 40mV and 50mV, respectively. This

improvement is attributed to the hysteresis boundaries during load transitions. When the system finds a decent frequency region, the CFM will take over the control and with 10-phase time-interleaving structure well regulates output voltage with a minimum ripple of only 12mV.

The transient waveform from heavy load to light load and from light load to heavy load without triggering hysteresis boundary are shown in Fig.45 and Fig.46

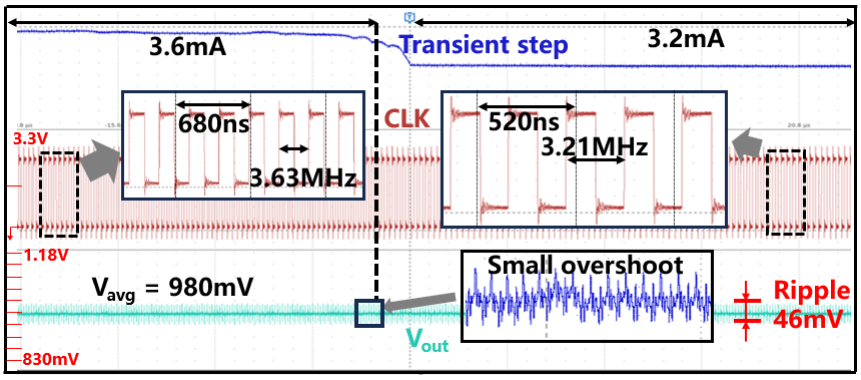

Figure 45: Transient Waveform from heavy load to light load within boundary.

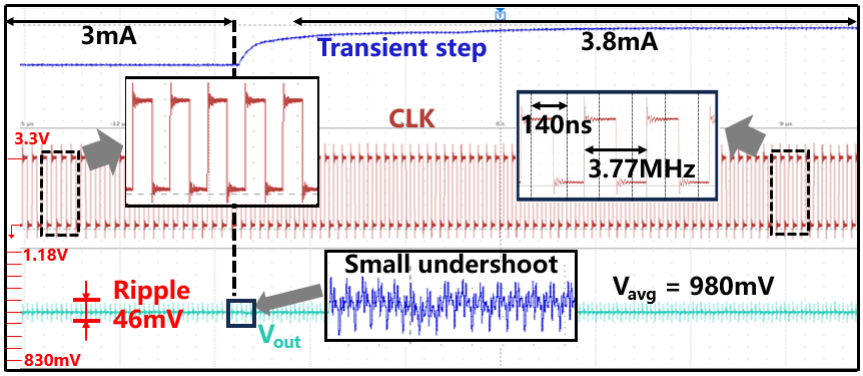

Figure 46: Transient Waveform from heavy load to light load within boundary.

From the measured transient waveform, when the load transition step is small, the increase and decrease on output voltage are also small that cannot even touch the output boundaries defined by the hysteresis band. In these cases, the CFM control can handle the load changes without engaging the hysteresis control.

Two more conditions for transient waveform from moderate load to light load and from light load to moderate load are shown in 47 and 48.

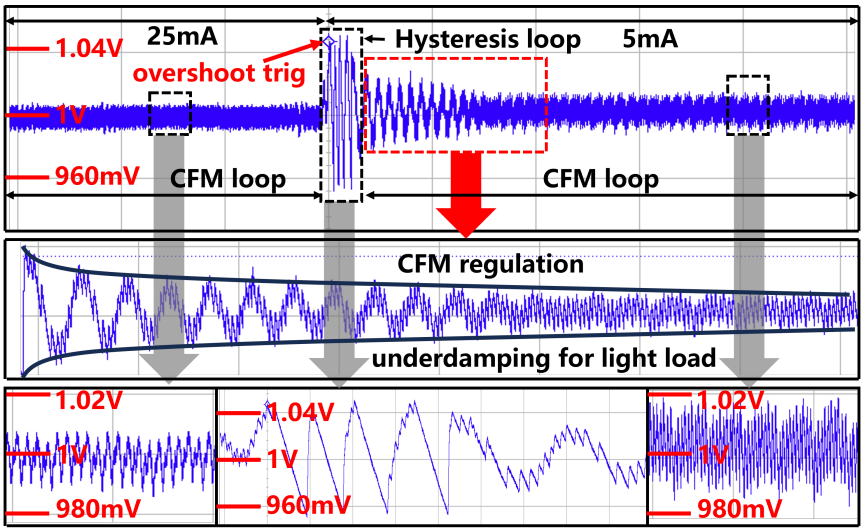

Figure 47: Transient Waveform from moderate load to light load.

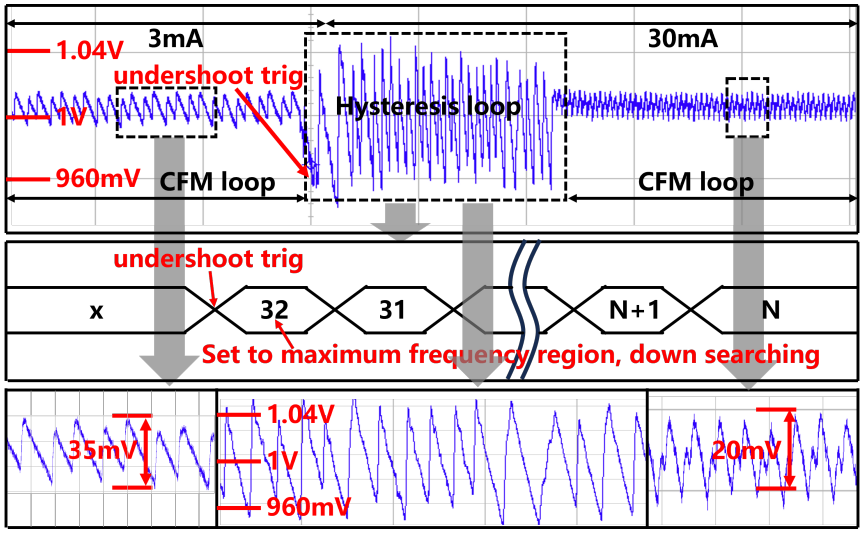

Figure 48: Transient Waveform from light load to moderate load.

During these two transient situations, the proposed system achieves significantly lower overshoot and undershoot, with values of 40mV. However, when observing the transient

waveform from moderate load to light load, it becomes evident that the system undergoes an under damping effect in CFM regulation. This indicates that the system faces challenges in achieving optimal regulation under low load conditions.

The start up performance of the proposed system is shown in Fig.49 and Fig.50. During start up, the system will determine the frequency region through the coarse/fine frequency tuning scheme and find the optimal frequency in the end.

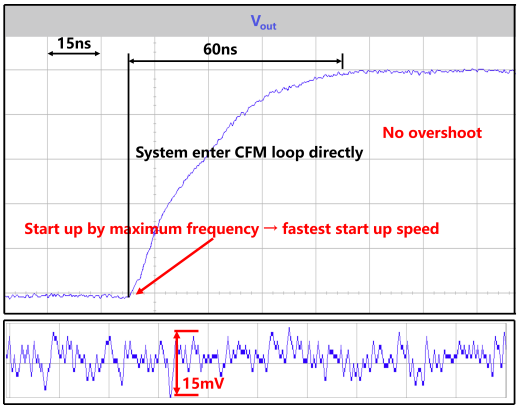

Figure 49: Start up process for heavy load condition.

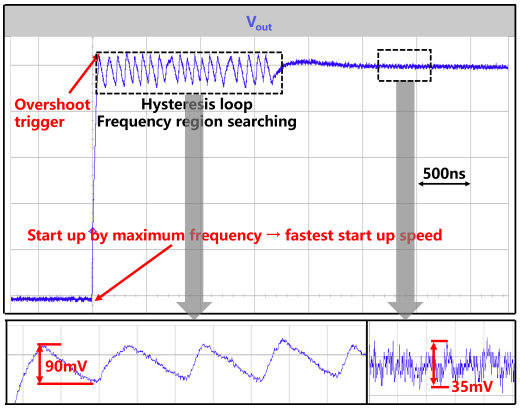

Figure 50: Start up process for moderate load condition.

To test the function of the RSC topology, a open loop test is conducted, the measured waveform for multi-VCR is shown in Fig.51 The function of the RSC topology is controlled by a 4-b binary code from out of the chip, the relationship between the code and VCR is also shown in this figure.

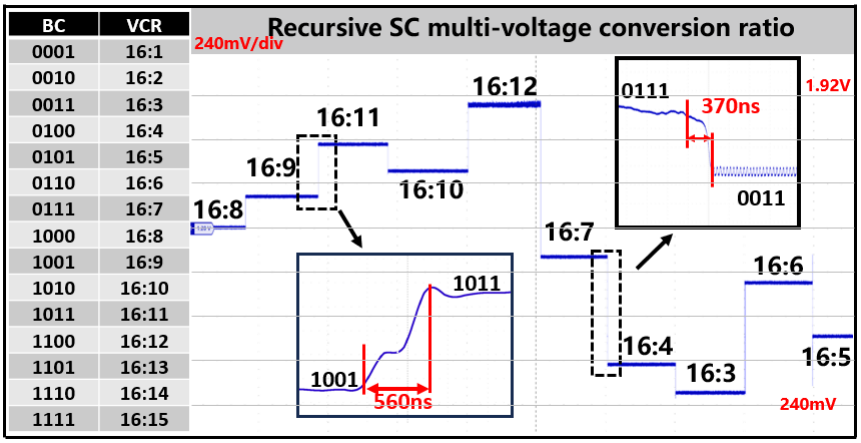

Figure 51: Recursive SC multi-voltage conversion ratio.

Fig.52 shows the system behavior operates in CFM loop, during CFM mode, the multi-phase time-interleaving strurcutre regulate the output voltage into minimum voltage ripple, two time-interleaving clock phases are also shown in this figure.

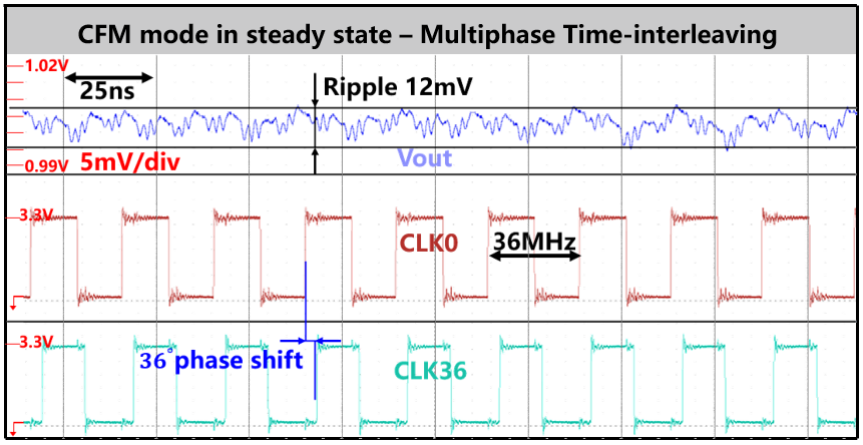

Figure 52: CFM mode in steady state - Multiphase Time-interleaving.

5.3 System performance measurement

Fig.53 shows the power conversion efficiency for multi-VCR open loop test. From the figure, the efficiency boost during 2:1 conversion ratio is basically due to the voltage stacking technique adopted in this conversion ratio. The input voltage range for the chip

is from 0.8V to 3.6V, the output range from 0.25V to 2V when the input voltage is 2.4V, the peak efficiency 82% happens at 2:1 conversion ratio when input is 2.4V and output is 1.1V.

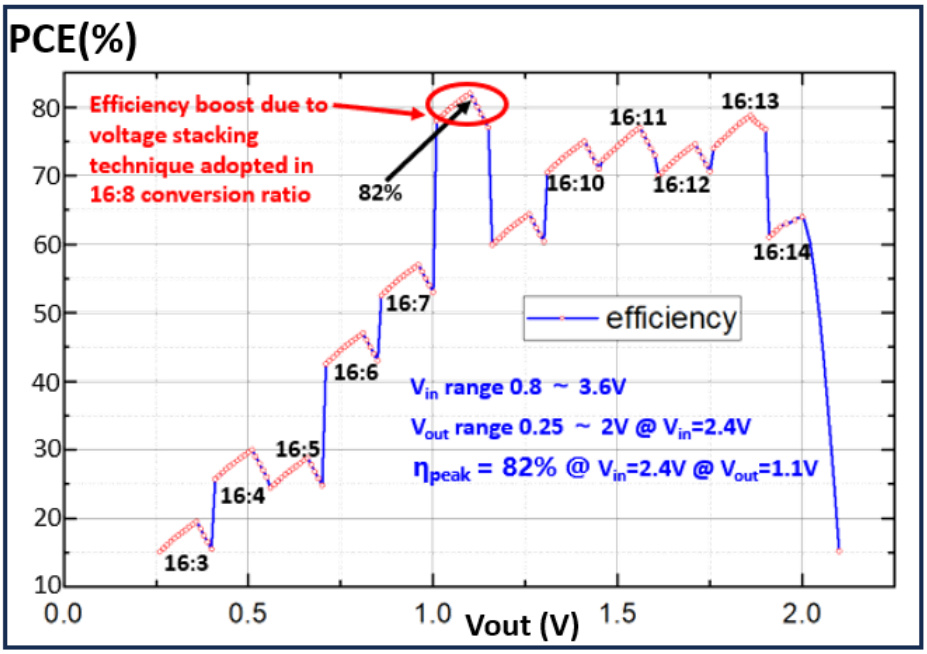

Figure 53: Power conversion efficiency for open loop multi-VCR test.

A close loop efficiency is also conducted, the power conversion efficiency for HHC control closed loop test conducted in 2:1 conversion ratio as shown in Fig.54. From the close loop test, the peak efficiency 80.6% is found at the conversion from 2.4V to 1.05V. From the efficiency curve and based on the trend of the curve, it can be seen that due to the adoption of adaptive switching sizing technology, efficiency has been significantly improved in light loads condition.

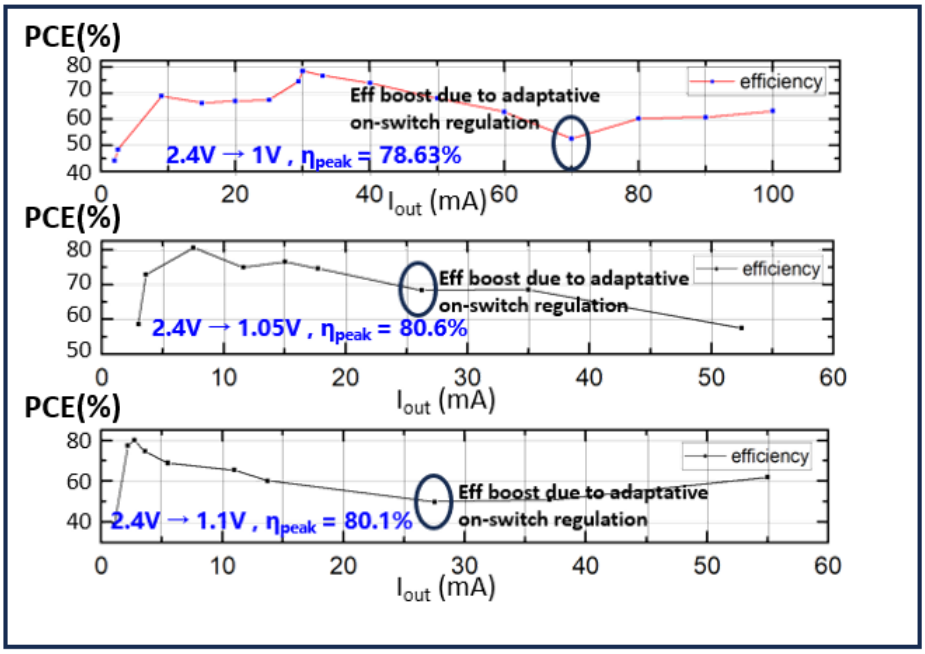

Figure 54: Power conversion efficiency for Hybrid control closed loop test @ 2:1.

Fig.55 shows the system behavior of Hybrid control system, the system achieves a minimum 12mV output voltage ripple thanks to the adoption of time-interleaving CFM control. and Fig.56 shows the shooting performance of the Hybrid control system, the system achieve a 50mV shooting voltage. for limiting case with transition from ultra low load to heavy load condition. The system shooting to 100mV due to the extra delay of the control loop. The power break down and area break down are shown in Fig.57 and Fig.58 respectively. The proposed controller occupies very small energy and area compared with power stage.

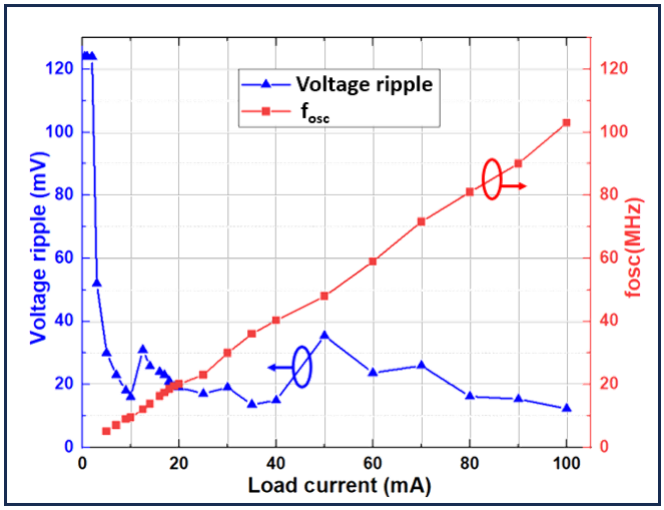

Figure 55: Voltage ripple and clock frequency vs load current.

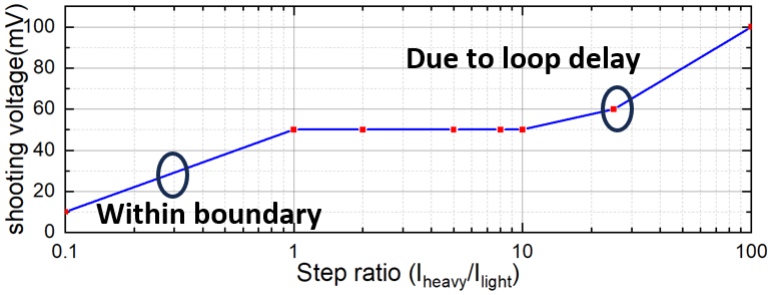

Figure 56: Shooting performance.

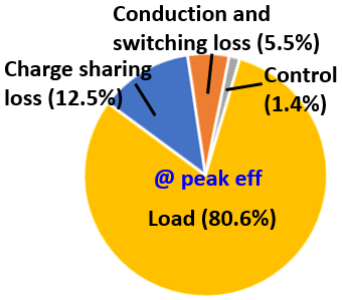

Figure 57: power breakdown.

A comparison between this work and State-of Art work is shown as Table 1. The

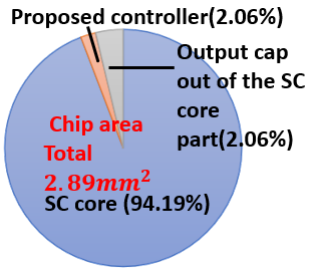

Figure 58: area breakdown.

proposed converter achieves the lowest voltage ripple and over/undershoot voltage at a larger load transient step.

Table 1: State of the art comparison

Design	ISSCC'11 [10]	ISSCC'13 [11]	ISSCC'14 [2]	ISSCC'18 [8]	JSSC'19 [6]	ISSCC'23 [22]	This work
Technology	130 nm	65 nm	32 nm	65 nm	65 nm	65 nm	180 nm
Fully-integrated	No	Yes	Yes	Yes	Yes	Yes	Yes
Active Area	5.12mm^2	0.64mm^2	0.15mm^2	2.42mm^2	0.61mm^2	4.76mm^2	2.89mm^2
Topology	Hybrid	3:1,5:2 SC	2:1,3:2 SC	AVFI	2:1 SC	RCSC	RSC
Cap type	N/A	MOS	Deep Trench	MIM+MOS	MOS	MOS+MOM	MIM+MOS
C_{fly}/C_{out}	18nF/5nF	3.88nF/0	1nF/0	8nF/6nF	2.56nF/0	19.8nF/0	1.8nF/3.4nF
Interleaving phases	4	18	16	4	15	66	10
V_{in}	2.4V	3-4V	1.8V	0.22-2.4V	2.4V	0.4-2.5V	0.8-3.6V
V_{out}	0.4-1.4V	1V	0.7-1.1V	0.85-1.2V	1V	0.2-2V	0.25-2V @ Vin=2.4V
Max I_{load}	N/A	162mA	365mA	80.1mA	138mA	20mA	100mA
Power density	N/A	253mW/mm^2	5600mW/mm^2	33mW/mm^2	240mW/mm^2	6.3mW/mm^2	34.6mW/mm^2
Peak eff	77%	74.3%	86.4%	84.1%	82.8%	83.9%	80.6%(close loop) 82%(open loop)
Control Strategy	PWM	CFM	Pulse skipping	Pulse skipping	CFM	CFM	Hybrid control
Load transient step	220mA-370mA (1.68x)	N/A	30mA-365mA (12x)	4mA-25mA (6x)	11mA-138mA (12.5x)	1mA-19.8mA (20x)	5mA-100mA (20x)
Overshoot/Undershoot	80mV	170mV	125mV	60mV	200mV	600mV	50mV
Voltage ripple	50mV	50mV	30mV	36mV	60mV	200mV	12mV

6 Conclusion and future work

6.1 Conclusion

This thesis proposes a Hybrid-Hysteresis-CFM control method for switched-capacitor DC-DC converter with output ripple reduction and load transient enhancement. The presented HHC strategy combines the strengths of hysteresis control and CFM control. During transient moments, the system employs coarse/fine frequency tuning to directly reach the target frequency region, while hysteresis control ensures that overshoot and undershoot remain within defined hysteresis boundaries. This approach significantly reduces the overshoot and undershoot during load transitions. During steady state, the CFM control with 10-phase time-interleaving structure well regulated the output voltage to the minimum output voltage ripple. The proposed system adopts a RSC topology with adaptive switch sizing, capacitor sizing and 10-phase time-interleaving to achieve configurable VCR and high PCE across an extended input-output range. Experimental results demonstrate the effectiveness of the HHC RSC converter, it achieves significantly lower onvershoot and undershoot at 50mV during load transitions, and minimal output voltage ripple at 12mV during steady state CFM operations. The PCE of the system has been test in both open loop and close loop condition and achieve 82% and 80.6% respectively, the comparison with state-of-the-art DC DC converters shows the proposed converter achieves the lowest voltage ripple and over/undershoot voltage at a larger load transient step. In conclusion, the proposed HHC SCPC combines the strengths of hysteretic control and CFM control to achieve superior transient and steady-state performance, making it a promising solution for various applications requiring efficient power conversion.

6.2 Future work

6.2.1 Advanced time-interleaving

As discussed previously, the time-interleaving technique serves the dual purpose of reducing voltage ripple and enhancing transient speed. Additionally, it can be harnessed to augment conversion efficiency. Through the implementation of soft-charge and charge

redistribution techniques, coupled with the utilization of a scalable SC topology, the converter's efficiency can be further improved.

6.3 Ultra-low load condition

In ultra-low load conditions, the system may enter a frequency-jumping hysteresis control mode. This occurs because the charge pumped per cycle is too high, triggering a voltage boundary. To address this issue, a technique involving the transfer of capacitors between the flying capacitor and output capacitor can be implemented. During ultra-low load conditions, some power cells will be deactivated, effectively converting the flying capacitor into an output capacitor. This action reduces the charge pumped per cycle during ultra-low load conditions and increases the buffer capacity, leading to a reduction in ripple. Consequently, this expands the load transition range, decreases voltage ripple at ultra-low load conditions, and improves overall system performance.

6.4 Frequency region searching algorithm

During transient states, the system undergoes a coarse-fine frequency region searching scheme. Although it can limit the output voltage within an acceptable boundary, this process is still too slow to locate the final suitable region. An algorithm for this searching scheme can be improved by incorporating the SAR algorithm, which can significantly accelerate the process.

Bibliography

[1] Toke M. Andersen, Florian Krismer, Johann W. Kolar, Thomas Toifl, Christian Menolfi, Lukas Kull, Thomas Morf, Marcel Kossel, Matthias Brändli, Peter Buchmann, and Pier Andrea Francese. A 4.6w/mm2 power density 86dc-dc converter in 32 nm soi cmos. In *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 692–699, 2013.

[2] Toke Meyer Andersen, Florian Krismer, Johann Walter Kolar, Thomas Toifl, Christian Menolfi, Lukas Kull, Thomas Morf, Marcel Kossel, Matthias Brändli, Peter Buchmann, and Pier Andrea Francese. 4.7 a sub-ns response on-chip switched-capacitor dc-dc voltage regulator delivering 3.7w/mm2 at 90in 32nm soi cmos. In *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pages 90–91, 2014.

[3] Suyoung Bang, David Blaauw, and Dennis Sylvester. A successive-approximation switched-capacitor dc–dc converter with resolution of $v_{\text{in}}/2^N$ for a wide range of input and output voltages. *IEEE Journal of Solid-State Circuits*, 51(2):543–556, 2016.

[4] Nicolas Butzen and Michel S. J. Steyaert. Design of soft-charging switched-capacitor dc–dc converters using stage outphasing and multiphase soft-charging. *IEEE Journal of Solid-State Circuits*, 52(12):3132–3141, 2017.

[5] Nicolas Butzen and Michiel S. J. Steyaert. Scalable parasitic charge redistribution: Design of high-efficiency fully integrated switched-capacitor dc–dc converters. *IEEE Journal of Solid-State Circuits*, 51(12):2843–2853, 2016.

[6] U-Fat Chio, Kuo-Chih Wen, Sai-Weng Sin, Chi-Seng Lam, Yan Lu, Franco Maloberti, and Rui P. Martins. An integrated dc–dc converter with segmented frequency modulation and multiphase co-work control for fast transient recovery. *IEEE Journal of Solid-State Circuits*, 54(10):2637–2648, 2019.

[7] Hong-Wei Huang, Ke-Horng Chen, and Sy-Yen Kuo. Dithering skip modulation, width and dead time controllers in highly efficient dc-dc converters for system-on-chip applications. *IEEE Journal of Solid-State Circuits*, 42(11):2451–2465, 2007.

[8] Yang Jiang, Man-Kay Law, Pui-In Mak, and Rui P. Martins. A 0.22-to-2.4v-input fine-grained fully integrated rational buck-boost sc dc-dc converter using algorithmic voltage-feed-in (avfi) topology achieving 84.1In *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, pages 422–424, 2018.

[9] Wing-Hung Ki, Feng Su, and Chi-Ying Tsui. Charge redistribution loss consideration in optimal charge pump design. In *2005 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1895–1898 Vol. 2, 2005.

[10] Wonyoung Kim, David M Brooks, and Gu-Yeon Wei. A fully-integrated 3-level dc/dc converter for nanosecond-scale dvs with fast shunt regulation. In *2011 IEEE International Solid-State Circuits Conference*, pages 268–270, 2011.

[11] Hanh-Phuc Le, John Crossley, Seth R. Sanders, and Elad Alon. A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19w/mm2 at 73In *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pages 372–373, 2013.

[12] Hanh-Phuc Le, Seth R. Sanders, and Elad Alon. Design techniques for fully integrated switched-capacitor dc-dc converters. *IEEE Journal of Solid-State Circuits*, 46(9):2120–2131, 2011.

[13] Yutian Lei and Robert Carl Nikolai Pilawa-Podgurski. A general method for analyzing resonant and soft-charging operation of switched-capacitor converters. *IEEE Transactions on Power Electronics*, 30(10):5650–5664, 2015.

[14] Pengfei Li, Lin Xue, Peter Hazucha, Tanay Karnik, and Rizwan Bashirullah. A delay-locked loop synchronization scheme for high-frequency multiphase hysteretic dc-dc converters. *IEEE Journal of Solid-State Circuits*, 44(11):3131–3145, 2009.

[15] M.S. Makowski and D. Maksimovic. Performance limits of switched-capacitor dc-dc converters. In *Proceedings of PESC '95 - Power Electronics Specialist Conference*, volume 2, pages 1215–1221 vol.2, 1995.

[16] Ahmed M. Mohey, Sameh A. Ibrahim, Ismail M. Hafez, and HyungWon Kim. Design optimization for low-power reconfigurable switched-capacitor dc-dc voltage converter. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 66(10):4079–4092, 2019.

[17] Salem and Mercier. A recursive switched-capacitor dc-dc converter achieving $2^N - 1$ ratios with high efficiency over a wide output voltage range. *IEEE Journal of Solid-State Circuits*, 49(12):2773–2787, 2014.

[18] Seth R. Sanders, Elad Alon, Hanh-Phuc Le, Michael D. Seeman, Mervin John, and Vincent W. Ng. The road to fully integrated dc–dc conversion via the switched-capacitor approach. *IEEE Transactions on Power Electronics*, 28(9):4146–4155, 2013.

[19] Michael D. Seeman and Seth R. Sanders. Analysis and optimization of switched-capacitor dc–dc converters. *IEEE Transactions on Power Electronics*, 23(2):841–851, 2008.

[20] Thomas Souvignet, Bruno Allard, and Severin Trochut. A fully integrated switched-capacitor regulator with frequency modulation control in 28-nm fdsoi. *IEEE Transactions on Power Electronics*, 31(7):4984–4994, 2016.

[21] Tom M. Van Breussegem and Michiel S. J. Steyaert. Monolithic capacitive dc-dc converter with single boundary–multiphase control and voltage domain stacking in 90 nm cmos. *IEEE Journal of Solid-State Circuits*, 46(7):1715–1727, 2011.

[22] Yuanfei Wang, Mo Huang, Yan Lu, and Rui P. Martins. A continuously scalable-conversion-ratio sc converter with reconfigurable vcf step for high efficiency over an extended vcr range. In *2023 IEEE International Solid- State Circuits Conference (ISSCC)*, pages 1–3, 2023.