A Self-Regulating Bias-Flip Rectifier for Piezoelectric Energy Harvesting

Xinling Yue, Yiwei Zou, and Sijun Du, *Senior Member, IEEE*

***Abstract*—Piezoelectric energy harvesting (PEH) efficiently converts ambient kinetic energy into electrical power, enabling sustainable, and autonomous operation of low-power electronic devices. To optimize power extraction, maximum power point tracking (MPPT) methods are commonly employed. Conventional MPPT approaches, such as perturb-and-observe and fractional open-circuit voltage, typically rely on incremental power measurements or theoretical voltage estimations, but suffer from high power overhead, slow convergence, and circuit complexity. Duty-cycle-based MPPT techniques partly overcome these limitations by regulating the rectifier's duty cycle at 50%, yet they still require a dedicated MPPT stage and large external capacitors, causing additional power loss and delayed convergence. To address these challenges, this article presents a self-regulating bias-flip rectifier that inherently integrates rectification and MPPT into a single stage, eliminating cascaded energy losses and enabling rapid convergence to the maximum power point. Fabricated in a 0.18-μm CMOS process, the proposed rectifier achieves an end-to-end efficiency of 93%, MPPT efficiency of 98%, and provides a 7.7-fold improvement in energy extraction compared to conventional full-bridge rectifiers.**

***Index Terms*—Autonomous self-regulating, duty-cycled-based (DCB) MPPT, energy harvesting, maximum power point tracking (MPPT), piezoelectric transducer (PT).**

I. Introduction

With the rapid expansion of the Internet of Everything (IoE), wireless sensors play a crucial role in seamlessly bridging the physical world with digital networks. To enable these sensors to operate autonomously without frequent maintenance, energy harvesting has emerged as a key technology, allowing low-power devices to be self-sustained. Among various energy harvesting techniques, piezoelectric energy harvesting (PEH) is a promising solution for converting ambient kinetic energy into usable electrical power, particularly in applications such as health monitoring [1] and wearable electronics [2], where battery replacement is impractical. Compared to other energy harvesting methods, PEH offers relatively high power density [3], [4], [5] and scalability.

A typical piezoelectric transducer (PT) is modeled as a sinusoidal current source I_P in parallel with a capacitor C_P [6], [7], [8], [9] under weak coupling conditions, generating an ac voltage. To make this energy usable, a rectifier is required to convert the ac output into a stable dc voltage. The full-bridge rectifier (FBR) is the most widely adopted rectification solution due to its simplicity; however, it suffers from significant energy losses caused by the high voltage thresholds that must be overcome before energy can be extracted [10]. To improve power extraction, various active rectification techniques have been proposed [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], among which the synchronized switch harvesting on inductor (SSHI) rectifier has demonstrated one of the highest energy extraction efficiencies [6]. This technique operates by flipping the voltage across the PT, V_{PT}, synchronously using a switched inductor to reduce energy losses that would otherwise be used to build up V_{PT}.

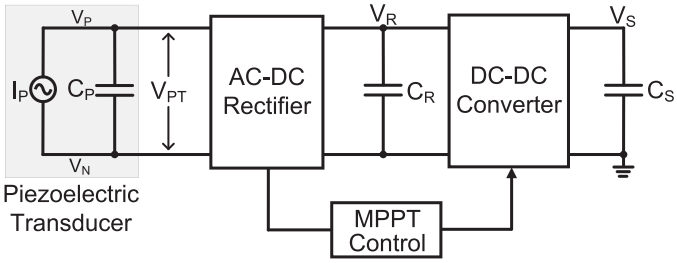

Fig. 1. Diagram of a typical PEH system with MPPT.

To further enhance power extraction performance, maximum power point tracking (MPPT) techniques are widely employed in PEH systems [30], [31], [32], [33], [34]. Fig. 1 illustrates a typical PEH system with MPPT, where the ac–dc rectifier converts the PT output into dc, followed by an MPPT controller that ensures operation at the optimal power point. Traditional MPPT methods, such as perturb-and-observe (P&O) and fractional open-circuit voltage (FOCV), rely on open-circuit voltage sampling or iterative power tracking. However, these approaches suffer from high power consumption, complex circuitry, and slow convergence. A duty-cycle-based (DCB) MPPT algorithm [32], [35], [36] was first introduced to regulate the duty cycle of the ac–dc rectifier at 50%, offering an alternative approach. While effective, it still requires a dedicated MPPT stage and a large external rectified capacitor, C_R, leading to prolonged convergence times and additional energy losses due to the cascaded energy transfer from C_P to C_R and then to C_S. Yue and Du [36] integrated MPPT but counts duty cycle with a MHz digital clock, which introduces complex digital timing,

Received 19 April 2025; revised 1 September 2025; accepted 27 September 2025. Date of publication 1 October 2025; date of current version 19 January 2026. Recommended for publication by Associate Editor S. N. Banavath. *(Corresponding author: Sijun Du.)*

The authors are with the Department of Microelectronics, Delft University of Technology, 2628CD Delft, The Netherlands (e-mail: sijun.du@tudelft.nl).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2025.3616400.

Digital Object Identifier 10.1109/TPEL.2025.3616400

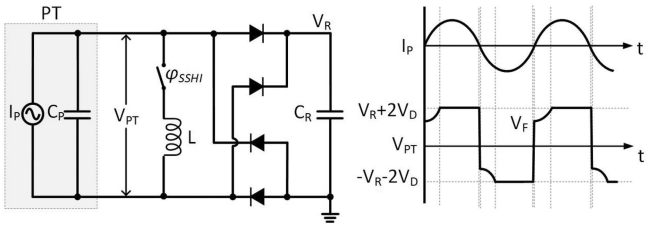

Fig. 2. Circuit diagram and associated waveforms of a conventional SSHI rectifier.

quantization/latency in duty-cycle updates, and power overhead for the clock and digital logic. The first integration should be applied to electromagnetic (EM) energy harvesting and integrated with impedance matching technique [37], [38], [39]. However, for PEH, there are less work investigated. Especially, when the bias-flipping technique was invented in 2009 in [6], impedance matching becomes difficult due to its semi-square waveform. That's the reason why P&O and FOCV are popular for MPPT. However, using P&O and FOCV is hard to integrated ac–dc and dc–dc into a single stage. For P&O, it has to calculate the power at different voltage levels in order to track its maximum power point (MPP), which means that the single regulation is impossible. Although conventional FOCV MPPT can be theoretically integrated into one stage but has to limited reference to report this and it has to sample the open-circuit voltage, which is an inherent drawback.

To address these limitations, this article proposes a self-regulating bias-flip rectifier that achieves MPPT without requiring a separate MPPT stage or an external rectified capacitor. The proposed rectifier employs a half-DCB (H-DCB) MPPT algorithm, which directly controls the PT voltage build-up time to reach the MPP voltage, V_{MPP}, within each half-cycle. Once V_{MPP} is reached, the ac–dc rectifier conducts, extracting energy efficiently while eliminating the delays and energy losses associated with conventional MPPT techniques.

The rest of this article is organized as follows: Section II introduces the self-regulating bias-flip rectifier concept and the H-DCB MPPT method. Section III presents the theoretical analysis of the proposed design. Section IV describes the system architecture, while Section V details the circuit implementation. Measurement results are discussed in Section VI. Finally, Section VII concludes this article.

II. Theoretical Analysis

A. Output Power Analysis of a Conventional SSHI Rectifier

Fig. 2 illustrates the circuit topology and associated waveforms of a conventional SSHI rectifier. The SSHI technique enhances energy extraction by flipping the voltage across the PT (PT) at each zero-crossing of the input current I_P. The switch ϕ_{SSHI} momentarily closes, forming a resonant loop with the inductor L and capacitor C_P, enabling the voltage inversion process.

The effectiveness of this voltage flipping process is quantified by the flip efficiency η_F, defined as the ratio of the postflip voltage to the preflip voltage

$$\eta_F = \frac{V_F}{V_R + 2V_D} \tag{1}$$

where V_F is the flipped voltage, V_R is the rectified output voltage, and V_D is the diode voltage drop. The flip efficiency η_F depends on the quality factor of the resonant loop and is expressed as follows:

$$\eta_F = e^{-\frac{\pi}{\sqrt{\frac{4L}{R^2C_P}-1}}}. \tag{2}$$

The output power of an SSHI rectifier can be derived by evaluating the charge transfer per cycle [17]

$$P_{\text{SSHI}} = 2f_P C_P V_R(2V_{\text{OC}} - (1-\eta_F)(V_R + 2V_D)) \tag{3}$$

where f_P is the frequency of the PT, V_{OC} is the open-circuit zero-to-peak voltage, and C_P is the equivalent transducer capacitance.

For maximum power extraction, the rectifier output voltage should be set to

$$V_R = \frac{V_{\text{OC}}}{1-\eta_F} - V_D. \tag{4}$$

Substituting this into (3), the maximum output power of the SSHI rectifier is obtained as follows:

$$P_{\text{SSHI,max}} = 2f_P C_P \frac{V_{\text{OC}}^2}{1-\eta_F} \tag{5}$$

assuming V_D is negligible.

However, achieving the exact MPP voltage V_R is challenging due to the strong dependency of η_F on inductor values and parasitics. Prior works [16] have applied P&O MPPT algorithms to dynamically adjust V_R. While effective, these approaches suffer from slow convergence and high power consumption, requiring tens to hundreds of cycles for stability. To overcome these limitations, we propose a self-regulating bias-flip rectifier, which eliminates the need for complex MPPT tracking by directly regulating the PT voltage.

B. Proposed Self-Regulating Bias-Flip Rectifier

Unlike conventional SSHI rectifiers that regulate the rectified output voltage, the proposed self-regulating bias-flip rectifier regulates the PT voltage directly, ensuring that it remains at the MPP. As shown in Fig. 3, the operation of the proposed rectifier is divided into three distinct phases, similar to the SSHI rectifier:

1) *Phase ϕ_1 (Voltage Build-up):* The PT voltage V_{PT} builds up from V_F to V_m, where V_m is the optimal voltage corresponding to the MPP.
2) *Phase ϕ_2 (Energy Extraction via dc–dc Converter):* Instead of relying on an FBR for rectification, a dc–dc converter is conditionally activated when V_{PT} exceeds V_m. The energy is directly transferred from C_P to the storage capacitor, avoiding cascaded losses.
3) *Phase ϕ_3 (Voltage Flipping):* The voltage across V_{PT} is flipped using an inductor, similar to the SSHI technique, reducing unnecessary voltage buildup losses.

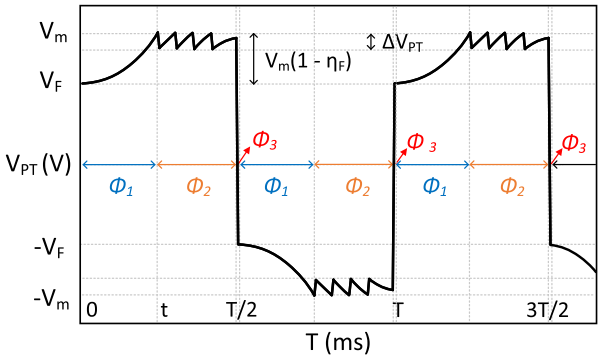

Fig. 3. Waveforms of the proposed self-regulating bias-flip rectifier.

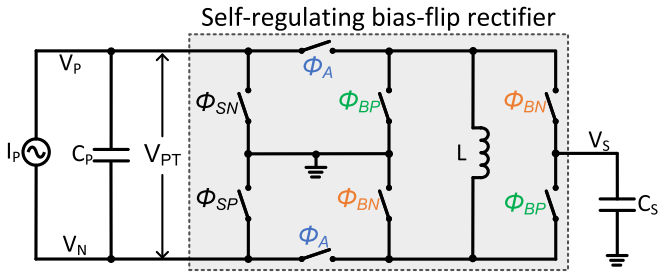

Fig. 4. Topology of the proposed self-regulating bias-flip interface.

By ensuring direct voltage regulation at the PT level, this approach eliminates slow MPPT convergence issues and minimizes energy losses associated with cascaded power transfer stages.

C. Derivation of the H-DCB Self-Regulating Period

To maintain operation at the MPP, the PT voltage build-up time must be carefully controlled. The PT current can be expressed as

$$I_P = I_0 \sin(\omega t) \tag{6}$$

where I_0 is the peak current and ω is the angular frequency.

The open-circuit peak voltage of the PT, V_{OC}, is related to I_P as [17]

$$V_{\text{OC}} = \frac{I_0}{\omega C_P}. \tag{7}$$

Assuming that ϕ_1 lasts for a time duration t, the voltage build-up equation is

$$V_m(1-\eta_F) = \frac{\int_0^t I_0 \sin(\omega t)dt}{C_P}. \tag{8}$$

Substituting (7) into (8), we obtain

$$V_m(1-\eta_F) = V_{\text{OC}}(1-\cos(\omega t)) \tag{9}$$

To determine the optimal energy extraction, we differentiate

$$\frac{dE_{\text{out}}}{dV_m} = \eta_{\text{dcdc}} V_{\text{OC}} C_P (1+\cos(\omega t) - (1-\cos(\omega t))). \tag{10}$$

Setting this to zero leads to

$$\cos(\omega t) = 0 \quad \Rightarrow \quad t = \frac{T}{4} \tag{11}$$

where $T = \frac{1}{f_P}$ is the period of the PT vibration.

This result forms the basis of the H-DCB MPPT algorithm, which ensures that ϕ_1 and ϕ_2 each last one-quarter of the period. By enforcing this timing, the rectifier self-regulates V_{PT} to remain at MPP, avoiding the need for external MPPT control.

This self-regulating behavior allows the proposed rectifier to adaptively achieve MPPT without the need for iterative voltage estimation or additional power-hungry control blocks. Even if the system starts away from the MPP, it naturally converges within a few cycles, making it highly efficient for PEH applications.

III. Proposed Self-Regulating Bias-Flip Rectifier

The circuit topology of the proposed self-regulating bias-flip rectifier is illustrated in Fig. 4. Unlike conventional designs, this topology does not require a FBR, significantly simplifying the interface by employing an inductor and eight controlled switches. This integrated structure allows the proposed rectifier to directly manage the PT voltage V_{PT}, optimizing energy transfer and minimizing cascaded energy losses.

The operating principle of the proposed rectifier can be separated into three distinct phases: voltage build-up (ϕ_1), direct dc–dc energy transfer (ϕ_2), and voltage flipping (ϕ_3). This approach leverages the H-DCB MPPT algorithm, ensuring that the PT voltage always reaches the optimal MPP level, denoted as V_m, during each vibration cycle. By enforcing equal durations for phases ϕ_1 and ϕ_2, the rectifier inherently converges to the MPP without requiring complex MPPT control circuitry.

Fig. 5 provides detailed configurations of the switches and current flow paths during the three operational phases for the positive half-cycle ($V_{\text{PT}} > 0$). In phase ϕ_1, the PT voltage increases from the flipped voltage V_F to the target MPP voltage V_m. The switch ϕ_{SP} (or ϕ_{SN} for $V_{PT} < 0$) ensures that the PT's lower node remains grounded, preventing floating nodes and unstable voltages.

When the MPP voltage level is reached, the system transitions to phase ϕ_2. During this phase, the circuit operates as a non-inverting buck–boost dc–dc converter, efficiently transferring energy directly from the PT capacitor C_P to the storage capacitor C_S. The two switches labeled ϕ_A close first, forming a resonant loop between I_P, C_P, and inductor L, partially transferring energy to L. The duration of the ϕ_A conduction is precisely controlled by a 3-bit digital signal to regulate the voltage change ΔV_{PT} within ϕ_2. After ϕ_A switches turn OFF, switches ϕ_{BP} (or ϕ_{BN} for negative polarity) activate to transfer the stored energy from the inductor to C_S. An integrated zero-current detector (ZCD) ensures these switches turn off precisely when the inductor current reaches zero, maximizing efficiency and minimizing losses.

Phase ϕ_3 involves voltage flipping, triggered when a peak detector identifies the zero-slope point of V_{PT}. Switches ϕ_A close again to create a resonant loop with C_P and L, rapidly reversing the PT voltage from V_m to $-\eta_F V_m$ (or vice versa), preparing

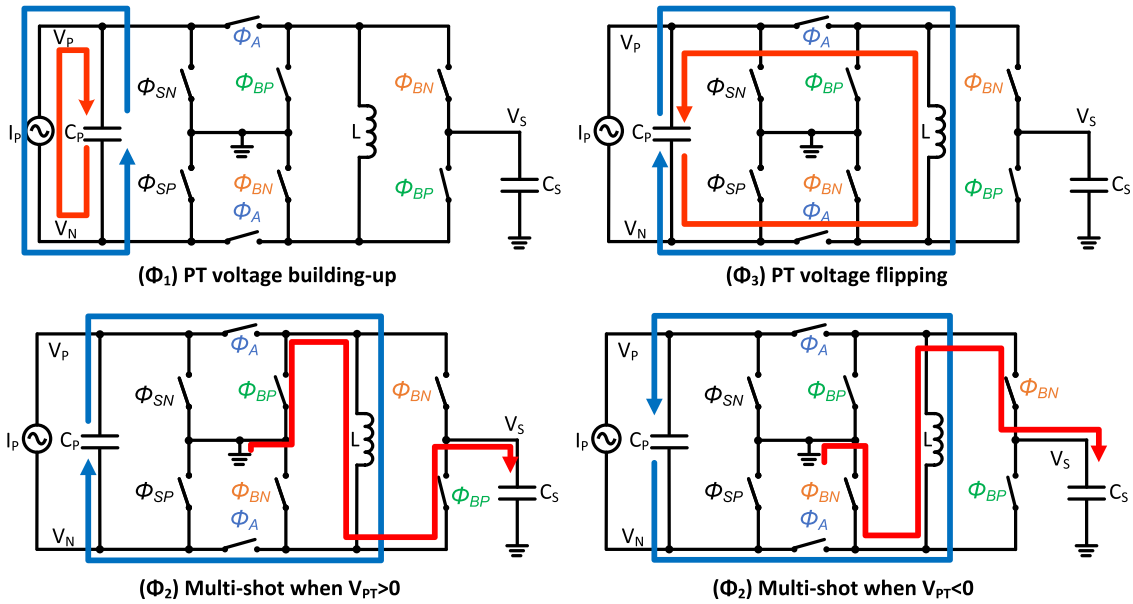

Fig. 5. Detailed switch configuration and current flow for each operational phase in the proposed self-regulating bias-flip interface.

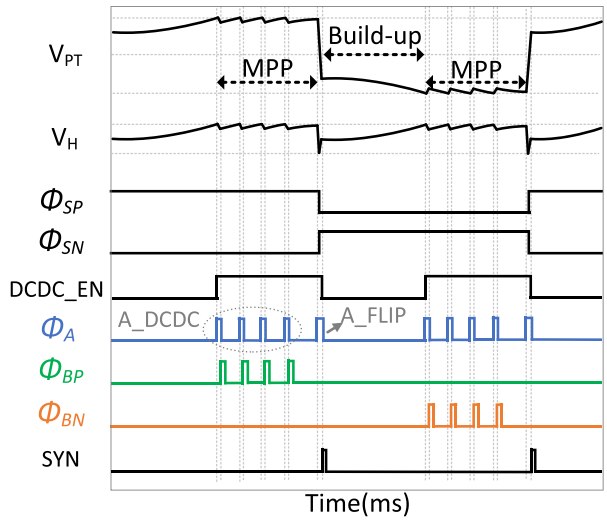

Fig. 6. Switching waveforms and control signals during operation.

the system for the subsequent half-cycle. The duration of this phase is carefully controlled using a 4-bit digital signal, ensuring consistent and precise timing.

Fig. 6 shows the detailed waveforms of the switching phases and associated control signals during typical operation. The polarity-sensitive signals ϕ_{SP} and ϕ_{SN} guide the rectifier's switching state. A synchronous half-duty-cycle signal, DCDC_EN, generated by the half-time generator, precisely defines the active period of the dc–dc converter. At each rising edge of DCDC_EN, the voltage V_{PT} is sampled to set the optimal reference voltage V_m. During phase ϕ_2, each energy transfer is initiated when $|V_{\mathrm{PT}}|$ exceeds V_m, resulting in an efficient and direct energy extraction without cascading losses typically observed in conventional MPPT methods.

IV. System Architecture

The top-level architecture of the proposed self-regulating bias-flip rectifier, illustrated in Fig. 7, comprises two main blocks: the power stage and the switch control circuitry. The power stage integrates eight switches specifically arranged to facilitate efficient energy transfer and voltage flipping without the need for a FBR.

The switches ϕ_{SP} and ϕ_{SN}, as well as the left-side switches ϕ_{BP} and ϕ_{BN}, are implemented using NMOS transistors ($M_{N0} \sim M_{N3}$), as their terminals are directly connected to ground. Conversely, the right-side switches ϕ_{BP} and ϕ_{BN} utilize PMOS transistors (M_{P0}, M_{P1}) due to their connection to the higher-voltage output node, V_S. To prevent unwanted conduction through body diodes, these PMOS transistors incorporate dedicated bulk regulation circuits [18]. The TGs serve as switches ϕ_A due to their capability to efficiently handle both low and high voltage levels during different operation phases.

All switches in the power stage are driven by five dedicated level-shifter buffers. Each buffer contains a level shifter to elevate the gate control signals to the higher operating voltage V_{DDA}, followed by an inverter chain to strengthen and sharpen signal transitions, ensuring reliable switch actuation.

The switch control circuitry is responsible for generating precise gate-driving signals, which orchestrate the systematic operation of the rectifier. It consists of multiple functional blocks: polarity-based PN switch control, half-time generator, peak detector, ZCD, dc–dc control block, and max voltage selectors.

Specifically, the PN switch control block determines the polarity of the PT voltage (V_{PT}) and accordingly generates signals ϕ_{SP} and ϕ_{SN}. The half-time generator monitors the PT vibration period and produces the half-duty-cycle enable signal DCDC_EN, defining the dc–dc converter's operational timing window. Within this window, the dc–dc control block, aided

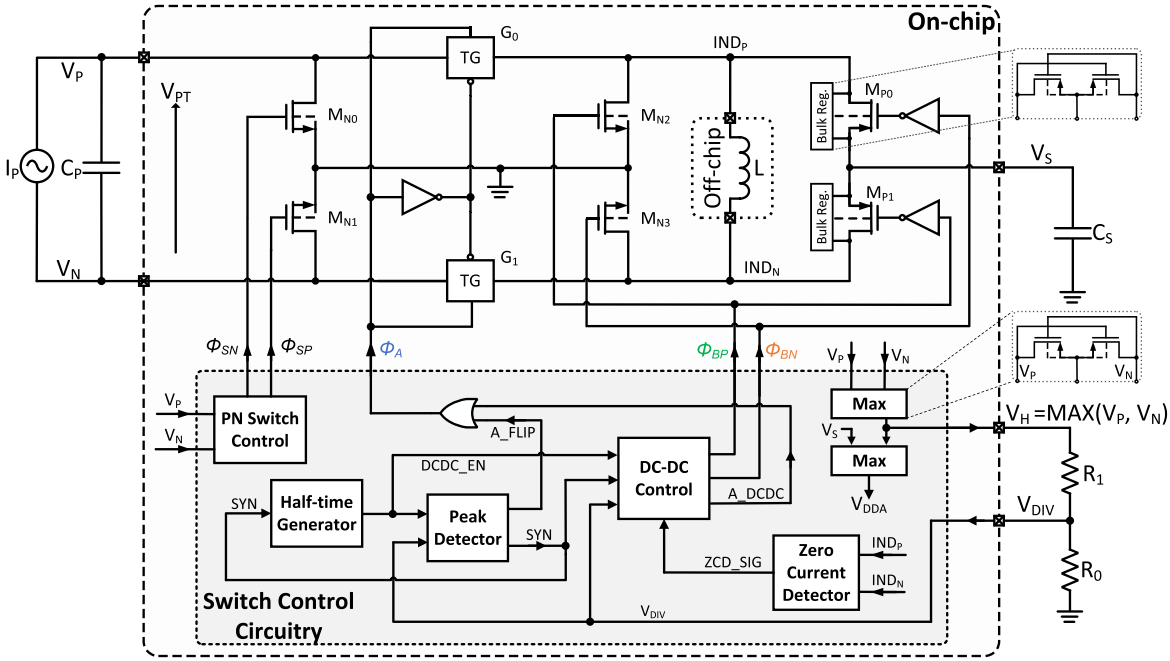

Fig. 7. Top-level system architecture of the proposed self-regulating bias-flip rectifier.

by zero-current detection, executes a noninverting buck-boost conversion, ensuring V_{PT} remains at the optimal voltage V_m.

The dc–dc control block initiates each energy transfer cycle with a fixed-length signal A_DCDC, immediately followed by a variable-length conduction phase (ϕ_{BP} or ϕ_{BN}). The conduction duration is precisely terminated by the ZCD, minimizing energy loss. The peak detector monitors for the zero-slope condition of V_{PT}, initiating the voltage flipping phase with the signal A_FLIP, subsequently indicated complete by the SYN signal.

Last, two max voltage selectors, sharing an identical schematic with the bulk regulators, generate critical supply voltages: the rectified PT voltage waveform V_H and the elevated supply voltage V_{DDA}, the latter selected as the maximum between V_H and the storage capacitor voltage V_S. A reduced fraction V_{DIV} of V_H is provided to the peak detector and dc–dc control block to reduce their input voltage range requirements, improving system robustness.

V. Circuit Implementations

A. Level-Shifter

The schematic in Fig. 8 illustrates the level shifter used in Fig. 7, which consists of two primary sections: a level shifter and an inverter chain. The level shifter is responsible for translating an input signal at a lower voltage level (V_{DD}) to a higher voltage domain (V_{DDA}). This is achieved using a cross-coupled PMOS transistor pair, which enhances noise immunity and ensures reliable signal conversion. The circuit also includes additional NMOS transistors to control the switching operation and stabilize the transition. The output of the level shifter feeds into an inverter chain composed of four cascaded inverters, which serve to amplify and sharpen the signal edges, ensuring robust signal propagation at the desired voltage level. This design is essential

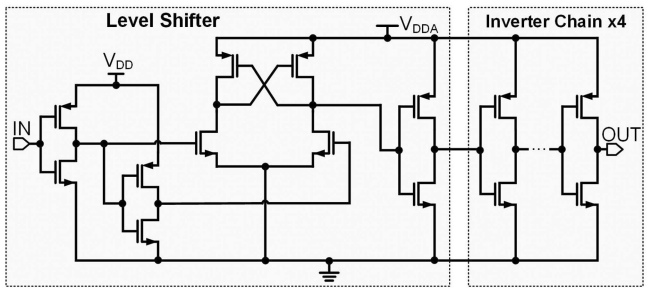

Fig. 8. Schematic of the level shifter buffer.

for interfacing circuits operating at different voltage domains, improving compatibility and signal integrity in mixed-voltage systems.

B. PN Switch Control

The switching phases of ϕ_{SP} and ϕ_{SN} are determined by the polarity of V_{PT}: when $V_{\mathrm{PT}} > 0$, ϕ_{SP} is closed, whereas when $V_{\mathrm{PT}} < 0$, ϕ_{SN} is activated. A comparator is employed to determine the polarity of V_{PT}, and a series of logic gates are integrated to generate the corresponding control signals for ϕ_{SP} and ϕ_{SN}, as shown in Fig. 9. In addition, a transmission gate (TG) is incorporated to ensure that both PN signals experience the same propagation delay, thereby maintaining timing consistency. When the reset signal (RST) is triggered, both PN and $\overline{PN}$ experience the same propagation delay, thereby maintaining timing consistency. When the reset signal (RST) is triggered, both ϕ_{SP} and ϕ_{SN} are simultaneously activated to set V_{PT} to zero ensuring that the system starts from a well-defined initial state rather than an undefined or unpredictable condition.

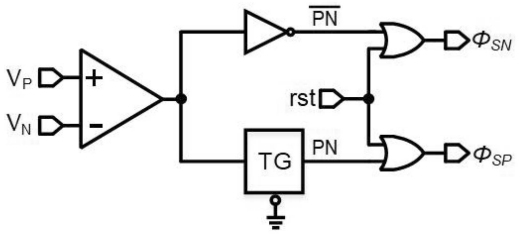

Fig. 9. Switching phases generation.

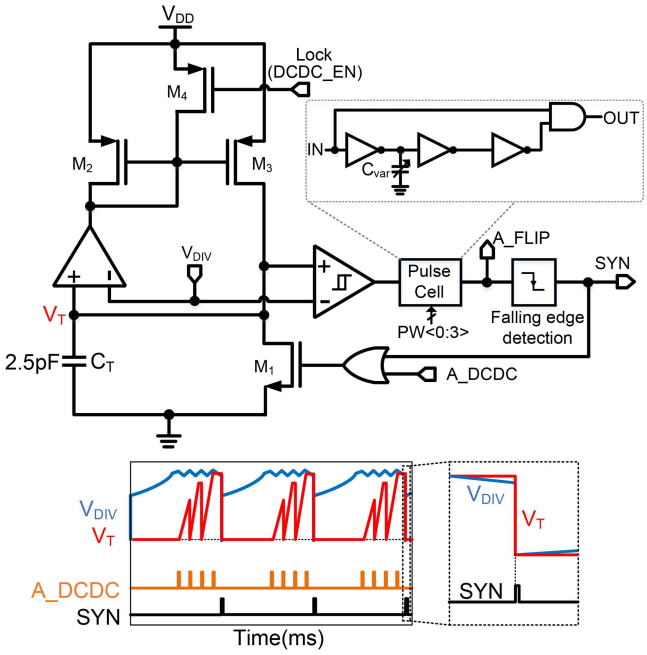

Fig. 10. Circuit diagram of the peak detector.

C. Peak Detector

Fig. 10 shows the circuit diagram of the peak detector for detecting the zero-crossing moment of I_P and some corresponding waveforms. The circuit implementation is composed of a voltage tracker, a hysteresis comparator, and some signal generation cells. When V_{DIV} in the voltage tracker is rising, M_2 and M_3 are turned ON and will charge a C_T so that the voltage V_T can follow the ascent of V_{DIV}. When V_{DIV} just begins to decrease, V_T will be held on C_T, and the hysteretic comparator will rise from low to high. In this way, the peak in V_{DIV} can be detected. The MOSFET M_1 is used to clear the charge on C_T to reset the state of the voltage tracker, while M_4 is used to disable and lock the voltage tracker during off-state. When a peak voltage is detected, the pulse cell will generate a A_FLIP pulse to turn on the switch ϕ_A to activate the voltage flipping. When the A_FLIP pulse is over, a SYN signal will be produced by the falling edge detection circuit, which has a similar structure to the pulse cell.

The bottom waveform shows the voltage of V_{DIV}, V_T, A_DCDC, and SYN signals. Every time, when the A_DCDC is high, V_{DIV} starts to drop, and the V_T hold on the initial voltage value of V_{DIV}. A synchronized signal (SYN) is generated when the V_T is higher than the voltage V_{DIV} as shown in the right zoomed-in figure.

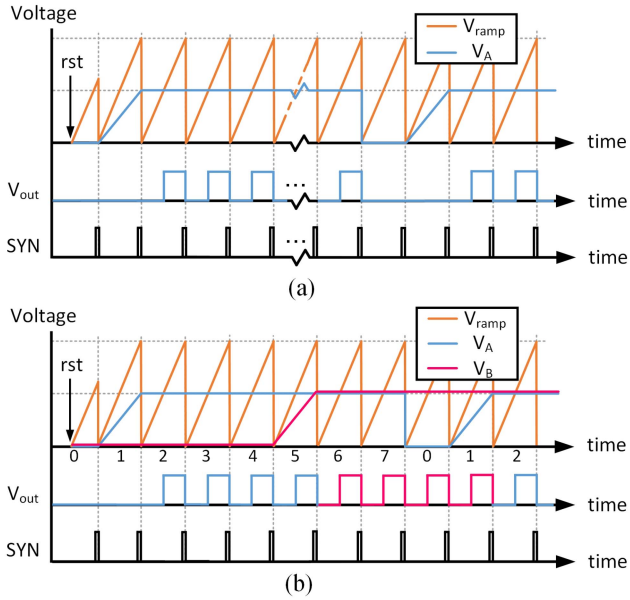

Fig. 11. Waveform of the half-time generator with (a) two capacitors and (b) three capacitors.

D. Half-Time Generator

Based on the previous derivation of H-DCB MPPT in Section II, the optimal V_m can be achieved by making the lengths of ϕ_1 and ϕ_2 equal, hence reducing the need for a voltage reference and complicated voltage calculation. In order to realize the H-DCB-based MPPT, a half-time generator is designed to record the half-period $T/2$ of I_P and generate a half-duty-cycle signal. With the SYN signal output by the peak detector, it can sense the period of PT and turn it into a voltage by using a constant current source to charge an on-chip capacitor. A half-duty-cycle signal can be generated by using the same current to charge another capacitor with half capacitance.

Fig. 11(a) shows the operating waveform of the half-time generator with two capacitors. By comparing V_{ramp} and V_A, which are the voltages on the two capacitors, a half duty-cycle signal V_{out} can be generated. However, since the charge stored on the capacitor of V_A will leak slowly, it needs to be refreshed periodically. Because each refreshing process requires two half cycles to complete, V_{out} is inconsecutive when V_A refreshes, which is undesired. To solve this problem, a three-capacitor topology is proposed, the waveform of which is depicted in Fig. 11(b). Two identical capacitors are used to hold the voltages, and their refreshing time is staggered so that by comparing V_{ramp} with V_A and V_B during different periods, we can obtain a continuous V_{out}. In this design, a base eight counter is employed, which means each capacitor is refreshed after eight SYN signals. In this way, the capacitance of the two capacitors can be relatively small, and the chip area is reduced.

Fig. 12 illustrates the schematic of the proposed capacitor charger within the half-time generator. The circuit consists of a cascode current mirror and three branches dedicated to charging capacitors C_1 through C_3. The transistors M_1 to M_3 serve the purpose of clearing any residual charge on C_1 to C_3, ensuring

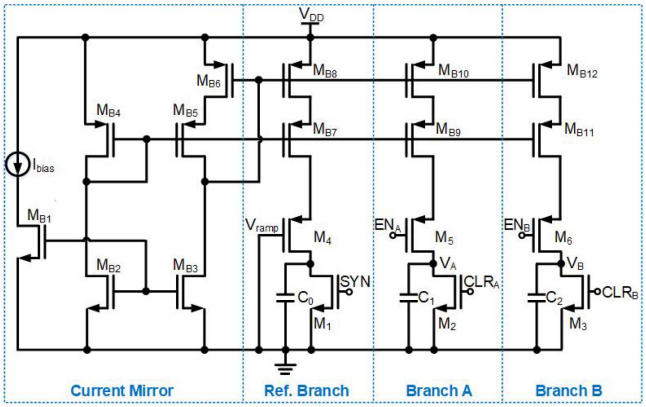

Fig. 12. Schematic of the capacitor charger in the half-time generator.

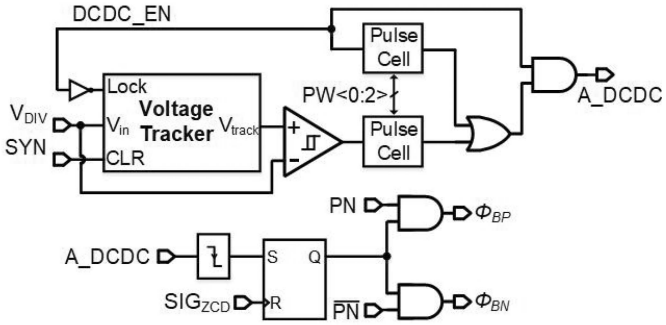

Fig. 13. Diagram of the DC–DC control block.

proper initialization before each charging cycle. Transistors M_5 and M_6 are responsible for controlling the charging process in Branch A and Branch B, allowing precise charge distribution. Each branch is designed to carry a current of 2 nA, and the capacitance values are set as $C_1{=}C_2{=}2C_0{=}10$ pF. As a result, the voltage rise on C_1 and C_2 within a half-cycle is approximately 500 mV, ensuring stable and predictable capacitor charging behavior. This structure is essential for achieving accurate timing in the half-time generator.

E. DC–DC Control

Fig. 13 shows the circuit diagram of the dc–dc control block. It is also based on the voltage tracker circuit, as illustrated in Fig. 10. The voltage tracker's output V_{track} will follow the ascent of V_{DIV} until dcdc_EN signal rises from low to high, which will lock the value of V_{track} at that moment and also trigger the pulse cell to generate a A_dcdc signal. From then on, whenever $|V_{\text{PT}}|$ exceeds the level of V_m, the hysteresis comparator will output a rising edge and the pulse cell will produce a A_dcdc to start a new energy transfer process. During the dc–dc conversion, each ϕ_A (A_dcdc) is followed by a ϕ_{BP} (or ϕ_{BN}, depending on the polarity of V_{PT}), whose pulse width is determined by the ZCD_SIG generated by the ZCD. When the energy transfer and voltage flipping are over, the SYN signal will release the charge stored on the capacitor, and V_{track} is capable of tracking V_{DIV} afterward.

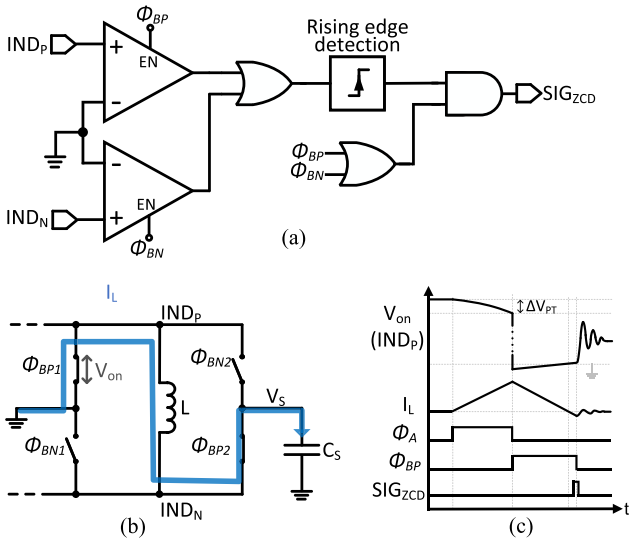

Fig. 14. ZCD: (a) Circuit diagram of the ZCD; (b) Diagram of the interface circuit when the inductor charges C_S during DC-DC conversion. (c) Waveform of one energy transfer process (when $V_{PT} > 0$).

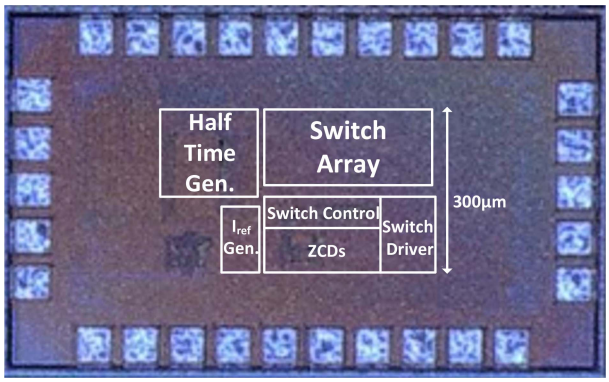

Fig. 15. Chip micrograph.

F. Zero Current Detector

To detect the inductor current zero-crossing in the dc–dc conversion to switch off the converter, a ZCD is proposed, as shown in Fig. 14(a). From Fig. 14(b) and (c), it can be noticed that when the inductor charges the capacitor C_S (ϕ_{BP} or ϕ_{BN}) during the energy transfer, the voltage drop V_{on} across the switch ϕ_{BP1} (or ϕ_{BN1}) remains negative until the inductor current polarity is reversed. Therefore, we can use comparators to detect the voltage zero-crossing of IND_P and IND_N to generate the ZCD signal, as shown in Fig. 14(a). Meanwhile, in order to balance the trade-off between speed and power consumption, each comparator consumes a relatively large average quiescent current of 2 μA, but they are only activated when they need to function (ϕ_{BP} or ϕ_{BN}) and no power is consumed during off-state.

VI. Measurement Results

The proposed rectifier was fabricated using a 180-nm BCD process, occupying an active chip area of 0.156 mm^2. The chip micrograph, shown in Fig. 15, identifies key blocks including the half-time generator, reference current generator, switch array

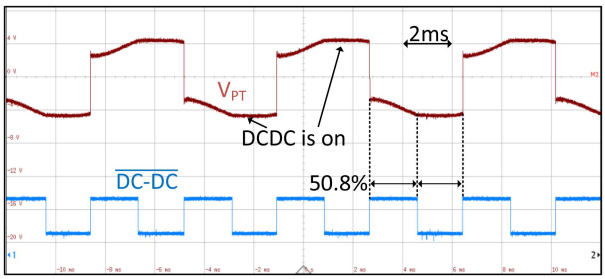

Fig. 16. Measured waveform of PT voltage and DC–DC signal.

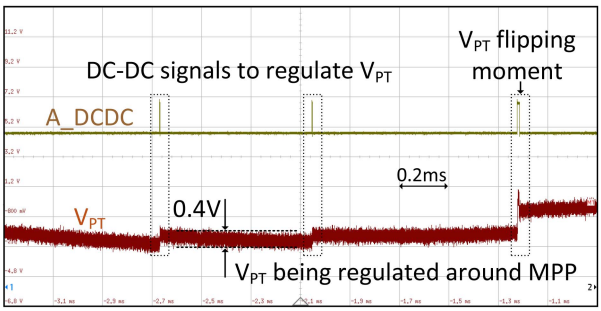

Fig. 17. Measured waveform of PT voltage and DC–DC signal.

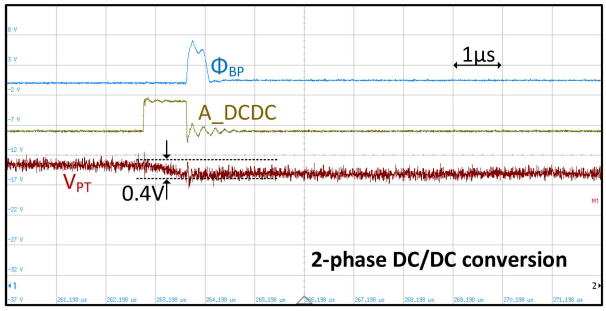

Fig. 18. Measured zoomed-in waveform of V_{PT} and 2-phase DC/DC conversion switching signals.

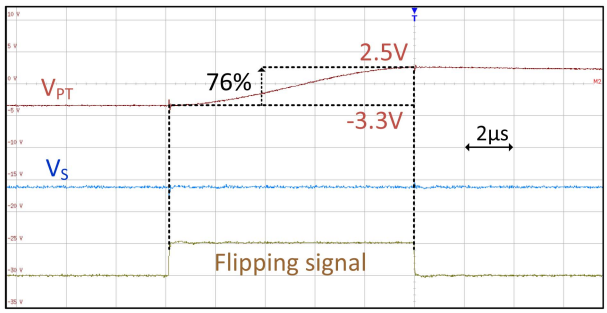

Fig. 19. Measured waveform of PT voltage and DC–DC signal.

and control circuits, ZCD, and switch driver block. The tested PT (S129-H5FR-1803YB) has a capacitance of 23 nF and operates optimally at a resonant frequency of 130 Hz. The employed inductor is WE-TI Radial Leaded Wire Wound Inductor with inductance of 220 μH.

Fig. 16 presents the measured waveform of the PT voltage, V_{PT} and the inverted dc–dc signal. The red waveform represents V_{PT}, while the blue waveform corresponds to the inverted dc–dc switching signal. The figure highlights the correlation between the operation of the dc–dc converter and the variations in V_{PT}. When the inverted dc–dc signal is high, indicating that the rectifier is inactive, and when it is low, the rectifier is active. The duty cycle of the dc–dc signal is measured to be approximately 50.8%, ensuring balanced operation. This waveform analysis confirms the expected behavior of the dc–dc regulation and its impact on the PT voltage, validating the system's performance in maintaining stable maximum power conversion.

Fig. 17 provides a detailed view of the dc–dc conversion process, illustrating the regulation of the PT voltage (V_{PT}) and the corresponding dc–dc control phases (A_dcdc signal). During dc–dc operation, charge transfer from capacitor C_P to the inductor induces a slight drop in PT voltage, which remains regulated around the MPP. The measured voltage ripple during the dc–dc operation is approximately 0.4 V, ensuring stable power regulation. In addition, the A_dc–dc phase includes an OR-ed flipping phase, as indicated on the right. The zoomed-in figure of the A_dcdc signal and the flipping signal are shown in the following figure.

Fig. 18 presents a zoomed-in view of one dc/dc conversion cycle, illustrating the interaction between the switching signals A_dcdc and Φ_{BP}, which correspond to the two sub-phases of the energy transfer phase (Φ_2) depicted in Fig. 5. During phase Φ_A (pulse of A_dcdc), the inductor is energized by extracting energy from the PT, causing the voltage across the PT (V_{PT}) to drop. This phase ensures that the energy harvested from the PT is temporarily stored in the inductor before being transferred to the output. The amplitude of the voltage drop, approximately 0.4 V as highlighted in the figure, indicates the controlled nature of energy extraction, which prevents excessive loading of the PT and maintains V_{PT} around the MPP. Following this, in phase Φ_{BP}, the stored energy in the inductor is released and transferred to the storage capacitor, C_S. This process is marked by the activation of the Φ_{BP} signal, which enables the charge redistribution from the inductor to the capacitor.

Fig. 19 provides a detailed view of the PT voltage flipping moment, along with the corresponding flipping phase of the zoomed-in signal. In addition, it illustrates the storage voltage (V_S), offering insight into the overall energy transfer process. During the flipping moment, the PT voltage undergoes a rapid transition from -3.3 V to 2.5 V, highlighting the effectiveness of the flipping mechanism. This transition achieves a flipping

TABLE I
COMPONENT POWER BREAKDOWN

Component	Power Consumption	Percentage (%)
PN Switch	0.042 µW	3.6
ZCD	0.064 µW	5.5
DC-DC Control	0.085 µW	7.3
DC-DC ZCD	0.107 µW	9.1
LS + Driver	0.128 µW	10.9
Switches	0.149 µW	12.7
Half Time	0.170 µW	14.5
Current reference	0.192 µW	16.4
Other	0.213 µW	18.2
Total	1.170 µW	100

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUS WORK

	JSSC'14 [40]	JSSC'15 [41]	JSSC'16 [42]	JSSC'19 [43]	SSCL'19 [16]	JSSC'23 [22]	**This work**
Technology	350 nm	350 nm	350 nm	130 nm	130 nm	180 nm	180 nm
Technique	MS-SECE	FBR	SSHI	MS-SSHI	SSHI	SSHI	**SSHI**
C_P (nF)	23	11	27.5/20.8/9.6	22/14	20/100	42	**23**
Frequency (Hz)	1*	N/R	225	219	182/135	230	**130**
Inductor	Yes	No	Yes	Yes	Yes	Yes	**Yes/220μH**
V_{OC}(V)	20*	0.5*	2.5	2	1.6	1.2/2	**1/1.5**
Chip Area (mm^2)	3.6	5.6	1.17	0.53	1.07	0.47	**0.17**
MPPT?	No	Yes/FOCV	No	No	Yes/P&O	Yes/DCB	**Yes/DCB**
Cascaded Stage	2	2	1 (w/o MPPT)	1 (w/o MPPT)	2	2	**1**
Flipping Efficiency	No	No	81%	79%	86%	82%	**76%**
DCDC Efficiency	61%	80%	96.6%	N/R	75%	N/R	**93%**
MPPT Efficiency	N/R	99%	N/R	N/R	97%	98%	**98%**
P_{IC}/P_{FBR}	N/R	1.0×	6.81×	4.48×	4.17×	7.3×	**7.7×**

*: Estimated value. N/R: Not reported.

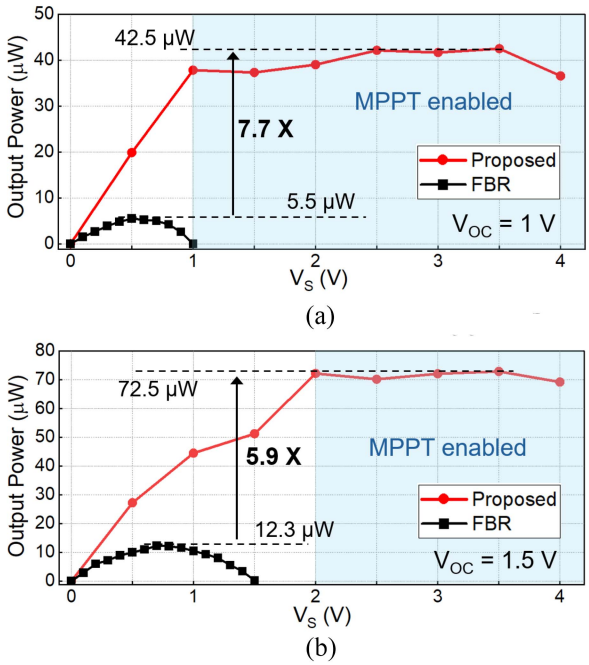

Fig. 20. Output power versus V_S voltage at different V_{OC}. (a) Output power versus V_S when $V_{OC} = 1$ V. (b) Output power versus V_S when $V_{OC} = 1.5$ V.

efficiency of 76%, demonstrating the system's capability to efficiently reverse the PT voltage while minimizing energy loss.

Fig. 20 compares the output power of the proposed rectifier with that of a conventional FBR for varying storage voltages (V_S). When the open-circuit voltage (V_{OC}) is 1 V, the proposed rectifier provides up to 42.5 μW, significantly higher than the FBR's 5.5 μW, showing a 7.7× enhancement. With an increased excitation (V_{OC}=1.5 V), the output reaches 72.5 μW, surpassing the FBR's 12.3 μW by 5.9×. These results underline the rectifier's superior efficiency and effectiveness in maximizing harvested energy.

When the MPPT mode is active, the total measured power consumption is approximately 1.17 μW. A detailed breakdown of power consumption by key circuit blocks is summarized in Table I, highlighting the primary contributors to overall power use.

Performance comparisons with prior published works are provided in Table II. Unlike previous designs, which often employed separate MPPT and rectifier stages leading to additional cascaded energy losses, the proposed rectifier uniquely integrates these functions into a single stage. Consequently, this work achieves superior end-to-end efficiency (93%), excellent MPPT efficiency (98%), and a significant 7.7× power enhancement compared to conventional FBR-based systems.

These results validate the efficacy and practicality of the proposed design for real-world applications, especially in scenarios where battery replacement or external charging is impractical, reinforcing its suitability for self-sustaining IoE, and wearable applications.

VII. CONCLUSION

This article presents a self-regulating bias-flip rectifier integrated with a H-DCB MPPT algorithm, specifically designed for PEH. By combining the rectification and MPPT functionalities into a single stage, the proposed design effectively eliminates cascaded energy losses inherent in conventional two-stage approaches, resulting in significantly improved power efficiency. Unlike traditional MPPT methods, which rely on complex control circuits and open-circuit voltage sampling, the proposed architecture simplifies implementation by inherently regulating the piezoelectric transducer voltage. Moreover, the elimination of the intermediate rectified capacitor ensures rapid convergence to the optimal power point. Experimental results demonstrate a substantial 7.7× enhancement in output power compared to a conventional FBR, validating the effectiveness and practical advantages of the proposed rectifier in real-world energy harvesting applications.

REFERENCES

[1] M. Meng et al., "27.4 multi-beam shared-inductor reconfigurable voltage/SECE-mode piezoelectric energy harvesting of multi-axial human motion," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2019, pp. 426–428.

[2] T. Oh, S. K. Islam, G. To, and M. Mahfouz, "Powering wearable sensors with a low-power CMOS piezoelectric energy harvesting circuit," in *Proc. IEEE Int. Symp. Med. Meas. Appl.*, 2017, pp. 308–313.

[3] Y. Manoli, "Energy harvesting — from devices to systems," in *Proc. Proc. ESSCIRC*, 2010, pp. 27–36.

[4] C.-W. Chen, W. Z. Pranoto, H.-S. Chen, and W.-J. Wu, "A 0.25-μm HV-CMOS synchronous inversion and charge extraction interface circuit with a single inductor for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 38, no. 12, pp. 15707–15718, Dec. 2023.

[5] M. Edla, Y. Y. Lim, D. Mikio, and R. V. Padilla, "A single-stage rectifier-less boost converter circuit for piezoelectric energy harvesting systems," *IEEE Trans. Energy Convers.*, vol. 37, no. 1, pp. 505–514, Mar. 2022.

[6] Y. K. Ramadass and A. P. Chandrakasan, "An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 189–204, Jan. 2010.

[7] S. Lu and F. Boussaid, "A highly efficient P-SSHI rectifier for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5364–5369, Oct. 2015.

[8] Z. Long, P. Li, J. Chen, H. S.-H. Chung, and Z. Yang, "Self-powered single-inductor rectifier-less SSHI array interface with the MPPT technique for piezoelectric energy harvesting," *IEEE Trans. Ind. Electron.*, vol. 69, no. 10, pp. 10172–10181, Oct. 2022.

[9] S. Du, G. A. J. Amaratunga, and A. A. Seshia, "A cold-startup SSHI rectifier for piezoelectric energy harvesters with increased open-circuit voltage," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 263–274, Jan. 2019.

[10] G. A. Rincón-Mora and S. Yang, "Tiny piezoelectric harvesters: Principles, constraints, and power conversion," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 63, no. 5, pp. 639–649, May 2016.

[11] S. Du, Y. Jia, C. D. Do, and A. A. Seshia, "An efficient SSHI interface with increased input range for piezoelectric energy harvesting under variable conditions," *IEEE J. Solid-State Circuits*, vol. 51, no. 11, pp. 2729–2742, Nov. 2016.

[12] L. Wu, X.-D. Do, S.-G. Lee, and D. S. Ha, "A self-powered and optimal SSHI circuit integrated with an active rectifier for piezoelectric energy harvesting," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 64, no. 3, pp. 537–549, Mar. 2017.

[13] S. Du and A. A. Seshia, "An inductorless bias-flip rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2746–2757, Oct. 2017.

[14] S. Du, Y. Jia, C. Zhao, G. A. J. Amaratunga, and A. A. Seshia, "A fully integrated split-electrode SSHC rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1733–1743, Jun. 2019.

[15] X. Yue and S. Du, "Performance optimization of SSHC rectifiers for piezoelectric energy harvesting," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 70, no. 4, pp. 1560–1564, Apr. 2023.

[16] S. Li, A. Roy, and B. H. Calhoun, "A piezoelectric energy-harvesting system with parallel-SSHI rectifier and integrated maximum-power-point tracking," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 12, pp. 301–304, Dec. 2019.

[17] S. Du, Y. Jia, C. Zhao, G. A. J. Amaratunga, and A. A. Seshia, "A nail-size piezoelectric energy harvesting system integrating a mems transducer and a CMOS SSHI circuit," *IEEE Sensors J.*, vol. 20, no. 1, pp. 277–285, Jan. 2020.

[18] T. Hehn et al., "A fully autonomous integrated interface circuit for piezoelectric harvesters," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2185–2198, Sep. 2012.

[19] X. Yue and S. Du, "Voltage flip efficiency optimization of SSHC rectifiers for piezoelectric energy harvesting," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2021, pp. 1–5.

[20] M. Dini, A. Romani, M. Filippi, and M. Tartagni, "A nanopower synchronous charge extractor IC for low-voltage piezoelectric energy harvesting with residual charge inversion," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1263–1274, Feb. 2016.

[21] G. Shi, Y. Xia, X. Wang, L. Qian, Y. Ye, and Q. Li, "An efficient self-powered piezoelectric energy harvesting CMOS interface circuit based on synchronous charge extraction technique," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 65, no. 2, pp. 804–817, Feb. 2018.

[22] X. Yue and S. Du, "A synchronized switch harvesting rectifier with reusable storage capacitors for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 58, no. 9, pp. 2597–2606, Sep. 2023.

[23] X. Yue, J. Mo, Z. Chen, S. Vollebregt, G. Zhang, and S. Du, "A fully integrated sequential synchronized switch harvesting on capacitors rectifier based on split- electrode for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 39, no. 6, pp. 7643–7653, Jun. 2024.

[24] Z. Long et al., "Self-powered SSDCI array interface for multiple piezoelectric energy harvesters," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9093–9104, Aug. 2021.

[25] Z. J. Chew and M. Zhu, "Adaptive self-configurable rectifier for extended operating range of piezoelectric energy harvesting," *IEEE Trans. Ind. Electron.*, vol. 67, no. 4, pp. 3267–3276, Apr. 2020.

[26] H. Xia et al., "Self-powered dual-inductor MI-PSSHI-VDR interface circuit for multi-PZTs energy harvesting," *IEEE Trans. Power Electron.*, vol. 37, no. 4, pp. 3753–3762, Apr. 2022.

[27] Z. Chen et al., "An energy harvesting interface based on reconfigurable piezoelectric harvester array," *IEEE Trans. Power Electron.*, vol. 40, no. 10, pp. 15949–15958, Oct. 2025.

[28] H. Qiu, X. Wei, L. Sui, and L. Shao, "A self-powered SICE circuit for piezoelectric energy harvesting with a complete charge extraction electronic breaker," *IEEE Trans. Power Electron.*, vol. 40, no. 8, pp. 11467–11476, Aug. 2025.

[29] X. Yue and S. Du, "An adaptive two-mode bias-flip rectifier with lowered cold-startup voltage requirement for multiple piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 40, no. 6, pp. 8283–8291, Jun. 2025.

[30] L. Wu and D. S. Ha, "A self-powered piezoelectric energy harvesting circuit with an optimal flipping time SSHI and maximum power point tracking," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 66, no. 10, pp. 1758–1762, Oct. 2019.

[31] C. Lu, C.-Y. Tsui, and W.-H. Ki, "Vibration energy scavenging system with maximum power tracking for micropower applications," *IEEE Trans. Very Large Scale Integration Syst.*, vol. 19, no. 11, pp. 2109–2119, Nov. 2011.

[32] X. Yue, S. Javvaji, Z. Tang, K. A. A. Makinwa, and S. Du, "A bias-flip rectifier with duty-cycle-based MPPT for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 59, no. 6, pp. 1771–1781, Jun. 2024.

[33] C. Xie, G. Zhao, Y. Ma, M.-K. Law, and M. Zhang, "Fully integrated frequency-tuning switched-capacitor rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 58, no. 8, pp. 2337–2348, Aug. 2023.

[34] Z. Chen, M.-K. Law, P.-I. Mak, X. Zeng, and R. P. Martins, "Piezoelectric energy-harvesting interface using split-phase flipping-capacitor rectifier with capacitor reuse for input power adaptation," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2106–2117, Aug. 2020.

[35] X. Yue, S. Javvaji, Z. Tang, K. A. A. Makinwa, and S. Du, "30.3 a bias-flip rectifier with a duty-cycle-based MPPT algorithm for piezoelectric energy harvesting with 98% peak MPPT efficiency and 738% energy-extraction enhancement," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2023, pp. 442–444.

[36] X. Yue and S. Du, "A single-stage bias-flip regulating rectifier with fully digital duty-cycle-based MPPT for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 60, no. 3, pp. 850–860, Mar. 2025.

[37] R. Dayal, S. Dwari, and L. Parsa, "Design and implementation of a direct AC–DC boost converter for low-voltage energy harvesting," *IEEE Trans. Ind. Electron.*, vol. 58, no. 6, pp. 2387–2396, Jun. 2011.

[38] S. Dwari and L. Parsa, "An efficient AC–DC step-up converter for low-voltage energy harvesting," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2188–2199, Aug. 2010.

[39] S.-H. Chen et al., "A direct AC–DC and DC–DC cross-source energy harvesting circuit with analog iterating-based MPPT technique with 72.5% conversion efficiency and 94.6% tracking efficiency," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5885–5899, Aug. 2016.

[40] P. Gasnier et al., "An autonomous piezoelectric energy harvesting IC based on a synchronous multi-shot technique," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1561–1570, Jul. 2014.

[41] M. Shim, J. Kim, J. Jeong, S. Park, and C. Kim, "Self-powered 30 μW to 10 mW piezoelectric energy harvesting system with 9.09ms/V maximum power point tracking time," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2367–2379, Oct. 2015.

[42] D. A. Sanchez, J. Leicht, F. Hagedorn, E. Jodka, E. Fazel, and Y. Manoli, "A parallel-SSHI rectifier for piezoelectric energy harvesting of periodic and shock excitations," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2867–2879, Dec. 2016.

[43] S. Javvaji, V. Singhal, V. Menezes, R. Chauhan, and S. Pavan, "Analysis and design of a multi-step bias-flip rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2590–2600, Sep. 2019.

Xinling Yue received the Ph.D. degree in microelectronics from the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands, in 2024.

Since 2024, she has been a Postdoctoral Researcher with the Integrated Systems Laboratory, ETH Zurich, Zurich, Switzerland. Her current research focuses on analog/digital mixed-signal integrated circuit design for bio-implant applications.

Dr. Yue was the recipient of the Best Student Paper Award at the 2022 IEEE International Conference on Electronics, Circuits, and Systems (ICECS), the Student Travel Grant Awards at the 2022 IEEE International Symposium on Circuits and Systems (ISCAS), the 2023 IEEE International Solid-State Circuits Conference (ISSCC), as well as the 20232024 IEEE Solid-State Circuits Society (SSCS) Predoctoral Achievement Award.

Yiwei Zou received the B.E. degree in integrated circuits and systems from the Huazhong University of Science and Technology, Wuhan, China, in 2022. He is currently working toward the Ph.D. degree in electrical and computer engineering with Rice University, Houston, TX, USA.

His research interests include power management and analog/mixed-signal integrated circuits for bioelectronics.

Sijun Du (Senior Member, IEEE) received the B.Eng. (Hons.) degree in electrical engineering from the University Pierre and Marie Curie (UPMC), Paris, France, in 2011, the M.Sc. degree (distinction) in electrical and electronic engineering from Imperial College, London, U.K., in 2012, and the Ph.D. degree in electrical engineering from the University of Cambridge, Cambridge, U.K., in 2018.

He started his Ph.D. research in 2014. He was at the Laboratoire d'Informatique de Paris 6 (LIP6), University Pierre and Marie Curie, Paris, France, and then was an IC Engineer in Shanghai, China, between 2012 and 2014. He was a Summer Engineer Intern with Qualcomm Technology, Inc., San Diego, CA, USA, in 2016. From 2018 to 2020, he was a Postdoctoral Researcher with the Department of Electrical Engineering and Computer Sciences (EECS), University of California, Berkeley, Berkeley, CA, USA. In 2020, he joined the Department of Microelectronics, Delft University of Technology (TU Delft), Delft, The Netherlands, as an Assistant Professor. His current research focuses on energy-efficient integrated circuits and systems, including power management integrated circuits (PMIC), energy harvesting, wireless power transfer, and dc/dc converters.

Dr. Du was the recipient of the Dutch Research Council (NWO) Talent Program VENI grant in the 2021 round, the Best Student Paper Award in IEEE ICECS 2022, and the SSCS Reviewer Award in 2024. He serves as a Technical Program Committee (TPC) Member of IEEE ISSCC, ISSCC ESSERC, and ISSCC Student Research Preview (SRP). He was the IEEE ICECS Sub-Committee Chair in 2022 and 2024, and has been the IEEE ISCAS Sub-Committee Chair since 2025.