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Sharma, Monika; Rueda Torres, José L.; Palensky, Peter

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# Improved Post-Fault Recovery in MMC-HVDC Networks using Enhanced Active Damping

Monika Sharma, José L. Rueda Torres, Peter Palensky Department of Electrical Sustainable Energy, TU Delft, Delft, Netherlands { M.Sharma-3@, J.L.RuedaTorres@, P.Palensky} @tudelft.nl

Abstract—High-Voltage Direct Current (HVDC) transmission with Modular Multi-level Converter (MMC) - Bipolar Pointto-Point (BPP) configuration is gaining traction as a solution for integrating renewable energy sources into future power grids. However, one critical challenge associated with MMC-BPP systems is the occurrence and mitigation of oscillations on the DC side. These oscillations can arise due to various factors, including interactions between the AC and DC systems, converter de-blocking after fault events, and the dynamic behavior of connected power sources. The research work presented in this paper addresses a gap by investigating and mitigating oscillations specifically occurring during post-fault converter de-blocking. An enhanced active damping method is proposed that achieves a substantial reduction of these oscillations, ensuring improved system stability during this critical phase. Furthermore, a meticulous parametric sensitivity analysis is conducted on a four-terminal MMC-BPP test system using a real-time simulator to extract valuable insights into the damping method's effectiveness under various operating conditions.

Index Terms—Active damping controller, Anti-windup mechanism, Bipolar point-to-point network, Electromagnetic Transient (EMT) simulation, High Voltage Direct Current (HVDC) Network.

#### I. INTRODUCTION

THE burgeoning growth of offshore wind farms necessitates robust and efficient power transmission solutions. High-Voltage Direct Current (HVDC) transmission based on Voltage-Sourced Converter (VSC) technology (VSC-HVDC) is rapidly emerging as a leading contender for this task [1]. Several studies have shown that VSC-HVDC offers distinct advantages over traditional AC transmission for long-distance applications, particularly those involving offshore wind farms [2].

Firstly, unlike AC transmission which suffers from power limitations due to cable capacitance, VSC-HVDC systems are not constrained by distance. This makes them ideal for connecting offshore wind farms located far from shore to mainland networks. Secondly, VSC-HVDC offers superior controllability compared to AC transmission. This enables valuable features like Power Oscillation Damping (POD) to mitigate inter-area oscillations within the AC system . Additionally, VSC-HVDC facilitates the operation of multiterminal HVDC networks (VSC-MTDC), paving the way for interconnected offshore networks across national borders [1] [2].

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As VSC technology evolves from low voltage and capacity to high voltage and capacity, the Modular Multi-level Converter (MMC) is becoming the mainstream method for constructing HVDC networks [3]. MMCs offer several advantages over traditional two-level VSC systems. Firstly, the output voltage at the AC terminal can be close to an ideal sinusoidal waveform, eliminating the need for filters at the Point of Common Coupling (PCC) [4]. Secondly, the expansion of DC voltage and capacity can be easily achieved by increasing the number of sub-modules in each arm, making MMCs a scalable solution for HVDC transmission systems [3]. This development in VSC technology paves the way for larger and more complex HVDC networks, which is the focus of this research.

While HVDC offers numerous benefits for integrating offshore wind farms, its integration into existing power networks presents new challenges regarding oscillation control and system stability [5]. The presence of significant inductance and stray capacitance in long HVDC cables can introduce poorly damped oscillations that interact with the control systems of power electronic converters, potentially leading to overvoltages and even system instability [6]. These oscillations at the DC side are particularly concerning, as current peak overshoots and large settling times can interact with converter control loops and lead to grid failures or blackouts.

Various supplemental controllers have been proposed to address this challenge and enhance damping on the DC side. For example, Virulkar et al. investigated the use of Model Predictive Control to achieve a 13.6% reduction in settling time compared to conventional PI control methods [7]. Li et al. proposed a novel virtual active damping or resonance suppression strategy to regulate DC-link voltages, effectively maintaining them within acceptable limits [8], [9]. Additionally, Wu et al. explored the potential of virtual synchronous generators with virtual inertia and damping control using a proportional-derivative (PD) controller to enhance damping and inertia within the DC network [10]. However, existing damping control methods like impedance-based damping control often require additional hardware or face challenges in parameter tuning [8].

Existing research primarily focuses on point-to-point networks, analyzing the impact of oscillations on the AC side. There is limited research addressing challenges on the DC side. This work addresses this gap by investigating a novel damping control method to improve Post-Fault (PF) recovery

in HVDC networks on the DC side using a bipolar configuration. This method leverages advanced control algorithms and utilizes existing converter control signals to achieve effective damping without additional complexity. The proposed approach employs a DC voltage regulation control mechanism in the outer control loop, complemented by an anti-windup mechanism for MMC- Bipolar Point-to-Point (BPP) networks. By evaluating its performance against existing methods and demonstrating scalability across diverse MTDC configurations, this research aims to enhance the damping of oscillations and stability in MTDC networks.

The paper is organized as follows: Section II presents an overview of state-of-the-art in damping control for HVDC networks. Section III elaborates on the mathematical DC-side equivalent circuit of the converter while focussing on EMT oscillations occuring during de-blocking event of the converter. Section IV delve into the proposed active damping control method. Section V offers a comprehensive analysis of the results obtained. In section VI, the work is concluded.

#### II. STATE-OF-THE-ART

Ensuring stable operation in HVDC networks following DC faults is critical, relying heavily on an effective PF recovery process. These faults, often caused by insulation failures and disrupt the normal operation of the network. During such events, the performance of converters within the network is crucial to the recovery process. Different fault scenarios, which are described by Fault Ride-Through (FRT) conditions, might necessitate temporarily blocking converters, significantly affecting power flow [11].

Re-enabling converters after resolving faults presents several challenges but also causes voltage and current oscillations, along with power fluctuations on the DC side. The frequency of these oscillations can vary depending on system characteristics and control strategies [11]. Current research mainly focuses on the recovery of single converters, pointing to a need for a deeper understanding of recovery in interconnected HVDC networks. In [11],the complex interaction between converters and the network during recovery in interconnected HVDC networks remains a largely unexplored area. Other studies [12], [13] also highlight the necessity for further investigation in this domain.

The PF recovery strategy aims to restore DC voltage to prefault levels quickly and stably. This requires balancing fast voltage (and power flow) recovery with effective management of oscillations, prevention of over-currents, and avoidance of over-voltages. The network's capacitive and inductive components (such as converters, cables, and inductors) create resonant frequencies, and switching or de-blocking converters at voltages different from the grid voltage can trigger oscillations at these frequencies.

Before exploring damping techniques, it is essential to understand the origin of oscillations during PF recovery. These oscillations occur during converter de-blocking and arise from the complex interaction between converters and the HVDC network [11]. The severity of these oscillations

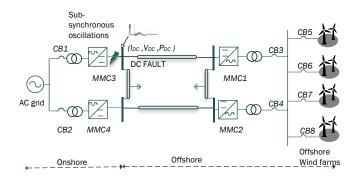


Fig. 1. Point-to-Point Bipolar offshore AC-DC network with four terminals.

depends on the network's damping characteristics unless the converter controller can effectively manage and suppress a broad range of non-DC component frequencies. Inadequate damping, often influenced by DC Circuit Breakers (DCCB), inductors or fault-induced converter de-blocking, can exacerbate these oscillations, potentially leading to overvoltages or overcurrents on the network's DC side. To illustrate a typical HVDC network configuration, Figure 1 depicts a point-to-point bipolar offshore AC-DC network with four terminals.

The configuration depicted in Fig. 1, features onshore MMCs connected to a robust onshore AC power system. MMC3 and MMC4 represent the positive and negative poles, respectively. These onshore MMC models enhance the accuracy of capturing dynamics during offshore-onshore power transfer. Offshore, MMC1 and MMC2 form the terminal connected to a 2GW offshore wind farm.

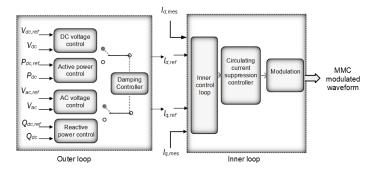


Fig. 2. MMC3 control loop structure.

This study explores Sub-Synchronous Oscillations (SSOs) that occur during converter de-blocking at the DC side of HVDC networks. MMC3 serves as the focus converter. The scenario assumes a temporary blocking event triggered by a short circuit near the onshore DC side cable. SSOs are power system oscillations with frequencies lower than the nominal system frequency. In this study, they are specifically investigated during the converter de-blocking process following a fault event. These oscillations can lead to power fluctuations and voltage deviations, potentially jeopardizing power system operation and equipment integrity [14].

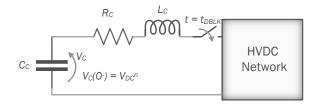


Fig. 3. Simplified circuit diagram for an MMC.

To mitigate SSOs, a supplementary damping controller is added in the outer control loop, as shown in Fig. 2. This controller introduces an additional control loop within the existing MMC-HVDC control scheme. The controller utilizes a modulated signal for implementing damping techniques. This method involves injecting an additional signal into the converter's current control loop to modulate the DC current/voltage and achieve better damping of the SSOs.

The next section III elaborates on the DC-side equivalent circuit's implications during post-fault recovery, emphasizing its role in understanding the converter's behavior and system dynamics, with a specific focus on oscillations.

### III. MATHEMATICAL DC-SIDE EQUIVALENT CIRCUIT OF THE CONVERTER

The examination of the interaction between the converter and HVDC networks during the phase of post-fault recovery can be facilitated through the analysis of the DC-side equivalent circuit. This circuit can be derived by expressing the DC voltage of the converter  $(V_{DC}(s))$  in terms of the DC current  $(I_{DC}(s))$ , the power balance between the AC and DC sides  $(\eta)$ , and the zero-sequence component of the internal voltage of the converter  $(V_c^{*0}(s))$ , as defined in equation (1). Notably, the variables  $V_s$ ,  $I_s$ , and  $\Psi$  denote the peak value of the output AC voltage, the peak value of the output AC current, and the phase shift between the output AC voltage and current, respectively. A thorough elucidation of these variables is given by (1).

$$V_{DC}(s) = \frac{1}{6} \left( \frac{3V_{DC}^{\sum}(0)}{s} - \frac{1}{s} L \frac{3NV_s I_s \cos(\phi)}{2V_{DC} C_{sub}} + \frac{NI_{DC}(s)}{sC_{sub}} \right) + \frac{2}{3} L_{arm} \left( sI_{DC}(s) - i_{DC}(0) + \frac{2}{3} R_{arm} I_{DC}(s) - \frac{1}{3} \xi V_c^{*0}(s) \right)$$

$$(1)$$

In Equation (1), the crucial role played by  $V_c^{*0}$ , which represents the zero-sequence component of the internal voltage, in determining the DC voltage of the MMC. This DC voltage is under the regulation of the Circulating Current Suppression Controller (CCSC). Various types of CCSCs are discussed in the literature [11], [15]–[17]. The CCSC method based on the D-Q coordinate is a typical method widely used in the

literature. In this particular method, the DC component of the circulating current is naturally determined by the power exchange between the converter and the HVDC network. Consequently, the zero-sequence reference of the internal voltage  $V_c^{*0}(s)$  is set in Equation (1) to zero.

At the point of de-blocking, following the clearance of a fault and the system's transition back to normal operation, we consider  $i_{DC}(0)$  to be zero. Additionally, assuming no power exchange between the AC and DC sides at the moment of deblocking, we can simplify Equation (1) by neglecting the term  $\eta$ . This simplification leads to Equation (2), where  $V_{DC}^{\Sigma}(0)$  in Equation (1) is assumed to be twice the nominal DC voltage, denoted as  $2V_{DC}^n$ .

To further illustrate the converter model during de-blocking, Figure 3 depicts a simplified circuit diagram of an MMC. The key components influencing the DC-side dynamics are the arm inductance  $(L_{arm})$ , arm resistance  $(R_{arm})$ , and the submodule capacitor  $(C_{sub})$ . These elements are combined to form the thevenin equivalent circuit seen from the DC terminals, represented by the impedance  $Z_{col}^{DC}$ .

$$V_{DC}(s) = Z_{c_i}^{DC} I_{DC}(s) + \frac{V_{DC}^n}{s}$$
where
$$Z_{c_i}^{DC} = s L_{c_i} + R_{c_i} + \frac{1}{s C_{c_i}},$$

$$L_{c_i} = \frac{1}{3} L_{arm}, R_{c_i} = \frac{2}{3} R_{arm}, \quad C_{c_i} = \frac{6C_{sub}}{N}$$
(2)

Equation (2) represents the RLC equivalent circuit of the converter's DC side during de-blocking, depicting a precharged capacitor voltage  $V^n_{DC}$ . This configuration resembles an RLC circuit where  $Z^{DC}_{c_i}$  characterizes the impedance seen by the DC current  $I_{DC}(s)$ .

Following de-blocking, the converter's recovery involves the activation of this RLC equivalent circuit. It's crucial to note that while this approximation holds immediately post-de-blocking, discrepancies between the actual converter's behavior and the RLC model escalate over time due to the influence of the power balance term  $\eta$  in Equation (1). The significance of  $\eta$  depends on the bandwidth of the outer control loops.

The activation of the RLC equivalent circuit during recovery induces electromagnetic oscillations if the HVDC network voltage deviates from  $V^n_{DC}$  at the switching instant. This phenomenon underscores the dynamic interplay between the converter's operational states and the system's response characteristics during post-fault scenarios. Section IV discusses the enhanced method for damping oscillations and improving post-fault recovery in HVDC networks.

#### IV. ENHANCEMENT OF THE DAMPING SUPPORT CAPABILITY

This section explores a novel control loop for DC-voltage regulation during the converter de-blocking process, as illustrated in Figure 4, aimed at damping the oscillations that occur during converter de-blocking. Following a fault event,

the DC-side voltage might consistently fall below a pre-defined minimum threshold  $(V_{DC}^{min})$ . This discrepancy between the grid-side and converter DC-side voltage can arise due to limitations in existing controls and voltage evaluation criteria.

To address this issue during de-blocking, the proposed method aims to precisely match the converter's DC-side voltage output with the grid-side voltage. This alignment is achieved by dynamically adjusting the number of active sub-modules within the converter. By strategically reducing the number of active sub-modules during de-blocking, the converter's DC-side voltage effectively decreases, minimizing the voltage difference with the grid. The control loop operates by subtracting the control loop output from the internal voltage reference. This subtraction effectively reduces the number of active sub-modules. The controller activation is specifically triggered only during de-blocking events through a dedicated signal  $S_{DBLK}$ .

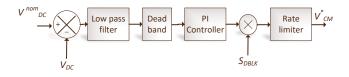


Fig. 4. Control Loop for Standard DC-Voltage Regulation in MMC-HVDC Network.

A rate limiter is implemented to manage the speed at which sub-modules are adjusted. This limiter ensures a smooth transition by accelerating sub-module reduction until the nominal DC-side voltage is reached. It prevents sudden voltage fluctuations while regulating the rate of sub-module insertion back into operation. The difference between the nominal DC voltage and the grid voltage, referred to as the voltage error, is integrated into the controller (G(s)) to optimize the system response during de-blocking. The integrator helps fine-tune the system's response during de-blocking by accounting for any persistent voltage differences.

A proportional controller is usually adequate for regulating the DC-side voltage, often supplemented with a low-pass filter to remove unwanted high-frequency components. During normal operations, the controller output stays at zero because the DC-side voltage is near the nominal value, thanks to the dead-band block. However, if the DC-side voltage drops below  $V_{DC}^{min}$  at the moment of de-blocking, causing the error to exceed the dead-band threshold, the controller output activates to reduce the number of inserted submodules, thereby aligning the system with the grid voltage [11].

While integrating the voltage error in the DC-voltage regulation controller offers benefits during de-blocking, it can introduce potential issues under certain circumstances. Continuous integration of the error signal, even when the controller output is saturated at its maximum or minimum value, can lead to a phenomenon known as integrator windup. This windup can manifest as unwanted oscillations, extended settling times, or sluggish response during de-blocking [18].

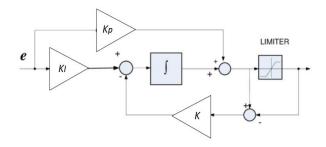


Fig. 5. Anti-windup Mechanism for Enhanced Damping Controller Performance.

To mitigate the effects of integrator windup, an anti-windup mechanism is implemented as depicted in Figure 5. This study employs the back-calculation method. This technique addresses windup by subtracting the "surplus" of the integrator output from the integrator input. The surplus refers to the difference between the integrator output signal and the actual control output after the saturation limiter.

Additionally, a proportional coefficient (K) can be introduced in the anti-windup loop to further refine the controller's behavior, allowing for adjustments based on system requirements. This method ensures precise DC-voltage regulation during de-blocking while maintaining the stability of HVDC networks.

#### V. RESULTS AND ANALYSIS

Fast and stable PF recovery is crucial for ensuring the reliable operation of HVDC networks. However, transient current surges and slow settling times can occur during the de-blocking of converters after faults, potentially leading to equipment stress and control instability. This study investigates an enhanced DC-voltage regulation method with an anti-windup mechanism to improve PF recovery in a four-terminal BPP HVDC network integrated with a 2 GW offshore wind farm.

The system model depicted in Figure 1 is simulated using the Real Time Digital Simulator (RTDS), which operates under the control loops detailed in Section II. RTDS is integrated with RSCAD software, specifically designed for performing EMT simulations on RTDS hardware. RSCAD offers a user-friendly interface on a computer, while the simulations are executed on specialized RTDS units, such as PB5 cards or NovaCor units [19]. In this research, three NovaCor units, each with four cores, are utilized.

The study parameters are derived from the model described in [20]. The HVDC network operates at a voltage level of 640 kV DC, requiring 320 submodules per arm to achieve  $\pm 320$  kV for the positive and negative poles. The offshore wind farm has a total capacity of 2 GW, consisting of four collective OWFs, each with a 500 MW installed capacity, represented by the Wind Generation System, and MMCs rated at 1 GW each. The cables are modeled using Bergeron models with RLC data parameters.

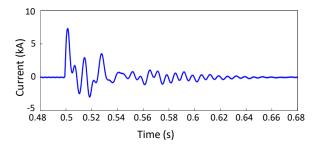


Fig. 6. Current at PCC after de-blocking of MMC3 converter.

In the event of a severe DC fault (short circuit) near MMC3 converter, the switch on the DC side is opened immediately to isolate the fault, effectively blocking MMC3. Once the fault is cleared, MMC3 is deblocked. Figure 6 illustrates the current at PCC near MMC3 converter without using a damping controller. A peak overshoot of 7.2 kA and a settling time of 0.159978 s are observed during the de-blocking of converter MMC3. This highlights the need for improved postfault recovery strategies.

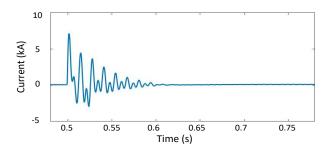


Fig. 7. Current near MMC3 converter using standard DC-voltage regulation method during de-blocking.

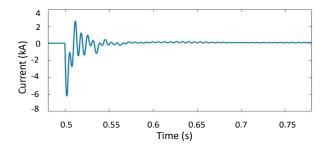


Fig. 8. Current near MMC3 converter using enhanced controller during deblocking.

To improve post-fault recovery, a DC voltage regulation method is adopted as a damping controller. The DC-voltage regulation method with damping reduced the peak overshoot by 4.03% and settling time by 23.22% compared to the

case without damping, as shown in Figure 7. This initial improvement demonstrates the effectiveness of the damping controller in mitigating post-fault transients.

The enhanced controller employs an anti-windup mechanism, as discussed in Section IV, using the back-calculation method. The proportional coefficient in the anti-windup loop significantly affects the controller's response to saturation. A higher proportional coefficient generally accelerates recovery from windup but may introduce oscillations. The optimal coefficient balances windup recovery and system stability. This analysis shows that a moderate (K) value effectively manages windup and maintains stability.

The impact of this enhanced controller during the deblocking event is evident in the peak overshoot and settling time. During the de-blocking of the converter, the enhanced controller achieved a significant reduction in overshoot by 62.37% and settling time by 44.54% compared to using only the damping controller, as depicted in Figure 8. This substantial improvement emphasizes the effectiveness of the antiwindup mechanism in further enhancing post-fault recovery.

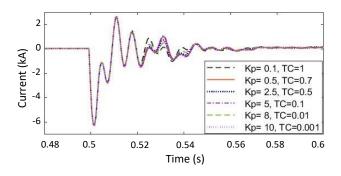


Fig. 9. Impact of  $K_P$  and TC in fine tuned enhanced controller.

A parametric sensitivity analysis is conducted on the crucial parameters of the enhanced controller, specifically the PI controller with an anti-windup mechanism, where stability depends on the relationship between the Proportional Gain  $(K_P)$  and the Integral Time Constant (TC). Various values of  $K_P$  and TC were examined to achieve the desired response for the DC voltage to closely track the DC reference. Table I and Figure 9 present different combinations of  $K_P$  and TC, with optimal values determined as 0.5 and 0.7, resulting in a notable reduction in overshoot and settling time at the PCC point when the MMC3 converter is deblocked.

An increase in  $K_P$  from 0.1 to 0.3 correlates with a noticeable increase in the peak overshoot value. Significantly, the settling time diminishes when TC is reduced from 1 to 0.7. This occurs because the smaller TC value enables the integral action to quickly accumulate and correct errors. Consequently, the controller with  $K_P = 0.5$  and TC = 0.7 strikes a balance, yielding relatively low overshoot (2.46 kA) and a rapid settling time (0.06643 s). Further increases in  $K_P$  and TC would lead to higher peak overshoot and settling time as shown in Table

TABLE I
FINE TUNING OF PARAMETERS FOR ANTI-WIND UP MECHANISM BASED
PI CONTROLLER

Proportional Gain	Integral Time	Peak Overshoot	Settling Time
$(K_P)$	Constant (TC)	Value	
0.1	1	2.47	0.06672
0.2	0.9	2.49	0.06681
0.3	0.8	2.5	0.06651
0.5	0.7	2.46	0.06643
2.5	0.5	2.52	0.06651
5	0.1	2.57	0.06969
8	0.01	2.56	0.0665
10	0.001	2.66	0.05131

I.

With finely tuned parameters, the damping controller achieves a further reduction in overshoot and settling time compared to the BPP-HVDC network without fine-tuning. As shown in Figure 9, fine-tuning the controller parameters resulted in an additional reduction of 5.39% and 2.48% in overshoot and settling time, respectively. The enhanced controller is compared by existing approach in literature and achieves 64.47% reduction in overshoot and 45.92% improvement in settling time compared to DC-side voltage regulation approach [11]. The comparison shows the effectiveness of enhanced controller when compared with key performance indices such as overshoot time and settling time.

#### VI. CONCLUSION

This research work presents an in-depth analysis of a 2 GW offshore network within the RSCAD-enabled BPP-HVDC network, focusing on an enhanced DC-voltage regulation method incorporating an anti-windup mechanism. This method is designed to improve post-fault recovery following the deblocking of the converter after severe faults. By implementing a meticulous parametric sensitivity analysis for the enhanced controller, the study demonstrates a significant reduction in peak overshoot and settling time by 64.47% and 45.92%, respectively, compared to the standard DC voltage regulation method without enhancement. These improvements contribute to the development of more effective post-fault recovery mechanisms, thereby strengthening the resilience and robustness of complex bipolar HVDC networks. This work underscores the critical importance of advanced control strategies in enhancing the performance and stability of HVDC systems in real-world applications.

#### ACKNOWLEDGMENT

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