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Characterization of PCB Embedded Package Materials for SiC MOSFETs

Fengze Hou, Wenbo Wang, Tingyu Lin, Liqiang Cao, G. Q. Zhang, *Fellow, IEEE*, J. A. Ferreira, *Fellow, IEEE*

***Abstract*—In this paper, a novel fan-out panel-level PCB embedded package technology for SiC MOSFET power module is presented to address parasitic inductances, heat dissipation, and reliability issues that are inherent with aluminum wires used in conventional packaging scheme. To withstand high temperature beyond 175 °C and high voltage over 1.2 kV and improve thermo-mechanical reliability of the fan-out panel-level PCB embedded SiC power module, BT laminate and prepreg with high temperature stability, high dielectric strength, CTE matching with SiC, and high Tg are selected as PCB embedded package materials. Then, high temperature stabilities, dielectric breakdown strength, and thermo-mechanical performances of the embedded materials are characterized. The experimental results show that the PCB embedded materials can withstand high temperature beyond 200 °C and high voltage above 1.2 kV. Tg is as high as over 260 °C and CTE is matching with SiC. Besides, in order to provide one guideline for the high-temperature and high-pressure laminating process during the PCB embedded SiC MOSFETs packaging, cure kinetics of BT prepreg are analyzed. The results show that one-hour curing time at 280 °C curing temperature and two-hour curing time at 210 °C curing temperature can ensure the full cure of the BT prepreg.**

***Index Terms*—PCB embedded package, SiC MOSFETs, high temperature, high voltage, material characterization**

I. INTRODUCTION

In low voltage (≤ 1.2 kV) applications, power modules are required to operate at high efficiency, high ambient temperature, small form factor, and high power density [1]. Silicon carbide (SiC) is a promising wide band gap (WBG) semiconductor material for high temperature, high voltage, and high frequency applications due to its electrical and physical properties [2]-[6].

Figure 1 illustrates a power module with conventional packaging scheme, which is the most preferred package structure for SiC power module. The package provides electrical interconnects (via aluminum wire-bonds and the upper copper tracks of direct bonded copper, i.e. DBC ceramic substrate), electrical insulation (by DBC ceramic substrate), device protection (power devices are protected by encapsulation material), and thermal management (heat generated by power device is dissipated through DBC substrate, baseplate, and heat sink) [7].

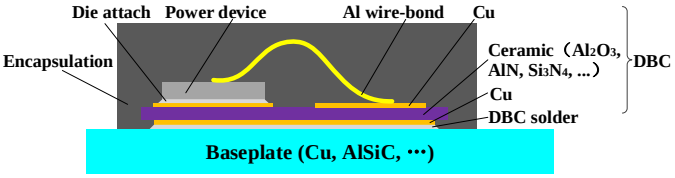

Figure 1. Conventional packaging scheme for a power module

Limited by available packaging materials and existing packaging techniques, junction temperatures of SiC power modules are subjected to ~175 °C, even though SiC devices are, in theory, capable of operating at much higher junction temperatures [8].

Most packaging materials adopted in the SiC power modules, e.g. die attach, encapsulant, etc., cannot survive temperatures over 175 °C for long time, prohibiting application of the SiC power modules in high temperature environment. High-temperature die-attach alternatives such as organic die attach, high-temperature lead-free solders, and sintering of micro- and nano-silver powders, etc., seem to be potential candidates [3]. These high-temperature die attach alternatives, however, need higher processing temperature, which could easily cause larger residue stress and strain in the power module. For encapsulant, it has not only thermal stability but also dielectric breakdown strength issues in the SiC power modules. With the conventional packaging scheme for SiC power modules, under high ambient temperature and operational temperature, thermally induced stress/strain resulting from the coefficient of thermal expansion (CTE) mismatch among the constituent materials could lead to wire failure, die attach/die crack, package warpage, etc. [11]. Moreover, most of the heat generated by SiC devices in the conventional packaging scheme is only dissipated through bottom side. A cooling system that can remove the heat through dual sides will be much more efficient. Besides, wire-bonds have stray inductances that can exceed 10 nH, increasing switching loss of power devices, limiting switching frequency, and affecting

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switching waveforms [7]. In order to solve these problems, new packaging interconnection technologies and materials need to be investigated to push the development of SiC power module.

So far, there have been development in wire-bondless interconnections for power module, such as flip chip and copper clip connection [12], multilayer planar interconnection [13], power overlay interconnect [14], copper pin connection [9], press-pack [15], power chip-on-chip [16], transfer molded power module [17], and PCB embedded package [1] [18]-[21].

Compared with other wire-bondless interconnections, PCB embedded power module package is a solution with small form factor, light weight, and simple process technology. In recent years, several PCB embedded package technologies have been developed for IGBT module, power diode, and GaN HEMT. Leadframe based PCB embedded package technology is one of the major representatives [1] [19]-[21]. The bottom side of a power device is soldered or sintered onto a copper leadframe, the resulting assembly is then fully embedded in prepreg. Electrical interconnections of a power device is realized through laser drilling, electroless plating, copper plating, and some other processes. However, the structure of the leadframe based PCB embedded package is asymmetry in thickness direction, which could easily cause large stress and strain in the package due to CTE mismatch between chip and copper leadframe in harsh environment. Balanced package structure can relieve the stress and strain. Besides, heat generated from a power device is mainly dissipated into the ambient through copper leadframe, which limits the thermal performance of a power module. For PCB embedded package materials, e.g. FR4 prepreg (glass fiber reinforced uncured epoxy resin), RCC (resin coated copper), ABF are often used [18]-[24]. Munding et al. [19] selected FR4 prepreg and RCC as PCB embedded material, respectively, evaluated thermo-mechanical reliability of the two leadframe based laminate chip embedded packages through temperature cycle and high temperature storage experiments. And it was found that high glass transition temperature (Tg) FR4 prepreg was more suitable for PCB embedded package.

Compared with Si counterparts, SiC devices have smaller size, higher power-density, and faster switching speed. In a power module, the superior properties of a SiC device cannot be exploited if it is used simply as a direct replacement of Si device [25]. SiC device has different requirements on packaging technologies and packaging materials. In fact, work on PCB embedded package technologies and package materials for SiC devices has already been conducted.

In section II of this paper, a novel PCB embedded package structure for SiC MOSFET module is presented. To withstand high temperature beyond 175 °C and high voltage over 1.2 kV, and also to improve thermo-mechanical reliability of the PCB embedded SiC module, Bismaleimide-Triazine (BT) laminate and prepreg with high temperature stability, high dielectric strength, CTE matching with SiC, and high Tg are selected as PCB embedded package materials. In section III, high temperature stabilities, dielectric breakdown strength, and thermo-mechanical performances of the selective materials and cure kinetics of BT prepreg are characterized for PCB embedded SiC MOSFETs packaging.

II. Fan-out panel-level PCB embedded package technology for SiC MOSFETs

Figure 2 shows a circuit diagram of a phase-leg SiC MOSFET module, which consists of two SiC transistors. Phase-leg is a building block for various electronic power converters and inverters in power electronics systems.

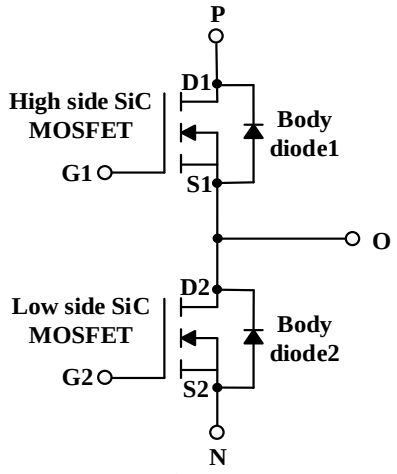

Figure 2. Circuit diagram of phase-leg SiC MOSFET module

In this work, a novel fan-out panel-level PCB embedded package technology for the SiC MOSFET phase-leg module is proposed. The key packaging process is demonstrated in Figure 3. PCB embedded materials adopted in the SiC MOSFETs packaging process will be investigated.

In order to withstand temperature beyond 175 °C, voltage over 1.2 kV, and improve thermo-mechanical reliability of the PCB embedded SiC package, SiC MOSFETs are placed in the grooves of BT laminate, which has high temperature stability, high dielectric strength, CTE matching, and high Tg, as shown in Figure 3 (a). It should be noted that SiC MOSFETs have the same thickness as BT laminate.

The resulting assembly is then embedded in BT prepregs through high-temperature and high-pressure laminating process to form a laminated PCB. Gaps btween SiC MOSFETs and BT laminate are filled with BT prepreg, as illustrated in Figure 3 (b). Because of the fact that source and drain are not on the same side, the laminated PCB must withstand maximum drain-source breakdown voltage over 1.2 kV. During the laminating process, degree of cure of BT prepreg could affect the mechanical properties of the final packages [26]. Although suppliers of commercial BT prepreg resins usually provide curing condition for the customers, the curing condition may not be the optimal ones for PCB embedded SiC MOSFETs packaging. Besides, high temperature stability and thermo-mechanical performances of the cured prepreg should be compared with BT laminate.

Electrical interconnection of the PCB embedded SiC MOSFETs is realized by redistribution layer (RDL), blind vias, and through vias. As shown in Figure 3(c), the final package mainly consists of switching devices (SiC MOSFETs), PCB embedded materials (BT laminate and BT prepreg), electrical interconnection (RDL, blind vias, and through vias), soldermask, and LGA (land grid array).

Compared with conventional SiC power module packages, the PCB embedded technology eliminates aluminum

wire-bonds, DBC substrate, die attach, and encapsulation structure, manufacturing processes are, accordingly, simplified. The innovative PCB embedded package technology has advantages such as higher power density, lower parasitic inductance, dual side cooling, etc.

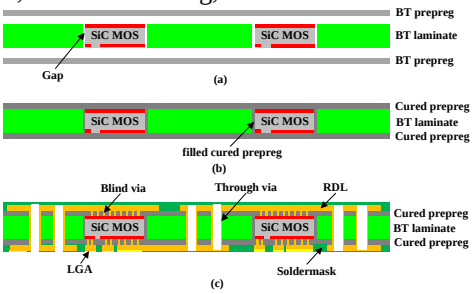

Figure 3. Fan-out panel-level PCB embedded SiC MOSFETs package (a) before laminating; (b) after laminating; (c) final package structure

III. PCB EMBEDDED PACKAGE MATERIALS

A. Selective creteria

- High temperature stability

SiC MOSFETs can operate at elevated temperatures in comparison with Si counterparts. In applications such as hybrid/electric vehicle, renewable energy/energy storage, etc., power modules need to suffer temperatures over 175 °C. And therefore, temperature of thermal stability of PCB embedded materials should be over 175 °C.

- High dielectric breakdown strength

SiC MOSFETs are embedded in the groove of BT laminate with the same thickness, so the laminated PCB must be able to withstand maximum drain-source voltage of over 1.2 kV to keep the laminated PCB from broken down. The dielectric breakdown strength E is defined as:

$$E = \frac{V_{\mathrm{BD}}}{d} \tag{1}$$

where V_{BD} is the dielectric breakdown voltage, d is the thickness of material.

Figure 4 shows electric field distribution simulation result of the laminated PCB when drain-source voltage of high-side SiC MOSFET is 1.2 kV. The maximum electric field strength is 8.56×10^5 V/m. And accordingly, the dielectric breakdown strength of the laminated PCB must be much higher than 8.56×10^5 V/m.

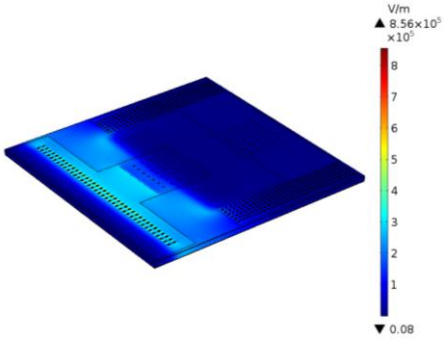

Figure 4. Electric field distribution of laminated PCB

- High glass transition temperature

As viscoelastic materials, thermo-mechanical properties of PCB embedded materials will change significantly below and above Tg, storage modulus decreases dramatically and CTE increases evidently. Therefore, choosing PCB embedded materials with high Tg can improve thermo-mechanical reliability of the PCB embedded SiC MOSFETs.

- CTE matching with SiC

PCB embedded SiC MOSFETs failures can happen when thermal stress is excessive. Thermally induced stress at different interfaces can be described by Eq. (2).

$$\sigma_T = \int_{T_1}^{T_2} \frac{\alpha_A(T)-\alpha_B(T)}{\left[\frac{1}{E_A(T)}+\frac{1}{E_B(T)}\right](1-\mu_A)}\,dT \tag{2}$$

where α_{A}, α_{B} are the CTE of material A and material B, respectively. E_{A} and E_{B} are the Young's modulus of material A and material B, respectively. μ_{A} is Poisson's ratio of material A. Therefore, when conducting package structure design, we should try to match the CTE of a PCB material to the SiC.

B. Material selection

The PCB embedded package materials adopted in the SiC power module pckage process are copper clad laminate (CCL-HL832NSF) and preperg (GHPL-830NSF) from Mitsubishi Gas Chemical. CCL-HL832NSF is a double-sided copper-clad BT laminate (E-glass fiber-reinforced BT resin), as shown in Figure 5 (a). Figure 5 (b) is a sheet of BT prepreg (E-glass fiber-reinforced uncured BT resin). In order to analyze and compare the properties of the laminate and the prepreg comprehensively, double-sided copper of copper-clad laminate is etched, as shown in Figure 5 (c). Cured prepreg, with the same thickness as BT laminate, is made of two layers of BT prepregs through high-temperature and high-pressure laminating process, as illustrated in Figure 5 (d). BT laminate is commonly used as a substrate core material in microelectronic packaging [27]. In this work, SiC MOSFETs are placed in the grooves of BT laminate and embedded using BT prepreg through high temperature and high pressure process.

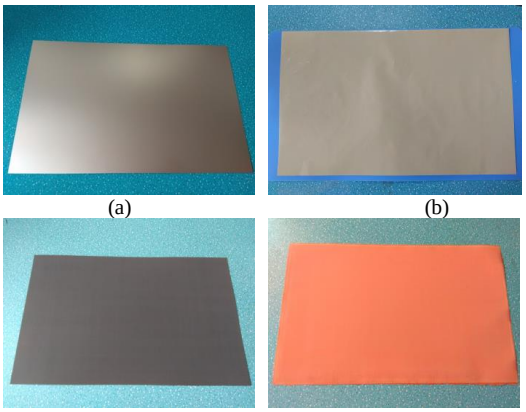

Figure 5. PCB embedded materials: (a) low CTE and high Tg copper clad BT laminate; (b) BT prepreg; (c) BT laminate; (d) cured prepreg

IV. EXPERIMENTAL APPROACH

Firstly, dynamic and isothermal thermal gravimetric experiments are performed using the TGA (thermal gravimetric analyzer) under purging nitrogen atmosphere to investigate the high temperature stability of the PCB embedded materials.

Secondly, thermo-mechanical performance of the PCB embedded materials are analyzed and compared using the film/fiber tensile clamp in TMA (thermal mechanical analyzer)

under purging nitrogen atmosphere. Tg of the PCB embedded materials and CTE match/mismatch between PCB embedded materials and SiC are also analyzed.

Thirdly, breakdown voltage of the PCB embedded materials are characterized through a withstanding voltage tester. Weibull statistical distribution is adopted to analyze the dielectric breakdown strength of the embedded materials. The breakdown voltage of the laminated PCB is evaluated to ensure that it can withstand maximum drain-source voltage of SiC MOSFET.

Lastly, dynamic and isothermal cure kinetics experiments of BT prepreg are conducted using DSC (differential scanning calorimetry) under purging nitrogen atmosphere. Effects of ramp rate, curing temperature, and curing time on degree of cure of the BT prepreg are analyzed to provide guidelines for high-temperature and high-pressure laminating process during the PCB embedded SiC MOSFETs packaging.

IV. EXPERIMENTAL RESULTS

A. *High temperature stability of the PCB embedded materials*

TGA is used to measure weight gain or loss of the material as a function of time, temperature, and environmental factors. Most of the changes in the properties can be traced back to the loss of weight [28]. In this section, first of all, high temperature stabilities of BT laminate and cured prepreg are compared at a ramp rate of 10 °C/min. Then, both dynamic and isothermal TGA are performed to further investigate the high temperature stability of the BT laminate. Dynamic TGA is used to determine the degradation temperature, while isothermal TGA is used to determine the decomposition temperature [28].

- High temperature stability comparison between BT laminate and cured prepreg

Figure 6 compares high temperature stability between BT laminate and cured prepreg. It can be seen that the two materials show similar weight loss rate from room temperature to 400 °C. The two materials are very stable below 300 °C. The weight loss rates of the two materials begin to increase as temperature continues to rise. When temperature scales from 400 °C to 600 °C, weight loss rates of two materials starts to deviate from each other. Therefore, the PCB materials are considered as stable when temperature is below 300 °C.

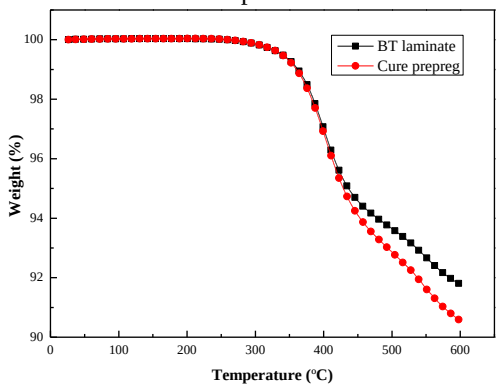

Figure 6. Comparison of high temperature stability between BT laminate and cured prepreg

- Dynamic thermal gravimetric analysis of BT laminate

Dynamic TGA is performed by heating the BT laminate until 800 °C through different ramp rates of 5 °C/min, 15 °C/min, and 30 °C/min, as depicted in Figure 7. The extrapolated onset temperature that denotes the degradation temperature at which the weight loss begins can be calculated. Onset temperature is a reproducible temperature calculation and it is specified to be used by ASTM and ISO [29]. It is clear that the onset temperature of the laminate rises as ramp rate increases. When ramp rate increases to 30 °C/min, onset temperature of the laminate reaches up to 381 °C. Therefore, increasing ramp rate can decrease the degradation of the material.

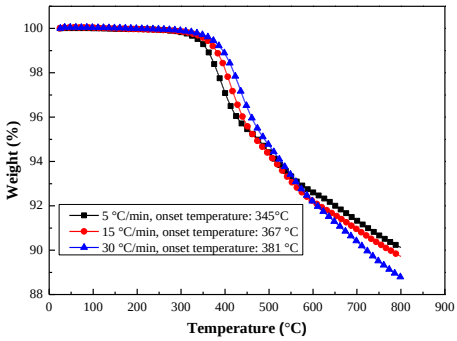

Figure 7. Dynamic thermal gravimetric analysis of the laminate material

- Isothermal thermal gravimetric analysis of BT laminate

The BT laminate is firstly heated up to an isothermal temperature from room temperature at a high ramp rate of 100 °C/min to avoid any dissipation of heat during heating, and then executed at 300 °C, 350 °C, 400 °C, 450 °C, and 500 °C for one hour, respectively.

Figure 8 shows weight losses of the laminate under different isothermal TGA experiments. It can be found that weight loss mainly occurs in the temperature rising process and the initial phase of isothermal process. As holding time goes on, little weight lost occurs. So, only one hour isothermal holding time is adopted. When the laminate material is subjected to the temperature of 300 °C for one hour, a slight weight loss is observed, which can be attributed to outgassing of solvents. However, when temperature ramps up to 350 °C and isothermally heated for one hour, decomposition of the laminate material begins to be evident and about 2% of weight is lost. Therefore, the laminate is thermally stable under the high temperature of 300 °C. The PCB embedded materials are suitable for SiC power module in high temperature applications over 175 °C.

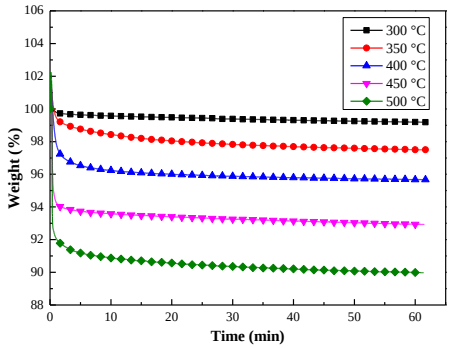

Figure 8. Isothermal thermal gravimetric analysis of the laminate material

B. *Dielectric breakdown strength of the PCB embedded materials*

Breakdown voltage of BT laminate is also characterized. The thickness of the selective BT laminate is 60 µm. The thin laminate can be broken down by a withstanding voltage tester, the highest voltage of which is 20 kV. A series of voltage breakdown experiments are performed. Weibull statistical distribution is adopted to analyze the breakdown behavior of PCB embedded materials. The cumulative distribution function for two-parameter Weibull distribution is expressed as:

$$P(E) = 1 - \exp\left[-\left(\frac{E}{E_0}\right)^{\beta}\right] \quad (3)$$

where $P(E)$ is the cumulative probability, E_0 is the scale parameter representing the value of E corresponding to a cumulative probability of 63.2% and β is the shape parameter which is the slope of straight line of Weibull plot [30].
This equation can be rewritten as follows:

$$log\left(ln\frac{1}{1-P}\right) = \beta logE - \beta logE_0. \quad (4)$$

Assume that:

$$\mathrm{x} = \log E \quad (5)$$

$$\mathrm{y} = \log\left(ln\frac{1}{1-P}\right) \quad (6)$$

Then, y is a linear function of x, can be expressed as:

$$y = \beta x - \beta logE_0. \quad (7)$$

Figure 9 shows Weibull plot of dielectric strength data of BT laminate. From the figure, it can be seen that the fit linear function is

$$y = 5.37x - 12.9. \quad (8)$$

From Eq. (7), it can be calculated that the dielectric strength of the BT laminate is about 252 kV/mm. For PCB embedded SiC MOSFETs, the laminated PCB is about 300 µm, and the breakdown voltage is as high as about 75.6 kV, which is much higher than SiC MOSFET drain-source voltage of 1.2 kV. And therefore, the PCB embedded materials can withstand high voltage over 1.2 kV.

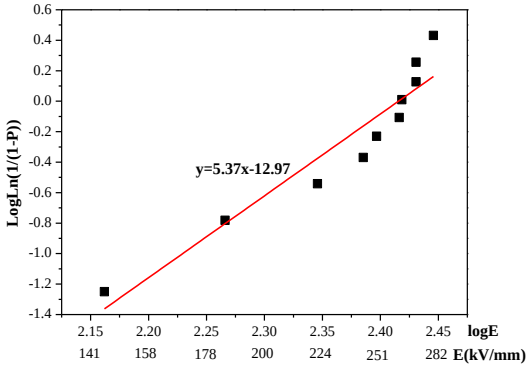

Figure 9. Weibull plot of dielectric strength data of BT laminate

C. *Thermo-mechanical performance of the PCB embedded materials*

CTE mismatch between PCB embedded materials and SiC could lead to package failure, e.g. die crack, interface delamination, etc. In order to ensure the thermo-mechanical reliability of the PCB embedded SiC MOSFETs package, Tg of the PCB embedded materials and CTE match/mismatch between the PCB embedded materials and SiC are analyzed. The BT laminate and cured prepreg are heated separately from 25 °C to 330 °C at a ramp rate of 5 °C/min. Then, effect of ramp rate on in-plane CTE of the cured prepreg is further investigated. The ramp rate increases from 5 °C/min to 25 °C/min.

- Thermo-mechanical comparison between BT laminate and cured prepreg

Figure 10 compares Tg and in-plane CTE between cured prepreg and BT laminate. As can be concluded from the result, the two materials show similar thermo-mechanical performance. Tg of the two materials are about 262~265 °C, which is much higher than Tg of the other PCB materials. Common PCB embedded materials, such as FR4 prepreg, Tg is usually around 150 °C. In-plane CTEs of the two materials above Tg are lower than those below Tg. When temperature is below Tg, in-plane CTEs of the two materials are about 5~7 ppm/°C. When temperature is above Tg, in-plane CTEs of the two materials are about 3 ppm/°C. Because the cured prepreg is made of two layers of BT prepregs through high-temperature and high-pressure laminating process and contains two layers of glass fibers, while BT laminate has only one layer of glass fiber, CTE of the cured prepreg is slightly bigger than that of the laminate. And thus, the PCB embedded materials have Tg as high as over 260 °C, CTE as low as 5.3 ppm/°C.

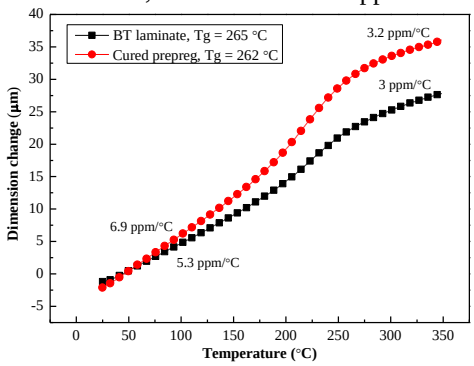

Figure 10. Comparison of Tg and in-plane CTE between cured prepreg and BT laminate

Table I lists thermo-mechanical properties of PCB embedded materials, DBC ceramics, and SiC MOSFET. DBC ceramic substrate is widely used in the power module package, a variety of ceramics can be selected as electrical insulation layer of DBC substrate, such as alumina (Al_2O_3), aluminum-nitride (AlN), silicon-nitride (Si_3N_4), and beryllia (BeO). CTEs of these ceramics are shown in Table I, from which it can be seen that AlN is closest CTE matching with 4H-SiC[31]. The in-plane CTE of BT laminate below Tg is very close to AlN, and therefore matching with 4H-SiC. In-plane CTE of cured prepreg is slight higher than 4H-SiC.

Table I. Thermo-mechanical properties of PCB embedded materials, DBC ceramics, and SiC material

Component	Materials	CTE (°C/ppm)	Tg (°C)
PCB embedded materials	HL832NSF	α1 = 5.3, α2 = 3	265 (TMA)
	GHPL-830NSF	α1 = 6.9, α2 = 3.2	262 (TMA)
DBC ceramic materials	Al_2O_3	7.2	--
	AlN	4.6	--
	Si_3N_4	3	--
	BeO	7	--
SiC MOSFET	4H-SiC	5.1	--

- Effect of ramp rate on thermo-mechanical performance of the cured prepreg

Figure 11 depicts the effect of ramp rate on thermo-mechanical performance of the cured prepreg. As the ramp rate increases, Tg of the cured prepreg rises, while CTE of the cured prepreg decreases. When ramp rate increases to 25 °C/min, Tg of the cured prepreg reaches 273 °C, while CTE below Tg decreases to 5.5 ppm/ °C, which is approaching CTEs of BT laminate and 4H-SiC. Therefore, from the thermo-mechanical performance point of view, the BT laminate and BT prepreg are ideal PCB embedded package materials for SiC power module.

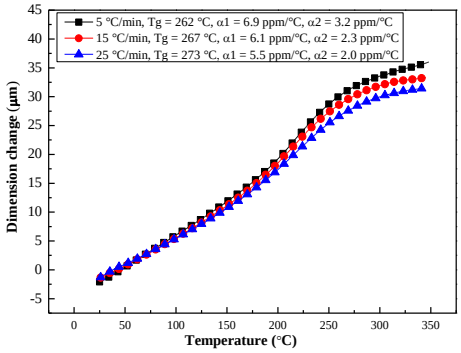

Figure 11. Effect of ramp rate on the in-plane CTE and Tg of the cured prepreg

D. Cure kinetics of BT prepreg

Both dynamic and isothermal DSC experiments are performed to reveal the degree of cure of BT prepreg to provide one guideline for high-temperature and high-pressure laminating process during the PCB embedded SiC MOSFETs packaging. Effects of ramp rate, curing temperature, and curing time on degree of cure of the BT prepreg are analyzed, respectively, and an optimal curing schedule of the prepreg is suggested.

DSC measures the quantitative difference of temperature and heat flow as a function of time and temperature between the target and reference materials when heat evolves from the chemical reaction within the target material. As a guideline, the upper temperature limit of the DSC experiment should not exceed a temperature of 2% weight loss due to decomposition. Based on above analysis results through TGA, when heating rate is 5 °C/min, the temperature of 2% weight loss is about 383 °C. In this section, the upper temperature of dynamic DSC experiment is set to be 330 °C.

- Effect of ramp rate on degree of cure of BT prepreg

Curing or cross-linking of a BT prepreg is an exothermic reaction, while melting of a BT resin is an endothermic reaction. Twice dynamic DSC experiments from room temperature to 330 °C are performed to study the effect of ramp rate on degree of cure of BT prepreg. Figure 12 shows the first heating curves of the prepreg at the ramp rates of 5 °C/min, 10 °C/min, and 20 °C/min. It can be seen that there is an endothermic peak and an exothermic peak when BT prepreg is heating at a ramp rate. There is an endothermic peak at about 50 °C, indicating BT resin inside the prepreg begins to melt. When temperature rises to about 150 °C, heat flow begins to increase, revealing that the prepreg starts to cure. As temperature continues to rise, an exothermic peak appears, at which point the released heat in the cross-link reaction of prepreg is the most. As ramp rate increases from 5 °C/min to 20 °C/min, the magnitude of the exotherm increases as well. The peak temperature shifts to a higher temperature range with increasing ramp rate.

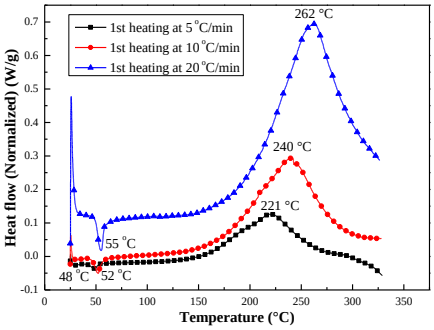

Figure 12. First heating curve of the prepreg at different ramp rates

The second dynamic DSC scans are performed at the same ramp rate as the first scans to examine the degree of cure of the prepreg, as illustrated in Figure 13. When ramp rate is 5 °C/min, exothermic does not exist, indicating that the prepreg is fully cured after first dynamic DSC scan at the heating rate of 5 °C/min. However, when ramp rate increases to above 10 °C/min, there is still exothermic, suggesting that the cross-linking reaction of the prepreg is ongoing as temperature rises. Therefore, lowering ramp rate can improve the degree of cure of the prepreg.

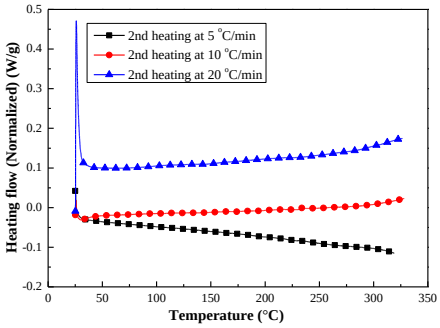

Figure 13. Second heating curve of the prepreg at different ramp rates

- Effect of curing temperature on degree of cure of the BT prepreg

The prepreg is firstly heated up from room temperature to an isothermal curing temperature at a high heating rate of 100 °C/min to avoid any dissipation of heat during heating process, and then isothermally heating for one hour through DSC. Following this scan, the prepreg is cooled down from the isothermal temperature to 25 °C with the same high cooling rate of 100 °C/min to prevent any dissipation of heat during cooling process, and then dynamic heating experiments at a heating rate of 10 °C/min from room temperature to 330 °C are conducted to verify the degree of cure of the prepreg. Figure 14 displays the dynamic DSC scans of the prepreg that have been isothermally for one hour at the curing temperature of 200 °C, 220 °C, 240 °C, 260 °C, and 280 °C. As expected, residual heat released by cross-linking reaction of prepreg decreases with increasing curing temperature. When curing temperature ramps up to 280 °C, after isothermally heating one hour, there is neither exothermic peak nor endothermic peak and the prepreg is fully cured. Therefore, when curing time remains constant, increasing isothermally curing temperature can improve the degree of cure of the BT prepreg. When curing time is one hour,

curing temperature of 280 °C can ensure the full cure of the BT prepreg.

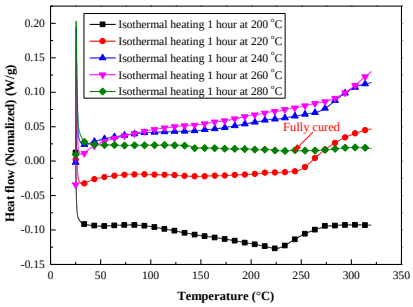

Figure 14. Effect of curing temperature on degree of cure of the BT prepreg

- Effects of curing time on degree of cure of the BT prepreg

The DSC cell is heated up to 210 °C at a high ramp rate of 100 °C/min and then isothermally kept at 210 °C for various time intervals ranging from 30 minutes to two hours. Following this scan, the DSC cell is immediately cooled down to 25 °C at the same ramp rate and then heated up to 330 °C at 10 °C/min to verify the degree of cure of the prepreg. Figure 15 illustrates the dynamic DSC scans of the prepreg that have been isothermally for various curing time at 210 °C. When curing time is below 90 minutes under the curing temperature of 210 °C, there still exists residual cure. After temperature ramps up to about 230 °C, as temperature continues to rise, uncured prepreg would be fully cured. However, when heating two hours, there is neither exothermic nor endothermic peak and the prepreg is fully cured. Therefore, when curing temperature remains constant, increasing curing time can improve the degree of cure of the BT prepreg. When curing temperature is 210 °C, curing time of two hours can ensure the full cure of the BT prepreg.

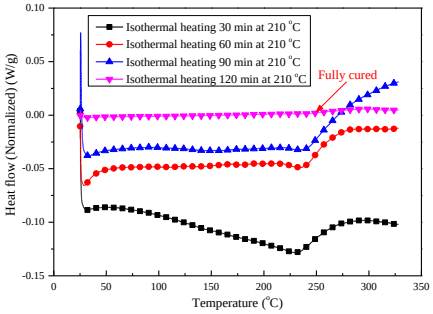

Figure 15. Effect of curing time on degree of cure of the BT prepreg

V. Discussion

From temperature stability, dielectric breakdown strength, thermo-mechanical performance points of view, the selective BT laminate and BT prepreg are ideal PCB embedded materials for SiC MOSFET module package. However, because thermal conductivities of the PCB embedded materials are relatively low, heat dissipation is a major challenge for PCB embedded high power and high power-density SiC MOSFET package. Two-phase cooling technique is a promising solution to address the heat dissipation issue of PCB embedded high power-density SiC module. Taking advantage of the latent heat absorbed during evaporation of the refrigerant fluid, two-phase evaporator can provide higher heat transfer coefficients, lower flow rates, more uniform surface temperatures, and lower pumping power than single-phase cold plates. Dual side cooling design and thermal vias can also improve the thermal performance of the SiC MOSFETs. Moreover, because the proposed PCB embedded SiC MOSFET package is a new packaging technique and novel packaging materials are used, packaging process, switching characteristics, and thermo-mechanical reliability of the PCB embedded SiC MOSFET package needs to be further studied to confirm the feasibility of the PCB embedded materials.

VI. Conclusions

In this work, a novel fan-out panel-level PCB embedded package technology for SiC power module is proposed. BT laminate and BT prepreg are selected as PCB embedded materials. High temperature stability, insulation breakdown strength, and thermo-mechanical performance of the embedded materials and cure kinetics of BT prepreg are characterized. Some conclusions are drawn.

(1) The PCB embedded materials are very thermally stable under the high temperature of 300 °C, and are suitable for SiC power module in the high temperature applications over 175 °C.

(2) The PCB embedded materials can withstand SiC MOSFET drain-source voltage of 1.2 kV, can also be used in the higher voltage SiC package.

(3) The PCB embedded materials have Tg as high as over 260 °C, CTE as low as 5.3 ppm/°C, and match with CTE of 4H-SiC.

(4) For dynamic curing process, lowering ramp rate can improve the degree of cure of the BT prepreg.

(5) For isothermal curing process, one-hour curing time at 280 °C curing temperature and two-hour curing time at 210 °C curing temperature can ensure the full cure of the BT prepreg.

References

[1] D. J. Kearney, S. Kicin, E. Bianda, and A. Krivda, "PCB Embedded Semiconductors for Low-Voltage Power Electronic Applications," *IEEE Trans. Comp. Packag. Manuf. Technol.*, vol. 7, no. 3, pp. 387-395. Mar. 2017.

[2] J. Hornberger, A. B. Lostetter, K. I. Olejniczak T. McNutt, S. Magan Lal, and A. Mantooth, "Silicon-Carbide (SiC) Semiconductor Power Electronics for Extreme High-Temperature Environments," in Proc. *IEEE Aerospace Conference*, Big Sky, MT, 2004, pp. 2538-2555.

[3] R. Khazaka, L. Mendizabal, D. Henry, and R. Hanna, "Survey of High-Temperature Reliability of Power Electronics Packaging Components," *IEEE Trans. Power Electron.*, vol. 30, no.5, PP. 2456-2464, 2015.

[4] J. Fabre, P. Ladoux, and M. Piton, "Characterization and Implementation of Dual-SiC MOSFET Modules for Future Use in Traction Converters," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4079-4090, 2015.

[5] J. Fabre and P. Ladoux, "Parallel Connection of 1200-V/100-A SiC-MOSFET Half-Bridge Modules," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 1669–1676, Jul. 2016.

[6] D. P. Sadik, K. Kostov, J. Colmenares, F. Giezendanner, P. Ranstad, and H. Nee, "Analysis of Parasitic Elements of SiC Power Modules with Special Emphasis on Reliability Issues," *IEEE J. Emerg. Sel. Topics Power*

Electron., vol. 4, no. 3, 2016.

[7] B. Mouawad, M. Soueidan, D. Fabr`egue, C. Buttay, B. Allard, V. Bley, H. Morel, and C. Martin, "Application of the Spark Plasma Sintering Technique to Low-Temperature Copper Bonding," *IEEE Trans. Comp. Packag. Manuf. Technol.*, vol. 2, no. 4, pp. 553-560. Apl. 2012.

[8] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC-DC Converter Systems by SiC Power Semiconductors," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, July 2011.

[9] M. Horio, Y. Iizuka, and Y. Ikeda, "Packaging Technologies for SiC Power Modules," *Fuji Electric Review*, Vol. 58 No. 2, pp. 75-78, 2012.

[10] M. L. Locatelli, R. Khazaka, S. Diaham, C. D. Pham, M. Bechara, S. Dinculescu, and P. Bidan, "Evaluation of Encapsulation Materials for High-Temperature Power Device Packaging," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2281-2288, 2014.

[11] L. Xu, M. C. Wang, Y. Zhou, Z. F. Qian, and S. Liu. "Effect of silicone gel on the reliability of heavy aluminum wire bond for power module during thermal cycling test", in Proc. *IEEE Electronic Components and Technol. Conf. (ECTC)*, Las Vegas, NV, 2016, pp. 1005-1010.

[12] Rhee, H. Y. Hwang, J. Li, J. B. Lee, H. Y. Zhang, "Miniaturized Double Side Cooling Packaging for High Power 3 Phase SiC Inverter Module with Junction Temperature over 220 °C," in Proc. *66th IEEE Electron Comp. Technol. Conf. (ECTC)*, Las Vegas, NV, 2016, pp. 1190-1196.

[13] Z. X. Liang, P. Q. Ning, F. Wang, and L. Marlino, "A Phase-Leg Power Module Packaged with Optimized Planar Interconnections and Integrated Double-Sided Cooling," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 3, Sep. 2014.

[14] L. Stevanovic, "Packaging Challenges and Solutions for Silicon Carbide Power Electronics," Presented at *ECTC Panel Session: Power Electronics – A Booming Market*, 2012.

[15] N. Zhu, H. A. Mantooth, D. H. Xu, M. Chen, and M. D. Glover, "A Solution to Press-Pack Packaging of SiC MOSFETS," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8224- 8234, Oct. 2017.

[16] J. L. Marchesini, P. O. Jeannin, Y. Avenas, J. Delaine, C. Buttay and R. Riva, "Implementation and Switching Behavior of a PCB-DBC IGBT Module Based on the Power Chip-on-Chip 3-D Concept," in IEEE Transactions on Industry Applications, vol. 53, no. 1, pp. 362-370, Jan.-Feb. 2017.

[17] T. Ueda, N. Yoshimatsu, N. Kimoto, D. Nakajima, M. Kikuchi, T. Shinohara, "Simple, compact, robust and high-performance power module T-PM (transfer-molded power module)," in Proc. *The 22nd International Symposium on Power Semiconductor Devices & ICs*, Hiroshima, Japan, pp. 47-50, 2010.

[18] Y. Pascal, A. Abdedaim, D. Labrousse, M. Petit, S. Lefebvre, and F. Costa, "Using Laminated Metal Foam as the Top-Side Contact of a PCB-Embedded Power Die," *IEEE Electron Device Letters*, vol. 38, no. 10, pp. 1453-1456, Oct. 2017.

[19] A. Munding, A. Kessler, T. Scharf, B. Plikat, K. Pressel, "Laminate Chip Embedded Technology-Impact of Material Choice and Processing for Very Thin Die Packaging," in *Proc. 67th IEEE Electron Comp. Technol. Conf. (ECTC)*, Orlando, FL, 2017, pp. 711-718.

[20] R. Randoll, W. Wondrak, A. Schletz, "Lifetime and manufacturability of integrated power electronics," *Microelectron. Rel.*, vol. 64, pp. 513-518, 2016.

[21] T. Löher, S. Karaszkiewicz, L. Böttcher, A. Ostmann, "Compact power electronic modules realized by PCB embedded technology," in *Proc. IEEE CPMT Symposium Japan (ICSJ)*, Kyoto, Japan, 2016, pp. 7-9.

[22] W. Kpobie, M. Martinya, S. Mercier, F. Lechleiter, L. Bodinb, A. Lecavelier des Etangs-Levallois, M. Brizoux, "Thermo-mechanical simulation of PCB with embedded components," *Microelectron. Rel.*, vol. 65, pp. 108-130, 2016.

[23] M. Guyenot, C. Mager, A. Birkhold, R. Ratchev, A. Khoshamouz, T. Gottwald, S. Kreuer, "New Resin Materials for High Power Embedded," in Proc. *67th IEEE Electron Comp. Technol. Conf. (ECTC)*, Orlando, FL, 2017, 690-695.

[24] K. Macurovaa, P. Angerera, R. Bermejob, M. Pletzb, R. Antretterc, T. Krivecd, M. Morianzd, M. Brizouxe, A. Lecaveliere, "Stress and deflection development during die embedded into printed circuit boards," Materials Today: Proceedings, vol. 2, pp. 4196–4205, 2015.

[25] S. Toyoshima, S. Hatsukawa, N. Hirakata, T. Tsuno, Y. Mikamura, "Compact SiC Power Module for High Speed Switching," EI TECHNICAL REVIEW, No. 80, pp. 81-84, 2015.

[26] L. F. Sun, I. I. Negulescu, S. S. Pang, and A. M. Sterling, "Characterization of BT Prepreg Curing Process," the Journal of Adhesion, vol.82, pp. 161-179, 2006.

[27] Y. He and X. J. Fan, "In-situ Characterization of Moisture Absorption and Desorption in a Thin BT Core Substrate," in *Proc. 57th IEEE Electron Comp. Technol. Conf. (ECTC)*, Reno, NV, 2007, 1375-1382.

[28] V. Chidambaram, E. P. H. Rong, G. X. Lip, R. M. W. Daniel, "Cyanate Ester-Based Encapsulation Material for High-Temperature Applications," *Journal of Electronic Materials*, vol. 42, no. 9, pp. 2803-2812, 2013.

[29] R. M. W. Daniel, H. Y. Hwang, J. Li, "High Power SiC Inverter Module Packaging Solutions for Junction Temperature over 220 °C," in Proc. *16th IEEE Electron. Packag. Technol. Conf. (EPTC)*, Singapore, pp. 31-35, 2014.

[30] L. Li, N. Bowler, P. R. Hondred and M. R. Kessler, "Statistical Analysis of Electrical Breakdown Behavior of Polyimide Following Degrading Processes," *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 18, no. 6, pp. 1955-1962.

[31] Z. Chen, Y. Y. Yao, D. S. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET Multichip Phase-Leg Module for High-Temperature, High-Frequency Applications," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2307-2320, 2014.