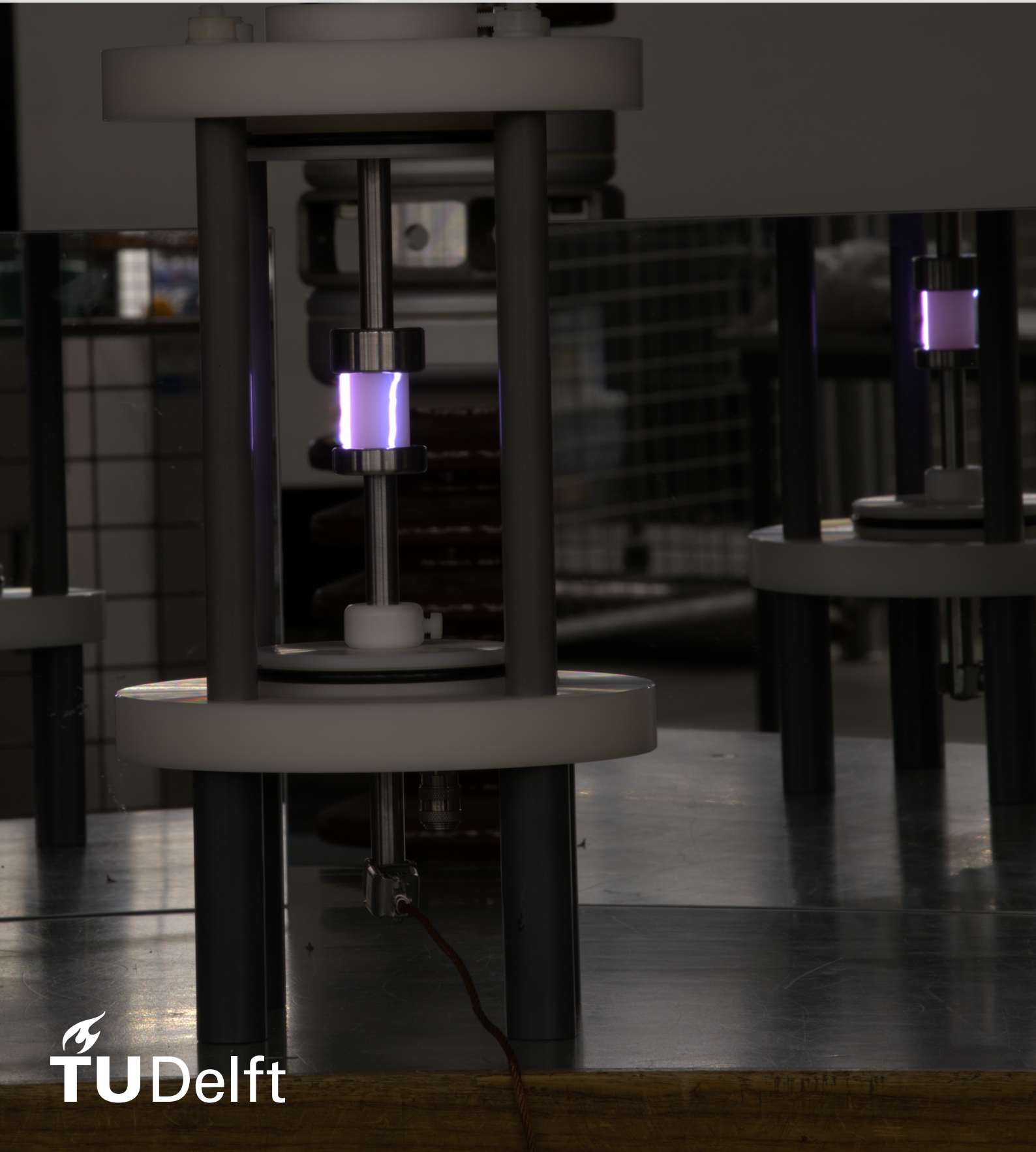
Laboratory scale HVDC GIS test setup for DC/LI flashover studies

Abhay Shenoy



TU Delft

Laboratory scale HVDC GIS test setup for DC/LI flashover studies

by

Abhay Shenoy

to obtain the degree of Master of Science

at the Delft University of Technology,

to be defended publicly on Monday July 24, 2026 at 14:00 PM.

Student number:	5510473
Project duration:	December 12, 2025 – July 24, 2026
Thesis committee:	Prof. ir. P. Vaessen, TU Delft, Responsible supervisor
	Dr. ir. D. van der Born, TU Delft, Daily supervisor
	Prof. ir. R. Santbergen TU Delft, Externalcomittee

An electronic version of this thesis is available at http://repository.tudelft.nl/.

TU Delft

Acknowledgments

The thesis is a culmination of 5 years of studying at TU Delft and would not have been possible without the help of many different people.

Firstly, I would like to thank my thesis advisor, Peter Vaessen, for helping guide my research and providing invaluable feedback on my work. I am also grateful to my daily supervisor, Dennis van der Born, for sharing his valuable knowledge with me, for the many discussions that shaped the direction of this research, and for his patience in working through problems with me whenever I got stuck. I would also like to thank the lab coordinator, Imke Splinter, for her continued support and practical guidance in the laboratory, without which much of the experimental work would not have been possible.

Secondly, I would like to thank all my friends and colleagues who, directly or indirectly, contributed to this thesis, whether through their insights or simply through their good company along the way. Their encouragement made the difficult times of this project far easier to carry.

Finally, I would like to thank my family, and especially my parents, who have supported me every step of the way and never stopped believing that I could achieve what I set out to do. Everything I have achieved is thanks to you.

Abhay Shenoy
Delft, July 2026

Abstract

The increasing adoption of High Voltage Direct Current (HVDC) transmission in recent years has been driven by the growth of long-distance bulk power transfer. This expansion is increasing the deployment of DC Gas-Insulated Switchgear (GIS) and Gas-Insulated Lines (GIL), which use pressurized SF_6 for greater compactness than existing air-based insulation systems. DC operation, however, introduces charge accumulation on spacers, resulting in greater electrical stress on the insulation. The effect of the accumulated charges becomes particularly important during Lightning Impulse (LI) overvoltages and may cause spacer flashovers. Although this phenomenon has been studied for SF_6, regulatory pressure is now driving a transition to alternative gases for which this behavior remains poorly understood.

The outcome of the thesis is a fully manufactured test cell with a camera arrangement to capture flashover across the insulator surface. A reduced-scale bowl plate electrode geometry is designed using Finite Element Method (FEM) simulations using an ion flow model to reproduce the quasi-homogeneous field distribution and surface charge accumulation behavior of HVDC GIS disc spacers, and the design is validated for operation at pressures up to 3 bar with technical air. A pressurized floating enclosure was also designed, dimensioned, and manufactured to safely contain alternative gases at a maximum operational stress of 30 kV DC with a superimposed $\pm$ 150 kV LI. A composite voltage test circuit was then designed from available laboratory equipment and validated in LTspice.

Verification in the lab revealed repeatability issues with the spacer electrode contact, which were resolved by redesigning the spacer electrode to use a screw arrangement. Surface charge measurements showed poor agreement with the initial simulation, with additional ionization sources in the test setup not being accounted for in the model. Comparisons with external data, however, showed good agreement with measured surface potentials. The composite test circuit using a spark gap and a coupling capacitor has been tested in the TU Delft HV lab, and the test experience is presented. Further work must be pursued on charge measurements under DC application in technical air, and validation of the test circuit with higher applied voltages and LI breakdown tests with pressurized gas. With this remaining work completed, the cell can be used to systematically measure and visualize spacer flashover under composite DC/LI voltages in alternative gases.

Contents

Preface i

Abstract ii

Nomenclature xii

1 Introduction 1
- 1.1 Background . . . 1
- 1.2 Research Objectives . . . 2

I Theory and Background 4

2 Theory of GIS Operation 5
- 2.1 GIS Fundamentals . . . 5
- 2.2 Electrical Stresses . . . 7
- 2.3 Charge Transport . . . 9
  - 2.3.1 Bulk Conduction . . . 10
  - 2.3.2 Surface Conduction . . . 10
  - 2.3.3 Gas Conduction . . . 10
- 2.4 Alternative Gases . . . 11

3 Literature Review 12
- 3.1 Comparisons of AC and DC GIS . . . 12
- 3.2 DC GIS Spacers . . . 14
- 3.3 Transient Behaviors . . . 17
- 3.4 Surface Flashover . . . 19

II Design 22

4 Electrode Design 23
- 4.1 Field Utilization Dimensioning . . . 23
  - 4.1.1 AC GIS Approximation . . . 24
  - 4.1.2 Extraction of Fields from Research . . . 24
- 4.2 Design Parameters . . . 25
  - 4.2.1 Numerical Requirements . . . 25
  - 4.2.2 Design Criteria . . . 26
  - 4.2.3 Scaling . . . 27
- 4.3 Finalized Electrode Geometry . . . 28

4.3.1 Shape Optimization . . . 29
4.4 Field Simulations . . . 30
4.4.1 DC simulations . . . 31
4.4.2 DC/LI simulations . . . 35
4.4.3 Charge Simulations . . . 37

5 Enclosure Design **41**
5.1 Models considered . . . 41
5.1.1 Floating Cell . . . 42
5.1.2 Spacer Cell . . . 42
5.1.3 Metal Flange Cell . . . 43
5.2 Clearance Distances . . . 43
5.2.1 Internal Volume . . . 44
5.2.2 External Sizes . . . 44
5.3 Field Simulations . . . 45
5.3.1 DC Simulations . . . 46
5.3.2 DC/LI Simulations . . . 47
5.3.3 Charge Simulations . . . 48

6 Test Circuit Design **51**
6.1 Equivalent Model . . . 52
6.1.1 DUT Equivalent Parameters . . . 52
6.2 Optimizing Impulse Parameters . . . 53
6.3 Choice of Impulse Coupling . . . 54
6.3.1 Coupling Capacitor . . . 55
6.3.2 Spark Gap . . . 56
6.4 Choice of DC Blocking . . . 58

III Verification **60**

7 Experimental Setup **61**
7.1 Manufacturing of the Cell . . . 61
7.1.1 Testing Preparation . . . 63
7.1.2 Camera Setup . . . 63
7.2 Testing Definitions . . . 64
7.2.1 DC Charge Testing . . . 64
7.2.2 LI Procedure . . . 66
7.2.3 DC/LI Procedure . . . 68

8 Laboratory Experiments **71**
8.1 Preliminary LI Tests . . . 71
8.2 Charge Accumulation Tests . . . 75
8.2.1 Comparison to measurements . . . 78
8.3 DC LI Circuit Verification . . . 79

9 Conclusion & Recommendations **84**
9.1 Conclusion . . . 84
9.2 Recommendations . . . 85

A Review of Standards **94**
A.1 IEC 60060-1 . . . 95
A.1.1 DC Voltages . . . 95
A.1.2 LI Voltages . . . 95
A.1.3 Composite Voltages . . . 96
A.2 CIGRE TB 842 . . . 97
A.2.1 DC Insulation Test . . . 98
A.2.2 Superimposed DC/LI test . . . 98

B Research Based Dimensioning **100**
B.1 DC GIS Simulation-Based Dimensioning . . . 100
B.2 Test Cell Review . . . 100

C Additional Modelling **102**
C.1 Simulation Method . . . 102
C.2 Implementation of Charge accumulation . . . 104
C.2.1 Bulk Current Density . . . 104
C.2.2 Surface Current Density . . . 106
C.2.3 Gas Current Density . . . 106
C.2.4 Model verification using Analytical Formula . . . 108
C.3 Spacer: Aluminum Filled epoxy Resin . . . 110
C.4 Electrode: Modified Parallel Plate . . . 110
C.4.1 Field Simulations . . . 111
C.4.2 DC/LI Simulations . . . 113
C.4.3 Charge Simulations . . . 113
C.5 Electrode: Modified Pinch Plate . . . 114
C.5.1 Field Simulations . . . 115
C.5.2 Charge Simulations . . . 116
C.6 DC GIS Model Simulation . . . 117
C.6.1 Field Simulations . . . 118
C.6.2 Charge Simulations . . . 119
C.7 Enclosure: Metal Cell . . . 120
C.7.1 Field Simulations . . . 122
C.7.2 Charge Simulations . . . 123
C.8 Enclosure: HV Flange . . . 124
C.8.1 Field Simulations . . . 125
C.8.2 Charge Simulations . . . 127

D LTSPICE simulation Netlist **129**

E Statistical Analysis **131**
E.1 Atmospheric Correction (IEC 60060-1) . . . 131

E.2 Statistical Analysis Up and Down Tests 132
E.2.1 Maximum Likelihood estimate 132

F Additional Information **134**
F.1 Electrostatic Voltmeter Recordings 135

List of Figures

2.1 Component diagram in a Siemens 8DN8 GIS system with the components 1) Control cubicle 2) Current Transformer 3) Disconnector/Earthing switch 4) Circuit Breaker 5) Disconnector/Earthing switch 6) Circuit Breaker Control 7) Voltage Transformer 8) High Speed Earthing Switch 9) Cable/Line Disconnector 10) Cable Sealing [14] 6
2.2 Model of the conductor and conical spacer used in a DC GIL with flanges(yellow) and electrode shielding (light blue) [16] 6
2.3 Superimposed DC/LI waveforms specified for testing according to CIGRE TB 842 [12] . 8
2.4 Simplified ion movement process across spacer surface given a positive applied voltage 9

3.1 Polarity reversal from +450 kV (t = 0^-) to -450 kV (t = 0^+) in an HVDC paper-insulated cable for two different temperature gradients [6] 13
3.2 Comparison of AC transitional and DC steady state stress for a simulated DC GIS section with a basin insulator [17] 14
3.3 Surface charge density across the radius of a spacer for different prestress times and under a temperature gradient [36] 15
3.4 Impact of pressure on surface charge accumulation for a real-size insulator under $\pm$ 100 kV DC for 3 gas pressures [37] 15
3.5 Flashover voltages for a coated and $\sigma - SFGM$ coated spacer under different temperature gradients [42] 16
3.6 Electric field distribution across basin and disc-shaped spacer under - 60 kV applied DC for a) basin type and b) disk type [43] 16
3.7 Total simulated electric field distribution along the spacer for superimposed voltages for Zero Load (a) and High Load (b) [20] 17
3.8 Flashover voltages of contaminated insulator under superimposed DC/LI voltages [48] . 18
3.9 Comparison of flashover voltages under superimposed DC/-LI for 3 alternative gasses and with a particle [49] 19
3.10 Surface and bulk breakdown voltages for a gap size of 4.71mm [22] 20
3.11 Possible flashover paths in a basin insulator [50] 20

4.1 Simulation of the electric field for a basin spacer from [21] under a +200 kV DC voltage 25
4.2 Effective ionization coefficient $(\alpha - \eta)$ as a function of reduced field E/P for many different gasses [55] 27
4.3 COMSOL model of the finalized electrode geometry with the given optimization parameters 29
4.4 Field profile of case 1 test setup compared to a simulated DC GIS system with a modified disc spacer [51] 30
4.5 Electric field streamlines across transition for PTFE given +30 kV DC 31

4.6 Simulations of electric field across 2 hrs for a given voltage of + 30 kV DC for nylon . . 32
4.7 Simulations of electric field across 120 hours for a given voltage of + 30 kV DC for PTFE 32
4.8 Derivative of Voltage across spacer surface and $t_{90\%}$ for +30 kV DC 32
4.9 Simulation of spacer field components across time 1 hour for Nylon, given applied +30 kV DC 33
4.10 Simulation of spacer field components across 128 hours for PTFE, given applied +30 kV 33
4.11 Applied SIMP OP waveform for 40 kV/-120 kV on COMSOL 35
4.12 Development of tangential fields across the spacer for applied +150 kV impulse with PTFE 35
4.13 Comparison of tangential fields from 2 hours of charges in both cases for +30 kV DC, where blue represents negative charge and red positive 36
4.14 Comparison of tangential fields during different polarities of superimposed stresses for 30 kV DC and $\pm$ 150 kV LI 36
4.15 Ion concentrations under steady-state DC given applied +30 kV DC 37
4.16 Ion density across spacer for steady state +30 kV DC 37
4.17 Gas conductivity derived from ion density in COMSOL 38
4.18 Conduction currents on spacer surface from gas and bulk for Nylon and PTFE 39
4.19 Conduction current process on charge accumulation (Red = Bulk dominated, Green = Gas dominated) 39
4.20 Simulation of the surface charge across the PTFE spacer for +30 kV DC 40

5.1 Floating Cell **(1)** 42
5.2 Spacer Topped Cell **(2)** 42
5.3 Metal Flange Cell **(3)** 43
5.4 3D CAD model of the floating cell with mechanical supports, considered courtesy of Javier Gonzalez Martin 43
5.5 Scale-accurate COMSOL setup of the simplified floating enclosure filled with technical air 45
5.6 Electric field of simplified floating cell comparison with applied +30 kV DC 46
5.7 Field streamlines for capacitive and resistive field given +30 kV DC 47
5.8 FEM results of the field across both the inside and outside of the Nylon flange and the plexiglass wall during DC application 47
5.9 Tangential field across both the inside and outside of the Nylon flange and the plexiglass wall during different superimposed DC/LI applications 48
5.10 Ion concentrations under steady-state DC for the test cell given applied +30 kV DC . . 49
5.11 Floating Cell gas conductivity 49
5.12 Surface charge across the inside and outside of all insulating materials for +30 kV DC . 50

6.1 DC/LI composite test circuit, Blue represents Impulse generator, Orange represents DC source, and the dashed sections represent the used dividers 51
6.2 Equivalent impulse ”b” circuit considered for simulation 52
6.3 Acceptable values of R_f to achieve a IEC standard Lightning impulse for the given C_L . 54
6.4 LTspice simulations of the superimposed circuit from Appendix D for both Coupling elements . Note that spark gap extinction was set to 0.001 V_{imp} 55
6.5 DUT impulse efficiency vs Coupling capacitor C_c size 56

6.6 LTspice simulations of both the dividers . . . 57
6.7 LTspice simulations of the spark gaps, including front chopping, based on different breakdown times for an assumed test capacitance of 2nf . . . 57

7.1 Manufacturing of the electrodes and spacer done by the HV lab of TU Delft . . . 62
7.2 Manufactured test cell with and without Plexiglass annotated . . . 62
7.3 Camera placement to capture surface flashovers on all sides . . . 63
7.4 Example image showing flashover location being captured by the mirrors . . . 64
7.5 Test circuit of DC charge measurement tests . . . 65
7.6 DC charge measurement test schematic . . . 65
7.7 Annotated charge measurement points across spacer surface . . . 65
7.8 Test circuit used for LI testing with labeled components . . . 66
7.9 LI breakdown testing schematic . . . 67
7.10 Up and down test procedure [81] . . . 67
7.11 Single discharge method . . . 68
7.12 Progressive stress test procedure [88] . . . 68
7.13 Spark gap test circuit used for DC/LI testing with labeled components . . . 69
7.14 Coupling Capacitor test circuit used for DC/LI testing with labeled components . . . 69
7.15 Flowchart for LI and composite DC/LI spacer flashover progressive stress test procedure 70

8.1 Preliminary up and down test performed with nylon spacer . . . 71
8.2 Flashover initiation marks from preliminary impulse testing, with red indicating triple-junction initiation and blue indicating shield initiation . . . 72
8.3 Different discharge paths of the tested nylon spacer under LI flashover . . . 72
8.4 Simulated effect of a 0.1 mm air gap between HV electrode and spacer arising from mounting errors . . . 73
8.5 Spacer modifications with screw mount into electrode . . . 74
8.6 Preliminary up and down test for both spacer materials with the new screw contact . . . 74
8.7 Time to breakdown across the different tests . . . 75
8.8 Different observed breakdown paths for PTFE under LI voltages . . . 75
8.9 Electrical conductivity in gas volume with ambient air parameters . . . 76
8.10 Charge accumulation across a section of the insulator compared to simulation with ambient air for +10 kV DC applied for 2 hours . . . 76
8.11 Charge accumulation across a section of the insulator compared to a simulation with IP = 1600 IP/cm^3s and 16000 IP/cm^3s for +10 kV DC applied for 2 hours . . . 77
8.12 2D axisymmetric simulation model used by Schueller et al. [94] with SF_6 at 0.4 MPa . . . 78
8.13 Simulation compared with measurements from Schueller et al. [94] for an applied $\pm$1 kV DC over 1 hour . . . 78
8.14 Recorded withstand voltage waveforms for early spark gap trigger at 41 kV . . . 80
8.15 Recorded withstand voltage waveforms for late spark gap trigger at 55 kV . . . 80
8.16 Recorded breakdown voltage waveforms for spark gap with common Impulse generator ground . . . 81
8.17 Recorded breakdown voltage waveforms for spark gap with separate Impulse generator ground . . . 81

8.18 Recorded withstand voltage waveforms for coupling capacitor 82
8.19 Recorded breakdown voltage waveforms for coupling capacitor 82

A.1 IEC 60060-1 specified 1.2/50 lightning waveform with T1 and T2 96
A.2 IEC 60060-1 specified composite voltage testing circuit with 3 measurements 97
A.3 CIGRE TB 842 specified DC/LI composite testing setup with a blocking capacitor 98
A.4 Image comparing the difference in tails(D1) and discharging to 0kv and returning to DC(D2) for a spark gap and coupling capacitor 99

C.1 COMSOL Multiphysics simulation workflow 103
C.2 Meshed system chosen for the defined geometry 103
C.3 Aluminum-filled Epoxy conductivities with σ_0 = 2×10^{-18} [S/m], $\alpha = 0.08$ and $\beta = 0.1$ [34] varied by temperature and electric field 105
C.4 Gas conduction current linearity for applied voltages [66] 107
C.5 Conduction Current on an insulator surface for different Ion generation rates 1/$(cm^3 * s)$ 107
C.6 Flowchart for simulation method used with coupled electric currents and electric discharge interface 108
C.7 Gas current ohmic and saturation behavior validation for a parallel plate electrode . . . 109
C.8 Electrical Conductivity of Epoxy Resin [115] 110
C.9 Capacitive to resistive transition with Epoxy Resin model[115] 110
C.10 COMSOL model of parallel plate electrode geometry 111
C.11 COMSOL modified parallel plate simulation for +30 kV DC 111
C.12 FEM results parallel plate comparison: AC (left) and DC (right). 112
C.13 Field components across spacer for AC and DC given a +30kV DC 112
C.14 Field simulation for different DC/LI stresses given nylon spacer 113
C.15 Ion densities simulated for +30 kV DC 113
C.16 FEM simulation of the surface charge across the spacer for +30 kV DC 114
C.17 COMSOL setup of pinch plate geometry 114
C.18 COMSOL parallel plate comparison: Potential streamlines(left) and Field contours (right) 115
C.19 FEM results pinch plate comparison: AC (left) and DC (right). 115
C.20 DC field components 116
C.21 DC/LI comparims 116
C.22 steady state ion distribution 117
C.23 FEM simulation of the surface charge across the spacer for +30 kV DC 117
C.24 Scale accurate COMSOL setup of the simplified floating enclosure filled with technical air 118
C.25 Model GIS steady state potential and field distribution for an applied +200kV 118
C.26 Model GIS field transition for applied voltage of +200 kV 119
C.27 Model GIS surface field components during steady state for applied voltage of +200 kV 119
C.28 Model DC GIS steady state ion concentrations for +200kV 120
C.29 Model GIS steady state charge accumulation across spacer for applied +200kV 120
C.30 Metal cell 126 kV Disc spacer model used from a paper by Wang et al.[117] 121
C.31 2D axisymetric metal cell setup simulated in COMSOL 121
C.32 COMSOL simulation of potential contour and electric field streamlines for the metal spacer topped cell 122

C.33 FEM results of simplified metal cell comparison with applied +30 kV DC: AC (left) and DC (right) . . . 122
C.34 DC Flange HV . . . 123
C.35 OP DC/LI Flange HV . . . 123
C.36 ion densities . . . 124
C.37 Charge Flange HV . . . 124
C.38 Scale accurate COMSOL setup of the simplified floating enclosure filled with technical air 125
C.39 . . . 125
C.40 FEM results of simplified HV flange cell comparison with applied +30 kV DC: AC (left) and DC (right) . . . 126
C.41 DC Flange HV . . . 126
C.42 OP DC/LI Flange HV . . . 127
C.43 ion densities . . . 127
C.44 Charge Flange HV . . . 128

D.1 LTSPICE TEST CIRCUIT . . . 130

F.1 Initial design of BP electrodes prior to optimization . . . 134
F.2 Effect of load capacitance on the chopping dip relative to the impulse circuit C_{load}. Blue (0.6pF) is significantly smaller, orange (600pF) approximately equivalent, and green (2 nF) much larger than the impulse circuit capacitance . . . 134

Nomenclature

Abbreviations

Abbreviation	Definition
AC	Alternating Current
AIS	Air-Insulated Substation
BDV	Breakdown Voltage
CAD	Computer Assisted Design
DC	Direct Current
DUT	Device Under Test
EHV	Extra-High Voltage
FEM	Finite Element Method
GIL	Gas-Insulated Line
GIS	Gas-Insulated Switchgear
GND	Ground
GWP	Global Warming Potential
HL	High Load
HV	High Voltage
HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineer
LI	Lightning Impulse
MV	Medium Voltage
OP	Opposite Polarity
OPR	Oscillating Polarity Reversal
PD	Partial Discharge
PRPD	Phase Resolved Partial Discharge
SP	Opposite Polarity
VSC	Voltage Source Converter
ZL	Zero Load

1

Introduction

1.1. Background

The global power system is currently expanding rapidly, driven by the growing scale of renewable energy installations worldwide. Bulk generation of renewable sources such as wind, solar, and hydro is primarily located far from urban centers, creating a need for long-distance, high-capacity, and economical transmission [1]. Historically, High-voltage Alternating Current (HVAC) was chosen as the primary transmission technology because the early development of transformers enabled voltage stepping up-/down and the transfer of energy over longer distances with lower I^2R losses. The development of mercury arc valves in the 1930s, followed by advancements in semiconductors in the 1960s, made High-voltage Direct Current (HVDC) a viable transmission option. HVDC is the preferred solution for bulk long-distance transmission, particularly for long-distance and submarine cable applications, due to advantages such as the absence of capacitive charging currents in long cables, improved conductor utilization, and the ability to interconnect asynchronous networks [2, 3, 4]. These operational benefits have made HVDC especially attractive for future long-distance grid interconnections.

Switchgear is an important substation component, as it provides dielectric insulation, switching capability, and fault-interrupting capability at the interfaces between lines, cables, and converters. Early switchgear relied on air as the primary insulating medium, which limited the achievable voltage levels and the system's compactness [5]. The introduction of GIS in the 1960s marked a technological step forward by enclosing the conductors in a high-performance dielectric gas, which enabled higher insulation strength, reduced equipment size, and greater isolation from environmental conditions. HVDC GIS has recently gained prominence and is being considered for the aforementioned DC transmission benefits and space savings. The use of HVDC GIS, however, fundamentally differs from HVAC GIS in that the constant field under operation causes charge accumulation on non-conductive materials such as the spacers [6].

Within GIS assemblies, solid components, such as epoxy spacers, are used to support the conductor and to separate it from the enclosure. Under AC operation, the field distribution is largely governed by the permittivity and is weakly dependent on the electric field and temperature. In HVDC operation, however, the field distribution is instead governed by the material's conductivity, which exhibits a much stronger dependence on the electric field and temperature. DC operation also leads to problems such as surface charge accumulation and local field enhancements at the triple junctions, which reduce the insulator's strength against incoming transients. Moreover, the geometry of the spacer, material, and position affects the electric field and must be carefully considered, as these factors can cause field enhancements, charge accumulation, and creepage paths for flashovers [7, 8].

Sulfur hexafluoride (SF_6) has been widely used as the benchmark insulating gas in GIS systems due to its dielectric strength and arc extinguishing capabilities. SF_6, however, has a global warming potential (GWP) approximately 23,500 times that of CO_2 and an atmospheric lifetime exceeding 3,200 years, making it a very potent greenhouse gas. There is therefore strong regulatory pressure to find alternatives and phase out the use of the gas from electrical equipment [9]. Many low GWP alternatives such as C_4F_7N ,CF_3I and other non fluoridated mixtures are currently being researched [9, 10, 11]. In practice, carrier gases are used to dilute the mixture, making it suitable for use in GIS or GIL systems. While the mixtures approach the dielectric strength of SF_6, the behavior at these gas-spacer interfaces and during breakdowns remains not completely understood. Characterizing the insulation behavior of HVDC systems using alternative gas mixtures under operational HVDC GIS stresses is important before widespread deployment.

Realistic insulation assessment for alternative gases in HVDC GIS must account for the combined stresses experienced in service, of which one of the most frequent and critical is the superimposition of a lightning impulse onto an established DC voltage (DC/LI), where a Lightning Impulse (LI) is applied on a DC stressed insulator. This condition is especially relevant for outdoor-installed overhead line terminations or outdoor converter stations and is consequently a key requirement in standards such as [12] and [13]. The spacer flashover behavior of alternative gas mixtures under such composite voltage conditions remains insufficiently characterized, representing a significant gap in the knowledge base required for confident technology qualification and market adoption. The development of a laboratory-scale test platform at TU Delft enables research for the improved understanding of spacer flashover behavior under DC/LI voltages in alternative gases.

1.2. Research Objectives

The main objective of this research is to design and build a representative scaled-down HVDC GIS system for testing composite voltages in alternative insulating gases. The research question guiding this project can be stated as follows:

Research Question

What is a suitable laboratory-scale test system for the study of spacer flashover behavior under composite DC/LI voltages in alternative gas-filled HVDC GIS?

This thesis is organized into three main parts, each building upon the previous to address the research

question systematically. The following parts present the theory and background, the design of the reduced-scale test platform, and the verification of the complete test system.

Part I: Theory and Background establishes the theoretical foundations for understanding insulation behavior in HVDC GIS systems. Chapter 2 introduces the fundamentals of GIS operation, covering system components, electrical stresses under DC conditions, charge transport mechanisms governing surface charge accumulation, and an overview of alternative insulating gases. Chapter 3 presents a comprehensive literature review examining the key differences between AC and DC GIS; the role of surface charge accumulation in spacer performance; transient stresses and electrically weak points in DC GIS; and the mechanisms governing surface flashover.

Part II: Design details the development of the reduced-scale test platform across three major areas. Chapter 4 covers the electrode system, which is designed to replicate the quasi-homogeneous field distributions of HVDC GIS disc spacers with charge and field simulations. Chapter 5 presents the enclosure design, including candidate models evaluated, internal clearance dimensioning, and field validation through DC, DC/LI, and charge simulations. Chapter 6 describes the test circuit design, covering the equivalent circuit model, impulse parameter optimization, and the selection of impulse-coupling and DC-blocking elements based on the equipment available in the TU Delft HV laboratory. Together, these chapters show how the test platform was designed to support the experimental verification.

Research Sub-Question 1

What is a suitable reduced-scale system to be designed for reproducing the dielectric stress conditions representative of HVDC GIS systems?

Part III: Verification presents the experimental validation of the complete test system. Chapter 7 describes the experimental setup, including cell manufacturing, laboratory setup, and the test methodology for LI, DC/LI, and charge accumulation procedures. Chapter 8 presents the air-based experimental results, covering preliminary LI flashover testing, charge accumulation measurements, and DC/LI circuit verification.

Research Sub-Question 2

What test circuit is required to safely generate and apply composite DC/LI voltages to a representative HVDC GIS geometry?

Finally, Chapter 9 summarizes the conclusions drawn with respect to the research questions, clarifies what was achieved, and provides recommendations for future work.

Part I Theory and Background

2

Theory of GIS Operation

This chapter presents the theoretical basis for the analysis conducted in this work. The operating principles of HVAC and HVDC GIS are considered with a focus on the internal components, electrical stresses, and insulation performance. The mechanisms of charge transport and the use of alternative gases are examined. The concepts in the chapter provide the knowledge needed to design and implement the test circuit and electrode setup in subsequent chapters.

2.1. GIS Fundamentals

GIS systems are compact, metal-enclosed systems designed for high-voltage transmission in areas where space, reliability, or protection are important. Gas-insulated lines share the same coaxial geometry and materials, but they differ in function. GIL is primarily used for long-distance power transmission and therefore contains only the conductor enclosure and supporting insulators, while GIS includes additional components such as circuit breakers, grounding switches, and current and voltage transformers. These components allow GIS to perform switching, protection, and measurement. The structure of a GIS, including the components, is shown in Figure 2.1 below.

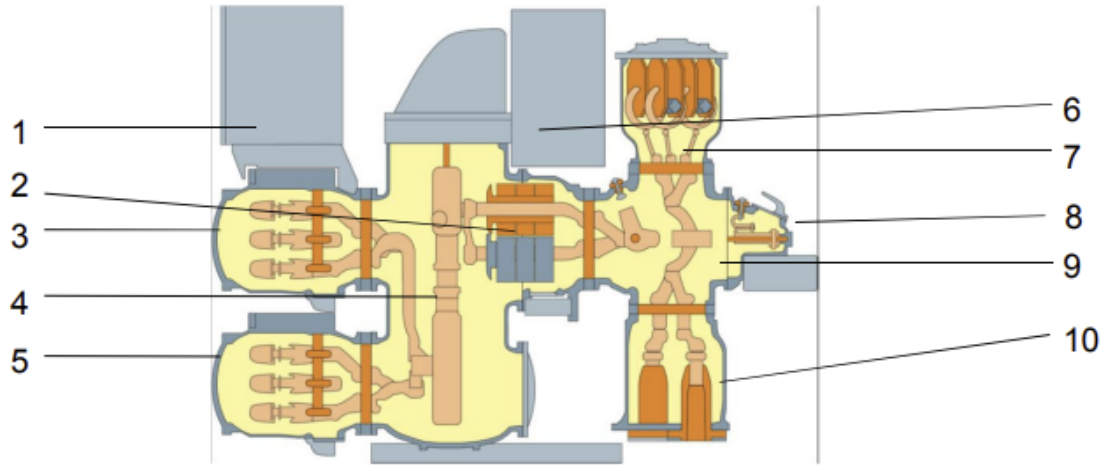


Figure 2.1: Component diagram in a Siemens 8DN8 GIS system with the components 1) Control cubicle 2) Current Transformer 3) Disconnector/Earthing switch 4) Circuit Breaker 5) Disconnector/Earthing switch 6) Circuit Breaker Control 7) Voltage Transformer 8) High Speed Earthing Switch 9) Cable/Line Disconnector 10) Cable Sealing [14]

The primary conduction components of a GIS/GIL system are the conductor, enclosure, and supporting spacers. The central conductor carries the high currents and is designed to maximize the current-carrying capacity while maintaining acceptable electric field levels. The outer shell of the GIS enclosure is normally grounded and made of materials such as steel or aluminum, depending on size, for strength to withstand internal gas pressures or for ease of welding. The internal conductor is also held in the center of the enclosure using spacers, most commonly with disk, conical, or basin geometry [15]. These components are common to GIS and GIL systems and will be the primary focus of the study. Figure 2.2 shows a 3D model of the components in a DC GIL with commonly found geometries.

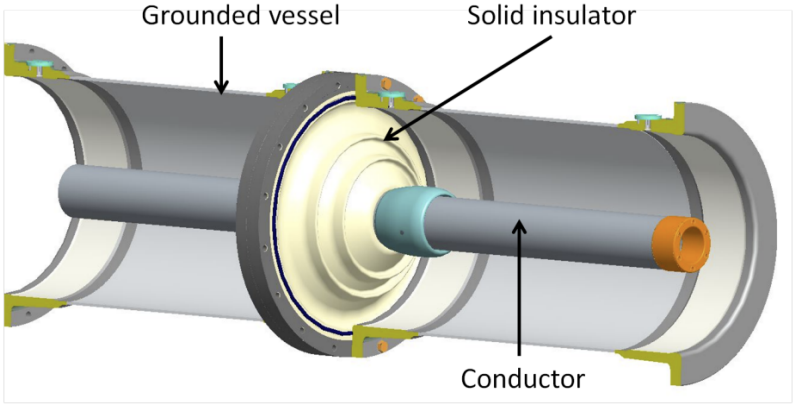


Figure 2.2: Model of the conductor and conical spacer used in a DC GIL with flanges(yellow) and electrode shielding (light blue) [16]

In addition to the primary conduction components, typical GIS systems also contain switching and grounding equipment to enable safe isolation and earthing during maintenance. Both HVAC and HVDC GIS include disconnector switches, which provide isolation points for de-energizing the high-voltage components, and grounding switches that earth the disconnected section [17]. In AC GIS, these are typically combined into a three-position switch, often complemented by high-speed earthing

switches on the line side, which are rated to close safely onto energized conductors. Surge arresters based on metal-oxide varistors (MOVs) are also employed in both AC and DC GIS to limit lightning and switching overvoltages. In DC GIS, they must additionally withstand the continuous DC operating voltage and be coordinated with the converter stations during fault energy dissipation. For measurement, AC GIS uses conventional instrument transformers to transform current and voltage down to metering levels [18], whereas DC GIS relies on optical or electronic sensors. Another distinction lies in fault interruption with AC GIS, which incorporates circuit breakers as the primary fault interruption device, whereas interrupting DC is inherently more difficult due to the absence of a natural current zero-crossing. DC fault clearing has therefore historically been managed at the converter level, and although dedicated HVDC circuit breakers have now been demonstrated and deployed. Table 2.1 shows commercially available Ultra High Voltage (UHV) AC and DC GIS.

Table 2.1: Comparison of the highest performing commercial UHV AC GIS and DC GIS

Parameter	Hitachi AC GIS[18]	Siemens DC GIS[19]
Rated voltage [kV]	1200	± 550
Rated frequency [Hz]	50	N.A
Rated short-duration power-frequency withstand (1 min) [kV]	1100	n/a
Rated lightning impulse withstand (1.2/50 µs) [kV]	2400	1550
Rated switching impulse withstand (250/2500 µs) [kV]	1800	1175
Rated normal current (feeder) [kA]	5	5
Rated normal current (busbar) [kA]	8	5
Rated short-time withstand current [kA]	63	50
Operational temperature range [°C]	[-30 … +40]	[-30 ... +50]

2.2. Electrical Stresses

Gas-insulated switchgear is subjected to a range of electrical stresses that vary significantly with system configuration, operating conditions, and transient events. For HVDC applications, the three most relevant stress categories for this paper are the continuous DC operating voltage, fast-transient overvoltage, such as lightning impulses (LI), and the superimposed combination of DC pre-stress and LI. DC stress occurs during system operation, and superimposed LI transients are considered among the most stressful conditions an insulation system must withstand. [20]

Under normal operating conditions, HVDC GIS is exposed to a continuous DC voltage that establishes a time-dependent electric field distribution. In the initial moments of voltage application, the electric field is governed by the capacitive response of the insulation, as no free charge has yet accumulated in the system. In this regime, the field distribution is determined solely by the permittivity of the materials. For such electrostatic problems, the Maxwell equations reduce to the Poisson equation, which is given below.

$$\nabla \cdot \mathbf{D} = \rho \qquad \Rightarrow \qquad \nabla \cdot (\varepsilon \mathbf{E}) = \rho, \tag{2.1}$$

where ρ is the volumetric space charge density and ε is the permittivity of the medium. Substituting $\mathbf{E} = -\nabla U$ into the equation above, and assuming ε is constant, yields Poisson's equation for the electric potential

$$-\varepsilon\nabla^2 U = \rho \qquad \Rightarrow \qquad \nabla^2 U = -\frac{\rho}{\varepsilon}. \tag{2.2}$$

In the absence of significant free charge accumulation, the equation above reduces to the following

$$\nabla^2 U = 0. \tag{2.3}$$

As the DC voltage is applied, the electric field distribution gradually transitions from the initial capacitive regime to a resistive regime. This transition occurs as free charges begin migrating through the insulating material under the influence of the constant applied electric fields. The speed of the transition is determined by the material's conductivity and varies with the electric field and temperature. The DC charging of the system also introduces charge accumulation, with the most important case being surface charging, as described in Section 2.3.

When a lightning impulse is subsequently applied to a system already under DC pre-stress, the accumulated surface charge acts as an additional source term in the Poisson equation, distorting the transient impulse field from what would be expected in a charge-free geometry. Depending on the polarity relationship between the existing charge and the superimposed impulse, the net field may be significantly enhanced or reduced relative to either stress applied in isolation. Figure 2.3 gives the possible superimposed scenarios for a DC GIS system based on CIGRE TB842 [12].

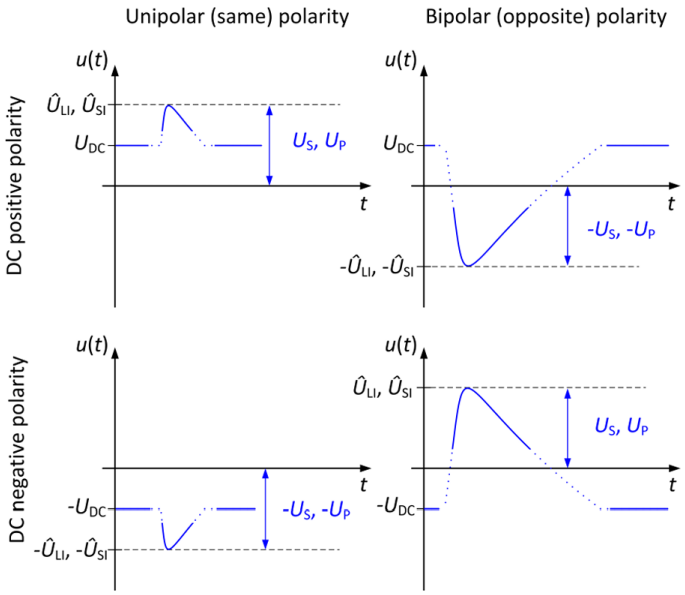


Figure 2.3: Superimposed DC/LI waveforms specified for testing according to CIGRE TB 842 [12]

This polarity-dependent field distortion is the central mechanism by which superimposed DC/LI stresses can lead to flashover at voltages well below the separately determined LI withstand levels. Reproducing this condition in a controlled laboratory environment is therefore essential for understanding the underlying failure mechanisms and developing reliable insulation design criteria for HVDC GIS. To this end, the present work describes the design and development of a reduced-scale test cell at TU Delft

that can apply superimposed DC/LI voltages to representative DC GIS geometries.

2.3. Charge Transport

Charge movement is the fundamental topic of this thesis; therefore, it is important that charge dynamics are understood. While charge transport in a GIS is a complex process with many interacting components, this section presents a simplified understanding of charge accumulation on the spacer that serves as the basis for subsequent discussion. The formula for the rate of change of surface charge density at any point on the spacer is given below.

$$\frac{\partial \sigma_{surf}}{\partial t} = \mathbf{n} \cdot J_{Bulk} - \mathbf{n} \cdot J_{Gas} - \nabla_s \cdot (J_{surface}) \tag{2.4}$$

Where J_{Gas} is the gas current density, J_{bulk} is the bulk volume conduction current density, and $J_{surface}$ is the surface conduction current density. These 3 mechanisms determine how charge accumulates, redistributes, and leaves across the spacer material over time. In real GIS spacers, understanding the values of these current components helps understand the dominant mechanism in surface charging to be addressed. Figure 2.4 shows an intuitive understanding of these current densities.

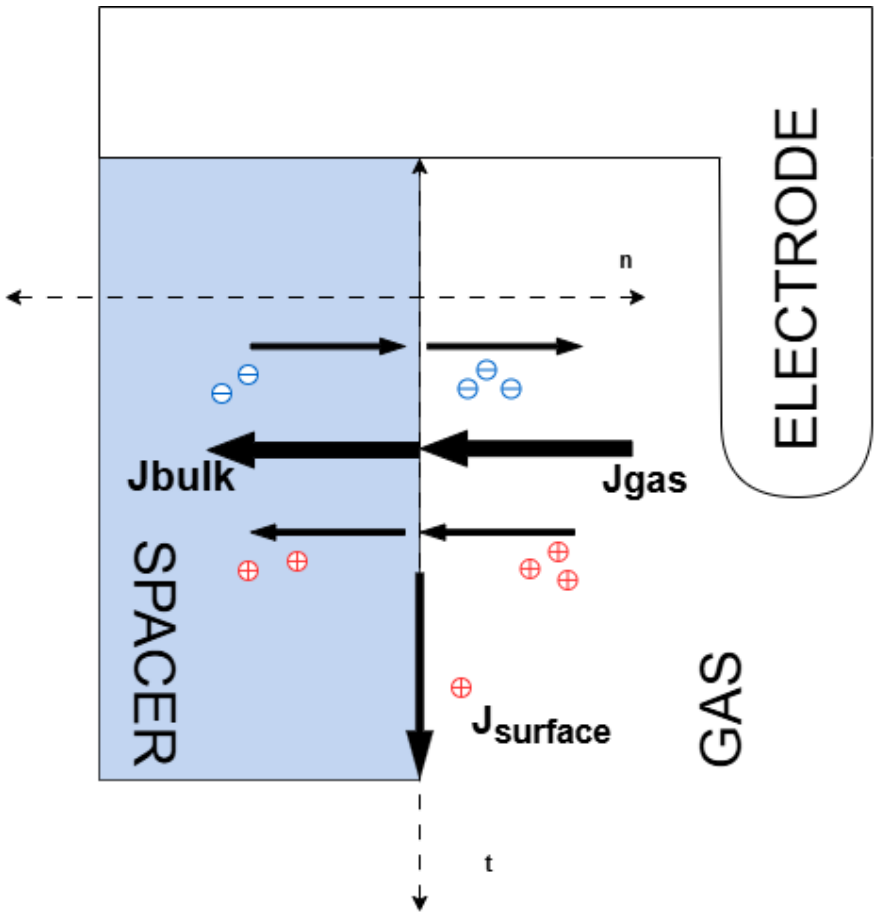


Figure 2.4: Simplified ion movement process across spacer surface given a positive applied voltage

Due to the difference in permittivity between the gas and the spacer, the electric field refracts at the interface, generally having both normal (E_n) and tangential (E_t) components. The tangential component of the electric field remains continuous across the interfaces and contributes to the surface conduction. Charge accumulation occurs on the interface through the normal current whenever $\mathbf{n} \cdot J_{Bulk} \neq \mathbf{n} \cdot J_{gas}$.

2.3.1. Bulk Conduction

Every dielectric can never be a perfect insulator and carries a small number of mobile charge carriers from impurities or lattice defects. These charge carriers then slowly drift in the applied electric field, forming a corresponding conduction current. The bound charges in every atom also shift with the field, creating electric dipoles that must reposition as the applied field changes over time. The bulk current density is therefore given as a sum of both the conduction current and displacement current following Ohm's law, as shown in Equation 2.5 below.

$$J_{Bulk} = \frac{\partial D}{\partial t} + \sigma_{bulk} E \tag{2.5}$$

In the case of DC and transients, the displacement current term dominates for fast-changing fields (impulses), and the conduction term dominates for steady-state situations (displacement approaches 0). An important note here is that the surface charge on the spacer is affected only by the component of J_{Bulk} that is normal to the spacer surface. The geometry of the electrodes and spacer therefore directly affects surface charge accumulation.

2.3.2. Surface Conduction

Due to the tangential component of the electric field on the interface, charge deposited on the spacer surface is not entirely stationary, resulting in a surface current density [21]. The resulting surface current density is given in Equation 2.6 below.

$$J_{surface} = \sigma_s \cdot E_t \tag{2.6}$$

where σ_s is the surface conductivity of the dielectric. The contribution of this lateral transport to the charge accumulation is the divergence of the surface current $\nabla_s \cdot (J_{surface})$, which shows the net charge flowing out of the surface element. The surface conduction term, therefore, acts as a redistributing mechanism for the charge deposited on the surface. An important note is that surface conduction is highly sensitive to factors such as surface conditions, contamination, and moisture, and varies with spacer material and gas interface [22].

2.3.3. Gas Conduction

Given that SF_6 under normal operating conditions is a weakly ionized gas, a small number of positive and negative ions always exist within it. This remains true for any electronegative insulating gas and is considered the primary charge driver under operational conditions. This population of ions in a gas is determined by both background ionization (cosmic rays or photoionization) and ion-ion recombination [23]. Under the influence of an electric field, the ions follow the field lines and drift towards the spacer surface, which creates a gas current density J_{gas}. The formula for the gas current can be given as in

Equation 2.8.

$$\sigma_g = e \cdot (\mu_p N_p + \mu_n N_n) \tag{2.7}$$

$$J_{\text{Gas}} = \sigma_g \cdot E = e \cdot (\mu_p N_p + \mu_n N_n) \cdot E \tag{2.8}$$

where N_p, N_n are the concentrations of ions in the gas volume of the positive and negative, and μ_+, μ_- are the ion mobilities. When there is no field, the current density is zero, and in non-uniform fields, there is a spatially varying normal component of J_{gas}. An important note is that the J_{gas} and J_{Bulk} deposit charge onto the spacer surface, whereas the surface terms merely redistribute the charges across the spacer.

2.4. Alternative Gases

SF_6 has dominated GIS usage since the 1960s due to its dielectric strength, arc-interruption performance, chemical inertness, and material compatibility. The use of SF_6, however, presents a caveat that it has a GWP of 23500, making it environmentally equivalent to about 23500 kg of CO_2 [10]. There is therefore a strong EU regulatory movement to replace gas in HV installations. The EU gas regulation aims to ban the use of SF_6 in new MV installations from January 2026 and phase out HV switchgear by the year 2035 [24].

Many current alternatives have appeared in research and practical use, such as C_4F_7N, $C_5F_{10}O$, and CF_3I [25]. The gases, while having a lower GWP than SF_6, do, however, pose a liquefaction problem. Most alternative gases, while having comparable dielectric strength to SF_6, cannot be used at pure concentrations because they have much higher boiling points. In typical GIS installations, as the pressure increases, the gases liquefy, which is hazardous for operation. The mixtures are therefore diluted with carrier gases such as CO_2, N_2, and technical air. The dilution ratio is typically about 90% or more carrier gas, which significantly weakens the dielectric strength of the mixtures. Table 2.2 shows a comparison of common alternative gases along with the GWP and dielectric strength.

Table 2.2: Environmental properties and relative dielectric strength of insulating gases compared to SF_6

Gas	GWP (100 yr)	Relative Dielectric Strength	Boiling Point (°C)
Sulphur Hexafluoride (**SF_6**)	23,900	1.00	-63.8
Fluoronitrile (**C_4-PFN**)	2,100	$\sim$2.00	-4.7
Trifluoroiodomethane (**CF_3I**)	<5	$\sim$1.20	-22.5
Fluoroketone (**$C_5F_{10}O$**)	$\sim$1	$\sim$2.00	$+26.5$
Carbon Dioxide (**CO_2**)	1	$\sim$0.40	-78.5
Nitrogen (**N_2**)	0	$\sim$0.36	-195.8
Oxygen (**O_2**)	0	$\sim$0.30	-183.0

Alternative gas mixtures are expected to see increasing use in DC GIS installations. The composition of the insulating gas and the interfacing solid strongly affects spacer flashover behavior [22], yet this effect has not been well characterized for alternative gases under composite DC/LI voltage stresses. There is therefore a need for a DC GIS representative test vessel for testing alternative gases.

3

Literature Review

This chapter reviews current developments in HVDC GIS research across spacer modifications, transient behavior, and surface flashover, with the goal of assessing research progress and identifying gaps in DC GIS and superimposed testing. The works chosen range from doctoral theses to published papers, providing insight into current HVDC GIS research.

3.1. Comparisons of AC and DC GIS

Studies comparing AC and DC GIS have primarily focused on differences in electric field distribution, insulation coordination, and testing protocols. The resistive DC field distribution, in contrast to the AC field distribution in Chapter 2, has long been modeled in both simulation and experiment for interfaces in solid materials, and charge accumulation under DC in insulating media is a widely understood phenomenon. AC GIS field modeling has likewise matured over decades in areas such as geometry optimization, material selection, and failure studies [26, 27, 28].

HVDC fields in other transmission media such as cables have also been studied for a significant time [29, 30], with Jeroense et al. [6] showing that DC fields in paper-filled HVDC cable insulation are well understood and depend on time, field, and temperature. These works emphasize the need to model the initial AC, steady-state DC, and polarity-reversal stages for comprehensive insulation design. The field and temperature dependencies of the coaxial DC geometry tested are shown in Figure 3.1.

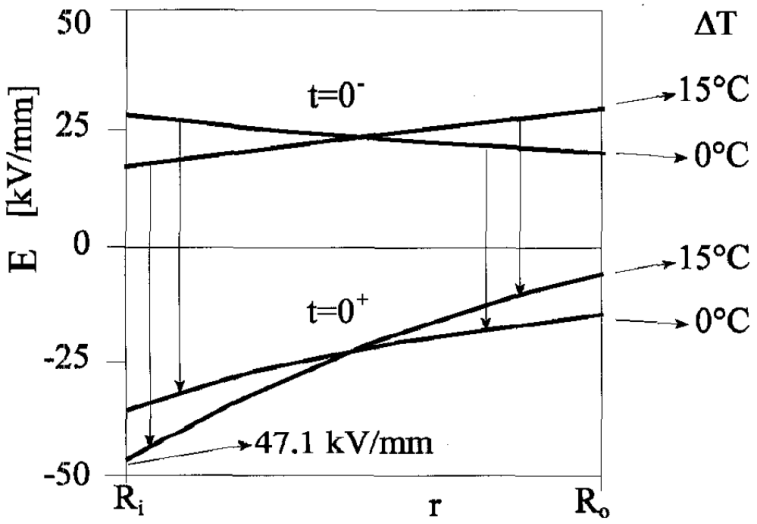


Figure 3.1: Polarity reversal from +450 kV (t = 0^-) to -450 kV (t = 0^+) in an HVDC paper-insulated cable for two different temperature gradients [6]

Early DC GIS studies by Messerer and Boeck [31] demonstrated that surface charge accumulation at spacer interfaces under DC stress leads to significant field distortion, establishing that, unlike AC operation, the time-dependent behavior of DC stress and spacer geometry is key to insulation reliability. AC spacers designed for AC GIS, therefore, cannot be used directly in HVDC GIS without modifying geometry, materials, or operational voltages.

Bo Qi et al. [32] experimentally studied the effect of charge accumulation on flashover on GIS insulators. Using a capacitive surface charge measurement system, they evaluated a GIS configuration under both AC and DC, with DC prestress voltages of 38 kV and 43 kV applied for 60 min, finding that increased surface charge consistently reduced the DC breakdown voltage by up to 23%. This further solidifies surface charge accumulation on the gas-solid interface as the fundamental difference between AC and DC GIS.

From a system-level perspective, the overview by Kosse et al. [17] represents the state of the art in UHV DC GIS. It concludes that DC GIS development up to ± 550 kV is complete in design and development, with work remaining to standardize and define tests. While DC GIS is newly entering markets, gaps such as failure data and behavior under alternative gases are still relatively unknown. Figure 3.2 shows a simulated DC GIS system in both transitional AC and DC steady-state fields.

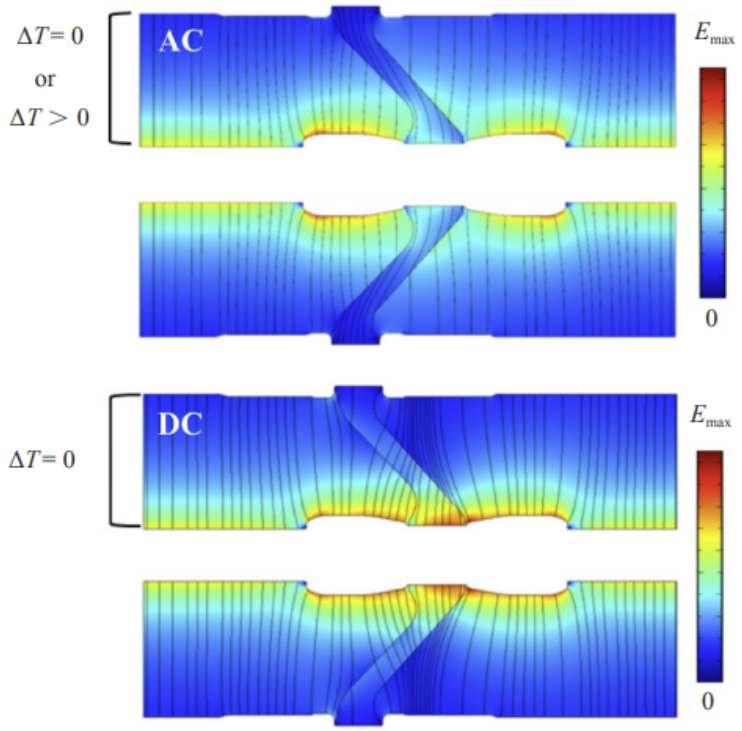


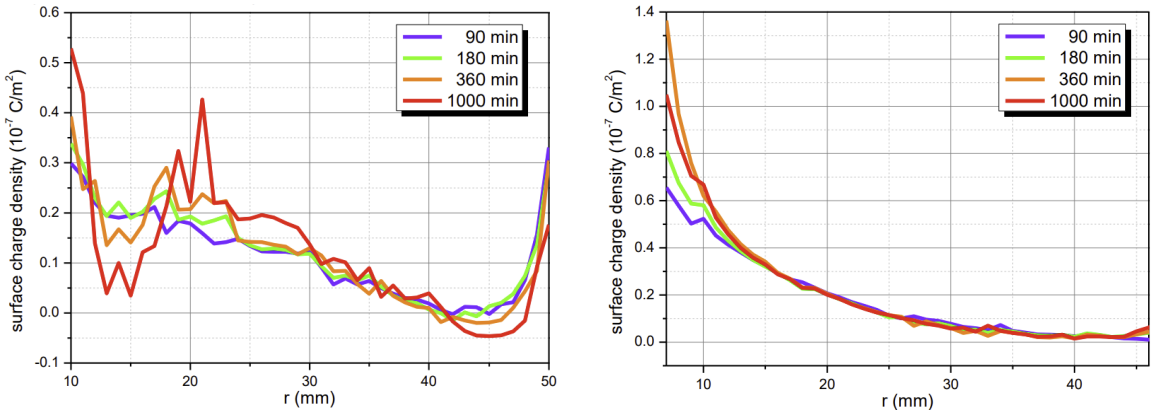
Figure 3.2: Comparison of AC transitional and DC steady state stress for a simulated DC GIS section with a basin insulator [17]

The reviewed literature indicates that although the operational principles of AC and DC GIS are the same, the shift from AC to DC introduces insulation challenges that remain poorly understood. Temperature and field dependent conductivity, surface charge accumulation, and field distortion on spacer insulation strength must all be considered in DC GIS operation.

3.2. DC GIS Spacers

Under DC stress, DC GIS spacer behavior diverges fundamentally from that in AC systems. The field distribution is governed not by material permittivity but by the system conductivities Section 2.3. Many studies show that spacer permittivity remains relatively stable, whereas electric field and temperature-dependent conductivity govern the resistive field distribution [33]. The transition time is usually set by the highest-conductivity material, which in many GIS can either be the spacer or the gas, and can range from hours to days [34].

Tschentscher et al. [35] and Zhang et al. [36] demonstrated that basin-type epoxy spacers experience a peak field at the triple junction, with the severity influenced by thermal gradients. Without temperature gradients, the field peaks near the spacer bend and the electrodes; with gradients, the charge density shifts markedly toward the HV electrode and increases in magnitude. The mid-spacer peak was attributed to microdischarges in the gas near the triple junction. Figure 3.3 shows a surface charge density measurement illustrating these temperature-gradient effects.



(a) Under Room Temperature

(b) Under temperature gradient (40°C)

Figure 3.3: Surface charge density across the radius of a spacer for different prestress times and under a temperature gradient [36]

Xu et al. [37] elaborated on this by testing the effects of temperature and gas pressure on charge accumulation dynamics. The relative dominance of the gas versus solid side depended on the insulator's volume resistivity, with a low resistivity, gas-side transport dominates, whereas high resistivity, the solid bulk governs. The simulated radial temperature gradient again increases surface charge density. Their detailed gas model, including heat transfer, shows scattered charge speckles alongside uniform charging from insulator or conductor defects [38]. Figure 3.4 shows surface charge buildup across a real-sized insulator under different pressures.

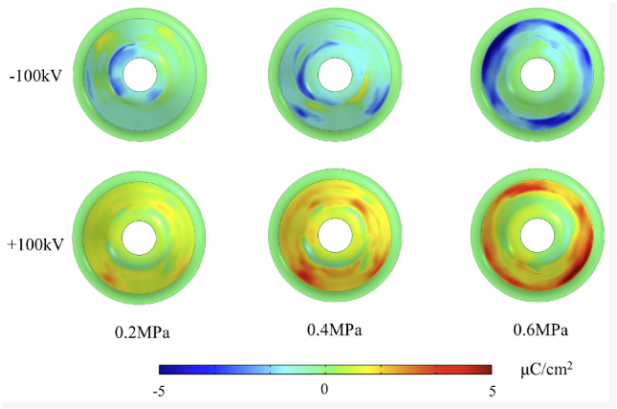


Figure 3.4: Impact of pressure on surface charge accumulation for a real-size insulator under ± 100 kV DC for 3 gas pressures [37]

The choice of spacer material and filler content significantly affects DC electrical behavior. A common research topic is conductive field-grading materials (FGM), epoxy filled with different fillers to reduce field concentration in high-stress areas [39, 40]. Liang et al. [41] reviewed the influence of nanofillers on bulk conductivity and space charge suppression, and Yao et al. [42] showed that coatings can effectively reduce triple-junction stress. A coating gradient thickest near the triple junction allowed up to a 62.7% decrease in maximum E-field strength, though the non-uniform conductivity also increases the flashover voltage, as shown for a σ-SFGM coated spacer in Figure 3.5. The correct coating and thickness can therefore reduce field enhancement and flashover probability.

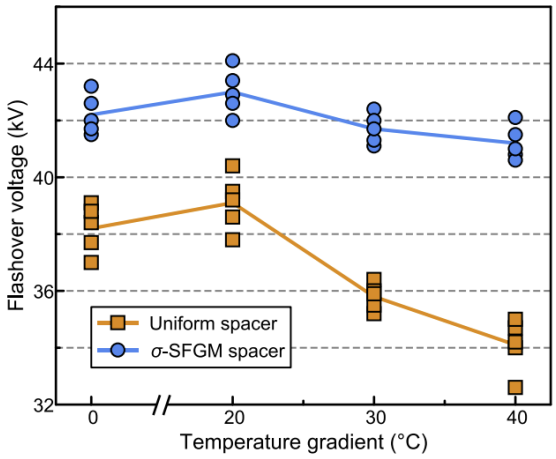


Figure 3.5: Flashover voltages for a coated and $\sigma - SFGM$ coated spacer under different temperature gradients [42]

Spacer geometry has also been a major research topic, including optimizing creepage distance, incline angle, and thickness, all of which have been shown to reduce triple-junction field enhancement. An ideal spacer shape under DC stress minimizes surface charge accumulation and provides sufficient creepage to prevent spacer flashover [15, 41]. Juni et al. [43] tested space charge accumulation on two common spacer geometries, finding that geometry strongly controls the location of surface charge under DC stress: disc-type spacers give more uniform field distributions and faster charge relaxation, whereas basin-type spacers have areas promoting localized ion deposition, slower dissipation, and increased flashover risk. Figure 3.6 shows the field distribution across both geometries over the transitional AC to DC period.

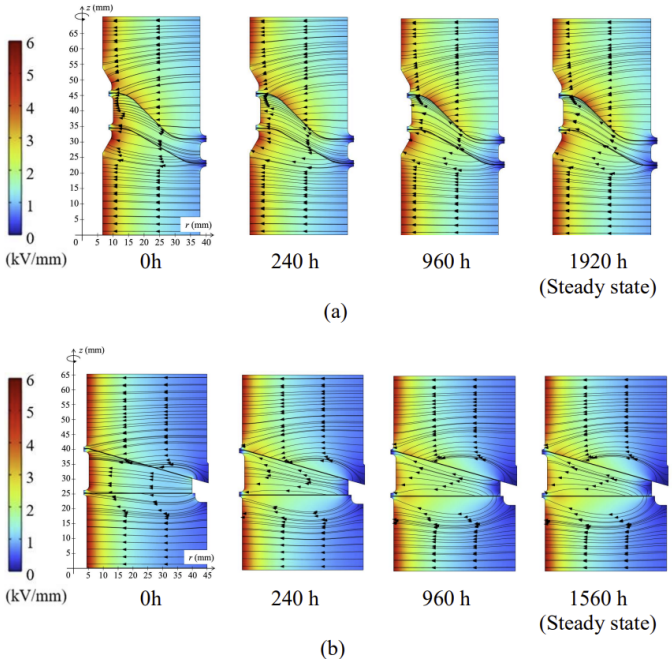


Figure 3.6: Electric field distribution across basin and disc-shaped spacer under - 60 kV applied DC for a) basin type and b) disk type [43]

The reviewed literature shows that spacer behavior under DC stress is governed by material conductivities, geometry, and temperature gradients. Unoptimized spacers pose a higher risk of field distortion and failure, and surface charge accumulation is felt most strongly when the insulation is stressed, such as during fast-front overvoltages or polarity reversals. These findings are critical for understanding how DC spacers, and thus representative geometries, react to transient voltages.

3.3. Transient Behaviors

The transient behavior of DC GIS under polarity reversal, superimposed voltages, and long-term DC stress has been a central research focus, as these scenarios impose rapid stresses on the insulation. Many simulations show how charge buildup distorts local fields and increases the susceptibility to flashover during superimposed conditions [20]. Polarity reversal and superimposed stresses often cause the greatest stress in DC GIS, and current research aims to better explain these mechanisms, improve simulation models, and design systems to better withstand these conditions.

Long-term DC application imposes additional spacer stress compared with AC. Standardization works such as CIGRE TB 842 and TB 957 [12, 44] show that prolonged DC stress leads to progressive space charge accumulation, surface charge migration, and accelerated spacer aging. Sato et al. [45] investigated corona discharge on epoxy spacer surfaces at different voltages, finding that for long-term applied voltages, the charge-density decay was less than 1% per hour. This implies that field distortions from surface charge persist and continue to affect insulation strength long after DC operation ceases.

Nakanishi et al. [46] measured surface charge accumulation on conical epoxy spacers in SF_6. Under +100 kV DC, the surface charge saturated after five hours and remained for 15 hours after the source was disconnected, while negative polarity deposited charge on different areas at higher magnitude. Charge accumulated under DC prestress therefore has long-lasting effects on the field distribution that must be considered in HVDC GIS operation. Toigo et al. [20] developed a simulation method for superimposed DC/LI voltages, considering both same- and opposite-polarity superimposition. Figure 3.7 shows the field in 5 bar SF_6 for the different waveforms.

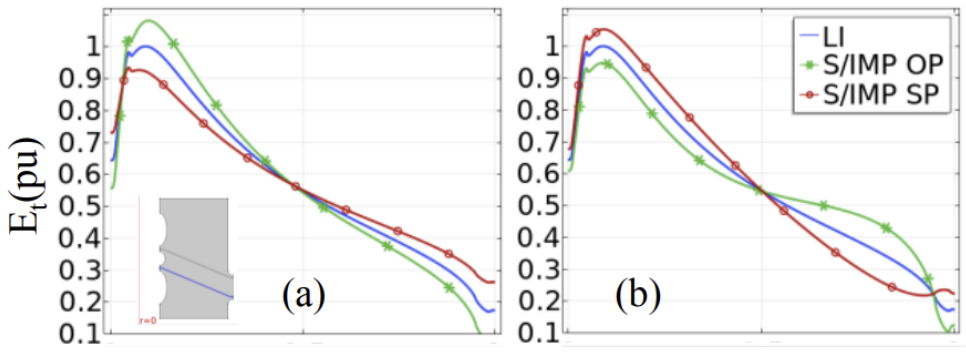


Figure 3.7: Total simulated electric field distribution along the spacer for superimposed voltages for Zero Load (a) and High Load (b) [20]

Early works such as Okabe et al. [47] reviewed flashover for 2 spacer models under superimposed DC and LI. The work showed that flashovers occurring from different pre-stress times for positive su-

perposition remained around the flashover of pure LI. This was explained as the charge field of the accumulated surface charge on the surface of the insulator opposed the polarity of the LI and resulted in minimal further weakening. The opposite superposition of voltages, however, led to easier streamer formations and reduced the flashover voltage for longer prestress times. Ma Jingtang et al. [48] corroborate this using a more representative GIL-based setup under SF_6. For the non-contaminated insulators, the flashover voltage of the superimposed remains the same as that of LI alone. Given contamination, the DC flashover voltages decrease. The deterioration of insulation through charge accumulation, free metal particles, and consideration of superimposed voltages are of great importance for DC GIS design. Figure 3.8 shows the flashover characteristics of the contaminated insulator under different DC/LI combinations.

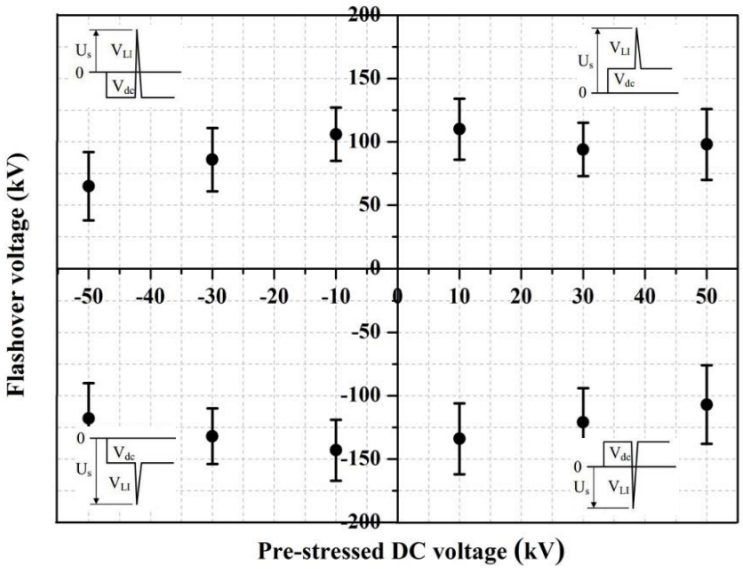


Figure 3.8: Flashover voltages of contaminated insulator under superimposed DC/LI voltages [48]

Recent work by Jian Wang et al. [49] further progressed by testing alternative SF_6 mixtures to perform surface charge measurements. The results show that gas type, such as CO_2, varies in ionization coefficient, electron attachment rate, and mobility, leading to different streamer development. The research also further tested for the inclusion of particles on the spacer surface and found local charge accumulation and field enhancements. The relation between existing surface conditions and superimposed stresses is also of great importance to operational HVDC GIS. Figure 3.9 shows the effect of particles and alternative gases on the flashover voltage for a GIL model.

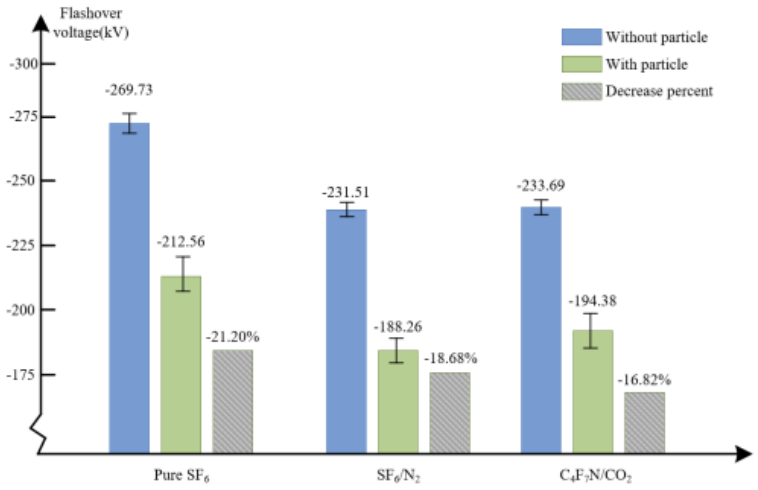


Figure 3.9: Comparison of flashover voltages under superimposed DC/-LI for 3 alternative gasses and with a particle [49]

Insights from superimposed voltage studies over recent years show how DC prestress voltage, polarity, gas type, and contamination affect an insulator's ability to withstand superimposed LI. Superimposed DC and LI transients are among the worst-case conditions for DC GIS and require careful consideration in testing. This section therefore serves as a foundation for the central research question and a baseline for the dimensioning and testing work in this thesis.

3.4. Surface Flashover

Surface flashover in GIS systems occurs when breakdown streamers propagate across the insulating surface rather than through the gas gap, and it is one of the most common failure modes in GIS systems [50]. Understanding the factors governing flashover inception and propagation is essential for reliable HVDC GIS design [22, 51]. This section reviews discharge behavior on gas-solid insulator surfaces to identify which aspects are most critical to designing a reduced-scale test system.

Bulk gas breakdown provides the baseline from which surface flashover deviates. Beroual et al. [52] established the breakdown characteristics of CO_2, N_2, and SF_6 mixtures under AC, DC, and impulse waveforms, showing that while CO_2 and N_2 exceed air in dielectric strength, both remain weaker than SF_6. Kumar et al. [53] characterized CO_2 and O_2 mixtures across waveform types, finding CO_2-based mixtures yield roughly a 6% increase in breakdown strength over air, and that the role of the first electron becomes less significant under long-duration DC. These bulk properties define an upper bound of dielectric performance against which surface flashover can be assessed.

Surface flashover adds complexity beyond bulk breakdown, as the solid-gas interface creates surfaces where tangential field components drive charge accumulation and migration. Li et al.[22] concluded that the resulting flashover voltage is consequently lower than the bulk breakdown threshold, typically around 70% at 0.1 MPa of SF_6. The authors further compared theoretical flashover models across vacuum and compressed-gas environments, identifying material surface conductivity as a key parameter, with PTFE and nylon showing the greatest resistance to charge deposition due to their low surface conductivities. Figure 3.10 shows surface and bulk breakdown voltages versus gas pressure and species.

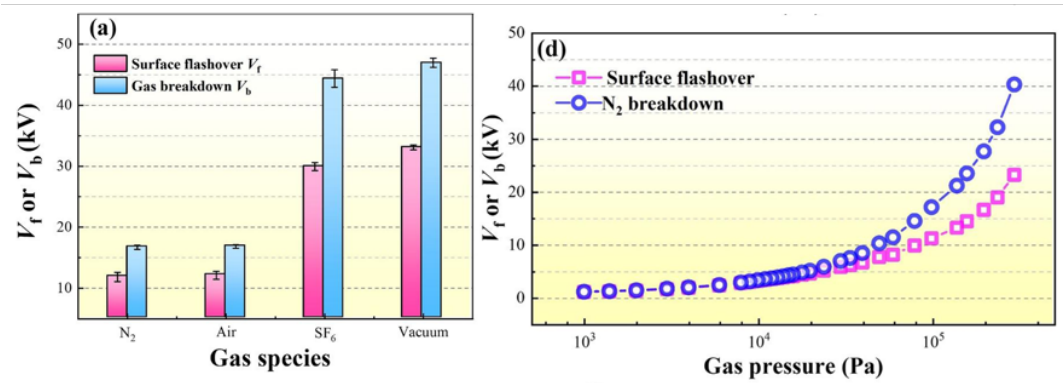


Figure 3.10: Surface and bulk breakdown voltages for a gap size of 4.71mm [22]

Wu et al. [51] further demonstrated that interface charge accumulation directly drives surface flashover, splitting the behavior into tangential-dominated and hybrid regimes and evaluating existing models. For tangential-dominated mechanisms, heteropolar charges most strongly reduce DC flashover voltages, while the more representative normal-tangential mixed mechanisms found in GIS, which depend more on material characteristics and gas-volume ionization, have a greater effect through the normal component. The paper highlights that surface flashover is not fully understood and needs further research.

Liu et al. [50] established knowledge on the morphology of post-flashover traces and discharge positions for impulse voltages in full scale basin insulators. There are 8 principal discharge-initiation paths identified, including shielding-originated (SSE), HV triple-junction-initiated (HVT), ground triple-junction-initiated, and particle-initiated (SIN), with some paths occurring more frequently. In clean GIS, the most likely paths are pure gas-gap breakdown, triple-junction-initiated spacer tracing breakdown, and shielding-initiated breakdown following the spacer. The primary focus is the frequency and risk of different paths, with SSE-based path 1 being the dominant failure mechanism for non-contaminated spacers. Figure 3.11 shows the possible flashover paths in a GIS.

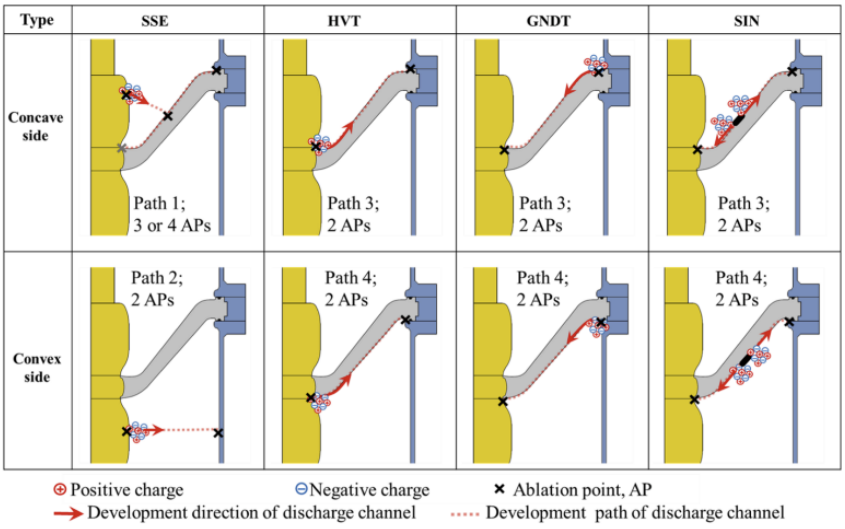


Figure 3.11: Possible flashover paths in a basin insulator [50]

Surface flashover depends on many factors, including insulator material properties, gas type, and contamination. While many models exist, there is no holistic framework, and surface flashover in DC GIS under superimposed stresses has not been extensively analyzed. The knowledge in this section is therefore used in the following chapters to design and dimension a reduced-scale representative DC GIS system.

Part II Design

4

Electrode Design

While a real DC GIS system would be preferable, this is not feasible due to the unavailability of gas-insulated test chambers and HVDC bushings at the TU Delft HV laboratory. The reduced-scale design must therefore reproduce the quasi-homogeneous field distributions found in DC GIS systems while appropriately scaling the electric field stresses. This representative system is defined not by a single parameter but by a combination of numerical requirements and design criteria, together verified by FEM simulations in COMSOL Multiphysics™. This chapter describes the determination of field uniformity, the definition of design parameters, the coupled COMSOL modeling process, and validation through COMSOL simulations.

4.1. Field Utilization Dimensioning

The first objective is to characterize the electric field distribution in real DC GIS systems so that the reduced-scale geometry can adequately replicate it. In HVDC GIS, the simplest approximation is two radial concentric conductors with a quasi-homogeneous field. The field utilization factor, defined as the ratio of average to maximum field across a spacer, quantifies this distribution and is given by Equation 4.1.

$$\eta = \frac{E_{avg}}{E_{max}} \tag{4.1}$$

Given the lower testing voltages of the reduced-scale system, the electrode dimensions and materials must be selected to achieve the target η_{DC}, as discussed in section 4.3. Initial dimensioning was obtained through two methods and synthesized into a baseline for all further design: AC GIS coaxial approximations and the extraction of field utilization factors from published simulation studies.

4.1.1. AC GIS Approximation

As a starting point, the dimensions of a 550 kV ELK 3 AC GIS from Hitachi are used as a UHV AC GIS reference, based on the thermal analysis by Stosur et al. [54]. The ELK 3 has inner and outer conductor diameters of 160 mm and 820 mm and a 10 mm enclosure wall. GIS dimensions vary across manufacturers and rated voltages, so the field utilization factor differs between systems; this is not a concern, since the representative system aims to mirror the quasi-uniform field of real DC GIS rather than model any particular commercial unit. Ignoring the effect of the spacer, the field can be approximated as that of a concentric coaxial conductor:

$$E(r) = \frac{V}{r \ln\left(\frac{R}{r}\right)},$$

With radii $\frac{820-160}{2} = 330$ mm, the maximum field at the conductor is $E_{max} = 4.20$ kV/mm. The average field follows from integrating over the distance:

$$E_{avg} = \frac{1}{R-r} \int_r^R \frac{V}{x \ln\left(\frac{R}{r}\right)} \, dx$$

giving $E_{avg} = 1.67$ kV/mm and $\eta_{AC} \approx 0.396$. Many GIL systems adopt an optimal ratio near $\ln(\frac{R}{r}) = 1$ and therefore fall within a narrow range of field utilization factors [55]. This simplified calculation neglects fringe effects from the curved spacer and the shielding typically present and the spacer, but still yields a quasi-homogeneous field above 0.2, which would cause corona inception before breakdown [56]. It is therefore treated as a first-order estimate, providing a practical target for the reduced-scale design rather than an exact figure.

4.1.2. Extraction of Fields from Research

The second approach uses electric field parameters extracted from existing DC GIS simulation studies. Although direct comparison is complicated by differences in geometry, material properties, and temperature dependencies, averaging the reported maximum fields and utilization ratios still yields a meaningful reference range for η_{DC}. From the 12 studies considered, compiled in section B.1, the DC steady-state E_{max} is estimated at roughly 3-5 kV/mm and η_{DC} at approximately 0.450, both consistent with the DC GIS spacer design literature discussed in section 4.2. Together, these bounds define the quasi-homogeneous field distribution that the reduced-scale geometry must replicate. To illustrate a real DC GIS field distribution, the system was simulated based on the work of Xiaolong et al. [21], with more detailed field and charge-accumulation simulations in Appendix C. Figure 4.1 presents the simulated field streamlines for a basin-type spacer at steady state under +200 kV DC.

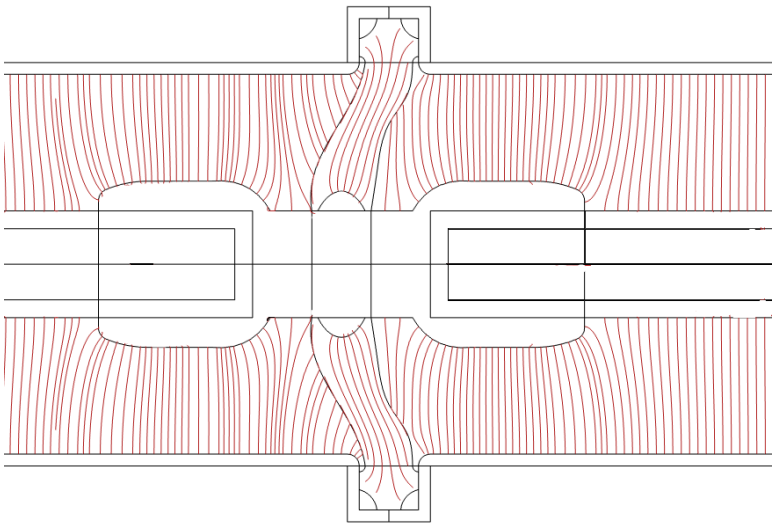


Figure 4.1: Simulation of the electric field for a basin spacer from [21] under a +200 kV DC voltage

Given the relative newness of DC GIS technology and the limited availability of commercial spacer dimensions in the open literature, a best-case approximation of η_{DC} is the one that can most reasonably be achieved. A target value of 0.4 was selected, at the lower end of the estimated range, and carried forward into the electrode design. This value does not replicate any single commercial DC GIS model, but captures the quasi-homogeneous field behavior characteristic of these systems more broadly.

4.2. Design Parameters

The design of an HVDC GIS spacer involves numerous considerations, with the three main aspects reported in the literature being the modification of upper and lower spacer profiles for non-symmetric geometries, the analysis of different spacer geometries, and the effect of key numerical requirements [15]. Electric field analyses typically focus on field components at nominal DC voltages, surface charge accumulation, and tangential fields under DC/LI-superimposed voltages. The design can therefore be separated into numerical requirements and design criteria, both of which allow the reduced-scale geometry to appropriately stress the insulation.

4.2.1. Numerical Requirements

DC GIS can be defined by numerical requirements specifying electric fields, surface charges, or other parameters proposed in the literature [15, 34, 42, 57]. Those considered in this work are listed below, with the most critical in bold.

1. Geometry of the insulator
2. Material of the insulator
3. **Maximum spacer tangential field strength AC operation** $E_{t_{AC}}$[57]
4. **Maximum spacer normal field strength AC operation** $E_{n_{AC}}$[57]

5. Maximum conductor field under DC operation E_{cond}
6. Maximum spacer gradient of tangential field ∇E_t [34]
7. **Maximum spacer tangential field strength DC/LI superimposed** $E_{t_{SIMP}}$ [15]
8. **Maximum spacer charge accumulation** [57]
9. **Field homogeneity DC** η_{DC}

The bold parameters can be used to dimension a DC GIS spacer, combining theoretical simulations [15, 34, 57] and operational testing [42] to determine acceptable values. Volpov et al. [57] provided design requirements for the normal and tangential spacer-surface fields, given in Equation 4.2.

$$E_n(0,l)_{\max} < EN \tag{4.2}$$

$$E_t(0,l)_{\max} < ET \tag{4.3}$$

Where l is the length of the spacer, and EN and ET are both 3.5 kV/mm in the capacitive transition regime. The same work set the target surface charge accumulation at ≈10–20 μC/m^2, based on simulations that do not account for ion drift. Spacer-optimization studies by Lorenzi et al. [34] and Hongyang et al. [58] reinforce these requirements. Li et al. [15] additionally consider DC/LI-superimposed fields, since GIS insulation is typically dimensioned for overvoltages such as lightning or switching impulses, with a maximum field of 11.1 kV/mm, which is close to the 12 kV/mm reported for a 0.7 MPa SF_6/N_2 mixture by Hongyang et al. [58].

4.2.2. Design Criteria

Beyond the numerical requirements, a set of qualitative design criteria must be met to replicate the field-management techniques used in DC GIS. These are applied to the geometry with the goal of mitigating charge accumulation and localized triple-junction field enhancements.

1. Reduce maximum fields at the triple junction [8, 59]
2. Minimize spacer tangential field on spacer relative to electrode [57]
3. Reduce the normal field component along the spacer surface to lower charge accumulation [57]

Each of the design criteria above addresses charge accumulation and local triple junction-based field enhancements, which are inherent failure mechanisms in DC GIS. The field at the triple junction must therefore be kept sufficiently low to prevent any possible discharges [59]. The field along the gas-solid interface of the spacer is also weaker than the gas bulk [22], and therefore it is of importance that the tangential field E_t across the spacer is kept less than at the electrodes. Volpov [57] also quantifies these in equations 6, 10, and 11. The final criterion follows from the fact that, as mentioned previously, charge accumulation on the spacer is determined by the normal component of the electric field E_n incident on the interface. These numerical requirements and design criteria are then further used to create a reduced test geometry that mimics an HVDC GIS disc spacer.

4.2.3. Scaling

The values above could not be used directly in a reduced-scale setup, as they would immediately break down the insulation; the relevant fields were therefore scaled to suit the dry-air setup up to 3 bar. For all electronegative SF_6-substitute gases, the streamer/inception criterion applies, with an electron avalanche starting at the cathode and growing until it crosses the gap, as expressed in Equation 4.4.

$$\int_0^{x_c} [\alpha(x) - \eta(x)]\, dx = K \tag{4.4}$$

where α is the first Townsend ionization coefficient, η the attachment coefficient, x_c the critical avalanche length, and K a constant representing the number of free electrons (commonly $K \approx \ln(10^6)$ to $\ln(10^8) \approx 13.8$ to 18.4) [60]. Since both α and η depend on the reduced field E/P, the relevant quantity considered is $(\alpha - \eta)$. When it is zero, ionization and attachment balance, and any positive value can lead to electron multiplication and breakdown. The critical reduced field $(\frac{E}{P})_{crit}$ is thus the field at which $(\alpha - \eta) = 0$ for any given gas. Figure 4.2 shows $(\alpha - \eta)$ for different alternative gases computed in BOLSIG+ by Lujia et al. [55].

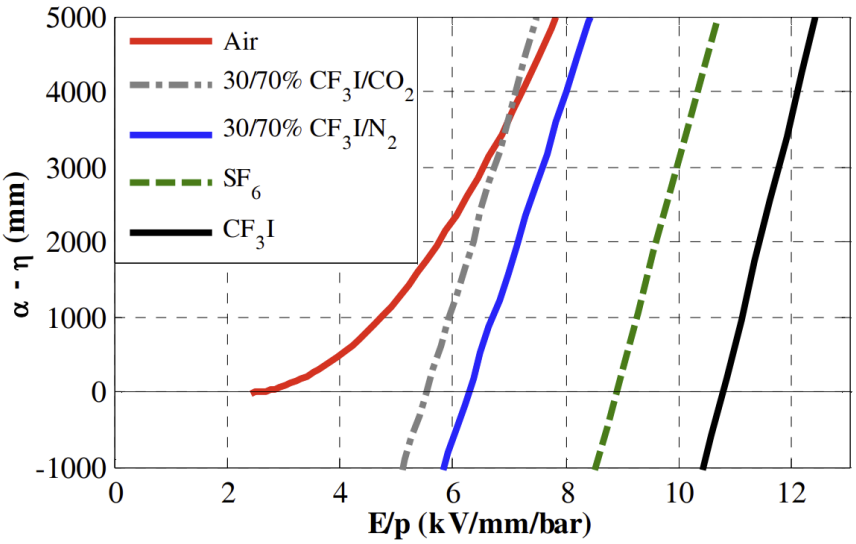


Figure 4.2: Effective ionization coefficient $(\alpha - \eta)$ as a function of reduced field E/P for many different gasses [55]

Experimentally, dry air (80% N_2, 20% O_2) at 1 bar has $(\frac{E}{P})_{crit} \approx$ 110–120 Td (1 Td = $10^{-21}\ V \cdot m^2$), while SF_6 is roughly 360 Td [25]. The approximate difference in dielectric strength is commonly taken as 2.5 -3 times that of dry air and therefore falls within the expected range. A κ factor is further defined, and the fields are scaled as below.

$$\kappa = \frac{(E/P)_{crit,\,air}}{(E/P)_{crit,\,SF_6}} = \frac{120\ \text{Td}}{360\ \text{Td}} \approx \frac{1}{3} \tag{4.5}$$

$$E_{air}(P) = \kappa \cdot \frac{E_{research}}{P_{research}} \cdot P \tag{4.6}$$

For 3.5 kV/mm at $P_{research}$=4 bar, the $P = 1$ bar field equivalent is 0.292 kV/mm. Table 4.1 shows the research-compiled and scaled targets for the representative system over the pressure range.

Table 4.1: Parameters: Research Values and Scaled-Down Values for 1, 2, and 3 bar Technical Air [15]

Design Parameters	SF_6, 4 bar	1 bar air	2 bar air	3 bar air
Max tangential field AC $E_{t_{AC}}$	3.5 kV/mm	0.292 kV/mm	0.583 kV/mm	0.875 kV/mm
Max normal field AC $E_{n_{AC}}$	3.5 kV/mm	0.292 kV/mm	0.583 kV/mm	0.875 kV/mm
Max superimposed field $E_{DC/LI}$	12 kV/mm	1 kV/mm	2 kV/mm	3 kV/mm
Max charge accumulation		10–20 $\mu C/m^2$		
Field Homogeneity DC η_{DC}		≈ 0.4		

Note that the DC operational spacer field is 3.5 kV/mm at 4 bar SF_6, well below the gases dielectric capability. The conductor fields are often much higher than the spacer fields, and no comprehensive numerical requirements for conductor fields in DC GIS or GIL were found in the literature.

The charge-accumulation limit from Volpov et al. [57] is also adopted as an approximate bound on the expected surface charge, as this limit was derived without an ion-drift model accounting for gas conduction, so the DC GIS literature often reports higher surface-charge values than it suggests. As the goal of the test system is, nonetheless, to explicitly match the fields of a DC GIS disc spacer, this approximate limit provides a useful reference point for the charge expected at the gas-solid interface.

Given these numerical requirements, a representative electrode system can be designed. The design and field validation are performed in COMSOL, as shown in Section C.1. Many preliminary geometries were considered and discarded because their fields did not match the target DC GIS disc spacer, as shown in Figure 4.4. A total of three designs were considered, including a modified parallel-plate and a pinch-plate geometry, with justifications in Appendix C.

4.3. Finalized Electrode Geometry

The modified bowl plate geometry accurately represents GIS geometry and has been used in many similar GIS simplifications, including studies by Okabe et al. [47] and Rodrigo et al. [61] . Figure 4.3 shows the simulated bowl plate geometry in COMSOL, along with relevant optimization parameters.

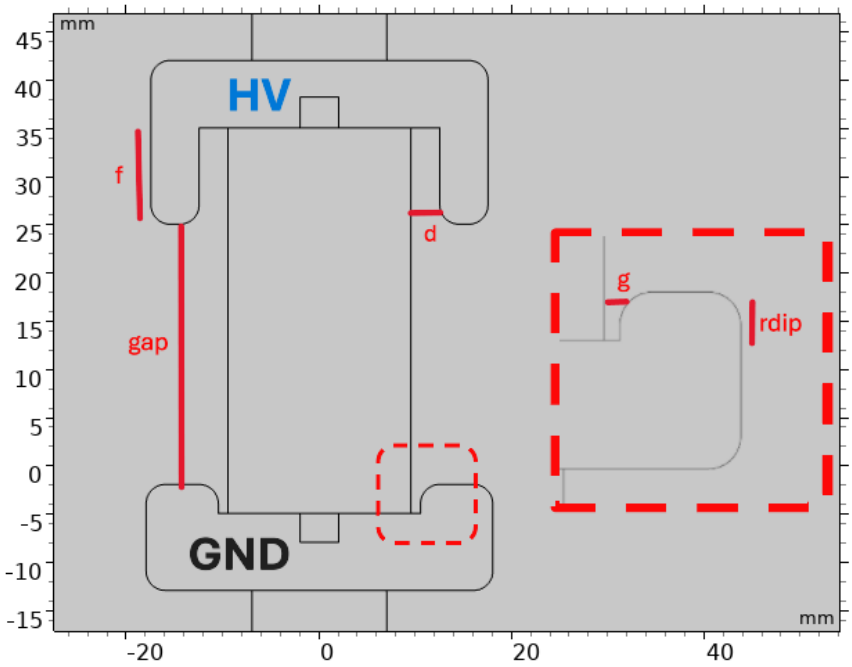


Figure 4.3: COMSOL model of the finalized electrode geometry with the given optimization parameters

The design accounts for the shielding and flange attachments found in real HVDC GIS systems, which directly address the requirement to reduce triple-junction fields at the cost of higher normal-field components on the spacer surface [59]. The shielding is separated from the spacer both to reduce the electric field on the spacer surface and to reduce the normal component of charge into the spacer. The flange divot at the bottom reduces the voltage at the ground triple junction and lowers the likelihood of triple-junction discharge initiation.

The design is rotationally symmetric about x = 0 and models the electric-field profile of disc spacers. Non-symmetrical geometries such as conical and basin spacers have a concave or convex side and are also frequent in DC GIS literature [62], but are not considered here, as they add the complexity of modeling two distinct electric-field and surface-charge profiles. The geometry includes insulating divots embedded in the electrode to allow mechanical mounting and alignment of the spacer. Since this insulating material is recessed within the electrode, its field effects, with proper mounting, are negligible.

4.3.1. Shape Optimization

The starting-point electrode shape, shown in Figure F.1, was taken as a baseline, and a non-mathematical optimization method was used to match the field homogeneity and field profile to a disc spacer. The parameters chosen were the gas gap **(gap)**, shield height **(f)**, divot height **(rdip)**, shield separation **(d)**, and divot separation **(g)**, as seen in Figure 4.3. Each was set to an initial value and swept over a given range using the COMSOL parametric sweep function. The field distribution was then verified against the requirements above, and where the field enhancement factor fell within 0.1 of the target η_{DC}, the configuration was noted. Other configurations were tested similarly, and the closest was chosen. Table 4.2 shows the parameter optimization results.

Table 4.2: Optimization parameters and their variation ranges

Geometrical parameter	Initial value [mm]	Variation range [mm]	Chosen value [mm]
Shielding height (f)	0	0-7	7
Shielding separation (d)	0	0-3	3
Gap distance (gap)	10	10-50	28
Divot height (rdip)	0	0-3	2
Divot separation (g)	0	0-1	0.5

Before assessing the numerical requirements, it was important to verify that the field profile of the optimized geometry closely matches that of the target disc insulator. The field components are therefore compared with those of a simulated 126 kV disc spacer reported in Wu et al. [51]. Figure 4.4 shows the comparison of the p.u. normal and tangential field components under DC for the optimized reduced-scale setup and the 126 kV disc spacer in case 3.

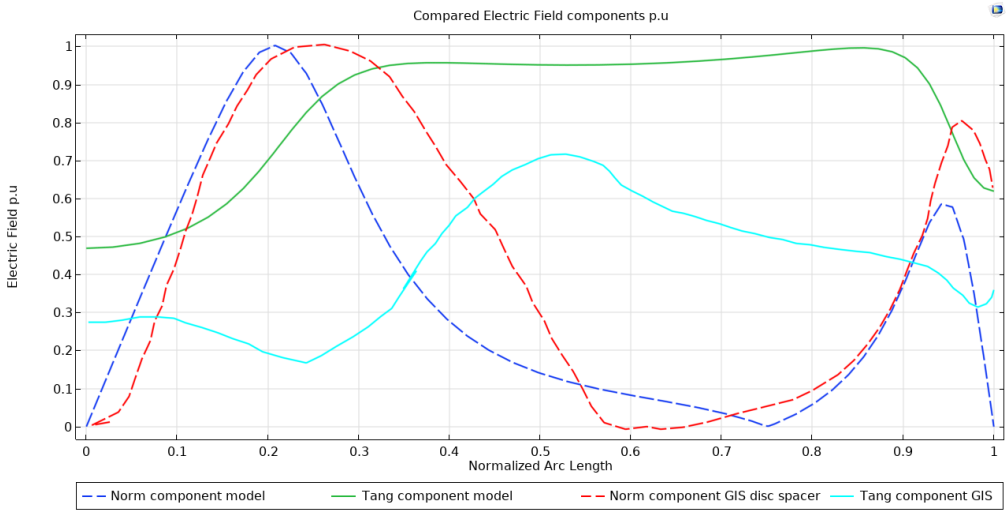


Figure 4.4: Field profile of case 1 test setup compared to a simulated DC GIS system with a modified disc spacer [51]

The field profiles of the test geometry and the disc spacer simulations [51] generally agree in shape, with only minor differences. The normal field component in the disc spacer extends further and peaks higher near the ground electrode, while the tangential components share the same shape but reach a higher magnitude in the reduced-scale configuration. These tangential differences can be attributed to the non-perpendicular spacer shape used in that study and the choice of materials in Wu's simulations. Given these constraints, the design can be considered representative of the electric field profile of disc spacers in DC GIS systems, with a field utilization factor of 0.41 and relevant DC GIS features, such as HV shielding and bottom flanges, taken into account.

4.4. Field Simulations

To verify the electrode configuration, the spacer fields must be considered, and equivalent voltages must be chosen to meet the design requirements in Section 4.2. The following section addresses the DC steady-state simulation, DC/LI superimposed voltages, and charge accumulation for the test electrode configuration.

4.4.1. DC simulations

Before any simulations, a timescale must be defined to reach the DC steady state. There are many methods for determining the time scale to DC steady state, including an approximation from Lorenzi et al. [34], an improved simulation-based calculation from Vu et al. [63], and a worst-case estimate from CIGRE TB 842 [12]. For the purpose of defining a simulation timescale, the improved model from Lorenzi et al. [34] is used and can be given as Equation 4.7 below

$$\tau = \frac{\varepsilon_0 \left(\varepsilon_{gas} + \varepsilon_v\right)}{\sigma_{gas} + \sigma_v + \frac{\sigma_s}{R_0}} \tag{4.7}$$

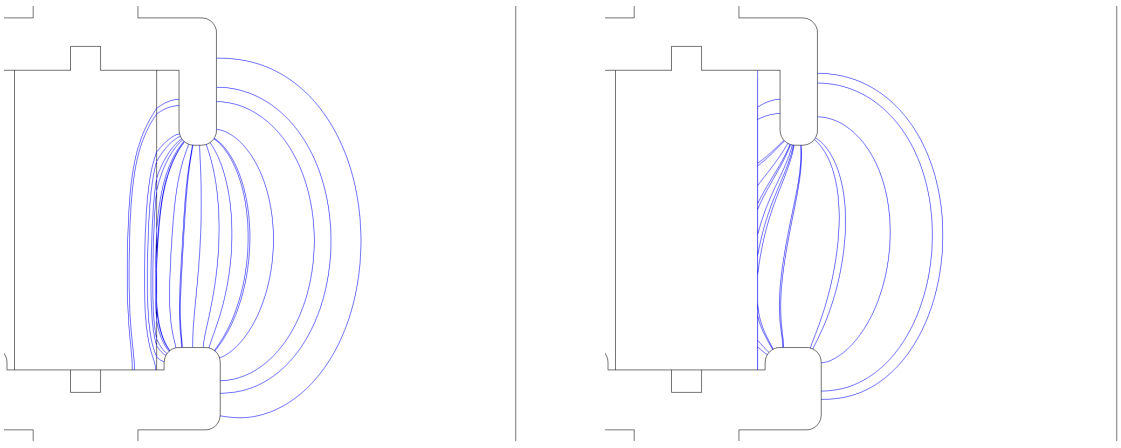
$$t90\% = 2.3\tau \tag{4.8}$$

In this work, the surface term is ignored, and the gas permittivity and conductivity are given as 1 and $\approx 3.59 \times 10^{-20}$ [S/m] from Section 8.2. The volume conductivities of extruded Nylon and PTFE are given in Table 4.3 and are chosen as they span the same range as epoxy resin, as seen in Figure C.8.

Table 4.3: Cases studied for spacer material

Case	Material	ϵ_r / σ (S/m)	Calculated τ(s)	$t_{90\%}$(s)
Ref	Epoxy Resin	5 / Equation C.1	2.9×10^5 s	6.7×10^5 s
1	Nylon	3.5 / 3.62×10^{-14}	1.1×10^3 s	2.5×10^3 s
2	PTFE	2.1 / 1.11×10^{-16}	2.51×10^5 s	5.78×10^5 s

It must be noted that, due to a lack of time, measurements of the substitute materials volume conductivity were not possible; the values were assumed from an online material database with comparable characteristics. The plots for the capacitive and resistive field streamlines for PTFE are presented in Figure 4.5 below.

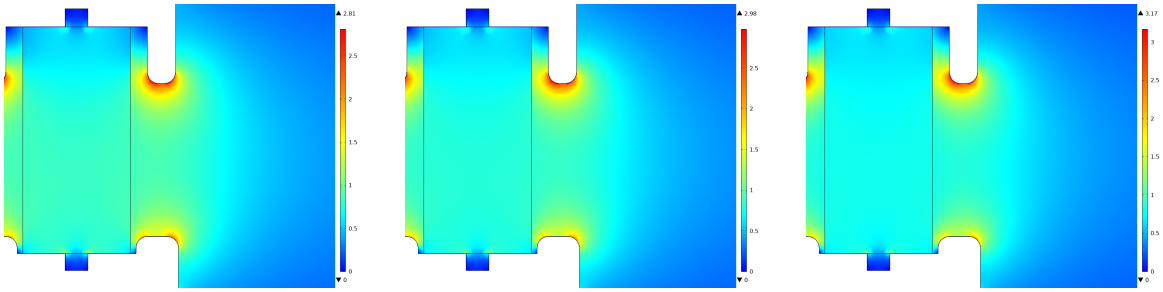


(a) Capacitive **(b)** Resistive

Figure 4.5: Electric field streamlines across transition for PTFE given +30 kV DC

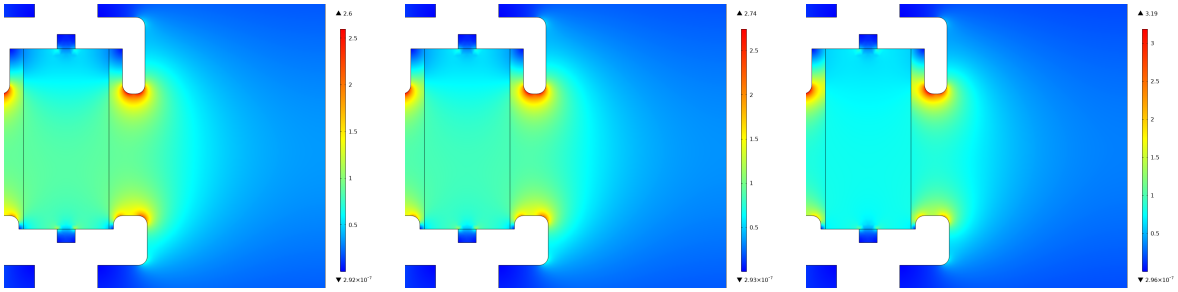
The streamlines of the fields vary with the choice of material and indicate the magnitude of the electrical field lines. It is observed that due to the charge accumulation, as explained in Section 4.4.3, the streamlines vary in shape. Figure 4.7 below further shows the surface-field transition from capacitive

to resistive in both Nylon and PTFE.



(a) Capacitive field distribution **(b)** Transitional field distribution **(c)** Resistive field distribution

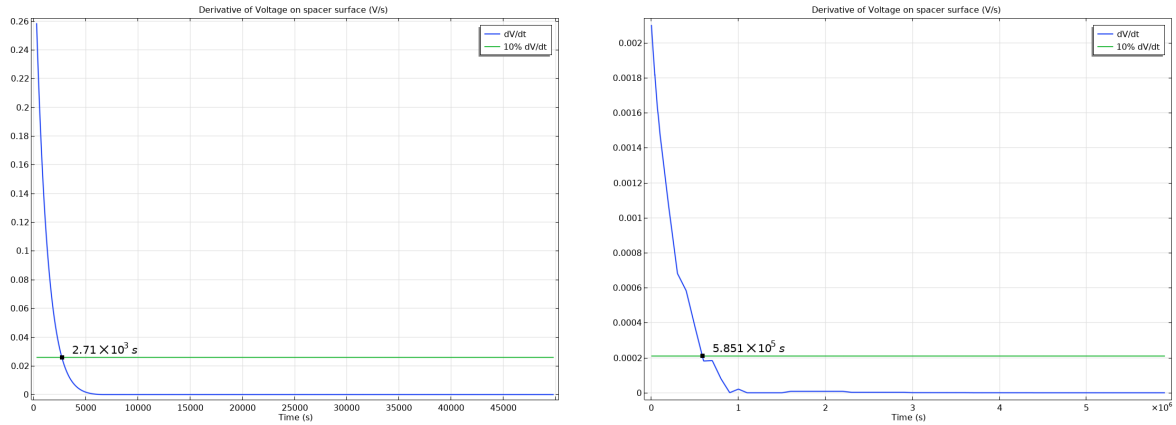
Figure 4.6: Simulations of electric field across 2 hrs for a given voltage of + 30 kV DC for nylon



(a) Capacitive field distribution **(b)** Transitional field distribution **(c)** Resistive field distribution

Figure 4.7: Simulations of electric field across 120 hours for a given voltage of + 30 kV DC for PTFE

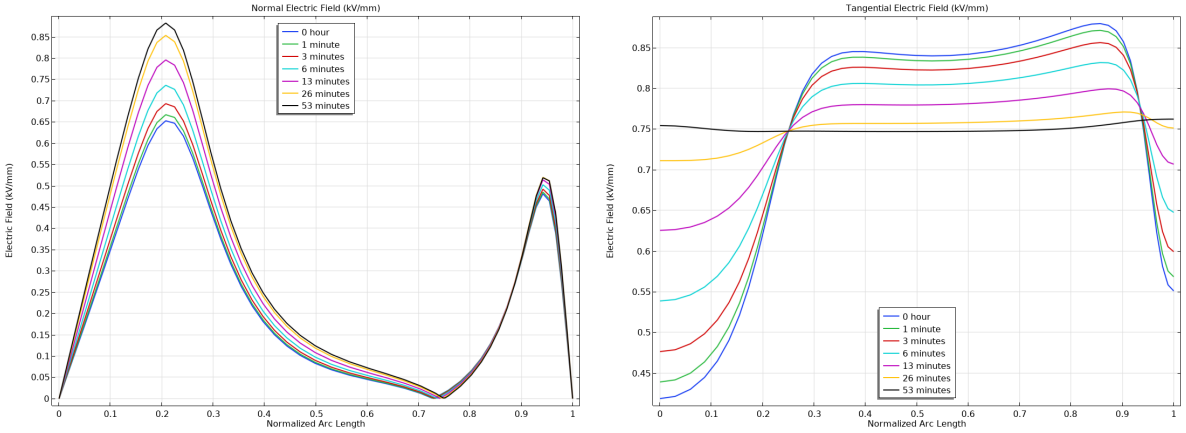
As seen in the plots above, the conductivity of the material is higher than that of the surrounding gas, as seen in Figure 4.17. For both Nylon and PTFE, the field transitions at the surface near the shielding with heteropolar charges accumulating from the ion deposition in the bulk. The peak capacitive fields of 2.81 and 2.6 kV/mm increase to 3.17 and 3.19 kV/mm, indicating that the resistive field imposes greater stress on the insulation. It can also be observed that the field profiles across both cases match the simulated Epoxy resin material given in Figure C.9. The time taken to reach the steady state in the simulations is also 0.7 hours and 90 hours, which closely match the previous $t_{90\%}$ calculated, as seen in Figure 4.8.



(a) Nylon **(b)** PTFE

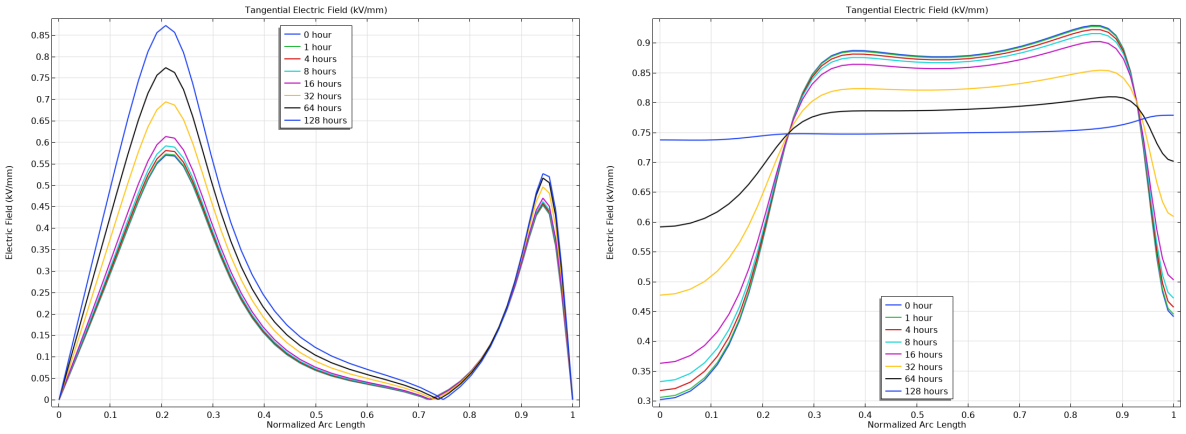
Figure 4.8: Derivative of Voltage across spacer surface and $t_{90\%}$ for +30 kV DC

It must be noted that in this test setup, using a spacer with lower gas conductivity than dry air of roughly 3.59×10^{-20} [S/m] would result in homopolar charge accumulation and fields on the conductor being pushed away from the spacer. Increases in ionization from the electrode emission or other sources would also increase the number of ions in the active gas volume, reducing the effective gas conductivity. In this scenario, an effective ion-pair generation value of S = 10^3 IP/$cm^3 s$ would be needed to observe homopolar charge accumulation with the PTFE spacer. The transition of the field components across the nylon spacer for both cases, and the maximum values of the normal and tangential field components are further presented in Figure 4.10 below.



(a) Normal Component E_n **(b)** Tangential Component E_t

Figure 4.9: Simulation of spacer field components across time 1 hour for Nylon, given applied +30 kV DC



(a) Normal Component E_n **(b)** Tangential Component E_t

Figure 4.10: Simulation of spacer field components across 128 hours for PTFE, given applied +30 kV

The heterocharge deposition for both nylon and PTFE results in an increase in the normal component of the field, while the tangential field similarly flattens. The same behavior is observed throughout the epoxy resin, as all tested scenarios exhibit higher bulk conduction currents than in the gas.

Choosing Appropriate Voltages

Given an optimized geometry that matches the general design criteria specified prior, the applied DC prestress voltages must be chosen to ensure that the field targets and surface charge accumulation

requirements match those in Table 4.1. The DC operational voltage of the system can therefore be determined as the voltage value that produces peak tangential and normal fields of 0.875 kV/mm for 3 bars of air.

A parametric sweep was run in COMSOL for each applied voltage, and the extracted normal and tangential components for Nylon and PTFE are presented in Table 4.4 below. Note that the varying voltages are set in 2.5 kV steps from 0 to 40 kV, and for the sake of brevity, the simulated DC voltages in this table are positive only.

Table 4.4: Maximum simulated field components for both cases under varying applied prestress voltages

Voltage (kV)	**Nylon**		**PTFE**	
	E_n (kV/mm)	E_t (kV/mm)	E_n (kV/mm)	E_t (kV/mm)
0.0	0	0	0	0
2.5	0.0740	0.0730	0.0479	0.0772
5.0	0.147	0.147	0.0958	0.154
7.5	0.223	0.220	0.144	0.232
10.0	0.297	0.294	0.192	0.309
12.5	0.371	0.367	0.240	0.386
15.0	0.446	0.441	0.287	0.463
17.5	0.520	0.514	0.335	0.540
20.0	0.594	0.587	0.383	0.618
22.5	0.669	0.661	0.431	0.695
25.0	0.743	0.734	0.479	0.772
27.5	0.814	0.808	0.527	0.849
30.0	0.891	0.882	0.575	0.926
32.5	0.962	0.955	0.623	1.00
35.0	1.04	1.03	0.671	1.08
37.5	1.11	1.10	0.719	1.16
40.0	1.19	1.18	0.766	1.24

From the table above, it is evident that the imposed design limits for normal and tangential fields are quite close together in both nylon and PTFE, with a linear trend across the table. It can therefore be seen that the difference in permittivity (3.5 vs 2.1) results in comparable capacitive fields. The cells highlighted in light orange represent the chosen DC prestress voltage for 1 bar, medium orange for 2 bars, and dark orange for 3 bars.

It is also useful to establish a reference LI voltage at which breakdown is expected, which can subsequently be simulated in the following section. Breakdown is considered to occur once the field in the gas medium exceeds the critical field E_{crit} of 3 kV/mm for streamer inception, with propagation subsequently sustained by an average field above 0.5 or 1.2 kV/mm for positive and negative streamers, respectively [64]. A rough voltage of 50kV is taken as the LI breakdown value for 1 bar of dry air. The voltages used in the simulations throughout this document are therefore +30 kV DC and $\pm$150 kV LI, unless otherwise specified.

4.4.2. DC/LI simulations

Superimposed DC/LI simulations were performed by applying a standard 1.2/50 μs impulse to a DC voltage, setting $V_{DC} + V_{imp}$ as a boundary condition for the HV electrode. The surface charge solution from the coupled simulation described above is used as the initial value for the study, with the modeling of the representative GIS systems following the recommendations in Chapter 4.3.1 of CIGRE TB 842 [12].

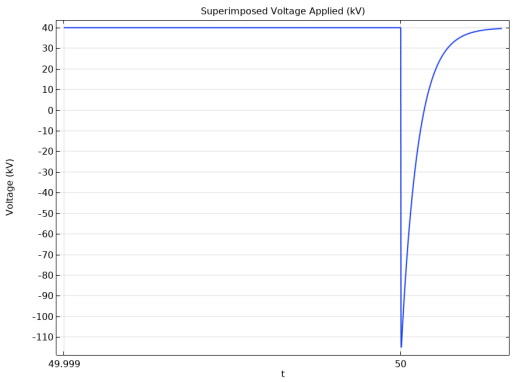


Figure 4.11: Applied SIMP OP waveform for 40 kV/-120 kV on COMSOL

The goal of the superimposed transient simulations is to visualize how the charge accumulated after DC application on both Nylon and PTFE affects the fields across the spacer under different applied impulse-voltage polarities. CIGRE TB 842 [12] specifies in Chapter 7.4.4 that type tests with superimposed DC/LI testing must be done under Zero load (ZL) conditions with a pre-stress time of 2 hours. This further aligns with many prior works on superimposed testing [48], [65]. For the sake of brevity, only positive DC and $\pm$ LI are considered in the simulations below, and Figure 4.12 shows the development of the tangential field across the spacer for an applied impulse voltage on the Nylon spacer.

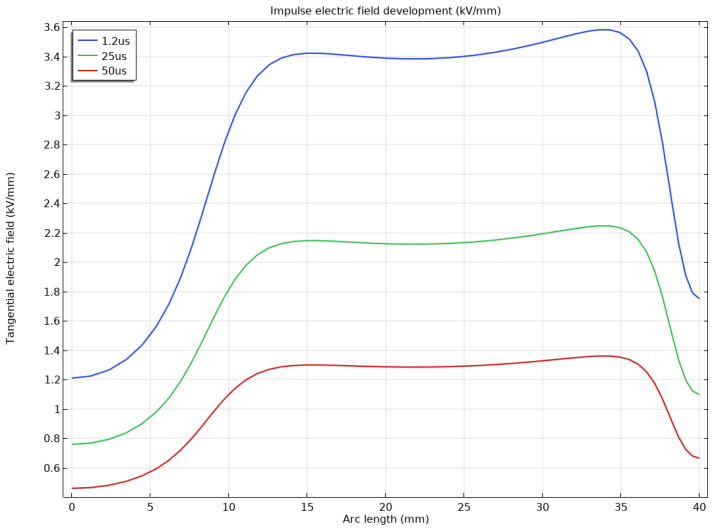
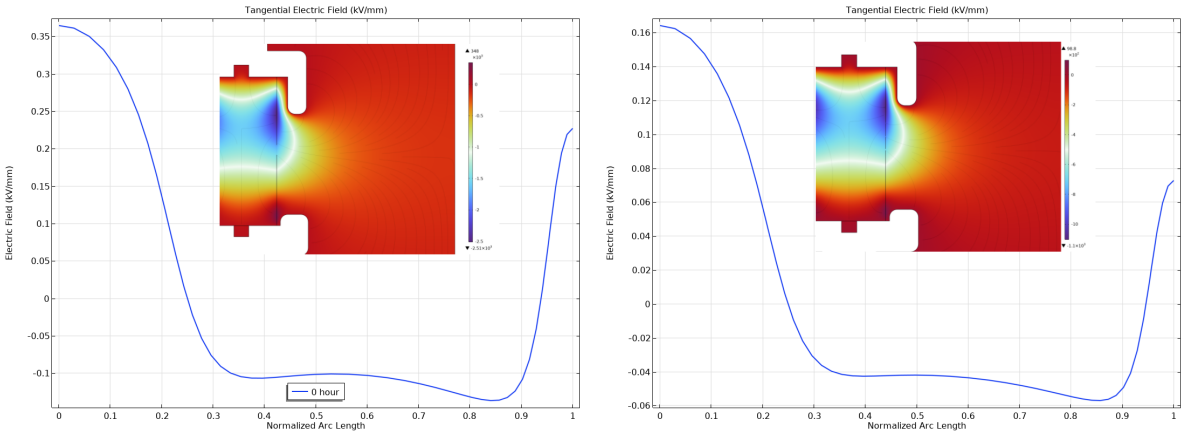


Figure 4.12: Development of tangential fields across the spacer for applied +150 kV impulse with PTFE

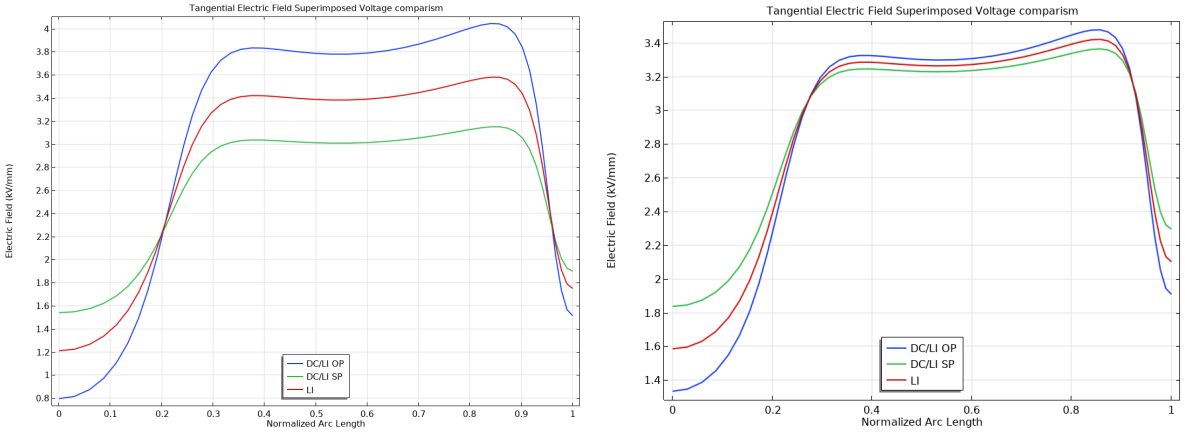
The impulse develops a peak tangential field across the spacer of 3.55 kV/mm and then rapidly decays, with the field magnitude at 1.2 μs considered most stressing on the insulation. The introduction of DC prestress induces charge accumulation on the spacer surface, which acts as a voltage source term that generates its own field and can cause a peak field increase as seen in Figure 4.13.



(a) Nylon **(b)** PTFE

Figure 4.13: Comparison of tangential fields from 2 hours of charges in both cases for +30 kV DC, where blue represents negative charge and red positive

Assuming the tangential field across the spacer has the same polarity as the LI waveform, the fields constructively add, with peak contributions of 0.17 kV/mm for PTFE and 0.36 kV/mm for nylon, resulting in lower flashover voltages. Figure 4.13 below shows the tangential fields of the superimposed DC/LI waveforms, simulated with different LI polarities.



(a) Nylon **(b)** PTFE

Figure 4.14: Comparison of tangential fields during different polarities of superimposed stresses for 30 kV DC and $\pm$ 150 kV LI

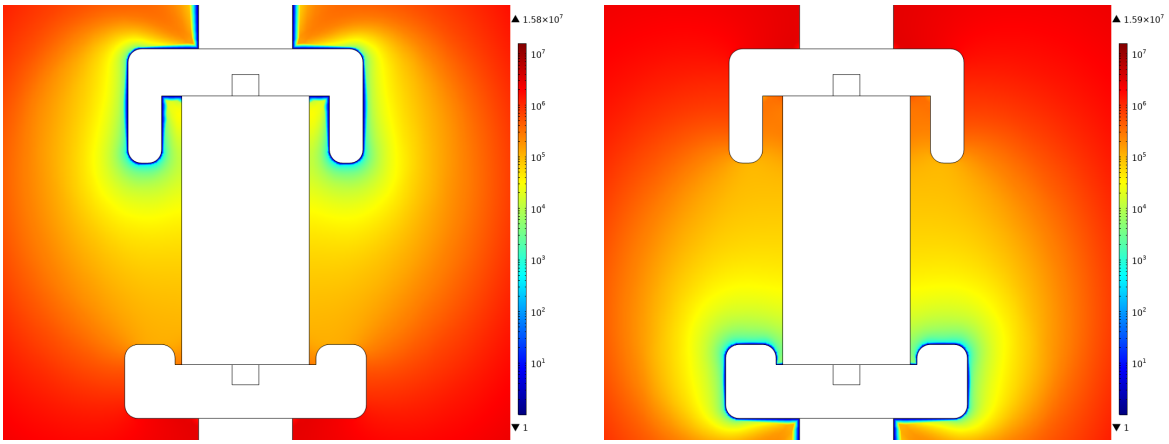
The worst-case stress can be observed as an opposite polarity (-150 kV) for both materials due to heteropolar charge accumulation near the shielding. The worst-case field increase is 0.06 pu and 0.1 pu, respectively, compared to only LI. The field distribution also differs from the standard LI shape for both superimposed waveforms due to the magnitude of the accumulated charges.

This behavior arises because the polarity-specific charge deposited by the bulk- or gas-dominated current produces its own E-field, independent of the applied voltage. A fast impulse transient of the same polarity superimposes with the tangential fields, adding constructively. This, therefore, reduces the effective breakdown strength of the insulation and causes superimposed flashovers at lower voltages than in purely LI. This also agrees with Toigo et al. [20], who similarly reported that a homopolar

charge on the disc spacer surface produces the highest stress for a positive superimposed impulse under ZL conditions. CIGRE TB 842 [12] therefore also specifies testing across all 4 DC/LI polarity combinations.

4.4.3. Charge Simulations

As mentioned in Section 2.3 and elaborated in section C.1, the charge accumulation on the gas-solid interface is a function of both Gas and Bulk normal conduction current. This ultimately depends on the ratio of permittivity and conductivities across the interfaces. The resulting steady-state ion concentration distributions under an applied voltage of +30 kV DC are shown in the Figure 4.15 below.



(a) N_p concentration **(b)** N_N concentration

Figure 4.15: Ion concentrations under steady-state DC given applied +30 kV DC

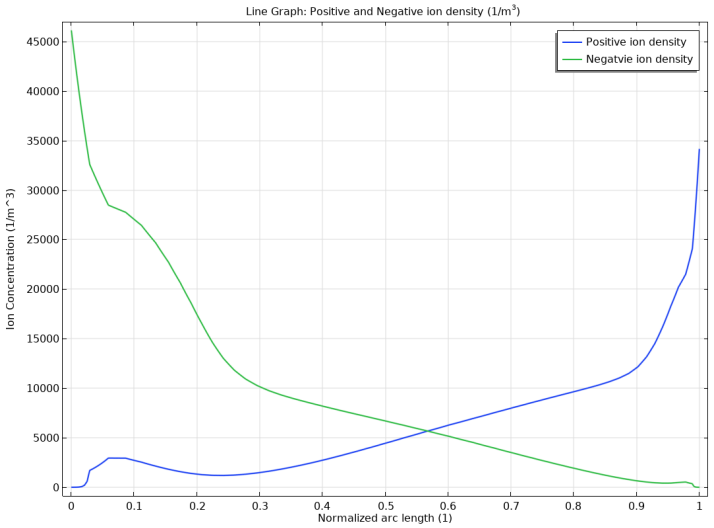


Figure 4.16: Ion density across spacer for steady state +30 kV DC

The charge deposited by the gas component on the spacer surface is governed by ion motion under the applied field. For the +30 kV DC voltage, positive ions migrate away from the high-voltage electrode, while negative ions similarly migrate away from the GND electrode, drifting rapidly toward the electrodes according to $t_{p/n} = \frac{d}{\mu_{p/n} \cdot E}$ [23].

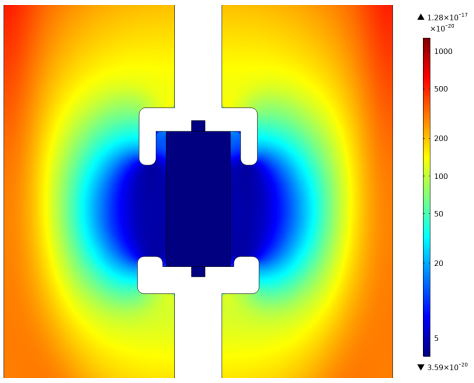


Figure 4.17: Gas conductivity derived from ion density in COMSOL

For the applied fields, the ions traverse the 28 mm gap in less than 100 μs. Because this transit time is much shorter than the timescale over which additional ions are generated, ions are swept out of the gas volume before they can accumulate, resulting in a very low steady-state charge density near the spacer surface, on the order of a few pC/m^3. The ions' motion also governs the gas's conductivity, which does not remain constant throughout the gas volume; the conductivity of 1 bar dry air is shown in Figure 4.17. The value near the spacer remains at 3.59×10^{-20} [S/m] for 3 bar dry air.

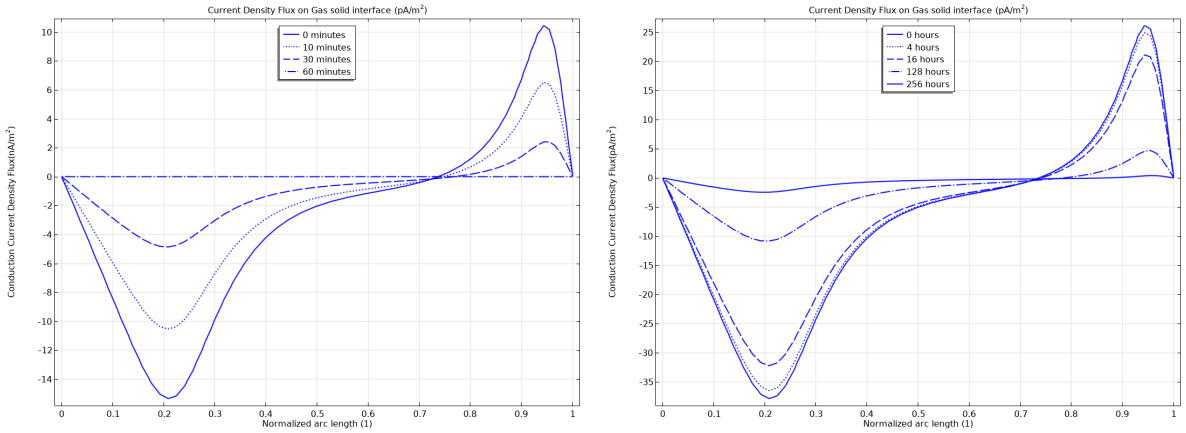
The charge accumulation at the spacer-gas interface under a constant electric field can therefore be expressed in terms of the displacement field, according to Gauss's law.

$$\sigma_{surf} = \mathbf{n} \cdot \mathbf{D}_G - \mathbf{n} \cdot \mathbf{D}_B = \varepsilon_G E_{Gn} - \varepsilon_B E_{Bn} \tag{4.9}$$

Where $\mathbf{D}_G$ and $\mathbf{D}_B$ are the displacement fields in the gas and bulk, respectively. When Equation 2.4= 0, the equation can be combined with Equation 4.9, resulting in the equation below.

$$\sigma_{surf} = \left(\varepsilon_G - \frac{\sigma_G}{\sigma_B} \varepsilon_B n \right) E_{Gn} \tag{4.10}$$

As mentioned in section C.1, gas-based current density is split into three regions: linearity, saturation, and avalanching, with this study effectively considering only the middle regime. The transition point between the linear and saturation regimes for a gas such as SF_6 is very low, as reported by Zhang et al. [66], in the order of a few V/mm, and was estimated as 20-50 V/m in a uniform field, as seen in Figure C.7. The current across the gas interface from the gas side can therefore be considered constant regardless of the field, while conduction on the bulk side follows Ohm's law and increases linearly with the applied field. The relative magnitudes of these two current components determine the polarity of the charge accumulation. Figure 4.18 below shows the current density flux across the gas-solid interface for both cases.



(a) Nylon **(b)** PTFE

Figure 4.18: Conduction currents on spacer surface from gas and bulk for Nylon and PTFE

In both cases, assuming a positive applied DC voltage, the material's conductivity yields different ohmic behavior with different J_{cond} vs E-field slopes, resulting in different current densities for a given applied voltage. The gas conduction current remains essentially constant and is around 0.35 pA/m^3, which is negligible compared to the current density of the bulk. At an applied voltage of 30 kV, the initial current density on the spacer side for nylon and PTFE is 15 nA/m^2 and 37 pA/m^2, respectively. Figure 4.19 below shows the linearity and dominant process for surface charge deposition.

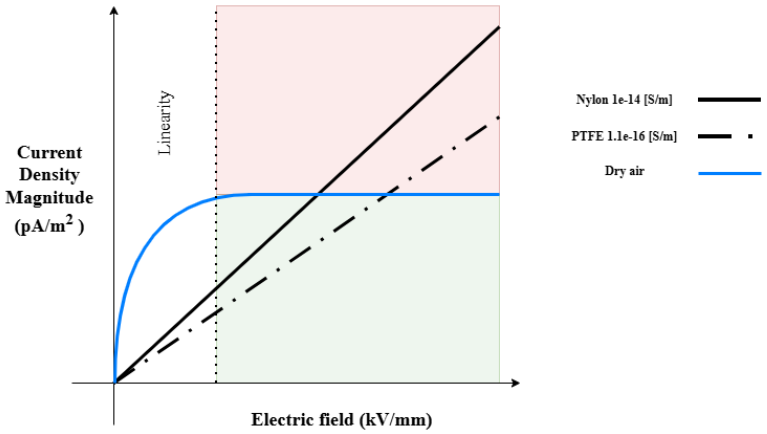


Figure 4.19: Conduction current process on charge accumulation (Red = Bulk dominated, Green = Gas dominated)

It can also be noted that there must be a conductivity where the difference between the two current densities is initially minimized for a given S rate, and the least surface charge is therefore accumulated. In this scenario, if the bulk conductivity remains around $3 \times 10^{-20} S/m$ for +30 kV, the charge can be minimized. The works by Lai et al. [62] found this "critical conductivity" of SF_6 to be roughly $2 \times 10^{-17} S/m$ for an S of 50 IP/cm^3. Given the +30 kV DC for the geometry in 3 bar technical air, the steady-state charge accumulation across the spacer surface for different applied voltages is illustrated in Figure 4.20 below.

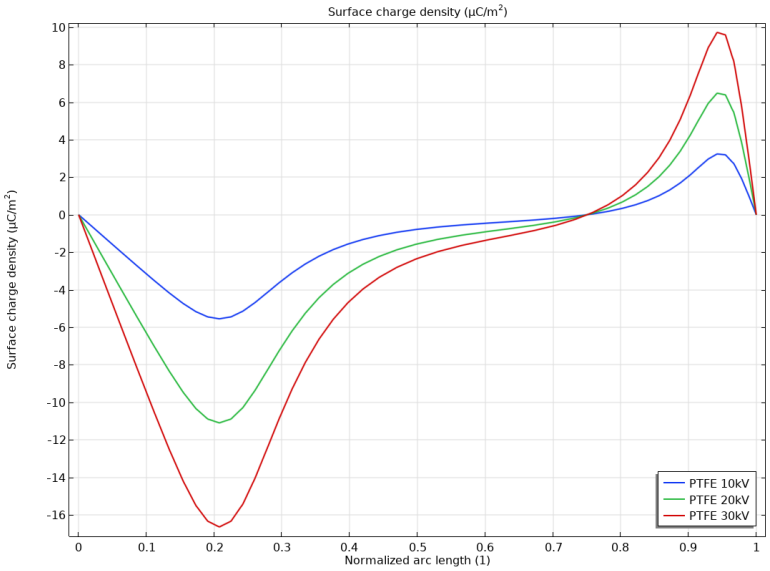


Figure 4.20: Simulation of the surface charge across the PTFE spacer for +30 kV DC

The simulated steady-state surface charge, as shown in the plot above, varies with the applied voltage and has the same polarity across all 3 cases. The peak observed charge on the PTFE spacer is -16.4 $\mu C/m^2$ with charge accumulation near the GND divots reaching 9.8 $\mu C/m^2$. The steady-state charge accumulation for Nylon and epoxy resin was also quite similar, given that the term $\frac{\sigma_G}{\sigma_B}\varepsilon_B n$ in Equation 4.10 was minimized from the very big conductivity mismatch in the gas and the bulk. It can therefore be seen that a reduced-scale electrode design has been realized with the field profile of a disc spacer, reduced-scale values, and FEM simulations.

5

Enclosure Design

Moving outwards from the electrode configuration, the design and dimensioning of the enclosure is the next step in realizing the system. Given the lack of available GIS/GIL test sections and HVDC bushings, a test cell had to be constructed that could be pressurized to 3 bar and support DC/LI superimposed testing. Many mechanical and electrical design requirements were considered, with the most important for this section given as

1. Feedthrough of the high-voltage connection
2. Creepage distance along the outer surface
3. Ensuring sufficient external clearances
4. Choice of gas-tight components
5. Allow for a camera to view the spacer sample
6. Mechanical stability of spacer sample

The project scope focused on the research, design, and FEM field simulation of an enclosure with general mechanical constraints and on identifying potential failure points, rather than explicitly manufacturing the cell. The technical drawings and manufacturing were assisted by a technician from TU Delft's HV lab. The two key considerations for the chapter are not significantly interfering with the field distribution near the spacer and ensuring breakdowns occur only between the test electrodes under operating pressures up to 3 bar. Note that the DC value of 30 kV and impulse value of 150 kV from section 4.3 are used in the analysis, as the test cell targets a maximum of 3 bar.

5.1. Models considered

The primary goal of the enclosure design was to accommodate both DC and LI impulses simultaneously, which introduced challenges of sufficient creepage and size constraints. Existing literature on

test cells offers few options dimensioned for superimposed voltages, with no broad reference designs found. A list of the closest comparable test cells is presented in Section B.2. From this survey, three initial designs are proposed: a completely floating model, a spacer-topped metal cell, and an HV flange setup, each adapted from concepts in the literature. The COMSOL implementations of all models are discussed below. The concepts were evaluated first against the requirements above, then by FEM simulations at the operational voltages, and finally through feasibility discussions with HV technicians at TU Delft. All cells are evaluated at a preliminary superimposed voltage of 30 kV/ 150 kV, with the initial potential problems of each design identified below.

5.1.1. Floating Cell

The floating cell design **(1)** was adapted from prior work [67, 68, 69], with the principle that all enclosure materials were non-conductive. It was primarily selected because it maximized the external creepage distance between the high-voltage conductor and earth (2.). As discussed in Section 5.2, the high LI amplitudes relative to DC made effective clearance a priority, and this design had the greatest among those considered (3.).

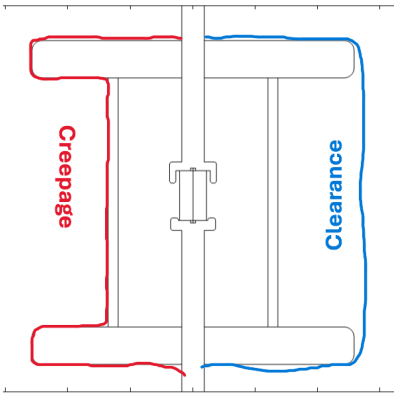


Figure 5.1: Floating Cell **(1)**

Since the cell walls could be made of clear insulating material such as PMMA, all sides of the spacer could be viewed (5.) with a camera and mirrors, as discussed in Section 7.1.2. The design was also preferred as the high-voltage feedthrough could be kept simple, as advised by the TU Delft technicians (1.). The main drawback is that the insulating materials throughout the cell led to surface charge accumulation, which both affects the field profiles near the electrodes and requires care in safely handling the cell after DC application. Given the relative simplicity of implementation, the cell was chosen for further dimensioning. Its electric field simulations and charge accumulation are presented in Section 5.3.

5.1.2. Spacer Cell

The spacer-topped metal cell design **(2)**, inspired by Wang et al. [70], used a commercial basin spacer as the top flange of a metal housing. A 126 kV disc spacer available in the TU Delft lab was considered for the upper flange, with an effective upper radius of 125 mm; the simulated cell and disc spacer model are given in Chapter C. The model was not chosen because the effective clearance and creepage across the spacer top were much smaller than those of the other models (2., 3.). No other spacers were available, so the applicable voltages were limited.

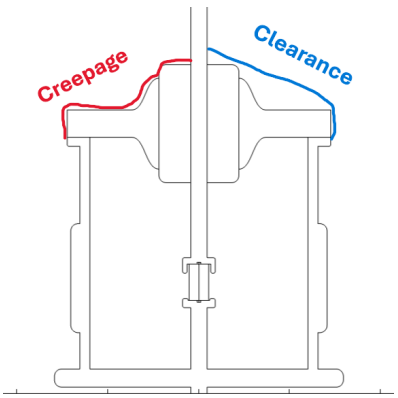


Figure 5.2: Spacer Topped Cell **(2)**

The HV feedthrough also faced problems, as the hole in the spacer was larger than the electrodes, requiring either an 88 mm conducting rod or an insulating material (1.), making gas tightness harder to achieve (4.). The effective internal volume was

also large, requiring substantial material for the metallic base, and the enclosure would need multiple windows to capture flashover on all sides of the spacer (5.). This design was not chosen as it was the weakest for most of the requirements above.

5.1.3. Metal Flange Cell

The metal flange design **(3)** has been used previously for AC GIS tests at Delft and for DC PD work [71, 72], primarily for DC PD testing at voltages up to 60 kV DC. The electrode configuration meant the creepage and clearance were less than those of the floating cell (3., 2.). The cell had plexiglass walls similar to the floating enclosure, allowing surface flashovers to be viewed from multiple directions (5.), and offered benefits in feedthrough and gas tightness, since the internal electrode and metal flange were connected. Overall, this model was not chosen because it showed smaller clearance and creepage distances and higher charge on the plexiglass wall, as shown in Chapter C.

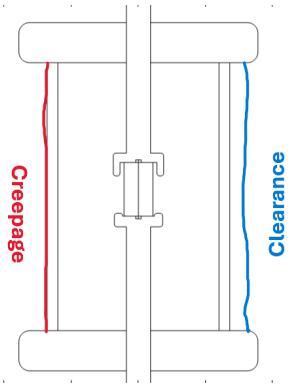


Figure 5.3: Metal Flange Cell **(3)**

Given the simulations in Chapter C and conversations with the lab technicians, the floating cell was chosen for its highest possible clearance and creepage distances and its ease of prototyping and modification as problems were observed. The finalized 3D floating cell geometry, modeled in CAD courtesy of the HV lab, is shown in Figure 5.4 with appropriate mechanical supports.

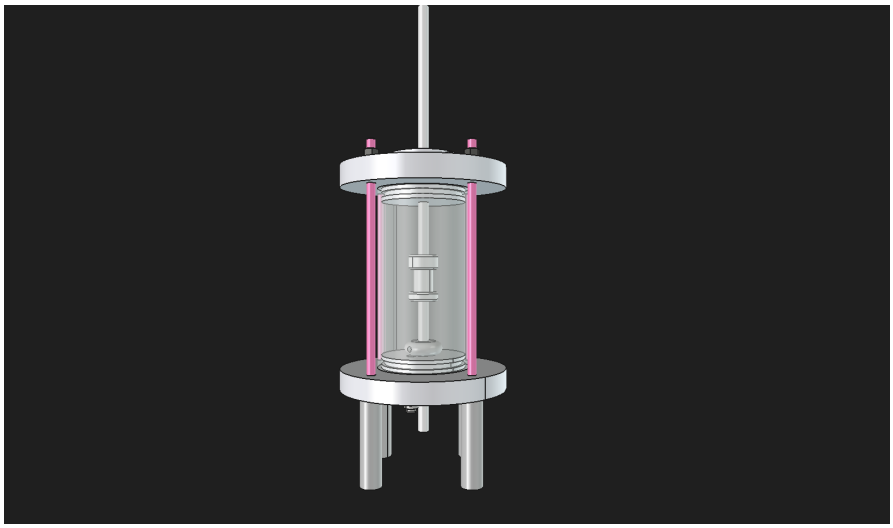


Figure 5.4: 3D CAD model of the floating cell with mechanical supports, considered courtesy of Javier Gonzalez Martin

5.2. Clearance Distances

The dimensional design of the test cell is of great importance as the primary goal was to ensure that breakdown occurred across the intended electrode gap rather than any external path. Insufficient clearance between the high-voltage electrodes and any external insulating materials would result in charge accumulation and an elevated risk of external flashover. Given that the test cell is also expected

to test until 3 bars, a maximum impulse magnitude of up to 150 kV would be considered. The internal volume and external dimensions are presented in the section below.

5.2.1. Internal Volume

The proximity of the Plexiglass to the electrodes poses a risk of charge accumulation and alternate flashover paths if not properly dimensioned. The effect of the distance between the Plexiglass and the spacer is evaluated for the capacitive fields, resistive fields, and surface charge on the PMMA. Table 5.1 shows the field and charge simulated for 3 different tested distances from the spacer.

Table 5.1: Effect of spacer and plexiglass distance on plexiglass Charge and capacitive/ resistive field at the conductor

Distance (mm)	Capacitive field (kV/mm)	Resistive field (kV/mm)	σ_{PMMA} (μC/m^2)
9.5	4.09	4.56	-4.96
29.5	3.7	3.85	-2.83
49.5	3.17	3.27	-1.98

It was noted that when the distance was less than 20 mm, the maximum field at the electrode pulled away from the spacer and towards the PMMA. The larger distances simulated showed fewer effects on the field of the spacer and resulted in lower surface charge accumulation on the Plexiglass. While it would be ideal to have as big a distance as possible, the maximum possible size was based on a pipe of 12.5 cm diameter available at the TU Delft HV lab and was therefore chosen as the dimensions of the Plexiglass wall. The internal gas volume of the cell is 22.6 dm^3

5.2.2. External Sizes

The flange sizing and height of the test cell also play a key role, as the use of pressurized gases increases the likelihood that the weakest dielectric path becomes the external atmospheric air surrounding the cell. At 3 bars, the breakdown strength of the inside air is roughly 9 kV/mm compared to the external 3 kV/mm, with it being observed that increasing pressure and voltage will eventually cause breakdown across the outside of the cell. Typically, HV bushings are used for this purpose to create sufficient clearance between the HV conductor and the grounded cell; however, the lab at TU Delft did not have access to HVDC bushings. The choice of the enclosure essentially had to fulfill this purpose by providing sufficient clearances (shortest path from HV to ground through air) and creepage (shortest path from HV to ground across the insulating surface).

Dimensioning of insulation for this scenario can be done using standards such as IEC 60071-1 [73], in which the system's maximum overvoltage determines the clearance distances. Table A.1 in the document prescribes the minimum clearance distances for insulators for a lightning withstand of 170 kV in a rod-plane configuration. The minimum clearance is therefore determined as 320 mm . The chosen distance ensures that no standalone lightning voltages would break down the insulation; however, the introduction of surface charging from the DC application can significantly reduce the stress, as seen in subsection 4.4.2. The chosen distances are based on a rod-plane setup in which no insulating medium exists between the HV conductor and the ground, and atmospheric conditions could vary. A high safety factor of about 50% was added to ensure that no external breakdowns would occur. The minimum required clearance of 480 mm was achieved with a 200 mm-tall plexiglass, a 120 mm flange radius, and a 30 mm flange height.

Dimensioning of creepage distances for DC insulators is much more difficult in that the pollution of the environment plays a much bigger role in choice of appropriate distances [74]. Given that the impulse voltage magnitude is much greater than the DC pre-stress and the very large safety factor attached above, the choice is made not to consider DC creepage distances. Testing of the cell under DC and LI under pressurized conditions must be performed and given that external breakdowns are observed can be remedied by increasing the height of the plexiglass walls.

It must be noted that the goal of this section is not to explicitly minimize insulation length or make the cell as compact as possible, but rather to arrive at an overdimensioned system that can both be created at the TU Delft HV lab and reliably withstand the full operational voltage range up to 3 bar. The cell, given the sizing, is expected to be capable of voltages up to +30 kV DC and 150 kV LI with further FEM simulations in Section 5.3.

5.3. Field Simulations

The Electric field simulations are performed using the finalized electrode geometry with a simplified floating cell configuration that has the same major components, such as the flange and the feed-through, but without the sealing components or mechanical supports found in the real cell, in order to save computational time. The 2D axisymmetric COMSOL model of the simplified floating cell is further presented in Figure 5.5 below.

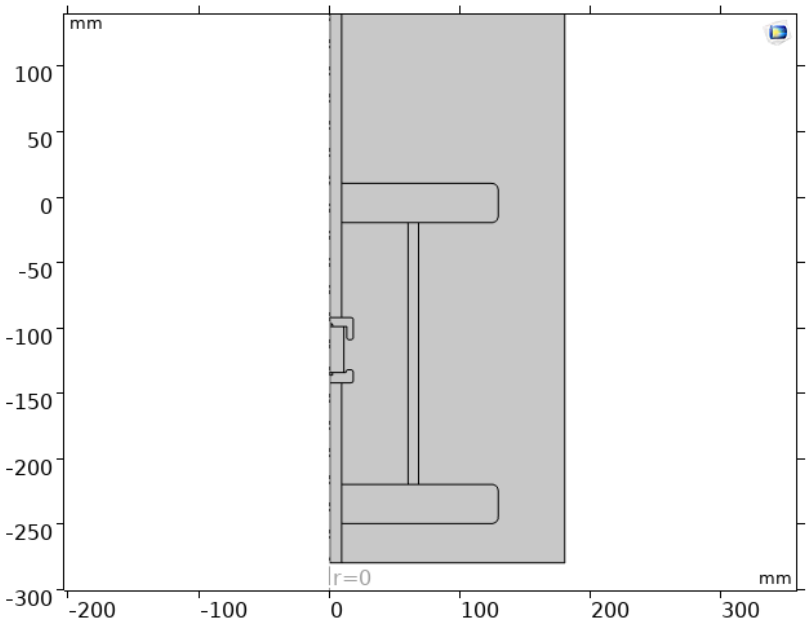


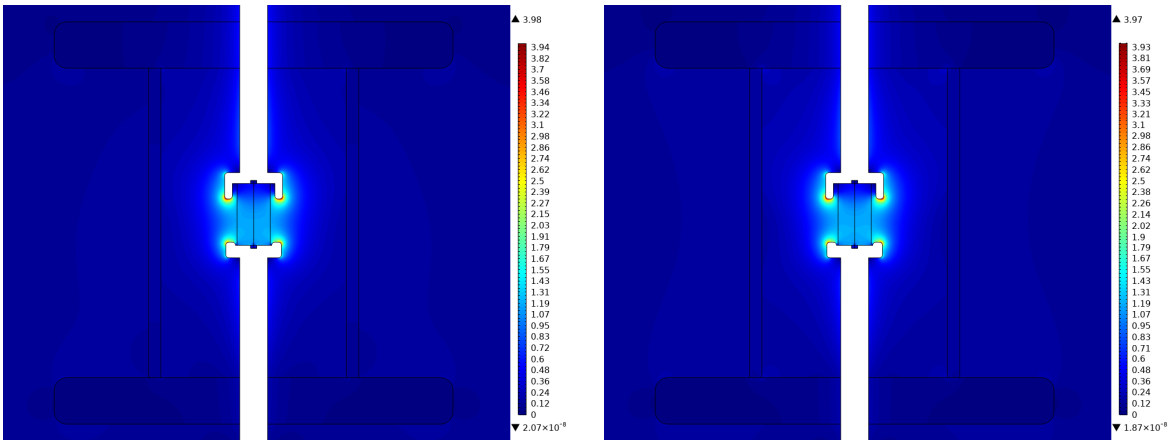
Figure 5.5: Scale-accurate COMSOL setup of the simplified floating enclosure filled with technical air

The key parameters for the test cell were dimensioned in section 5.2, with the height and the distance between the Plexiglass wall and the electrodes being the most important considered parameters. The height of the Plexiglass, as mentioned previously, is set to 200 mm, with the insulating flanges having a radius of 120 mm, leaving sufficient room for 4 mechanically threaded nylon supports as seen in Figure 7.2a.

5.3.1. DC Simulations

The goal of the DC simulation section is to simulate and verify that the electric fields generated by charges accumulated on the insulating enclosure do not affect the fields at the test electrode and that, under worst-case superimposition, the fields outside remain low enough to guarantee no breakdown. The materials chosen for the cell walls were Plexiglass to facilitate visualization of spacer flashovers. The material properties are taken from an online material database with a relative permittivity of 3.44 and a bulk conductivity of 3.26×10^{-14} [S/m] [75].

The timescale of the simulation at $t_{90\%}$ of the PTFE spacer, as given in subsection 4.4.1 and the simulations of the initial capacitive and resistive distributions under an applied +30 kV DC are illustrated in Figure 5.6 below.

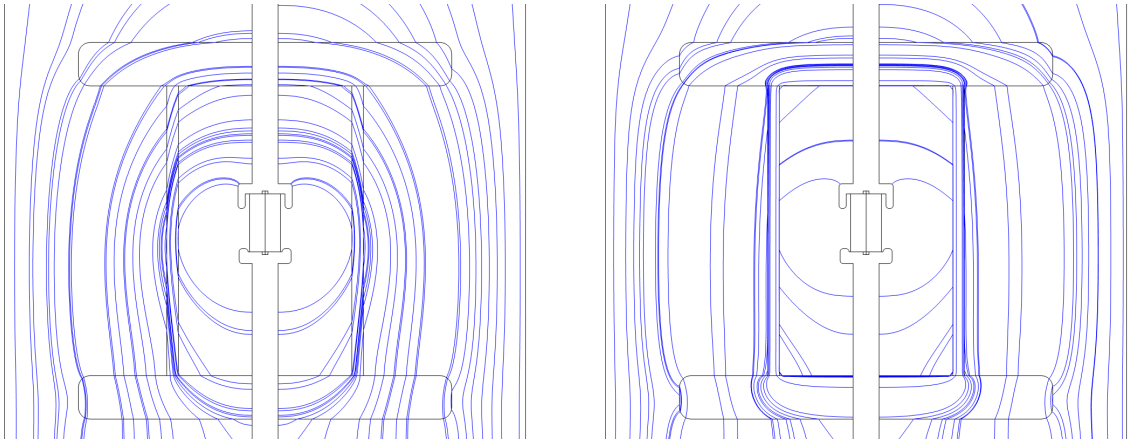


(a) Capacitive field distribution

(b) Resistive field distribution

Figure 5.6: Electric field of simplified floating cell comparison with applied +30 kV DC

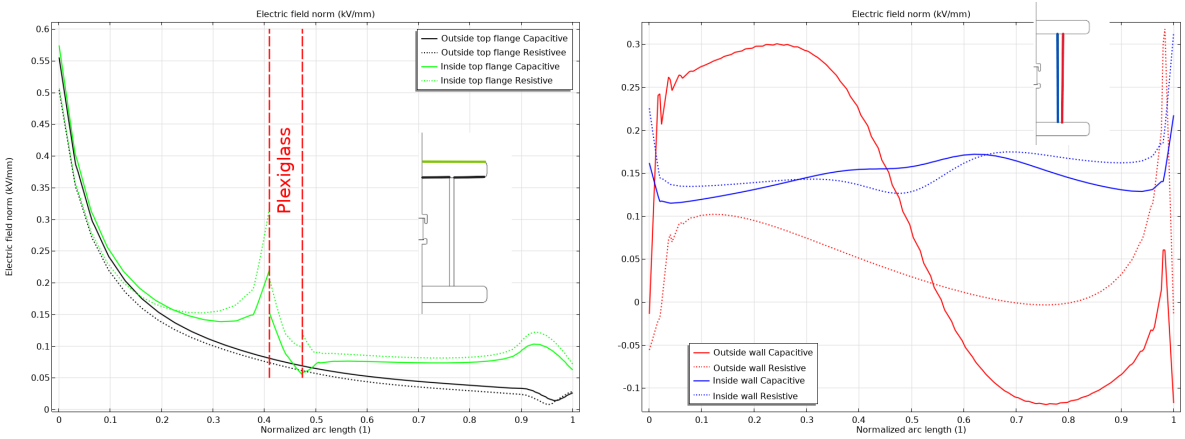
As seen in the simulation above, the field outside the cell on all sides remains far less than around the electrodes. The field in the internal volume of the cell is also very low, with values remaining around 0.5 kV/mm for 3 bar air. Under DC operation, it is therefore likely that discharges occur between the electrodes where expected. The DC steady-state plots also show some enhancements in areas on the insulator where charge has accumulated. However, these enhancements are very small, with the maximum observed field of 0.3 kV/mm at the intersection of the Plexiglass and the nylon flange. Figure 5.7 also shows the field streamlines for a capacitive and resistive field.



(a) Capacitive field **(b)** Resistive field

Figure 5.7: Field streamlines for capacitive and resistive field given +30 kV DC

It is observed that the streamlines in the resistive field distribution concentrate due to the conductivity of the materials, with greater concentration in plexiglass and nylon due to the charge built up across all the insulating surfaces. The Figure 5.8 below further shows the maximum electric fields across the Plexiglass and the nylon flange for an applied +30kV DC.



(a) Top nylon flange **(b)** Plexiglass wall

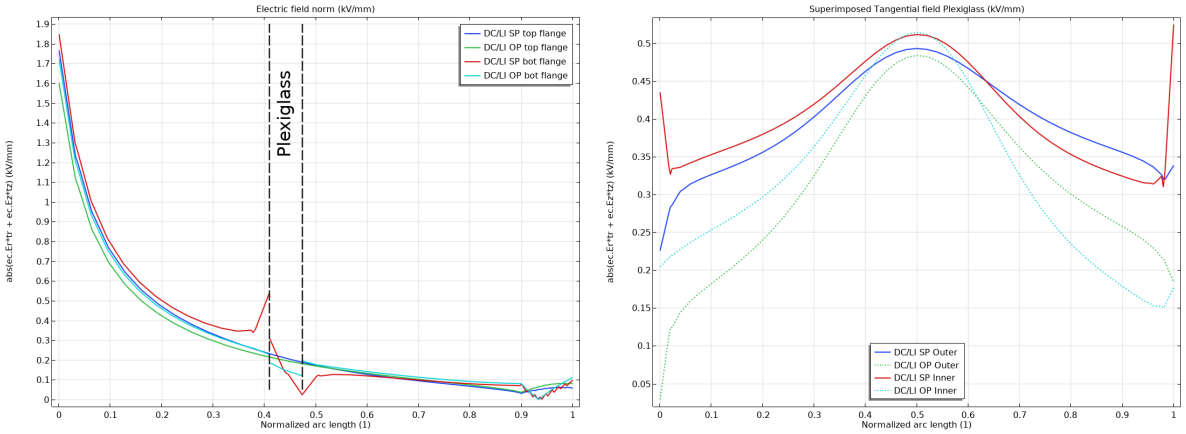
Figure 5.8: FEM results of the field across both the inside and outside of the Nylon flange and the plexiglass wall during DC application

It can be seen that the nylon flange experiences the highest field at the point where it borders the HV conductor at 0.55 kV/mm for 3 bar. It can be seen that charge deposition, especially at the intersection of nylon and plexiglass, increases the fields. The maximum fields across the inside and outside of the plexiglass wall are 0.32 kV/mm. It is observable that the field values on the nylon and Plexiglass remain well below the surface flashover fields, as concluded by Pillai et al. [76]. It is therefore expected that during DC application up to 3 bar, no flashovers across the outside are expected.

5.3.2. DC/LI Simulations

As mentioned previously, the LI and superimposed LI fields contribute significantly to the system's dimensioning, and it is of great importance that the fields experienced are not large enough to cause

an external breakdown. The method of the simulations is the same as presented in Section 4.4.2 with a voltage of +30 kV DC and ± 150 kV LI. The fields of different superimposed polarities simulated across the top flange and the plexiglass are given in Figure 5.9 below.



(a) Top flange **(b)** Plexiglass wall

Figure 5.9: Tangential field across both the inside and outside of the Nylon flange and the plexiglass wall during different superimposed DC/LI applications

As visualized in the plots above, the fields at the peak of the superimposed impulse are much higher than the DC operation, with a redistribution of the fields visible between DC/LI polarities. For the flange, the peak field on the outside is 1.85 kV/mm at the nylon and conductor interface and remains below the nylon LI surface flashover E field in 1 bar air of 2.37 kV/mm, as given by Pillai et al. [76]. It is also observed that the same polarity superimposition corresponds to the worst-case stress, since the accumulated charge inside the nylon flange is positive. The fields on the plexiglass interior follow the same trend due to homocharge accumulation and reach a worst-case value of 0.52 kV/mm at the interface with the nylon. The fields outside remain smaller. The outside fields across the Plexiglass and nylon remain well under the surface flashover voltage, with the fields in the gas gap remaining less than the critical field of air under 3 kV/mm. It can be concluded that the breakdown of the applied impulse levels is expected to be seen inside the cell and not outside.

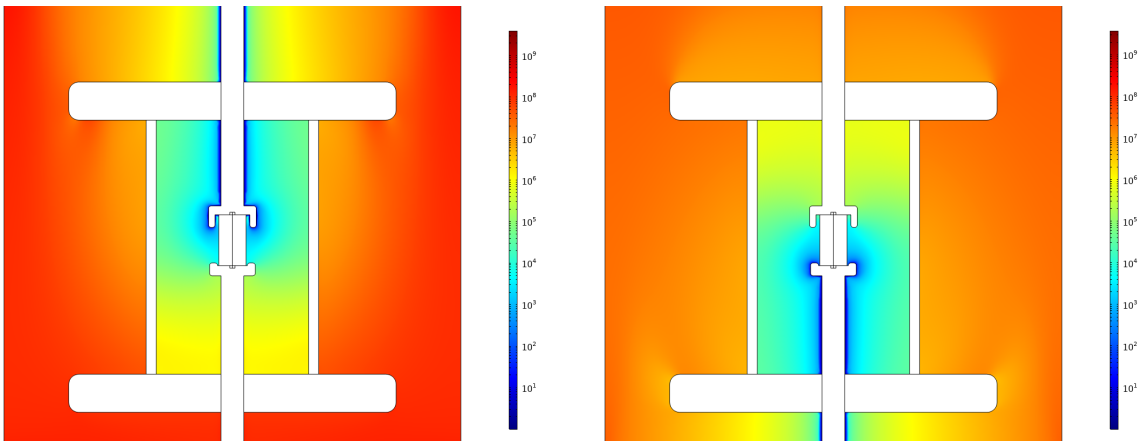
5.3.3. Charge Simulations

As discussed previously, the implementation of charge in the cell results in different conduction currents for the gas inside and outside the cell, and charge accumulation must be considered for both. The parameters defined for electrode simulations apply to the enclosed internal volume, whereas the definition for ambient air is slightly more complex.

Ambient air is essentially dry air with water vapor, and this affects the ion transport that governs gas conductivity. Modeling of the conductivity of ambient air in air was found from the works by Saltzer et al. [77] and Löfås et al. [78] with a recombination rate of $R = \frac{n^2}{S}$, where S is an ion generation rate of 1.6×10^7 IP/(m^{3}s), and ion mobilities of 1.6×10^{-4} m^2/(V·s), respectively. The effect of water molecules in the air is that they cluster around light ions to form heavier and slower ions that recombine faster [79]. The ion-ion recombination rate in air for a given moisture can be given as Equation 5.1.

$$R_0(H) = R^0 \left(1 + 14\frac{RH}{100}\right) \tag{5.1}$$

Where $R_0 = 2 \times 10^{-12}$ m^3/s [79] and RH is the relative humidity. This resulted in a gas conductivity that was in the order of $1 \times 10^{-16}[S/m]$, which is in the lower range of estimated conductivities for ambient air[78]. Figure 5.10 shows the simulated steady-state ion concentrations at + 30 kV DC.



(a) Steady state positive ion distribution

(b) Steady state negative ion distribution

Figure 5.10: Ion concentrations under steady-state DC for the test cell given applied +30 kV DC

As seen in the plots, ion drift results in deposition and collection at the interface between the flange and plexiglass. It is observable that there are more available that the inside volume of gas has high ion generation but similarly small active volume, resulting in very low gas conductivity in the range of 1×10^{-17} [S/m] to 1×10^{-18} [S/m]. Outside the cell, the ion concentration is much higher, and therefore the effective conductivity is much lower at around 2×10^{-16} [S/m]. Figure 5.11 shows the electrical conductivity across the gas volumes given 3 bar of dry air and ambient air. Figure 5.12 shows the charge accumulation on all insulating surfaces in the enclosure.

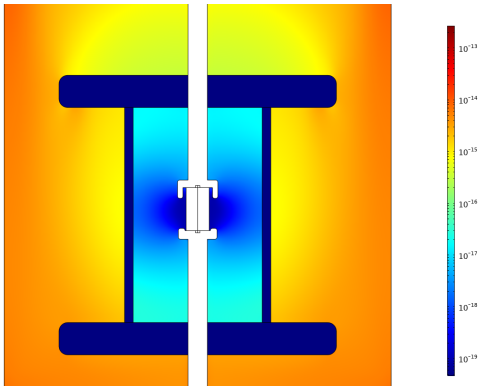
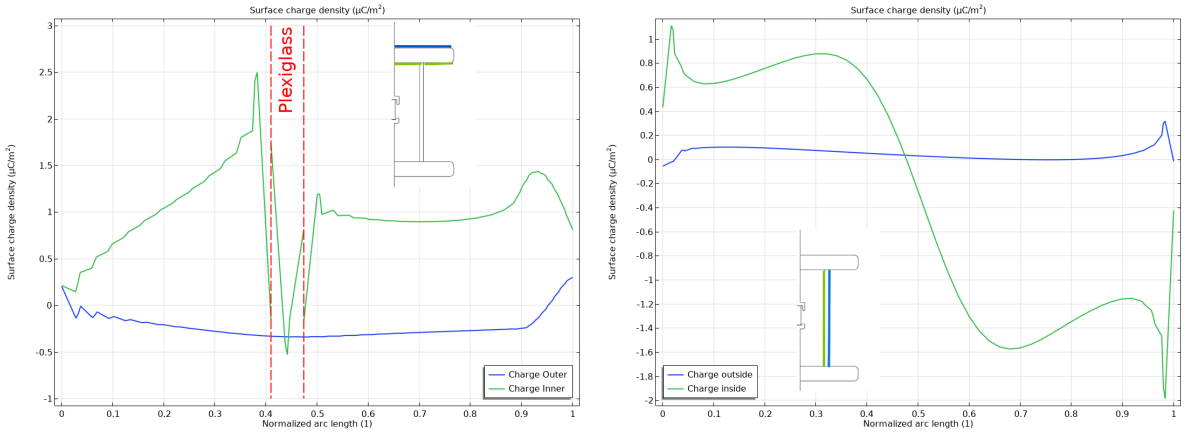


Figure 5.11: Floating Cell gas conductivity



(a) Nylon flange

(b) Plexiglass

Figure 5.12: Surface charge across the inside and outside of all insulating materials for +30 kV DC

As seen in the plots above, charge accumulation can be either positive or negative depending on the field lines and which current component dominates. For the nylon flange, the highest charge accumulation occurs at the intersection of the upper flange curve, with a peak of 2.5 $\mu C/m^2$. The field on the outside of the spacer appears very low, with a peak of 0.28 kV/mm attributed to the low normal component on the spacer surface. On the plexiglass, the inner surface exhibits a charge that peaks at -2 $\mu C/m^2$ at the flange intersections. It is clear that the charge deposited depends on the normal component of the electric field on the material, and, given the low electric field, insulating materials accumulate less charge than the spacer. It can therefore be concluded that the effects of the charges do not greatly change the field profile across the electrodes. The test setup can therefore be seen as sufficient for testing composite DC/LI voltages up to 30/ 150 kV, respectively.

6

Test Circuit Design

Taking the final step outwards results in the realization of a test circuit capable of applying the composite DC/LI voltages. As mentioned in Appendix A, the test circuit must be defined and calibrated to generate a 1.2/50 μs LI waveform using the equipment available at TU Delft, with appropriate protection elements to prevent the influence of one HV source on the other. The goal of the section is to consider and select a circuit that can be built at TU Delft to supply the required DC/LI test voltages. An overview of the test circuit to be implemented is given in Figure 6.1.

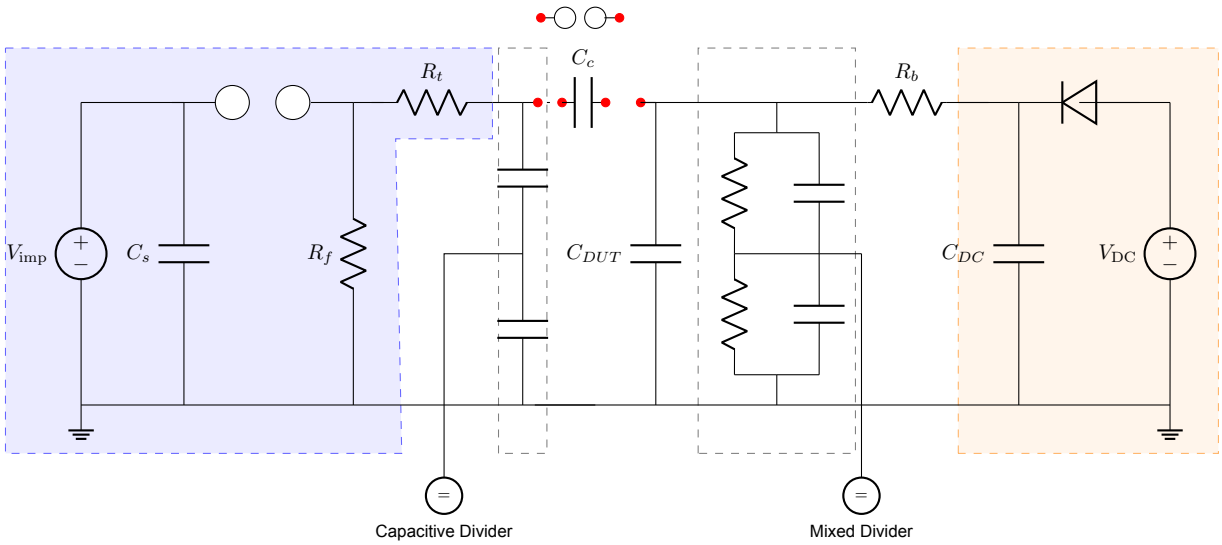


Figure 6.1: DC/LI composite test circuit, Blue represents Impulse generator, Orange represents DC source, and the dashed sections represent the used dividers

Given the circuit above, there are several challenges in implementing it, including effectively generating the impulse with correct LI time parameters, the choice of blocking on the DC and LI sides, and measurement options. The section below further describes these challenges.

6.1. Equivalent Model

The equivalent model of the components used in the lab for simulation is essential for understanding the behavior of composite voltages. The list below shows the equivalent models used and the simplifications made for each.

- The equivalent of the Homemade capacitive divider in the lab used in the simulation is 500 pF. Any additional stray capacitance to ground is determined empirically by parameter matching an impulse waveform to a circuit with the additional capacitance.
- The equivalent of the Northstar VD100 mixed divider available in the lab is 1600 MΩ and 25 pF. The model is only considered for the superimposed voltage measurements.
- For the sake of simplicity, the DC generator is represented as an AC voltage source connected to a diode with a capacitor in parallel. The model simplification is chosen because the main goal is to obtain a DC voltage with low ripple as input to the composite circuit.
- A single-stage impulse generator is intended for use at the TU Delft lab, and its equivalent model can be used. Two possible models, ”a” and ”b” circuits, can be used as equivalent models [56]; however, this paper uses the ”b” model as seen in Figure 6.2 below.
- The spark gap is slightly more complicated to implement, as there is no native LTSPICE model, and it presents nonlinear triggering and extinguishing behavior based on the voltage difference. A simple voltage-based switch oversimplifies the spark gap's behavior, as it remains conducting for a fixed duration, independent of the spark gap breakdown voltage. A detailed D flip-flop-based conditional statement model for the spark gap is used, following the work of Hawley Hobbies [80].

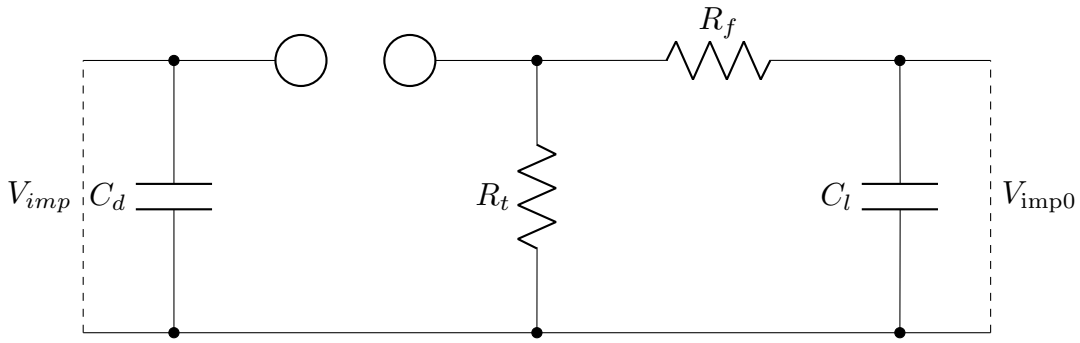


Figure 6.2: Equivalent impulse ”b” circuit considered for simulation

6.1.1. DUT Equivalent Parameters

To obtain the equivalent circuit parameters of the electrodes and the complete test cell, a COMSOL electrostatics simulation was performed, including the computation of capacitance and resistance. The energy of the system was computed and then given as in Equation 6.1.

$$C \approx \frac{2W}{V^2} \tag{6.1}$$

COMSOL automatically evaluates the capacitance using the Maxwell capacitance expression, yield-

ing approximately 0.612 pF. The computed capacitance is also slightly higher than the capacitance approximation for a parallel-plate capacitor with the same area and gap distance. The leakage resistance was also determined by applying a DC voltage and measuring the leakage current along the spacer surface, yielding an approximate resistance via Equation 6.2 below.

$$R \approx \frac{V}{I_{leak}} \tag{6.2}$$

The leakage resistance is determined as roughly 1.8 GΩ for PTFE and 1.2GΩ for nylon, which can be effectively ignored in the following circuit. The data here is then used to define the test circuit and to calculate relevant efficiencies and time parameters.

6.2. Optimizing Impulse Parameters

The goal of optimizing the impulse parameters is to maximize impulse efficiency at the output while meeting the 1.2/50 μs requirement within the 30% allowable tolerances as defined in IEC 60060-1 [81]. The impulse generation is below 200 kV; hence, a single-stage generator equivalent model was chosen, with the equivalent B-type circuit considered for analysis, as mentioned in Section 6.1. The parameter optimization is also limited because the impulse source capacitance C_d and the load resistance R_l are fixed. The definition of the standard lightning impulse as a double exponential, along with the relevant time parameters, is presented in Equation 6.3 below, as per IEC 60060-1 [81].

$$v(t) = \eta \frac{\tau_2}{\tau_2 - \tau_1} \left(e^{-t/\tau_2} - e^{-t/\tau_1} \right) \tag{6.3}$$

$$\tau_1 = R_f \frac{C_d C_l}{C_d + C_l} \qquad T_1 = 2.96\,\tau_1 \tag{6.4}$$

$$\tau_2 = R_t (C_d + C_l) \qquad T_2 = 0.73\,\tau_2 \tag{6.5}$$

$$\eta = \frac{C_d}{C_d + C_l} \left(1 - e^{-\frac{C_d + C_l}{C_d C_l R_f}} \right) \tag{6.6}$$

The front of the impulse is dominated by the discharge of capacitance C_d through R_f into the load capacitance C_l. The front time of the impulse can be effectively increased through either increasing C_l or R_f. The tail time is similarly defined through the slow discharge of both capacitances C_d and C_l through the tail resistor R_t. The tail time can therefore similarly be increased by increasing either C_l or R_t. The impulse efficiency is a function of the system's load capacitances and represents the fraction of the supplied voltage that reaches the output.

A few parameters of the circuit, such as inductances in the cables and the stray capacitance, were determined by recording an LI waveform of +20 kV and sweeping possible C_{stray} and L_{cable} in LTspice; these were determined at 0.225 nF and 7 nH, respectively.

There are 2 scenarios considered in which only impulses or DC/LI are applied, with different effective load capacitance observed at the output of the impulse generator. There is therefore a range of acceptable R_f and R_t values that result in an IEC-compliant waveform. The values of the load for only the impulse circuit are calculated as $C_{stray} + C_{CapDiv} + C_{DUT}$ at roughly 0.731 nF. The superimposed test also introduces a 25 pF mixed divider, bringing the total to 0.756 nF. The acceptable ranges for the R_f are presented in Figure 6.3 and the chosen resistance value for both tests was 512 Ω

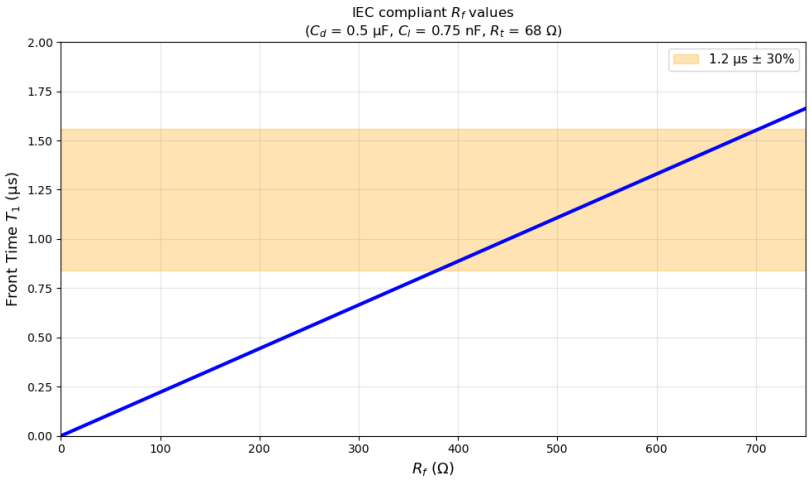
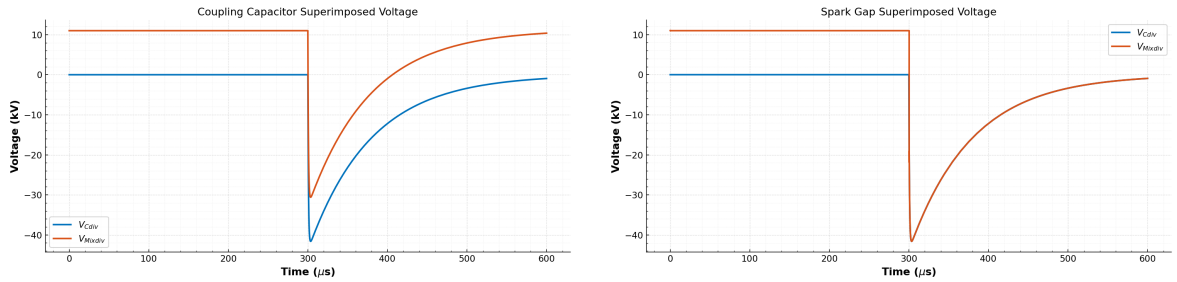


Figure 6.3: Acceptable values of R_f to achieve a IEC standard Lightning impulse for the given C_L

6.3. Choice of Impulse Coupling

In an ideal scenario, the coupling at the impulse should ensure that no DC component arrives at the output of the impulse generator. As mentioned in Appendix A, the 2 methods of protection include coupling capacitance and a spark gap. Both methods have valid uses, with the coupling capacitor more often chosen to avoid the probabilistic behavior of the spark gaps [12, 82].

The choice was made to initially use a spark gap due to problems with discharging large capacitors at TU Delft and concerns about the lack of a mixed divider capable of measuring the test voltages across the entire defined test range, as shown in Section 7.2. Testing was later performed under 1-bar test conditions with a coupling capacitor, as explained in Section 8.3. The section dimensions for both scenarios can be chosen based on the availability of future equipment and measurement needs. Figure 6.4 below shows the fundamentally different waveforms applied through both a coupling capacitor C_c and a spark gap, with +10 kV DC and a -50 kV impulse.



(a) Coupling Capacitor = 10 · C_{DUT}

(b) Spark Gap

Figure 6.4: LTspice simulations of the superimposed circuit from Appendix D for both Coupling elements . Note that spark gap extinction was set to 0.001 V_{imp}

The physics of both capacitors and spark gaps leads to different waveforms, but in principle, the DUT faces a transient that recovers to the DC value. It can also be observed that an impulse generator with a higher applied voltage must be used for the coupling capacitor to achieve the same effective superimposed voltage for opposite-polarity waveforms.

6.3.1. Coupling Capacitor

The design of the coupling capacitor C_c is preferred because the waveform does not experience any chopping or retriggering, as noted by M Hallas et al. [82]. The coupling capacitor, when considered, acts as a capacitive divider with the equivalent C_{eq} defined below.

$$C_{eq} = C_{DUT} + C_{MixDiv} \tag{6.7}$$

$$\frac{\eta'}{\eta} \leq \frac{C_c}{C_c + C_{eq}} \tag{6.8}$$

$$\therefore C_c \geq \frac{\eta'}{\eta - \eta'} C_{eq} \tag{6.9}$$

where η' represents the efficiency of the impulse peak at DUT and η represents the efficiency peak at the output of the single-stage impulse generator from before. The goal in choosing a coupling capacitor should be to maximize η' up to η using the available components in the lab. Figure 6.5 below gives the impulse efficiency at the DUT η' as a function of the coupling capacitor C_c sizes.

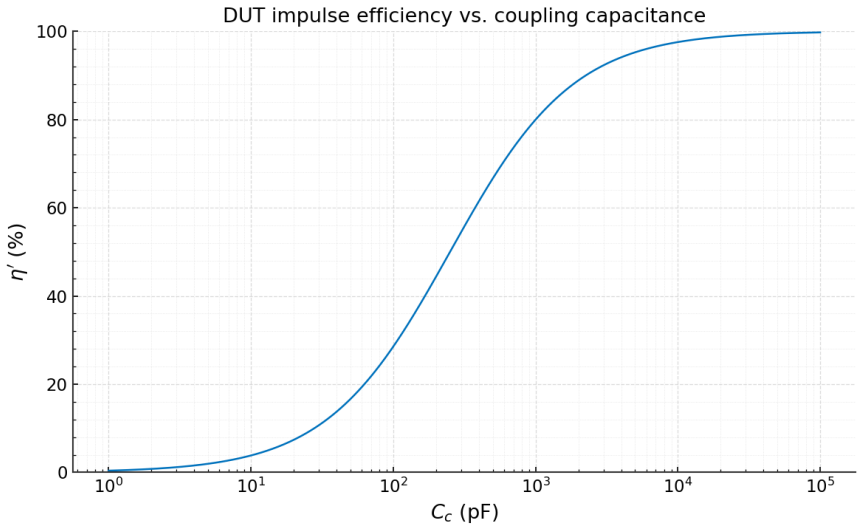


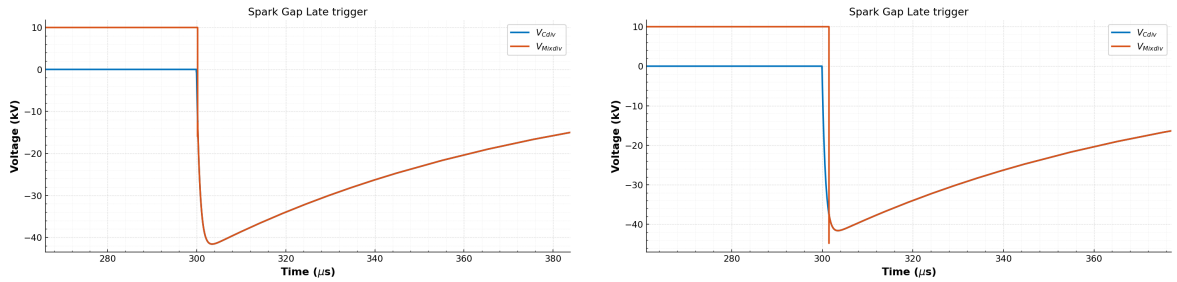
Figure 6.5: DUT impulse efficiency vs Coupling capacitor C_c size

The main drawback in using a coupling capacitor is that they alter the waveform at the DUT, meaning that a suitable divider is needed that can measure both the DC and LI voltages across the expected test range without the option of being able to individually measure each HV source and combine them as given in Appendix A. Given the test object's small capacitance, the coupling capacitor size was not a major issue; however, the rated voltage was. DC bias also means that the energy stored in capacitors after a test must be discharged, which can cause large sparks at sufficiently high voltages when the capacitors are touched with low-impedance earthing sticks.

6.3.2. Spark Gap

The use of the spark gap is considered simpler for implementation; however, it presents a few issues that must be addressed. The spark gap operates by isolating the HV sources until the voltage difference across the gap, $|U_{imp}| - |U_{DC}|$, exceeds the gap's breakdown voltage. When the gap triggers, a low-impedance arc forms, and the impulse is applied to the DUT until the arc is extinguished. The spark gap, however, introduces 2 major concerns that need to be addressed: capacitive and mixed-divider waveform alterations.

When the voltage across the spark gap is above the breakdown, the DUT voltage immediately begins following the applied impulse, and a high dV/dt signal is viewed from the DUT. The steep dV/dt is a signal of very high frequency and, due to the circuit's inductances and capacitances, produces overshoot. Evaluation of T1 times across waveforms is done by choosing the $T_{30\%}$ and $T_{90\%}$ times as mentioned in Appendix A and can be significantly distorted based on when the trigger voltage is set. The Figure 6.6 demonstrates this phenomenon simulated in LTSpice.

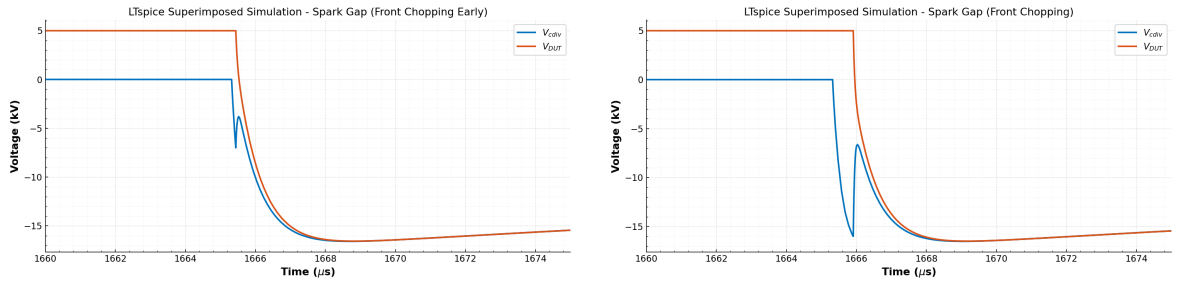


(a) Early spark gap breakdown 12.5 kV

(b) Late spark gap breakdown 35kV

Figure 6.6: LTspice simulations of both the dividers

The second challenge for spark-gap-based circuits is if the ratio between the load capacitance of the impulse generator and the capacitance of the DUT is too large. The spark gap triggering creates an essentially short circuit, causing the impulse to see another capacitance in parallel. If the DUT capacitance is too large, the voltage on the LI divider drops to compensate. The effect of pulling down can result in inaccuracies in T1 time evaluations, and the chopping severity depends on the size of C_{DUT} relative to C_l. Figure 6.7 below shows the effect of C_{DUT} on the chopping.



(a) Spark gap trigger at 7 kV, $C_{eq} < C_{Cdiv}$

(b) Spark gap trigger at 7 kV, $C_{eq} > C_{Cdiv}$

Figure 6.7: LTspice simulations of the spark gaps, including front chopping, based on different breakdown times for an assumed test capacitance of 2nf

It is known that the capacitances of the divider and test object add up to 25.6 pF, which is smaller than the capacitive divider, and therefore chopping is not a significant expected effect. Figure F.2 shows the effect of different load capacitances on the drop measured on the capacitive divider.

The CIGRE TB842 [12] also specifies that the spark gap breakdown should be set before 80% of the LI peak, but should be adjusted lower based on the distortion to the waveshape. It can be noted that for the same polarity superposition, the voltage difference allows for less variation in trigger voltages. The definition of the minimum impulse magnitudes for both polarity superimposition can be given as shown in Equation 6.10

$$\text{Same polarity: } \Big\{ U_{imp} > 2U_{DC} + \Delta U \qquad \text{Opposite polarity: } \Big\{ U_{imp} > U_{DC} + \Delta U \tag{6.10}$$

Where ΔU is an additional safety margin that should be kept as low as possible. Due to the simplicity and potential constraints of the mixed divider, the spark gap was initially implemented for testing at TU Delft as shown in section 7.2.

6.4. Choice of DC Blocking

Blocking high-frequency transients from the DC source can only be done with a sufficiently large resistance, as it then acts as a low-pass filter with the DC source capacitor, attenuating the impulse, which has frequencies in the MHz range. The cutoff frequency of the DC low-pass filter is given by Equation 6.11 below.

$$f_{cutoff} = \frac{1}{2 \cdot \pi \cdot R_b \cdot C_{DC}} \tag{6.11}$$

The range of cutoff frequencies typically yields values on the order of 10^2 Hz. The selection of the blocking resistance R_b is also based on the operational limits of the DC voltage generator and the required impulse performance at the DUT. As previously mentioned, a higher R_b blocks more of the impulse from being observed at the output of the DC generator, but also reduces the charging current available to the DUT, given by $\tau_{charging} = R_b \cdot C_{DUT}$. If the choice of R_b is too low, a significant percentage of the impulse appears at the DC source output, which can cause unwanted damage. The choice of R_b must therefore consider,

1. Limiting the impulse voltage stress on the DC power supply and filter capacitor.
2. Avoiding excessive DC voltage drop when charging.

To protect the DC source, the impulse must be attenuated by the blocking resistor. The voltage across the capacitor in the DC supply is given by Equation 6.12 below.

$$U_{C_{DC}}(t) = U_{\text{imp}} \left(1 - e^{\frac{-t}{R_b \cdot C_{DC}}}\right) \tag{6.12}$$

To protect the DC generator, the voltage across C_{DC} must not exceed a fraction $U_{\text{Imp}\%}$ of the impulse peak voltage at the half peak time T_t. The constraint can be given below, with the minimum bound given by

$$U_{C_{DC}}(T_t) \leq U_{\text{Imp}\%} \cdot U_{\text{imp}} \tag{6.13}$$

$$U_{Imp\%} \leq 1 - e^{-T_t / R_b C_{DC}} \tag{6.14}$$

$$R_b \geq \frac{T_t}{C_{DC} \ln\left(\frac{1}{1 - U_{\text{Imp}\%}}\right)} \tag{6.15}$$

For $U_{\text{imp}\%} = 0.5\%$ with a $C_{DC} = 25$ nF, the required minimum blocking resistance from the circuit above becomes

$$R_b \geq 400 \text{ k}\Omega$$

The voltage drop across the blocking resistor should be minimized to maximize the voltage on the DUT. For the sake of simplicity, the equivalent voltage across the DUT is ignored, and a series voltage division can be observed with R_b and R_{rcd}. The upper limit for the blocking resistance can therefore be determined by

$$U_{R_b} = U_{DC} \frac{R_b}{R_b + R_{MixDiv}} \tag{6.16}$$

$$\frac{U_{R_b}}{U_{DC}} \leq U_{Drop\%} \tag{6.17}$$

$$\frac{R_b}{R_b + R_{MixDiv}} \leq U_{Drop\%} \tag{6.18}$$

The equation can be solved for R_b to give the Equation 6.19 for the upper bound below.

$$R_b \leq \frac{U_{Drop\%}}{1 - U_{Drop\%}} R_{MixDiv} \tag{6.19}$$

For $U_{Drop\%} = 0.5\%$ and a $R_{MixDiv} = 1600\ M\Omega$ the maximum permissible blocking resistance is

$$R_b \leq 8.0\ \text{M}\Omega$$

Given that the final resistance is on the order of a few MΩ, the choices of HV resistors in the lab are limited. The HV resistors in the lab must also withstand both DC and LI, which is a problem for certain inductively wound resistors, where the impedance would collapse under high-frequency transients. The choice was then made to use demi water-filled 1-meter resistors, which were capable of reaching values up to 10 MΩ. The simulated netlist of the circuit for generating composite voltages in LTspice is given in Appendix D.

Part III Verification

7

Experimental Setup

This chapter describes the setup and test methodology used to verify the simulated and designed test circuit from Chapter 4, Chapter 5, and Chapter 6 for surface flashover under composite DC/LI voltages. Before testing, the cell's mechanical adequacy had to be confirmed, steps defined to ensure repeatability, and a test procedure established for each experiment.

7.1. Manufacturing of the Cell

The cell and electrodes were manufactured by the TU Delft HV lab. The electrodes were made from stainless steel for its mechanical strength and chemical resistance, fitted with an M6x14 mm thread for easy mounting, and surface-polished to minimize field enhancement and charge injection. They also included a 4 mm divot to mechanically align the spacer, with the mount later changed to a screw design based on the results in Section 8.1. The spacers were manufactured from nylon and PTFE. Figure 7.1 shows the manufactured top and bottom electrodes with the spacer.



(a) Top Electrode



(b) Bottom Electrode



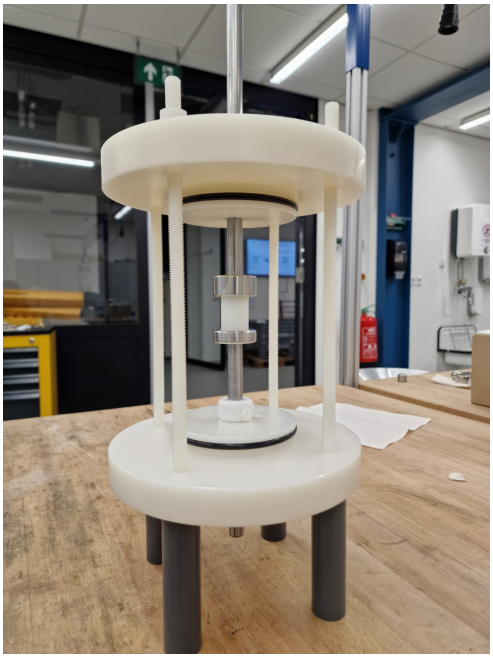
(c) Initial Nylon Spacer

Figure 7.1: Manufacturing of the electrodes and spacer done by the HV lab of TU Delft

The test cell was manufactured by the HV lab as per the CAD design in Figure 5.4. It is kept gas-tight at the conductor entrances via O-rings in the top and bottom flanges, with the conductors having a possibility of connection with either banana clips or crocodile clamps. The cell consists of a few different components labeled as shown in Figure 7.2a.



(a) Complete cell



(b) Cell without Plexiglass

Figure 7.2: Manufactured test cell with and without Plexiglass annotated

As seen in Figure 7.2a, the HV electrode **(1)** is stainless steel and is fed through the nylon flanges **(3)**. The flanges have 4 threaded holes where support rods **(6)** are passed through and tightened with nylon bolts **(2)**. The plexiglass wall **(4)** is mounted on the HV flange with O-rings, maintaining the flange separation. The test electrodes **(5)** are held with a nylon screw **(7)**. The chamber is pressurized

and depressurized by the DILO valve **(8)**, and the gas pressure is measured through a gauge **(9)**.

The cell is disassembled by loosening the holding screws and removing the nylon bolts at the top. Given the O-ring seal, a strong force is required to pull the top flange apart. The initial design required ensuring sufficient clamping before the placement of the plexiglass; however, this was later changed to allow for ratcheting clamping of the electrodes and spacer, as further explained in Chapter 8. The test cell must first be depressurized to 0.4 mbar for 30 s before filling as specified by CIGRE TB 849 [83] for non-fluorinated gases. The filled gas can then be measured based on the pressure reading. A 10 minute wait time was then set for the homogenization of the gas mixtures. The test cell was pressurized to 3 bar and left overnight to ensure no significant leakage and that the structure could withstand the pressure. The cell lost negligible pressure and showed no signs of damage, indicating it could contain non-fluoridated pressurized gases up to 3 bars.

7.1.1. Testing Preparation

To ensure consistent procedures, three steps were taken before testing. The electrodes were cleaned with Brasso ™ polishing solution to remove oils and particulates that could possibly enhance the field and introduce variability. Electrodes and spacers were always handled with gloves and cleaned with propanol and a fine microfiber cloth before every experiment, then dried for at least 1 minute before installation. Any carbonization marks on the spacer required cleaning, sanding, or replacement.

For the initial clamping mechanism, each nylon nut on the top flange was tightened at least 15 times; this was later changed to a screw-through mechanism with a torque wrench ensuring at least 2.2 Nm, as described in Chapter 8. The gap distances were always verified with a spark gap separation tool before every test, and the ambient lab conditions were recorded to correct all measured flashover voltages, as given in Appendix E.

7.1.2. Camera Setup

The camera setup must account for the cell's rotational symmetry, as surface flashover can occur on any side. A single camera captures at most half the spacer surface, so two mirrors were placed in the camera's field of view behind the cell to capture an almost 360 degree view. The figure below shows a top-down view of the setup.

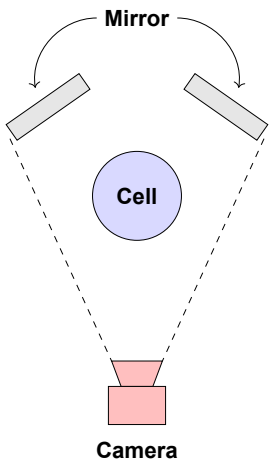


Figure 7.3: Camera placement to capture surface flashovers on all sides

Given the single camera constraint, the depth of field can significantly affect the mirrored images; the solution is to place the camera as far away as possible and zoom in to reduce relative depth differences between the object and the mirrors. Reducing ambient lighting also improves flashover visibility, with Figure 7.4 showing an example image taken.

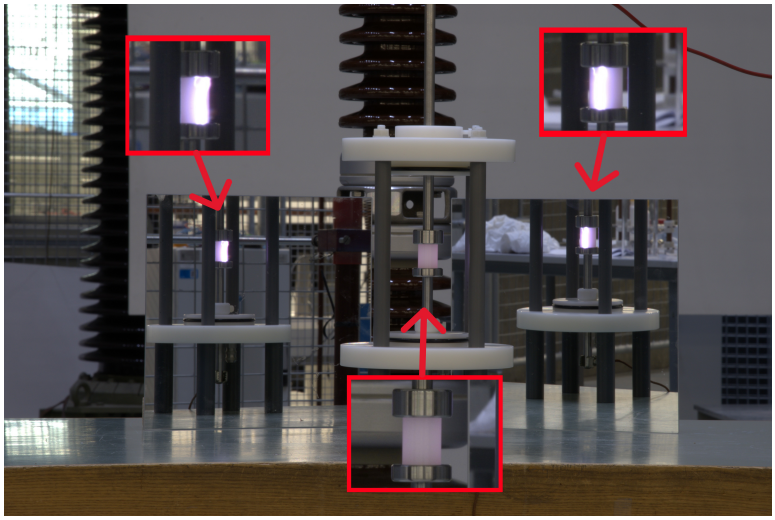


Figure 7.4: Example image showing flashover location being captured by the mirrors

A fundamental constraint is that the camera is not fast enough to capture the development of flashover, so detailed conclusions about initiation and propagation cannot be drawn. The setup is, however, seen to have sufficient resolution to determine flashover location and distinguish surface from gas-gap flashover.

7.2. Testing Definitions

The primary goals of this work are the verification and validation of the designed test cell, which requires a defined methodology for aspects such as charge and voltage before quantitative testing. This section describes test methodology from the literature, the methodology used in this work, and a process for future researchers.

7.2.1. DC Charge Testing

The goal of the DC charge testing is to verify that the charge accumulated on the surface was comparable to the simulations and to improve the simulation-based results to more closely match the laboratory conditions. The test is performed by applying a DC voltage for 2 hours at 10 kV and then using a Trek model 341B electrostatic voltmeter to measure potential across 3 points on the spacer surface. Figure 7.5 and Figure 7.6 shows the test setup.

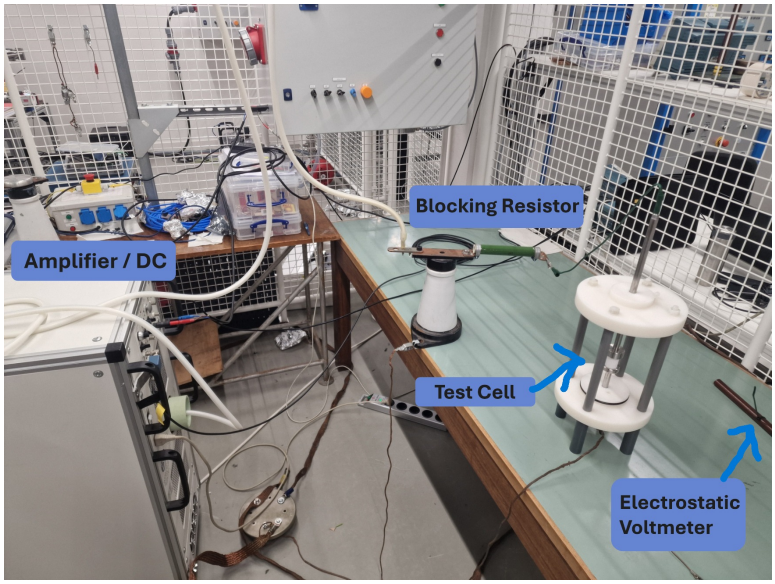


Figure 7.5: Test circuit of DC charge measurement tests

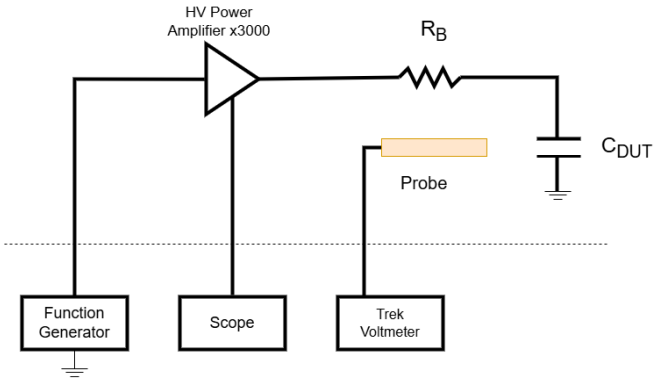


Figure 7.6: DC charge measurement test schematic

A 3455ET probe and holder with ± 1 V accuracy and range of 20kV was used, and the measured potential is compared to the simulated surface charge in ambient air Chapter 5. The probe and voltmeter operate on the vibrating Kelvin principle, resulting in the tip of the probe being brought to a high voltage. Sufficient precaution was taken while handling the probe, and it is recommended that 2 people be operationally present for any measurement.

Several constraints limited the measurement accuracy and the conclusions drawn. Given the available time, probe size, and difficulty in quickly disassembling the cell, ambient air was used rather than a dry-air-filled cell.The metal shielding and ground electrode limited the effective measurable surface to 7-38 mm across the 40 mm spacer length. The probe and holder diameters of 1.52 mm and 20 mm further limited measurements to 17-28 mm, as shown in Figure 7.7. The holder was also susceptible to

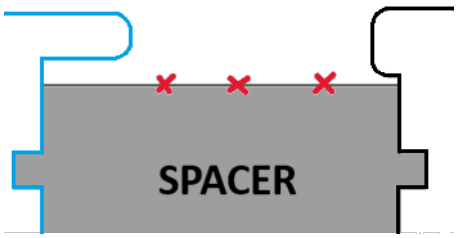


Figure 7.7: Annotated charge measurement points across spacer surface

noise due to hand shaking and the need to hold the probe perpendicular to the spacer surface. The tests were repeated 4 times due to limited time, with 3 measurements at 17 mm, 22.5 mm, and 28 mm, taken for all 4 sides in succession.

It is important to acknowledge that these conditions do not provide perfectly accurate surface charge distributions; rather, they verify that the polarities, shapes, and magnitude differences relative to the simulation fall within the expected range. The charge results are given in Section 8.2.

7.2.2. LI Procedure

For reference, in the DC superimposed stresses case, only an impulse waveform is applied, and the Lightning breakdown U_{50} is estimated. It is proposed that future pursuers of the work plot a quadrant diagram similar to Figure 3.8, where the x-axis is the prestress voltage or time, and the y-axis is the superimposed flashover voltage with respect to earth. A review of the limited body of literature reveals multiple test methods with different procedures, assumptions, and levels of statistical certainty. The following sections will evaluate the test methods for the LI used to motivate choices for this and future work. The test circuit used only for the Lighting impulses, along with the labeled components, is shown in Figure 7.8 and Figure 7.9 below.

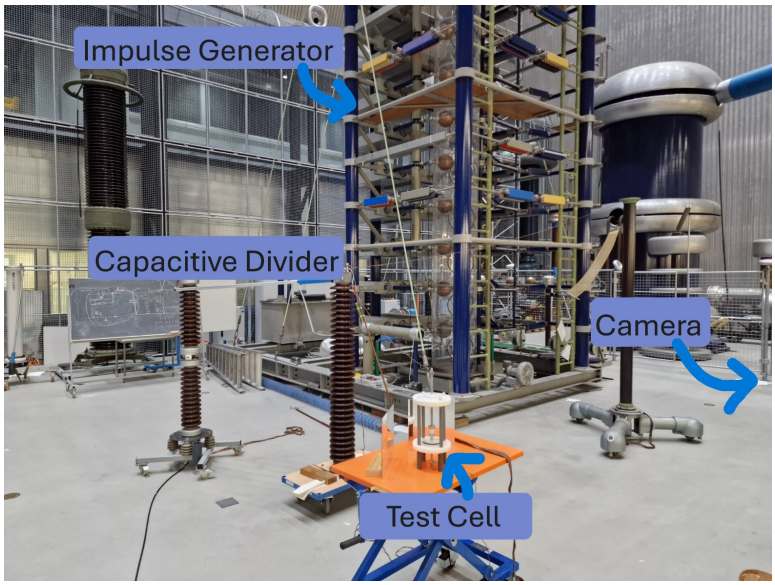


Figure 7.8: Test circuit used for LI testing with labeled components

A single stage of the Marx generator is used for the test voltages, with an equivalent homemade 500 pF capacitive divider with a divider ratio of 258 V :1 V.

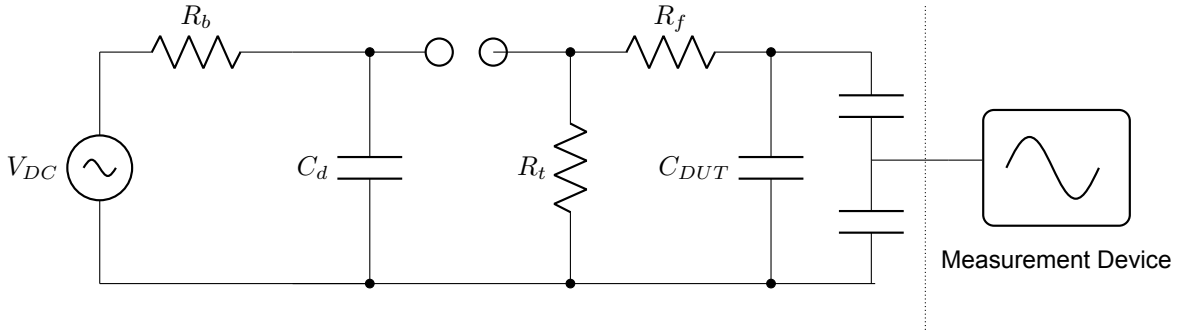


Figure 7.9: LI breakdown testing schematic

Up and Down Method

The up-and-down method is the most widely adopted procedure for estimating the probability of breakdown voltage of self-restoring insulation under LI stress, as specified in IEC 60060-1 [81]. The methods consist of stepping the applied LI voltage up by a ΔU of up to 3% of the expected U_{50} while maintaining the voltage withstand, and reducing it upon a breakdown event. It is recommended that at least n = 20 trials be conducted to obtain a sufficiently large sample size [84]. The aim is that, for independent voltage-application events, the breakdown voltage oscillates around a specified 50% breakdown voltage U_{50}, defined as the mean of all applied impulse voltages during the test. The statistical handling of the data is shown in Appendix E, and the test method is shown in Figure 7.10.

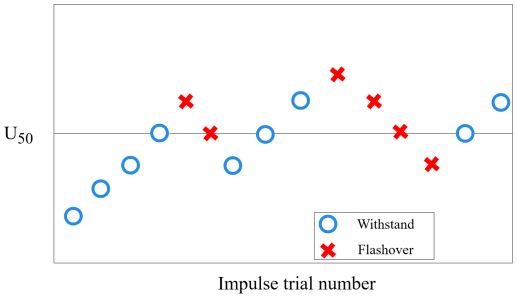


Figure 7.10: Up and down test procedure [81]

The up-and-down method has been applied in several superimposition studies [48, 82, 85], where the implicit assumption is that surface charge redistribution induced by preliminary non-breakdown impulse applications does not affect the results. In real DC GIS type tests, a system either withstands or breaks down at a given rated DC and impulse voltage, with no conclusion drawn about changes in the system's breakdown voltage [12]. The time constant of fast transients such as impulses or polarity reversals is in the order of 100 μs, which is much smaller than the time constant of surface charge accumulation, effectively making the charge accumulation stationary for impulses [86]. Repeated breakdown impulses may subsequently cause damage and carbonization of the spacer or electrode surfaces, which can affect the insulation strength of successive impulses. For preliminary testing, this method is chosen because it is simpler to perform than the others and because the lower voltage levels do not cause sufficient damage to the spacer. However, for quantitative future measurements, it is not recommended to use this method.

Single Discharge Method

The second approach encountered in the literature [47, 58, 87] involves applying a single LI impulse with a magnitude of approximately 1.2 times the expected U_{50} breakdown voltage, thereby ensuring a high probability of breakdown on first application. The test is then repeated at the same voltage for 5 trials. The stated motivation for this approach is to eliminate the influence of preceding non-

breakdown impulse applications on the surface charge state and subsequent breakdown behavior. The test method is shown in Figure 7.11.

The statistical validity of this method is further questionable on several grounds. The test functions like a multiple-level test described in IEC 60060-1 [81]; however, only one voltage level is tested. The method for determining the expected U_{50} is not defined and would require a separate approach. In the referenced works, 5 tests were conducted per level, which further limits the statistical confidence of the conclusions that can be drawn. Due to the poor explanation of the method and results, which cannot be used to determine a U_{50}, this method was not chosen.

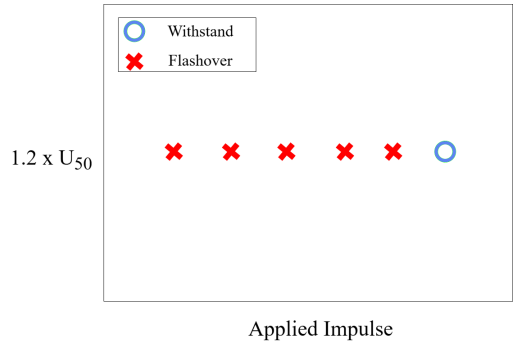


Figure 7.11: Single discharge method

Progressive Step Method

The Progressive stress procedure, as described by Hauschild et al. [88], involves the sequential application of impulses until a breakdown occurs, with the breakdown being imminent while the voltage magnitude is the random variable. A starting voltage v_0 is chosen low enough to withstand the fixed step size. The procedure is repeated multiple times, and an estimate of U_{50} can be made. The method is considered, as it is designed for non-self-restoring insulation and does not account for the influence of previous damage. The work by Wilson et al. [89] provides a more comprehensive method for evaluating breakdown voltages and times for non-restoring insulation, which is recommended for use.

The progressive stress test has been used in many DC/LI studies, including [49, 90]. The method used does not suffer from the same problems as previous methods, in which impulses affect subsequent trials, and is clearly defined to ensure repeatability. The only problem with using such a method is the time-consuming nature of having to both depressurize and empty the setup, clean/ replace the spacer after every flashover attempt. The independence of each test also allows the breakdown voltages and breakdown times for each test can be analyzed and fitted using a Weibull distribution [89]. Therefore, it is proposed to use this method for future testing of different gases and gas pressures, with a recommendation from IEC 60060-1 [81] to collect a minimum of 10 breakdown trials for the standalone LI tests .

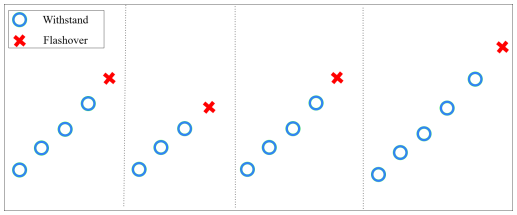


Figure 7.12: Progressive stress test procedure [88]

7.2.3. DC/LI Procedure

The goal of the DC/LI section is to first verify that the designed test circuit can be implemented and what precautions and limitations exist to measure the DC/LI superimposed waveform in reality. The process for conducting superimposed DC/LI testing, as outlined in the section above, is given below. The Figure 7.13 and Figure 7.14 show the implemented test circuit from Figure 6.1 with labeled components used for DC/LI verification in the TU Delft lab.

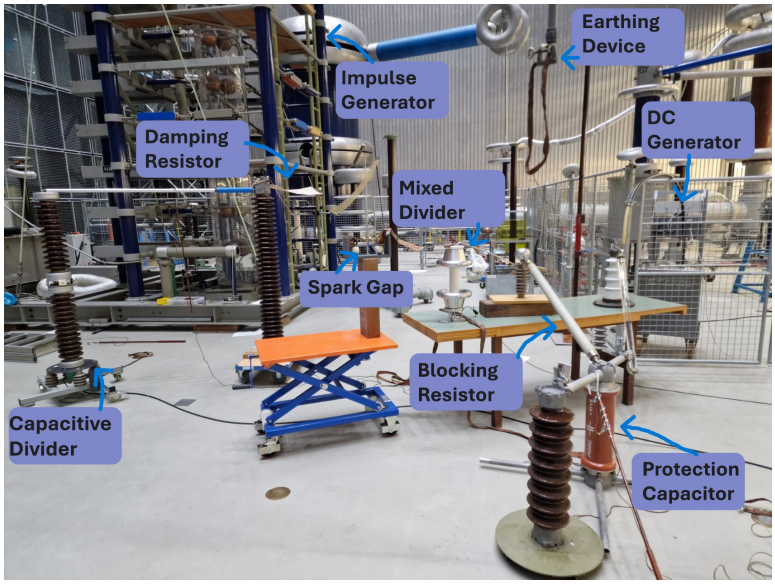


Figure 7.13: Spark gap test circuit used for DC/LI testing with labeled components

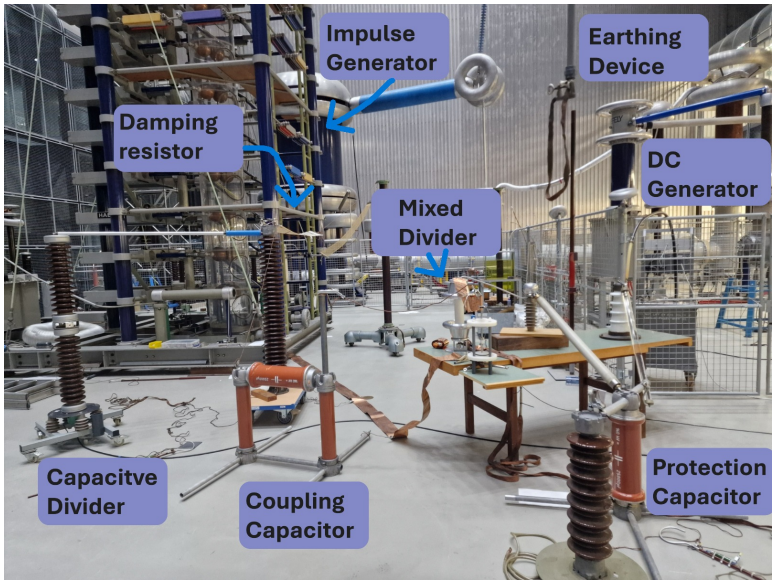


Figure 7.14: Coupling Capacitor test circuit used for DC/LI testing with labeled components

The testing for DC/LI consists of two sequential phases. Firstly, the DC voltage is raised to the target prestress level at a ramp rate of 1 kV/s. The voltage is then held for a prestress time of 2 hours as specified in CIGRE TB842 [12]. The impulses are finally applied according to the progressive step method described in the section above, and a breakdown concludes the trial. The gas must be depressurized, and the system must be cleaned before the test can be repeated. Due to the time-consuming nature of the tests, it is recommended that future researchers run at least 10 trials for each changed variable [81]. The comprehensive testing procedure is given in the Figure 7.15 below.

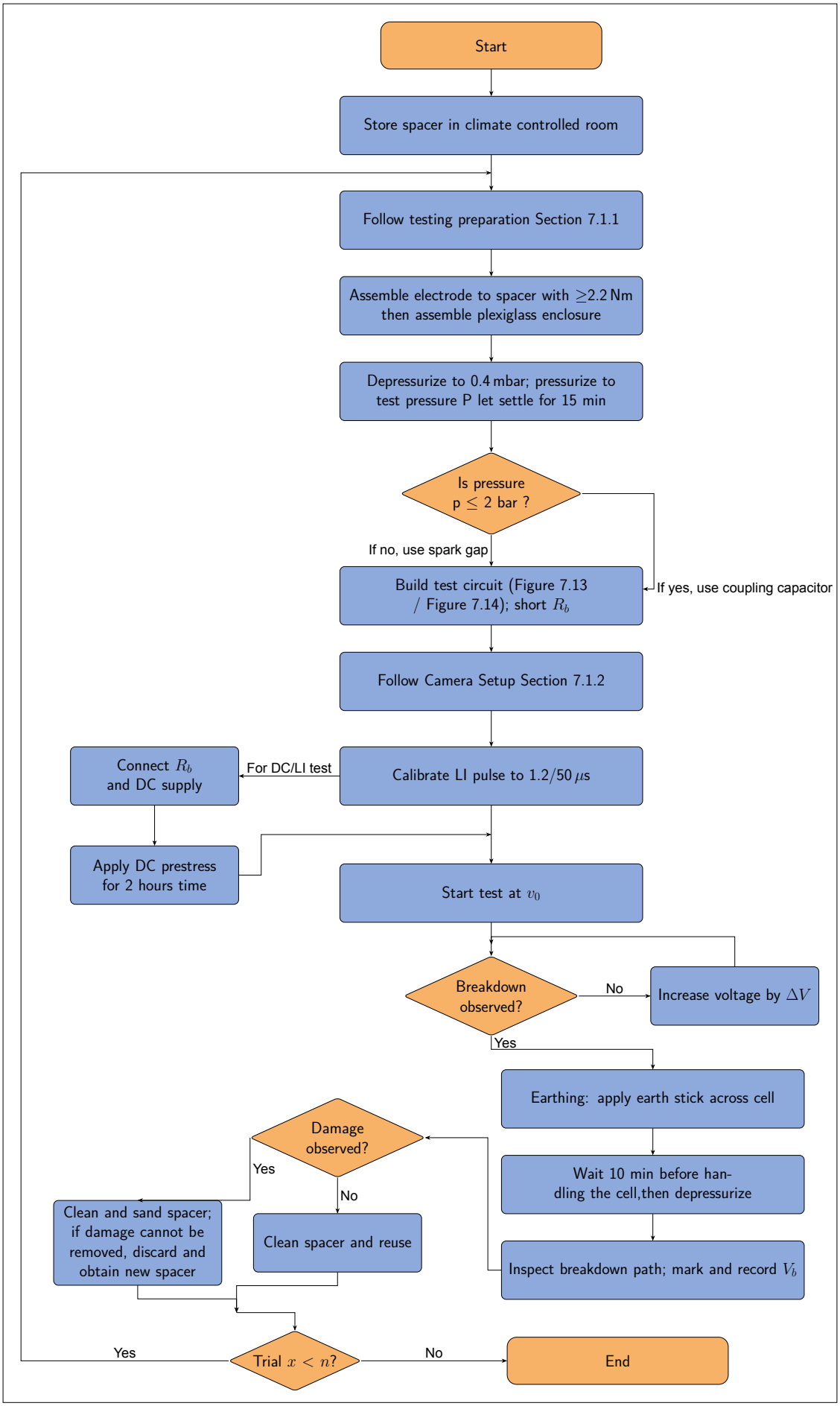


Figure 7.15: Flowchart for LI and composite DC/LI spacer flashover progressive stress test procedure

8

Laboratory Experiments

This section presents the air-based validation tests conducted to assess the test cell's electrical performance. The tests are structured to verify that the charge distribution over time for a given spacer was comparable to the COMSOL simulation, that preliminary LI flashovers were repeatable and matched simulation results, and to realize the DC/LI test circuit in the TU Delft lab, with the feasibility of future testing considered.

8.1. Preliminary LI Tests

The preliminary testing was conducted to determine the approximate U_{50} of the system and compare it against the prior simulation values, to observe the flashover paths for a given spacer material, and to verify that testing with the setup was repeatable. The up and down method described in Figure 7.2.2 was applied due to limited time, and no damage was observed across the spacer for the applied voltage range. All voltages are corrected based on IEC 60060 -1 [81] specified atmospheric conditions given per Appendix E. Figure 8.1 below shows the results of $n = 63$ applied impulses on a nylon spacer.

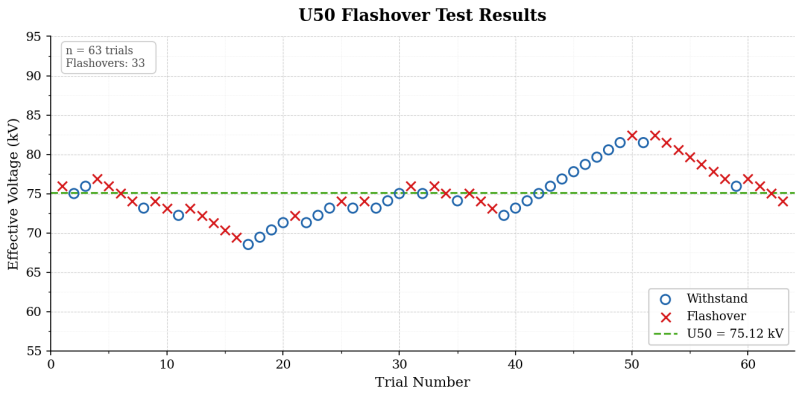


Figure 8.1: Preliminary up and down test performed with nylon spacer

The calculated U_{50} was 75 kV and a standard deviation σ = 4.25 kV. However, the sequence in Figure 8.1 shows extended runs of consecutive withstands and consecutive flashovers rather than oscillation about the U_{50}, which is characteristic of statistically dependent trials. Table F.1 shows a graphical dependency test, in which the breakdown frequency of the grouped n=10 subsets deviated substantially from the cumulative breakdown frequency. As noted by Hauschild et al. [88], the statistical independence of successive tests must be verified before any statistical conclusions can be drawn; since this assumption was evidently not satisfied, three different causes of dielectric polarization of the spacer, cumulative material degradation, and mechanical contact variation between trials were considered

Dielectric polarization was ruled out for the nylon sample as the conductivity was estimated to be around the order of 10^{-12} [S/m] from charge measurements, giving a dielectric relaxation time constant $\tau = \varepsilon/\sigma \approx 30$ s. This is well below the roughly 2-minute wait between successive impulses, so any accumulated surface charge would have relaxed before the next trial. Cumulative degradation was also similarly ruled out, as the material showed no carbonization or visible signs of degradation after the impulses, indicating that charge deposited during breakdown impulses and material erosion from surface flashovers did not meaningfully contribute to the effect.

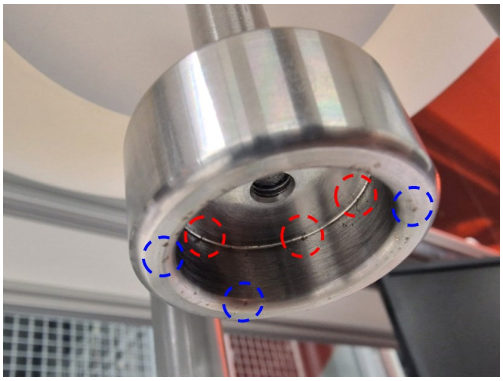
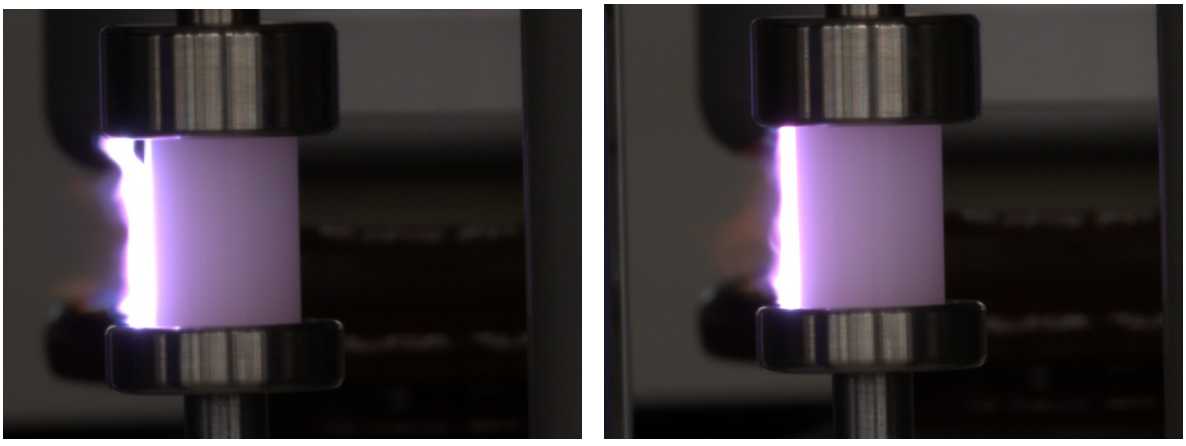


Figure 8.2: Flashover initiation marks from preliminary impulse testing, with red indicating triple-junction initiation and blue indicating shield initiation

Inspection of the top electrode as seen in Figure 8.2 revealed that discharges originated from both the intended shielding region and the triple junction. This indicated inadequate contact pressure between the electrode and the spacer, creating an artificial air gap. The captured flashover images in Figure 8.3 confirm this behavior with several occasions showing the discharge path initiated at the high-voltage triple junction (HVT) rather than at the shielding.



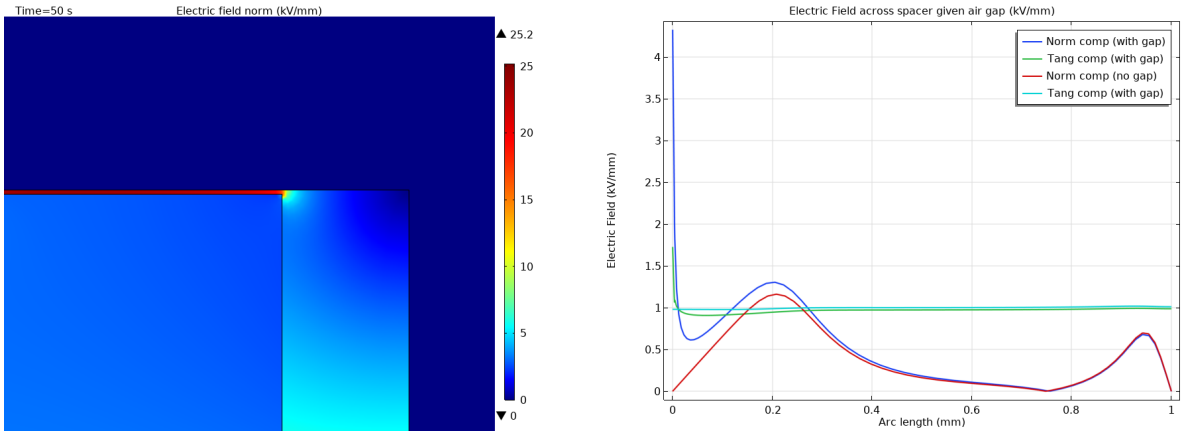
(a) Shielding-initiated breakdown **(b)** HVT-initiated breakdown

Figure 8.3: Different discharge paths of the tested nylon spacer under LI flashover

To verify the independence of the tests, a further independence test was conducted at the previously

calculated U_{50} of 75 kV, in which an impulse with a peak magnitude of the calculated U_{50} was applied and the breakdown frequency was compared. Between tests, the cleaning procedure was followed as per subsection 7.1.1, and the spacer was tightened using mechanical clamps.

There were 30 trials performed, and the expected U_{50} from the preliminary test had a cumulative flashover probability of 93%, indicating an additional problem of lack of repeatability existed in the test setup. The evaluation of the electrodes and spacer post-independence test also revealed fewer triple-junction discharges and, similarly, no spacer damage, indicating that inconsistent clamping force and handling created significant variability between tests. A COMSOL model was also created to verify this behavior by simulating a 0.1 mm air gap, which reasonably represented the possibility of installation error in the test cell. The field simulations in Figure 8.4 below show the effect of the introduced triple junction on the electric fields.



(a) Electric field at the triple junction

(b) Field components across the spacer side

Figure 8.4: Simulated effect of a 0.1 mm air gap between HV electrode and spacer arising from mounting errors

As shown in the figure above, the electric field is enhanced in the 0.1 μm air gap, with peak fields up to 22.2 kV/mm, which was high enough to initiate breakdown. The discharge marks on the inside of the upper HV bowl can therefore be explained by this phenomenon. In real GIS systems, the spacer is typically cast in with the conductor, effectively reducing the effect of the air gap, and in the initial design, could not be repeated. There were insufficient studies in the literature on the contact force between the spacer and the conductors.

A Redesign of the spacer and electrode was then performed, using a screw-based divot to enable more repeatable contact force. The design included a torque wrench hole at the top of the upper conductor, which offered the added benefit of allowing tightening in a gas-filled compartment after the installation of the plexiglass walls. The Figure 8.5 below shows the CAD model of the modification to the spacer electrode contact.

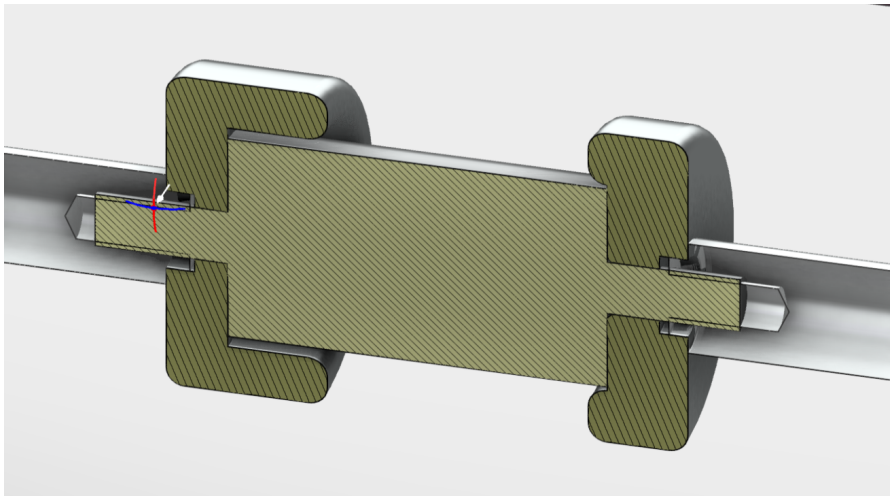
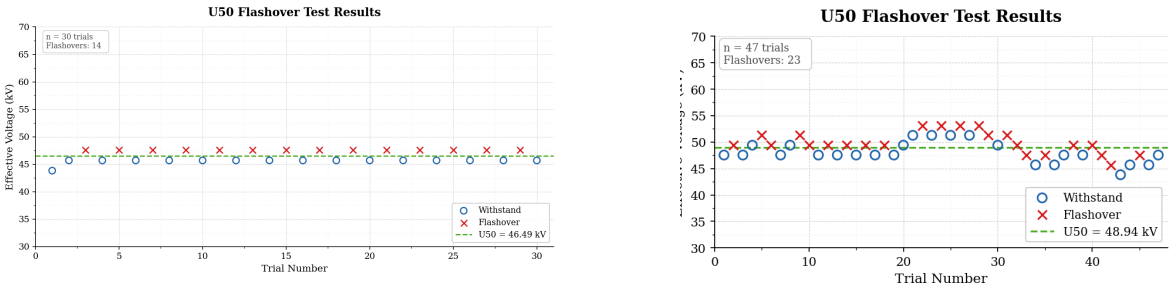


Figure 8.5: Spacer modifications with screw mount into electrode

New nylon and PTFE spacers were manufactured to the revised design and tested with positive LI voltages using the same cleaning procedure. An up and down test was performed on each material, shown in Figure 8.6.



(a) PTFE spacer

(b) Nylon spacer

Figure 8.6: Preliminary up and down test for both spacer materials with the new screw contact

From the image above, two different behaviors can be observed, including the perfect oscillations around the U_{50} for the PTFE spacer and that the redesigned nylon spacer showed much less dependent behavior.

For the PTFE test, the chosen step size of 4 % of the expected U_{50} proved too big as the applied voltage levels were split perfectly into either only withstands or flashovers, resulting in complete separation of the data. The MLE estimation as per Chapter E returned $U_{50} = 46.3$ kV, $\sigma = 0.05$ kV with very tight confidence bounds but without knowing the exact location of the statistical U_{50}.

The nylon spacer, by contrast, performed significantly better, oscillating about the U_{50} with far fewer runs of consecutive flashovers or withstands. The graphical independence test gave grouped probabilities close to the cumulative value, and the MLE fit yielded $U_{50} = 49.0 \pm 1.3$ kV and $\sigma = 3.1 \pm 2.3$ kV (95% CI). The wide relative uncertainty on σ reflects the limited number of trials, but the estimate of U_{50} is well constrained. The spread in time to breakdown, shown in Figure 8.7, was also substantially narrower for the redesigned nylon tests than for the initial tests, providing further evidence of improved repeatability.

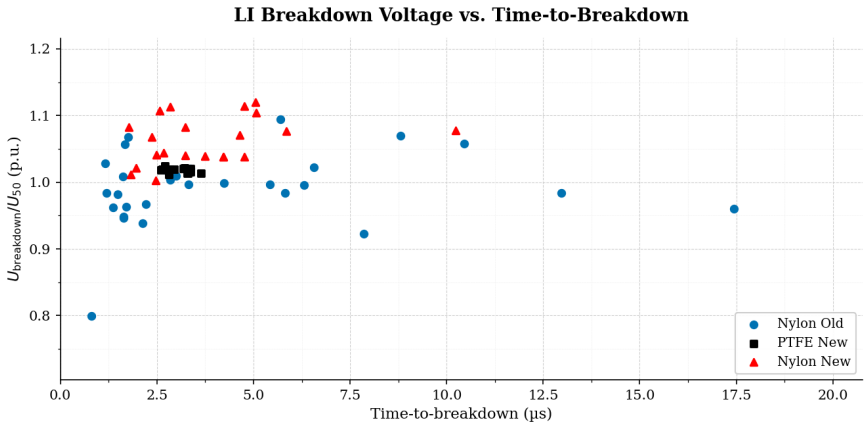


Figure 8.7: Time to breakdown across the different tests

The breakdown path also differed markedly between the two materials, with a much higher proportion of PTFE breakdowns occurring solely in the gas phase. Figure 8.8 below shows the breakdown paths observed for the PTFE spacer under the applied impulse voltage.



(a) Gas-gap breakdown

(b) Gas-to-surface breakdown

Figure 8.8: Different observed breakdown paths for PTFE under LI voltages

In summary, the measured spacer flashover voltages were consistent with the LI breakdown values predicted by COMSOL, and the flashover paths varied based on spacer materials. A redesign of the spacer contact mechanism was also performed to eliminate the effect of artificial triple junctions during installation and to establish a more repeatable method for tightening the spacers The independence of the tests was then verified with the redesigned spacer, resulting in behavior more consistent with an independent up and down test. Future work still remains regarding testing at higher voltages and under pressurized conditions.

8.2. Charge Accumulation Tests

To verify that the charge accumulation assumptions used in the simulations hold, a series of charge accumulation tests was conducted. The overall goal was to determine the degree of error in the

simulation and to further match it to better represent observed behaviors in the lab. The procedure for measuring the charges is given in Section 7.2.1. The raw voltage measurements recorded with the electrostatic voltmeter are presented in Appendix F.

The simulation was run with the same parameters as for ambient air from prior, with an R parameter corrected based on an average relative humidity of 36.1% from the Equation 5.1 prior. The values used were S = 16 IP/cm^3s and $R = 1.2 \times 10^{-11}$ m^3/s. The simulation was done by removing the plexiglass and applying DC for 2 hours. Figure 8.9 shows the gas conductivity of the setup as per the ion drift model.

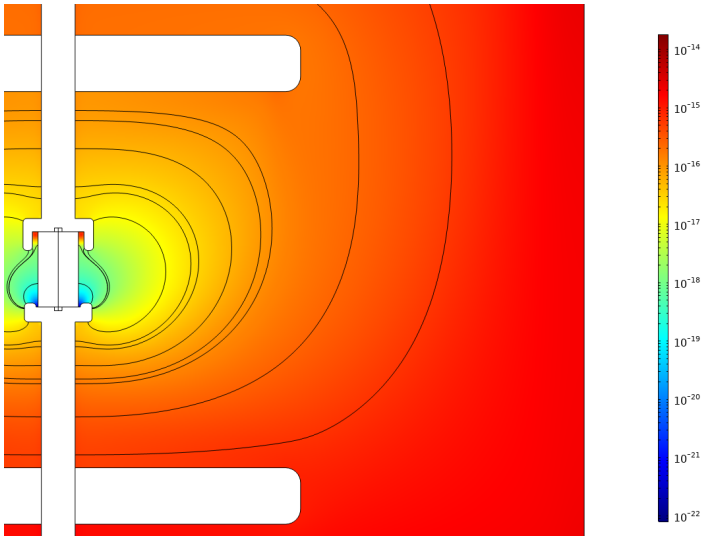


Figure 8.9: Electrical conductivity in gas volume with ambient air parameters

As shown in the model, the effective conductivity near the spacer remains very low, at approximately 2.8×10^{-18} [S/m]. The comparison of the ion drift model to the measurements at the 3 points is shown in Figure 8.10.

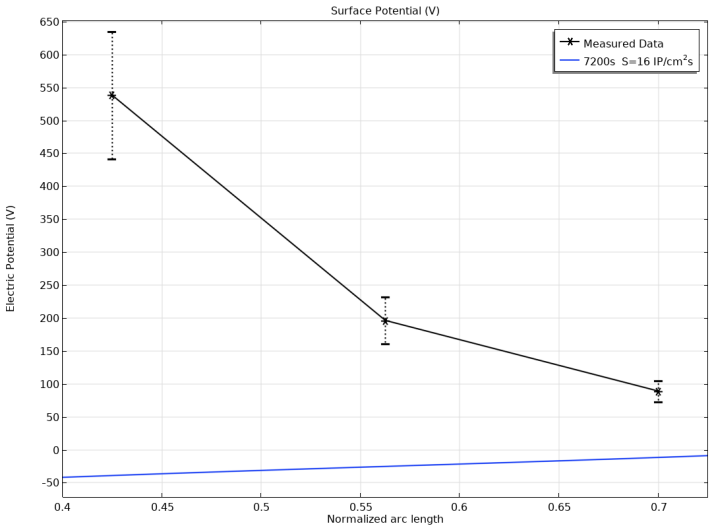


Figure 8.10: Charge accumulation across a section of the insulator compared to simulation with ambient air for +10 kV DC applied for 2 hours

As seen in the simulations, the assumed conductivity yields potentials of opposite polarity, with a maximum difference of 600V at point 0.425. It was also observed that, for individual measurements, charges of wildly higher magnitudes, up to 1kV, or opposite polarities up to -390 V. The observed behaviors indicate three phenomena: charge deposition on the surface occurred much faster than simulations predict, gas conduction current appeared to be the dominant force driving charge deposition with ambient air, and localized charge ”spots” occurred on the spacer.

The micro-discharge phenomenon from electrodes across studies by Vu Cong et al. [20] is modeled by the formula given in Equation 8.1 below for SF6, with the observation that the term only significantly affects generation at higher electric fields. In 5 bar SF_6 the emitted current from the HV electrode into the gas has been fitted and provided below.

$$J_{emitted} = 25[\frac{pA}{m^2}] * exp(0.3 * E) \tag{8.1}$$

The equation shows an exponential increase in electrode ionization; for low field strengths, electrode emission can be effectively ignored. However, the parameters fitted to the equation for this are not known for technical air at 1 bar. It was also seen that field emission is much more pronounced for an equivalent voltage in dry air compared to SF_6, as seen by Zhang et al. [91]. The roughness of the electrode is also thought to have an effect, as tiny protrusions produce local field enhancements and therefore emission, as reported by Scheuller et al. [92]. It is clear that the ion drift model for the ambient air does not accurately represent the behavior of the surface charge accumulation unless additional ionization sources are considered. Figure 8.11 shows the effect of increasing the S rates on the measured surface potential.

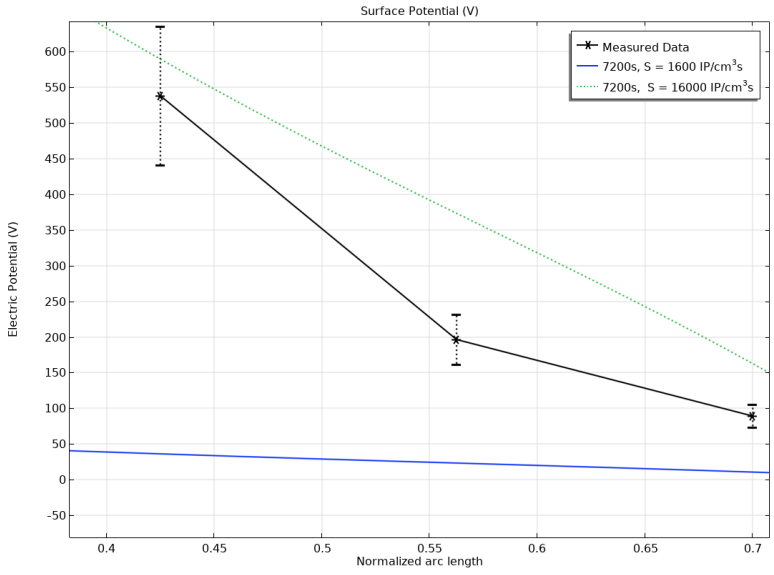


Figure 8.11: Charge accumulation across a section of the insulator compared to a simulation with IP = 1600 IP/cm^3s and 16000 IP/cm^3s for +10 kV DC applied for 2 hours

It is noted that a constant conductivity of 8×10^{-16} [S/m] yields similar results to S= 16000 IP/cm^3s above which is slightly higher than estimated by Kallstrand et al.[93]. The behavior considered is

also only for a small section of the spacer, and only 3 separate points were considered; However it is clear that additional ion sources must be added to the ion drift model to better match the measured charge profile in the TU Delft HV lab. The proposed causes are electrode surface roughness and additional background radiation, and addressing them should involve polishing the electrode surface and repeating the tests in an enclosed volume with dry air.

8.2.1. Comparison to measurements

A direct validation of the charge-accumulation model against dry air measurements could not be completed within the time available for this thesis. It was therefore chosen to compare the model with parameters of SF_6 to measurement data from Schueller et al. [94] given the relatively low gas conductivity of both gases [95]. The used test setup is given in Figure 8.12 and the simulation parameters are given in Figure 8.1.

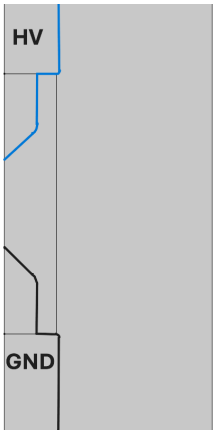
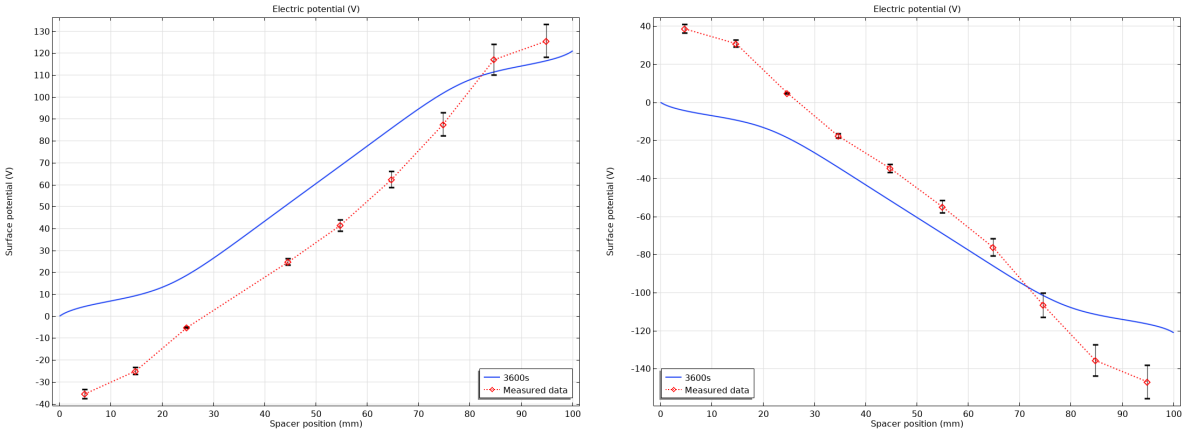


Figure 8.12: 2D axisymmetric simulation model used by Schueller et al. [94] with SF_6 at 0.4 MPa

Table 8.1: Simulation parameters for the Schueller et al. [94] simulation

Parameter	Value
Gas / pressure	SF_6 / 0.4 MPa
Positive/negative ion mobility	4.8×10^{-6} m^2/Vs
Ion-pair generation S	29 IP/cm^{3}s
Recombination R	2.3×10^{-13} m^3/s

In the simulations, the coupled ion drift model was used, and the comparison was for an applied voltage of $\pm$ 1 kV over 1 hour. Figure 8.13 below shows the result of measurements vs simulations.



(a) $V_{dc} = +1$ kV **(b)** $V_{dc} = -1$ kV

Figure 8.13: Simulation compared with measurements from Schueller et al. [94] for an applied $\pm$1 kV DC over 1 hour

For both polarities, the simulated surface potential matches the measurements' magnitude and polar-

ity. The maximum observed deviation between measurement and the simulation is 40V at a position of 5 cm. Given the sensitivity of surface charge accumulation to ionization in the gas volume. These differences indicate general agreement and that the model can reasonably predict surface charge on gas-solid interfaces.

It can be concluded that the initial comparison of the simulation with the ambient air parameters showed poor agreement with the measured data, with opposite polarity and very different magnitudes. This was explained by additional ion-generation terms, such as those arising from electrode roughness or the background, and was addressed in the simulation by using a very high ion-pair generation rate. Comparison of the model with data from Scheuller [94] yielded a much better fit, with similar polarity and magnitudes.

For future work, it is suggested that tests be performed using the setup above, with the charge probe and test cell placed in a sufficiently large enclosed volume filled with dry air, and with the electrodes polished to 1 mum to further reduce the possibility of field emission.

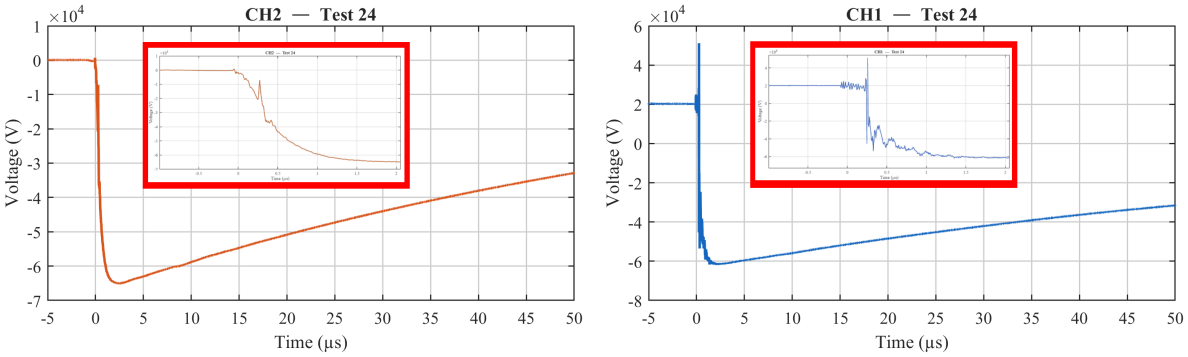
8.3. DC LI Circuit Verification

The circuit for the DC/LI test circuit verification was built at the TU Delft HV lab according to Figure 7.13, and the impulse front and breakdown are evaluated with both the spark gap and coupling capacitor used as DC blocking components. The overall goal of the section is to verify whether a given circuit topology is well suited to composite DC/LI waveforms and whether certain voltage levels are better suited to that topology.

Spark Gap

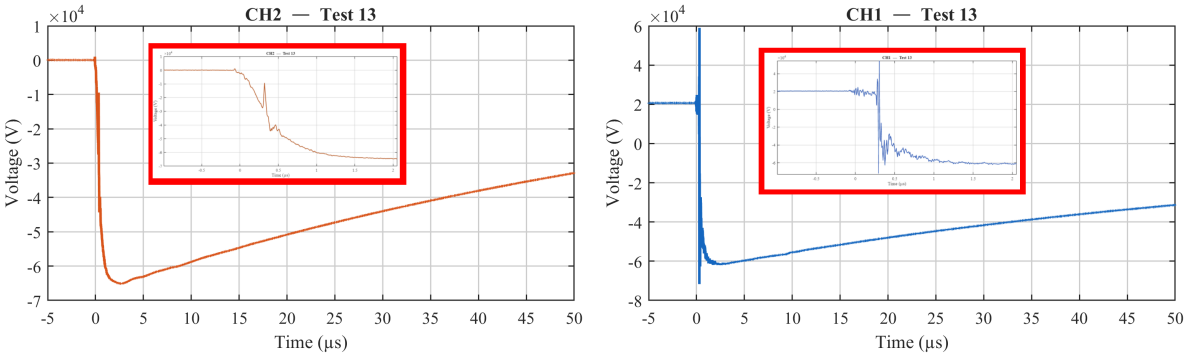
The spark gap used at TU Delft was 4 cm in diameter, and breakdown voltages were selected in accordance with a 5 cm gap, as specified in IEC 60052 [96], for all tests. The temperature of the testing environment and absolute humidity were recorded every 2 hours and used along with the relevant atmospheric correction factors from Appendix E. Unless stated otherwise, tests were performed at a fixed polarity combination of $+20$ kV DC and -60 kV LI.

It was observed that, as mentioned in subsection 6.3.2, the timing of the spark gap firing relative to the rising front strongly affects the shape of the composite waveform recorded at the DUT and the corresponding T1 evaluation. For an early trigger of 32 kV, chosen based on a 1 mm gap spacing, the observed triggers ranged from 41 kV (21 kV referenced to ground) to 55 kV (35 kV referenced to ground), as shown in Figure 8.14 and Figure 8.15.



(a) LI divider **(b)** Mixed divider

Figure 8.14: Recorded withstand voltage waveforms for early spark gap trigger at 41 kV



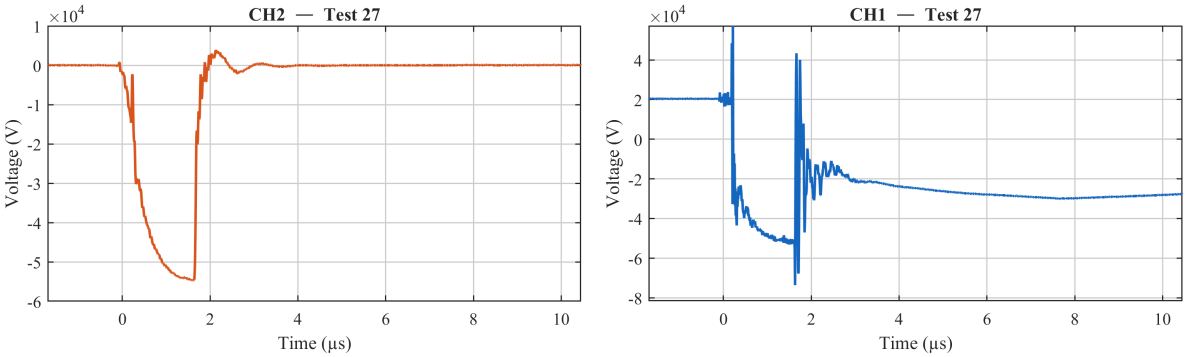
(a) LI divider **(b)** Mixed divider

Figure 8.15: Recorded withstand voltage waveforms for late spark gap trigger at 55 kV

As seen in the waveforms above, it was also observed that setting the spark-gap trigger earlier resulted in fewer deviations near the peak of the impulse and led to closer evaluations of T1 to the LI divider. The spark-gap trigger should be chosen as early as possible above U_{DC} to minimize disturbance to the front of the wavefront, with a small voltage drop across the LI divider due to the low load capacitance explained in subsection 6.3.2. It was observed that evaluating T1 on the mixed divider was always faster than on the LI divider due to the steep dV/dt from the spark-gap triggering.

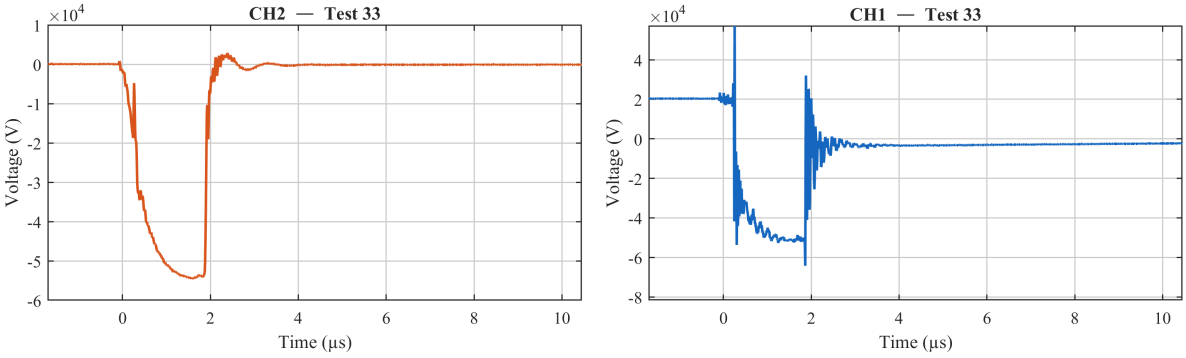
Across all DC/ LI tests, the spark gap consistently broke down at voltages approximately 30% higher than those predicted by IEC 60052 [96]. While testing was done in one of the hottest weeks in the Netherlands with temperatures reaching 30 °C and 60% RH in the lab. The atmospheric corrections from Appendix E could also not explain the discrepancy and indicated problems with the spark gap used. The only spark gaps available in the lab were 4 cm and 50 cm, with the larger ones suited only to voltages above 60 kV. The larger spark gaps were tested but did not result in consistent triggering at the given voltage either.

A breakdown of the LI voltage of the test object was also considered to view the behavior across the dividers. The breakdowns occurred simultaneously; however, the voltage waveform on the mixed divider did not settle at 0 but instead bounced to a negative voltage. The DC/LI setup was tested with 2 potential grounding configurations and the Figure 8.16 Figure 8.17 below shows the voltage chopping observed on the mixed divider for an impulse polarity of -60 kV.



(a) LI Divider **(b)** Mixed Divider

Figure 8.16: Recorded breakdown voltage waveforms for spark gap with common Impulse generator ground



(a) LI Divider **(b)** Mixed Divider

Figure 8.17: Recorded breakdown voltage waveforms for spark gap with separate Impulse generator ground

As seen in the image above, the circuit's breakdown behavior changes dramatically depending on the chosen grounding scheme, with common grounding for the Impulse generator, LI divider, and mixed divider. The breakdown waveform, as mentioned, jumps to a non-zero value, which can be explained by the ground potential rise during an impulse from the inductances present in the common ground. The change in the ground resulted in a better waveform that reached 0 V as expected. It must therefore be noted that the grounding of the LI divider and impulse generator must be kept separate from the grounding of the mixed divider. It is also recommended that grounding be done with copper sheets rather than ground wires,as this introduces problems of overshoots and noise in the recorded waveform, likely attributed to the higher inductances.

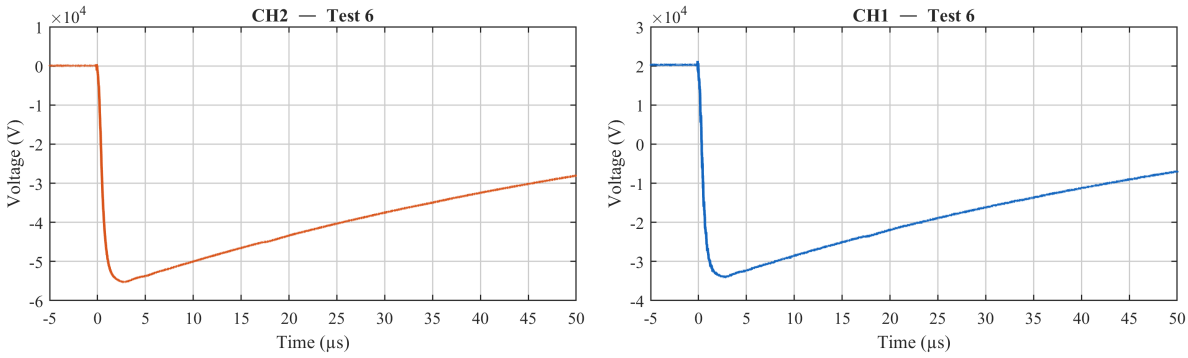
It can be concluded that a spark gap can be used to generate a composite waveform, with some caveats. The test circuit with a spark gap as suggested by CIGRE TB842 [12] states that a spark gap can be used for composite waveforms without the need for a mixed divider at the DUT. In the TU Delft HV lab, the spark gap exhibited highly variable behavior, leading to different measured DUT waveforms. The observed behavior of the spark gap also reinforces the recommendation to use a mixed divider.

The grounding of a mixed divider must be different from the impulse generator, and grounding for all components should be done with copper sheets. The test circuit using spark gaps is generally not preferred at lower test voltages, as the range of early triggering is narrower. Further tests are

suggested using the large spark gap and voltages of 30 kV DC and 150 kV LI to verify whether the front distortion remains significant for higher voltages and whether the same-polarity DC/LI can be generated.

Coupling Capacitor

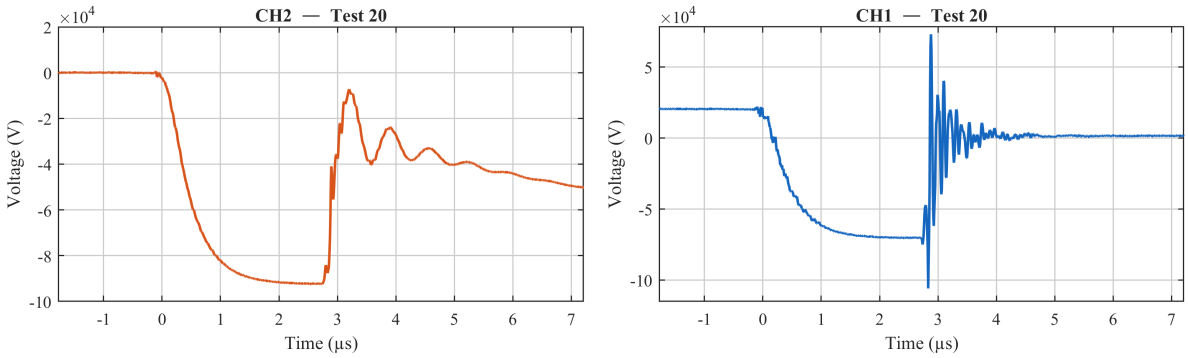
A testing circuit with a coupling capacitor was used in place of the spark gap due to the aforementioned unreliability in triggering and waveform distortions. A 25 nF capacitor rated at 140 kV was used, and the Figure 8.18 below shows the waveform observed on both the LI and mixed divider for a non-breakdown superimposed LI impulse.



(a) LI divider **(b)** Mixed Divider

Figure 8.18: Recorded withstand voltage waveforms for coupling capacitor

As seen in the image above, the waveform measured by the mixed divider more closely resembles the LI waveform, with minimal distortion at the front. The IEC evaluation of front times is nearly identical for both waveforms and is considered a better option for testing up to 2 bars, where a maximum of $\pm$ 20 kV DC and $\mp$ 100 kV LI is expected. The use of a coupling capacitor is also preferred, given that realizing a same-polarity superimposition was much easier for lower voltages. A breakdown waveform was also observed with a 20 kV DC applied and -60 kV LI, as shown in Figure 8.19a and Figure 8.19 below, which show the observed voltage chopping.



(a) LI Divider **(b)** Mixed Divider

Figure 8.19: Recorded breakdown voltage waveforms for coupling capacitor

It can be seen that the chopping of the waveform on both the dividers occurs within around 100 ns of each other. An interesting behavior was also observed, in which the LI voltage bounces back to

the impulse waveform after a flashover, speculated to be due to the charge in the tail capacitor of the impulse generator not being fully discharged through the flashover arc. This, however, is not important to the breakdown event, as the chopping time is captured accurately on both dividers.

It can be concluded that the coupling capacitor produced better waveforms and less random behavior than a spark gap and is preferred for testing up to 2 bar. For higher voltages, while a capacitor is preferred, a spark gap is the only option, and the trigger voltage must be set as early as possible. Testing past 3 bar also does not seem possible, given the mixed divider would not be rated for it. It is recommended that future tests use the larger available spark gap and assess the randomness and front distortion observed at higher applied LI magnitudes.

9

Conclusion & Recommendations

9.1. Conclusion

This thesis has presented the design, development, and partial experimental verification of a laboratory-scale test system for investigating spacer flashover behavior under composite DC/LI voltages in alternative gas-filled HVDC GIS systems. The primary objective was to design, build, and verify an electrode, test cell, and circuit capable of testing for spacer flashovers under composite voltages, reproducing the electrical conditions representative of disc spacers in DC GIS systems. The work was guided by the research question given below.

Research Question

What is a suitable laboratory-scale test system for the study of spacer flashover behavior under composite DC/LI voltages in alternative gas-filled HVDC GIS?

A modified bowl plate electrode geometry was selected and optimized to reproduce the quasi-homogeneous field distributions characteristic of disc spacers in DC GIS systems. Coupled multiphysics simulations across different spacer material scenarios were performed, demonstrating that charge accumulation under DC and DC/LI stresses is a complex, multidirectional phenomenon governed by bulk and gas conductivity, with nylon and PTFE proposed as an alternative to epoxy resins typically used. Voltages were then chosen based on operation pressures to produce scaled field stresses representative of nominal DC operation in full scale DC GIS systems.

From a review of existing enclosure cell topologies, A floating cell configuration was designed, dimensioned, and built to prevent external breakdown while preserving the internal field distribution between the electrodes. Field simulations verified that the enclosure withstands composite DC/LI voltages up to 30/150 kV, filled with 3 bar of technical air, confirming that the enclosure design met its functional requirements. A composite voltage test circuit was subsequently designed using available compo-

nents from the TU Delft HV laboratory and validated via LTspice simulation, with coupling elements on the DC and LI sides considered.

Initial experimental verification revealed that reliable spacer contact with the high-voltage electrode was critical for test reproducibility, and the initially designed setup could not provide sufficient clamping force. Initial LI tests were affected by HV triple-junction discharges, resulting in poor repeatability. A redesigned screw-based spacer clamping system was developed to address this, improving both contact reliability and assembly repeatability. The introduction of the new design resulted in more independent U_{50} behaviors with a lower standard deviation than in the initial tests.

Experimental verification of the surface charge under a +10 kV DC application was conducted using ion parameters for ambient air and showed poor initial agreement in shape and polarity. Additional ion generation sources had to be considered, such as from field emissions or additional background generation with a match at S= 1.6×1.6^4 IP/cm^3s. The simulation was also compared to measurements from other authors and showed a much better agreement in both polarity and magnitude.

The test circuit from LTspice was also verified using spark gaps and a coupling capacitor, and it was observed that the spark gaps at TU Delft exhibited very inconsistent triggering behavior. Coupling capacitors resulted in significantly better waveforms but could only be used up to 2 bar stress due to their voltage rating. It is recommended, based on the tests, that spark gap or coupling capacitor test setups both must use a mixed divider to record voltage on the DUT.

In conclusion, the aims of the thesis have been partially met with the design and simulation objectives were fully achieved. The experimental validation, though not fully completed, has been clearly defined for future pursuers.

9.2. Recommendations

Based on the work done in this thesis, the verification of this cell remains largely complete, with the following recommendations pending.

1. It is recommended that the volume and surface conductivity of the nylon and PTFE spacers be measured across 0 to 5 kV/mm. Current simulations assume a fixed temperature and a field-independent conductivity, obtained from an online materials database. The variation of conductivity could significantly affect the charge accumulation and DC field components, with it being recommended to especially measure the surface conductivity of the used sample. The measured profiles of surface and volume conductivity should then be imported into COMSOL to better capture DC-related charging behavior.
2. It is recommended to perform LI breakdown tests at 3 bar gas pressure to confirm that the cell withstands the electrical stresses and that breakdown occurs only between the electrodes. Breakdown testing has been demonstrated at 1 bar, but the insulation performance at the elevated pressures remains uncharacterized.
3. The third recommendation is to investigate the charge accumulation behavior of the solid-gas interface for the same applied +10kV DC in technical air with no humidity, to compare with the simulation model and verify that the expected polarity and magnitudes are observed. Given the

dimensions of the cell and the used probe, it was not possible to measure surface charge in dry air. A recommendation is made to create a large enclosed volume that the probe and test cell can fit within, so the charge accumulation results can be compared with the simulation model. This can present a more accurate idea of the leakage through the dry air and whether the used simulation parameters hold.

4. The fourth recommendation is to test the spark gap at higher-voltage levels of 30 kV DC and 150 kV LI to visualize the severity of waveform distortions at higher voltages. The spark gap tested showed erratic behavior and was very unpredictable, which distorted the fronts and the chopping time evaluated. Testing must also be done with the same polarity to verify the distortion's effects on the waveform and whether it can be sufficiently minimized at higher voltages.

5. Given the above implementations, the final recommendation is that DC/LI testing is performed as given as per section 7.2 and that initial testing should be performed for 1 bar technical air with the voltages prescribed in subsection 4.4.1. A quadrant map should be made to compare the difference in flashover voltages for pure LI against superimposed DC/LI. The camera should also be used to compare the breakdown path under different applied voltages. The weakening of the insulation strength with DC charge and the difference in surface flashover path can then be quantified.

References

[1] GE Vernova Grid Solutions. *The History of Gas-Insulated Substations*. Accessed: 2025-01-29. Mar. 2024. URL: https://library.grid.gevernova.com/articles/the-history-of-gas-insulated-substations.

[2] Hitachi Review Editorial Team. *Gas-Insulated Reactors for Power Transmission Systems*. Accessed: 2025-01-29. 2020. URL: https://www.hitachihyoron.com/rev/archive/2020/r2020_04/gir/index.html.

[3] Manu K P. "High-Voltage Direct Current (HVDC) Transmission: Reliability and applications". In: *World Journal of Advanced Research and Reviews* (2022). Accessed: 2025-01-29. URL: https://wjarr.com/sites/default/files/WJARR-2022-1074.pdf.

[4] *Global HVDC Transmission Report*. Tech. rep. Accessed: 2025-01-29. Global Transmission, 2024. URL: https://globaltransmission.info/wp-content/uploads/2024/11/HVDC_Report_Final.pdf.

[5] U. Schichler, C. M. Franck, et al. "Gas-Insulated Transmission Lines and Gas-Insulated Substations: State of the Art and Future Trends". In: *Proceedings of the IEEE Power and Energy Society General Meeting*. Accessed: 2025-01-29. 2012. DOI: 10.1109/PESGM.2012.6281403. URL: https://ieeexplore.ieee.org/document/6281403.

[6] M.J.P. Jeroense and P.H.F. Morshuis. "Electric fields in HVDC paper-insulated cables". In: *IEEE Transactions on Dielectrics and Electrical Insulation* 5.2 (1998), pp. 225–236. DOI: 10.1109/94.671940.

[7] Dongxin He et al. "Space Charge Behaviors in Cable Insulation under a Direct Current-Superimposed Pulsed Electric Field". In: *HAL Open Science* (2020). Submitted on 12 Nov 2020. URL: https://hal.science/hal-03002410/document.

[8] Haoluan Li. "Characterisation of HVDC Gas Insulated Systems". PhD Thesis. PhD thesis. Cardiff University, 2023. URL: https://orca.cardiff.ac.uk/id/eprint/166102/.

[9] Qasim Khan et al. "Partial discharge detection and diagnosis in gas insulated switchgear: State of the art". In: *IEEE Electrical Insulation Magazine* 35.4 (2019), pp. 16–33. DOI: 10.1109/MEI.2019.8735667.

[10] Rami S. Rzouq et al. "Comparison Between Different Gases Used as Insulation Medium in High Voltage Technology and Their Effect on the Environment". In: *Ecological Engineering & Environmental Technology* 24.3 (2023), pp. 60–70. DOI: 10.12912/27197050/159630. URL: https://www.ecoeet.com/pdf-159630-87994?filename=Comparison%20Between.pdf.

[11] Luke Silvestre et al. "Nanosecond Breakdown Characteristics of C4F7N and Various Mixtures at Pressures Above 1 Atmosphere in Comparison with SF6". In: *Applied Sciences* 14.23 (2024), p. 11268. DOI: 10.3390/app142311268. URL: https://www.mdpi.com/2076-3417/14/23/11268.

[12] CIGRE JWG TB 842 contributors. "Dielectric testing of gas insulated HVDC systems". In: *ELECTRA (CIGRE)* (2021). Technical Brochure TB 842 summary in ELECTRA. URL: https://electra.cigre.org/318-october-2021/technical-brochures/dielectric-testing-of-gas-insulated-hvdc-systems.html.

[13] International Electrotechnical Commission. *IEC TS 62271-318:2024 - High-voltage switchgear and controlgear – Part 318: DC gas-insulated metal-enclosed switchgear for rated voltages including and above 100 kV*. Geneva: International Electrotechnical Commission. 2024. URL: https://webstore.iec.ch/en/publication/66210.

[14] Siemens Energy Management Division / Transmission Solutions. *Alabama Power Company Siemens EM TS: GIS Overview*. https://site.ieee.org/alabama/files/2018/02/RC-US-EM-TS_FY18-APC_v3.pdf. Presentation document, accessed January 2026. Siemens Industry, Inc., Mar. 2018.

[15] Yixuan Li et al. "Optimization of insulators in ±550 kV HVDC GIS for offshore wind platform considering charge accumulation". In: *Electric Power Systems Research* 223 (2023), p. 109549. ISSN: 0378-7796. DOI: https://doi.org/10.1016/j.epsr.2023.109549. URL: https://www.sciencedirect.com/science/article/pii/S0378779623004388.

[16] Laëtitia Zavattoni. “Conduction phenomena through gas and insulating solids in HVDC gas insulated substations, and consequences on electric field distribution”. Theses. Université de Grenoble, Oct. 2014. URL: https://theses.hal.science/tel-01305949.

[17] Maria Kosse et al. “Overview of development, design, testing and application of compact gas-insulated DC systems up to ±550 kV”. In: *Global Energy Interconnection* 3.6 (2020), pp. 567–577. DOI: 10.1016/j.gloei.2020.01.011. URL: https://doi.org/10.1016/j.gloei.2020.01.011.

[18] Hitachi Energy. *ELK-4 Gas-Insulated Switchgear up to 800 kV*. Accessed: 2025-12-30. 2025. URL: https://www.hitachienergy.com/in/en/products-and-solutions/high-voltage-switchgear-and-breakers/gas-insulated-switchgear/gis-for-72-5-1200-kv/gis-elk-4-up-to-800-kv.

[19] Siemens Energy. *Gas-Insulated Switchgear (DC-GIS)*. Accessed: 2025-12-30. Product page describing Siemens Energy DC GIS up to ± 550 kV and 5 kA. 2025. URL: https://www.siemens-energy.com/global/en/home/products-services/product/dc-gis.html.

[20] T. Vu-Cong, F. Jacquier, and A. Girodet. “Electric field computation for HVDC GIS/GIL spacer under superimposed impulse conditions”. In: *2019 IEEE Conference on Electrical Insulation and Dielectric Phenomena (CEIDP)*. 2019, pp. 409–412. DOI: 10.1109/CEIDP47102.2019.9009868.

[21] Xiaolong Li et al. “Improved method in calculating the surface charge distribution of DC□GIL insulators with 3D geometry models”. In: *IET Science, Measurement & Technology* 16 (7 2022), pp. 400–411. DOI: 10.1049/smt2.12113. eprint: https://digital-library.theiet.org/doi/pdf/10.1049/smt2.12113. URL: https://digital-library.theiet.org/doi/abs/10.1049/smt2.12113.

[22] Zhen Li et al. “Surface flashover in 50 years: Theoretical models and competing mechanisms”. In: *High Voltage* 8.5 (2023), pp. 853–877. DOI: https://doi-org.tudelft.idm.oclc.org/10.1049/hve2.12340. eprint: https://ietresearch-onlinelibrary-wiley-com.tudelft.idm.oclc.org/doi/pdf/10.1049/hve2.12340. URL: https://ietresearch-onlinelibrary-wiley-com.tudelft.idm.oclc.org/doi/abs/10.1049/hve2.12340.

[23] A. von Engel. *Ionized Gases*. 2nd. Oxford: Oxford University Press, 1965.

[24] PROMOTioN Project Consortium. *Work Package 15: HVDC GIS Technology Demonstrator*. Accessed: 2025-12-30. Listed under project deliverables as Work Package 15. 2020. URL: https://www.promotion-offshore.net/results/deliverables/.

[25] Geng Chen et al. “Environment-friendly insulating gases for HVDC gas-insulated transmission lines”. In: *CSEE Journal of Power and Energy Systems* 7.3 (2021), pp. 510–529. DOI: 10.17775/CSEEJPES.2019.01060.

[26] Haoran Wang et al. “Calculation and optimization for UHV AC GIS spacer in electrical and mechanical fields”. In: *2016 IEEE International Conference on High Voltage Engineering and Application (ICHVE)*. 2016, pp. 1–4. DOI: 10.1109/ICHVE.2016.7800634.

[27] Roland Piccin et al. “Partial discharge analysis of gas insulated systems at high voltage AC and DC”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 22.1 (2015), pp. 218–228. DOI: 10.1109/TDEI.2014.004711.

[28] Zhang Shiling, Zhang Siyu, and Su Xialin. “Multi-Physics Field Simulation of 1100kV GIS SF6 Gas Insulated Composite Bushing”. In: *2019 IEEE Conference on Electrical Insulation and Dielectric Phenomena (CEIDP)*. 2019, pp. 247–250. DOI: 10.1109/CEIDP47102.2019.9009764.

[29] Uberto Vercellotti. “HVDC links at increased voltage, CESI experience on extruded cable systems up to 525kV”. In: *2019 AEIT HVDC International Conference (AEIT HVDC)*. 2019, pp. 1–5. DOI: 10.1109/AEIT-HVDC.2019.8740439.

[30] Ziwei Zhao et al. “Investigation on Dielectric Insulation Properties of ±525 kV HVDC XLPE Material for High Temperatures Applications”. In: *2024 International Conference on HVDC (HVDC)*. 2024, pp. 915–919. DOI: 10.1109/HVDC62448.2024.10723025.

[31] F. Messerer and W. Boeck. “Gas insulated substation (GIS) for HVDC”. In: *2000 Annual Report Conference on Electrical Insulation and Dielectric Phenomena (Cat. No.00CH37132)*. Vol. 2. 2000, 698–702 vol.2. DOI: 10.1109/CEIDP.2000.884054.

[32] Bo Qi et al. “Effect of surface charge accumulation on flashover voltage of GIS insulator in SF6 under DC and AC voltages”. In: *2015 IEEE Conference on Electrical Insulation and Dielectric Phenomena (CEIDP)*. 2015, pp. 848–851. DOI: 10.1109/CEIDP.2015.7352094.

[33] B. Du and H. Liang. *Epoxy-based Spacers for Gas Insulated Power Apparatus*. Springer, 2023. ISBN: 978-981-19-7111-2.

[34] A. De Lorenzi et al. “Modeling of epoxy resin spacers for the 1 MV DC gas insulated line of ITER neutral beam injector system”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 16.1 (2009), pp. 77–87. DOI: 10.1109/TDEI.2009.4784554.

[35] Malte Tschentscher and Christian M. Franck. “Conduction processes in gas-insulated HVDC equipment: from saturated ion currents to micro-discharges”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 25.4 (2018), pp. 1167–1176. DOI: 10.1109/TDEI.2018.007171.

[36] Boya Zhang, Zhe Qi, and Guixin Zhang. “Thermal gradient effects on surface charge of HVDC spacer in gas insulated system”. In: *2016 IEEE Conference on Electrical Insulation and Dielectric Phenomena (CEIDP)*. 2016, pp. 703–706. DOI: 10.1109/CEIDP.2016.7785563.

[37] Lu Xu et al. “Impact of Pressure and Temperature on Charge Accumulation Characteristics of Insulators in Direct-Current Gas-Insulated Switchgear”. In: *Energies* 17.11 (2024), p. 2739. DOI: 10.3390/en17112739. URL: https://www.mdpi.com/1996-1073/17/11/2739.

[38] Qiang Wang, Guixin Zhang, and Xinxin Wang. “Characteristics and mechanisms of surface charge accumulation on a cone-type insulator under dc voltage”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 19.1 (2012), pp. 150–155. DOI: 10.1109/TDEI.2012.6148513.

[39] Rachmawati et al. “Electric Field Grading and Discharge Inception Voltage Improvement on HVDC GIS/GIL Spacer With Permittivity and Conductivity Graded Materials (ε/σ-FGM)”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 29.5 (2022), pp. 1811–1817. DOI: 10.1109/TDEI.2022.3194489.

[40] Naoki Hayakawa et al. “Fabrication and simulation of permittivity graded materials for electric field grading of gas insulated power apparatus”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 23.1 (2016), pp. 547–554. DOI: 10.1109/TDEI.2015.005237.

[41] Zuodong Liang et al. “Designing HVDC GIS/GIL Spacer to Suppress Charge Accumulation”. In: *High Voltage* 7.4 (2022), pp. 645–651. DOI: 10.1049/hve2.12220. URL: https://doi.org/10.1049/hve2.12220.

[42] Hang Yao et al. “DC/AC Electric Field Relaxation With Multidimensional Functionally Graded Materials (ε/-σ-MFGM) for Offshore Bipolar HVDC GIS Spacer”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 30.5 (2023), pp. 2059–2066. DOI: 10.1109/TDEI.2023.3296070.

[43] Koki Juni et al. “Effect of Spacer Geometry on Surface Charge Accumulation on DC-GIS Insulating Spacer”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* (2025), pp. 1–1. DOI: 10.1109/TDEI.2025.3647375.

[44] CIGRE JWG Recommendations. *Recommendations for dielectric testing of HVDC gas□insulated cable connection assemblies*. Tech. rep. Ref. 957. CIGRE, 2025. URL: https://www.e-cigre.org/publications/detail/957-recommendations-for-dielectric-testing-of-hvdc-gas-insulated-cable-connection-assemblies.html.

[45] S. Sato, W. S. Zaengl, and A. Knecht. “A Numerical Analysis of Accumulated Surface Charge on DC Epoxy Rrsin Spaces”. In: *IEEE Transactions on Electrical Insulation* EI-22.3 (1987), pp. 333–340. DOI: 10.1109/TEI.1987.298999.

[46] K. Nakanishi et al. “Surface Charging On Epoxy Spacer At Dc Stress In Compressed SF6 GAS”. In: *IEEE Transactions on Power Apparatus and Systems* PAS-102.12 (1983), pp. 3919–3927. DOI: 10.1109/TPAS.1983.317931.

[47] Shigemitsu Okabe et al. “Insulation characteristics of GIS insulators under lightning impulse with DC voltage superimposed”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 22.6 (2015), pp. 1–9. DOI: 10.1109/TDEI.2015.005178.

[48] Jingtan Ma et al. “Study on insulation characteristics of GIS under combined voltage of DC and lightning impulse”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 24.2 (2017), pp. 893–900. DOI: 10.1109/TDEI.2017.006535.

[49] Jian Wang et al. “Mechanism Analysis of Particle-Triggered Flashover in Different Gas Dielectrics Under DC Superposition Lightning Impulse Voltage”. In: *IEEE Access* 8 (2020), pp. 182888–182897. DOI: 10.1109/ACCESS.2020.3026695.

[50] Lin Liu et al. “Surface flashover patterns of GIS basin insulator under impulse voltage”. In: *Engineering Failure Analysis* 130 (2021), p. 105800. ISSN: 1350-6307. DOI: https://doi.org/10.1016/j.engfailanal.2021.105800. URL: https://www.sciencedirect.com/science/article/pii/S1350630721006610.

[51] Shaocong Wu et al. “Towards the surface flashover in DC GIL/GIS: the electric field distribution and the surface charge accumulation”. In: *Physica Scripta* 97.7 (2022), p. 072001. DOI: 10.1088/1402-4896/ac6f25. URL: https://doi.org/10.1088/1402-4896/ac6f25.

[52] A. Beroual and M-L. Coulibaly. “Experimental investigation of breakdown voltage of CO2, N2 and SF6 gases, and CO2-SF6 and N2-SF6 mixtures under different voltage waveforms”. In: *2016 IEEE International Power Modulator and High Voltage Conference (IPMHVC)*. 2016, pp. 292–295. DOI: 10.1109/IPMHVC.2016.8012898.

[53] Siddharth Kumar et al. “Electrical Breakdown Study in CO2 and CO2-O2 Mixtures in AC, DC and Pulsed Electric Fields at 0.1–1 MPa Pressure”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 28.1 (2021), pp. 158–166. DOI: 10.1109/TDEI.2020.009115.

[54] Mariusz Stosur et al. “Thermal behaviour analyses of gas-insulated switchgear compartment using thermal network method”. In: *IET Generation, Transmission & Distribution* 10.12 (2016), pp. 2833–2841. DOI: https://doi-org.tudelft.idm.oclc.org/10.1049/iet-gtd.2015.0489. eprint: https://ietresearch-onlinelibrary-wiley-com.tudelft.idm.oclc.org/doi/pdf/10.1049/iet-gtd.2015.0489. URL: https://ietresearch-onlinelibrary-wiley-com.tudelft.idm.oclc.org/doi/abs/10.1049/iet-gtd.2015.0489.

[55] Lujia Chen et al. “Potential of CF3I Gas Mixture as an Insulation Medium in Gas-Insulated Equipment”. In: Oct. 2015. DOI: 10.1109/CEIDP.2015.7352013.

[56] Mehmet Murat Ispirli, Ozcan Kalenderli, and Michael Rock. “The Design and Application of Composite AC & DC and DC & LI High Voltage Test Circuits”. In: *2021 13th International Conference on Electrical and Electronics Engineering (ELECO)*. 2021, pp. 147–151. DOI: 10.23919/ELECO54474.2021.9677794.

[57] E. Volpov. “Dielectric strength coordination and generalized spacer design rules for HVAC/DC SF/sub 6/ gas insulated systems”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 11.6 (2004), pp. 949–963. DOI: 10.1109/TDEI.2004.1387818.

[58] Hongyang Zhou et al. “Insulation Design Rule for a Spacer in SF 6/N 2-filled DC Gas Insulated Apparatus”. In: *CSEE Journal of Power and Energy Systems* 10.2 (2024), pp. 727–735. DOI: 10.17775/CSEEJPES.2020.02100. URL: https://www.sciopen.com/article/10.17775/CSEEJPES.2020.02100.

[59] S. Chakravorti. “Modified E-field analysis around spacers in SF/sub 6/ GIS under DC voltages”. In: *1999 Eleventh International Symposium on High Voltage Engineering*. Vol. 2. 1999, 91–94 vol.2. DOI: 10.1049/cp:19990603.

[60] Andreas Hopf et al. “Dielectric strength of SF6 substitutes, alternative insulation gases and PFC-gas-mixtures”. In: *2017 IEEE Electrical Insulation Conference (EIC)*. 2017, pp. 209–212. DOI: 10.1109/EIC.2017.8004635.

[61] A.P. Purnomoadi, A. Rodrigo Mor, and J.J. Smit. “Spacer flashover in Gas Insulated Switchgear (GIS) with humid SF6 under different electrical stresses”. In: *International Journal of Electrical Power & Energy Systems* 116 (2020), p. 105559. ISSN: 0142-0615. DOI: https://doi.org/10.1016/j.ijepes.2019.105559. URL: https://www.sciencedirect.com/science/article/pii/S0142061519306064.

[62] Yundong Lai et al. “Characteristics of Surface Charge Accumulation on Spacers and Its Influencing Factors”. In: *Electronics* 13.7 (2024). ISSN: 2079-9292. DOI: 10.3390/electronics13071294. URL: https://www.mdpi.com/2079-9292/13/7/1294.

[63] Cong-Thanh Vu et al. “Time constant evaluation of transient AC - DC field distribution”. In: Aug. 2015.

[64] Baohong Guo. “Simulating Positive and Negative Streamer Discharges in Air and in Strongly Attaching Gases”. PhD thesis. Eindhoven University of Technology and Centrum Wiskunde & Informatica (CWI), 2023. URL: https://research.tue.nl/en/publications/simulating-positive-and-negative-streamer-discharges-in-air-and-i/.

[65] Jian Wang et al. “Mechanism Analysis of Particle-Triggered Flashover in Different Gas Dielectrics Under DC Superposition Lightning Impulse Voltage”. In: *IEEE Access* 8 (2020), pp. 182888–182897. DOI: 10.1109/ACCESS.2020.3026695.

[66] Zhousheng Zhang et al. “Multiphysics coupled modelling in HVDC GILs: Critical re-examination of ion mobility selection”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 26.3 (2019), pp. 835–842. DOI: 10.1109/TDEI.2018.007841.

[67] Xiaoang Li et al. “Discharge Characteristics of Insulation Defects in GIS Under AC/LI Superimposed Voltage”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 29.5 (2022), pp. 2017–2025. DOI: 10.1109/TDEI.2022.3201438.

[68] M. S. Kamarudin et al. “Purpose-built test rig for gas insulation breakdown tests under lightning impulse”. In: *2016 IEEE International Conference on Power and Energy (PECon)*. 2016, pp. 333–337. DOI: 10.1109/PECON.2016.7951583.

[69] Haoyang You et al. “Motion and discharge characteristics of metal particles existing in GIS under DC voltage”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 24.2 (2017), pp. 876–885. DOI: 10.1109/TDEI.2017.006210.

[70] Xin Wang et al. “Surface Flashover Characteristics of Epoxy Resin Composites in SF6/CF4 Gas Mixture with DC Voltage”. In: *Energies* 15.13 (2022). ISSN: 1996-1073. DOI: 10.3390/en15134675. URL: https://www.mdpi.com/1996-1073/15/13/4675.

[71] A. Pirker and U. Schichler. “Partial discharges of defects in different insulating gases: N2, CO2, dry air and SF6”. In: *2018 12th International Conference on the Properties and Applications of Dielectric Materials (ICPADM)*. 2018, pp. 140–143. DOI: 10.1109/ICPADM.2018.8401150.

[72] Hyeon-Su Song, Ho-Seung Kim, and Bang-Wook Lee. “Comparison of DC PDIV and BDV of GIS defects between SF6 gas and C4F7N/CO2 gas mixture”. In: *2022 9th International Conference on Condition Monitoring and Diagnosis (CMD)*. 2022, pp. 529–532. DOI: 10.23919/CMD54214.2022.9991555.

[73] *IEC 60071-1: Insulation Co-ordination – Part 1: Definitions, Principles and Rules*. Geneva, Switzerland: International Electrotechnical Commission, 2019.

[74] Kubranur Varli. “Procedures & Challenges When Dimensioning DC Insulators”. In: *INMR (Insulation Network & Market Report)* (June 2025). Accessed: July 5, 2026. URL: https://www.inmr.com/procedures-challenges-when-dimensioning-dc-insulators/.

[75] MatWeb, LLC. *Overview of materials for PMAA*. Accessed: 2026-02-27. URL: https://www.matweb.com/search/DataSheet.aspx?MatGUID=3cb08da2a0054447a3790015b7214d07.

[76] A. Sivathanu Pillai and Reuben Hackam. “Surface flashover of solid insulators in atmospheric air and in vacuum”. In: *Journal of Applied Physics* 58.1 (1985), pp. 146–153. DOI: 10.1063/1.335700.

[77] Markus Saltzer et al. “Observation of space charge dynamics in air under DC electric fields”. In: *2011 Annual Report Conference on Electrical Insulation and Dielectric Phenomena*. 2011, pp. 141–144. DOI: 10.1109/CEIDP.2011.6232616.

[78] H. Löfås and N. Lavesson. “Ion drift simulations of the DC electric field in air around a high voltage bushing”. In: *2017 IEEE Conference on Electrical Insulation and Dielectric Phenomenon (CEIDP)*. 2017, pp. 30–33. DOI: 10.1109/CEIDP.2017.8257457.

[79] Jianfeng Hui et al. “Variation of the Dynamics of Positive Streamer with Pressure and Humidity in Air”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 15.2 (2008), pp. 382–389. DOI: 10.1109/TDEI.2008.4483456.

[80] Hawley Hobbies. *How to Model a Spark Gap in LTSPICE*. https://youtu.be/yiGsnCSDGuA. Accessed: 2026-06-01. 2020.

[81] International Electrotechnical Commission. *IEC 60060-1:2010 - High-voltage test techniques – Part 1: General definitions and test requirements*. Geneva: International Electrotechnical Commission. 2010. URL: https://webstore.iec.ch/publication/2229.

[82] M. Hallas, V. Hinrichsen, and M. Tenzer. “Comparison of Superimposed Voltage Tests with Spark Gap and Coupling Capacitor at a Gas-Insulated Model Arrangement”. In: *Proceedings of the IEEE Conference on Electrical Insulation and Dielectric Phenomena (CEIDP)*. © 2022 IEEE. Hosted on TUprints, TU Darmstadt. 2022. URL: https://tuprints.ulb.tu-darmstadt.de/server/api/core/bitstreams/%2031b2632a-b3e2-4a12-809e-b12d31b25e17/content.

[83] CIGRE Working Group D1.67. *Electric Performance of New Non-SF6 Gases and Gas Mixtures for Gas-Insulated Systems*. Technical Brochure 849. Paris, France: CIGRE, 2021.

[84] Wolfgang Hauschild and Wolfgang Mosch. *Statistical Techniques for High-Voltage Engineering*. IET Power and Energy Series 13. Reprinted 2007. London, United Kingdom: The Institution of Engineering and Technology (IET), 1992. ISBN: 978-0-86341-205-9.

[85] Jingtan Ma et al. “Study on flashover characteristics of insulators in SF6 under combined voltage of DC and lightning impulse”. In: *2017 IEEE Electrical Insulation Conference (EIC)*. 2017, pp. 62–65. DOI: 10.1109/EIC.2017.8004608.

[86] C.T. Vu et al. “DC GIS: Importance of Simulations for the Design and Testing”. In: *CIGRE Session 2016*. D1-102. Paris: CIGRE, 2016.

[87] Guoming Ma et al. “Flashover behavior of cone-type spacers with inhomogeneous temperature distribution in SF6/N2-filled DC-GIL under lightning impulse with DC voltage superimposed”. In: *CSEE Journal of Power and Energy Systems* 6.2 (2020), pp. 427–433. DOI: 10.17775/CSEEJPES.2018.00480.

[88] Wolfgang Hauschild and Eberhard Lemke. *High-Voltage Test and Measuring Techniques*. 2nd ed. Cham, Switzerland: Springer International Publishing, 2019. ISBN: 978-3-319-97459-0. DOI: 10.1007/978-3-319-97460-6.

[89] Mark P. Wilson et al. “Impulse-driven Surface Breakdown Data: A Weibull Statistical Analysis”. In: *IEEE Transactions on Plasma Science* 40.10 (2012), pp. 2449–2456. DOI: 10.1109/TPS.2011.2181172.

[90] Qi Hu et al. “Surface Flashover Induced by Metal Contaminants Adhered to Tri-Post Epoxy Insulators under Superimposed Direct and Lightning Impulse Voltages”. In: *Polymers* 14.7 (2022). ISSN: 2073-4360. DOI: 10.3390/polym14071374. URL: https://www.mdpi.com/2073-4360/14/7/1374.

[91] Boya Zhang et al. “Surface Charging Characteristics of a Real-Sized DC GIS Insulator in Pressurized Clean Air as a Feasible SF6 Alternative”. In: *IEEE Transactions on Power Delivery* PP (Apr. 2024), pp. 1–10. DOI: 10.1109/TPWRD.2024.3391916.

[92] Michael Schueller et al. “Micro discharges in HVDC gas insulated systems”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 22.5 (2015), pp. 2879–2888. DOI: 10.1109/TDEI.2015.004835.

[93] Birgitta Källstrand et al. “DC field distribution around an HVDC cable termination”. In: *2015 IEEE Conference on Electrical Insulation and Dielectric Phenomena (CEIDP)*. 2015, pp. 35–38. DOI: 10.1109/CEIDP.2015.7352109.

[94] Michael Schueller, Ueli Straumann, and Christian Franck. “Role of Ion Sources for Spacer Charging in SF6 Gas Insulated HVDC Systems”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 21 (Feb. 2014), pp. 352–359. DOI: 10.1109/TDEI.2014.6740759.

[95] Josef Kindersberger and Christoph Lederle. “Surface charge decay on insulators in air and sulfurhexafluorid - part I: simulation”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 15.4 (2008), pp. 941–948. DOI: 10.1109/TDEI.2008.4591214.

[96] International Electrotechnical Commission. *IEC 60052:2002 Voltage Measurement by Means of Standard Air Gaps*. Geneva, Switzerland: International Electrotechnical Commission, 2002.

[97] Boxue Du, Jianan Dong, and Hucheng Liang. “Electric field control by permittivity functionally graded and superficially non□linear conductivity materials for DC□GIS spacer”. In: *High Voltage* 7 (Mar. 2022). DOI: 10.1049/hve2.12199.

[98] Yi Luo et al. “Transition of the dominant charge accumulation mechanism at a Gas-solid interface under DC voltage”. In: *IET Generation, Transmission & Distribution* 14.15 (2020), pp. 3078–3088. DOI: https://doi-org.tudelft.idm.oclc.org/10.1049/iet-gtd.2019.1523. eprint: https://ietresearch-onlinelibrary-wiley-com.tudelft.idm.oclc.org/doi/pdf/10.1049/iet-gtd.2019.1523. URL: https://ietresearch-onlinelibrary-wiley-com.tudelft.idm.oclc.org/doi/abs/10.1049/iet-gtd.2019.1523.

[99] Hendrik Hensel, Christoph Jörgens, and Markus Clemens. “Simulation of Permittivity and Conductivity Graded Materials for HVDC GIL for Different Voltage Forms”. In: *Proceedings of the Conference*. arXiv:2308.14405. Wuppertal, Germany, 2023.

[100] Xiaolong Li et al. “Transient surface charge of SF6-filled direct current gas-insulated transmission lines insulator under thermal-electric coupled fields: effects of ambient temperature, load current and gas pressure”. In: *IET Generation, Transmission & Distribution* 16.13 (2022), pp. 2688–2700. DOI: https://doi-org.tudelft.idm.oclc.org/10.1049/gtd2.12483. eprint: https://ietresearch-onlinelibrary-wiley-com.tudelft.idm.oclc.org/doi/pdf/10.1049/gtd2.12483. URL: https://ietresearch-onlinelibrary-wiley-com.tudelft.idm.oclc.org/doi/abs/10.1049/gtd2.12483.

[101] Zhou Hongyang et al. “Impact of temperature on surface charges accumulation on insulators in SF6-filled DC-GIL”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 24 (Feb. 2017), pp. 601–610. DOI: 10.1109/TDEI.2016.005838.

[102] Pinhao Huang et al. “Numerical Simulation of Surface Charge Accumulation on Epoxy Insulator in DC-GIS Considering Temperature Gradient”. In: *2024 IEEE 5th International Conference on Dielectrics (ICD)*. 2024, pp. 1–4. DOI: 10.1109/ICD59037.2024.10613057.

[103] Alexander Pirker and Uwe Schichler. “Partial discharge measurement at DC voltage — Evaluation and characterization by NoDi pattern”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 25.3 (2018), pp. 883–891. DOI: 10.1109/TDEI.2018.006742.

[104] E. Onal. “Breakdown Mechanism of Different Sulphur Hexafluoride Gas Mixtures”. In: *Advances in Materials Science and Engineering* 2018 (2018), p. 3206132. DOI: 10.1155/2018/3206132.

[105] Ruixue Liang et al. “Research on discharge phenomenon caused by cross□adsorption of linear insulating fibre and metal dust under DC voltage”. In: *High Voltage* 7.2 (2020), pp. 269–278. DOI: 10.1049/hve2.12040.

[106] Ayuamira Zahari et al. “Development of Test Vessel for Gas Insulation Breakdown Test”. In: *International Journal of Power Electronics and Drive Systems* 9.2 (2018), pp. 873–879. DOI: 10.11591/ijpeds.v9.i2.pp873-879.

[107] MatWeb, LLC. *Overview of materials for Nylon 66*. Accessed: 2026-02-27. URL: https://www.matweb.com/search/DataSheet.aspx?MatGUID=a864b9f98b734bdaa6abb9ceda93f097.

[108] MatWeb, LLC. *Overview of materials for PTFE*. https://www.matweb.com/search/DataSheet.aspx?MatGUID=4e0b2e88eeba4aaeb18e8820f1444cdb. Accessed: 2026-02-27. 2024.

[109] MatWeb, LLC. *Overview of materials for HDPE*. Accessed: 2026-02-12. 2024. URL: https://www.matweb.com/search/DataSheet.aspx?MatGUID=482765fad3b443169ec28fb6f9606660.

[110] A. Winter and J. Kindersberger. “Stationary resistive field distribution along epoxy resin insulators in air under DC voltage”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 19.5 (2012), pp. 1732–1739. DOI: 10.1109/TDEI.2012.6311522.

[111] Shaohua Cao et al. “Development of ± 550 kV DC GIS Basin Insulator”. In: *High Voltage* (2026). DOI: 10.1049/hve2.70164.

[112] N. Lavesson and C. B. Doiron. “Hybrid Resistive-Capacitive and Ion Drift Model for Solid Gas Dielectrics”. In: *Proceedings of the COMSOL Conference*. Grenoble, France: COMSOL, 2015.

[113] Ueli Straumann, Michael Schuller, and Christian M. Franck. “Theoretical investigation of HVDC disc spacer charging in SF6 gas insulated systems”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 19.6 (2012), pp. 2196–2205. DOI: 10.1109/TDEI.2012.6396980.

[114] Woo Seok Kang et al. “Numerical study on influences of barrier arrangements on dielectric barrier discharge characteristics”. In: *IEEE Transactions on Plasma Science* 31.4 (2003), pp. 504–510. DOI: 10.1109/TPS.2003.815469.

[115] T. Vu-Cong, F. Jacquier, and A. Girodet. “Electric field computation for HVDC GIS/GIL spacer under superimposed impulse conditions”. In: *2019 IEEE Conference on Electrical Insulation and Dielectric Phenomena (CEIDP)*. 2019, pp. 409–412. DOI: 10.1109/CEIDP47102.2019.9009868.

[116] Youping Tu, Geng Chen, and Chuanyang Li. “±100-kV HVDC SF6/N2 Gas-Insulated Transmission Line”. In: *IEEE Transactions on Power Delivery* (June 2019).

[117] Chao Wang et al. “Dielectrically Graded Spacer for 126-kV GIS: Design and Construction Strategy”. In: *IEEE Transactions on Dielectrics and Electrical Insulation* 29.4 (2022), pp. 1590–1598. DOI: 10.1109/TDEI.2022.3185578.

A

Review of Standards

Understanding the dielectric behavior of HVDC GIS systems, as discussed in chapter 3, provides a basis for interpreting the phenomena that occur in DC GIS systems. However, scientific literature alone is insufficient to motivate the design of components and test methodologies. Industrial experience, accumulated through validation and consolidated experiences, defines the testing for the HVDC GIS systems. The goal of this section is to examine the standards to better understand testing choices.

The formalization of HVDC GIS testing has accelerated considerably in the last few years. A significant contribution came from the EU funded PROMOTioN WP15 project, which conducted large scale experimental validation of HVDC GIS systems at $\pm 320\,\text{kV}$ and $\pm 550\,\text{kV}$, supplied by Siemens and Hitachi, respectively. The programme assessed dielectric withstand performance along with long-term simulated test routines, advancing the technology readiness level of HVDC GIS from TRL 7/8 to TRL 9. Consortia such as CIGRE and IEC also compiled experts and experience with HVDC GIS and defined the test sequences, measurement requirements, and acceptance criteria that are needed for composite DC/LI application.

The progress of many key standards/ suggestions from both CIGRE and IEC has been growing, addressing all the steps from HVDC GIS design considerations all the way to measurement setups. Many standards provide a foundation for understanding composite voltage testing or HVDC GIS systems, with the focus of this chapter being the 2 key documents of

- **IEC 600600-1** : High voltage test techniques and definitions
- **CIGRE TB 842** : Dielectric testing of HVDC GIS systems

The review of these documents for composite testing for HVDC GIS systems is presented below with Table A.1 summarizing the other broader set of considered standards and technical brochures relevant to HVDC GIS/ composite voltage testing.

Code	Document title
IEC 60060-1	High-voltage test techniques - Part 1: General terminology and test requirements
IEC 62271-318	High-voltage switchgear and controlgear - Part 318: DC gas-insulated metal-enclosed switchgear for rated voltages including and above 100 kV
IEC 62271-1	High-voltage switchgear and controlgear - Part 1: Common specifications for alternating current switchgear and controlgear
IEC 62271-203	High voltage switchgear and controlgear – Part 203: Gas insulated metal enclosed switchgear for rated voltages above 52 kV
CIGRE TB 842	Dielectric Testing of Gas Insulated HVDC Systems
CIGRE TB 506	Gas Insulated Systems for HVDC Applications
CIGRE TB 757	HVDC GIS: Design, Performance and Testing Considerations
CIGRE TB 957	Latest Developments in HVDC GIS Technology and Testing
PROMOTioN WP15	PROMOTioN Project – Work Package 15: HVDC GIS

Table A.1: Summary of standards and technical documents relevant for composite voltages or HVDC GIS

A.1. IEC 60060-1

A.1.1. DC Voltages

Testing regarding DC is very important for verifying the insulation performance on components under steady-state DC stresses. The testing for HVDC remains slightly mature, for HVDC with the document specifying requirements on generating and measuring DC voltages. The measurement of DC voltages remains pretty straightforward, as the signal that must be measured is slowly varying with essentially no high-frequency components. The recommendation of resistive or capacitive dividers is suggested, with the scale factor of the divider being constant over the full voltage range. The current through the HV arm for dividers must be considered as resistive elements that lose power and heat according to the power law. The definition of DC generation also permits a ripple of at most 3% from the mean voltage to the peak voltage.

A.1.2. LI Voltages

Tests with lightning impulses have been done for many years, and therefore, the process of setup and measurement is very mature. The main goal of the tests regarding LI regards the ability of a device or component to withstand lightning strikes. Lightning events are very fast transient events that last less than 100 μs with large air clearances in a lab to prevent air insulation breakdown. The fast nature of the signal also introduces noisiness, which the standard accounts for with certain operations. The standard characteristics of LI are defined as a front time with 1.2 μs and a tail time (time to half) of 50 μs with a waveform of a combined exponential. The Figure A.1 below shows the waveform of an LI impulse with certain IEC-determined time parameters.

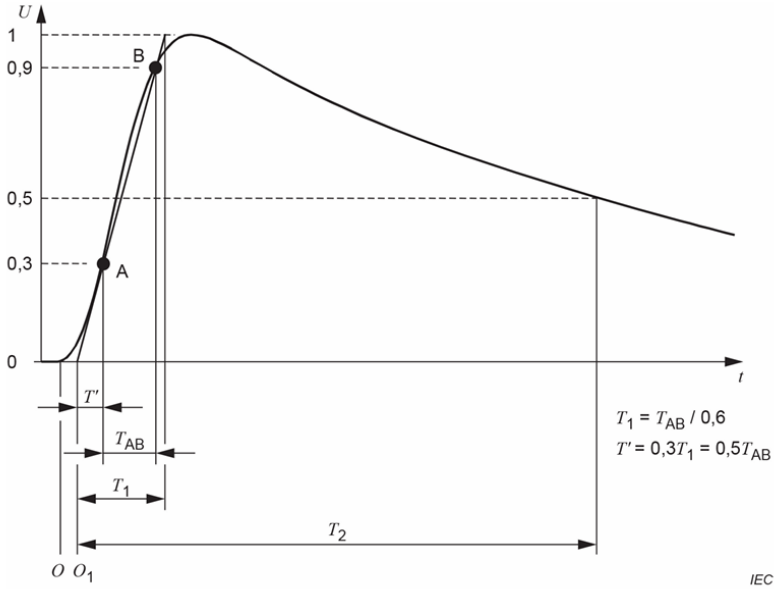


Figure A.1: IEC 60060-1 specified 1.2/50 lightning waveform with T1 and T2

The process described in the standard involves the creation of a base curve fitted on the actual recorded curve, which is then used by finding the difference between the 2 curves, called a residual curve. A filter is applied to get the filtered base curve, which is then added to the base curve to obtain the test curve. The extraction of the time parameters, such as the max voltage of the test curve U_t, the overshoot magnitude Beta', and the front time T1 and tail time T2. The calculation of the T parameters is done through intermediate time parameters and a scale factor, as shown in the Equations below.

$$\beta' = \frac{U_t - U_b}{U_b} \tag{A.1}$$

$$T_1 = 1.67 \cdot (t_{90\%} - t_{30\%}) \tag{A.2}$$

$$t_{O_1} = t_{30\%} - \frac{0.3 \cdot (t_{90\%} - t_{30\%})}{0.6} \tag{A.3}$$

$$T_2 = t_{50\%} - t_{O_1} \tag{A.4}$$

* An important note to also consider is that up until voltages of 800kV, the maximum permissible error for T1 and T2 are $\pm$ 30% and $\pm$ 20% respectively.

A.1.3. Composite Voltages

Tests for both composite and combined waveforms are defined in IEC 60060-1, with the superposition of 2 different waveforms applied on the same terminal of a test object called composite voltages.

The voltages applied are mostly a combination of a slow phenomenon, such as AC or DC, and a fast phenomenon, such as LI or SI. Composite voltages of AC and DC have also been studied, however, to a lesser extent, due to their occurring situationally less frequently. The general methods of protection and measurement, however, are uniquely defined for certain waveforms with the unifying goal to test and verify that a device under test can withstand these events. The basic circuit for testing and measuring the composite voltage is given in the Figure A.2 below.

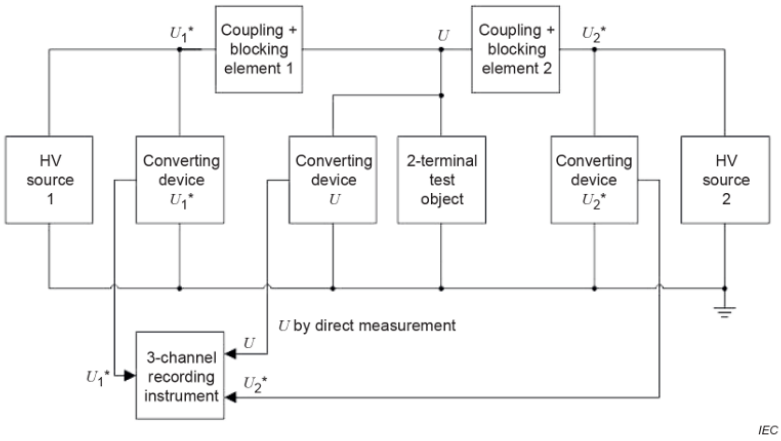


Figure A.2: IEC 60060-1 specified composite voltage testing circuit with 3 measurements

As seen in the circuit above the general measuring circuit for the 2 HV elements must be performed alongside the measurement of the device under test. The measurement of the individual sources is placed before the protection elements and is best done by measurement equipment suited for the specific voltages. The converting device U specified, however, must be chosen to measure across the range of frequencies of both signals, most often through a mixed RC divider. The dividers must also be ensured to hold a uniform scale factor throughout the operational range, as the signals being measured range from low frequency DC to close to 10 Mhz Lightning. The inclusion of protection devices in the form of coupling blocking is done to prevent damage or the influence of one HV source on the other. The complexity in the system depends on the choice of HV source and must be carefully selected to allow for both HV signals to reach the DUT. In the case of this paper, the relevant HV sources are DC and LI, which introduces complexity in blocking the DC signal on the impulse side and blocking the impulse on the DC side. The waveforms shown in Figure 2.3 are the composite voltage waveforms for DC and LI signals.

A.2. CIGRE TB 842

The CIGRE 842 is an important document as it contains industry experience and literature review consolidated into test specifications and recommendations. The most interesting part of the document pertains to the type tests with a focus on the DC insulation tests and superimposed voltage (DC/LI) tests. The type testing for HVDC GIS systems is defined in Chapter 7 in the CIGRE document

A.2.1. DC Insulation Test

The DC insulation systems test is performed to verify the dielectric performance of the GIS under HL steady state conditions, with a maximum electric field occurring at the triple point of the spacer-conductor and gas. The time specified for the testing is required to cover the field transitional time and must be estimated with the dielectric time constant from subsection 4.4.3 previously. The DC fields must also be performed on the insulation under realistic temperature gradients of within $\pm$ 20%. The tests can be scaled to lab settings with permissible interruptions and disconnections as long as the voltages remain representative. The DC insulation test is considered passed if the impulses applied at the withstand levels occur without any visual indications of failure, and visual inspection confirms no flashover tracks.

A.2.2. Superimposed DC/LI test

The superimposed voltage tests are critical for HVDC as they represent some of the worst possible case stress experienced by HVDC GIS systems. The testing of superimposed voltages is recommended to follow the composite test protocol of IEC 60060-1 protocol with a few important clarifications. The initial condition for the superimposed impulse is a DC pre-stress time of 2 hours at the rated DC voltage U_r, which is chosen as a compromise as both the most charge accumulating components become sufficiently charged and following established methods for other HVDC components such as bushings. The pre-stress must always be reapplied at the disconnection of the device or the change of the waveform. The test is specified to be repeated for unipolar and bipolar combinations covering four quadrants of a DC-LI plane. The test requires no flashover for at least 15 impulses with a minimum 1 minute interval between each impulse. The calibration of impulses is allowed with pre shots between 60% and 80% to tune the impulse signal. The standard also describes clearly how the appropriate protections for the DC and impulse circuit must be chosen to ensure the composite voltage across the DUT is a proper superposition. The Figure A.3 below shows an example of a test circuit that uses a blocking capacitor as the impulse blocking element.

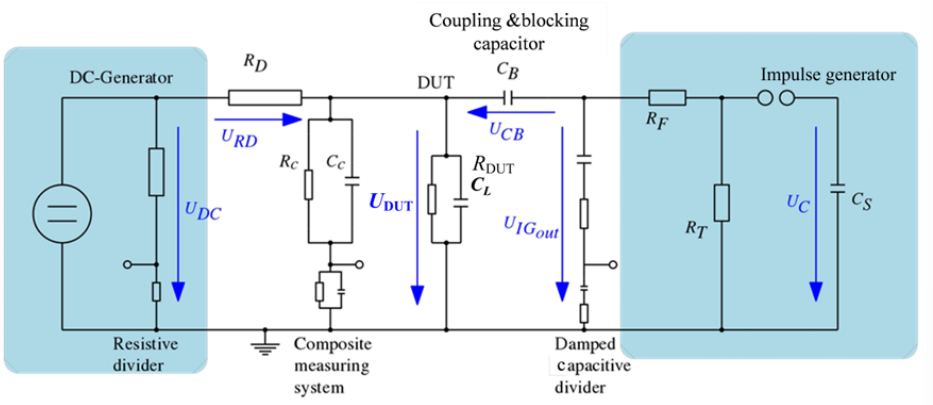


Figure A.3: CIGRE TB 842 specified DC/LI composite testing setup with a blocking capacitor

The blocking of the impulse on the DC generator is done through a sufficiently large resistor. The blocking of DC bias on the impulse generator is specified through either a spark gap or a blocking capacitor. The design of spark gaps is more widely applicable, but with the caveats of spark gap ignition and quenching. The chosen spark gap must ignite at the impulse front at $\leq$ 80% of the LI

peak to avoid distortions. The standard also provides improvements for spark gap setups such as the use of triggered spark gaps, placing the impulse generator's load capacitor in parallel with the test object and with optimized protection elements. The Figure A.4 below shows the use of a spark gap with ignition and quenching.

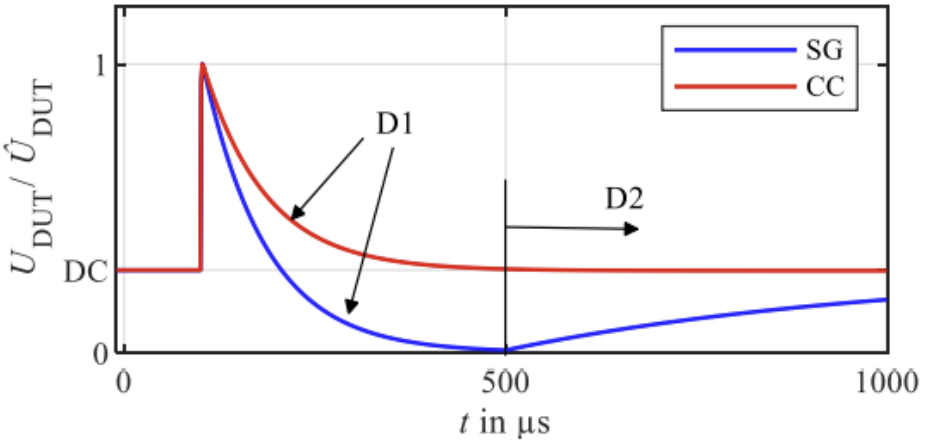


Figure A.4: Image comparing the difference in tails(D1) and discharging to 0kv and returning to DC(D2) for a spark gap and coupling capacitor

The use of a blocking capacitor is preferred due to an essentially infinite impedance for DC voltages, and how the capacitor conducts almost instantaneously and does not discharge the DUT. The design of the circuit, including accounting for voltage drops and efficiency of the impulse source, is considered further in Chapter 6.

The IEC 60060-1 standard is again referenced for accurate measurements of the composite voltages with the direct measurement at the DUT using a universal voltage divider with a constant ratio and sufficient bandwidth compliant with IEC 60060-2. The use of spark gap setups again presents a challenge, as impulse voltage dividers only provide the correct measurement when the spark gap is ignited. The calibration of the time parameters (T1 and T2) must be performed with the DC source disconnected and the blocking element short-circuited for a zero base reference. The standard states that only when the time parameters of the impulse are verified can the DC source be reapplied and the tests executed.

B

Research Based Dimensioning

B.1. DC GIS Simulation-Based Dimensioning

This appendix summarizes the maximum and average electric field values from recent literature on DC GIS simulations. An important note here is that the avg values are not explicitly provided and are estimated, but this is not of much concern, as the tested geometries of spacers and materials already create a huge variance in possible η_{DC} values. The table B.1 below gives the values of DC E_{max} , η_{AC} and η_{DC} where available.

Table B.1: Literature-based electric field parameters for HVDC GIS and GIL systems.

Source	Material / Setup	$\mathbf{E_{max}}$ (kV/mm)	$\mathbf{E_{avg}}$ (kV/mm)	Field Utilization n_{DC}
[97]	FGM Spacer	6.8 (DC)	2.45	0.360
[41]	AC/DC study (AC)	2.5	1.14	0.475
[41]	AC/DC study (DC)	2.4	1.26	0.521
[**IET2020_Peak**]	Peak field analysis	3.97 (DC)	2.0	0.504
[98]	GIS insulator	5.0 (DC)	2.1	0.420
[99]	Graded materials (AC)	2.65	1.1	0.415
[99]	Graded materials (DC)	2.76	1.3	0.471
[100]	DC-GIL insulator (DC)	2.20	1.037	0.472
[101]	SF_6 DC-GIL	5.1 (DC)	2.2	0.431
[39]	HVDC GIS (DC)	2.8	1.2	0.429
[102]	DC GIS accessory	1.5 (DC)	1.03	0.453

The average extracted value for the field utilization ratio is approximately 0.45, which indicates a quasi-uniform field. An important note here is that the goal is not to mimic a single spacer configuration but the overall behavior of the field.

B.2. Test Cell Review

This appendix summarizes the different types of test cells constructed and used in the literature, relevant to either DC or LI. The table below covers the type of feedthrough, the type of voltage used in the cell, and the maximum voltage tested in it. The Table B.2 shows a compiled list of information

available.

Table B.2: Literature-based enclosure and feedthrough parameters for DC and LI test cells.

Source	Voltage Type	Potential Feedthrough	Maximum Voltage (kV)
A Pirker [103]	DC PD	Flange at V	50kV [0.1MPa]
H.S. Song [72]	DC PD	Flange at V	60 kV [0.3Mpa]
A Beroual [52]	DC / LI	Condcutor thorugh	
Kamrudin [68]	DC / LI	Conductor through	67 kV
H You [69]	DC	Conductor through	120 kV [0.4MPa]
X Li [67]	AC / LI	Conductor through	250kV
Onal [104]	AC	Flange at V	32kV [0.4MPa]
L Ruixue [105]	DC	Conductor through	35kV [0.4MPa]
Zahari [106]	AC	Bushing	52kV [0.1MPa]
X Wang [70]	DC	Conductor/spacer	70 kV [0.4MPa]

C

Additional Modelling

In order to verify the proper electrical and relevant workings of a system, the system is chosen to be first simulated. Given the main goal of this thesis, dealing with superimposed DC/LI fields, electric fields, and discharges was considered without the influence of temperature and gas flow dynamics. The section in tandem with Chapter 4 and Chapter 5 was used to design and model a reduced-scale GIS system.

C.1. Simulation Method

The simulation of the geometries and the determination of their components are performed in COMSOL. The electrode and enclosure geometries, the material definitions, and the boundary conditions are first handled using the relevant physics modules, after which a mesh is generated for the solution step, and the results are finally evaluated and post-processed. The general COMSOL workflow is presented in Figure C.1 below.

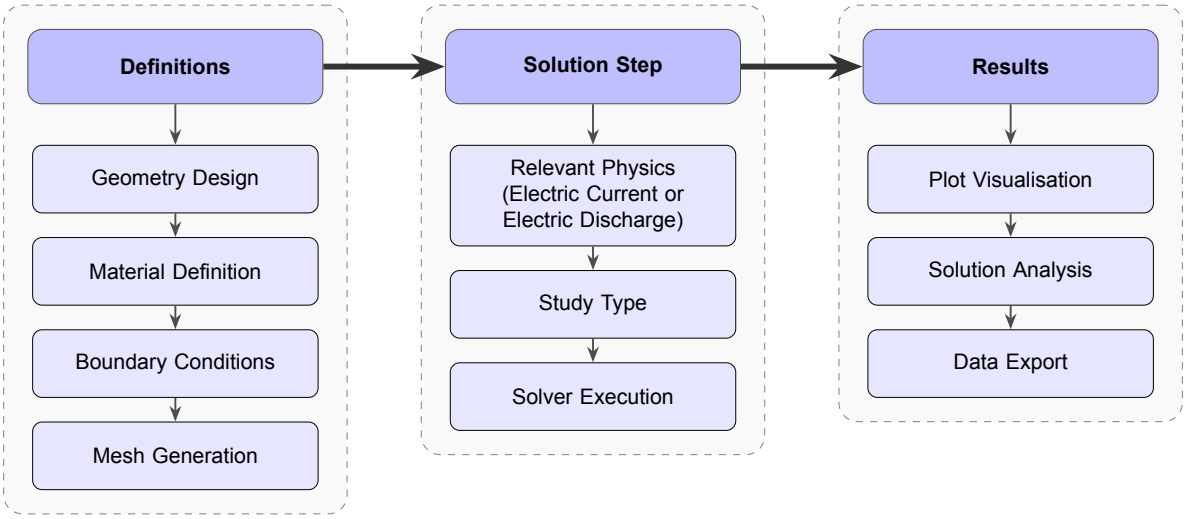
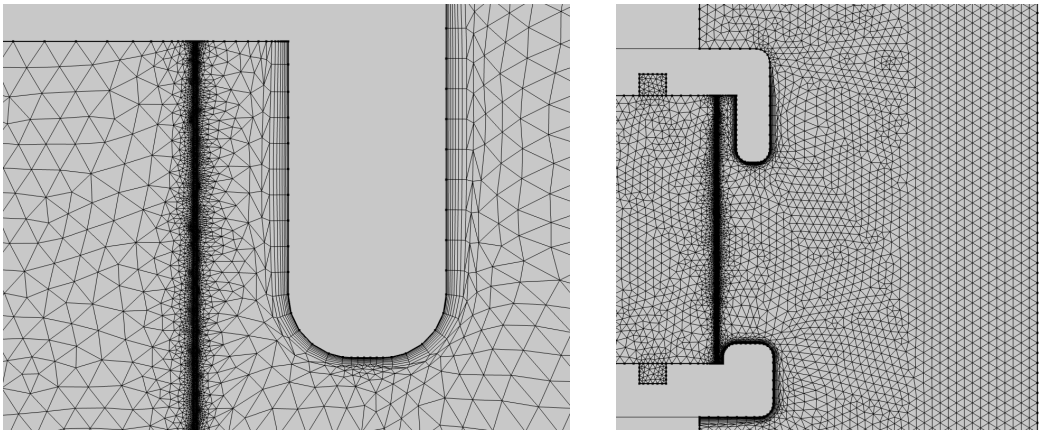


Figure C.1: COMSOL Multiphysics simulation workflow

The mesh definition is important, as element size affects both accuracy and convergence time. Smaller elements are used near the spacer and HV electrode where more non-linearity is expected, and larger triangular elements farther away. Figure C.2 shows the mesh used for the final electrode geometry.



(a) Upclose Mesh **(b)** Whole geometry mesh

Figure C.2: Meshed system chosen for the defined geometry

Boundary layers were applied around the electrodes to improve convergence during ion-drift simulations, with the smallest element size set to 0.0005 mm and the largest to 1.5 mm. Each material is characterized by a permittivity and, for solids, a conductivity, and by electron swarm parameters for gases, all of which must be accurately specified. For the solids used here, permittivities are assumed temperature- and field-independent, with a constant conductivity. All solid parameters are given in Table C.1 below.

Table C.1: Material electrical properties used in the COMSOL model.

Material	ε_r (–)	σ (S/m)	Source
Air (simplified)	1.06	3.59×10^{-20}/ Ion drift	subsection C.2.3
Plexiglass (PMMA)	3.44	3.667×10^{-14}	[75]
Epoxy	5	1×10^{-18} Equation C.1	[34]
Nylon	3.5	3.623×10^{-14}	[107]
PTFE	2.1	1.11×10^{-16}	[108]
HDPE	2.3	2.39×10^{-17}	[109]
Aluminum	1	3.774×10^{7}	COMSOL natively

C.2. Implementation of Charge accumulation

Surface charge accumulation on the gas-solid interface arises from the current density flux on both the spacer and gas sides, both of which must be accurately accounted for [110]. Many works, such as [21, 86, 111, 100, 112], propose methods for simulating gas-medium charge transport using different physics nodes. The primary idea is to address ohmic conduction currents in the Electric Currents module and non-ohmic variations in an alternative TDS, TCC, or EDIS module. Details regarding solver convergence, meshing, and method comparisons are presented in Appendix C. The implementation for this problem is presented below.

C.2.1. Bulk Current Density

The bulk current density J_{bulk}, as mentioned in section 2.3, follows Ohm's law in the expected voltage range and is given by Equation 2.5. It is readily calculated for solid dielectrics using the materials' bulk conductivity in the Electric Currents module, with parameters from Table C.1.

The conductivity of epoxy spacer materials is typically field- and temperature-dependent, with most studies, such as Li et al. [8]and Luo et al. [98], using this model. It is generally described through an extension of Poole's law, as shown in Equation C.1.

$$\sigma(E,T) = \sigma_0 \cdot \exp(\alpha \cdot |E| + \beta \cdot T) \tag{C.1}$$

where σ_0, α and β are constant parameters for a given material and determined through measurements. The conductivity versus field for the commonly used aluminum-filled epoxy resin, with $\sigma_0 = 1 \times 10^{-18}$ [S/m] [8], is shown in Figure C.3.

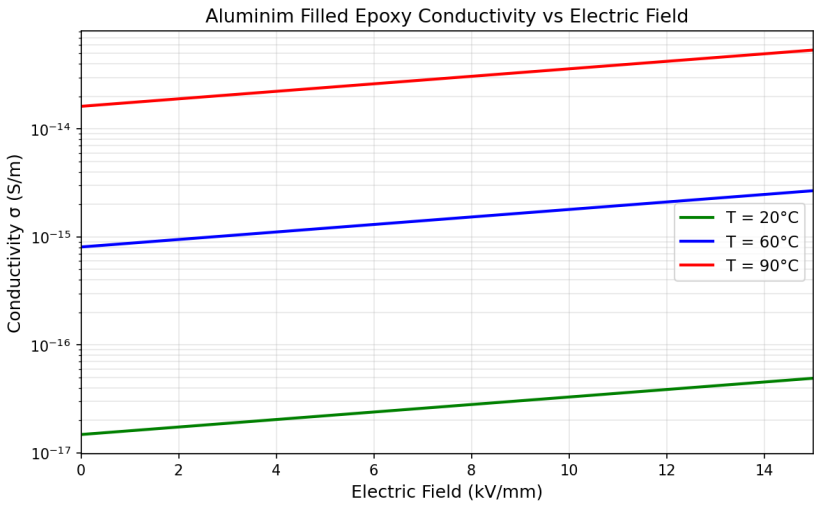


Figure C.3: Aluminum-filled Epoxy conductivities with σ_0 = 2×10^{-18} [S/m], $\alpha = 0.08$ and $\beta = 0.1$ [34] varied by temperature and electric field

The insulation conductivities of insulating materials are often far more temperature- than field-dependent, with CIGRE TB842 [12] reporting an order-of-magnitude increase between 1 and 10 kV, and almost three orders of magnitude from 20 to 90 °C in most insulating materials.

For the reduced-scale superimposed testing, a ZL condition is imposed [12], so no current is applied to the conductor, and no temperature gradient is established. The maximum expected spacer field at reduced scale is therefore under 4 kV/mm in the worst case, as dimensioned for 3 bar in Section 4.2, so conductivity does not vary significantly over this range. These field and temperature simplifications allow the use of a single material conductivity at 20 °C.

Typical GIS systems use epoxy resins with different fillers, and σ_0 between 1×10^{-14} and 1×10^{-20} [S/m] as reported by Lorenzi et al. [34]. In the time frame of this thesis, it was not possible to manufacture or procure the material, and therefore the choice was made to use insulators with a similar volume conductivity. The two considered materials are Nylon and PTFE, which were readily available at the TU Delft HV lab. The goal of the platform is to be able to test different spacer materials, and the goal of the thesis is verification

As the epoxy resin could not be procured, and the aim of this work is the design and building of the test platform, two insulator materials available in the HV lab with equivalent conductivities were simulated instead. Two recommendations are made for future work:

1. Order aluminum oxide-filled epoxy resin samples directly from a GIS spacer manufacturer or specialty epoxy supplier, matching the target σ_0 and ε_r ranges in Table C.1.
2. Alternatively, characterize the bulk conductivity and permittivity through measuremtnes of the available HV lab insulators directly and use them as a substitute for the aluminum-filled epoxy.

C.2.2. Surface Current Density

Surface conductivity follows a similar exponential trend but is tied to the tangential field[34], following an extension of Poole's formulas from Section 2.3. Equation C.2 gives the tangential field(E_t) dependent surface conductivity.

$$\sigma_{surf}(E) = \sigma_{surf0} \cdot \exp(\alpha \cdot |E_t|) \tag{C.2}$$

Surface conductivity depends strongly on the interfacial gas, insulating material, and material condition; however, for most epoxies γ_{s0} is assumed to be one to two orders of magnitude below the bulk conductivity σ_0, and α is empirically estimated at 1.2 to 1.4 mm·k/V for epoxy spacers [34]. In many studies, surface conductivity is ignored, as its current density is lower than the gas or bulk normal contribution [62, 113]. It is not considered in this work, though the method was tested following Lorenzi et al. [34] by introducing a 0.05 mm surface layer (d) on the insulator with a converted surface volume conductivity of $\gamma_s^* = \frac{\gamma_s}{d}$ [S/m].

C.2.3. Gas Current Density

According to Lavenson et al. [112], gas conduction differs from that of solids as ion transport is the primary factor governing conduction current. Below the critical field (2.5 kV/mm for 1 bar dry air), conduction can be modeled primarily through ion transport, as streamer discharge does not yet occur, with the current depending on the ion production rate, recombination rate, and gas pressure. As all substitute gases considered are electronegative and readily absorb free electrons, ion modeling is acceptable for the chosen operational DC field ranges below the critical field [66]. Gas conduction is also non-ohmic, as seen in Figure C.4, and depends on the applied voltage. A simplified model that accounts for positive and negative ion motion is described here and implemented via the drift-diffusion equations in Equation C.4.

$$\frac{\partial N_n}{\partial t} = S - RN_pN_n - \nabla \cdot \left(N_n \mu_p n \vec{E} - D_n \nabla N_n \right) \tag{C.3}$$

$$\frac{\partial N_n}{\partial t} = \underbrace{S}_{\text{generation}} - \underbrace{RN_pN_n}_{\text{recombination}} - \nabla \cdot \left(\underbrace{-N_n\mu_n\vec{E}}_{\text{drift}} - \underbrace{D_n\nabla N_n}_{\text{diffusion}} \right) \tag{C.4}$$

- S is the gas ion pair generation rate (IP/cm^3)
- R is the gas recombination rate (m^3/s)
- N_p, N_n are the concentration of positive and negative ions (1/m^3)
- μ_p, μ_n are the mobility of positive and negative ions (cm^2/(V s))
- D_p, D_n are the diffusion coefficients of positive and negative ions (m^2/s)

The ion diffusion coefficient is given by the Einstein relation in Equation C.5.

$$D_{p,n} = \frac{k_B T}{e_0} \mu_{p,n} \tag{C.5}$$

This drift-diffusion model suits the absence of a temperature gradient, as it excludes convection and radiation terms. For the operational fields simulated, drift vastly dominates diffusion when the ratio $\frac{D_{p,n}}{\mu_{p,n}} << 1$ V [113]. At 1 bar dry air, μ_p and μ_n are 2.34 and 2.70 cm^2/(V·s) respectively, and the recombination coefficient R is 1.7×10^{-6} cm^3/s [114].

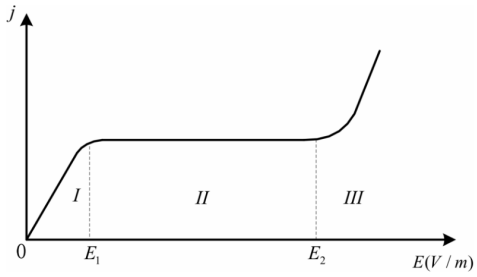


Figure C.4: Gas conduction current linearity for applied voltages [66]

The ion pair generation rate S depends on environmental conditions and location; under natural ionization at 1 bar, it is empirically estimated at approximately 10 IP/(cm^3·s) [91, 95]. At higher internal pressure, the increased molecular density raises the recombination rate R and lowers the ion mobility, while the ion pair generation S approximately doubles. As the mobility does not significantly affect the saturation current, it is left unchanged, and the assumed values are $S = 2 \times 10^7$ IP/(m^{3}s) and $R = 3 \times 10^{-12}$ m^3/s [91]. As shown by Luo et al. [98], natural ionization rates strongly influence the conduction component of charge accumulation; the effect of different generation rates on the gas conduction current normal to a nylon insulator is presented in Figure C.5.

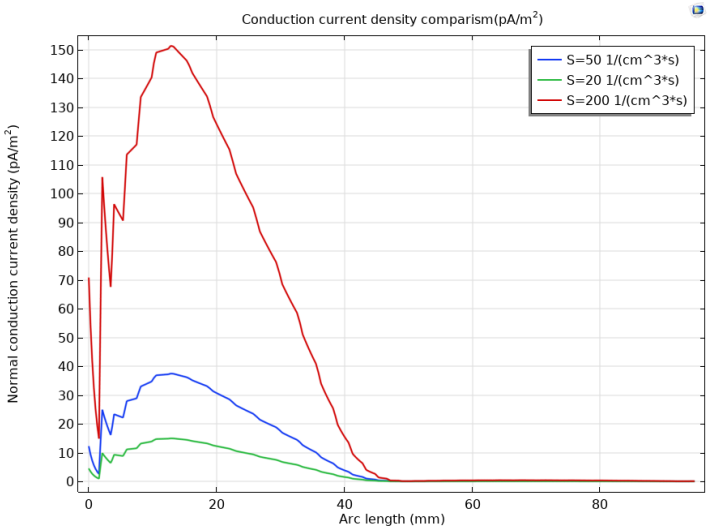


Figure C.5: Conduction Current on an insulator surface for different Ion generation rates $1/(cm^3 * s)$

The gas-domain potential is a function of the charges and is obtained from the Poisson equation in Equation C.6.

$$\nabla^2 U = -\frac{\rho}{\varepsilon_{air}} = -\frac{e \cdot (N_p - N_n)}{\varepsilon_{air}} \tag{C.6}$$

In the gas domain, ion concentration is assumed volume-dependent and ions are generated primarily by background ionization. In practice, electrode surfaces are not perfectly flat, and in real GIS systems field emission and secondary electron emission under high fields deposit charge that increases the gas-volume ion count and can raise surface charge accumulation. This is often ignored in simulations,

as sufficient electrode smoothness and low fields yield negligible emission [92].

The initial ion density is approximated as $\sqrt{\frac{S}{R}}$ to reduce computation time [67]. The electrode ion-density boundary conditions are given in Equation C.7.

$$\text{Outflow: } \begin{cases} N_p = 0 \\ \nabla N_n = 0 \end{cases} \qquad \text{Inflow: } \begin{cases} N_n = 0 \\ \nabla N_p = 0 \end{cases} \tag{C.7}$$

The problem was tackled using a method similar to that of Lavesson et al. [112] where the materials for the gas domain were set very low 1×10^{-25} [S/m] and a current flux density was implemented into the electric currents module through a boundary current source on the gas-solid interface. The surface charge computed per timestep is also fed into the electric discharge module through a surface charge density on the spacer surface. The process of solving the coupled problem is given in Figure C.6

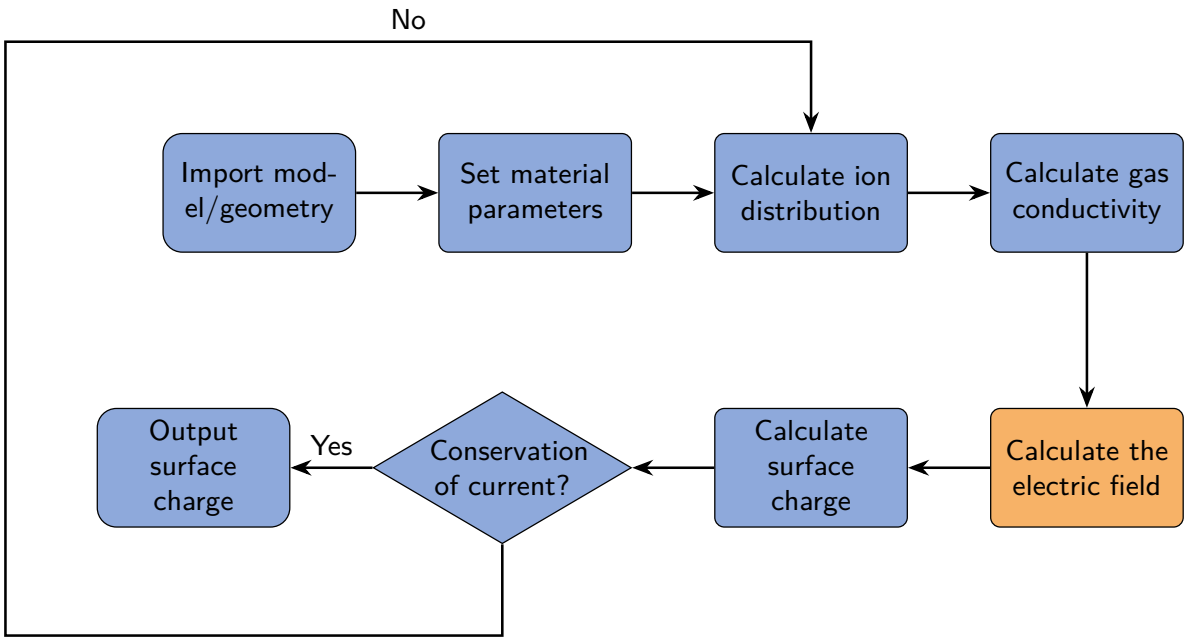


Figure C.6: Flowchart for simulation method used with coupled electric currents and electric discharge interface

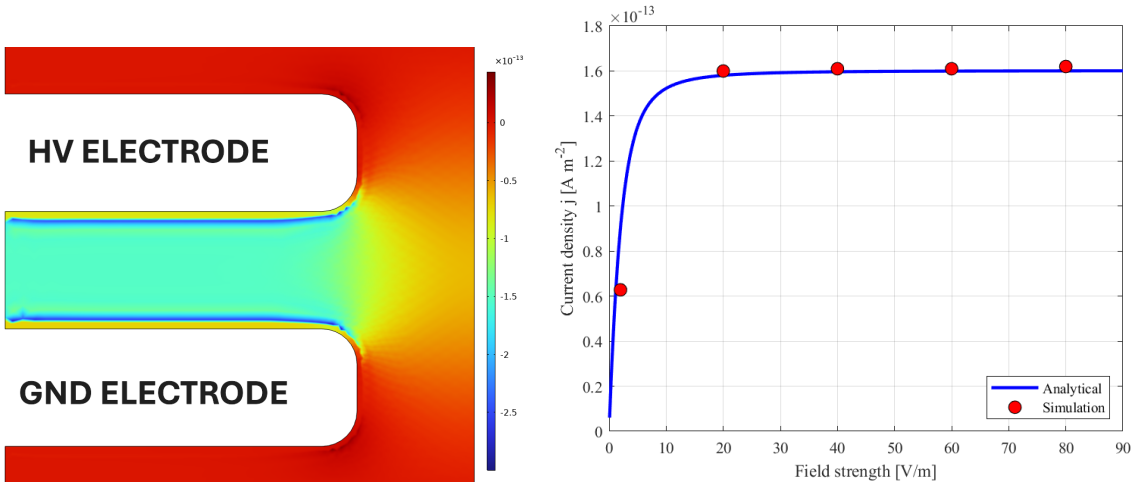
C.2.4. Model verification using Analytical Formula

In a finite gas volume, the conduction process is determined by the recombination rate (R), ion generation rate (S), and ion transport between the electrodes. For 2 parallel plate electrodes separated by a distance d, as shown in Figure C.7a, the field lines between the plates are uniform and the field magnitude is constant throughout the gap. Given sufficient field strengths, the ions are accelerated towards the electrodes and are removed from the area. To ensure that the ion transport equations are accurate, it is important to verify this behavior and compare it to an analytical formula. Equation C.8 shows the analytically derived solution for the gas current density in this configuration, taken from the work of Engel et al.[23]

$$j = eY\left[\sqrt{1+\frac{2d}{Y}}-1\right], \tag{C.8}$$

$$Y = \frac{(\mu^+ + \mu^-)^2 E^2}{2Rd}, \tag{C.9}$$

where e is the elementary charge 1.6×10^{-19} [C], d is the distance between the 2 electrodes in m, E is the field strength, μ^+ and μ^- are the positive and negative ion mobilities, and R is the ion-ion recombination rate. This equation is solved in MATLAB, and Figure C.7 shows the comparison of the ion drift equations against the COMSOL simulation.



(a) Simulation setup **(b)** MATLAB verification

Figure C.7: Gas current ohmic and saturation behavior validation for a parallel plate electrode

As seen in the plots above, the current saturation from the simulation occurs at very low E-fields and closely matches the simulation results, especially in the saturation region, with an error of 2.25% at 20 V/m. Given that most operational voltages in the study remain in the saturation region, a high degree of confidence can be placed in the saturation value of the gas conduction current density.

It is important to acknowledge that aspects of the simulation do not accurately represent surface charging, as simplifications are made in the material properties and physical effects. Factors such as electrode field emission and material charge trapping, which occur in real DC GIS, are not accounted for; however, no comprehensive model simulating all these phenomena together was found in the literature.

C.3. Spacer: Aluminum Filled epoxy Resin

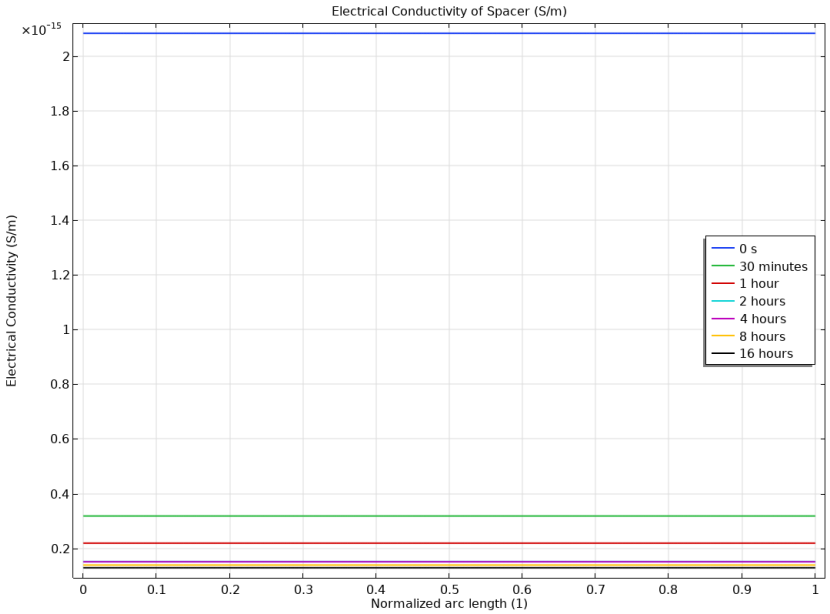
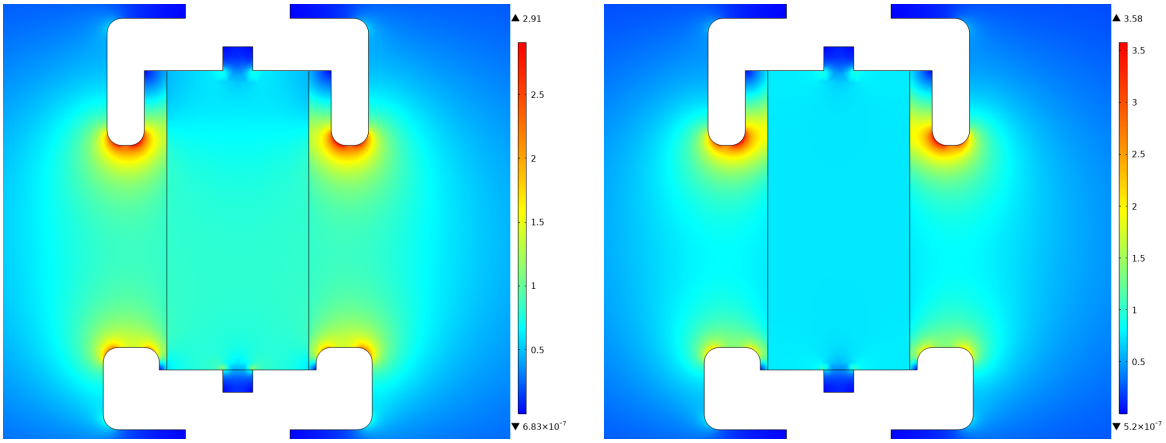


Figure C.8: Electrical Conductivity of Epoxy Resin [115]



(a) Potential Contour

(b) Field streamlines

Figure C.9: Capacitive to resistive transition with Epoxy Resin model[115]

C.4. Electrode: Modified Parallel Plate

The parallel-plate configuration is the simplest setup type, used in many studies, such as those by Jingtan and Volpov [48, 57], and is chosen to mimic a higher field utilization factor. In this scenario, there exists no normal component of the field on the spacer and therefore it does not suffer from large magnitudes of charge accumulation. The triple point stresses, however, are very great due to material imperfections and/or the lack of mounting pressure. Studies such as those by Chakravorti et al. and Youping et al. [59, 116] include a metal divot to reduce triple-junction stress as a field-management strategy in DC GIS spacers. Figure C.10 shows the COMSOL implementation of this electrode and spacer geometry.

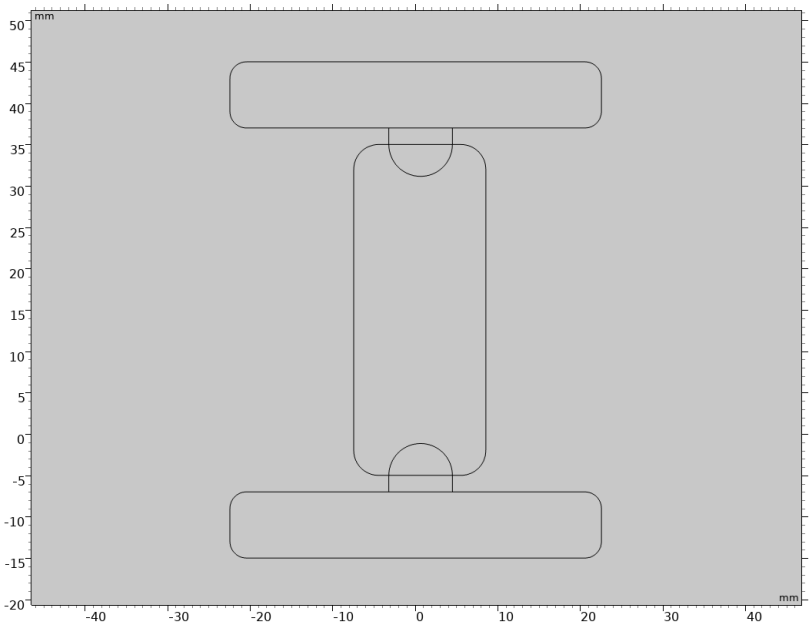
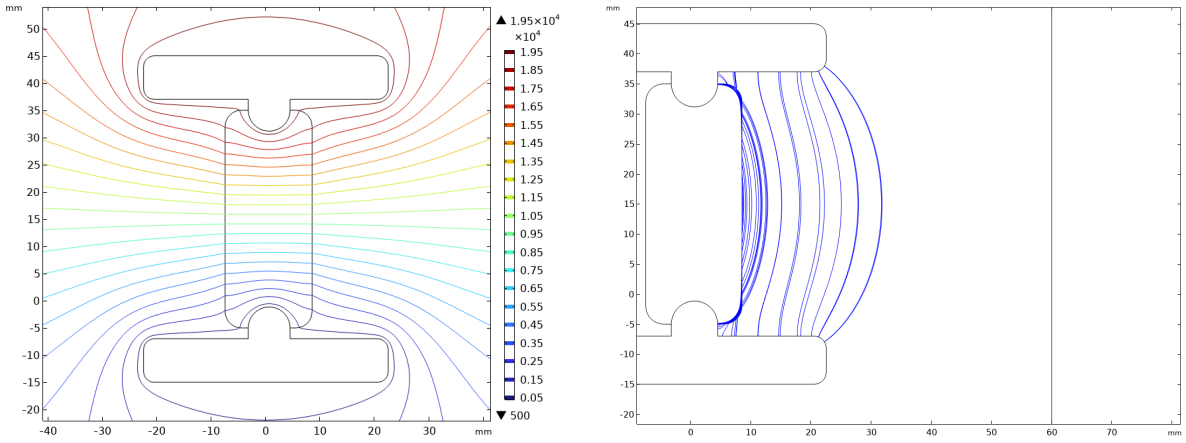


Figure C.10: COMSOL model of parallel plate electrode geometry

The introduction of the divots and the separation of the spacer from the electrodes prevents extreme field enhancements at the triple junction and yield a field utilization factor closer to that of the quasi-homogeneous case found in real GIS systems. The chosen materials are air at 1 bar for the surrounding gas, aluminum for the metal electrodes, and nylon 6 for the spacer. A spacer height of 40 mm is used, consistent with Chapter 4, to simplify comparisons.

C.4.1. Field Simulations

The goal of the field simulations, similar to chapter 4, is to view the fields across the spacer and gas gap for both DC and DC/LI fields. The considered field magnitudes are +30 kV and 150 kV, respectively. The simulation methodology for charges and DC/LI is presented in section C.1. The potential and field contour line plots of the setup for +30 kV DC are given in Figure C.11.

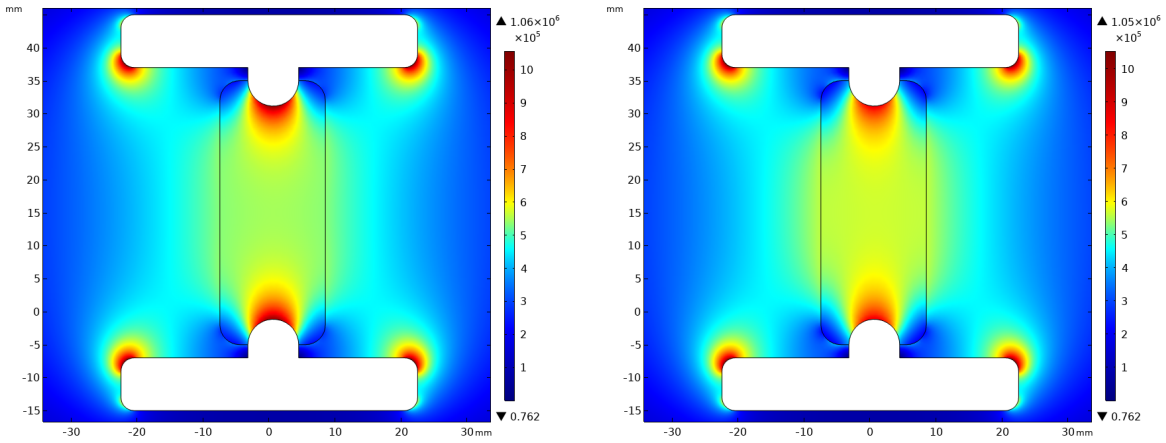


(a) Potential Contour

(b) Field streamlines

Figure C.11: COMSOL modified parallel plate simulation for +30 kV DC

The potential streamlines are curved from the introduction of the metallic insert and become more parallel further away from it. At DC steady state, the field near the spacer bends and follows the spacer surface, attributed to the metallic insert and charge accumulated on the upper and lower spacer surfaces. Curved field lines are also observed at the edge of the metallic plates due to their finite length and edge rounding. The electric field map for transitional AC and steady state DC is shown in Figure C.12.



(a) AC field distribuiton **(b)** DC field distribution

Figure C.12: FEM results parallel plate comparison: AC (left) and DC (right).

A strong field is visible in the center of the spacer through the divots, as expected given the closest distance. The edges of the electrodes also experience peaks from their finite length. The benefit of the model is that fields near the triple junctions on the HV and GND electrodes are reduced; however, a new problem arises from the high normal component on the spacer and corresponding surface charge accumulation. Figure C.13 shows the field components across the spacer for transitional AC and steady state DC.

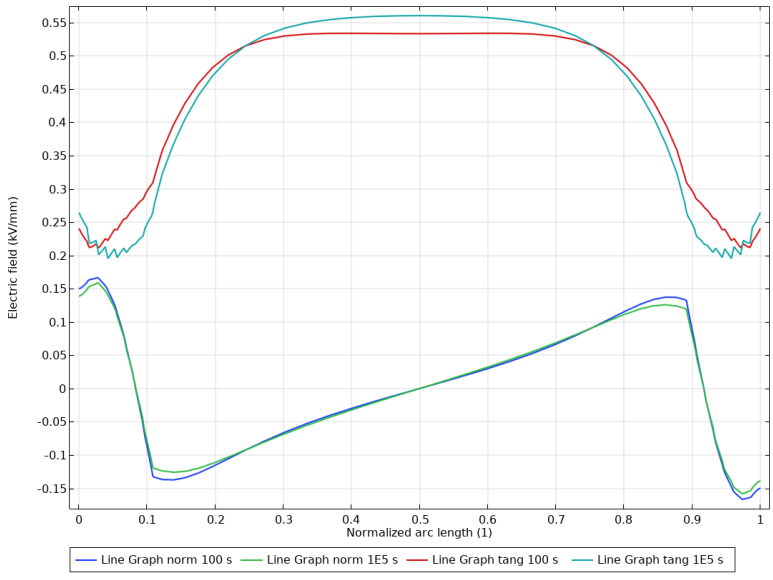


Figure C.13: Field components across spacer for AC and DC given a +30kV DC

Both the normal and tangential field components redistribute, with the normal component peaking at 0.12 kV near the contact with the HV and ground electrode. The field shape of the normal and tangential components does not match that of a disc spacer, as targeted in section 4.2, since the peak field is inside the material rather than lower than the electrode field as required.

C.4.2. DC/LI Simulations

The simulation for the DC/LI superimposed stress is performed as prescribed in Appendix C, using 30 kV and 150 kV. Figure C.14 shows the field simulations for both polarities of superimposed DC/LI.

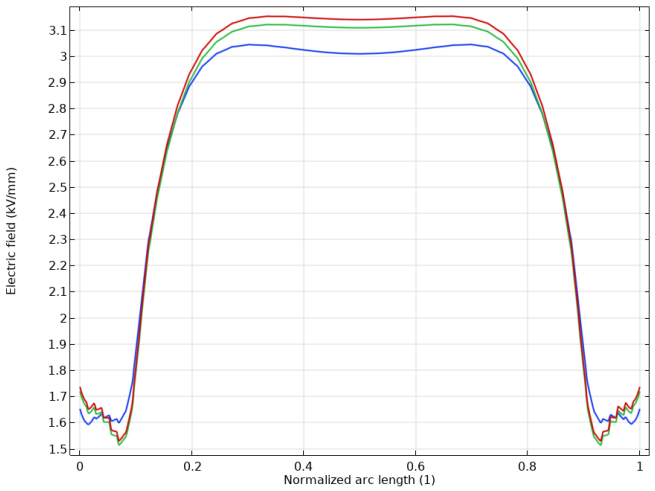
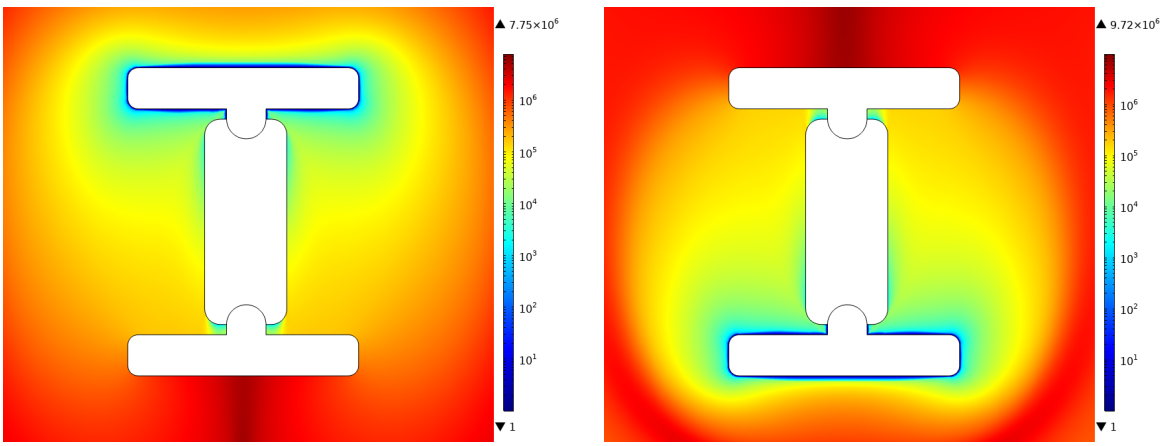


Figure C.14: Field simulation for different DC/LI stresses given nylon spacer

C.4.3. Charge Simulations

The charge simulation is solved using the coupled approach mentioned in Appendix C, with the same air and material parameters. Figure C.15 and Figure C.16 show the steady state ion densities and surface charge density.



(a) N_p concentration

(b) N_n concentration

Figure C.15: Ion densities simulated for +30 kV DC

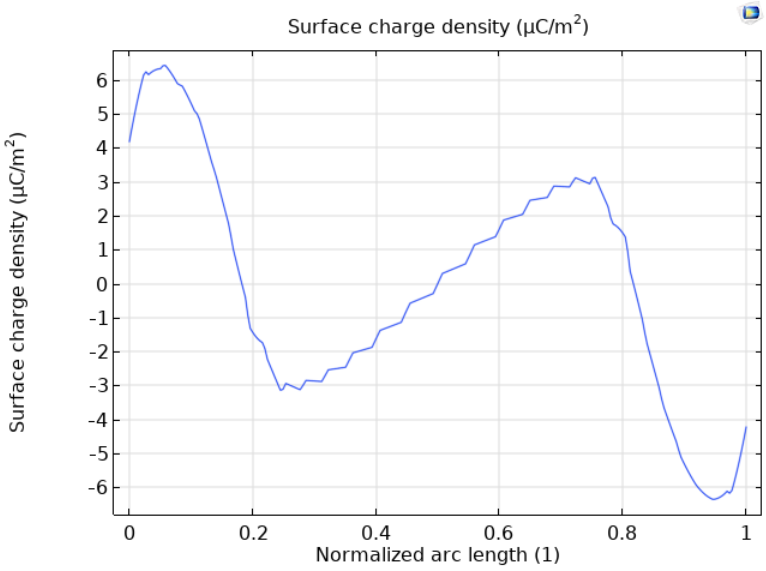


Figure C.16: FEM simulation of the surface charge across the spacer for +30 kV DC

The ion distribution follows the field lines, with positive and negative ions accumulating at the GND and HV electrode, respectively. The charge in the gas at steady state is small (20 pC/m^3), with gas conductivity equivalent to the BP electrode case. The surface charge shows two distinct peaks where the normal field component is greatest, with a magnitude of 6.3 $\frac{\mu C}{m^2}$ at +30kV DC. Since the field profile did not match the target disc spacer geometry from Wu [51] and the gas fields were not lower than spacer surface fields, this model was not chosen.

C.5. Electrode: Modified Pinch Plate

The Ingrained Insulator geometry modifies the pinch plates used in surface flashover studies, such as by Wu et al. [51], offering a high tangential component across the insulator surface to capture flashover behavior. The flat pinch plate concept was rotated to be axisymmetric. Figure C.17 shows the COMSOL implementation of the ingrained insulator with the spacer setup.

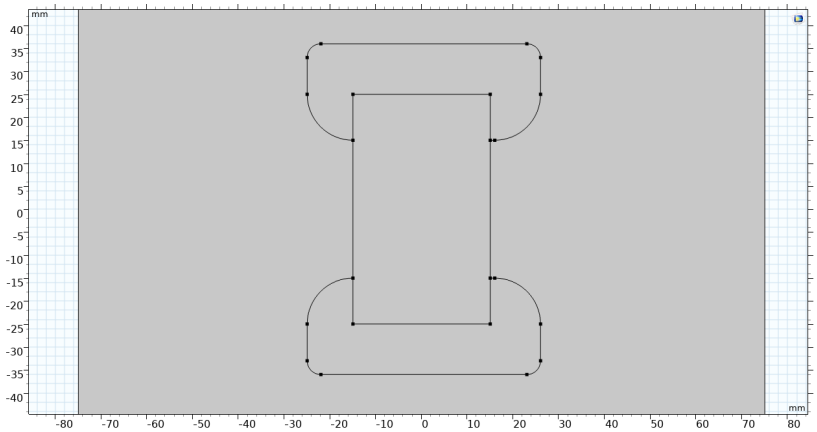
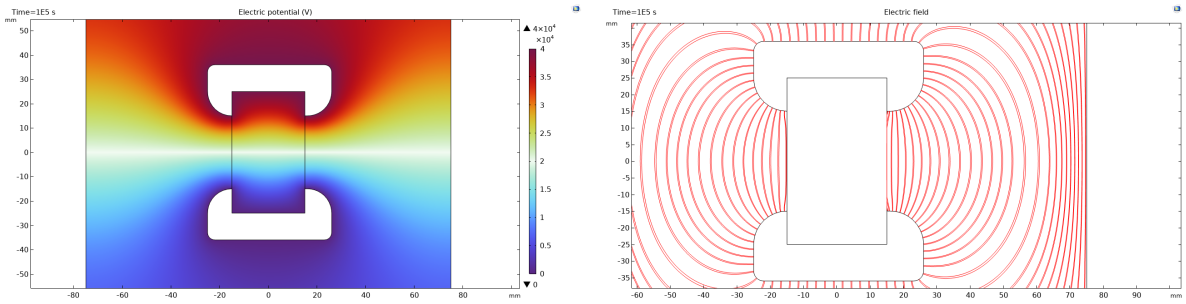


Figure C.17: COMSOL setup of pinch plate geometry

The spacer length is maintained at 40mm, with a gas gap of 30mm. The chosen design did not include any divots or separation, and a triple junction stress is visible.

C.5.1. Field Simulations

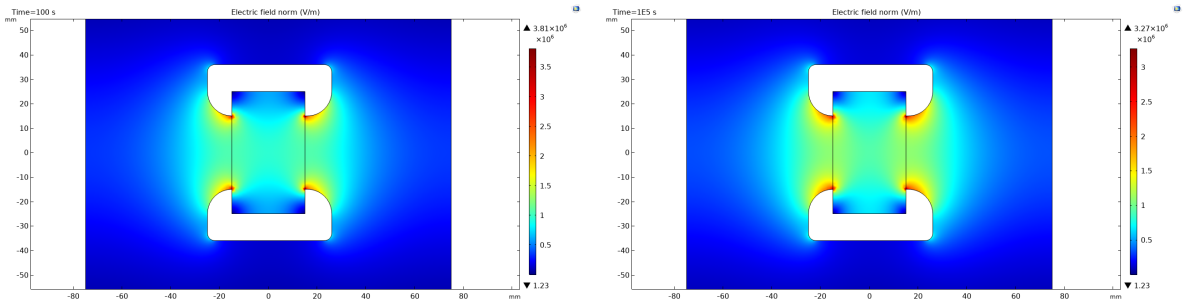
The potential and field contour line plots for +30kV DC are given in Figure C.18.



(a) Voltage potential streamlines **(b)** Electric field distribution

Figure C.18: COMSOL parallel plate comparison: Potential streamlines(left) and Field contours (right)

The voltage bends around the top electrodes into the solid material due to the electrode shape. The streamlines near the spacer run mostly parallel, indicating a high tangential component compared to normal, and thus low expected charge accumulation compared to the other models. The transition from AC capacitive to DC steady state is shown in Figure C.19.



(a) AC field distribuiton **(b)** DC field distribution

Figure C.19: FEM results pinch plate comparison: AC (left) and DC (right).

The strongest field component is near the triple junction, with the field redistributing away from the surface. The peak field value reduces from 3.81 kV/mm to 3.27 kV/mm due to accumulation of homopolar charges at the HV and GND junction. Figure C.20 shows the field components at steady state DC.

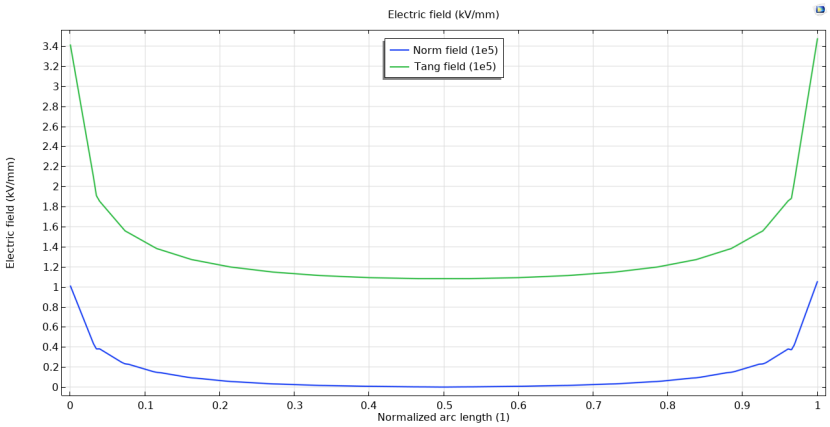


Figure C.20: DC field components

The tangential component is vastly greater than the normal component on the spacer, as the field lines between the electrodes near the spacer are mostly perpendicular. The fields are strongest at both the HV and GND triple junction.

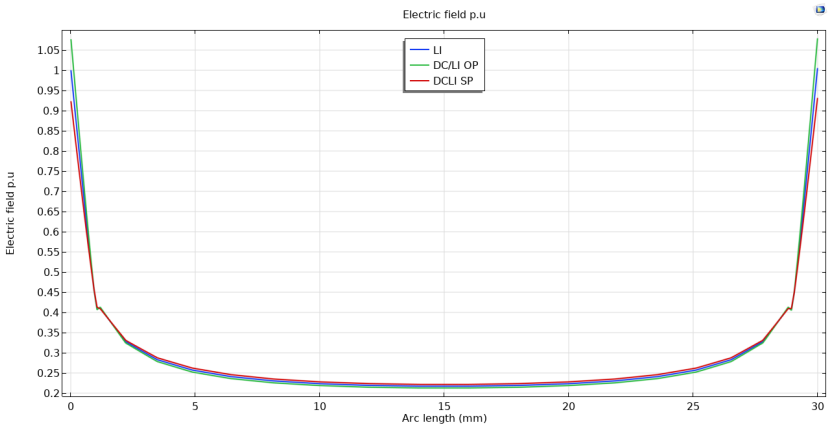
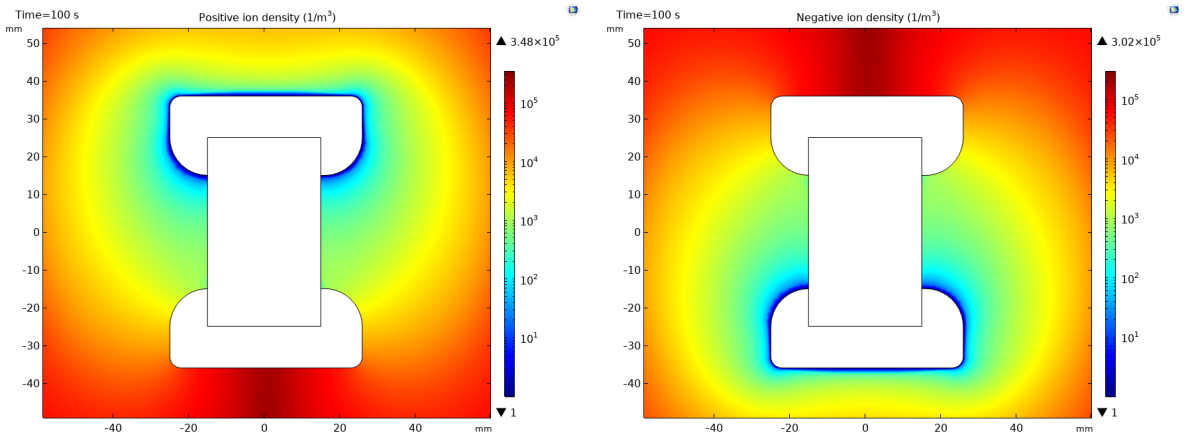


Figure C.21: DC/LI comparims

C.5.2. Charge Simulations

The charge simulation for the pinch plate follows a similar method, with ion density used to determine gas conduction and the bulk/surface components solved ohmically. Figure C.22 shows the simplified ion transport solved to DC steady state.



(a) pos ion distribution **(b)** negative ion distribution

Figure C.22: steady state ion distribution

As with the previous case, ion concentrations follow the electric field, with positive ions flowing away from the HV electrode and vice versa for the GND electrode. Figure C.23 shows the steady state charge accumulation across the spacer.

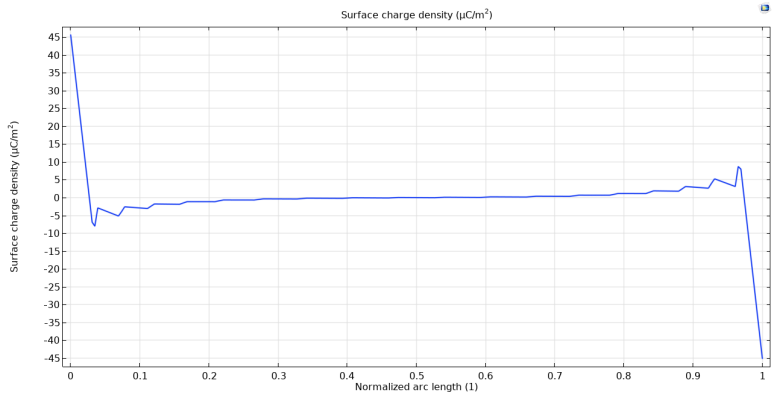


Figure C.23: FEM simulation of the surface charge across the spacer for +30 kV DC

The charge accumulation is primarily focused near the electrodes; the tangential-to-normal field ratio means little charge accumulates in the middle of the spacer. While this model approximates the high tangential fields used for surface flashover tests, it violates the design requirement of both reducing triple junction fields and lowering fields across the spacer, and was therefore not chosen.

C.6. DC GIS Model Simulation

To verify design principles and observe field/charge accumulation behavior in a real DC GIS system, a basin spacer model was selected from Xiaolong et al.[100], representing a realistic DC GIS basin spacer geometry used to validate simulation principles under DC stress. Figure C.24 shows the model used for the COMSOL simulations.

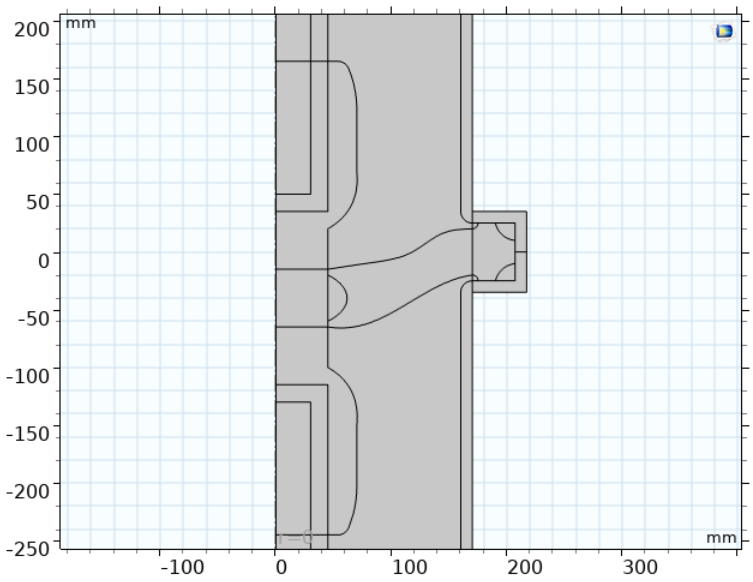
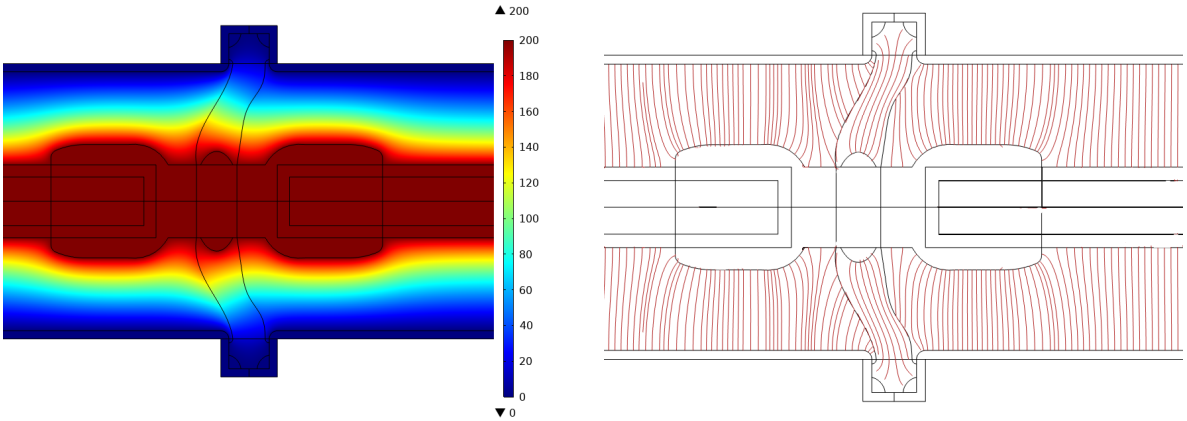


Figure C.24: Scale accurate COMSOL setup of the simplified floating enclosure filled with technical air

The basin spacer is rated for 200kV and includes the HV shielding, GND divot, and ingrained electrode design considered in previous sections. The conductor has a radius of 45 mm and an outer shell of 160mm, with the spacer shape taken from the paper.

C.6.1. Field Simulations

The field simulations were performed at the rated voltage of 200 kV and a lightning-rated voltage of 600 kV. The capacitive distribution depends on the relative permittivity $\epsilon_r = 5.5$ of the epoxy spacer, with the resistive distribution based on a conductivity of 4×10^{-16} [S/m]. Figure C.25 shows the potential and field streamlines for the basin spacer.



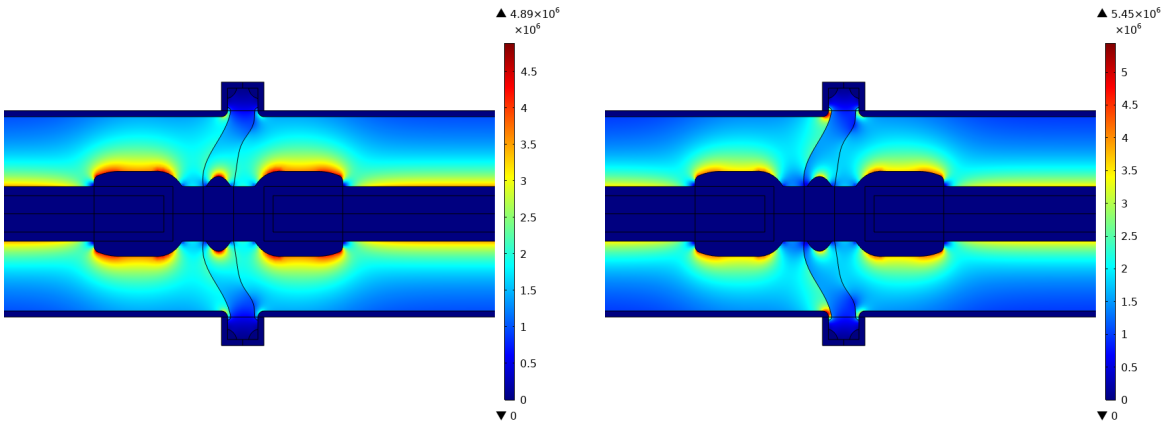
(a) DC potential contour

(b) DC field streamline

Figure C.25: Model GIS steady state potential and field distribution for an applied +200kV

The potential contour curves with the shape of the electrode. The field streamlines depend on the spacer side, with the concave side (facing the HV conductor) showing a higher normal component and the convex side experiencing higher tangential fields. This agrees with other non-symmetric spacer

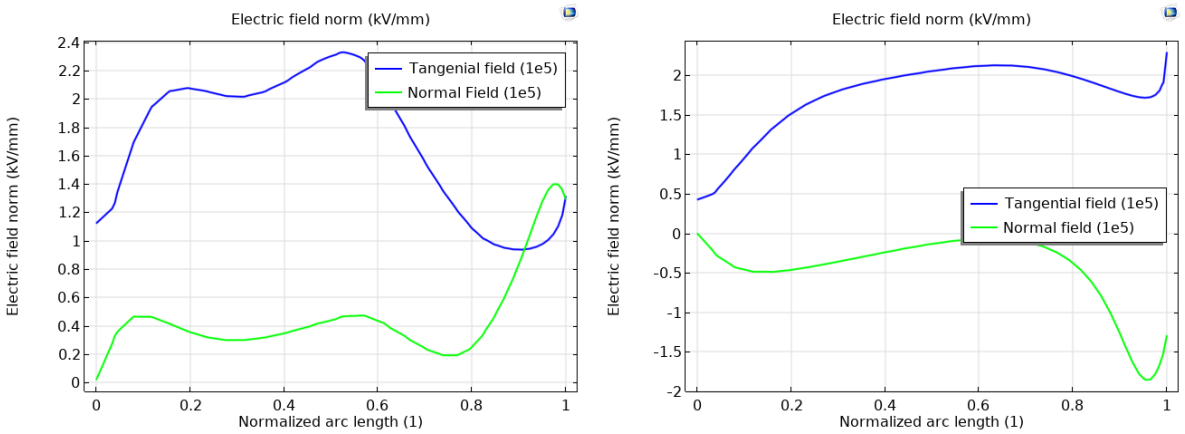
simulations, where the concave side is typically the insulation's weak point. Figure C.26 shows the capacitive to resistive distribution.



(a) AC field distribuiton **(b)** DC field distribution

Figure C.26: Model GIS field transition for applied voltage of +200 kV

The field maximum of the DC GIS spacer is 4.89 kV/mm for the capacitive field and 5.45 kV/mm for the resistive field, respectively. The increase indicates the effect of charge accumulation across the spacer surface. Figure C.27 shows the field components over the spacer at steady state.

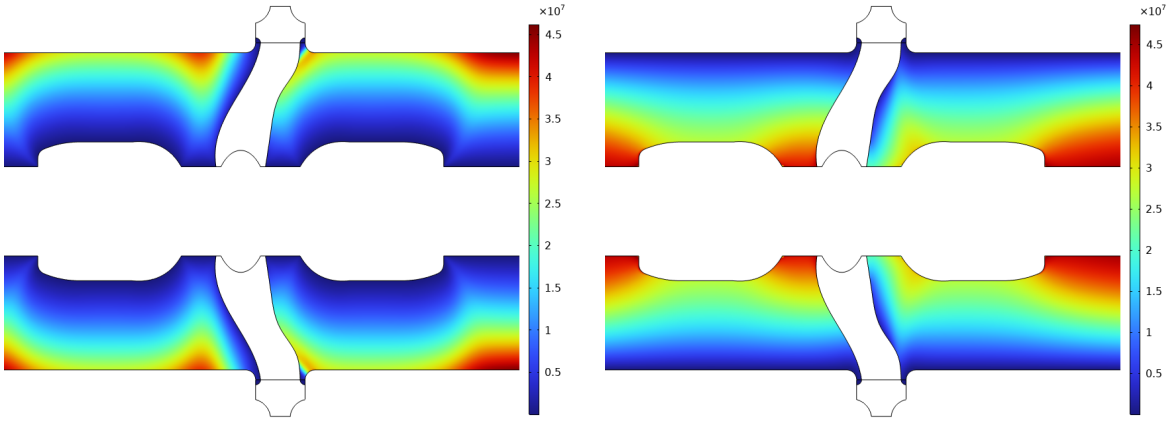


(a) Upper concave surface **(b)** Ldower convex surface

Figure C.27: Model GIS surface field components during steady state for applied voltage of +200 kV

C.6.2. Charge Simulations

The charge simulation of the DC GIS model was performed with SF6 at 5 bars, with mobility, recombination rate, and generation scaled accordingly: $\mu_p = \mu_n = 0.07cm^2/(V \cdot s)$, recombination rate $R_{rec} = 1.3 \times 10^{-13}$, and ion generation rate of 29 IP/m^3 [100]. Ion drift is again the only primary condition considered, as in Appendix C. Figure C.28 shows the steady-state ion distribution for an applied +200 kV.

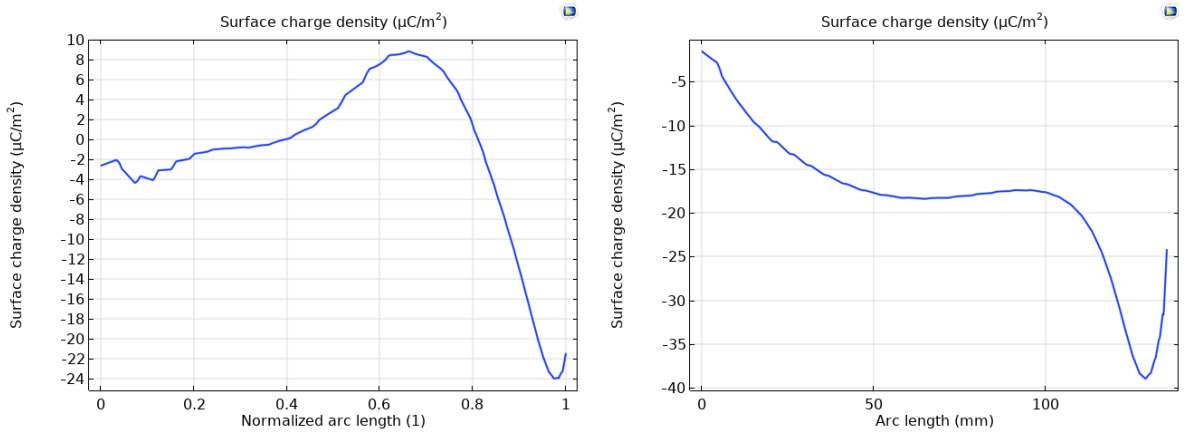


(a) Positive ion concentration

(b) Negative ion concentration

Figure C.28: Model DC GIS steady state ion concentrations for +200kV

The ion concentrations follow the field, with the highest concentration of positive ions away from the HV electrode and vice versa for negative ions; positive and negative ions accordingly accumulate more on the convex and concave surfaces, respectively. Gas conductivity remains a few orders of magnitude smaller than the epoxy spacer, so bulk current can be considered dominant across the operational voltage range. Figure C.29 shows the steady state charge density across both sides of the profile.



(a) Upper surface

(b) Lower surface

Figure C.29: Model GIS steady state charge accumulation across spacer for applied +200kV

The charge polarity and location occur near the HV shieldings or divots, where the field component is highest.

C.7. Enclosure: Metal Cell

The simulation of the metal cell consists of determining an available AC 126 kV spacer geometry and simulating the fields and charges experienced during use. The model for an equivalent 126 kV spacer, similar to the one in the HV lab of TU Delft, is given in a study from Wang et al.[117]. Figure C.30 shows the modeled 126 kV spacer in COMSOL.

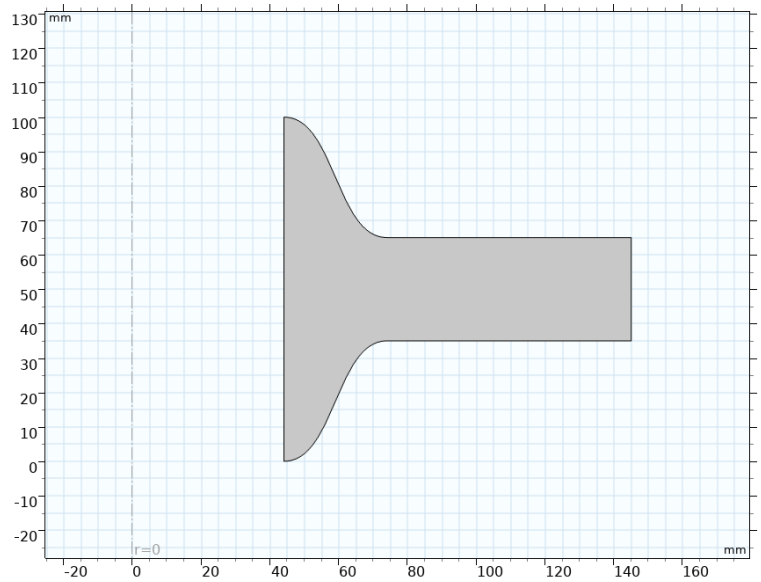


Figure C.30: Metal cell 126 kV Disc spacer model used from a paper by Wang et al.[117]

The spacer dimensions are not very large given the relatively low operational voltage expected in filled SF6 compartments. A key problem was that the conductor passage required a radius of 42mm, much bigger than the electrode test geometry in the cell; a block of nylon was therefore used to allow a more reasonable conductor size. Figure C.31 shows the total metal cell geometry considered.

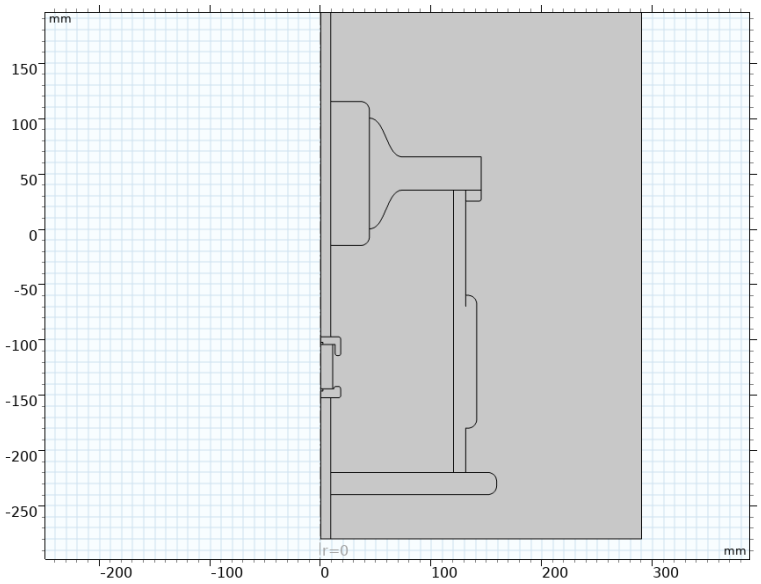
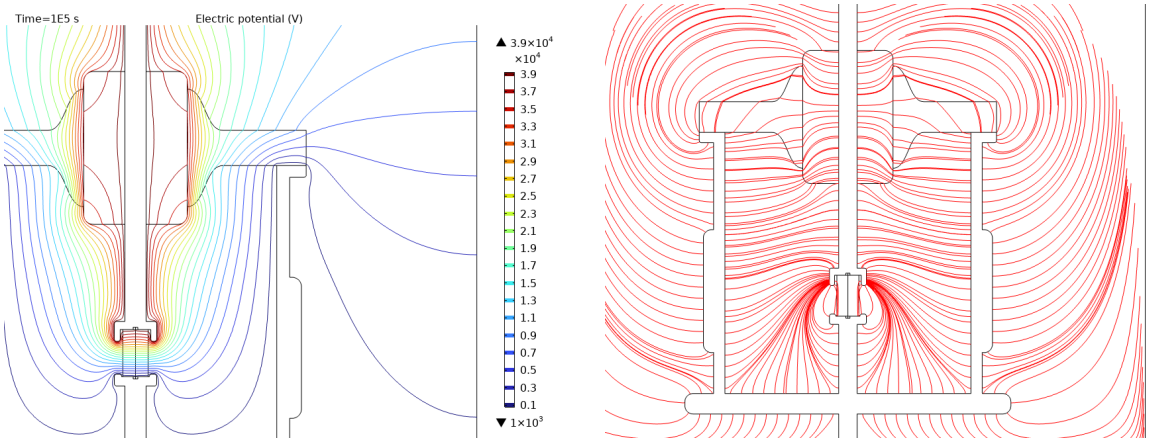


Figure C.31: 2D axisymetric metal cell setup simulated in COMSOL

The cell has a rough internal volume of 120mm x 220mm with all sides constructed out of metal, with a small circular viewing chamber in the side walls for viewing one side of the test spacer. The cell's field problems, limited viewing, and greater difficulty of mechanical realization led to it ultimately not being chosen.

C.7.1. Field Simulations

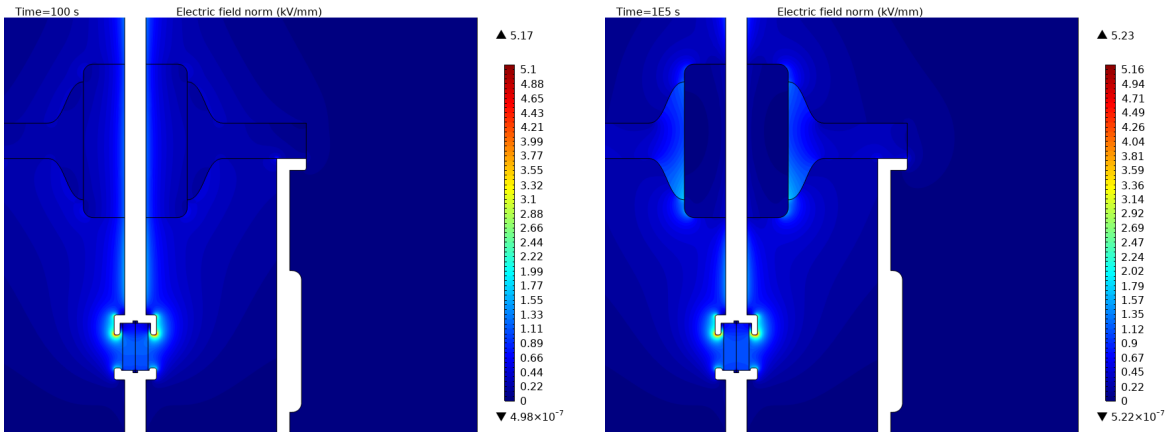
The field simulations for the cell assumed +30 kV DC and -150kV LI, as determined in section 4.3 to be the worst case operational range of the cell at 2 bar. Figure C.32 shows the DC steady state voltage contour and field streamlines.



(a) Voltage Contour **(b)** DC Streamline

Figure C.32: COMSOL simulation of potential contour and electric field streamlines for the metal spacer topped cell

The potential lines are mostly concentrated in the nylon insulation between the disc spacer and the conductor, with field streamlines spanning the whole enclosure. Figure C.33 shows the transition from a capacitive to a resistive field distribution.



(a) AC field distribution **(b)** DC field distribution

Figure C.33: FEM results of simplified metal cell comparison with applied +30 kV DC: AC (left) and DC (right)

The field transitions from being spread in the gas to becoming more concentrated at the intersection of the disc spacer and nylon insulation, due to charges accumulating on the surfaces. Figure C.34 shows the field components across the disc spacer under DC application only.

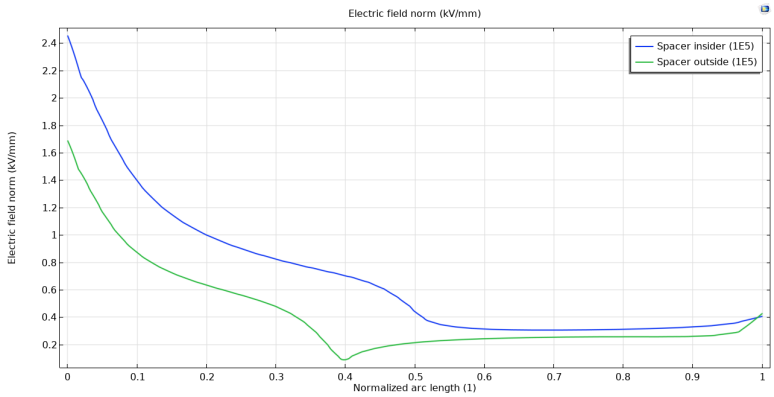


Figure C.34: DC Flange HV

The peak field on the inside of the spacer at DC steady state is 2.43 kV/mm, and 1.67 kV/mm on the outside, remaining within the expected flashover bounds outside. Figure C.35 shows the fields under superimposed DC/-LI voltages.

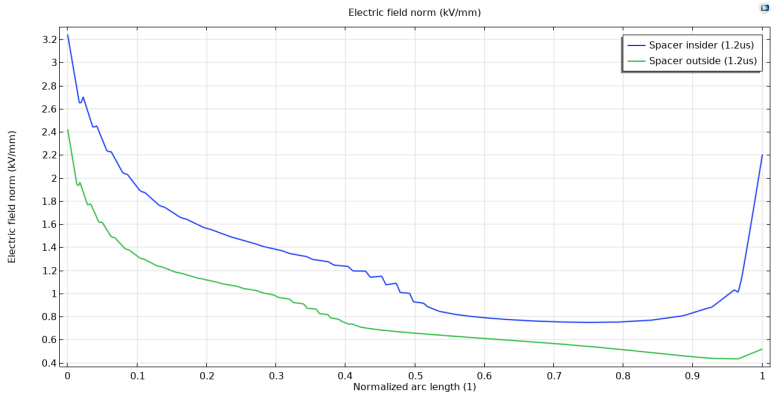
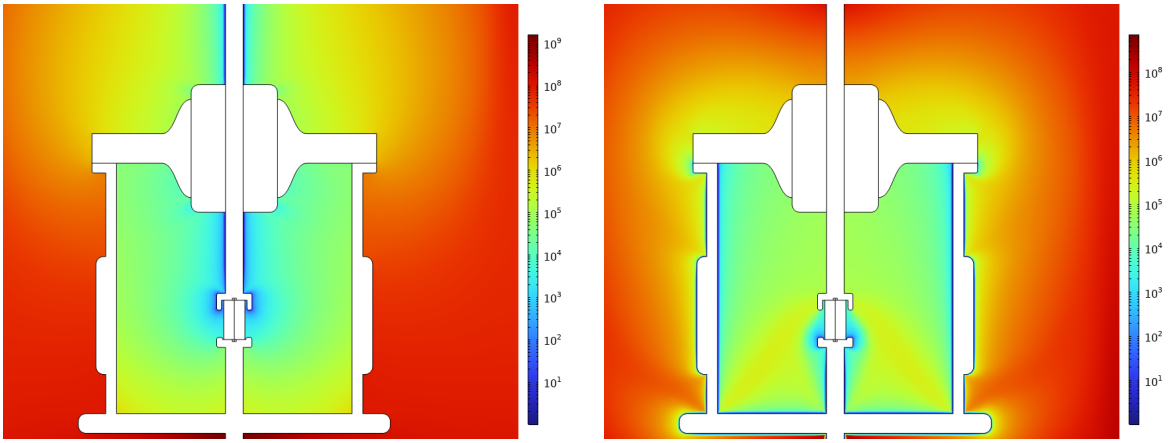


Figure C.35: OP DC/LI Flange HV

The fields across the outside approach 2.4 kV/mm, with internal fields approaching 3.2 kV/mm — the highest of any considered enclosure model, and not easily adjustable given the fixed 126 kV disc spacer length.

C.7.2. Charge Simulations

While the metal side wall does not accumulate charges, the disc spacer and nylon insulating block still do. The charge simulation is solved by treating the gas and solid side accumulations separately and coupling them, using the same assumed gas values under 2 bar from section C.1. Figure C.36 shows the ion densities at steady state DC.



(a) positive ion distribution **(b)** negative ion distribution

Figure C.36: ion densities

The charge accumulation across the lower and upper surfaces of the disc spacer is given in Figure C.37.

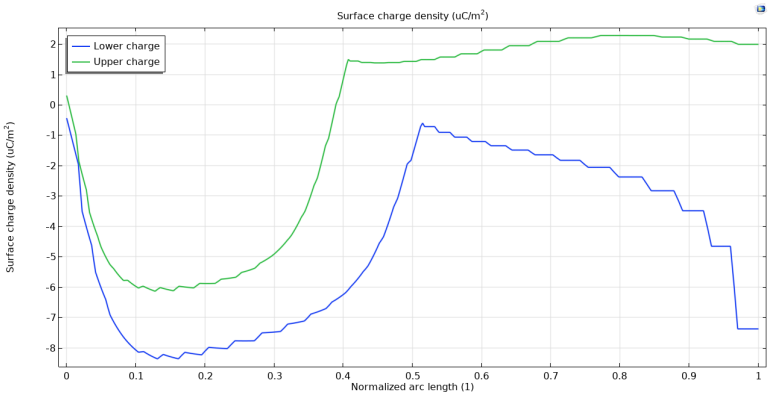


Figure C.37: Charge Flange HV

There is significant charge accumulation on the surfaces, with a peak of -8.3 $\mu C/m^2$ on the lower surface. The required clearance of 270 mm was also bigger than the distance between the exposed HV conductor and the grounded wall. The metal cell was ultimately not chosen, presenting both realization difficulties and the least margin for error of the considered superimposed voltages.

C.8. Enclosure: HV Flange

The HV flange cell uses 2 metal flanges kept at potential and ground, with the external separating insulation being plexiglass walls. Previous AC GIS studies at TU Delft used a smaller electrode setup where charge accumulation and impulse clearance were not a concern. Since the existing test cell was too small to fit the new electrode, a cell following the same principles was dimensioned, keeping the plexiglass height the same as the floating and metal cells for comparison. Figure C.38 shows the 2D axisymmetric COMSOL model of the HV flange setup used.

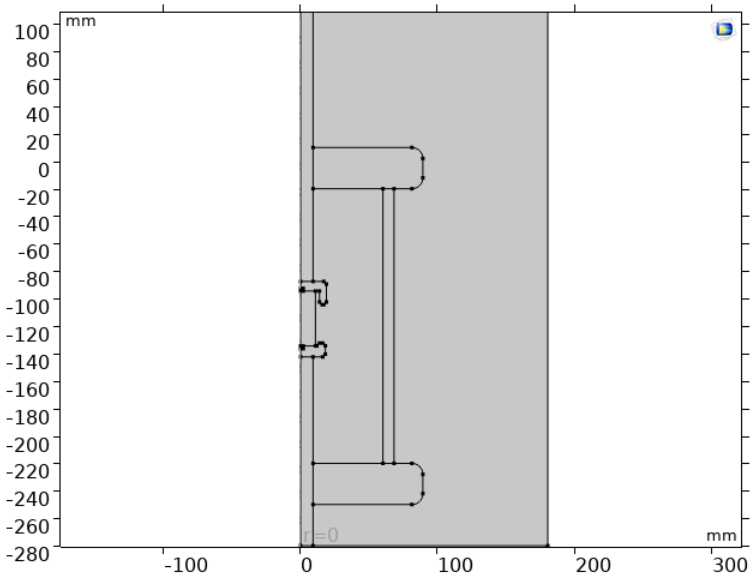
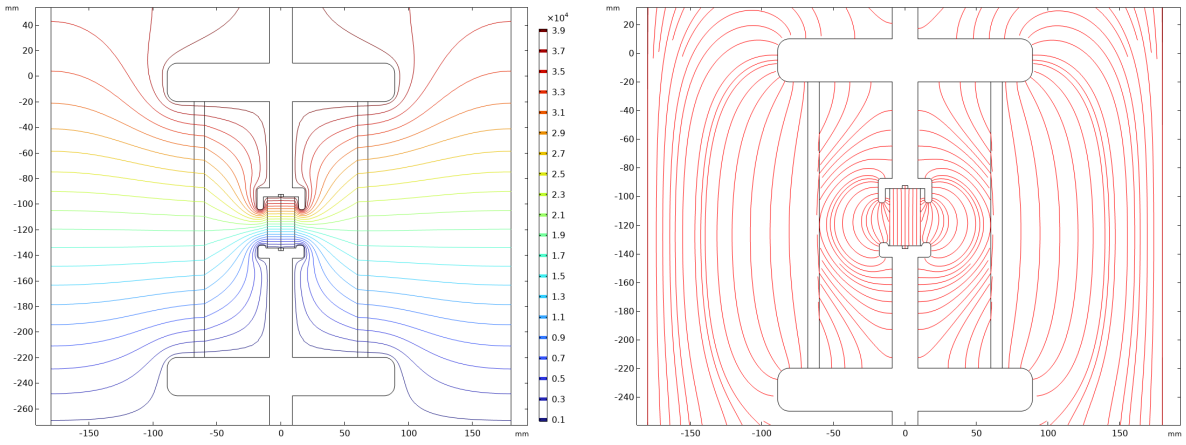


Figure C.38: Scale accurate COMSOL setup of the simplified floating enclosure filled with technical air

The metal flange size is kept smaller, ignoring the support structure to keep cost and weight lower. The flanges use the same aluminium as the electrodes, and the plexiglass conductivity is assumed at 1e-15 S/m.

C.8.1. Field Simulations

The field simulations for the cell also assumed +30kV DC and 150kV LI, as determined in section 4.3. Figure C.39 shows the DC steady state voltage contour and field streamlines.

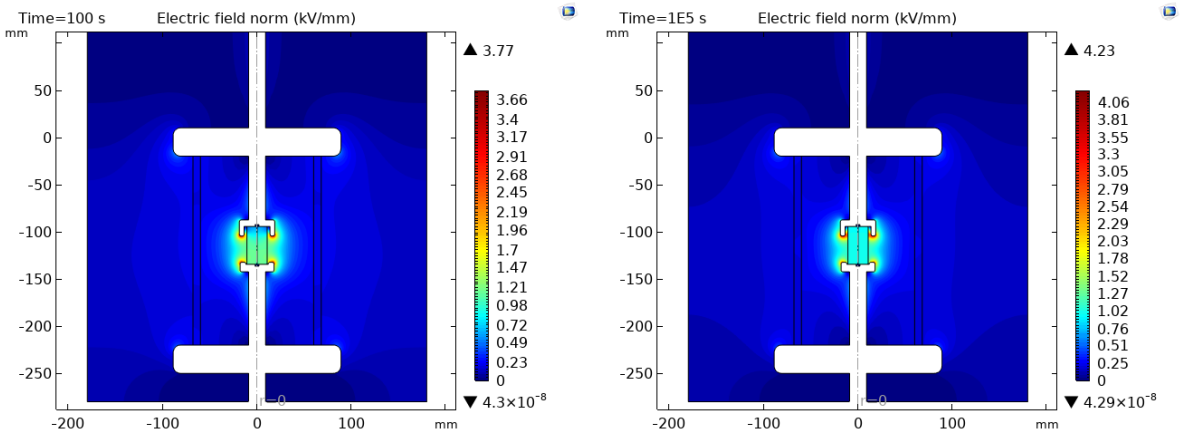


(a) Voltage Contour

(b) DC Streamline

Figure C.39

The voltage contour spreads evenly across the surface, with bending observed at the bowl plate. The field streamlines on the outer flange approximate a parallel plate setup with fringe curve effects at the corners, and the outer field component is mostly tangential. Figure C.40 shows the transition from a capacitive to resistive field distribution.



(a) AC field distribution

(b) DC field distribution

Figure C.40: FEM results of simplified HV flange cell comparison with applied +30 kV DC: AC (left) and DC (right)

Very little field is observed at the plexiglass, and its charge accumulation does not significantly affect the fields at steady state for an applied +30 kV DC. Figure C.41 shows the field components across the inside and outside of the plexiglass at DC steady state.

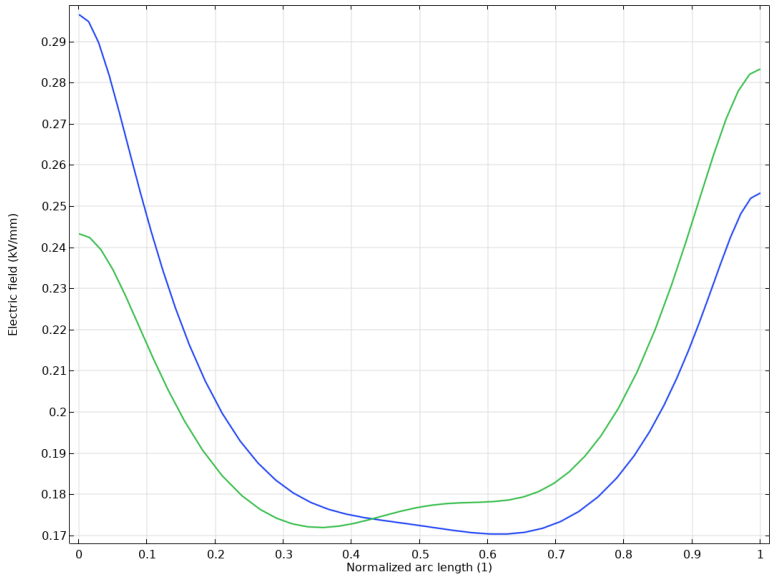


Figure C.41: DC Flange HV

The observed field magnitude remains under 0.297 kV/mm on the outside of the plexiglass, with 0.282 kV/mm on the inside and virtually no field across the outside, meaning the HV cell can be considered not to flashover. Figure C.42 shows the tangential field components across the inside and outside of the plexiglass for a superimposed DC/-LI voltage.

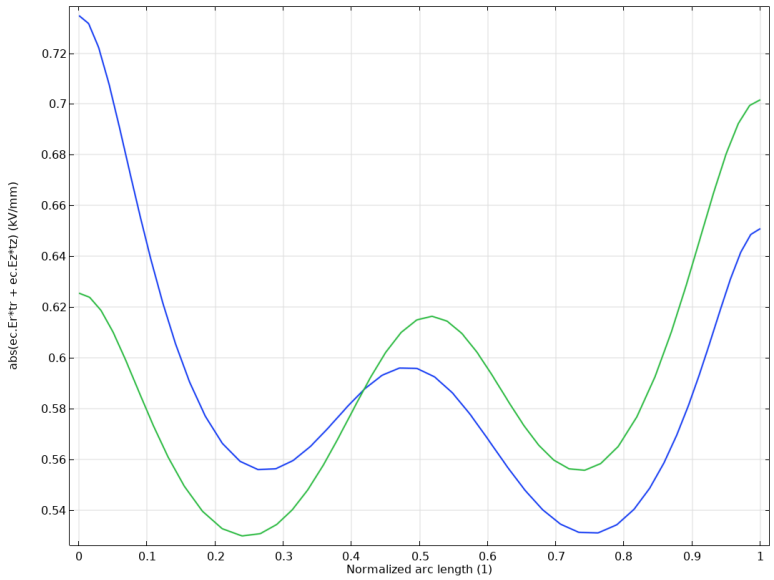
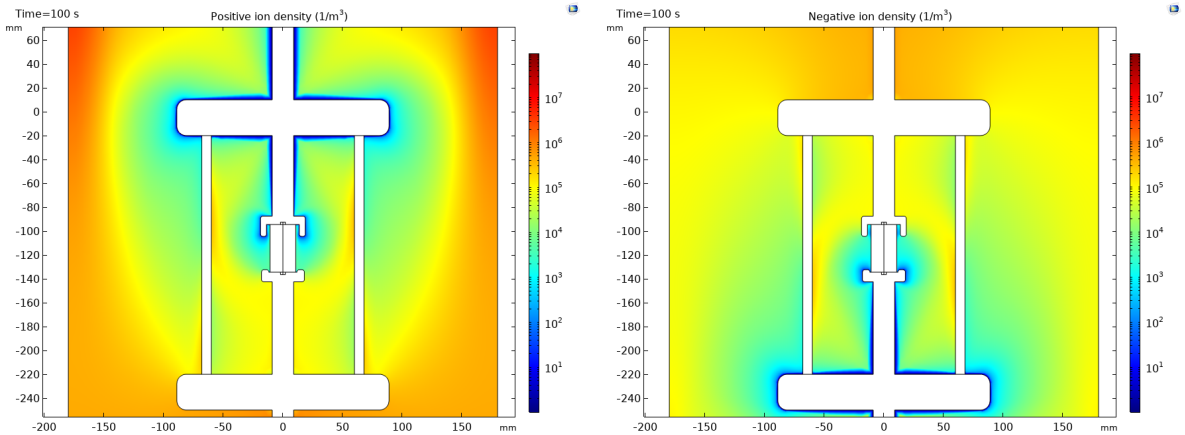


Figure C.42: OP DC/LI Flange HV

The fields on the outside remain at 0.728 kV/mm, well under the surface flashover voltage of PMMA as per Pillai [76]. Internal voltages remain at 0.7 kV/mm, also not causing breakdown across the internal plexiglass surface. It can be concluded that the HV flange setup resists external breakdown for the chosen operational voltages.

C.8.2. Charge Simulations

In this enclosure, charge accumulation only occurs on the plexiglass, simulated as in prior sections with the gas and solid solved in separate interfaces and coupled. Figure C.43 shows the ion densities at steady-state DC.



(a) positive ion distribution

(b) negative ion distribution

Figure C.43: ion densities

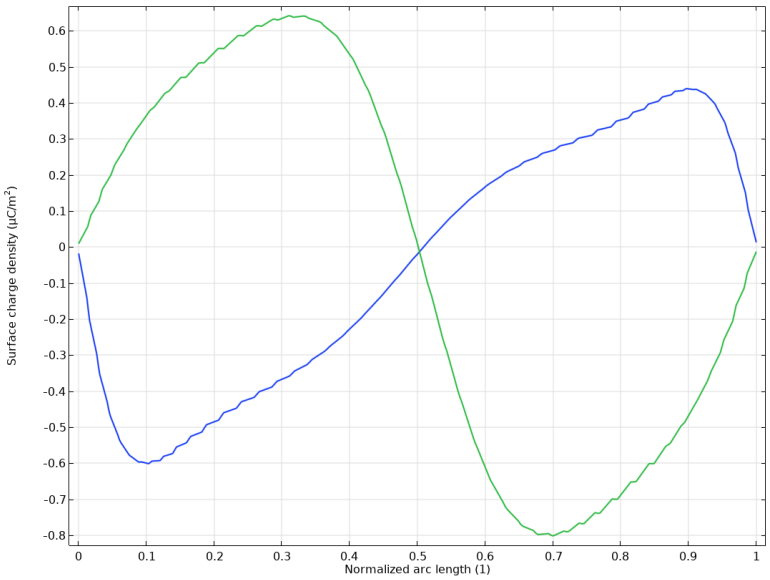


Figure C.44: Charge Flange HV

The charge magnitude of the plexiglass is very small, with a maximum of -0.8 $\mu C/m^2$, due to the low normal component, and therefore charge accumulation is not a major concern for external breakdown. While this cell had lower fields than the spacer-topped cell, it was not chosen, as it presented higher fields than the floating cell and performed worse on the creepage design requirement across the outer surface. The required clearance distance of 432 mm could also be achieved by making the plexiglass taller, which would be difficult to implement. Overall, the complexity and poorer performance of this enclosure compared to the floating cell led to its not being chosen for implementation.

D

LTSPICE simulation Netlist

The simulated composite voltage circuit for the spark gap and coupling capacitor is presented below. A relevant note is that every time the voltage of the impulse generator is changed, the relevant breakdown statements and if conditions on the D flip-flop must be adjusted. The values for all other components should be adjusted to model the relevant HV components available in one's setup.

```
V_IMPULSE N014 0 -20.8k
CS N009 0 1u
Rt N015 0 68
Rf N016 N015 12
Cdiv N011 0 500p
S1 0 0 N022 0 SW
V1 N022 0 PULSE(0 1 100 1us 1ns 1 10 102)
R2 N009 N014 1Meg
Lwire N011 N017 70n
Rwire N017 N016 300
Cstray N011 0 0.225n
Cb 0 0 10n
Cdut N018 0 {X}
S2 0 0 N021 N013 SW
V2 N021 N013 PULSE(0 1 100 1us 1ns 200us 10 102)
RDUT N018 0 1G
VDC N020 0 SINE(0 5k 50)
Rb N019 N018 100k
CDC N019 0 25n
D1 N020 N019 D
S3 N010 N009 Control 0 Sgap
V3 N010 N015 0
C1 0 Control 10pf
R1 N007 Control 0.01
A1 N003 0 N001 0 N005 0 N007 0 DFLOP
Bdischarge N005 0 V=if(((ddt(I(V3))>0)&(I(V3)>-Icutoff)),1,0)
V4 N003 0 1
```

```
Bcharge N001 0 V=if(V(N009)<=Vbreakdown,1,0)
S4 N012 N011 Control1 0 Sgap1
V5 N012 N018 0
C2 0 Control1 10pf
R3 N008 Control1 0.01
A2 N004 0 N002 0 N006 0 N008 0 DFLOP
Bdischarge1 N006 0 V=if(((ddt(I(V5))>0)&(I(V5)<Icutoff1)
              &(V(N011)>0.0000001*Vbreakdown)),1,0)
V6 N004 0 1
Bcharge1 N002 0 V=if((V(N011)<=0.55*Vbreakdown)
              &(ddt(V(N011))<0),1,0)
R4 N018 0 1600Meg
C3 N018 0 25p
.tran 0 0.6m 0 1n
.model SW VSWITCH(Ron=10 Roff=0.1G Vt=0.5 Vh=-0.1)
.ic V(Control)=0
.param Vbreakdown=-20000 Icutoff=0.1 Icutoff1=-0.0001
.model Sgap SW(Ron=10 Roff=100Meg Vt=0.5 Vh=0)
.model Sgap1 SW(Ron=100 Roff=100G Vt=0.5 Vh=0)
.ic V(N009)=-19999.85
.ic V(N021)=4998.183
* .step param X list 0.6p 600p 2n
.param X 0.6p
* Spark gap simple model (timer based switch)
.ic V(Control1)=0
* blocking capacitor
* INITIIALIZATIONS
.backanno
.end
```

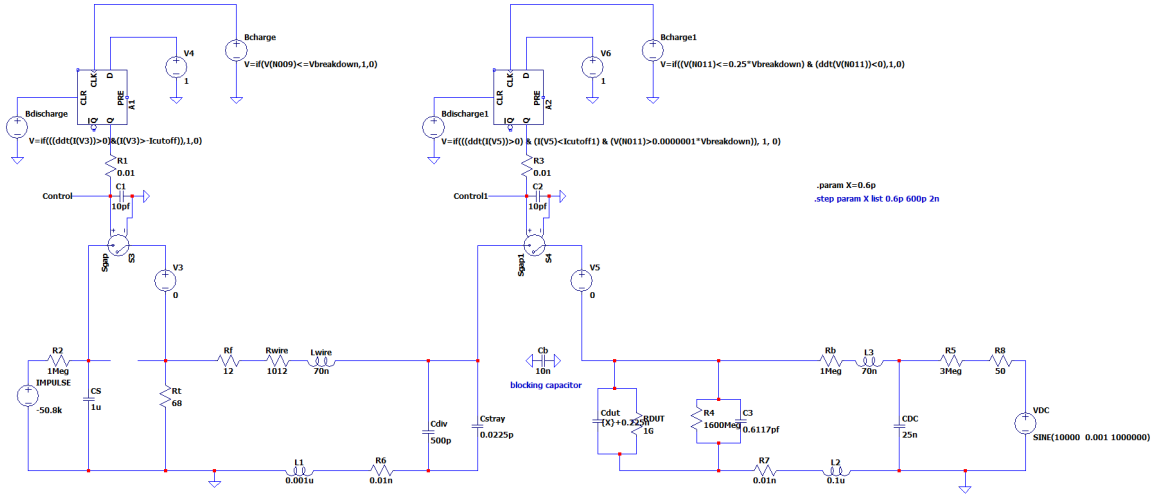


Figure D.1: LTSPICE TEST CIRCUIT

E

Statistical Analysis

Electric breakdown across an insulating medium is an inherently stochastic process in which an applied voltage has a chance of causing it. The initiation of the discharge depends on the electrons avalanching, which becomes more likely at increasing voltage levels. Different testing methods present flashovers and withstands which give an idea of the U_{50}, but this is not the true nature of the breakdown. Correction and statistical analysis are therefore needed to account for this.

E.1. Atmospheric Correction (IEC 60060-1)

The breakdown voltage of an external air insulation depends on the ambient air density and humidity. To make results comparable, IEC 60060-1 [81] refers all values to a standard reference atmosphere defined by a temperature $t_0 = 20\,^{\circ}\mathrm{C}$, an absolute pressure $p_0 = 1013\,\mathrm{hPa}$ and an absolute humidity $h_0 = 11\,\mathrm{g/m^3}$. A breakdown voltage U measured at the actual conditions is referred to as the standard reference atmosphere by

$$U_{corrected} = \frac{U}{k_1 k_2}, \tag{E.1}$$

where k_1 is the air density factor and k_2 is the humidity factor. The factors can be further defined as follows:

$$k_1 = \delta^{\,m}. \tag{E.2}$$

$$k_2 = k^{\,w}, \tag{E.3}$$

The definitions of δ and k are given in the formulas below

$$\delta = \frac{p}{p_0} \cdot \frac{273 + t_0}{273 + t}, \tag{E.4}$$

$$\text{DC:} \quad k = 1 + 0.014\,(h/\delta - 11) - 0.00022\,(h/\delta - 11)^2, \qquad 1 < h/\delta < 15\,\mathrm{g/m^3}, \tag{E.5}$$

$$\text{LI} \quad k = 1 + 0.010\,(h/\delta - 11), \qquad 1 < h/\delta < 20\,\mathrm{g/m^3}. \tag{E.6}$$

The correction exponents m and w are also obtained as per the equation below

$$g = \frac{U_{50}}{500\,L\,\delta\,k}, \tag{E.7}$$

in which U_{50} is the measured or estimated $50\,\%$ breakdown voltage at the actual atmospheric conditions and L is the smallest discharge distance. For withstand tests, it may be assumed $U_{50} \approx 1.1\,U_t$, with U_t being the test voltage. The exponents then follow from g according to Table E.1 from [81] given below.

Table E.1: Air-density and humidity correction exponents m and w as functions of the parameter g, per IEC 60060-1 [81].

g	m	w
< 0.2	0	0
0.2–1.0	$g(g-0.2)/0.8$	$g(g-0.2)/0.8$
1.0–1.2	1.0	1.0
1.2–2.0	1.0	$(2.2-g)(2.0-g)/0.8$
> 2.0	1.0	0

For the work in this paper, a few points must be clarified: the use of atmospheric correction pertains to the choice of spark-gap trigger and to correcting for the LI breakdown tests conducted in the lab. It is recommended per IEC for composite tests that the correction factors for both DC and LI are calculated and the worst case is applied.

E.2. Statistical Analysis Up and Down Tests

The up-and-down tests used in this section are class 2 tests as prescribed in IEC 60060-1 [81], which rely on the primary assumption of independence between successive tests. Provided independence holds, the U_{50} and σ of the given up-and-down tests are determined using the maximum likelihood estimate (MLE), described below.

E.2.1. Maximum Likelihood estimate

Since a flashover is a binary outcome at each applied voltage level, the number of flashovers x_i observed in n_i impulses at voltage level V_i follows a binomial distribution

$$f(x_i) = \binom{n_i}{x_i} p_i^{x_i} (1 - p_i)^{n_i - x_i}, \tag{E.8}$$

where p_i is the true flashover probability at V_i, expressed as a function of the population mean U_{50} and standard deviation σ via the normal cumulative distribution function

$$p_i = \Phi\left(\frac{V_i - U_{50}}{\sigma}\right). \tag{E.9}$$

As flashover trials are independent events, the likelihood of observing the complete test sequence over N voltage levels is the product

$$L = \prod_{i=1}^{N} f(x_i). \tag{E.10}$$

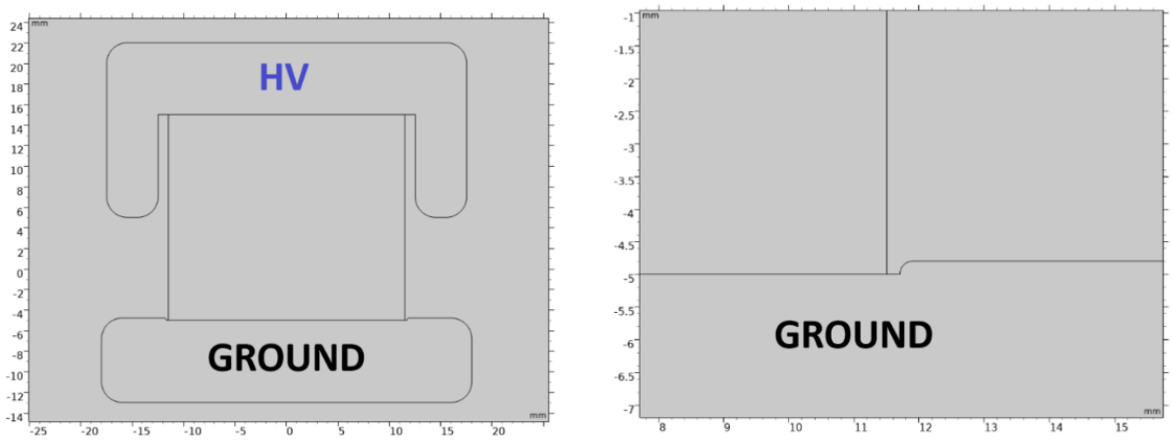
The maximum likelihood estimates of U_{50} and σ are obtained by setting the partial derivatives of the log-likelihood to zero,

$$\frac{\partial \ln L}{\partial U_{50}} = \frac{\partial \ln L}{\partial \sigma} = 0, \tag{E.11}$$

which is solved numerically rather than in closed form. The resulting U_{50} and σ describe the population from which the tested samples were drawn as per IEC 60060-1 and Hauschild et al[88]. MATLAB was used to solve (E.11) numerically.

F

Additional Information



(a) Initial BP design

(b) Initial BP closeup

Figure F.1: Initial design of BP electrodes prior to optimization

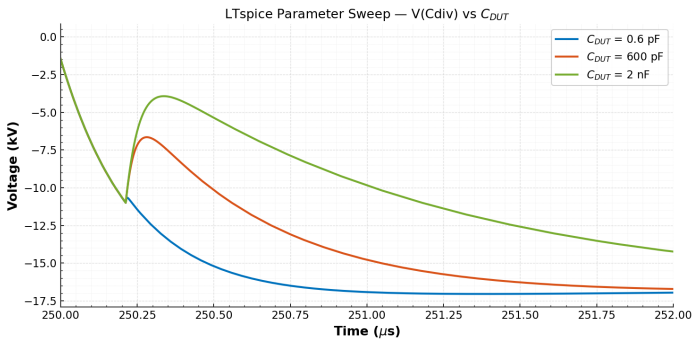


Figure F.2: Effect of load capacitance on the chopping dip relative to the impulse circuit C_{load}. Blue (0.6pF) is significantly smaller, orange (600pF) approximately equivalent, and green (2 nF) much larger than the impulse circuit capacitance

Table F.1: Graphical Independence tests for Initial Nylon samples based on method from Hauschild et al. [88](withstand: $-$; breakdown: x), $n = 10$ per row

Sequence	Probability of flashover $n = 10$	Probability of flashover all
x--xxxx-xx	0.700	0.5238
-xxxxx----	0.500	
x---x-x---	0.300	
x-xx-xxx--	0.600	
---------x	0.100	
-xxxxxxx-x	0.800	

F.1. Electrostatic Voltmeter Recordings

The section below presents the charge measurements from section 7.2, with four tests performed on each of the four sides. Surface potentials were recorded with a Trek electrostatic voltmeter, with the measurement probe placed 2 mm from the surface, set and verified using calipers. Several sources of uncertainty must be accounted for. All voltages are rounded to the nearest 10 V, since the surface potential fluctuated continuously even with a steady hand, and the probe standoff of 2 mm carries an estimated uncertainty of ± 0.05 mm from the caliper measurement and mounting.

Table F.2: Charge measurements, Set 1 (T = 19.52 °C, p = 1030 hPa, AH = 6.31 $\mathrm{g/m^3}$)

Measured Point	Voltage Side 1 [V]	Voltage Side 2 [V]	Voltage Side 3 [V]	Voltage Side 4 [V]
0.425	660	490	670	620
0.5625	420	340	270	360
0.7	560	350	230	280

Table F.3: Charge measurements, Set 2 (T = 21.23 °C, p = 1013 hPa, AH = 7.43 $\mathrm{g/m^3}$)

Measured Point	Voltage Side 1 [V]	Voltage Side 2 [V]	Voltage Side 3 [V]	Voltage Side 4 [V]
0.425	880	1020	360	540
0.5625	290	100	280	190
0.7	130	240	-70	10

Table F.4: Charge measurements, Set 3 (T = 18.92 °C, p = 1015 hPa, AH = 5.89 $\mathrm{g/m^3}$)

Measured Point	Voltage Side 1 [V]	Voltage Side 2 [V]	Voltage Side 3 [V]	Voltage Side 4 [V]
0.425	210	310	420	-320
0.5625	40	160	120	180
0.7	-240	30	-50	140

Table F.5: Charge measurements, Set 4 (T = 20.10 °C, p = 1017 hPa, AH = 6.10 $\mathrm{g/m^3}$)

Measured Point	Voltage Side 1 [V]	Voltage Side 2 [V]	Voltage Side 3 [V]	Voltage Side 4 [V]
0.425	420	780	520	1030
0.5625	-150	450	-140	230
0.7	320	-250	-390	140