Millimeter-Wave Transceiver Frontends for Broadband, Energy-Efficient, and Linear Phased-Array Systems

Pashaeifar, M.

DOI
10.4233/uuid:03d46004-baa9-47ce-86cf-c46774b19a96

Publication date
2024

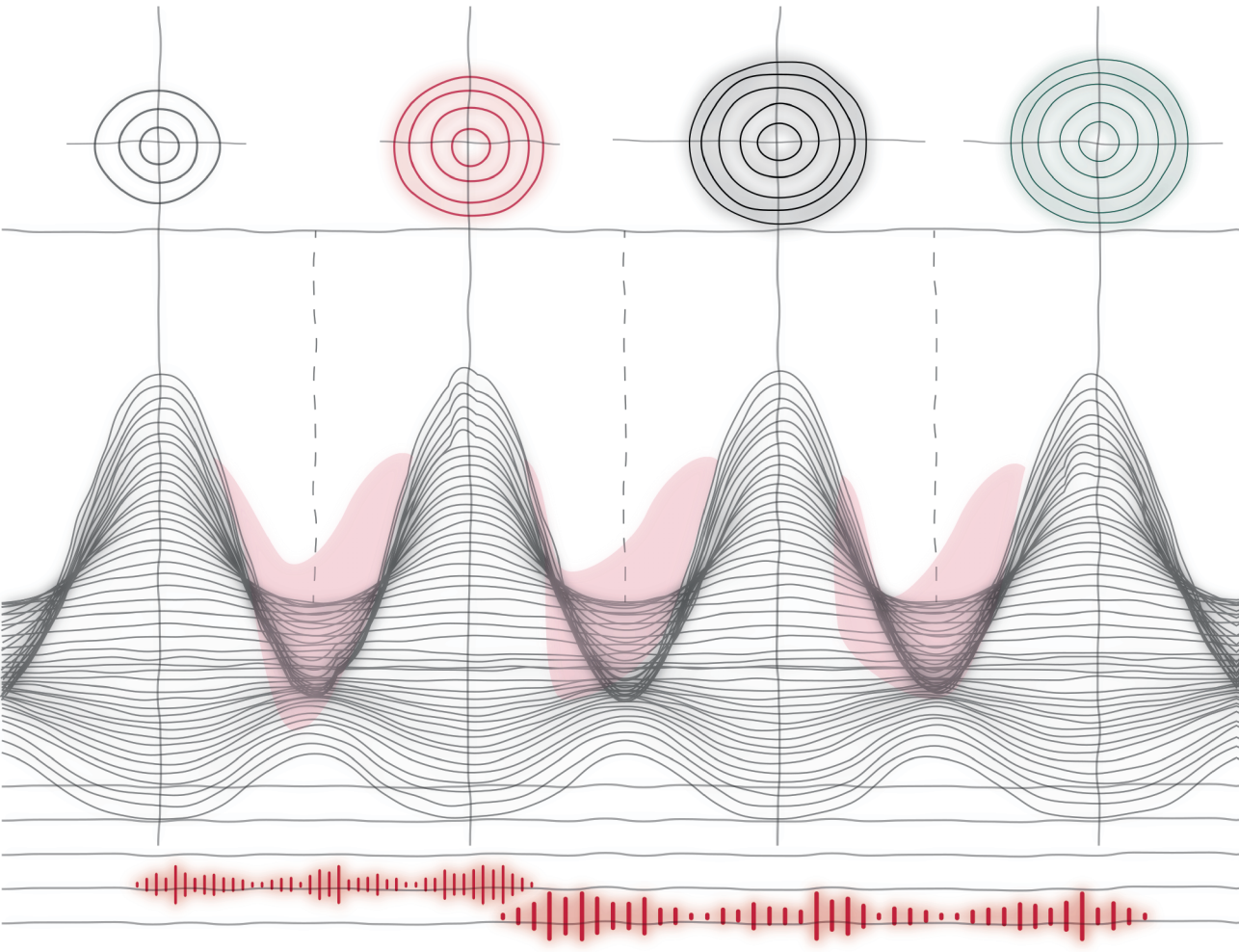
Document Version
Final published version

Citation (APA)
Pashaeifar, M. (2024). *Millimeter-Wave Transceiver Frontends for Broadband, Energy-Efficient, and Linear Phased-Array Systems*. [Dissertation (TU Delft), Delft University of Technology].
https://doi.org/10.4233/uuid:03d46004-baa9-47ce-86cf-c46774b19a96

Important note
To cite this publication, please use the final published version (if applicable).
Please check the document version above.

Millimeter-Wave Transceiver Frontends

for Broadband, Energy-Efficient, and Linear Phased-Array Systems



Masoud Pashaeifar

Millimeter-Wave Transceiver Frontends

for Broadband, Energy-Efficient, and Linear Phased-Array Systems

Millimeter-Wave Transceiver Frontends

for Broadband, Energy-Efficient, and Linear
Phased-Array Systems

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology
by the authority of the Rector Magnificus prof.dr.ir. T.H.J.J. van der Hagen
chair of the Board for Doctorates
to be defended publicly on
Thursday 10 October 2024 at 12:30 o'clock

by

Masoud PASHAEIFAR

Master of Science in Electrical Engineering,
University of Tehran, Tehra, Iran,
born in Tabriz, Iran.

This dissertation has been approved by the promoters.

Composition of the doctoral committee:

Rector Magnificus,	chairman
Prof. dr. ing. L.C.N. de Vreede,	Delft University of Technology, promoter
Dr. M.S. Alavi,	Delft University of Technology, copromoter
Independent members:	
Prof. dr. ir. B. Nauta	University of Twente
Prof. dr. ir. A. B. Smolders	Eindhoven University of Technology
Prof. dr. P. Wambacq	Vrije Universiteit Brussel, Belgium
Prof. dr. H. Wang	Eidgenössische Technische Hochschule (ETH) Zürich, Switzerland
Prof. dr. K. A. A. Makinwa	Delft University of Technology
Prof. dr. ir. W. A. Serdijn	Delft University of Technology, reserve member

The work presented in this thesis has been performed at TU Delft and financed by the Dutch Technology Foundation NWO-TTW (Entergy Efficient Wideband Supply Interpolation (gENESIs), 15593), as part of the TTW-NXP partnership program "Advanced 5G Solutions".

Keywords: 5G, AM-AM, AM-PM, balanced power amplifier, calibration-free, blocker-tolerant receiver, circulator, chain-weaver, direct upconverter, double-quadrature, duplexer, FDD, full-duplex, image-rejection ratio, impedance sensor, isolator, mm-wave, mutual-coupling, quadrature hybrid coupler, N-path filter, power amplifiers, power sensor, root mean square (rms) detector, series-Doherty PA, transmitter, VSWR resilience, wideband.

ISBN 978-94-6384-638-7

Cover designed by Aylin Nourghasemi *(Instagram: aylenina.illustrations)*

Printed in the Netherlands.

To my lovely parents, Maman and Baba!
To my dearest, Mahsa!
and
To my Lenna!

CONTENTS

1

INTRODUCTION

1

1.1. INTRODUCTION AND MOTIVATION

Although we have observed the shutdown of second-generation (2G) mobile networks in recent years, which are expected to be fully retired in 2033, 2G initiated the extreme development of mobile communications. Ever since, through various generations up to the fifth generation (5G) of mobile networks, the data rate and capacity increased by more than 1,000,000x [1]. The ever-increasing demand for higher data rates fuels the mobile communication industry to keep pace or even improve it. As such, the TSMC's estimation shows that by 2030, the mobile industry will share 30% of the total 1 Trillion US$ semiconductor market as illustrated in Fig. 1.1(a) [2]. This imposes an ambitious goal for ongoing 5G development, which is considered not just an upgrade but a paradigm shift driver.

The 5G standard includes all mobile spectrum allocations, such as low-band (below 1GHz) for long-range applications and mid-band (1-6GHz) for high data rate applications. However, to keep up with the "10x data rate increase every five years" trend [1], millimeter wave (mm-wave) frequencies, which refer to the spectrum range of 30GHz to 300GHz, are a key enabler. It offers huge bandwidth (up to 1.4GHz), thus huge data throughput, beam forming, high transmission quality, low latency, and detection capabilities[3–5]. Mm-wave 5G can, as such, satisfy the huge traffic demand of wireless communication and enables the digitalization of societies and industries through video streaming, virtual reality, and internet-of-things (IoT) [6]. On the other hand, unlike the digital front-end and computing processors whose performance and power efficiency significantly improved by technology scaling (see Fig. 1.1(b)), the analog front-end (RF/mm-wave and baseband circuitry) performance improvement mainly relies on circuits and architectural innovations. Therefore, the first step is understanding the challenges and opportunities of mm-wave communication system design.

In spite of its huge potential, mm-wave 5G has several natural disadvantages, as we review here.

- Mm-wave signal's shorter wavelength leads to lower penetrability and higher free-

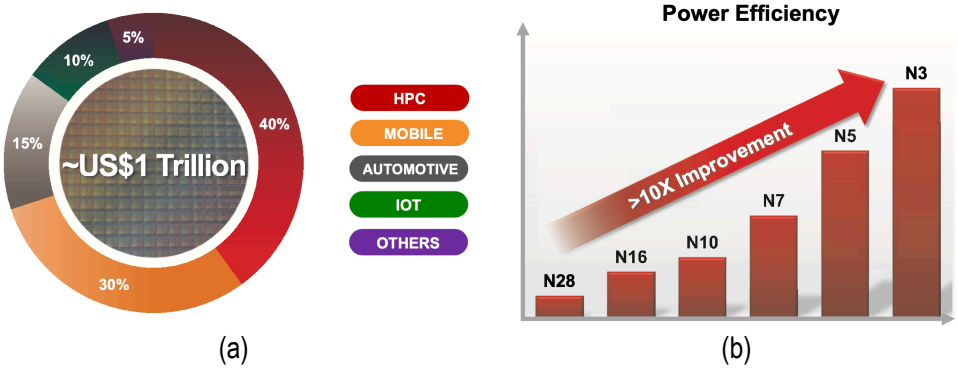


Figure 1.1: (a) TSMC's estimation of the semiconductor market in 2030 [2], and (b) the power efficiency improvement of computing devices by the technology scaling of semiconductors [2].

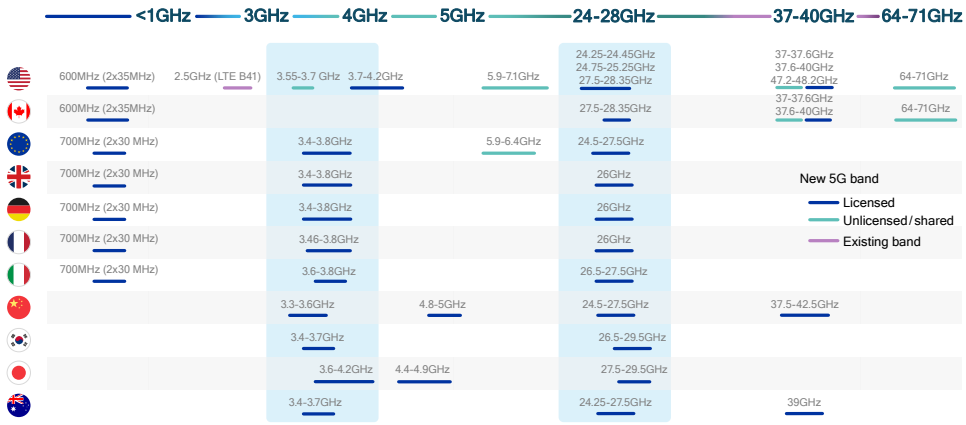


Figure 1.2: Snapshot of the 5G spectrum [10].

space path loss, thus limited coverage[7]. Besides, the absorption of atmospheric gases can attenuate the mm-wave signal.

- 5G communication systems aim to support multi-Gb/s data throughput by allocating wider bandwidth (BW) up to 1.4GHz, which means a higher RX noise floor ($-174dBm + 10\log BW + NF_{dB}$ where NF_{dB} is receiver's (RX's) noise figure). They also employ more complex data modulation schemes, requiring higher signal-to-noise ratio (SNR). As a result, the RX sensitivity ($P_{S-RX} = -174dBm + 10\log BW + NF_{dB} + SNR_{dB}$) increases, thus, the link budget decreases.

- The limited supply voltage and operating frequency of nanoscale CMOS technologies alongside the high peak-to-average power ratio (PAPR) of the complex data modulation schemes restrain designing transmitters (TXs) with high average output power. This limits the maximum equivalent isotropic radiated power (EIRP) for a given array size, thus limiting the link budget.

- The short mm-wave signal wavelength prevents employing isolators in the phased-array TXs. Hence, the power amplifier (PA), as the TX front-end, faces the antenna impedance mismatch. This attribute becomes more complex when considering a time-varying voltage standing wave ratio (VSWR) caused by the beam-angle-dependent element-to-element mutual coupling of the phased-array TX and environmental changes. This time and frequency-dependent VSWR deteriorates PA gain-flatness, output 1dB compression point (oP_{1dB}), AM-AM, AM-PM, and reliability.

- High PAPR (e.g., 10-11dB) data modulation signal enforces the PA to operate at deep power back-off. Since it governs the overall performance of the TX, a low average efficiency directly degrades the system efficiency and, in turn, its thermal handling capability [8, 9].

But as stated earlier, operating at mm-wave frequencies unlocks new opportunities to address the above-mentioned challenges and innovate beyond initial expectations. Below, we mention a few advantages of designing transceivers at mm-wave frequencies.

- Beamforming architectures can provide the required link budget while reducing interference and increasing link security [11].
- Mm-wave phased-array systems are scalable in both bandwidth and array size to further improve their data rate and link budget.
- Mm-wave enables new architectures and circuits for integrated transceivers, which are inconvenient to use at the lower frequencies due to related area occupation and low-quality factors. Besides, higher integration is mandatory and possible at these frequencies, where even the antenna can be accommodated on the chip [12]. Therefore, the innovation in passive circuit design is one of the driving forces in developing mm-wave 5G systems.
- Fully integrated advanced PA architectures such as Doherty PA and balanced amplifier can be implemented in a compact area to improve the power back-off efficiency of the TX and VSWR resilience.
- Novel phased-array transceiver architectures can be introduced to improve the performances, such as security [13], SNR, and I/Q mismatch by over-the-air combining the signals.

1.2. THESIS OBJECTIVES

This dissertation aims to introduce novel TX/PA architectures to address the key performance indicators (KPIs) of the mm-wave phased-array transceivers, considering their practical challenges. The intention is to exploit the mm-wave opportunities while minimizing the tuning and calibration of the phased-array TXs.

As discussed in Section 1.1, the PBO efficiency of the PA is one of the most crucial KPI of the mm-wave 5G TX. Therefore, the first objective is to introduce a wideband Doherty PA that can offer close to ideal (2x in a Doherty PA compared to a class-B PA) 6dB PBO efficiency enhancement. Reusing the same passive structure, we extend the load modulation concept of Doherty PA to improve linearity instead of efficiency enhancement. Hence, we introduce the load-modulation-based third-order inter-modulation distortion (IMD3) cancellation PA architecture to address the high linearity demand of the 5G system.

The main challenge of designing phased-array PA is the time-varying VSWR due to mutual coupling between the antenna elements. Therefore, the second objective is to extend PA's KPIs, such as PBO efficiency and output power, while maintaining the performance under VSWR. We introduce a novel N-way balanced power combiner to achieve high output power and extend the VSWR resilience of a balanced amplifier. Additionally, we utilized a balanced amplifier structure to maintain the proposed Doherty PA performance under load mismatch. Additionally, we utilized the quadrature hybrid coupler—a passive device that combines two signals with a 90° phase difference—along

with its associated mathematical operation known as the Hilbert transform within the TX path.This way, we implement a second image-rejection stage in a direct upconversion TX architecture to maximize its image-rejection ratio and avoid I/Q mismatch calibration.

In traditional communication systems, duplexing allows for simultaneous transmission and reception of signals, typically using either Frequency Division Duplexing (FDD) or Time Division Duplexing (TDD). Similarly, the low- and mid-band 5G standard employ both TDD and FDD, while only TDD has been considered for high-band systems. This thesis explore alternative duplexing methods, including FDD, which separates transmission and reception into different frequency bands, and Single-Frequency Full-Duplex (SF-FD), which allows both operations on the same frequency. To serve these alternatives, a fully integrated mm-wave FDD transceiver frontend is introduced by using a CMOS circulator structure. We introduce an mm-wave N-path filter to enable the implementation of such a compact CMOS circulator.

1.3. ORGANIZATION OF THESIS

This dissertation is organized as follows:

- In Chapter 2, the architectures and system specifications of phased-array TX are analyzed, and circuit-level design challenges and potential solutions are discussed.

- Chapter 3 presents a wideband series-Doherty PA for mm-wave 5G applications. It features a compact two-step impedance inverting-based series-Doherty power combiner that provides broadband PBO efficiency enhancement. The AM-AM/AM-PM performance of the load-modulated Doherty PA for broadband operation is analyzed. We also devise a post-silicon inter-stage passive validation approach to evaluate the mm-wave chip prototype utilizing embedded voltage root mean square detectors.

- Chapter 4 presents a wideband mm-wave energy-efficient TX for phased-array systems. It features an advanced double-quadrature direct-upconverter to improve its in-band linearity and spectral purity. The proposed TX architecture incorporates an efficiency-enhanced balanced PA that mitigates VSWR fluctuations in phased-array systems while enhancing efficiency at power back-off.

- Chapter 5 introduces a novel load-modulation-based IMD3 cancellation technique for class-B CMOS PAs. In a class-B PA, the IMD3 generated by the third-order transconductance (g_{m3}) and the gain compression have opposite signs. Thus, they can cancel each other at specific bias and loading conditions. The proposed Doherty topology allows for the adjustment of gain compression by modulating the effective loading, facilitating IMD3 cancellation over the entire load modulation region.

- Chapter 6 introduces an N-Way chain-weaver balanced PA for mm-wave phased-array TXs. Taking advantage of the proposed combining network, an embedded

impedance/power sensor is implemented, which can be utilized for output power regulation, built-in self-test, and load-based performance optimization. The proposed PA architecture offers linearity and gain robustness under the antenna's frequency/time-dependent VSWR.

- Chapter 7 presents two distinct functions: 1) a fully integrated FDD transceiver front-end and 2) a PA with an integrated isolator. These concepts are implemented as a configurable chip comprising a PA and an integrated nonreciprocal ultra-compact isolator/circulator/RX.
- In chapter 8, the dissertation is concluded, and suggestions are given for future developments.

2

FUNDAMENTALS AND CHALLENGES OF MM-WAVE PHASED ARRAY TXS

Millimeter wave (mm-wave) fifth-generation (5G) communication systems employ phased arrays to overcome the free-space path loss while providing high data throughput and low-latency line-of-sight links. In this chapter, the architectures and system specifications of phased-array transmitters (TX) are analyzed, and circuit-level design challenges are discussed.

2.1. INTRODUCTION

Beamforming architectures are the key enablers of developing millimeter wave (mm-wave) communication systems to achieve multi-Gb/s data throughput. A traditional phased-array TX architecture providing RF/mm-wave beamforming is shown in Fig 2.1 (a). It is based on analog beamforming, while the direct up-conversion architecture has been chosen as the most simple, thus potentially most energy-efficient TX architecture. It comprises a data stream through a pair of I/Q digital-to-analog converters (DACs), which are converted and split into N_A mm-wave paths. The TX beam is formed by weighting each signal path at mm-wave frequencies using a designated phase-shifter and variable-gain amplifier (VGA). This mm-wave beamforming offers the lowest complexity, thus the most efficient implementation [14–16]. However, it supports only single-beam communication, which is not suitable for multi-user massive multi-input multi-output (m-MIMO) systems. Moreover, scaling the mm-wave beamforming structure is challenging since a 1-to-N_A power splitter is required.

Digital beamforming TX architecture, on the other hand, provides the highest flexibility and capacity, where the TX beam is formed by weighting each path digitally at the baseband (see Fig 2.1 (b)). In this architecture, each antenna element requires a full TX up conversion chain, including I/Q DACs, baseband filters, a quadrature upconverter, and a PA. Even though the LO generation part could be shared, digital beamforming dauntingly increases power consumption. However, the digital approach enables the holy grail of multi-beam/-user m-MIMO systems, and extensive digital pre-distortion (DPD) for each element separately. Nevertheless, the digital signal processing (DSP) resources and baseband high-speed interfaces of the whole beamforming system dramatically increase the cost and the power consumption. For instance, assuming 12-bit I/Q DACs with a 3.2GHz sampling rate are required to support an 800MHz OFDM modulated signal, the data rate of each TX can be calculated as 76.8Gb/s. Thus, phased array TXs with 64 and 256 elements require 4.9152Tb/s and 19.6608Tb/s data rate, respectively, in total if no additional measures are taken to limit the amount of data.

Generally, it is agreed that hybrid beamforming is a suitable architecture for mm-wave 5G systems [17]. As shown in Fig 2.1, hybrid beamforming combines digital and analog beamforming. It comprises N_D data stream up conversion paths, where each output is split in N_A mm-wave beamforming paths. Overall, this architecture supports $N_D \times N_A$ antenna elements, capable of steering all energy at a single user or producing multiple beams for supporting multi-user m-MIMO. In a multiple beam-steering scenario assuming (M_B) as the number of beams, the effective isotropic radiated power (EIRP) of each beam can be calculated as

$$EIRP_{B,dBm} = EIRP_{max,dBm} - 20\log M_B \tag{2.1}$$

were $EIRP_{max,dBm}$ is the maximum EIRP of the TX when transmitting a single beam. It means producing multiple beams reduces the link budget for each beam by $20\log M_B$. Therefore, even in a digital beamforming architecture with the highest flexibility/capacity, the number of beams is limited by the link budget.

In summary, hybrid beamforming establishes a trade between the energy/cost efficiency of analog beamforming and the high flexibility/capacity of digital beamforming.

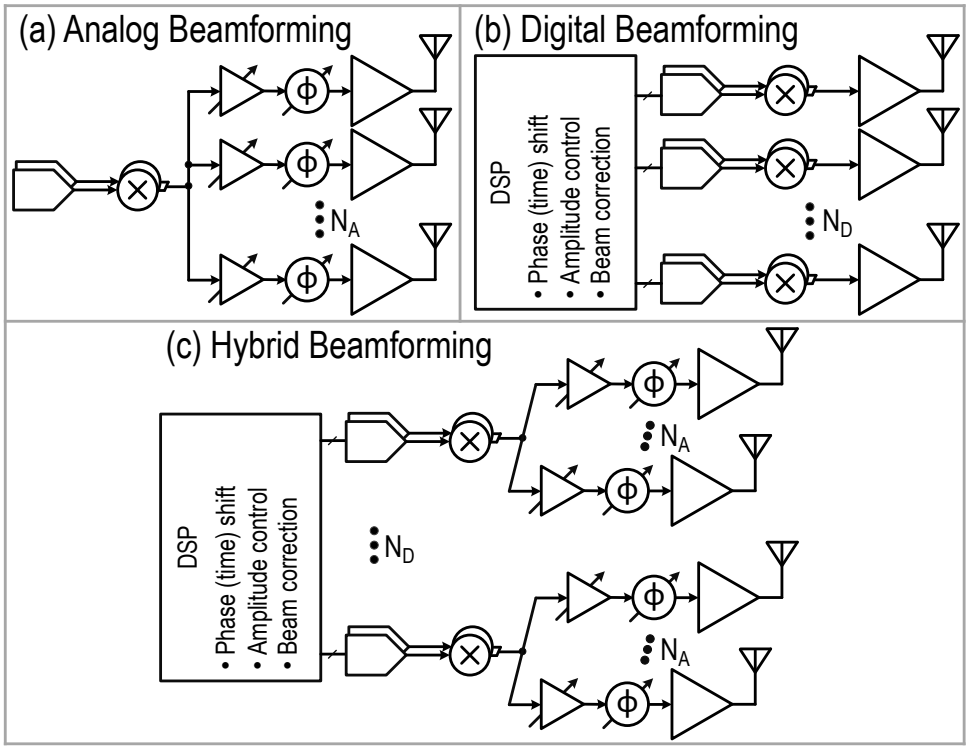


Figure 2.1: Simplified analog, digital, and hybrid beamforming phased array TX architectures.

2.2. LINK BUDGET

In a phased-array TX consists of N_{TX} elements, each TX element radiates the transmit signal by its antenna. Assuming the output power and antenna gain of each element are $P_{TX,dBm}$ and $G_{A-TX,dBi}$, respectively, the EIRP can be calculated as

$$EIRP_{TX,dBm} = P_{TX,dBm} + G_{A-TX,dBi} + 20\log N_{TX} \tag{2.2}$$

At the 5G frequency range 2 (FR2) bands, e.g., 24.25-to-29.5GHz and 37-to-43.5GHz, the channel loss at practical distances is mainly determined by the path loss (L_{path}). According to the Friis equation, assuming a line of sight (LOS) link, the path loss can be calculated as

$$L_{path,dB} = 20\log\frac{4\pi d}{\lambda} \tag{2.3}$$

where λ is the wavelength of the radiated signal and d is the distance.

Communication standards specify the allowable EIRP. On the other hand, the sensitivity of the phased-array receiver (RX) determines the minimum received power. Knowing the maximum EIRP ($EIRP_{max,dBm}$) and RX's sensitivity ($P_{RX-S,dBm}$), the maximum allowable path loss ($MAPL_{dB}$) can be calculated as

Table 2.1: The number of bits per symbol and the minimum EVM requirements of each modulation scheme in a 256-element phased-array TRX. The maximum EIRP (60dBm) at 28GHz is utilized to calculate the related MAPL and maximum distance.

Modulation		π/2 BPSK	QPSK	16-QAM	64-QAM	256-QAM
Bits per Symbol		1	2	4	6	8
Required EVM*		30%	17.5%	12.5%	8%	3.5%
Required SNR**		10.5 dB	15 dB	18 dB	21.9 dB	29.1 dB
SR=0.8 GS/s	MAPL	142.6 dB	138.1 dB	135.1 dB	131.2 dB	124 dB
	Maximum Distance	11.44 km	6.81 km	4.82 km	3.08 km	1.34 km
	Bit Rate	0.8 Gbit/s	1.6 Gbit/s	3.2 Gbit/s	4.8 Gbit/s	6.4 Gbit/s
BR=3 Gbit/s	MAPL	136.8 dB	135.3 dB	135.3 dB	133.2 dB	127.2 dB
	Maximum Distance	5.9 km	4.98 km	4.98 km	3.89 km	1.96 km
	Symbol Rate	3 GS/s	1.5 GS/s	750 MS/s	500 MS/s	375 MS/s

*3GPP Minimum EVM Requirements **Calculated based on Minimum EVM Requirements

$$MAPL_{dB} = EIRP_{max,dBm} - P_{RX-S,dBm} - LM_{dB} \tag{2.4}$$

where LM_{dB} is the link margin (also called fade or fading margin). The link margin is considered to compensate for practical losses such as reflection loss, polarization mismatch, implementation loss, and gain/loss flatness.

Moreover, the sensitivity of a phased-array RX with N_{RX} elements is expressed as

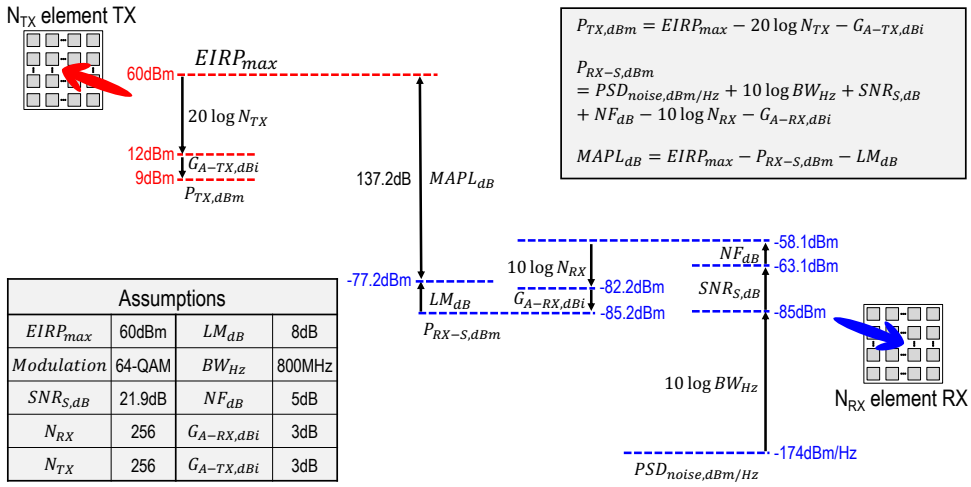
$$P_{RX-S,dBm} = PSD_{noise,dBm/Hz} + 10\log BW_{Hz} + SNR_{S,dB} + NF_{dB} - 10\log N_{RX} - G_{A-RX,dBi} \tag{2.5}$$

where $PSD_{noise,dBm/Hz}$ is the available noise power density at room temperature (-174dBm/Hz). NF_{dB} is the noise figure (NF) of each RX element, and $G_{A-RX,dBi}$ is antenna gain, including its connection losses. Additionally, BW_{Hz} is the desired signal's bandwidth, and $SNR_{S,dB}$ is the required signal-to-noise ratio (SNR) of the modulated signal to achieve the required bit error rate (BER). Note that only thermal noise contribution is considered for simplicity in this context. In practice, the sensitivity must be calculated based on signal-to-noise and distortion ratio (SNDR), considering the thermal noise, phase noise, in-band and out-of-band inter-modulation products, spurs, and blockers.

Assuming $EIRP_{max,dBm}$, LM_{dB}, NF_{dB}, and $G_{A-RX,dBi}$ are 60dBm, 8dB, 5dB, and 3dBi, respectively, and replacing (2.5) in (2.4), the MAPL_{dB} can be calculated as

$$MAPL_{dB} = 224dB.Hz - 10\log BW_{Hz} - SNR_{S,dB} + 10\log N_{RX}. \tag{2.6}$$

It shows the MAPL, and subsequently, the maximum allowable distance directly depends on N_{RX}. On the contrary, since the maximum EIRP is specified by standard, N_{TX} does not affect the link budget but determines the required output power of each TX element. Moreover, the MAPL is also related to the employed digital modulation and the signal bandwidth. The signal or channel bandwidth determines the symbol rate of the



Assumptions			
$EIRP_{max}$	60dBm	LM_{dB}	8dB
$Modulation$	64-QAM	BW_{Hz}	800MHz
$SNR_{S,dB}$	21.9dB	NF_{dB}	5dB
N_{RX}	256	$G_{A-RX,dBi}$	3dB
N_{TX}	256	$G_{A-TX,dBi}$	3dB

Figure 2.2: Link Budget calculation of a 256-element phased-array TRX.

communications link. Depending on the digital modulation scheme, one or more bits can be transmitted at each symbol. Therefore, employing a more complex modulation scheme with multiple bits per symbol results in higher spectral efficiency. However, the required SNR for demodulation at RX is higher for complex modulation schemes, thus affecting the MAPL. $\pi/2$ binary phase-shift keying (BPSK), quadrature phase-shift keying (QPSK), and 16/64/256 quadrature amplitude modulation (QAM) are considered as modulation schemes for 5G FR2 communications systems [8, 18].

The number of bits per symbol and the minimum error vector magnitude (EVM) requirements of each modulation scheme are presented in Table 2.1. Note that at the lower RX signal power levels, if we neglect all other nonidealities of the 5G communication link, the minimum required SNR is equal to the minimum EVM. Using (2.6) and considering a 256-elements phased array RX, the MAPL, the maximum distance, and the bit rate of the link are reported in Table 2.1. As discussed, by employing more complex modulations with a higher number of bits per symbol, the bit rate increases at the cost of supporting only shorter distances. This means there is a trade-off between spectral efficiency and link budget. To elaborate more, the link budget is calculated for various modulation schemes by targeting 3Gbit/s data throughput. This study illustrates the cost of increasing spectral efficiency. For instance, the 16-QAM signal occupies x2 more bandwidth than the 256-QAM signal while supporting x2.54 longer distance. Additionally, as 256-QAM signal demands 11.1dB better EVM, making its circuit design very challenging, thus dramatically increasing the power consumption. Nonetheless, the signal bandwidth is usually dedicated, and to satisfy the required throughput, employing complex modulation schemes is inevitable. Fig 2.2 shows the link budget calculation of a phased-array TRX with 256 elements for a 64-QAM 800MHz OFDM signal.

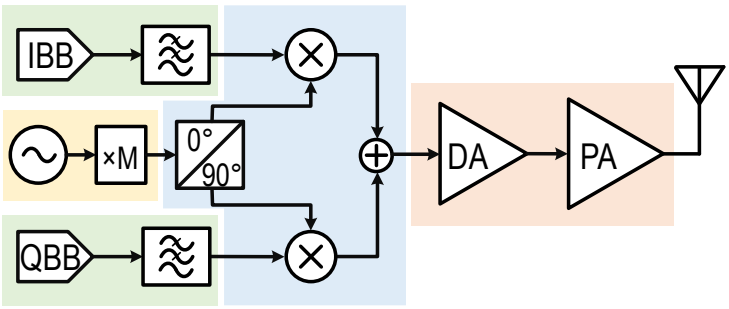


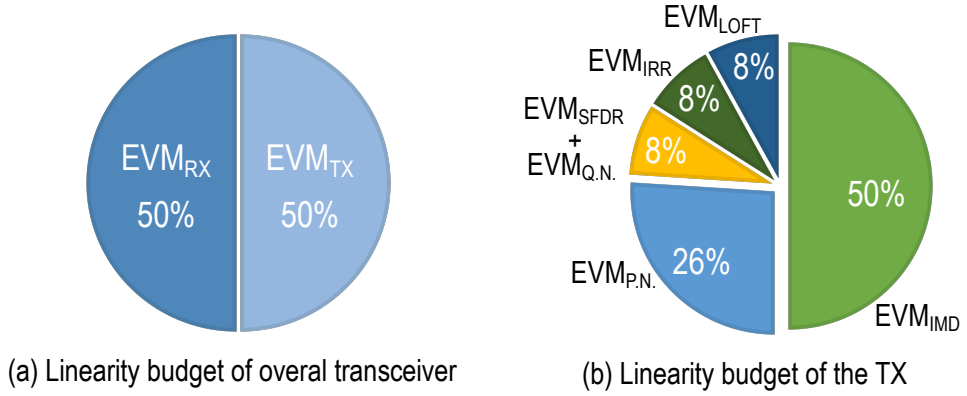
Figure 2.3: A simplified direct up-conversion TX architecture.

2.3. DIRECT UP-CONVERSION TX ARCHITECTURE AND DESIGN CHALLENGES

Among all possible TX architectures, direct up-conversion (DUC) TXs are equipped with a simple structure that leads to less power consumption, compact silicon size, and more amenability for integration in CMOS technologies. These make DUC an attractive architecture, particularly for digital or hybrid beamforming TXs, which must be extensively integrated with massive digital calibration and processing. However, DUC TX requires in-phase and quadrature-phase LO signals with high quadrature accuracy and phase noise at mm-wave frequencies. Additionally, the LO pulling can impair DUC TX since the PA amplifies the signal with the same frequency as the VCO oscillates. Fig. 2.3 illustrates a simple DUC TX architecture without any phase shifter or VGA in the mm-wave path. The TX consists of four parts, namely: 1) a frequency synthesizer and a multiplier, 2) an in-phase/quadrature (I/Q) modulator and a quadrature LO generator, 3) baseband DACs and low pass filter, and 4) a drive amplifier (DA) and a power amplifier (PA).

As shown in Fig. 2.3, the VCO oscillation frequency is ω_0/M to avoid the LO pulling. The phased noise of VCO depends on the resonator's quality factor (Q). At mm-wave frequencies, the inductors offer higher Q, while the varactor shows a limited Q. However, choosing a considerably large varactor portion is inevitable to achieve a wide tuning range. Therefore, despite the high Q of the inductor at mm-wave frequency, the limited Q of the large varactors determines the Q of the resonator, thus degrading the phase noise. Hence, implementing the synthesizer at a lower frequency and employing multipliers to bring the LO signal to mm-wave frequencies leads to a better phase noise than an mm-wave synthesizer. Moreover, typically, the synthesizer is shared between all DUC beamforming blocks, and each beamforming block is equipped with its own frequency multiplier [16]. In these architectures, the LO distribution splitter is realized at a low frequency with a simpler implementation and less loss.

As discussed, the 5G communication systems employ spectrally efficient modulation schemes, such as 64- and 256-QAM signals. Similar to RX, exploiting these complex modulated signals entails meeting stringent TX in-band linearity requirements verified by EVM. The nonideality of all parts of DUC TX contributes to the overall TX EVM, which comprises phase noise, quantization noise, spurious free dynamic range (SFDR), I/Q



(a) Linearity budget of overal transceiver

(b) Linearity budget of the TX

Figure 2.4: The linearity budgeting of a complete mm-wave transceiver and its TX part.

modulation imbalance, LO feedthrough (LOFT), and the PA non-linearity. The overall EVM of the TX can be estimated by

$$EVM_{TX} = \sqrt{EVM_{P.N.}^2 + EVM_{Q.N.}^2 + EVM_{SFDR}^2 + EVM_{IRR}^2 + EVM_{LOFT}^2 + EVM_{IMD}^2} \tag{2.7}$$

where $EVM_{P.N.}$, $EVM_{Q.N.}$, EVM_{SFDR}, EVM_{IRR}, EVM_{LOFT}, and EVM_{IMD} are the EVM degraded by phase noise, quantization noise, SFDR, I/Q modulation imbalance, LOFT, and the inter-modulation distortion (IMD), respectively. Note that the IMD is dominated by the nonlinearities of the PA, such as the nonlinear transconductance, the voltage-dependent nonlinear parasitic capacitors, and the gain compression at peak output power levels.

The overall linearity budgeting of an mm-wave transceiver (TRX) and its TX part are illustrated in Fig. 2.4. As depicted, an equal contribution is considered for both the TX and the RX. It means the EVM_{TX} and EVM_{RX} must be at least 3dB better (less) than the required EVM of the designated modulation scheme (for example, EVM_{TX}/EVM_{RX} < -32.1dB for a 256-QAM signal). On the contrary, the TX linearity is budgeted unequally because meeting the required specs is more challenging for some blocks than others. For instance, designing a highly linear PA with high efficiency is very challenging while achieving a considerably low LOFT is possible by calibration. Therefore, the largest portion of the nonlinearity budget is assigned to PA relaxing its design specifications. Additionally, more phase noise flexibility is considered for frequency synthesizer and multiplier, while the I/Q DACs, quadrature LO generator, and I/Q modulator should provide a considerably low EVM. For example, the required EVMs of the PA, phase noise, quantization noise, and SFDR, IRR, and LOFT for supporting a 256-QAM signal must be less than -35.1dBc, -38dBc, -43.1dBc, 43.1dB, and -43.1dBc, respectively. Note that the IRR and LOFT calibrations are challenging and expensive at mm-wave frequencies. Therefore, an architecture with inherently high IRR and low LOFT can drastically reduce the cost and complexity of the system calibrations.

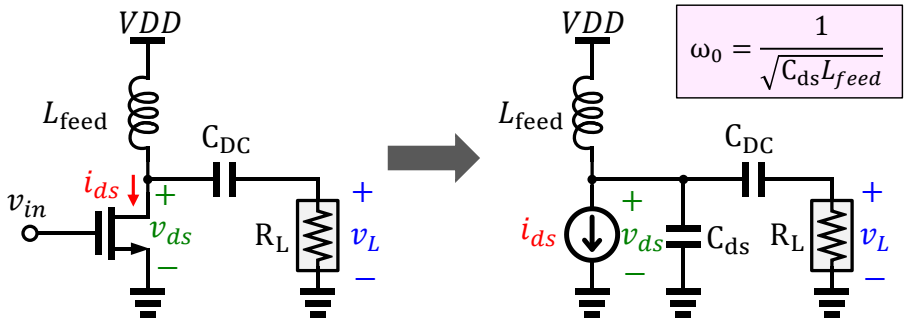


Figure 2.5: A simplified schematic of a class-B CMOS PA.

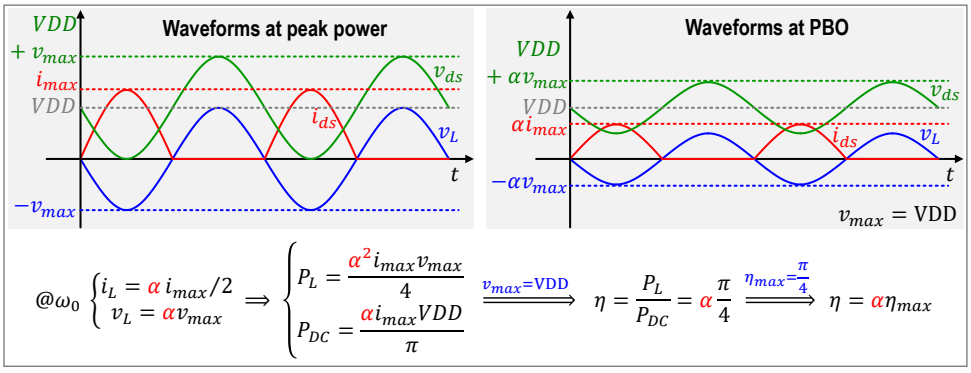


Figure 2.6: Current and voltage waveform of a class-B CMOS PA at peak and back-off power.

2.4. ENERGY EFFICIENT PAS AND DESIGN CHALLENGES

As the front-end, PA plays a critical role in determining the whole TX performance. The PA must deliver the required high-power signal to the antenna with high energy efficiency while maintaining the required linearity. This is particularly more challenging in mm-wave phased-array communication links dealing with wideband complex-modulated signals with large peak-to-average ratios (PAPRs). Moreover, the PA governs the TX performance against the voltage standing wave ratio (VSWR) of the antenna and its connection. Unfortunately, the VSWR effect is even worse in practical situations in which the mutual coupling among the closely spaced antennas yields a beam-steering angle-dependent and time-varying VSWR condition for the PAs driving these antenna elements [19–23]. In other words, the unwanted element-to-element coupled signal reflects the antenna, radiates alongside the desired signal, and, subsequently, deteriorates the phased-array beam pattern and TX linearity. In summary, the mm-wave 5G TXs demand a compact, broadband, highly efficient, VSWR resilient, and super linear PA.

A linear PA can be realized in different classes of operation, such as A, AB, B, C, and F, where each employs a dedicated conduction angle and requires a specific harmonic termination condition [24]. Fig. 2.5 depicts a simplified schematic of a class-B CMOS

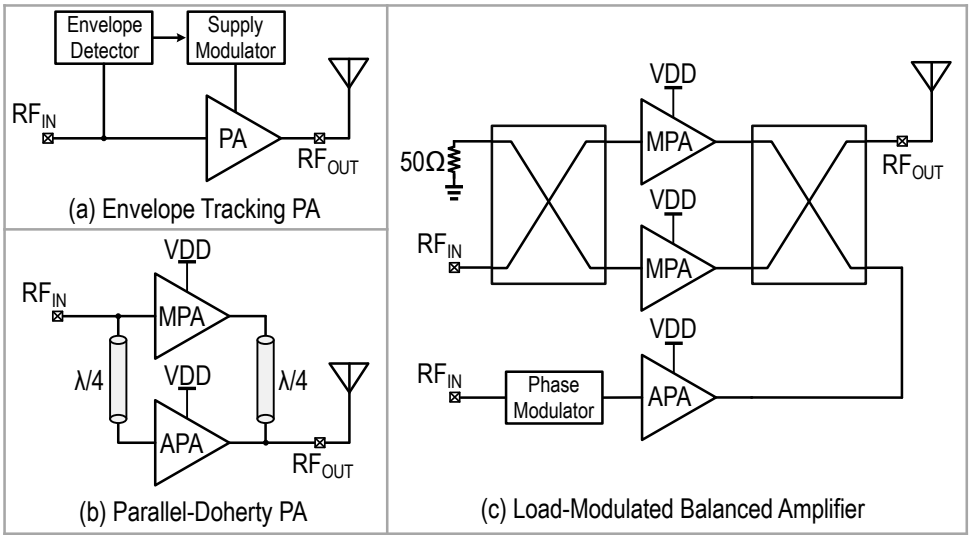


Figure 2.7: Conventional "RF-in RF-out" efficiency enhanced PA architectures: (a) envelope tracking PA, (b) Doherty PA, and (c) load-modulated balanced PA.

PA, with an LC resonator as its necessary harmonic terminations. In a class-B PA, the output voltage is directly determined by the drain current and the output matching applied. Fig. 2.6 illustrates current and voltage waveforms of a class-B PA and its power and efficiency equations, where α is the PA's normalized current amplitude. As shown, since both current and voltage are proportional to α, the output power (P_L) is proportional to α^2. In contrast, considering a constant supply voltage (VDD), the power consumption of a class-B PA is only determined by its drain current and, thus, is proportional to α. Consequently, as shown in Fig. 2.6, the drain efficiency is calculated as $\alpha\eta_{max}$ and decreases at back-off output power levels.

A straightforward way to improve the PA's efficiency is to increase its η_{max}. Low-loss distributed balun [25], class-F/F^{-1} [26–30], and dual-drive [31] PA architectures are recently proposed introducing high peak efficiency at mm-wave. However, the modern mm-wave PAs are operating at deep PBO amplifying complex modulation schemes with high PAPR, e.g., 10dB. Since the efficiency is still proportional to the signal's amplitude (α), the average efficiency of the mm-wave PAs is low, leading to a low TX system efficiency. Therefore, modern mm-wave TXs demand alternative PA architectures with PBO efficiency enhancement.

To extend the high peak efficiency of the PA to the back-off power levels, the efficiency needs to be constant and independent from α. Envelope tracking (ET) is an efficiency-enhanced PA architecture developed for providing a close to constant efficiency [32–34]. As depicted in Fig. 2.7(a), an ET PA is a linear PA where its supply voltage is modulated to track the envelope of the output signal. In this case, since the supply is a function of α, the power consumption becomes proportional to α^2, leading to a constant efficiency. However, practically, the supply modulator's bandwidth and dynamic range

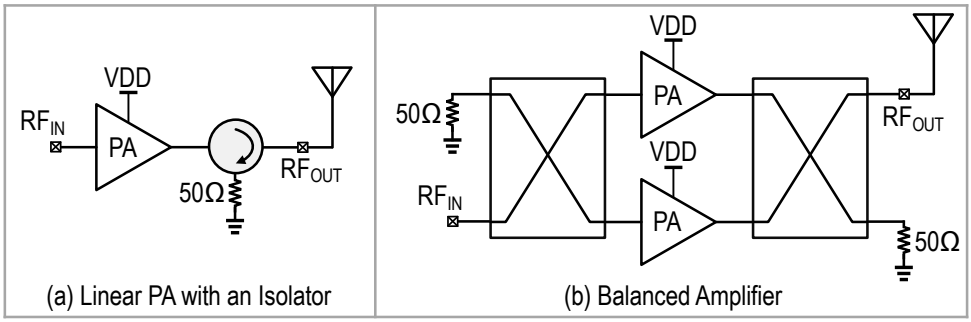


Figure 2.8: Conventional VSWR resilient PA architectures: (a) linear PA with an isolator, and (b) balanced amplifier.

are limited, making the ET not a proper solution for the large modulation bandwidth of the mm-wave 5G TX.

Another approach to enhance PBO efficiency is to modulate the load impedance of the PA in order to keep its voltage swing constant, independent from α. As a result, the power delivered to the load becomes proportional to α, resulting in a constant efficiency. Outphasing TX, Doherty PA, and load-modulated balanced amplifiers (LMBAs) are popular architectures to enhance efficiency at deep PBO by load modulation [35].

Outphasing PA combines two constant-envelope phase-modulated signals to generate envelope-vary output signal [36–40]. Consisting of two constant-envelop PAs enables high efficiency at both the peak and PBO. However, due to the nonlinear I/Q to phase conversion required in the Outphasing operation, the bandwidth of phase-modulated signals is expanded up to approximately ten times, while this architecture requires extremely fast digital signal processing and complex DPD.

In contrast, LMBAs [41–45] and Doherty PAs [12, 13, 46–63] are "RF-in–RF-out" PBO efficiency enhancement frontend solutions that support wideband modulation. As shown in Fig. 2.7(c), the LMBA structure consists of two main PAs and an auxiliary PA combined through a quadrature-hybrid coupler. Apart from its intrinsic wideband operation, the LMBA's power combiner complexities require a large die area, giving rise to a high insertion loss, thus diminishing its peak PAE. On the other hand, mm-wave DPAs are inherently narrowband due to their lumped-element quarter-wave transmission line (QTL) impedance inverter, necessary for load modulation (Fig. 2.7(b)). However, the broadband operation is achievable by increasing the complexity of the Doherty power combiner, compromising its passive efficiency [51, 52]. Also, their optimum PAE at PBO is narrowband in these architectures while providing broadband P_{1dB} [13, 56]. Therefore, realizing a compact mm-wave front-end with high average efficiency over broad operating frequencies while satisfying the tight element-to-element $\lambda/2$ lattice spacing requirement of the phased arrays is still challenging.

As mentioned, in an mm-wave phased array system, PAs experience high VSWR due to antenna impedance mismatch and the time-varying mutual coupling. Moreover, employing load modulation-based efficiency enhancement techniques, such as Outphasing, Doherty, and LMBA, makes the PA inevitably sensitive to the VSWR [8].

As illustrated in Fig. 2.8(a), a conventional solution for a VSWR resilient PA employs an isolator at its output. Due to the area constraint of the phased-array transceivers, an integrated isolator would be a viable solution. However, the integrated state-of-the-art mm-waves circulators/isolators [64–66] occupy a large area (>1.3mm^2) compared to the designated area of the whole transceiver [11]. Moreover, they demonstrate high TX-to-antenna loss (>3.2dB) and require extra power consumption to generate their quadrature clocks. Recently, balanced power amplifiers (BPAs) have been used at mm-wave to mitigate VSWR conditions [67, 68].

Fig. 2.8(b) depicts a conventional BPA comprising two identical PAs combined through a quadrature hybrid coupler (QHC). In the presence of an antenna load mismatch, the QHC provides an inverted antenna impedance for one of the PAs while the other PA sees the actual load. This balanced loading condition leads to the VSWR resilience of BPA. However, BPAs still suffer from low PBO drain efficiency.

2.5. SUMMARY

This chapter discussed the potential beamforming architectures for 5G FR2 communication systems. Besides analyzing the phase-array's link budget, its whole system has been studied, in which the maximum allowable distance is determined by the number of RX elements, modulation scheme, and channel bandwidth. It has been shown that the link budget can be optimized by employing a particular modulation scheme if the channel bandwidth is flexible. Moreover, the direct up-conversion TX is introduced as an energy-efficient and integration-friendly architecture for mm-wave phased array TXs. Likewise, the allowable nonlinearity of the TX for supporting a particular modulation scheme is budgeted based on the practical circuit design challenges of each contributor in the TX path. Since the PA's linearity and average efficiency directly determine the system performance, it obtains the highest nonlinearity budget for trading its performance. Moreover, PAs in a phased array TX experience a great VSWR due to the antenna placement and mutual coupling. Therefore, a VSWR-resilient PA structure is greatly appreciated in m-MIMO systems.

3

A MM-WAVE SERIES-DOHERTY PA WITH POST-SILICON INTER-STAGE PASSIVE VALIDATION

This chapter presents a wideband series-Doherty power amplifier (SDPA) for millimeter-wave (mm-wave) fifth-generation (5G) applications. It features a compact two-step impedance inverting-based series-Doherty power combiner that provides broadband close-to-perfect power back-off (PBO) efficiency enhancement. The AM-AM/AM-PM performance of the load-modulated Doherty power amplifier for broadband operation is analyzed. We also devise a post-silicon inter-stage passive validation (PSIV) approach to evaluate the mm-wave chip prototype utilizing the embedded voltage root mean square detectors. The proposed SDPA is realized in a 40-nm bulk CMOS, delivering 20.4dBm PAE_{SAT} with 39.1%/34% PAE at 0-/6-dB PBO. Over a 23.5-to-30GHz band, its PAE is >24% at 6-dB PBO. At 27GHz, applying a "2GHz 16-QAM OFDM" signal, the proposed SDPA generates 10.2dBm average power with 18.9% average PAE. The average error vector magnitude is better than -24.5dB without digital pre-distortion for a "400MHz 64-QAM OFDM" signal while generating an average output power of 8.8dBm with 15% PAE. The AM-AM/AM-PM of the realized SDPA is investigated employing a "50MHz 64-QAM OFDM" signal, validating our analysis and showing that the linearity limitation of DPAs is systematic and predictable. Utilizing the proposed PSIV approach, the frequency response of the input/inter-stage passive circuits are measured, indicating an excellent agreement with 3D EM simulation results.

This chapter is based on the paper published in the IEEE Journal of Solid-State Circuits [69].

3.1. INTRODUCTION

Mm-wave fifth-generation (5G) communication systems employ phased arrays to overcome the free-space path loss while providing high data throughput and low-latency line-of-sight links [5, 70, 71]. They typically employ spectrally efficient complex modulation schemes, such as high-order quadratic-amplitude modulations (QAMs) with high peak-to-average-power ratios (PAPRs) [4]. As discussed in Section 2.2, they pose stringent requirements on power amplifier's (PA) in-band linearity, verified by the error vector magnitude (EVM), and out-of-band spectral purity, examined by adjacent channel leakage ratios (ACLRs) [8, 18].

Meanwhile, low-cost nanoscale CMOS technologies are exploited for maximum integration, compact die area, and high yield. Nevertheless, generating the required power levels using CMOS technologies is challenging, especially with their limited supply voltage and maximum oscillation frequency (f_{max}). For instance, in the backhaul application with 16×16 antenna arrays, the average/peak PA power should exceed 9/20dBm. Furthermore, since the PA governs the overall performance of the transmitter (TX), its average efficiency directly determines the system efficiency, thus its thermal handling capability [8, 9].

Several mm-wave linear PAs are proposed to address the 5G specifications [25, 72–77]. To alleviate the efficiency issue, outphasing TXs offer high average efficiency, but they demand significant baseband overhead to generate outphasing signals and intensive digital pre-distortion (DPD) [36–40]. Doherty PAs (DPAs) [12, 13, 46–58, 60, 61] are "RF-in-RF-out" PBO efficiency enhancement front-end solutions that support wideband modulations. Conventional mm-DPAs are inherently narrowband due to their lumped-element quarter-wave transmission line (QTL) impedance inverter, which is necessary for load modulation. However, the broadband operation is achievable by increasing the complexity of the Doherty power combiner, compromising its passive efficiency [48, 52, 55]. Therefore, realizing a compact mm-wave front-end with high average efficiency over broad operating frequencies while satisfying the tight element-to-element $\lambda/2$ lattice spacing requirement of the phased arrays is still challenging.

This chapter introduces a series-DPA architecture with a two-step impedance inverting-based power combiner [59, 69]. In addition to its broad P_{1dB} bandwidth operation, it supports the desired 5G band, 24-to-30GHz, with >24% 6-dB PBO PAE. The design strategy is first to investigate the limitations of the basic Doherty topologies by examining their operational bandwidth. Choosing the series-DPA structure, we then synthesize a compact power combiner comprising two identical transformers, a coupled line connection, and a capacitor. Double-neutralized cascode push-pull PAs are utilized in the main/auxiliary paths to ensure stability over the entire operating band while generating the required output power with high PAE at both peak power and 6-dB PBO.

Moreover, the proposed DPA features embedded voltage root mean square (RMS) detectors to verify the system's reliability. We proposed a post-silicon inter-stage passive circuit validation (PSIV) approach to evaluate the mm-wave front-end chip prototype utilizing the embedded RMS detectors. The proposed PSIV approach can prevent discrepancies caused by modeling inaccuracy in the final product. It becomes particularly crucial when accounting for all parasitics, which cannot always be included in the sim-

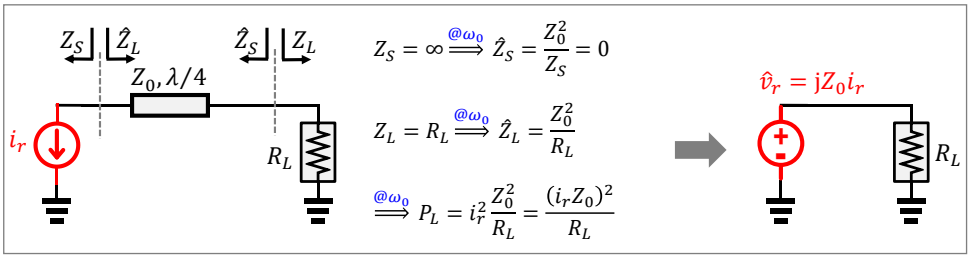


Figure 3.1: An ideal current source connected to the load with a quarter wave transmission line. At center frequency, this structure can be represented as an ideal voltage source connected to the load.

ulation [78].

This chapter is organized as follows. Section 3.2 reviews parallel- and series-DPA topologies and investigates their bandwidth and linearity limitations. The proposed two-step series-DPA is presented in Section 3.3. Section 3.4 elaborates on circuit implementation details of the DPA prototype fabricated in the 40nm bulk CMOS technology. The proposed post-silicon inter-stage passive validation approach is described in Section 3.5, comparing simulation and measurement results. Section 3.6 presents the experimental results, and we conclude the paper in Section 3.7.

3.2. DOHERTY PA TOPOLOGIES AND BANDWIDTH LIMITATIONS

As mentioned in Section 2.4, in a load modulation based efficiency enhanced PA structure such as Doherty, the goal is to keep the drain voltage swing constant (see Fig. 2.5 and Fig. 2.6). As the Doherty PA's operation basically relies on impedance inversion, it is necessary to learn how a quarter wave transmission line (QTL) is utilized to form the basic blocs of a Doherty PA. Fig. 3.1 illustrates an ideal current source connected to the load through a QTL. Note that the QTL serves as an impedance inverter at the design center angular frequency (ω_0). Therefore, as the impedance of the ideal current source (Z_S) is infinitive, its inverted impedance ($\hat{Z}_S$) becomes zero. On the other hand, the current source sees the inverted load impedance ($\hat{Z}_L = \frac{Z_0^2}{Z_L}$). Knowing that the impedance inverter converts the current to a determined voltage ($\hat{v}_r = jZ_0 i_r$), the load power is $\frac{(Z_0 i_r)^2}{R_L}$ where i_r is root-mean-square (rms) of current. As a result, the combination of the ideal current source and the impedance inverter can be modeled as an ideal voltage source, as illustrated in Fig. 3.1.

3.2.1. DOHERTY PA'S CONCEPT

A current source driving a resistive load (R_L) is depicted in Fig. 3.2 (left). Its voltage is dictated by the load voltage, thus is proportional to the current ($v_M = i_M R_L$). However, the voltage must stay constant independent of i_M to have a constant efficiency. Therefore, an auxiliary current-controlled voltage source (v_A) is utilized at the tail of the current

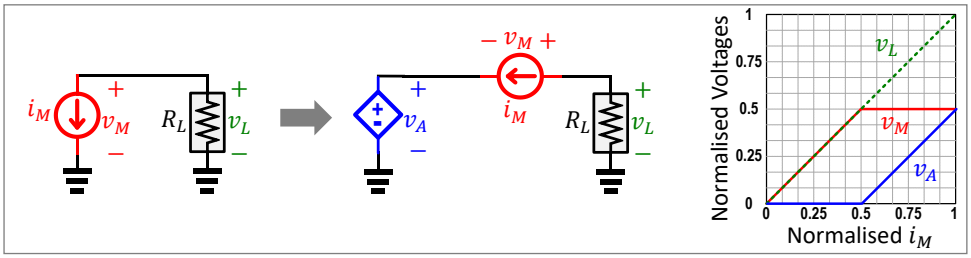


Figure 3.2: Constant efficiency current source structure utilizing a series connected auxiliary voltage source.

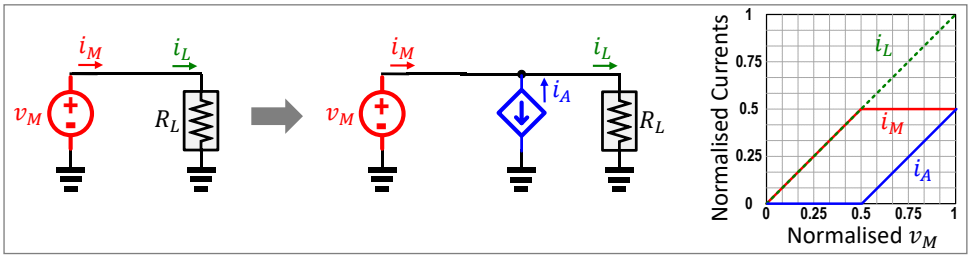


Figure 3.3: Constant efficiency voltage source structure utilizing a parallel connected auxiliary current source.

source, providing a voltage proportional to i_M. As a results, when the auxiliary voltage source is operating, the current source's voltage ($v_M = v_L - v_A$) stays constant, thus, its efficiency remains constant. As shown in Fig. 3.1, the voltage source can be implemented as a current source and an impedance inverter. It is crucial to mention that the infinitive impedance of the ideal current source isolates the auxiliary source from the load, meaning that the auxiliary source, indeed, does not contribute to the load power.

Fig. 3.3 shows, this time, a voltage source driving a resistive load (R_L). Obviously, its current (i_M) is the load current and proportional to its voltage ($i_M = \frac{v_M}{R_L}$). In this case, to achieve a constant efficiency, i_M must remain constant, independent of v_M. Therefore, an auxiliary voltage-dependent current source is employed in parallel with the main voltage source. As the auxiliary current (i_A) is proportional to the load current, the current of the main voltage source remains constant ($i_M = i_L - i_A$). Please note that since the output impedance of the voltage source is 0 and stands in parallel with the load, i_A indeed does not contribute to the output current but assists the main voltage source in maintaining a constant current. Again, the main voltage source can be implemented with a current source and an impedance inverter. In this case, the constant current of the voltage source will represent a constant voltage for the current source, owing to the impedance inverter.

Fig. 3.4 exhibits simplified Doherty PA (DPA) topologies [79] and their current/voltage profiles. In general, a DPA is a combination of the main PA (i_m), which determines the output power, and the auxiliary PA (i_a) that modulates the main PA's load

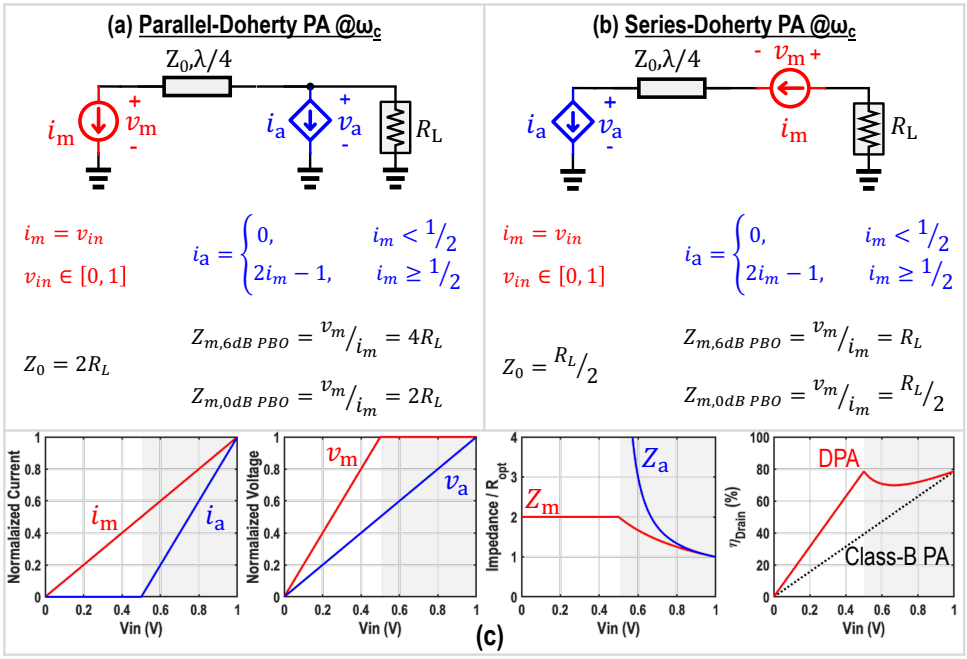


Figure 3.4: A simplified form of (a) the parallel-DPA and (b) the series-DPA at their designated carrier frequency. (c) Currents, voltages, impedances, and drain efficiency of the parallel-/series-DPAs.

(Z_m) to keep its drain voltage (v_m) at the maximum swing, maintaining the maximum efficiency. Therefore, in Fig. 3.4(a-b), the main PA is modeled as an independent current source (i_m) while the auxiliary PA is modeled as a current-controlled current source (i_a). Besides, a quarter-wave transmission line (QTL) is employed as an impedance inverter to realize load modulation. The DPA can be configured either in parallel-DPA (PDPA) or series-DPA (SDPA). However, the main and auxiliary PAs current forms are the same as demonstrated in Fig. 3.4(c). As shown, owing to the load modulation, the overall drain efficiency obtains a peak efficiency at 6-dB PBO, improving the efficiency by ×2 over a conventional class-B PA.

3.2.2. GAIN AND PHASE DEVIATION CAUSED BY Q MODULATION

The linearity limitations of conventional DPAs are investigated in the literature [80, 81]. However, the mm-wave CMOS DPA design requires thorough analysis to address 5G stringent design specifications. As illustrated in Fig. 3.4, a QTL is used as an impedance inverter to maintain load modulation. However, the QTL acts as a perfect impedance inverter only at its designated center frequency (f_c), thus deviating from f_c, which affects its performance. In addition, an inductor (L) is typically utilized to absorb the parasitic capacitor (C) of the PA, adding an LC resonator at f_c to the Doherty combiner. Subsequently, as shown in Fig. 3.5(a), the resonator's quality factor (Q) is modulated by load

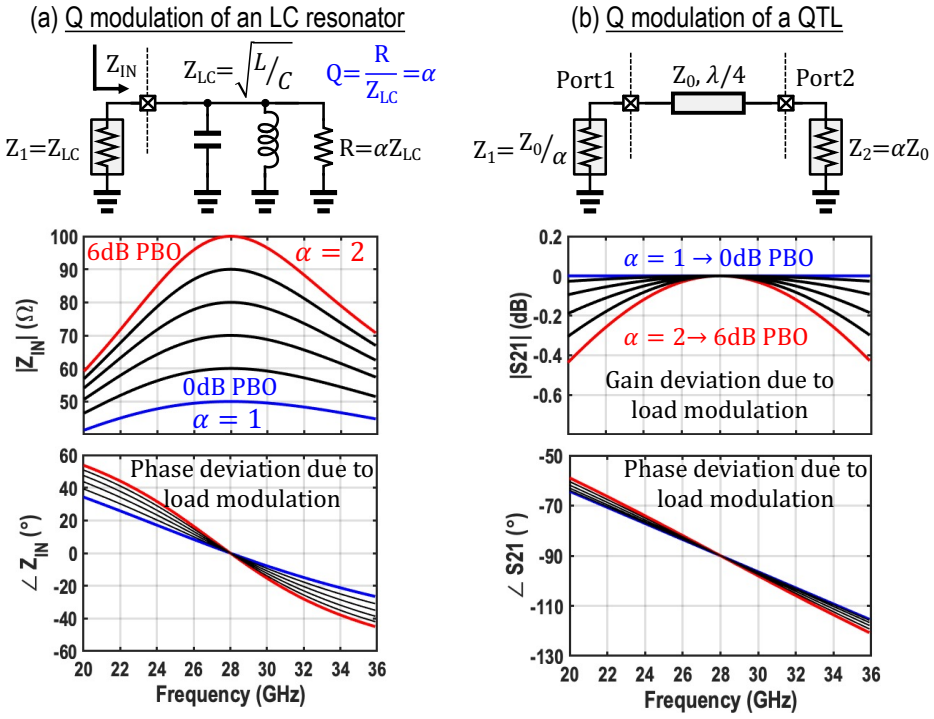


Figure 3.5: (a) Q modulation of a RLC resonator at 28GHz showing magnitude and angle deviation of its impedance. (b) Gain and phase deviations of a QTL under load modulation.

modulation, resulting in magnitude and angle deviations. Likewise, the bandwidth of the QTL varies while its load modulates from $2Z_0$ to Z_0 where Z_0 is QTL's characteristic impedance. Fig. 3.5(b) exhibits the S-parameter simulation results of a QTL at 28GHz, showing gain and phase deviations.

In mm-wave DPAs, the device parasitic capacitors are absorbed in either a transformer-based [49–54] or coupled line-based [13, 55, 56] baluns. In either case, the described phenomenon is directly translated into amplitude-to-amplitude (AM-AM) and amplitude-to-phase (AM-PM) distortions in wideband operation.

3.2.3. BANDWIDTH ANALYSIS OF PARALLEL- AND SERIES-DPAS

Fig. 3.6 demonstrates practical mm-wave PDPA and SDPA models. The current sources are connected to the matching network by an ideal 1:n transformer. Note that employing transformers is inevitable for connecting the push-pull PAs to its Doherty combiner at mm-wave frequencies. Besides, the LC resonators are considered alongside the current sources to model their absorbed device capacitors. Applying the current waveforms shown in Fig. 3.4(c), the normalized main PA's load impedance is depicted versus normalized output power at various frequencies (Fig. 3.7). As demonstrated, even without

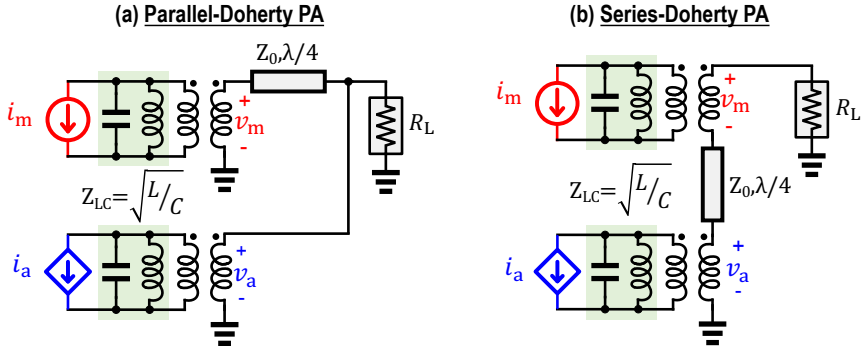


Figure 3.6: Practical forms of (a) parallel- and (b) series-DPAs with ideal transformers and inductors to resonate out PAs' parasitic capacitors.

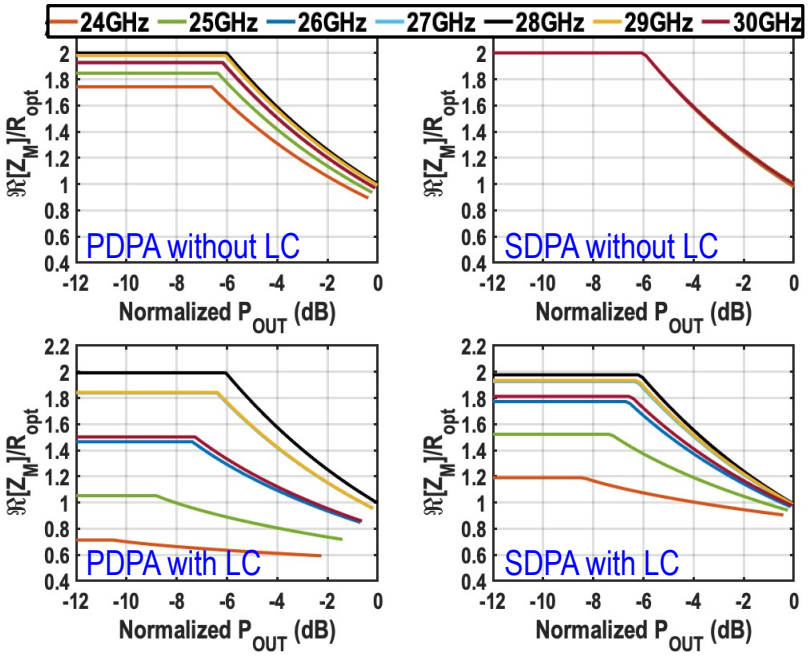


Figure 3.7: The real part of main PA's load, normalized to R_{opt}, for PDPA and SDPA with and without LC resonators.

an LC, due to the QTL at the main PA path, the load modulation of PDPA and output power slightly degrade when operated away from its center frequency (28GHz). Adding LC resonators exacerbates PDPA's performance.

On the other hand, SDPA offers frequency-independent output power with ideal load modulation. It is due to its main PA acting as a high-impedance power device, which is modeled as an ideal current source, and perfectly isolates the auxiliary PA from the

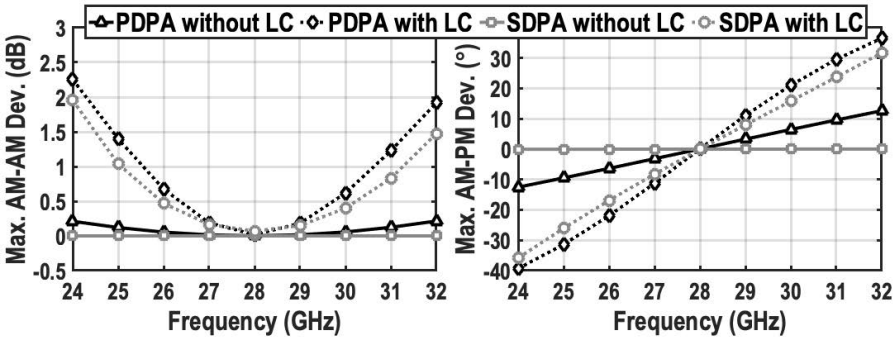


Figure 3.8: Maximum AM-AM/AM-PM deviations of PDPA and SDPA with and without LC resonators.

output. Besides, since the main PA directly drives the resistive output load, the output power is frequency-independent. However, the auxiliary PA is no longer isolated from the output by adding an LC resonator alongside the main PA, causing output power and load modulation degradation, as shown in Fig. 3.7. Nevertheless, it can be observed that even with an LC resonator, the SDPA provides a broader load modulation and much more stable output power than PDPA, where the output power deviations of SDPA and PDPA are 0.4dB and 2.2dB, respectively (see Fig. 3.7, bottom).

Moreover, the AM-AM and AM-PM of PDPA and SDPA are simulated with and without LC resonators. As depicted in Fig. 3.8, without an LC resonator, the maximum AM-AM/AM-PM deviations of PDPA slightly increase when operated away from its center frequency (28GHz), while SDPA's AM-AM/AM-PM deviations are always zero. Adding LC resonators exacerbates their AM-AM/AM-PM performance, becoming 2.3dB/-40° and 1.9dB/-36.5° for PDPA and SDPA, respectively. It indicates that even though the SDPA offers significantly broader load modulation performance, the Q modulation phenomena shown in Fig. 3.5 degrade the AM-AM/AM-PM distortions of both topologies almost equally.

In summary, in both configurations with realistic device capacitance, load modulation creates AM-AM and AM-PM distortions when a DPA operates far from its center frequency. However, SDPA clearly shows broader load modulation and output power as an efficiency enhancement PA, making it a suitable choice to support the mm-wave 5G operational band (e.g., 24-to-30GHz). Furthermore, in practice, lossy components mitigate the AM-PM distortions by diminishing Q modulation of LC resonators and QTLs. Moreover, we can infer that extending the load modulation backward (e.g., 12-dB PBO) exacerbates Q modulation, thus worsening the AM-AM/AM-PM deviations. Additionally, as suggested in [52], the frequency coverage can be extended in the cost of the die area overhead by employing static phase aligners in the main and auxiliary PAs.

3.2.4. WIDEBAND LUMPED-ELEMENT TWO-STEP IMPEDANCE INVERTER

Heretofore, an ideal QTL is considered as the impedance inverter in the earlier discussions and simulations. However, the impedance inverter of an mm-wave DPA is often realized by a lumped-element QTL to address phased array systems' strict die area re-

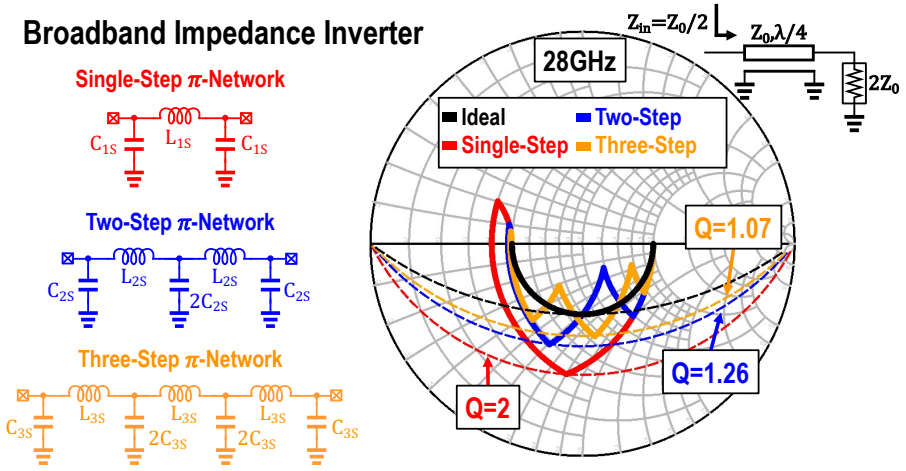


Figure 3.9: Single-, two-, and three-step C-L-C π-network QTLs implementations and their inversion paths from $2Z_0$ to $Z_0/2$.

strictions. The designated QTL plays a critical role in a Doherty power combiner performance. Therefore, in this sub-section, three possible lumped component implementations of the QTLs are investigated. Fig. 3.9 illustrates the single-step ($\lambda/4 \rightarrow \theta_{1S} = 90°$), two-step ($2 \times \lambda/8 \rightarrow 2 \times \theta_{2S} = 90°$), and three-step ($3 \times \lambda/12 \rightarrow 3 \times \theta_{3S} = 90°$) capacitor-inductor-capacitor (C-L-C) π-network QTLs. Considering an n-step lumped element QTL with Z_0 characteristic impedance, the L_{nS} and C_{nS} can be calculated as [12]

$$L_{nS} = \frac{Z_0 \sin\theta_{nS}}{\omega_c} \tag{3.1}$$

$$C_{nS} = \frac{\tan\frac{\theta_{nS}}{2}}{Z_0\omega_c} \tag{3.2}$$

where $\theta_{nS} = 90°/\mathrm{n}$ and ω_c is designated center angular frequency ($\omega_c = 2\pi \times f_c$).

The inversion paths of a $2Z_0$ impedance to $Z_0/2$ of an ideal QTL compared to three C-L-C π-networks are plotted in the Smith chart depicted in Fig. 3.9. Considering that the quality factor represents the bandwidth ($Q = \frac{\omega_c}{\Delta\omega}$, where $\Delta\omega$ is the half-power bandwidth) during impedance inversion, the inversion path of single-step touches constant Q=2 line while the two-step and three-step cross Q=1.26 and Q=1.07. Therefore, the broadband operation is achievable by a higher-order approximation of the QTL. Comparing the simulated Q of QTLs, Fig. 3.9 indicates that a two-step structure compared to a single-step one improves the bandwidth by 59%, whereas it becomes 87% using a more complicated three-step counterpart. Fig. 3.10 exhibits S-parameter simulation results of different QTLs, where Port1 and Port2 are $Z_0/2$ and $2Z_0$, respectively. As demonstrated, the S_{11} of single-step is narrow-band, while two-/three-step QTLs provide the matching condition as good as an ideal QTL. Likewise, the S_{21} of the single-step QTL exhibits narrower bandwidth than the three other QTLs. Consequently, choosing a two-step QTL improves the bandwidth reasonably while trading off with its passive complexity.

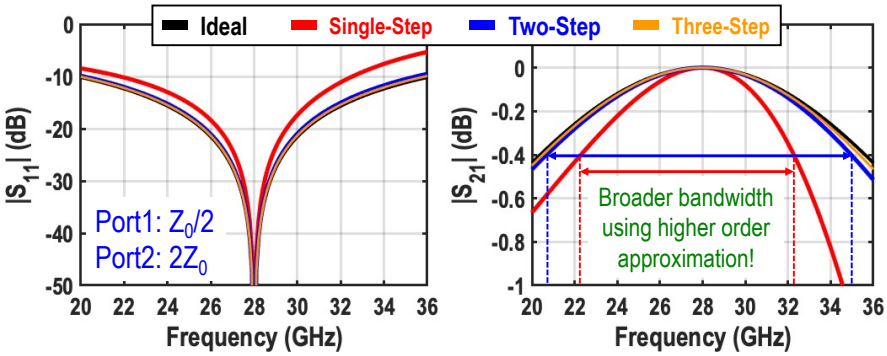


Figure 3.10: The simulated S_{11} and S_{21} of different QTLs.

3.3. PROPOSED SERIES-DOHERTY POWER COMBINER

Fig. 3.11 unveils the proposed transformer-based two-step series-Doherty power combiner in four progressive steps considering identical main and auxiliary PAs. First, the SDPA introduced in Fig. 3.6(b) is depicted by replacing the ideal QTL with the proposed two-step C-L-C π-network (Fig. 3.11(a)). The phase shift of the QTL's first and second steps (θ_1 and θ_2) are considered different as a degree of freedom, while their combined phase must be 90°. However, θ_1 and θ_2 should be almost the same to benefit bandwidth improvement. The shunt inductors (L_M) resonate out the main/auxiliary PAs parasitic capacitors (C_P) at the desired frequency. Besides, n is chosen to provide the PAs' optimum load (R_{opt}).

As shown in Fig. 3.11(b), a series inductor (L_3) is employed to absorb the output pad's parasitic capacitor (C_L). Additionally, the shunt inductors are moved to the secondary side of the transformers (L'_M). By assuming L_1=L_3=L_K, L'_M and L_K can be considered magnetizing and leakage inductors of a non-ideal transformer, respectively. Consequently, the ideal transformers and their corresponding inductors are replaced by non-ideal transformers with a k_m coupling factor, as demonstrated in Fig. 3.11(c). Besides, the C_1 shunt capacitor of the impedance inverter is absorbed into the parasitic capacitor of the auxiliary PA ($C_P \rightarrow C_P + C'_1$).

Lastly, the second single-ended π-network is replaced by a three-port coupled lined with a differential input and single-ended output to improve ground signal path loss and diminish the auxiliary PA's unbalanced signals. The progressive steps of this transformation are demonstrated in Fig. 3.12. First, the single-ended π-network is converted to a differential network. As the characteristic impedance must stay the same, the value of inductances becomes half of its single-ended counterpart ($\frac{L_S}{2}$). Since self-coupling of a differential inductor is inevitable, the inductors are replaced by a coupled line, assuming a positive coupling. The positive coupling factor (k_S) reduces the differential inductance by ($1-k_S$), thus the required inductance becomes larger ($L'_S = \frac{L_S}{2(1-k_S)}$). As the last step, the output was modified to a single-ended connection intact. However, in practice, since a single-ended connection changes the parasitic capacitors' states, a minor modification is required to recover the desired performance. Note that k_S is a degree of freedom to ad-

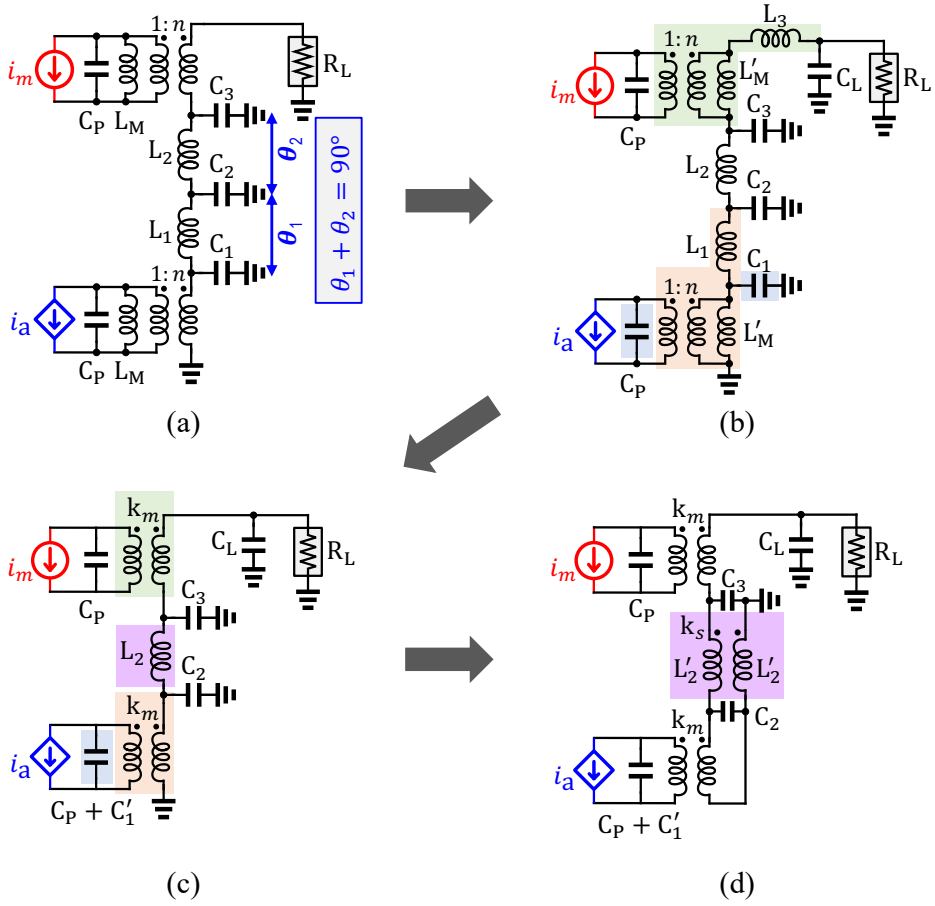


Figure 3.11: (a) The SDPA with two-step C-L-C π-network. (b) The output PAD's parasitic capacitor (C_L) and a series inductor (L_3) for impedance matching are added, while L_M moved to the secondary sides of the transformers. (c) The ideal transformers and their corresponding inductors are replaced by non-ideal transformers with a k_m coupling factor. (d) The second π-network series inductor (L_2) is replaced by a coupled-lines connected as a triaxial balun.

just the length of the lines and achieve the optimum layout. Also, the C_3 is removed for further Doherty phase alignment.

3.3.1. PROPOSED SERIES DOHERTY COMBINER DESIGN FRAMEWORK

In this sub-section, the closed-form design equations of all parameters introduced in Fig. 3.11 are derived. Fig. 3.13 reflects the equations of the lumped-element model of a transformer [82] and L-network impedance matching, which will be employed to synthesize the proposed series combiner. The primary and secondary inductors of the transformer are denoted as L_P and L_S, respectively.

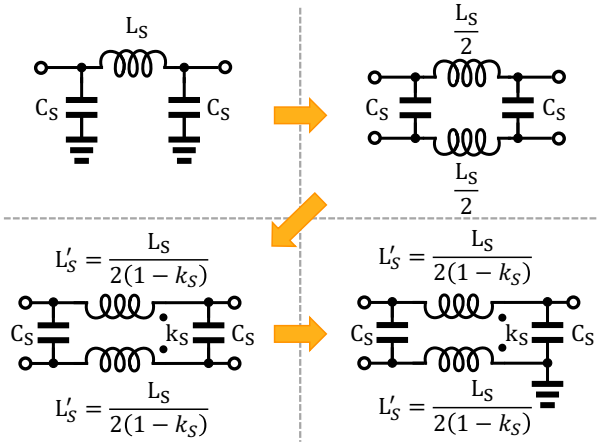


Figure 3.12: The progressive steps of replacing the two-port single-ended π-network with a three-port differential-to-single-ended network.

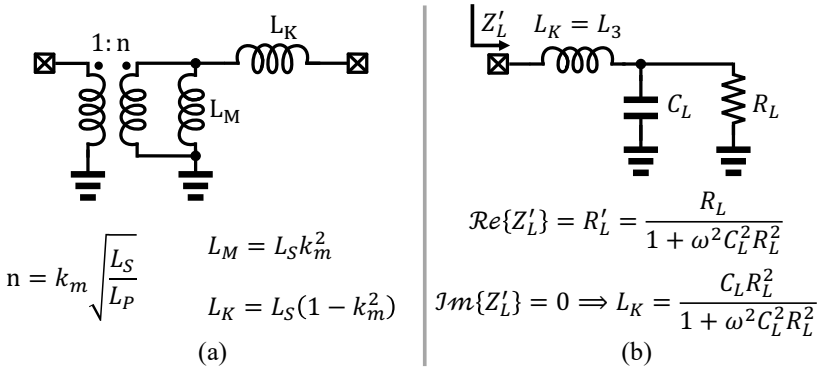


Figure 3.13: The equations of (a) the lumped-element model of a transformer and (b) an L-network impedance matching.

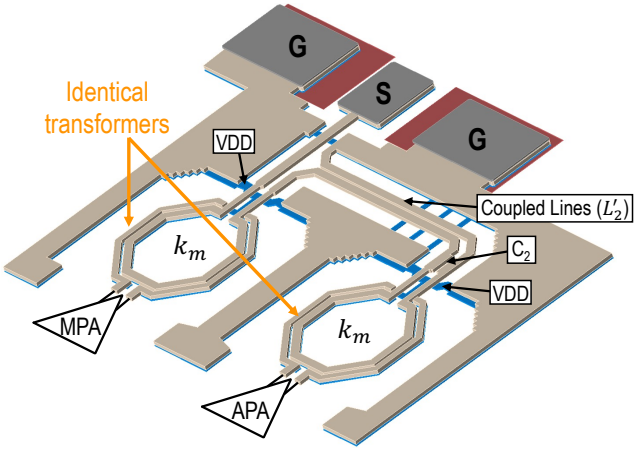
To begin with, the primary inductor of the transformer, exploited to absorb the parasitic capacitor of the PA (C_P), can be calculated as

$$L_P = \frac{1}{\omega_c^2 C_P} \tag{3.3}$$

Using the equations introduced in Fig. 3.13, the converted load can be expressed as

$$R'_L = \frac{R_L}{1+Q^2} = \frac{R_L}{1+\omega_c^2 C_L^2 R_L^2}. \tag{3.4}$$

Note that we assume C_P and PA's optimum load (R_{opt}) are extracted according to the desired peak output power. Besides, the turn ratio of the transformer can be expressed



	Components	Value	
Transformer Parameters	Secondery Side Connection	Diff.	Single-ended
	L_P	198pH	206pH
	L_S	164pH	178pH
	k_m	0.65	0.67
	Passive Efficiency	86.7%	85.6%
Lamped Elemets	C_2	290fF	
	L'_2	172pH	
	k_S	0.66	
	R_{opt}	56.2Ω	

Figure 3.14: The proposed series-Doherty power combiner layout and its 3D EM simulated parameters.

as follows:

$$R_{opt} = \frac{R'_L}{2n^2} \Rightarrow n = \sqrt{\frac{R'_L}{2R_{opt}}} = k_m \sqrt{\frac{L_S}{L_P}}. \tag{3.5}$$

Moreover, using the equations shown in Fig. 3.13, we calculate

$$L_3 = L_K = (1 - k_m^2) L_S = \frac{R_L^2 C_L}{1 + \omega_c^2 C_L^2 R_L^2}. \tag{3.6}$$

Then, by solving (3.5) and (3.6), L_S and k_m can be derived as follows:

$$L_S = R'_L (R_L C_L + \frac{L_P}{2R_{opt}}), \tag{3.7}$$

$$k_m = \sqrt{\frac{L_P}{2R_{opt} R_L C_L + L_P}}. \tag{3.8}$$

Since we assumed L_1=L_3, using (3.1) and (3.2), the phase shift of the first step π-network and its corresponding capacitors can be calculated as

$$\theta_1 = \sin^{-1} \frac{2(1 - k_m^2) L_S \omega_c}{R'_L}, \tag{3.9}$$

$$C_1 = \frac{2 \tan \frac{\theta_1}{2}}{R'_L \omega_c}, \tag{3.10}$$

Consequently, considering that θ_2=90°-θ_1, the inductor and capacitors of the second step π-network are expressed as

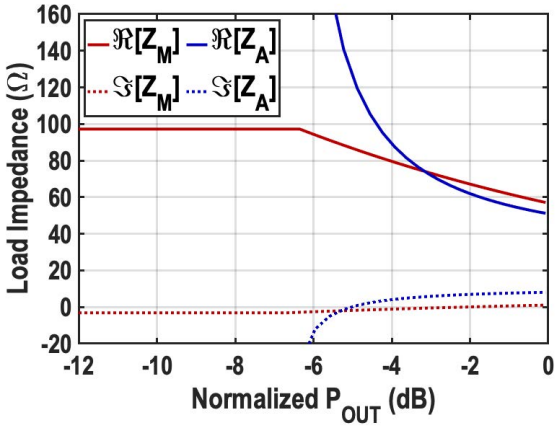


Figure 3.15: The real (solid) and imaginary (dotted) parts of main and auxiliary PAs' load impedance versus normalized output power at 28GHz.

$$C_3 = \frac{2\tan\frac{90°-\theta_1}{2}}{R'_L\omega_c}, \tag{3.11}$$

$$L_2 = \frac{R'_L \sin(90° - \theta_1)}{2\omega_c}. \tag{3.12}$$

Since C_2=C_1+C_3 all design parameters are calculated. The last step is to choose k_S based on layout consideration and to calculate the required L'_2 using (see Fig. 3.12)

$$L'_2 = \frac{L_2}{2(1-k_S)}. \tag{3.13}$$

In summary, first, the parasitic capacitors of the output PAD (C_L) and the push-pull PA (C_P) are estimated using the available technology. Then, by employing the introduced framework, all initial design parameters can be calculated using (3.3) to (3.13). Lastly, we realize the series-Doherty PA in the available technology and optimize its performance through EM simulations. Note that employing advanced technologies with lower parasitic capacitors leads to better agreement between the initial calculated values based on first-order models and the final realized parameters obtained from EM simulations.

3.3.2. LAYOUT AND EM SIMULATION RESULTS

The layout of the proposed series-Doherty combiner is depicted in Fig. 3.14. It consists of two identical transformers with a coupling factor of k_m=0.65 to provide the optimum load of the PAs. The passive efficiency reported in Fig. 3.14 is calculated based on the maximum passive efficiency formula introduced in [83]. Nonetheless, due to the capacitive coupling between the primary and secondary sides of the transformer, its parameters are slightly different when configured as a balance-to-unbalance (balun) converter.

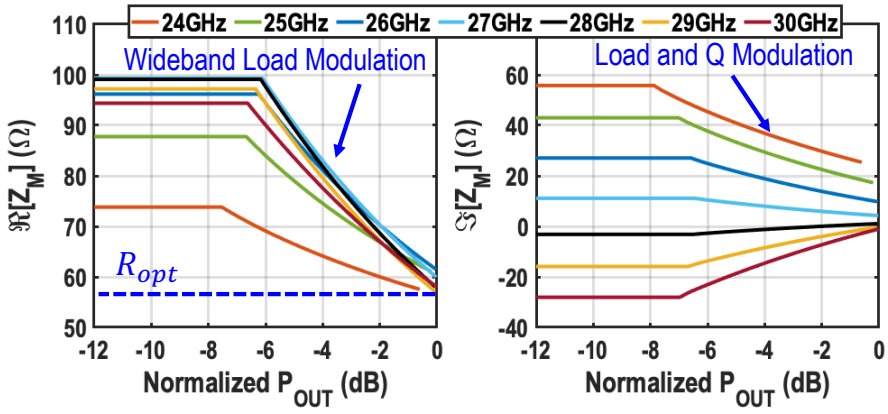


Figure 3.16: The real (left) and imaginary (right) parts of the main PA's load impedance at various frequencies.

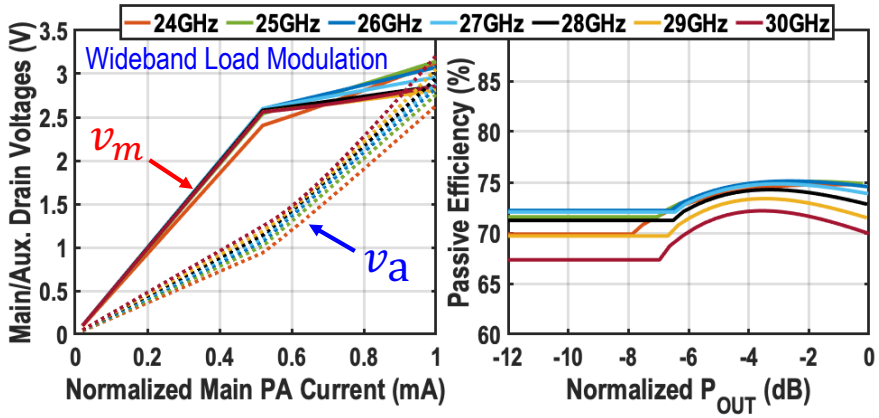


Figure 3.17: The main and auxiliary PAs' drain voltages and the passive efficiency of the proposed series-Doherty combiner at various frequencies.

Therefore, since the configurations of the transformers are different for main and auxiliary PAs, the calculated parameters should be adjusted to achieve the desired performance. The real and imaginary parts of the main and auxiliary PA's load impedance are exhibited in Fig. 3.15. According to simulations with an ideal PA model, the proposed layout offers wideband load modulation and efficiency enhancement. Fig. 3.16 shows the simulated main PA's real and imaginary impedance versus normalized output power in the 24-to-30GHz band. Additionally, the main and auxiliary PAs' drain voltages and the passive efficiency of the proposed series-Doherty power combiner are demonstrated in Fig. 3.17.

Moreover, the AM-AM/AM-PM using the proposed combiner's 3D EM simulation results are illustrated in Fig. 3.18. Compared to an ideal loss-less SDPA with LC resonators (See Fig. 3.6), the inherent loss of the power combiner alleviates PA's AM-PM while worsening its AM-AM performance.

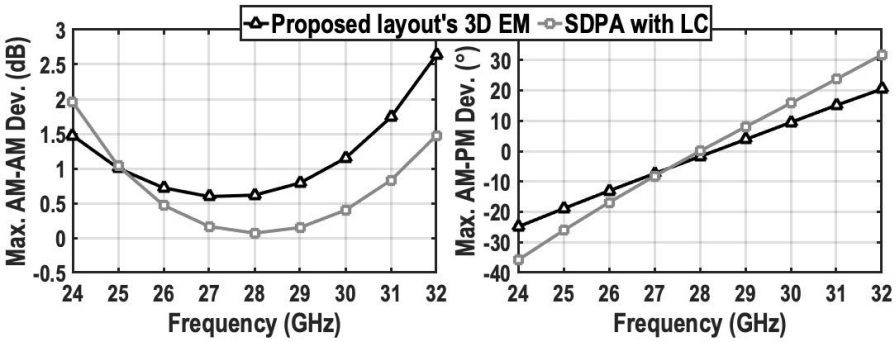


Figure 3.18: Maximum AM-AM/AM-PM deviations using 3D EM model of the proposed series-Doherty combiner compared to ideal SDPA with LC resonators.

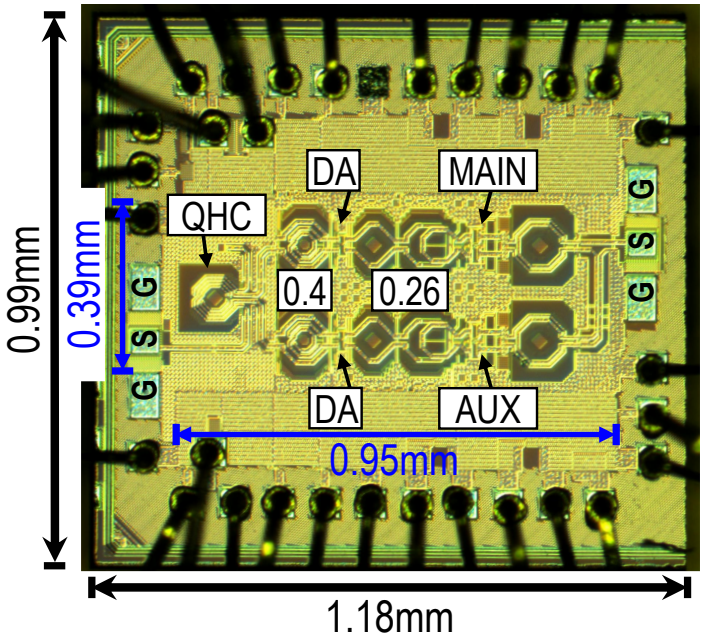


Figure 3.19: Die photo of the implemented series-DPA.

3.4. CIRCUIT IMPLEMENTATION

The proposed series-DPA is implemented in 40nm bulk CMOS technology (Fig. 3.19). The chip occupies an area of 1.18mm × 0.99mm, while its core area is 0.39mm × 0.95mm. Fig. 3.20 exhibits a detailed schematic of the DPA architecture. A quadrature hybrid coupler (QHC) is employed to generate the 90° phase advance for the DPA and provide wideband input impedance matching. Fig. 3.21 demonstrates the schematic and

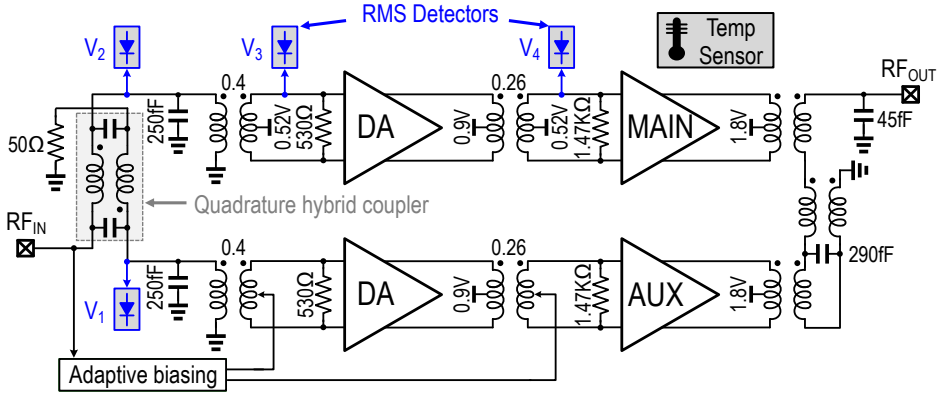


Figure 3.20: A detailed schematic of the DPA architecture.

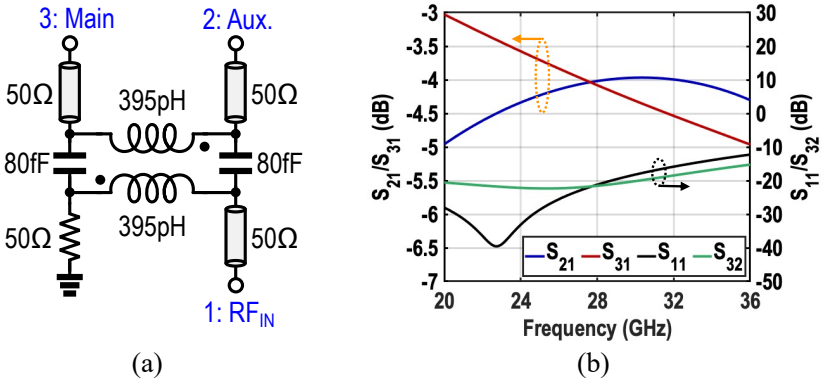


Figure 3.21: (a) Schematic of the input QHC and (b) its S-parameter simulation results.

S-parameter simulation results of the input QHC including the 50-Ω coplanar transmission lines insertion losses. In the simulation, Port1, Port2, and Port3 are input, auxiliary, and main paths, respectively. Its insertion loss is 1.05 dB while providing more than 21 dB isolation between two PAs. 3D view of the input QHC and main/Aux PAs' Balun is depicted in Fig. 3.22. The double-tuned input Balun offers >9GHz 1dB bandwidth owing to its 0.4 coupling factor. Each main/auxiliary branch consists of a neutralized driver amplifier (DA), a double-tuned transformer as an inter-stage matching network, and a cascode PA. Adaptive biasing circuits modulate the biases of the auxiliary branch to perform Doherty load modulation. Moreover, four embedded voltage root mean square (RMS) detectors are utilized to measure all mid-stage signal levels (V_1-V_4) of the proposed DPA structure. Also, a temperature sensor, i.e., a diode-connected bipolar transistor, is employed to measure chip temperature and calibrate the RMS detectors.

Fig. 3.23 depicts the detailed schematic of cascode PA and DA. In [73], the drain-

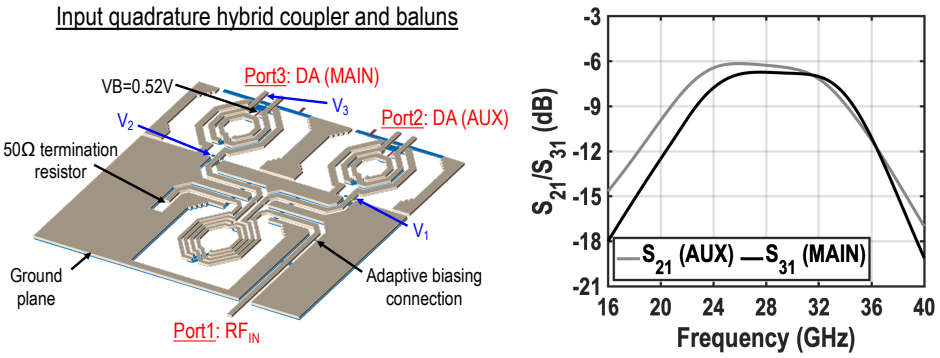


Figure 3.22: 3D view of the input quadrature hybrid coupler and baluns, and its S_{21}/S_{31} simulation results.

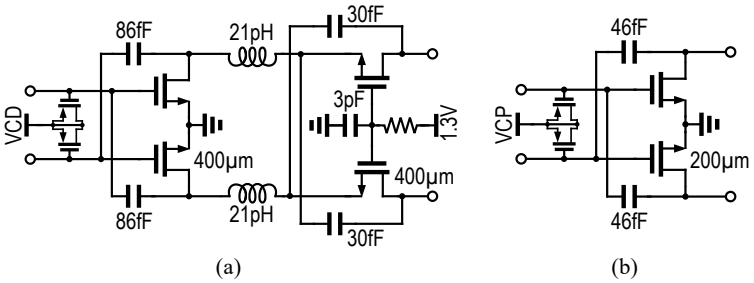


Figure 3.23: The schematic of (a) the double-neutralized cascode PA, and (b) the common-source driver amplifier.

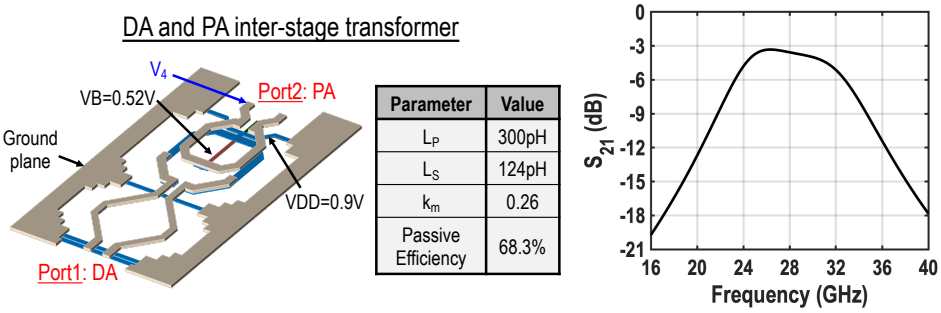
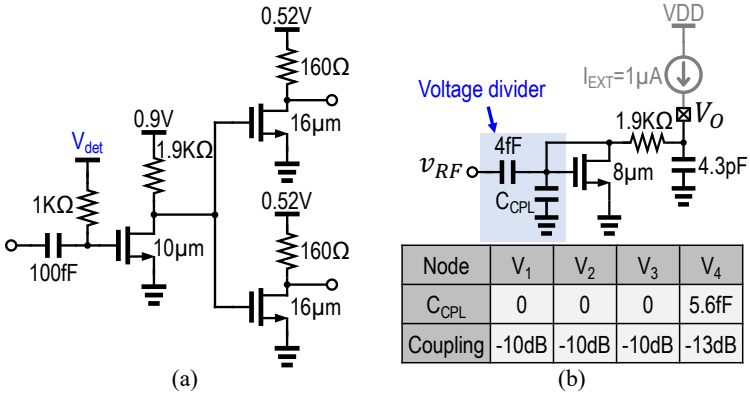


Figure 3.24: DA and PA inter-stage matching transformer and its S_{21} simulation results.

source capacitors of the common-gate transistors are used to boost the gain, owing to the common-gate transistor's high gain (>1) in a class-AB operation with a sizeable quiescent current. In this work, to realize class-B main/auxiliary PAs, two pairs of neutral-



Node	V_1	V_2	V_3	V_4
C_{CPL}	0	0	0	5.6fF
Coupling	-10dB	-10dB	-10dB	-13dB

Figure 3.25: (a) The schematic of the adaptive biasing circuits, and (b) the schematic of the RMS detector with its capacitive coupler.

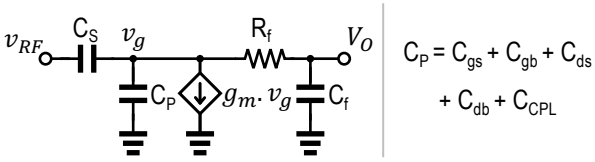


Figure 3.26: A simplified small-signal model of an RMS detector.

ization capacitors are used for common-source and common-gate transistors to maximize output-to-input isolation of the PA, resulting in unconditional stability [84]. Besides, two 21pH inductors align voltage and current wave phases, thus improving the drain efficiency [72]. Each common-source transistor of PA/DA consists of eight/four unit-cells with a transistor aspect ratio of 50μm/40nm, optimized to mitigate the impact of device parasitics and interconnections [78]. The cascode transistors comprise five unit cells with a transistor aspect ratio of 80μm/40nm. Besides, two varactors are utilized at the PA and DA inputs to improve their AM-PM profiles [85].

Fig. 3.25 illustrates the schematic of the adaptive biasing circuits and the RMS detector [86]. Adaptive biasing circuits consist of a single-ended envelope detector and two drivers for DA and PA. The load modulation can be adjusted using the detection bias voltage of the envelope detector (V_{det}). The RMS detectors are biased with an external 1μA current source to work in the subthreshold region. Due to the exponential subthreshold voltage-to-current profile of the NMOS, the RMS of the input RF signal is down-converted to DC [86]. As demonstrated, capacitive coupling is employed to sense the signal at each node. The series capacitor (4fF) and shunt capacitors, e.g., C_{CPL} and NMOS's parasitic capacitor, form a capacitive voltage divider. Therefore, large C_{CPL} is chosen at the nodes with large swing voltages. Since the series capacitor is 4fF, the input capacitor of the RMS detector is significantly small, and thus its loss is negligible.

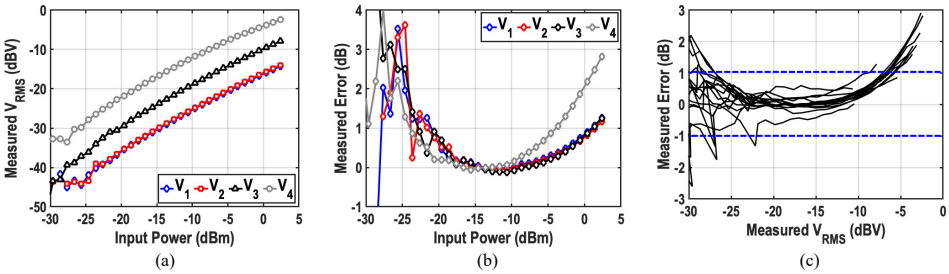


Figure 3.27: (a) The measured RMS voltages at various nodes versus PA input power. (b) The measured error of each RMS detector compared to an ideal RMS detection line. (c) The detection error of V_4 at the 20-to-34GHz band versus its measured output voltage.

3.5. POST-SILICON INTER-STAGE PASSIVE VALIDATION (PSIV)

Although the front-end passive stages (e.g., PA and LNA matching networks) directly determine the system's performance in the mm-wave circuit design, the inter-stage passive networks also affect the overall performance [74, 87]. They include matching networks of inter-amplification stages, quadrature LO generators (e.g., quadrature hybrid coupler) [88], passive phase shifters [11], splitters, and combiners. In inter-stage matching networks, achieving a broad operating band with reasonable insertion loss is challenging. For instance, in a mm-wave PA, as the transistors' gate resistance is optimized to achieve high f_{max}, they provide high-Q parasitic capacitors. Subsequently, using a transformer to absorb the parasitic capacitors results in an overall high-Q resonator and, thus, narrow bandwidth. Therefore, adding an extra resistor to enhance the related operational bandwidth is inevitable. Since the additional resistor decreases power gain, it establishes a critical design trade-off between bandwidth and PAE, significantly affecting the PA performance.

Therefore, to fully evaluate a prototype chip, measuring the performance of the inter-stage passive circuits is crucial. Typically, the designers fabricate these circuits separately to measure their passive performance, increasing die area and measurement cost. Nonetheless, considering the variable parasitic capacitance of the active devices, the "dynamic" performance of inter-stages passive networks may vary compared to a standalone implementation. Besides, process/temperature variation and aging can also influence the performance, whereas their effect cannot be measured separately.

This section proposes a post-silicon inter-stage passive validation (PSIV) approach to measure the inter-stage matching networks bandwidth with negligible insertion loss, die area, and power consumption overhead.

3.5.1. PROPOSED PSIV APPROACH AND ITS LIMITATIONS

To realize the proposed PSIV approach, we used the earlier introduced RMS detectors to quantify the voltage level at each stage [89]. Then, the voltage gain can easily be calculated by dividing the measured voltages. Subsequently, by sweeping the frequency, the inter-stage gain is obtained versus frequency, representing the bandwidth of the desig-

nated inter-stage passive network.

The accuracy of the PSIV approach is mainly defined by RMS detectors' performance and their error mismatches. Fig. 3.26 depicts a simplified small-signal model of the RMS detectors, dismissing all parasitic resistances. Assuming $\frac{1}{|j\omega C_f|} \ll R_f$, and $\frac{1}{|j\omega C_P|} \ll R_f||\frac{1}{g_m}$, the capacitive coupling ratio (A_{CP}) can be determined as

$$A_{CP} = \frac{v_g}{v_{RF}} \cong \frac{C_S}{C_S + C_P}. \tag{3.14}$$

The basic theory of a nonlinear device is analyzed in [90]. In the square-law detection region, the detected low-frequency current Δi is proportional to the microwave power dissipated in the nonlinear device P_D. The ratio $\Delta i/P_D$, called current responsivity and denoted by β, determines the DC output voltage to microwave RMS voltage detection gain. As shown in [90] and [91], the detection gain is expressed as

$$\beta = \frac{\Delta i}{P_D} = \frac{V_O}{v_{g,RMS}^2} = \frac{i''(v_g)}{2i'(v_g)} = \frac{q}{2nkT}, \tag{3.15}$$

where n is ideality factor, V_O is DC output voltage, and $v_{g,RMS}$ is RMS of v_g. Also, $i(v_g)$ represents the drain current, whereas its first and second derivations are proportional to DC output and RMS voltages, respectively [90]. Subsequently, considering the capacitive coupling ratio, the overall detector gain is

$$\frac{V_O}{v_{RF,RMS}^2} = \beta \times A_{CP}^2 = \frac{q}{2nkT} \times (\frac{C_S}{C_S + C_P})^2. \tag{3.16}$$

According to (3.16), the overall gain can be configured by adjusting C_{CPL} to reduce the coupling ratio, as shown in Fig. 3.25. C_{CPL}=5.6fF is chosen for V_4 to reduce its voltage coupling ratio by -3dB. Moreover, since β depends only on the ideality factor and temperature, the detection gain is independent of bias and geometry. Thereby, the detection gain variation over process mainly depends on capacitors' mismatches and does not impose any sizing constraint on the device.

Fig. 3.27(a) demonstrates the measured RMS voltages at various nodes versus PA input power at 25GHz. It affirms 6.2dB passive voltage gain of DA input transformer (1:2 turn ratio) and 6.9dB DA voltage gain. The measured RMS voltages are compared to an ideal RMS detection line, and the errors are presented in Fig. 3.27(b). Since the RMS detectors are employed in an energy-efficient PA, the power consumption increases at the higher input power levels. Thus, the chip temperature increases accordingly. The chip temperature is measured using an on-chip sensor, showing only a 3.8° increase during measurement thanks to the proposed highly efficient PA structure. Note that each input power level is applied for a relatively long time to ensure the chip temperature reaches its steady-state mode during the measurement.

Even though (3.16) shows detection gain directly depends on temperature, the detection accuracy is mostly limited by the device's dynamic range rather than temperature. For instance, V_4 shows a more significant error than V_3 because it experiences 6.9dB larger voltages while its coupling factor is only 3dB less than V_3. Therefore, choosing an

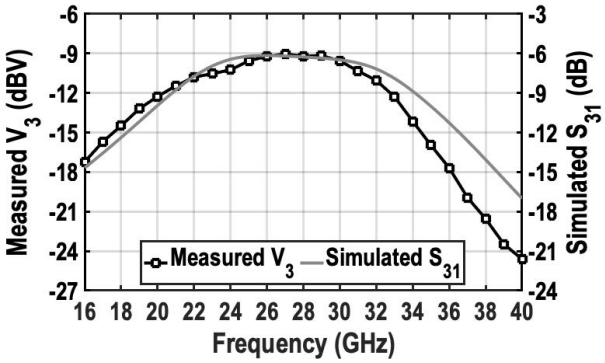


Figure 3.28: The measured RMS voltage at DA's input while the input power is 0dBm (left axis), and the 3D EM simulation results (right axis).

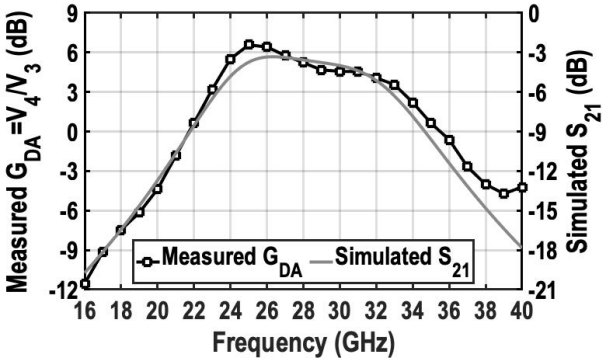


Figure 3.29: The measured DA's gain using RMS voltages at inputs of DA and PA (left axis), and the 3D EM simulation results (right axis).

appropriate coupling ratio at each stage is essential to keep the detectors' signal levels the same to experience almost the same inaccuracy, thus mitigating their error in calculating the gain. Nevertheless, the interstage gain can be measured at the back-off power levels, where all RMS detectors provide significantly high accuracy. Fig. 3.27(c) exhibits the detection error of V_4 at various frequencies versus its measured output voltage.

3.5.2. INTER-STAGE PASSIVE CIRCUITS EVALUATION RESULTS

Fig. 3.28 exhibits the measured RMS voltage at the DA input (V_3) while the input power is 0dBm (left axis). Besides, the S-parameter simulation adopting the order of the ports as mentioned in Fig. 3.22 is plotted (right axis). The simulated 3dB bandwidth (BW_{3dB}) is 21-to-34GHz, while it became 20-to-32.7GHz on the prototype chip. Furthermore, as illustrated in Fig. 3.29, the DA gain is measured using $G_{DA} = \frac{V_4}{V_3}$ and compared to the corresponding inter-stage matching network's (see Fig. 3.24) S-parameter simulations. Despite the more in-band ripple mainly exacerbated by DA's active devices, it exhibits an excellent agreement between measurement and simulation. It achieves more than

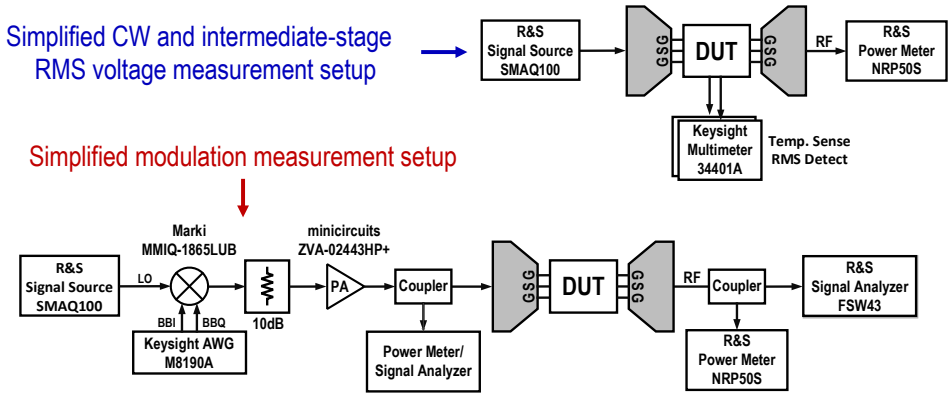


Figure 3.30: Simplified CW and modulation measurement setups.

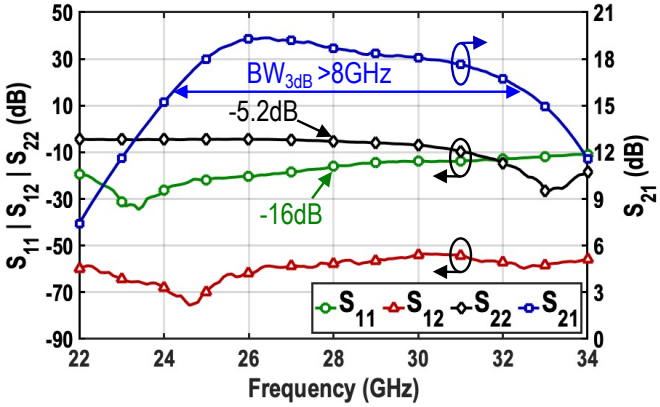


Figure 3.31: The S-parameter measurement results of the proposed SDPA.

10GHz BW_{3dB}, slightly higher than the simulations.

3.6. MEASUREMENT RESULTS

All measurements are performed using a high-frequency probe station. The DC supplies, bias voltages, and RMS detector pads are wire-bonded directly to an FR4 printed circuit board (PCB). In this work, 1.8V supply voltage is used for the PAs, and 0.9V for the driver amplifiers. Fig. 3.30 exhibits the CW and modulated signal measurement setups. The power loss of the probes is obtained from the specific measured S-parameter files provided by the producer. The insertion loss of the cables and the directional couplers are measured and de-embedded.

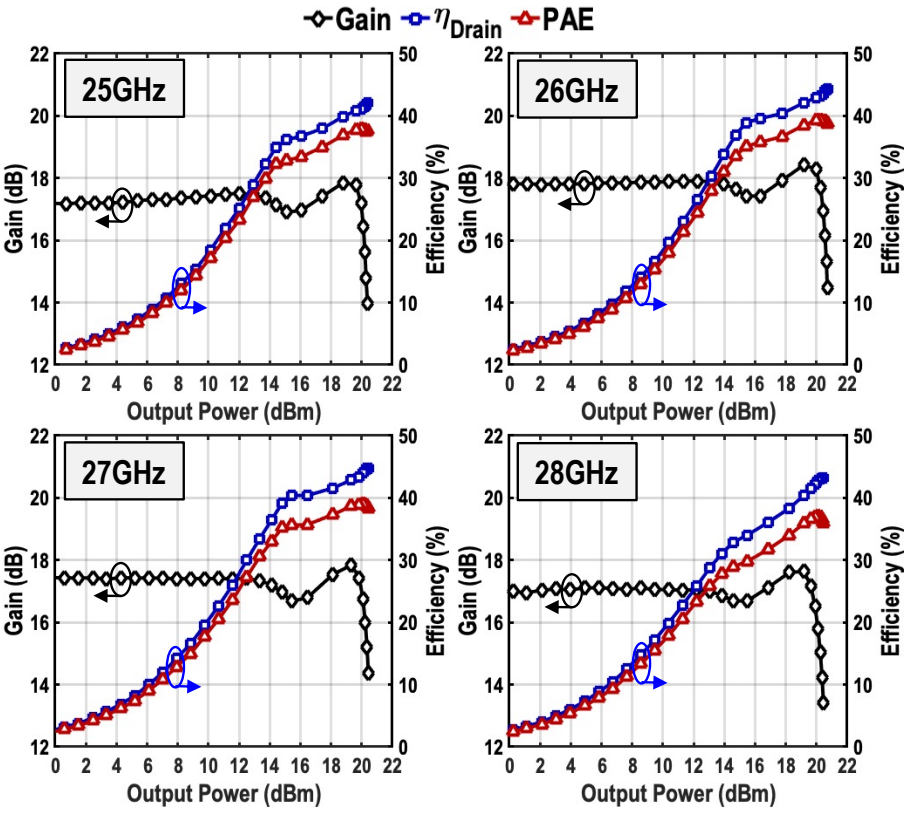


Figure 3.32: The measured gain, last-stage drain efficiency, and PAE versus output power at various frequencies.

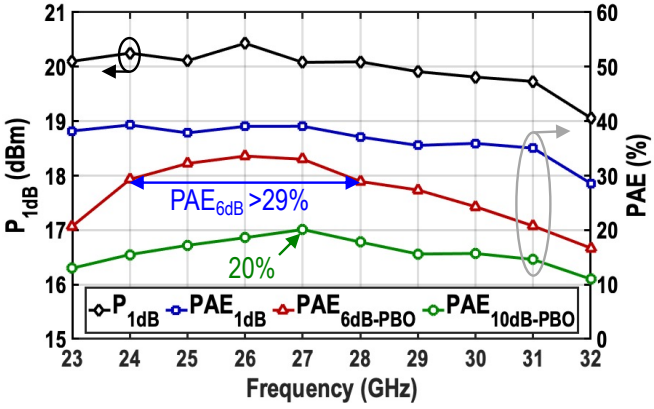


Figure 3.33: The measured output power and PAE at 0-/6-/10-dB PBO versus frequency.

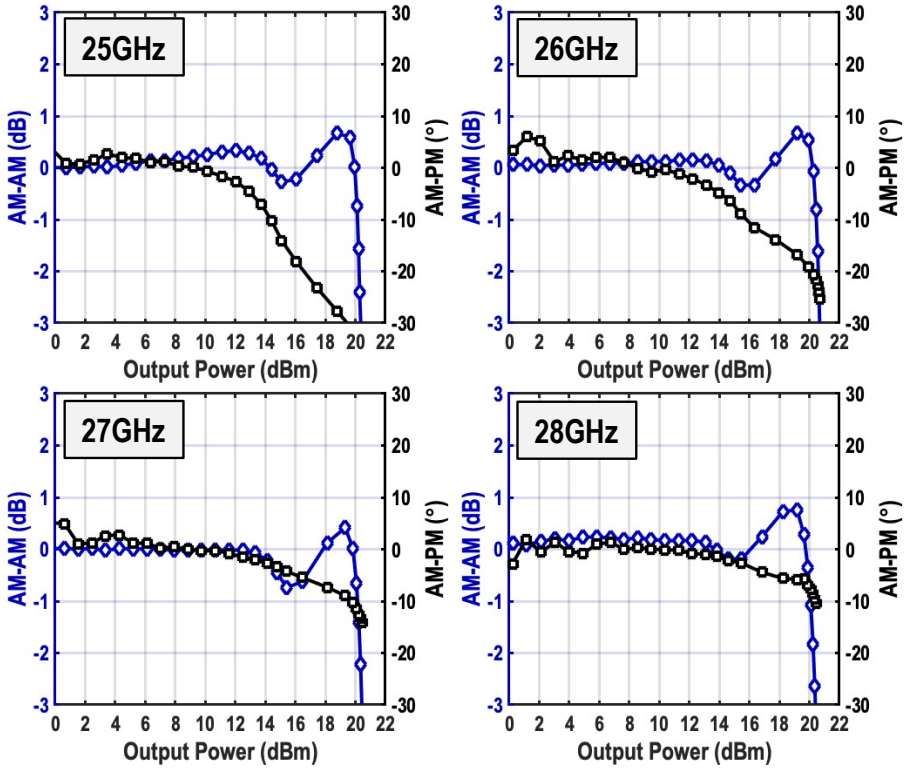


Figure 3.34: The measured AM-AM and AM-PM distortion versus output power at various frequencies.

3.6.1. CONTINUOUS-WAVE MEASUREMENT RESULTS

The small-signal S-parameter performance is measured using the Keysight N5227A network analyzer. As Fig. 3.31 demonstrates, the PA achieves more than 8GHz small-signal BW_{3dB} where its S_{12} and S_{11} are less than -54dB and -12.8dB, respectively. At 28GHz, PA's S_{22} is -5.2dB while its input matching is -16dB. The PA offers 18.3dB small-signal gain at 28GHz.

The large signal CW measurement results are reported in Fig. 3.32 for various operational frequencies. At 27GHz, the P_{1dB} and P_{SAT} are 20.2dBm and 20.43dBm, respectively. Its PAE at P_{1dB}, 6-dB PBO, and 10-dB PBO are 39.1%, 34%, and 20%, respectively. Moreover, as shown in Fig. 3.33, the PA provides more than 19dBm P_{1dB} over a 23-to-32GHz band (i.e., -1dB bandwidth). The proposed DPA's 6-dB PBO PAE is >29% over the 24-to-28GHz band and >24% over the 23.5-to-30GHz band. Besides, a slow amplitude-modulated ramp signal (2μs) is applied to measure AM-PM distortion, employing the modulation measurement setup shown in Fig. 3.30. The measured AM-AM/AM-PM distortions are demonstrated in Fig. 3.34 for various frequencies. Note that the input varactors of the DAs and the PAs (see Fig. 3.23) are used to minimize AM-PM distortions at each operational frequency.

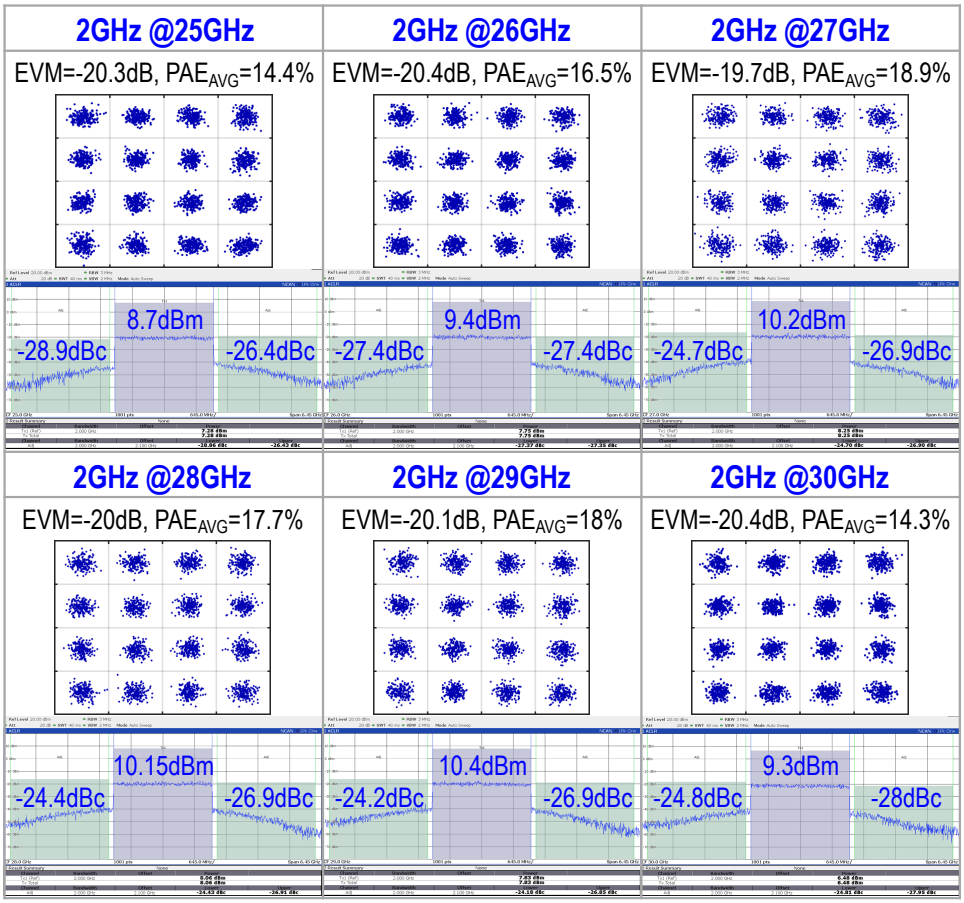


Figure 3.35: The measured constellations/spectrums for a "2GHz 16-QAM OFDM" signal at various frequencies.

3.6.2. MODULATED SIGNAL MEASUREMENT RESULTS

The PA dynamic performance is verified by wideband modulated signals such as "16-QAM OFDM" and "64-QAM OFDM" signals. As demonstrated in Fig. 3.30, the baseband I/Q modulated signals are generated with an arbitrary waveform generator (Keysight AWG M8190A) and upconverted using a Marki I/Q mixer. A directional coupler is employed at the output to provide the signal for an R&S FSW43 signal analyzer, while an R&S NRP50S measures the output power. Fig. 3.35 exhibits measured constellations and spectrums of a 2GHz 16-QAM OFDM signal at 25-to-30GHz carrier frequencies. Without using any DPD, the DPA achieves almost -20dB EVM while the PAPR is 9.5~10dB. At 27GHz, the proposed DPA generates 10.2dBm average power (P_{AVG}) with 18.9% average PAE.

A 64-QAM OFDM signal is utilized to verify the performance of the proposed DPA for

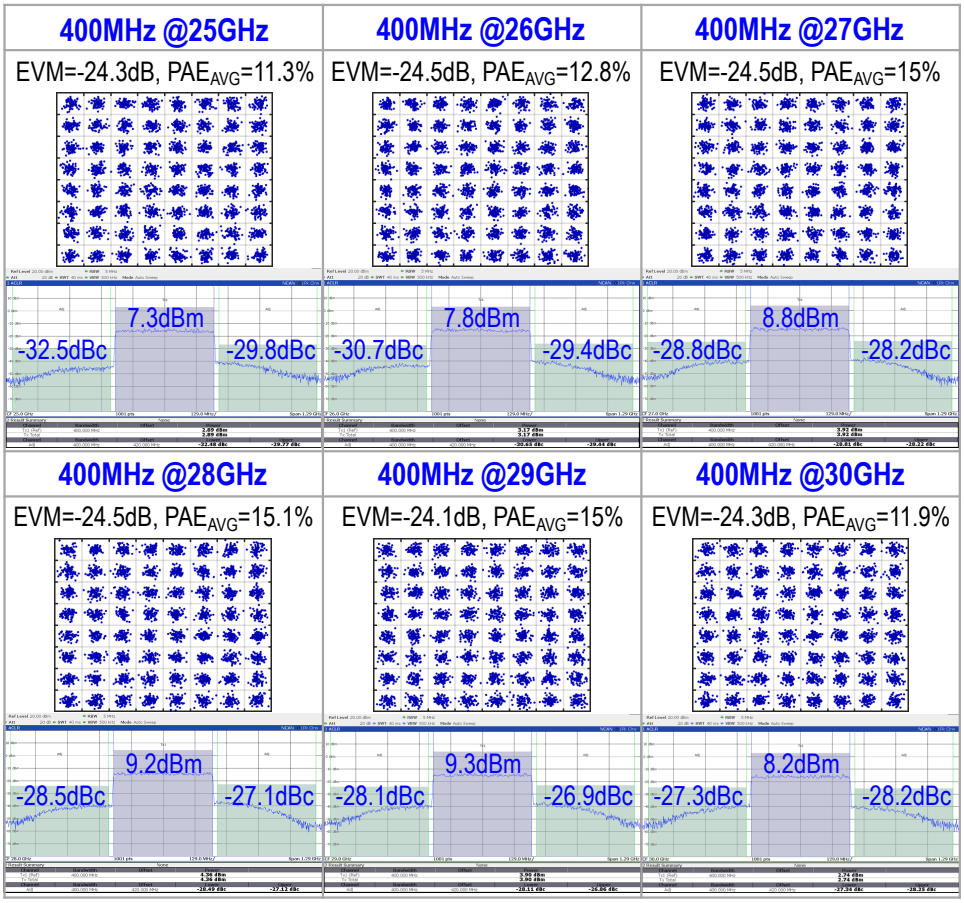


Figure 3.36: The measured constellations/spectrums for a "400MHz 64-QAM OFDM" signal at various frequencies.

the mm-wave 5G system. Fig. 3.36 shows the measured constellations and spectrums for a 400MHz signal with 9.3~10.1dB PAPR. At 27GHz, with 8.8dBm P_{AVG} and 15% PAE, PA achieves an EVM of -24.5dB and an ACLR of –28.8/-28.2dBc without DPD. As summarized in Fig. 3.37, over 25-to-30GHz carrier frequencies, the DPA supports a 400MHz 64-QAM OFDM signal with >7.3dBm P_{AVG} and >11.3% average PAE. Besides, Fig. 3.38 demonstrates the measured EVM/ACLRs versus P_{AVG} at 27GHz.

As discussed in Section II, the load modulation dramatically increases the maximum AM-AM/AM-PM deviations by modulating the Q of the passive network. To support the described analysis, in addition to the AM-AM/AM-PM results illustrated in Fig. 3.34, the AM-AM/AM-PM of the proposed PA (black) is reported for various frequencies employing a "50MHz 64-QAM OFDM" signal with 10~10.5dBm P_{AVG} (Fig. 3.39). Here, to elaborate more, the measured AM-AM/AM-PM performance of the proposed PA, which re-

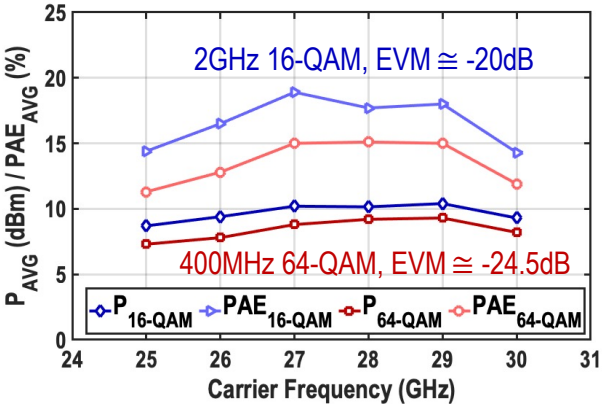


Figure 3.37: The measured average output power and PAE of 16-/64-QAM signals with ~10dB PAPR at -20/-24.5dB EVM versus carrier frequency.

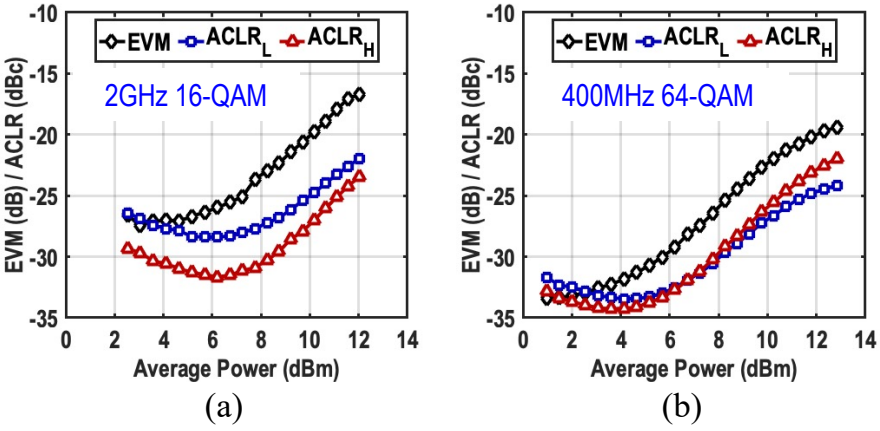


Figure 3.38: The measured EVM/ACLRs versus P_{AVG} at 27GHz for (a) a "2GHz 16-QAM OFDM" signal and (b) a "400MHz 64-QAM OFDM" signal.

configured (V_{det}=0.9V, see Fig. 3.25) to operate without efficiency enhancement (gray), is presented. In other words, the PA performance is measured when its auxiliary PA is always on, performing as a simple power combining without any load modulation.

As demonstrated in Fig. 3.39, the AM-PM deviation is as high as 23.6° at 25GHz, and it decreases while operating at the higher frequencies. On the other hand, the maximum AM-PM deviation of the SDPA without efficiency enhancement is -3~-5°, and relatively stable over the bandwidth of interest, thus confirming the load modulation impact on the linearity as analyzed earlier.

Furthermore, the measured AM-AM/AM-PM distortion of a 400MHz 64-QAM OFDM signal measured at 10~10.5dBm P_{AVG} at various carrier frequencies is presented in Fig. 3.40. Due to the memory effect, the measured AM-AM/AM-PM profiles are worse

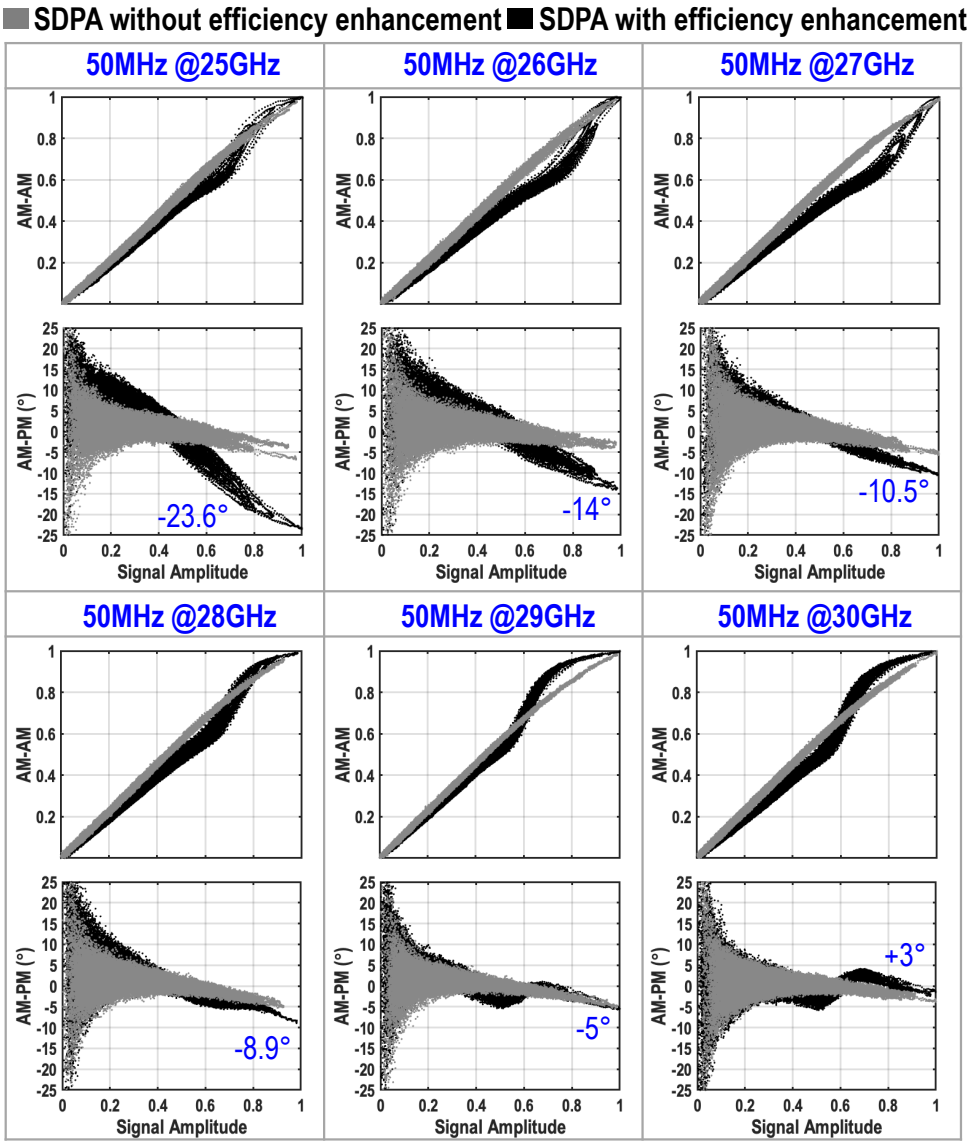


Figure 3.39: The measured AM-AM/AM-PM of the proposed SDPA with (V_{det}=0.37V) and without (V_{det}=0.9V) efficiency enhancement employing "50MHz 64-QAM OFDM" signals with 10~10.5dBm P_{AVG} and 8.6~9.4dB PAPR.

than the 50MHz 64-QAM OFDM signal. In this regard, the adaptive biasing limited bandwidth poses more time-related errors in the efficiency enhancement mode, leading to a more significant memory effect.

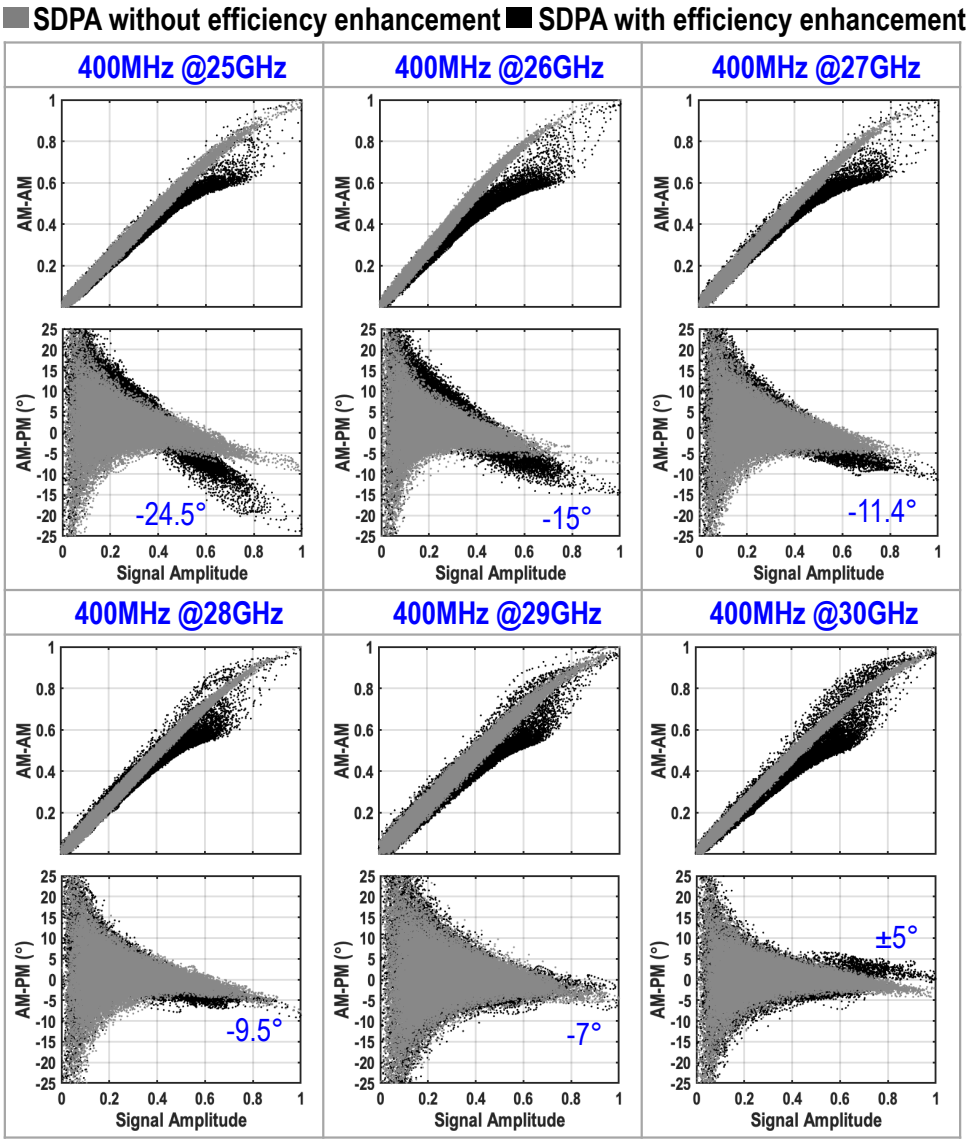


Figure 3.40: The measured AM-AM/AM-PM of the proposed SDPA with (V_{det}=0.37V) and without (V_{det}=0.9V) efficiency enhancement employing "400MHz 64-QAM OFDM" signals with 10~10.5dBm P_{AVG} and 9.3~11.1dB PAPR.

Fig. 3.41 shows the simulation results of ideal PAs AM-AM/AM-PM deviations using 3D EM models and compares them to the measured performance. As demonstrated, there is good agreement between simulation and measurement results, proofing that

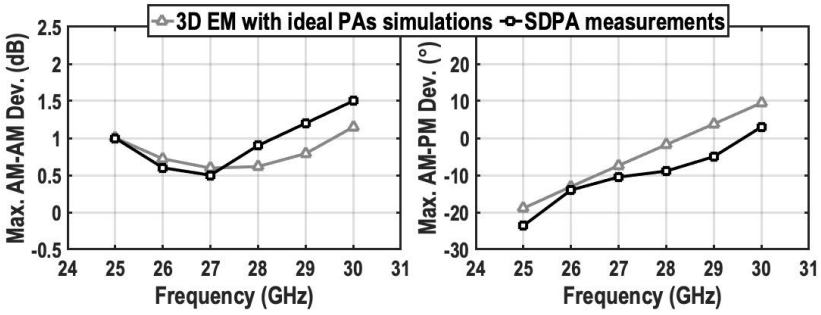


Figure 3.41: The measured maximum AM-AM/AM-PM deviations of the realized SDPA compared to its 3D EM simulations (Fig. 3.18).

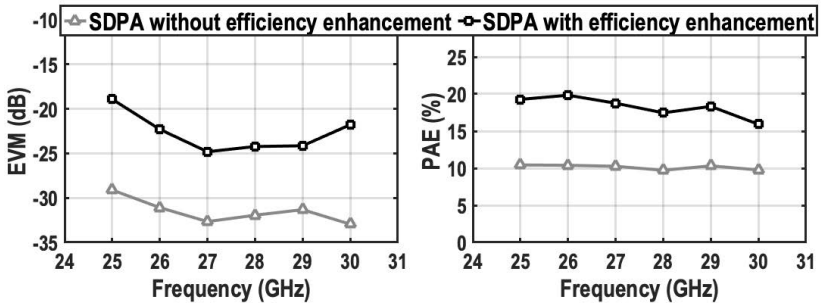


Figure 3.42: The measured EVM and average PAE (P_{AVG}=10~10.5dBm) of implemented SDPA with and without efficiency enhancement.

although the load modulation degrades the linearity performance, its behavior is predictable and stable.

Lastly, Fig. 3.42 depicts the measured EVM and average PAE of a "50MHz 64-QAM OFDM" signal for the realized SDPA with and without efficiency enhancement. It demonstrates almost ×2 average PAE improvement over the 5G band. This close-to-perfect broadband load modulation is the significant advantage of the proposed SDPA architecture. However, Fig. 3.42 also shows compromising the in-band linearity due to inherent AM-AM/AM-PM distortions of DPAs.

Table II summarizes the measured performance of the proposed SDPA and compares it to that of prior-art silicon-based mm-wave PAs. The realized SDPA satisfies the 5G requirements by providing >20dBm P_{SAT} with >36% PAE_{SAT} over the 24-to-30GHz band. It also provides 34% PAE at 6-dB PBO, the highest among mm-wave DPAs. Besides, considering the Doherty combiners typically occupy a large die area, the realized SDPA is reasonably compact, only larger than [54].

In [56] and [13], impressive broadband DPA architectures are presented, achieving PAE_{6dB} as high as 32.8%. However, their excellent performance occurs mostly at 30-to-38GHz, operating less efficiently at other prevailing mm-wave 5G bands (e.g., 24-to-30GHz and 37-to-43.5GHz). For instance, in [13], the $P_{SAT}/PAE_{SAT}/PAE_{6dB}$ at 29GHz

and 38GHz are 21.8dBm/33.1%/18.6% and 22.6dBm/30.6%/25.3%, respectively. Meanwhile, our proposed SDPA provides state-of-the-art efficiency enhancement over the 24-to-30GHz band (see Fig. 3.33).

3.7. CONCLUSION

This chapter introduces three significant contributions: (i) A two-step impedance inverting-based series-Doherty combiner is proposed featuring broadband load modulation, compact footprint, and a simple design structure without demanding advanced technology. Additionally, a step-by-step design framework is presented where all design parameters have been derived based on 5G specifications. (ii) We reveal the inherent linearity limitation of DPAs, namely AM-AM/AM-PM distortions, caused by Q modulation. We meticulously discussed and exhibited this phenomenon all the way from the basic ideal component modeling and post-layout 3D EM simulations up to the modulated signal measurements. (iii) A post-silicon inter-stage passive validation approach is presented to enhance prototype evaluation and address simulation shortcomings. It can also facilitate long-term operation monitoring.

The chip prototype is realized using 40nm bulk CMOS technology. The proposed SDPA achieves state-of-the-art performance over the 24-to-30GHz band. Overall, the experimental results have demonstrated an excellent agreement between our analysis, simulations, and measurement results.

Table 3.1: Silicon-Based mm-Wave PAs Performance Comparison

	Mm-Wave Doherty PAs									Mm-Wave LMBAs		Linear Mm-Wave PAs		
	This work			Wang ISSCC'19 [28]	Hu JSSC'19 [29]	Mannem JSSC'21 [34]	Huang ISSCC'21 [33]	Kim RFIC'21 [31]	Pashaeifar JSSC'21 [40]	Qunaj ISSCC'21 [21]	Chappidi IMS'20 [20]	Vigilante JSSC'18 [48]	Shakib ISSCC'17 [10]	Wang JSSC'21 [14]
Architecture	Two-step impedance inversion series-DPA			Mixed-signal DPA	Multiband DPA	Role-exchange DPA	Continuous Coupler DPA	Parallel-series DPA	Balanced series-DPA	Doherty-Like LMBA	LMBA	Transformer based network	Analog linear PA	Distributed Balun based PA
Technology	40nm CMOS			45nm SOI	130nm SiGe	45nm SOI	45nm SOI	28nm CMOS	40nm CMOS	28nm CMOS	65nm CMOS	28nm CMOS	40nm CMOS	45nm SOI
Supply (V)	1.8 (PA), 0.9 (DA)			2	1.5	2, 1	2, 1	1.8	1	1	1.1	0.9	1.1	2
Freq. (GHz)	24 to 32			27	28 to 42	26 to 60	26 to 60	24 to 30	24 to 30	36	26 to 40	29 to 57	27	25.8 to 43.4
Core area (mm^2)	0.37			0.52	1.76#	0.67	0.62	0.16	1.38	1.44#	1.47#	0.16	0.27	0.21
Gain (dB)	17.4 (27GHz)			19.1	18.2 (28GHz)	16*	15.5*	16.5	N/A	18	12.5*	20.8	22.4	20.5
P_{SAT} (dBm)	20.43			23.3	16.8	22.62 (32GHz)	22	18.8	NR	22.6	20	16.6	15.1	20.4 (28GHz)
P_{1dB} (dBm)	20.2			22.4	15.2	NR	21.5	17.5	20	19.6	NR	13.4	13.7	19.1
PAE_{SAT} (%)	38.2			40.1	20.3	41.9	40.5	30	NR	32	23.3	24.2	33.7	45
PAE_{1dB} (%)	39.1			39.4	19.5	NR	39.9	NR	39.8†	30.5	NR	12.6	NR	42.5
PAE_{6dB} (%)	34			33.1	13.9	31.5	32.8	22	31†	24.2	23.3‡	NR	15.1	
Modulation scheme	16-QAM OFDM	64-QAM OFDM	64-QAM OFDM	SC 64-QAM	SC 64-QAM (28GHz)	1-CC 64-QAM 5G NR FR2	1-CC 64-QAM 5G NR FR2	8-CC 64-QAM OFDM	8-CC 64-QAM OFDM	SC 64-QAM	SC 64-QAM	SC 64-QAM (34GHz)	8-CC 64-QAM OFDM	2-CC 64-QAM 5G NR FR2
Data rate (Gb/s)	2GHz	400MHz	100MHz	6	3	200MHz	200MHz	800MHz	800MHz	12	6	3	800MHz	800MHz
PAPR (dB)	9.6	9.7	8.6	6.5	6	9.64	9.64	10	10.8	≈6	NR	8.3	9.7	11.78
EVM_{rms} (dB)	-19.7	-24.5	-25.1	-25.3	-27**	-24	-25.4	-25	-27.1	-25	-27	-25	-25	-25.1
ACLR (dBc)	-24.7/-26.9	-28.8/-28.2	-36.3/-27.1	-29.6	-28.4	-28.8	-27/-25.8	-25.9	-33.4/-32.1	NR	-29	-30.2	-31/-29	-25.6
P_{avg} (dBm)	10.2	8.8	9.8	15.9	9.2	10.7	9.5	11.4	8.4	16	10.6	8.9	6.7	11.3
PAE_{avg} (%)	18.9	15	17.7	29.1 (27.6††)	18.5†	14.5	15.5	18.1	10.8†	22	12.1†	4.4	11	16.6

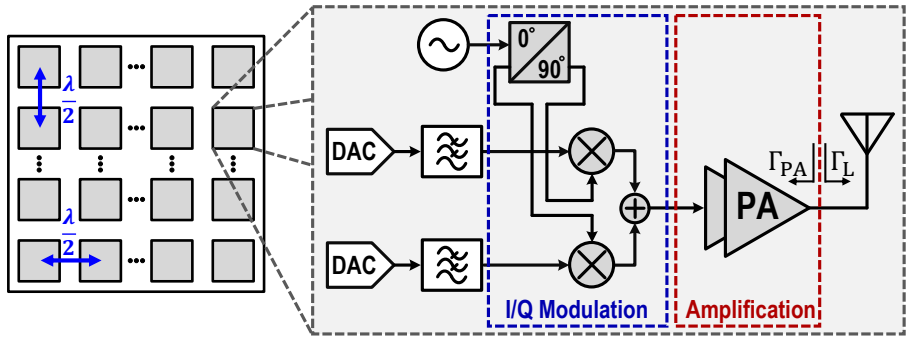
Chip area. *Graphically estimated. ‡Last stage drain efficiency at 4dB PBO. †Last stage drain efficiency **EVM normalized to peak signal. ††Efficiency with digital circuits.

4

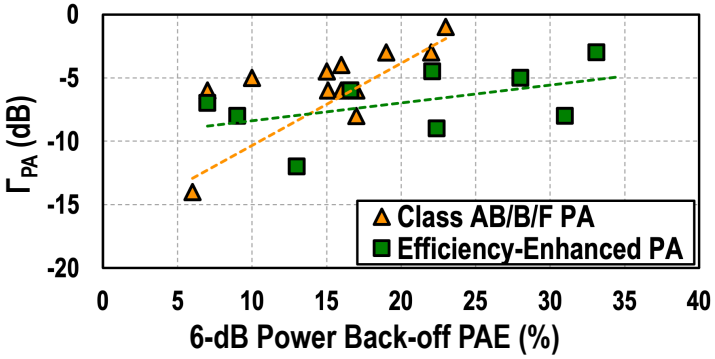
A MM-WAVE MUTUAL-COUPLING-RESILIENT DOUBLE-QUADRATURE TX

This chapter presents a wideband energy-efficient transmitter (TX) for 5G mm-wave phased-array systems. It features an advanced double-quadrature direct-upconverter to improve its in-band linearity and spectral purity. The proposed TX architecture incorporates an efficiency-enhanced balanced power amplifier (EEBPA) that mitigates VSWR fluctuations in phased-array systems while enhancing efficiency at power back-off (PBO). The EEBPA comprises two identical series-Doherty PAs combined through a quadrature hybrid coupler forming a balanced PA. The proposed double-quadrature direct-upconverter (DQ-DUC) consists of a pair of I/Q modulators and the proposed EEBPA's quadrature combiner to further suppress the I/Q image. To verify the proposed techniques, a 40-nm CMOS prototype is implemented. It delivers 20dBm P_{1dB} with 40%/31% drain efficiency at P_{1dB}/6-dB PBO. The measured TX output reflection coefficient is better than -18dB over a 22.5-to-30GHz band. Its intrinsic LO feedthrough and image-rejection ratio for a 100MHz tone-spacing over a 24-to-30GHz band are better than -45dBc/50dB, respectively, without calibration. The average error vector magnitude (EVM) is better than -27.1dB without digital pre-distortion for an 8-carrier "100MHz 64-QAM OFDM" signal with an 800MHz aggregated bandwidth while generating an average output power of 8.4dBm with 10.8% drain efficiency. Its maximum forward-power/EVM deviations are better than 0.3/3.9dB, respectively, for a "100MHz 64-QAM" signal under a voltage standing wave ratio of 3.

This chapter is based on the paper published in the IEEE Journal of Solid-State Circuits [88].



(a)



(b)

Figure 4.1: (a) A conventional Cartesian TX architecture employed in a digital-beamforming phased array system, and (b) recently published PA's output matching versus their 6-dB PBO PAEs.

4.1. INTRODUCTION

Mm-wave communication systems have been considered as key enablers for developing the fifth-generation (5G) of a mobile network offering high data throughput, low network latency, and improved link robustness [5, 7, 70, 71]. Taking advantage of mm-wave phased arrays empowers 5G communication systems to establish directional links with large bandwidth between the base station and user equipment. To realize such a high data-rate communication link, 5G transmitters (TXs) typically employ spectrally efficient complex modulation schemes with high peak-to-average power ratios (PAPRs) [4]. However, this feature entails operation at a power back-off (PBO), imposing stringent requirements on the TX modulation accuracy, spectral purity, and PBO efficiency.

Fig. 4.1(a) shows a conventional Cartesian TX architecture employed in a digital-beamforming phased-array system [92]. It comprises two distinct parts: (1) A wideband in-phase/quadrature (I/Q) modulator, which needs to provide low error vector magnitude (EVM) to facilitate multi-Gb/s high-order complex modulations, and; (2) A highly energy-efficient RF power amplifier (PA) to properly boost its radiated power, addressing the required link budget.

In this architecture, the I/Q modulators must exhibit minimal I/Q imbalance and LO feedthrough (LOFT) to yield low-EVM modulation [93]. These requirements are challenging when operating at the mm-wave bands due to employing relatively small transistors and passive components that are extremely sensitive to process, voltage, and temperature (PVT) variations [94]. A typical solution is adopting I/Q and LOFT calibrations that require complicated and exhaustive search methods [95–101]. Consequently, an I/Q TX architecture with inherently low I/Q imbalance and LOFT is highly desirable, especially in the context of the large-scale 5G mm-wave phased-array systems [11].

On the other hand, the 5G link budget demands 60dBm EIRP to cover a relatively short distance [4]. To generate such radiated power, considering 16×16 phased-array antennas, each single antenna element must radiate 12dBm average power. Consequently, assuming a single patch antenna with 5dBi antenna gain and 2dB connection loss, the average/peak TX power should exceed 9/20dBm for a modulated signal with an 11dB PAPR. Generating these power levels is challenging, especially in nanoscale bulk CMOS technology with limited supply voltage and operating frequency. Stacked-FET PAs and power combining TX architectures are widely used to generate more than 20dBm peak power [9, 47, 73–77, 102]. Additionally, efficiency enhancement techniques such as Doherty PAs and out-phasing TXs can simultaneously offer high output power and high average efficiency for modulation schemes with high PAPRs [12, 36, 37, 39, 48, 49, 51–53, 55, 56, 103–105].

Nevertheless, as depicted in Fig. 4.1(b), improving PBO efficiency exacerbates the PA's output reflection coefficient (Γ_{PA}), making them inevitably sensitive to the voltage standing wave ratio (VSWR) of the antenna and its connection. Additionally, Doherty PAs are more sensitive to the antenna VSWR due to the load modulation. Unfortunately, this becomes even worse in practical situations in which the mutual coupling among the closely spaced antennas yields a beam-steering angle-dependent and time-varying VSWR condition [19–23]. In other words, the unwanted element-to-element coupled signal reflects to the antenna, radiates alongside the desired signal, and subsequently deteriorates the phased-array beam pattern and TX linearity. A previously promoted solution for this antenna VSWR problem is load mismatch detection followed by tuning of the output matching network (self-healing) [106]. However, this technique requires a reconfigurable and inevitable lossy matching network. Furthermore, active load pulling [107] and using a reconfigurable series/parallel Doherty PA structure [104] are proposed to realize a VSWR resilient efficiency-enhanced TX. Nevertheless, all these techniques are only suitable when dealing with a known and stable antenna impedance mismatch, which is, unfortunately, not the case in practical situations.

A conventional solution for a VSWR resilient PA is employing an isolator at its output. Due to the area constraint of the phased-array transceivers, an integrated isolator would be a viable solution. However, the integrated state-of-the-art mm-waves circulators/isolators [64–66] occupy a large area (>1.3mm^2) compared to the designated area of the whole transceiver[11]. Moreover, they demonstrate high TX-to-antenna loss (>3.2dB) and require extra power consumption to generate their quadrature clocks. Balanced power amplifiers (BPAs) have recently been used at mm-wave to mitigate VSWR conditions but still suffer from low PBO drain efficiency [67, 68].

In [57], we recently proposed a TX architecture with an efficiency-enhanced bal-

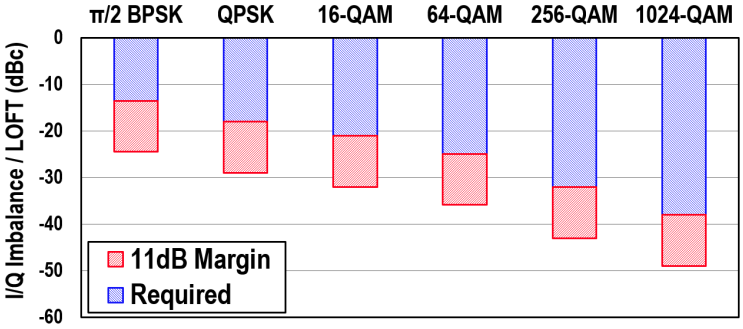


Figure 4.2: The required LOFT and I/Q imbalance for various modulation schemes considering 11dB margin.

anced PA (EEBPA) combiner. It consists of two identical series-Doherty PAs combined through a quadrature hybrid coupler, forming a balanced PA. The quadrature combiner has three crucial roles in this architecture: (1) Combine the output of two Doherty PAs to achieve the desired output power; (2) Suppress output injected wave, resulting from mutual-coupling, by offering close to perfect matching conditions; (3) Act as a second image-rejection stage and provide a calibration-free low I/Q imbalance modulation.

This chapter investigates the architectural analysis and elaborates on the system- and circuit-level design considerations and extensive measurement results. It is organized as follows. Section 4.2 presents the proposed double-quadrature direct-upconversion TX architecture and investigates its performance under process variation. The EEBPA is presented in Section 4.3. Circuit implementation details of the proposed TX are described in Section 4.4. Section 4.5 presents the measurement results, and Section 4.6 concludes the chapter.

4.2. DOUBLE-QUADRATURE I/Q MODULATOR

5G communication systems employ spectrally efficient modulation schemes such as 64-QAM and 256-QAM signals. Exploiting these complex modulated signals entails meeting stringent TX in-band linearity requirements verified by EVM, which comprises quantization noise, phase noise, I/Q modulation imbalance, LOFT, and the PA non-linearity [4, 94]. Fig. 4.2 shows the required LOFT and I/Q imbalance for various modulation schemes, assuming an ideal condition for the remaining EVM contributors. The required I/Q imbalance/LOFT for 64-QAM and 256-QAM are -24.9dBc and -32.1dBc, respectively. Therefore, the design specs are defined considering an 11dB margin to include the non-ideality effect of the remaining EVM contributors. However, achieving a better than 11dB margin will relax the required specs of the other parts of the system, such as PA and PLL, resulting in better system efficiency. Consequently, the first design challenge is obtaining calibration-free I/Q imbalance/LOFT <-43.1dBc and eventually diminishing the I/Q imbalanced performance even further.

A conventional approach for generating highly accurate quadrature LO signals seamlessly operating in the 24-to-30GHz 5G mm-wave band comprises a multi-stage RC polyphase filter (PPF) [108]. Although this approach has a small footprint, it is suscepti-

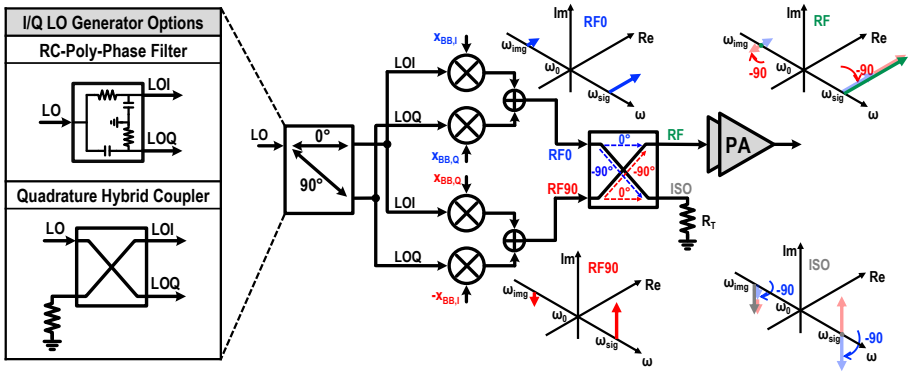


Figure 4.3: The double-quadrature direct-upconverter concept. The LO generator could be either an RC poly-phase filter or a quadrature hybrid coupler.

ble to inductive/capacitive parasitics and temperature variations [94]. Recently, multi-stage transformer-based quadrature hybrid couplers (QHCs) are widely used at mm-wave bands with reasonable die-area [109, 110]. However, even though the quadrature accuracy of the LO signals was close to a perfect condition, the interconnect parasitics and device mismatch significantly degrade the I/Q modulator's performance at the designated mm-wave band. Thus, employing I/Q calibration is inevitable, which increases the system complexity. Additionally, large-scale digital/hybrid beamforming phased-array systems demand high yield and minimal system complexity [11].

Double-quadrature receiver architectures are a well-known structure to mitigate IRR [111], commonly used in two-step down-conversion topologies [112, 113]. In this section, we first present the direct double-quadrature upconversion concept. Afterward, by employing Monte Carlo (MC) simulations, the yield of the proposed architecture will be investigated.

4.2.1. DOUBLE-QUADRATURE DIRECT-UPCONVERSION CONCEPT

Fig. 4.3 conceptually illustrates a double-quadrature direct upconverter (DQ-DUC). The DQ-DUC comprises an I/Q modulator, acting as the first image-reject filter, and a quadrature combiner, operating as the second image-reject filter. The I/Q modulator consists of an I/Q LO generator, either a PPF or a QHC, followed by a pair of I/Q mixers whose baseband inputs of the bottom I/Q mixer are swapped while its in-phase signal, $x_{BB,I}$, is negated. As a result, the desired signals' phase excursion at the output of these mixers is +90° out of phase while their image signals have a phase difference of -90°(see Fig. 4.3).

Subsequently, by employing an isolated quadrature combiner, e.g., a QHC, with a constant -90° phase shift, the desired signals are constructively combined at the output port, whereas the image signals are canceled (see Fig. 4.3). The opposite operation occurs at the isolation port. The mathematical relationship is derived in Appendix A.

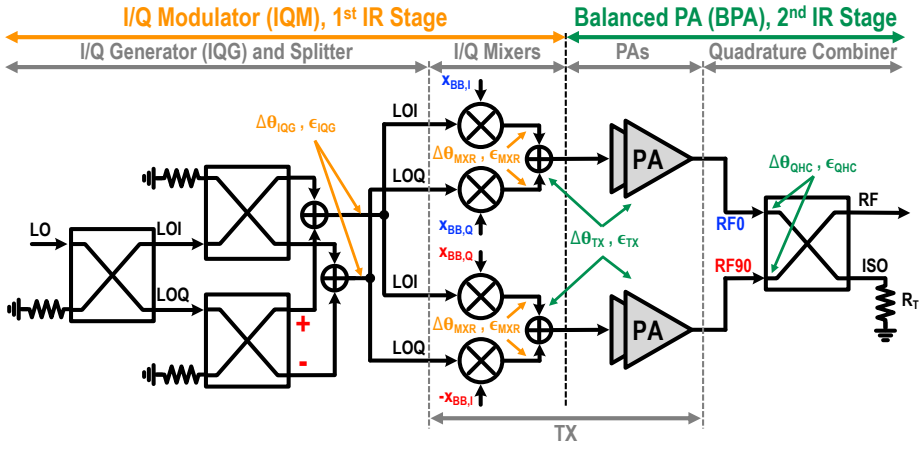


Figure 4.4: The proposed double-quadrature direct upconverter with two-stage I/Q LO generator. The contribution of each part in IRR has been shown.

4.2.2. DOUBLE-QUADRATURE DIRECT-UPCONVERSION TX ARCHITECTURE

The proposed TX architecture is depicted in Fig. 3. A two-stage transformer-based QHC is employed as an I/Q generator (IQG) to minimize I/Q imbalance and widen operational frequency [110]. The output QHC and its following PA (see Fig. 4.3) are swapped to establish a balanced power amplifier (BPA). The motivation for this PA structure will be further explained in Section III. The image-rejection ratio (IRR) of the I/Q modulator (IRR_{IQM}), which is the first image rejection stage, is determined by the amplitude and phase inaccuracy of IQG (ϵ_{IQG},$\Delta\theta_{IQG}$) and I/Q mixers (ϵ_{MXR},$\Delta\theta_{MXR}$)

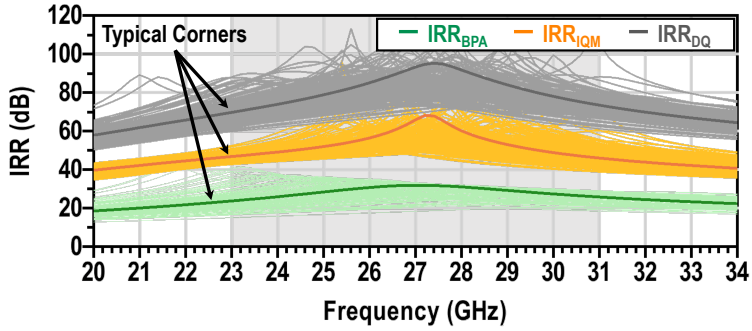
$$IRR_{IQM} = f\left(\epsilon_{IQG},\epsilon_{MXR},\Delta\theta_{IQG},\Delta\theta_{MXR}\right) \tag{4.1}$$

It is worth mentioning that the device and interconnection mismatch of mm-wave I/Q mixers play an equally important role as that of the LO I/Q imbalance [94]. Nevertheless, increasing the IQG's number of cascaded stages does not necessarily improve the IRR_{IQM}, which is already constrained by mixers' mismatches. Fig. 4.5(a) shows the IRR_{IQM} based on 200 MC simulations where the active parts are modeled as ideal components with their relative mismatches to speed up simulation time. Additionally, the mismatch of all passive components, such as capacitors and resistors, are considered in these simulations.

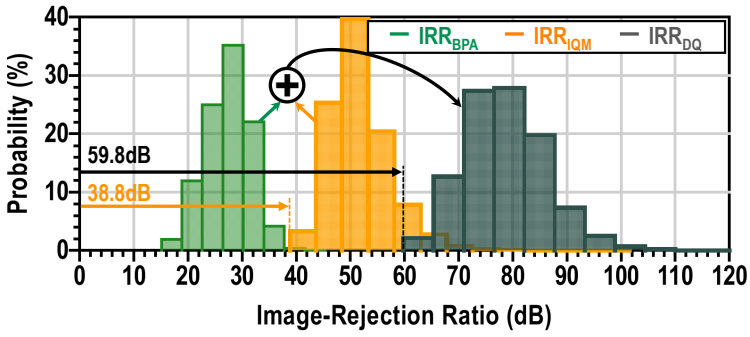
The IRR of the balanced PA (IRR_{BPA}), the second IR stage, can be calculated by mismatches of top and bottom TX paths (ϵ_{TX},$\Delta\theta_{TX}$), and I/Q imbalance of QHC (ϵ_{BPA},$\Delta\theta_{BPA}$).

$$IRR_{IQM} = f\left(\epsilon_{TX},\epsilon_{BPA},\Delta\theta_{TX},\Delta\theta_{BPA}\right) \tag{4.2}$$

The MC simulation results for IRR_{BPA} and overall IRR (IRR_{DQ}) are shown in Fig. 4.5 and can be expressed as



(a)



(b)

Figure 4.5: (a) IRR of I/Q modulator, BPA, and overall TX over 200 trails of an MC simulation. (b) IRR resulted from an MC at the 23-to-31GHz band. The overall IRR is always higher than 59.8dB.

$$IRR_{DQ} = IRR_{IQM} \times IRR_{BPA} \tag{4.3}$$

According to (4.1) and (4.2), the IRR_{IQM} and IRR_{BPA} are uncorrelated. Consequently, although they might not individually meet the aimed mismatch performance, their combined performances satisfy the overall designated IRR. Therefore, the proposed approach relaxes the mismatch requirement and makes this architecture less sensitive to PVT variations than a conventional structure for the same overall targeted IRR.

4.3. EFFICIENCY-ENHANCED BALANCED PAS

In a phased-array TX front-end, two impedance mismatch mechanisms affect the PA/TX performance: 1) antenna impedance mismatch and 2) mutual coupling. Fig. 4.6(a) illustrates the forward and reverse waves of the PA and its antenna. In this context, the antenna impedance mismatch, including its transmission line connector, is modeled as a two-port passive component that indicates the antenna is considered a perfectly matched port. As depicted in Fig. 4.6(b), alongside the PA represented as a Norton equivalent source, we have also modeled the mutual-coupling signal as a secondary power source at the antenna port. Since the mutual-coupling signal is correlated to the PA sig-

nal and the antenna is considered as an ideal port, the antenna's forward voltages can be expressed as

$$a_2 = S_{MC} a_1 \tag{4.4}$$

where a_1 is PA's forward signal when a_2=0 and S_{MC} is a time-varying element-to-element coupling coefficient, depending on the beam-steering angle.

The reverse waves and impedances seen by the PA are shown in Fig. 4.6(c) for three different cases: 1) Only antenna impedance mismatch, 2) only mutual-coupling signal, and 3) antenna impedance mismatch and mutual-coupling signal. In a large-scale phased-array TX with narrow beamwidth capability, the radiated signal robustness of each antenna element is essential for beamforming accuracy. This indicates that the radiated signal, i.e., b_2, must stay relatively stable during beamforming, as shown in Fig. 4.6. However, in the presence of the mutual coupling alongside the desired signal, S_{MC} a_1, the time-varying reflected mutual-coupling signal, i.e., $(S_{22} + S_{12}S_{21}\Gamma_{PA})S_{MC}a_1$, is radiated, deteriorating the beam pattern. Therefore, S_{22} and Γ_{PA} must be relatively small.

On the other hand, although the efficiency and overall TX performance benefit from small S_{11}/S_{22}, small Γ_{PA} leads to low PA efficiency (see Fig. 4.1(b)). Thus, our motivation is to design a PA structure with high efficiency and relatively low Γ_{PA}. Moreover, as illustrated in the last column of Fig. 4.6(c), when a PA experiences a large VSWR condition, its stability, efficiency, and output power deteriorate significantly. This section presents the proposed VSWR resilient efficiency-enhanced balanced PA for mm-wave phased-array systems.

4.3.1. THE PROPOSED EFFICIENCY-ENHANCED BALANCED PA

As depicted in Fig. 4.7, the proposed efficiency-enhanced balanced PA (EEBPA) consists of two identical efficiency-enhanced PAs (EEPAs) combined through a quadrature hybrid coupler. The PAs can be Doherty, out-phasing, or any other efficiency-enhanced structure. In the proposed PA architecture, the EEPAs perform PBO efficiency enhancement, whereas the balanced PA combiner provides VSWR resilience. To validate the proposed PA's output matching, as mentioned before, we modeled the mutual-coupling signal as a power source at the antenna port. As illustrated in Fig. 4.8(a), the unwanted coupled signal, i.e., "a_{MC}", is split by the hybrid coupler reflected from PAs, constructively added at the isolation port, and eventually absorbed in the 50Ω termination. However, the reflected waves are canceled at the antenna port. Consequently, the "Γ_{BPA}" is zero if the EEPAs are identical ($\Gamma_{PA1} = \Gamma_{PA2}$), and the hybrid coupler is an ideally symmetric structure.

Assuming two identical PAs, Fig. 4.8(b) depicts the forward and reflected waves of each PA in the steady state. The PAs' forward wave consists of two parts. The first part is the desired signals with 90° out of phase ($\frac{a_{PA}}{\sqrt{2}}$ and $\frac{ja_{PA}}{\sqrt{2}}$) that are eventually combined at the output port (a_{PA}). However, due to antenna impedance mismatch, part of the desired signal reflects ($\Gamma_{ant.}a_{PA}$). The hybrid coupler splits this reflected signal into two waves ($\Gamma_{ant.}a_{PA} \Rightarrow \frac{\Gamma_{ant.}a_{PA}}{\sqrt{2}}$ and $\frac{-j\Gamma_{ant.}a_{PA}}{\sqrt{2}}$), and then they proceed to the PAs' ports. Note that Γ_{PA} and $\Gamma_{ant.}$ are the reflection coefficients of the PAs and the antenna, respectively.

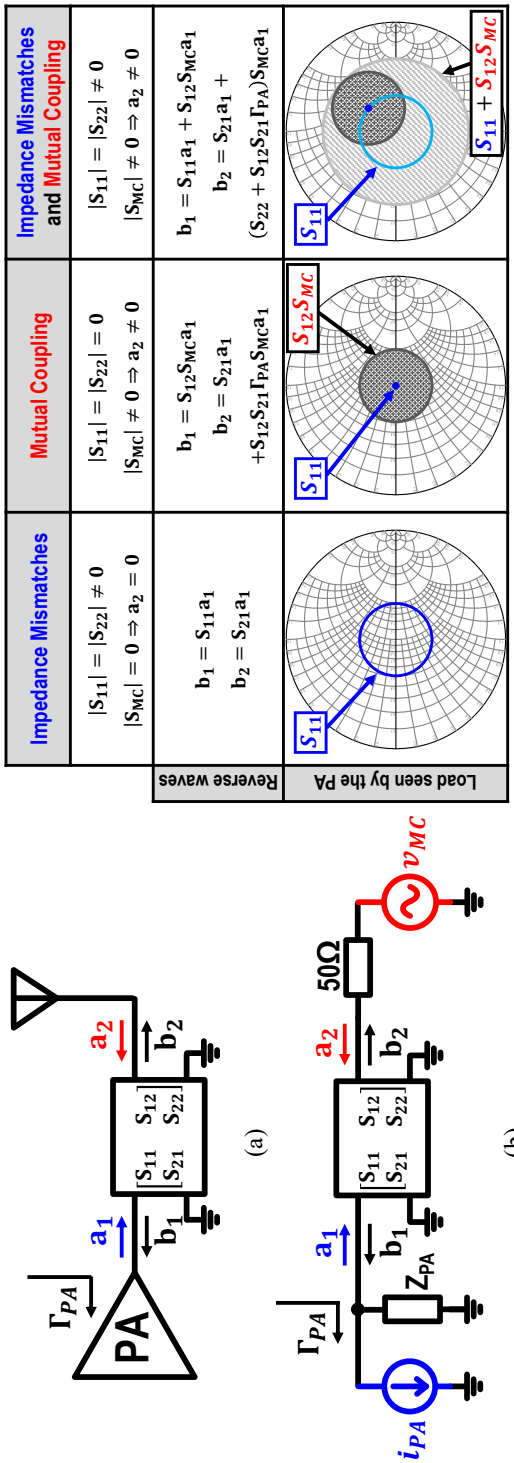


Figure 4.6: (a) Forward and reverse waves of the PA and antenna, where the connection and antenna mismatches are modeled using a two-port symmetric passive component. (b) A Norton model represents PA, whereas the mutual-coupling signal is modeled as a secondary power source at the antenna. (c) The reverse waves and impedances seen by PA for three cases are 1) only antenna impedance mismatches, 2) only mutual-coupling signals, and 3) antenna impedance mismatches and mutual-coupling signals.

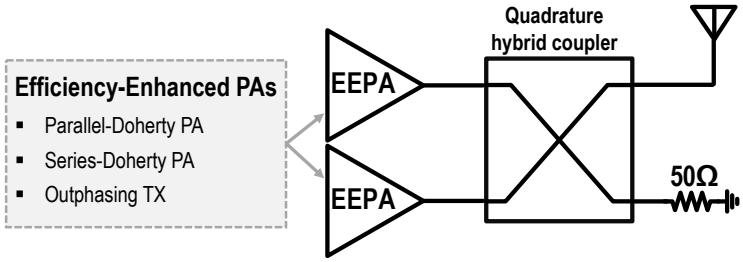


Figure 4.7: The proposed efficiency-enhanced balanced PA structure.

On the other hand, the second part of PAs' forward signals are proportional to the antenna mismatch that are reflected from the PAs ($\frac{\Gamma_{PA}\Gamma_{ant.}a_{PA}}{\sqrt{2}}$ and $\frac{-j\Gamma_{PA}\Gamma_{ant.}a_{PA}}{\sqrt{2}}$). Since the signals are -90° out of phase, they are combined and absorbed at the termination port, as in the case of the mutual coupling scenario. Hence, the load seen by each PA can be calculated as

$$\Gamma_{L1} = \frac{\Gamma_{ant.}\frac{a_{PA}}{\sqrt{2}}}{\frac{a_{PA}}{\sqrt{2}} + \Gamma_{PA}\Gamma_{ant.}\frac{a_{PA}}{\sqrt{2}}} = \frac{\Gamma_{ant.}}{1+\Gamma_{PA}\Gamma_{ant.}} \rightarrow Z_{L1} = \frac{1+\Gamma_{L1}}{1-\Gamma_{L1}}Z_0 = \frac{1+\Gamma_{PA}\Gamma_{ant.}+\Gamma_{ant.}}{1+\Gamma_{PA}\Gamma_{ant.}-\Gamma_{ant.}}Z_0, \tag{4.5}$$

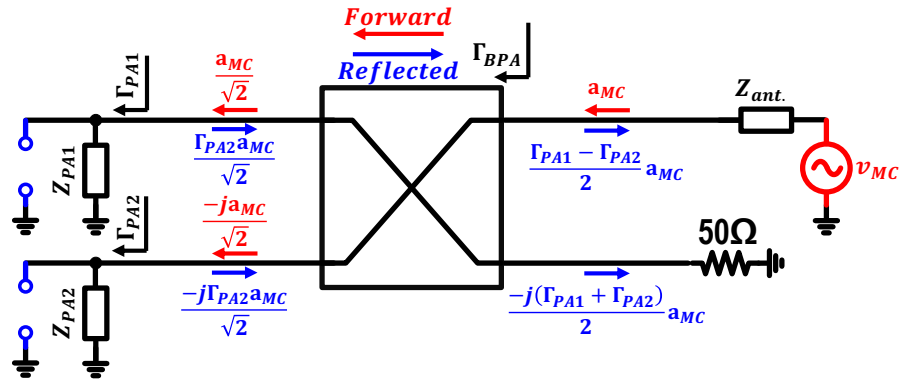
$$\Gamma_{L2} = \frac{\Gamma_{ant.}\frac{-ja_{PA}}{\sqrt{2}}}{\frac{ja_{PA}}{\sqrt{2}} + \Gamma_{PA}\Gamma_{ant.}\frac{-ja_{PA}}{\sqrt{2}}} = \frac{-\Gamma_{ant.}}{1-\Gamma_{PA}\Gamma_{ant.}} \rightarrow Z_{L2} = \frac{1+\Gamma_{L2}}{1-\Gamma_{L2}}Z_0 = \frac{1-\Gamma_{PA}\Gamma_{ant.}-\Gamma_{ant.}}{1-\Gamma_{PA}\Gamma_{ant.}+\Gamma_{ant.}}Z_0. \tag{4.6}$$

As a result, the forward wave of the balanced amplifier is always constant (i.e., a_{PA}, depicted in Fig. 4.8(b)), independent of the antenna's and PAs' impedances. Besides, the delivered power to the antenna is determined by the antenna mismatch loss ($1-|\Gamma_{ant.}|^2$). This, in turn, degrades the drain efficiency. Nevertheless, the unmatched loading condition can further degrade the delivered power and efficiency in the large-signal operation, where a large impedance leads to an early power saturation condition for the PAs. The Z-parameter analysis of the balanced amplifier is presented in Appendix B.

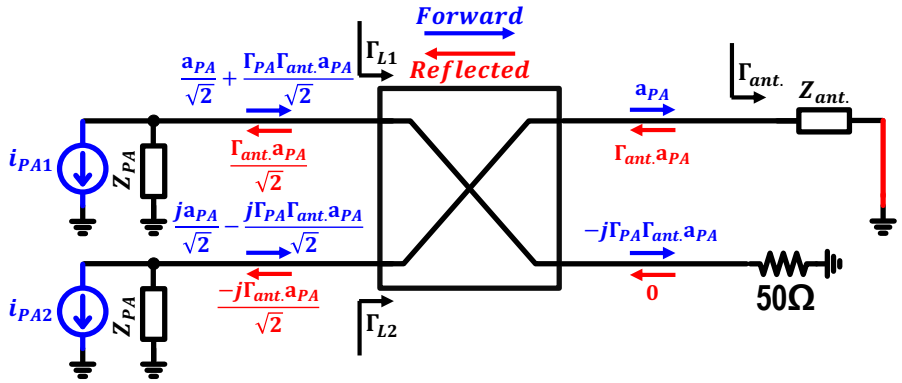
For further elaboration, we assume two extreme cases: 1) the PAs are impedance matched to the characterization impedance of hybrid coupler ($Z_{PA}=Z_0 \Rightarrow \Gamma_{PA}=0$), and 2) the PAs are ideal current sources ($Z_{PA}=\infty \Rightarrow \Gamma_{PA}=1$).

1) $\Gamma_{PA}=0$: In this case, $\Gamma_{L1}=\Gamma_{ant.}$ and $\Gamma_{L2}=-\Gamma_{ant.}$. It means one of the PAs drives $Z_{ant.}$, while the other one drives $\frac{Z_0^2}{Z_{ant.}}$. This balanced loading condition makes the proposed EEBPA relatively robust against VSWR in large-signal operations where only one of the PAs can be saturated by the large load impedance.

2) $\Gamma_{PA}=1$: In this case, which is a more practical assumption, $\Gamma_{L1}=\frac{\Gamma_{ant.}}{1+\Gamma_{ant.}}$ and $\Gamma_{L2}=\frac{-\Gamma_{ant.}}{1-\Gamma_{ant.}}$, which means $Z_{L1}=(1+2\Gamma_{ant.})Z_0$ and $Z_{L2}=(1-2\Gamma_{ant.})Z_0$. Even though the reflection coefficients are not equal in magnitude, they are still in opposite signs. Hence, the magnitude of the impedance seen by one of the PAs is always equal to or larger than $\sqrt{1+|2\Gamma_{ant.}|^2}Z_0$. Likewise, the other load impedance is equal to or smaller



(a)



(b)

Figure 4.8: Forward and reflected waves in (a) mutual-coupling, and (b) TX scenarios.

than $\sqrt{1+|2\Gamma_{ant.}|^2}Z_0$.

In summary, operating in power back-off, the proposed EEBPA offers a close-to-perfect termination for an impedance mismatch caused by a mutual-coupling signal. Moreover, it limits the delivered power degradation to mismatch losses presented by static antenna mismatch. Furthermore, the analysis shows that even in the near power saturation operation, by providing a balanced loading condition, the proposed structure diminishes forward power deviation, delivered power loss, and efficiency degradation in both mutual-coupling and impedance mismatch scenarios [114].

In terms of stability, according to (4.5) and (4.6), if $|\Gamma_{ant.}| > |1 \pm \Gamma_{PA}\Gamma_{ant.}|$, one of the PAs' load impedances is negative, which may lead to an unstable state. In the extreme case of $\Gamma_{PA} = 1$, this undesired condition is occurred if $|\mathscr{R}e(\Gamma_{ant.})| > 0.5$. Nevertheless, in practice, the $|\Gamma_{PA}| < 1$ and the loss of quadrature hybrid coupler reduce the risk of a negative load impedance.

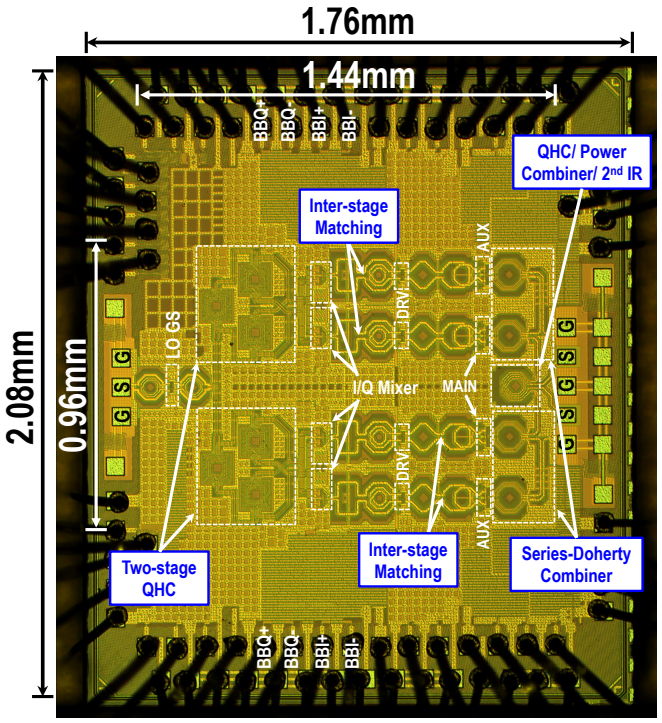


Figure 4.9: Die micrograph of the proposed TX.

4.3.2. SERIES-DOHERTY BALANCED PA

To realize the efficiency-enhanced PA, we chose a Doherty PA. The most common structure is a parallel-Doherty PA, which has frequency-dependent output power [115], making it less suitable for broadband operation. Consequently, in this work, a series-Doherty PA structure is selected. Compared to the parallel configuration, the series-Doherty PA ideally provides a frequency-independent output power, as well as lower impedances to its PAs, features that are highly desirable to obtain sufficient output power from a CMOS technology with a low breakdown voltage [56].

4.4. CIRCUIT IMPLEMENTATION

The proposed double-quadrature direct-upconversion TX is implemented in 40nm bulk CMOS technology. The chip occupies an area of 2.08mm × 1.76mm, while its core area is 0.96mm × 1.44mm (see Fig. 4.9). Fig. 4.10 exhibits a detailed schematic of the overall TX architecture. It consists of four sub-TXs; each comprises a double-balanced I/Q active mixer, a pre-driver (DRV), and a PA. Each pair of sub-TXs is connected to a series-Doherty power combiner. Subsequently, their outputs are combined with a 50Ω quadrature hybrid coupler (QHC) to realize the overall balanced PA while simultaneously acting as a second image rejection stage of the DQ-DUC. Moreover, a two-stage transformer-based quadrature hybrid coupler is adopted [110] to increase the TX operational fre-

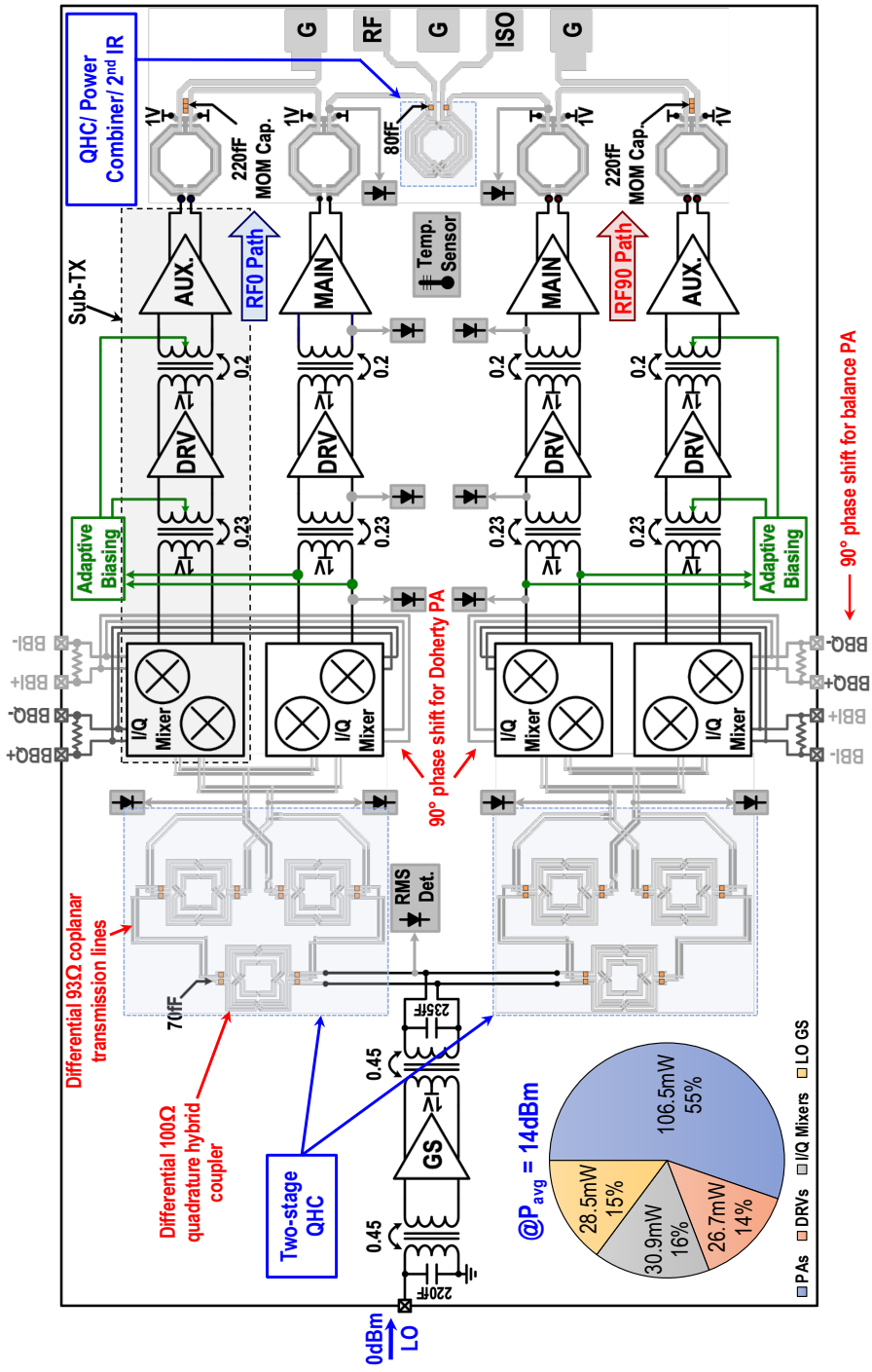


Figure 4.10: A detailed schematic of overall TX architecture.

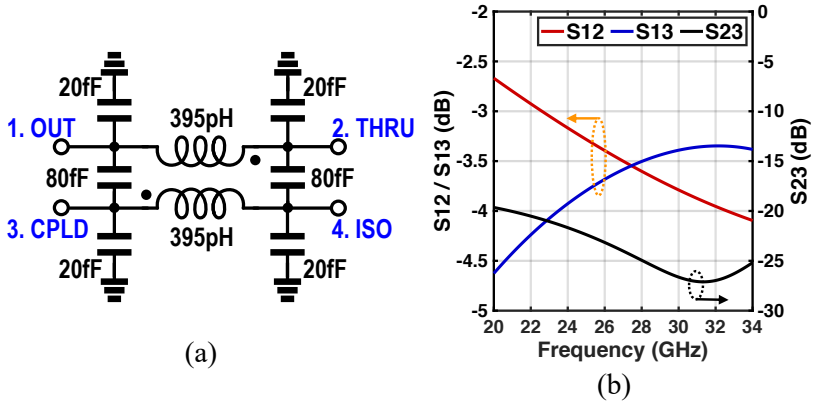


Figure 4.11: (a) The schematic of the output QHC, and b) its S-parameter simulation results.

quency. Since the I/Q generator should provide I/Q LO signals for four sub-TXs, to avoid a 1-to-4 power splitter, two identical two-stage QHCs have been implemented. Note that the I/Q generator's ports are directly connected to the I/Q mixers without employing any termination to increase voltage gain and diminish the circuit complexity [110]. Moreover, an LO gain-stage (GS) is employed to bring the external LO signal's level (0dBm) to the required level.

The measured power consumption of each part is summarized in Fig. 4.10 when the TX average output power is 14dBm at 27GHz. The PAs and their pre-drivers consume 133mW, i.e., 69% of the total power, while delivering 25mW to the load. Moreover, the active mixers and LO gain-stage dissipate 30.9mW and 28.5mW, respectively. Namely, the power consumption of each mixer is 7.7mW.

Fig. 4.11 shows the schematic and S-parameter simulation results of the output QHC. Its insertion loss is 0.55dB, whereas providing more than 22dB isolation between two PAs. Furthermore, the series-Doherty PAs are connected to QHC by two 50Ω coplanar transmission lines that add an extra 0.25dB loss. Fig. 4.12 illustrates the layout and schematic of the series-Doherty combiner. A two-step transformer-based impedance inverter is implemented in the auxiliary path of the proposed series-Doherty combiner to perform load modulation. The combiner consists of two identical transformers connected by a lumped-element transmission line providing a 50° phase shift. The capacitors at the primary side of transformers are absorbed in the parasitic capacitors of the PAs. Therefore, only a 220fF capacitor is placed at the secondary side of the auxiliary transformer. Compared to a conventional single C-L-C π-network, a two-step transmission line offers lower loss and broader bandwidth. It is worth mentioning that the metal slotting technique [116] is employed to increase the quality factor (Q) of the transformer due to reducing the skin effect (see Fig. 4.12(a)). Additionally, the secondary (sec.) is placed between the two slots of the primary (prim.) to boost the coupling factor.

In each Doherty branch, the PA, pre-driver, I/Q mixer, inter-stage matching networks, and most of their biases are the same for main and auxiliary paths. However, in the auxiliary path, the pre-driver and PA biases are modulated by the adaptive bias-

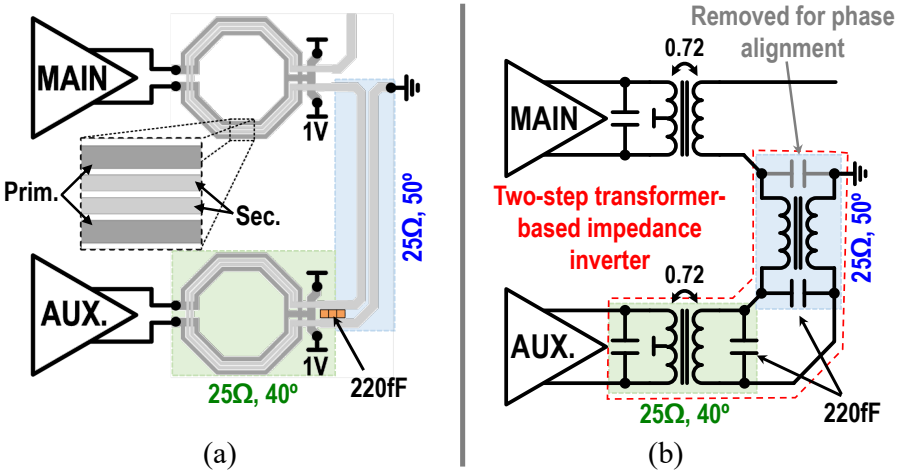


Figure 4.12: (a) The layout, and (b) schematic of the proposed series-Doherty combiner with the two-step transformer-based impedance inverter.

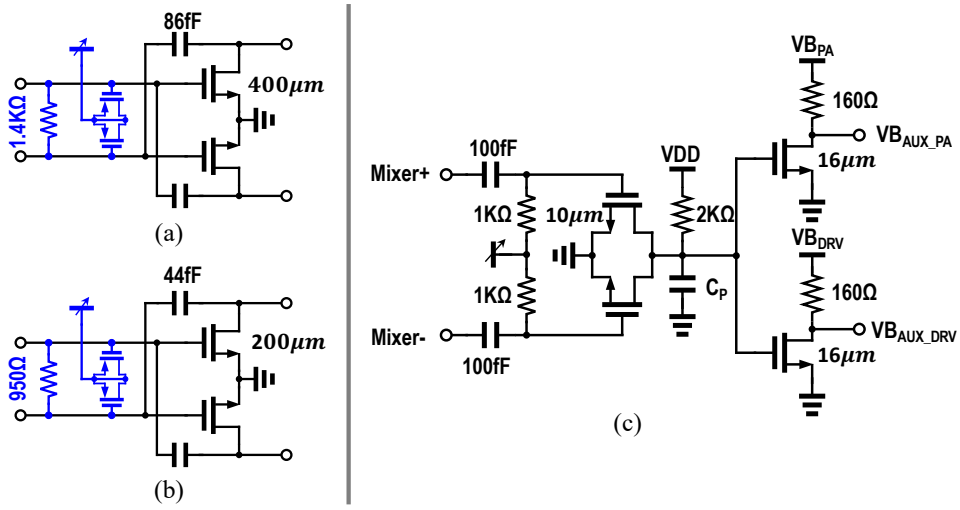


Figure 4.13: The schematic of (a) the PA, (b) pre-driver, and (c) adaptive-biasing circuit.

ing circuit to perform the Doherty operation. Fig. 4.13 depicts the detailed schematic of PA, pre-driver, and adaptive biasing circuitry [12]. A push-pull common-source amplifier with a cross-coupled drain-gate feedback capacitor is exploited to improve stability and reverse isolation. Each transistor consists of eight unit cells with a transistor aspect ratio of 50μm/40nm, which are optimized to mitigate the impact of device parasitics and interconnections [78]. The pre-driver employed the same structure comprising four unit cells (overall W/L=200μm/40nm). Besides, two varactors are utilized at the pre-driver and PA inputs to improve their AM-PM profiles and tune the inter-stage matching

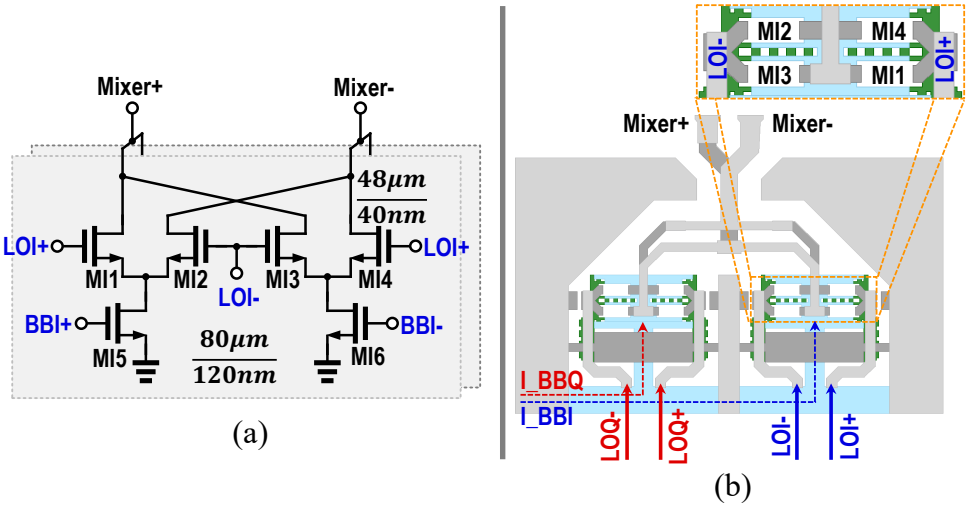


Figure 4.14: (a) The schematic and (b) simplified layout of the implemented double-balanced I/Q active mixer.

network [85]. Double-tuned transformers are implemented as the inter-stage matching network. Moreover, the PA/pre-driver transistors contain parasitic capacitors with a relatively high-quality factor (Q), indicating the real part of the input impedance of the PA/pre-driver is large. Therefore, a parallel resistor is employed at the input of the PA/pre-driver to increase the operational bandwidth and reduce passive loss by lowering the Q of the resonator.

A double-balanced I/Q active mixer is exploited to realize an I/Q modulator with high conversion gain and decent LO leakage performance. Fig. 4.14 shows the schematic and simplified layout of the I/Q mixer. The baseband transistors are chosen large enough to minimize LOFT. As mentioned before, at mm-wave frequencies, to achieve minimum I/Q imbalance and LOFT, the layout symmetry plays a crucial role. As depicted in Fig. 4.14(b), the I and Q paths are laid out symmetrically. The baseband signals are shielded to minimize mixers' undesired inter-modulation spurs.

Embedded voltage root mean square (RMS) detectors are utilized to monitor all signal levels of the proposed transmitter chain from the outputs of the LO gain stage to the PAs' outputs, represented by the diodes in Fig. 4.10. Wideband RMS detectors, comprising gate-drain connected NMOS transistors biased in the sub-threshold region, are adopted [86]. A temperature sensor, i.e., a diode-connected bipolar transistor, is employed to measure the chip temperature and calibrate the RMS detectors.

4.5. MEASUREMENT RESULTS

All measurements are performed using a high-frequency probe station. The low-frequency pads, including the I/Q baseband signals and DC bias voltages, are wire-bonded directly to an FR4 printed circuit board (PCB). The high-frequency ports comprising the input LO signal and the PA output ports, including the RF and isolation

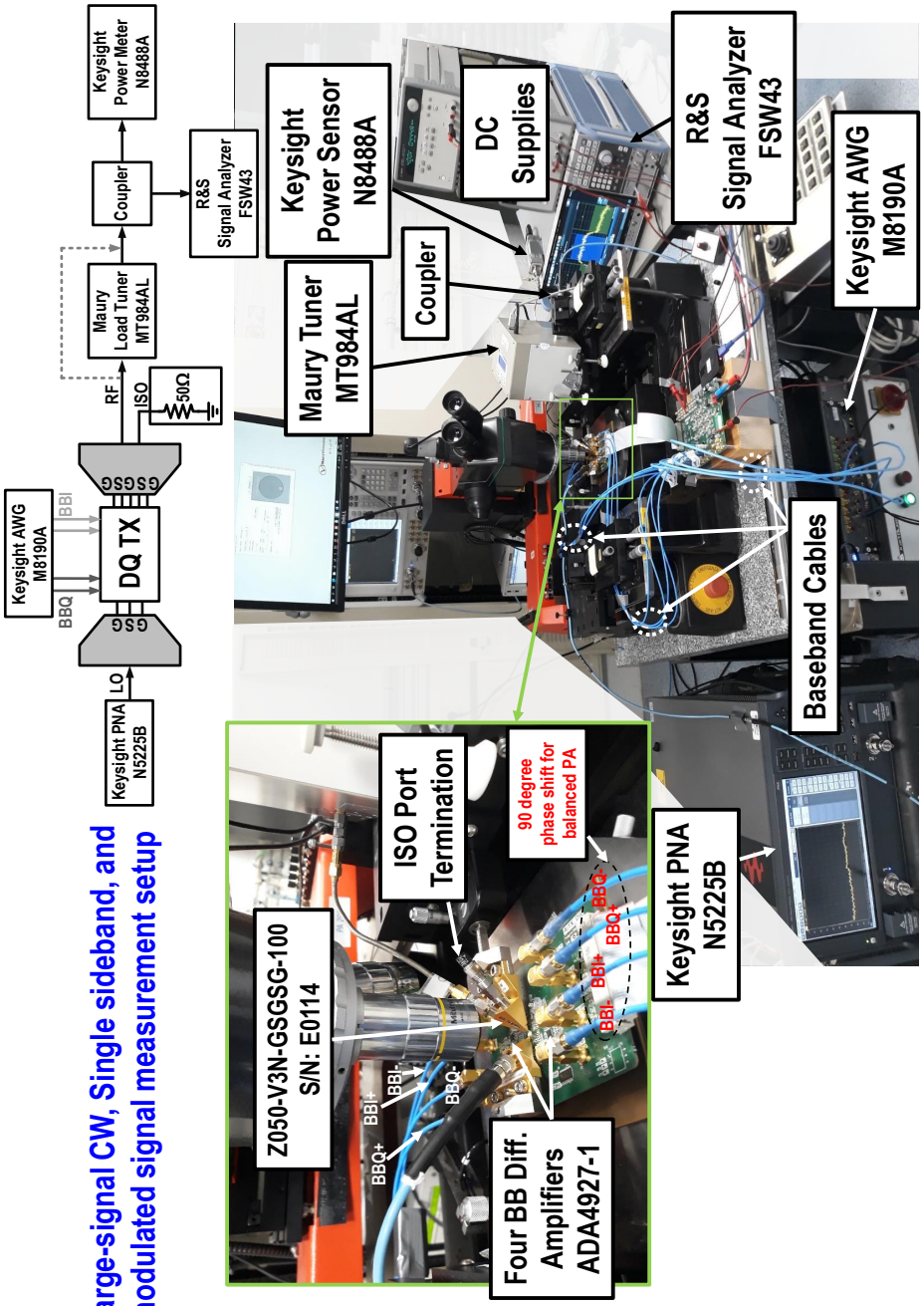


Figure 4.15: CW, SSB, modulated signal, and VSWR measurements setup.

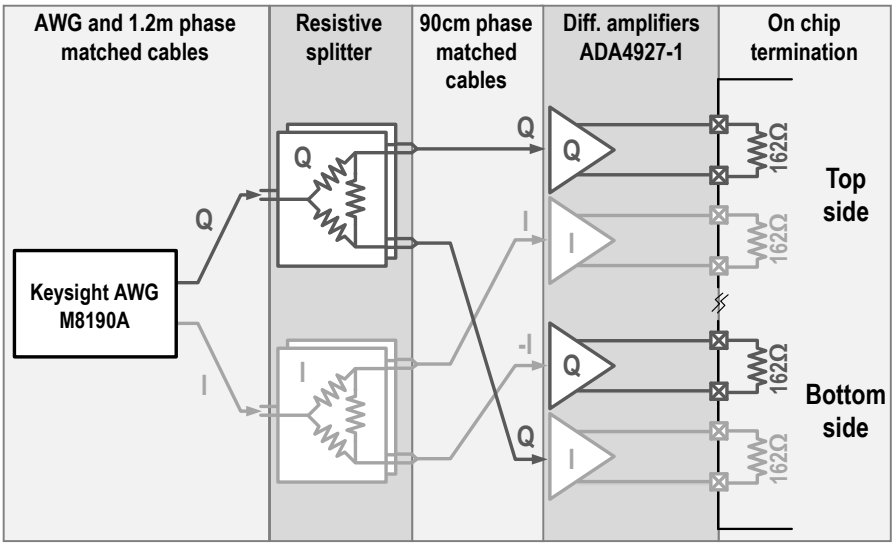


Figure 4.16: Baseband connections for the top and bottom sides of TX.

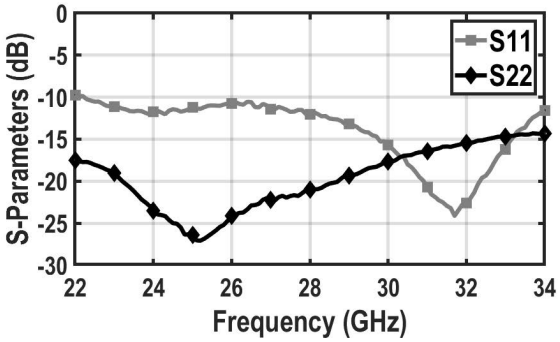


Figure 4.17: Small-signal S-parameter measurement results.

pads, are characterized by GSG and GSGSG probes, respectively. In this work, a 1V supply voltage is used for the PAs, pre-drivers, mixers, and the LO gain stage. Fig. 4.15 exhibits the measurement setup and its baseband connections. A Maury MT984AL load tuner is used for the VSWR measurement. The insertion losses of the probes, cables, and the directional coupler are measured and de-embedded.

4.5.1. CONTINUOUS-WAVE MEASUREMENTS

The input LO and the PA output reflection coefficients are characterized under small-signal conditions using a Keysight N5227A four-port network analyzer. Fig. 4.17 demonstrates the measured s-parameters over a 22.5-to-34GHz band. The corresponding LO port matching is better than -10.5dB. The PA's output reflection coefficient, S_{22}, is bet-

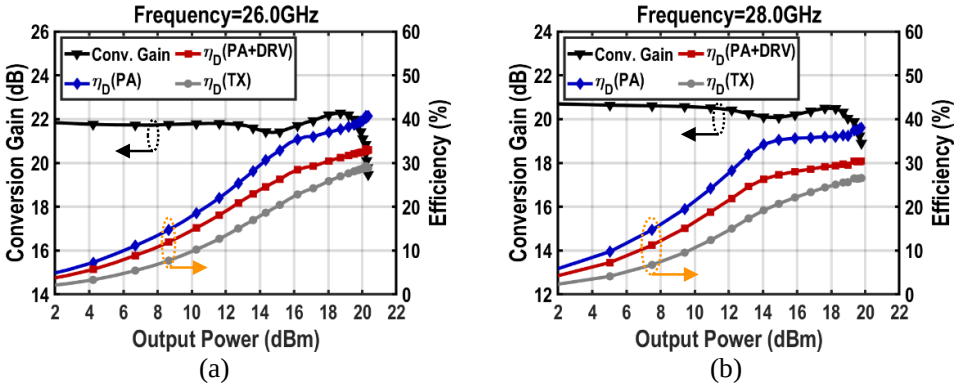


Figure 4.18: Large-signal CW measurement results (a) at 26GHz, and (b) at 28GHz.

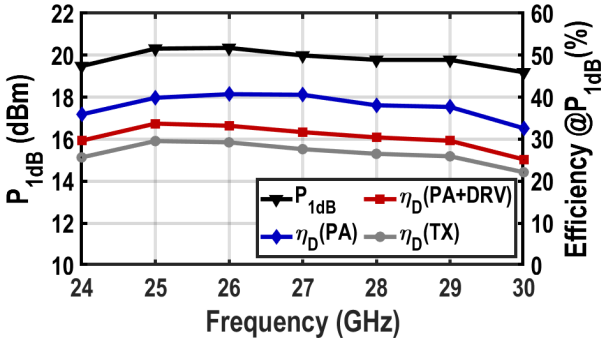


Figure 4.19: Large-signal CW measurement results across operational frequency.

ter than -18dB over the 22.5-to-30GHz band, while at 27GHz, it is -22.2dB. Thus, any unwanted coupled signal at 27GHz is suppressed by -22.2dB. Note that for the isolation port, a 50Ω termination is employed.

The large-signal continuous wave (CW) measurement results are reported in Fig. 4.18. At 26/28GHz, the P_{1dB} is 20.1/19.75dBm, while TX front-end drain efficiency is 28.76/26.4%. Moreover, at 6dB PBO, the PA drain efficiency is 30/33% at 26GHz/28GHz, while the TX conversion gain is 21.8dB/20.6dB. As depicted in Fig. 4.19, the TX delivers 20dBm over a 24-to-30GHz (i.e., -1dB bandwidth). Over this frequency band, the PA and TX peak drain efficiencies are more than 32.6% and 22.1%, respectively.

4.5.2. SINGLE-SIDEBAND MEASUREMENTS

Single-sideband (SSB) measurements evaluate the IRR performance of the proposed TX architecture. Since the double-quadrature structure offers high uncalibrated IRR, I/Q baseband signal mismatches significantly degrade the TX IRR performance. Fig. 4.15(b) shows the I/Q baseband connections in the measurement setup. These signals are first generated in MATLAB and then converted to differential analog signals using an

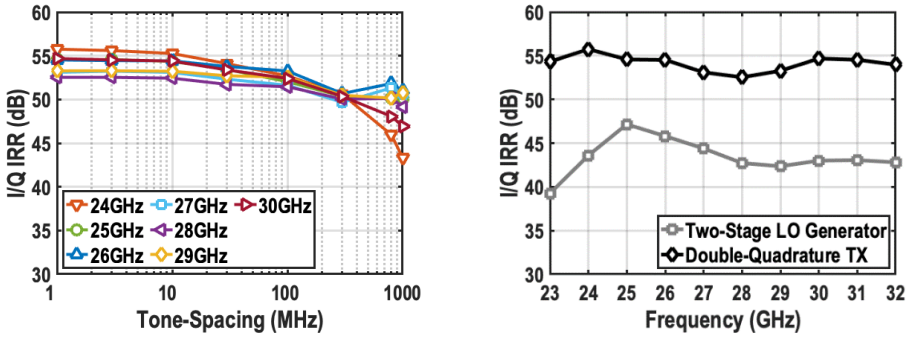


Figure 4.20: (a) Measured IRR versus tone-spacing across operational frequencies. (b) Measured IRR of two-stage LO generator showing IRR improvement by second IR stage.

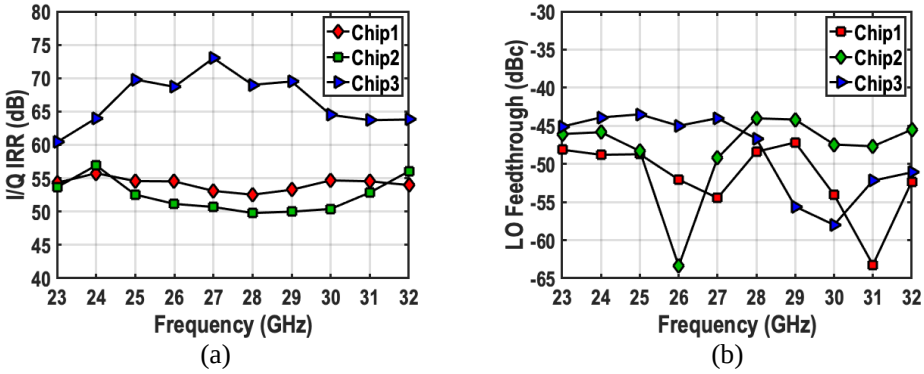


Figure 4.21: Measured (a) IRR, and (b) LOFT of three chips versus frequency without any calibration.

arbitrary-wave generator (AWG).

Fig. 4.20(a) demonstrates the measured IRR performance versus various tone-spacings at the 24-to-30GHz operational band. The TX achieves an uncalibrated IRR of better than 50dB over the desired frequency band owing to the proposed double-quadrature direct upconverter technique. Due to the minimal variation of IRR over the frequency band, it can be inferred that the I/Q baseband mismatches, i.e., cables, splitters, amplifiers, on-chip terminations, and baseband transistors of the mixers (see Fig. 4.15(b)) are the dominant imbalanced sources. Furthermore, by connecting the same I/Q signals to both the top and bottom TX paths, we can disable the second image rejection stage and measure only the IRR performance of the two-stage LO generator. As shown in Fig. 4.20(b), the second image rejection stage improves IRR by 11dB on average. However, according to the MC simulations, the IRR improvement should be at least 20dB, primarily degraded by the I/Q baseband mismatches that were discussed earlier. Additionally, as depicted in Fig. 4.21(a), three chips are validated, proving

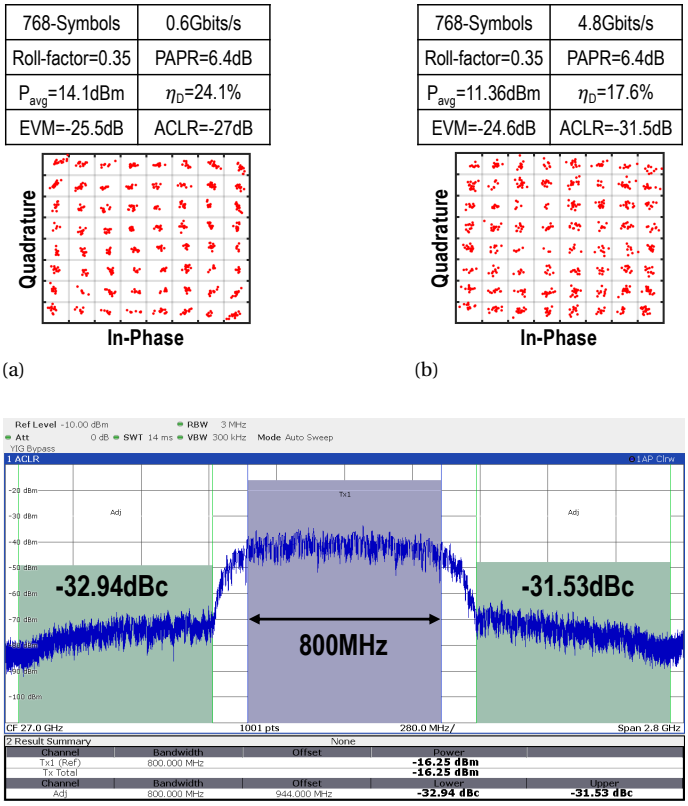


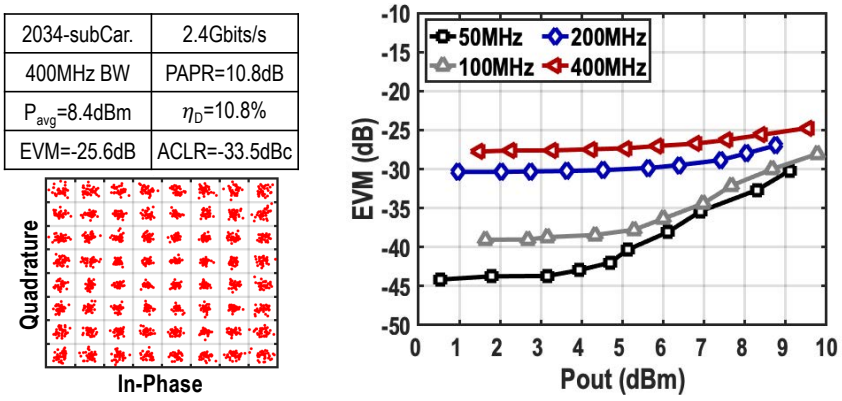
Figure 4.22: Measured constellations of a single-carrier 64-QAM signal with (a) 100MHz and (b) 800MHz bandwidth. (c) The spectral purity of an 800MHz 64-QAM signal with 6.4dB PAPR at 27GHz carrier frequency.

that the proposed architecture offers more than 50dB IRR over frequency without any calibration.

The LO feedthrough must be relatively low to achieve decent EVM. Due to the symmetric mixer layout and proper baseband transistors sizing based on the mismatch consideration, the TX attains better than -45dB uncalibrated LOFT. The measured LOFTs of three chips are demonstrated in Fig. 4.21(b). LOFT variation over frequency shows the mismatch of high-frequency parts significantly affects the LOFT performance.

4.5.3. MODULATED SIGNAL MEASUREMENTS

The TX dynamic performance is verified by wideband modulated signals such as a multi-carrier "64-QAM OFDM" signal. As illustrated in Fig. 4.15(a), the mm-wave TX output is directly captured by R&S FSW43 signal analyzer. Fig. 4.22 exhibits measured constellations, EVMs, and performance of 0.6Gb/s and 4.8Gb/s 64-QAM at 27GHz carrier



(a) (b)

Figure 4.23: (a) Measured constellations of a 400MHz single-carrier 64-QAM OFDM signal at 27GHz. (b) The measured EVMs versus average power for 50MHz, 100MHz, 200MHz, and 400MHz 64-QAM OFDM signals.

frequency. The TX achieves -25.5dB EVM for a 0.6Gb/s signal, while its average output power and PA drain efficiency are 14.1dBm and 24.1%, respectively. Additionally, its ACLR/EVM are -31.5dBc/-24.6dB for a 4.8Gb/s signal with 11.36dBm average output power and 17.6% drain efficiency. The spectral purity of 4.8Gb/s 64-QAM signal is shown in Fig. 4.22(c).

A 64-QAM OFDM signal is utilized to verify the performance of the proposed TX for 5G mm-wave systems. Fig. 4.23 shows the measured constellation for a "400MHz single-carrier 64-QAM OFDM" signal. With 8.4dBm output power and 10.8% drain efficiency, TX achieves an EVM of -25.6dB and an ACLR of -33.5dBc. The measured EVM of various modulation bandwidths of 50MHz, 100MHz, 200MHz, and 400MHz versus average output power is reported in Fig. 4.23(b). Their EVM significantly degrades by increasing their modulation bandwidth at lower average power. The primary limitations for high data rate signals are 1) The gain flatness of the baseband amplifiers, 2) the loss flatness of inter-stage and output matching networks, and 3) the loss flatness of the probe, cables, coupler, and signal analyzer. Likewise, considering all the EVM limitations, e.g., flatness, phase noise, third-order distortion, and thermal noise, measuring -44dB of EVM for 50MHz signal confirms that the contribution of IRR and LOFT on EVM is at least less than -44dB.

To further evaluate the TX performance under different 5G system scenarios, "64-QAM OFDM" signals with 50MHz, 100MHz, and 200MHz component carriers (CCs) and the overall aggregated bandwidth of 800MHz and 10% guard bands are exploited. Fig. 4.24 shows the spectrum and EVM of an "8-CC 64-QAM OFDM" signal with 8.4dBm average power and -27.1dB average EVM. The measured average EVM versus output power of 4, 8, and 16-CC OFDM signals with an 800MHz aggregated bandwidth are reported in Fig. 4.25. It shows that increasing the number of carriers improves its EVM for a dedicated data rate.

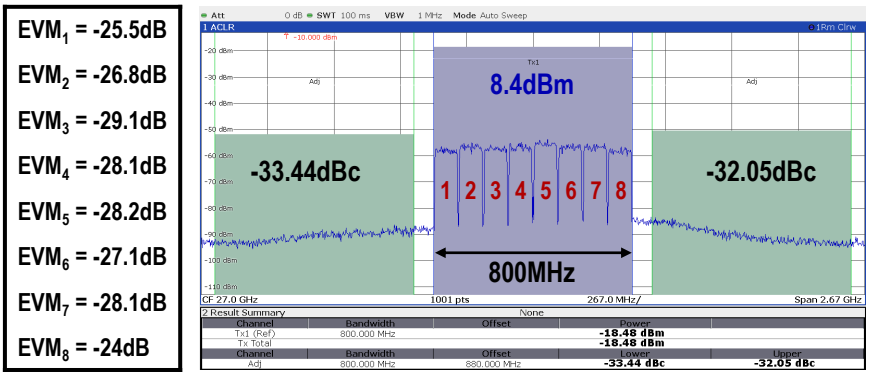


Figure 4.24: (a) The spectrum of an 8-CC 64-QAM OFDM signal and measured EVMs of each channel.

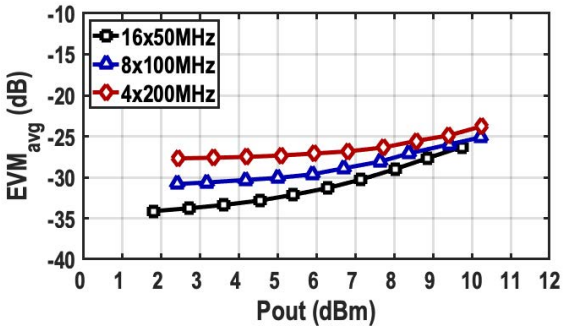


Figure 4.25: The measured average EVMs versus average power for 4, 8, and 16-CC 64-QAM OFDM signals with 800MHz bandwidth.

Finally, the following measurement sequences are performed to verify the impact of TX's IRR in a non-contiguous carrier aggregation scenario. First, a 2-CC "50MHz 64-QAM OFDM" signal is applied, whose spectrum (blue) is depicted in Fig. 4.26. Next, its mirror spectrum (red) is exploited. As illustrated in Fig. 4.26, the I/Q images of the first case are precisely on top of the second scenario and vice versa. It clearly indicates that poor IRR performance dramatically degrades the EVM. Eventually, the two signals presided at four different locations, i.e., two pairs of mirrored channels are simultaneously applied. Their measured EVMs are reported, exhibiting that the channels' EVM is not significantly degraded due to the decent I/Q image performance of the proposed double-quadrature TX.

4.5.4. VSWR MEASUREMENTS

As discussed in Section III, the robustness of EVM and forward power (P_{FWD}) under load mismatch are crucial in a phased-array system with mutual coupling. The VSWR resilience of the proposed efficiency-enhanced balanced PA is evaluated by measuring a "100MHz 64-QAM" signal under a VSWR of 3. The characterization of the Maury tuner

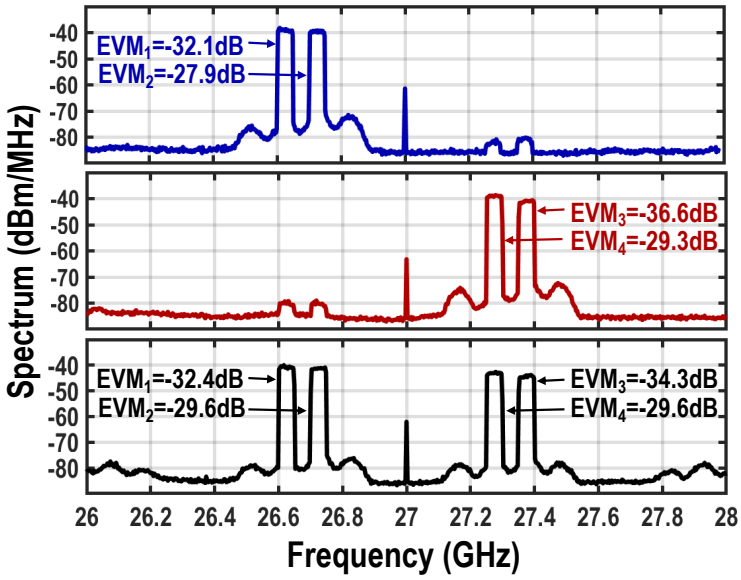


Figure 4.26: Measured spectrum and EVMs of a 2-CC 50MHZ 64-QAM OFDM signal at lower sideband (blue), a 2-CC 50MHZ 64-QAM OFDM signal at upper sideband (red), and a 4-CC OFDM signal.

and its calibration is done as described in [104]. Moreover, the bandwidth of the modulated signal is limited by the performance of the load tuner.

To begin with, the TX performance is measured for the matched impedance loading condition. The average output power and drain efficiency are 10.35dBm and 15%, respectively. Additionally, EVM=-28dB and ACLR=-30.6dBc are measured (Fig. 4.27). Then, the tuner is adjusted for the same input signal level to provide VSWR=3 loading condition, and the TX performance is measured for various VSWR angles. Consequently, assuming constant mismatch losses of passive components between the TX and the power sensor, the output power (P_{out}) fluctuation is also the deviation of forward power, reverse power, and gain. The measured P_{out}, P_{FWD}, average drain efficiency, EVM, and ACLR of the modulated signal versus VSWR angle are presented in Fig. 4.27.

Two drain efficiencies are exhibited in Fig. 4.27(b): the first drain efficiency is related to P_{FWD} (η_{FWD}), and the second one is related to P_{out} (η_{out}). In the antenna mismatch scenario, as discussed in Section 4.3.1, a portion of forward power is reflected and subsequently dissipated in the matching network losses and the isolation port. Therefore, P_{out} is considered as the radiated power, and its drain efficiency is then calculated based on P_{out}. However, in the mutual coupling scenario, since the reflected power is the coupled signal generated by the other TX elements in a phased-array system, assuming matched antenna impedance, the radiated power is equal to P_{FWD}. Therefore, the drain efficiency is eventually calculated based on P_{FWD} rather than P_{out}.

Similar to the average power and its efficiency, the measured EVM and ACLR are relatively robust under VSWR as demonstrated in Fig. 4.27(c). The maximum EVM and ACLR deviation are 1.65dB and 1dB, respectively. Additionally, the measured EVMs un-

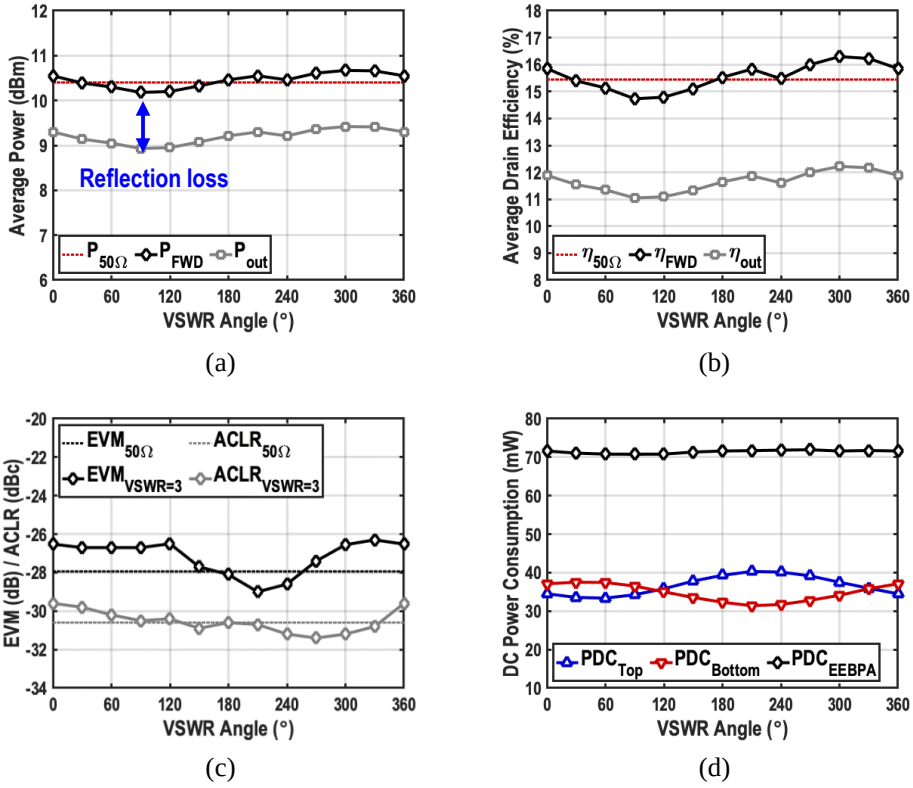
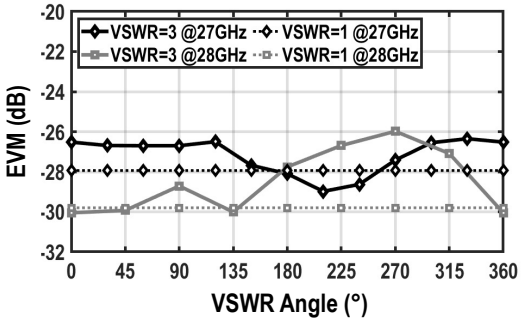


Figure 4.27: Measured (a) forward and output average power, (b) average drain efficiency of the related forward and output power, and (c) EVM/ACLR of a 100MHz 64-QAM signal versus VSWR angle under VSWR=3 compared to the impedance matched load measurement results.

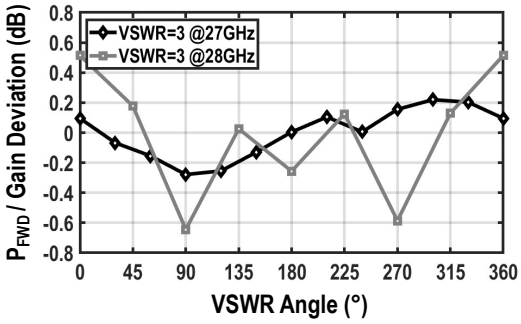
der VSWR of 1 and 3 at 27GHz and 28GHz are compared in Fig. 4.28(a). The maximum EVM deviation at 28GHz is 3.9dB. The gain and P_{FWD} deviation at 27GHz and 28GHz are depicted in Fig. 4.28(b). At 27GHz, the maximum deviation is 0.3dB, which occurs at a 90° VSWR angle. Likewise, at 28GHz, this deviation is only 0.65dB.

4.5.5. PERFORMANCE SUMMARY AND COMPARISON

Table I summarizes the measured performance of the proposed double-quadrature TX and compares it to that of prior-art mm-wave TXs/PAs. The TX occupies a 1.38mm^2 core area slightly larger than [104], which is only a PA. The proposed series-Doherty balanced PA provides a better output impedance termination than the state-of-the-art while enhancing the efficiency over a wide operational bandwidth of 24-to-30GHz with 40% peak drain efficiency. The measured drain efficiency at P1dB and 6dB PBO are comparable to [39] and [51], which have the best PAE at P1dB and 6dB PBO, respectively. Moreover, under VSWR, the proposed TX achieves less than 0.3dB and 1.9dB forward power and EVM



(a)



(b)

Figure 4.28: The measured (a) EVMs and (b) forward power/gain deviations of a 100MHz 64-QAM signal under VSWR of 1 and 3 at 27GHz and 28GHz.

deviation, respectively. Furthermore, the proposed double-quadrature modulator offers wideband IRR without calibration, outperforming state-of-the-art TXs utilizing the I/Q imbalance calibration. Additionally, thanks to the symmetrical layout of the I/Q modulator and mismatch considerations, the uncalibrated LOFT of three measured chips over various operational frequencies is less than -44dBc.

4.6. CONCLUSION

In this chapter, an efficient broadband TX comprising a double-quadrature direct-upconverter and a series-Doherty balanced PA in 40nm bulk CMOS is presented for 5G mm-wave phased-array systems. The proposed efficiency-enhanced balanced PA structure provides 20dBm output power while achieving 6-dB PBO efficiency enhancement under VSWR caused by the mutual coupling of phased-array systems. Moreover, the proposed double-quadrature direct-upconversion architecture inherently offers high IRR. Its second image-rejection stage is elegantly combined with the proposed quadrature hybrid balanced PA, resulting in superior I/Q image performance. The measured uncalibrated LOFT is among the best thanks to the symmetric layout and

Table 4.1: CMOS mm-Wave Transmitters/PAs Performance Comparison

	This Work		mm-Wave 5G Power Amplifiers						mm-Wave TX/Quadrature LO Generators		
			Mannem JSSC 2020	Chappidi TMTT 2020	Wang JSSC 2019	Li JSSC 2020	Huang ISSCC 2021	Shakib ISSCC 2017	Zhao JSSC 2015	Piri JSSC 2018	Kim JSSC 2018
Architecture	**Double-quadrature DUC with series-Doherty BPA**		Reconfigurable Doherty PA	Broadband Doherty PA	Mixed-signal Doherty PA	Inverse outphasing TX	Continuous Coupler Doherty PA	Analog linear PA	E-band TX	Wideband IQ generator	Transceiver
Technology	**40nm CMOS**		45nm SOI	65nm CMOS	45nm CMOS	45nm SOI	45nm SOI	40nm CMOS	40nm CMOS	55nm CMOS	28nm CMOS
Supply	**1V**		2V, 1V	1.1V	2V	2V, 1V	2V, 1V	1.1V	0.9/1.1V	1.2V	1.8/1.05/0.8V
Freq. (GHz)	**24 to 30**		39	26 to 42	27	29	26 to 60	27	71 to 86	28 to 44	28
Core area (mm^2)	**1.38**		1.18	1.35#	0.52	0.96	0.62	0.23	0.225	0.195	7.28#
Gain (dB)	**21.8 (at 27GHz)**		12.4*	13.5*	19.1	30	15.5*	22.4	11	N/A	48
P_{1dB}/P_{sat} (dBm)	**20 (at 27GHz)**		20.2/20.8	19.2/19.6	22.4/23.3	22.7	21.5/22	13.7/15.1	8.8/12	N/A	9.5
PAE_{peak}/PAE_{6dB} (%)	**31/26‡ (at 27GHz)**		33.3/22.4	24/20.2	40.1/33.1	41.3/29.6	40.5/32.5	33.7/15.1	N/A	N/A	8.5/5
S_{22} (dB)	**-22.2 (at 27GHz)**		-9*	N/A	-2*	N/A	N/A	-7*	N/A	N/A	-4*
LOFT (dBc)	**-45**		N/A	N/A	N/A	N/A	N/A	N/A	-40.2†	N/A	-39†
IRR (dB)	**>50**		N/A	N/A	N/A	N/A	N/A	N/A	40.5†	>40†	62†
TX Efficiency (%)	**28.5 (at 27GHz)**		N/A	N/A	N/A	N/A	N/A	N/A	15	N/A	N/A
Calibration / DPD	**No / No**		N/A / No	N/A / No	N/A / No	No / Yes	N/A / No	N/A / No	Yes / No	Yes / N/A	Yes / No
Modulation scheme	**64-QAM**	**64-QAM 8-CC OFDM**	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM	64-QAM 8-CC OFDM	64-QAM	N/A	LTE 64-QAM
Data rate (Gb/s)	**4.8**	**800MHz**	3	2	6	3	3	800MHz	4.5	N/A	20MHz
EVM_{rms} (dB)	**-24.6**	**-27.1**	-22.9	-24	-25.3	-25.3	-25	-25	-24	N/A	-33
ACLR (dBc)	**-31.45**	**-32**	-25.4	-25	-29.6	-29.8	-28.8	-29	N/A	N/A	N/A
P_{avg} (dBm)	**11.36**	**8.4**	12.2	9.8	15.9	16	13.4	6.7	N/A	N/A	3
PAE_{avg} (%)	**17.6 ($\eta_{D,PA}$)**	**10.8 ($\eta_{D,PA}$)**	16.1	10.2	29.1	23.8	24.8	11	N/A	N/A	3
Modulation / VSWR	**64-QAM / 3:1**		64-QAM / 3:1	CW / 4:1	N/A	N/A	N/A	N/A	N/A	N/A	N/A
EVM deviation (dB)	**1.9/3.9 (at 27/28GHz)**		1.6	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
P_{FWD} variation (dB)	**0.51/1.2 (at 27/28GHz)**		0.62 (2.6)**	2	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Chip area. *Graphically estimated. ‡Drain efficiency of the PAs and pre-drivers. †After calibration. **P_{1dB} (Gain) variations: gain variation is graphically estimated.

mismatch consideration. Occupying a 1.38mm^2 core area, TX delivers more than 20dBm P_{1dB} with 40% drain efficiency while achieving reasonable PBO drain efficiency and linearity. Additionally, this prototype obtained excellent uncalibrated IRR and LOFT performance.

4.7. APPENDIX A

The mathematical relationship of the image rejection at the second stage of the proposed DQ-DUC is elaborated. In this context, $x_{BB,I}$ and $x_{BB,Q}$ are I/Q baseband signals. Considering this, the I/Q LO signals with phase and amplitude mismatches are represented as follows:

$$LO_I = (1+\frac{\epsilon}{2})\cos(\omega_c t + \frac{\Delta\theta}{2}), \tag{4.7}$$

$$LO_Q = (1-\frac{\epsilon}{2})\sin(\omega_c t - \frac{\Delta\theta}{2}), \tag{4.8}$$

were ϵ and $\Delta\theta$ are amplitude and phase error of I/Q LO signals. The RF_0 and RF_{90} signals shown in Fig. 4.3 can be calculated as

$$RF_0 = x_{BB,I}LO_I - x_{BB,Q}LO_Q, \tag{4.9}$$

$$RF_{90} = x_{BB,Q}LO_I + x_{BB,I}LO_Q, \tag{4.10}$$

Now, by placing (4.7) and (4.8) in (4.9) and (4.10), the combined RF signal at the PA port of QHC can be calculated as

$$\begin{aligned} RF &= RF_0 + H(RF_{90}) = x_{BB,I}(1+\frac{\epsilon}{2})\cos(\omega_c t + \frac{\Delta\theta}{2}) \\ &- x_{BB,Q}(1-\frac{\epsilon}{2})\sin(\omega_c t - \frac{\Delta\theta}{2}) + x_{BB,Q}(1+\frac{\epsilon}{2})\cos(\omega_c t \\ &+ \frac{\Delta\theta}{2} - \frac{\pi}{2}) + x_{BB,I}(1-\frac{\epsilon}{2})\sin(\omega_c t - \frac{\Delta\theta}{2} - \frac{\pi}{2}) \implies \\ RF &= x_{BB,I}[(1+\frac{\epsilon}{2})\cos(\omega_c t + \frac{\Delta\theta}{2}) + (1-\frac{\epsilon}{2})\cos(\omega_c t \\ &- \frac{\Delta\theta}{2})] - x_{BB,Q}[(1-\frac{\epsilon}{2})\sin(\omega_c t - \frac{\Delta\theta}{2}) + (1+\frac{\epsilon}{2}) \\ &\sin(\omega_c t + \frac{\Delta\theta}{2})], \end{aligned} \tag{4.11}$$

where $H(RF_{90})$ is the Hilbert transform of the RF90 waveform. We can derive a similar expression for the combined signal at the isolation port of QHC. Performing some mathematical expansions and simplifications (4.11) using well-known trigonometric identities, RF can be expressed as

$$\begin{aligned} RF &= 2\cos(\frac{\Delta\theta}{2})(x_{BB,I}\cos(\omega_c t) - x_{BB,Q}\sin(\omega_c t)) \\ &- \epsilon\sin(\frac{\Delta\theta}{2})(x_{BB,Q}\cos(\omega_c t) + x_{BB,I}\sin(\omega_c t)). \end{aligned} \tag{4.12}$$

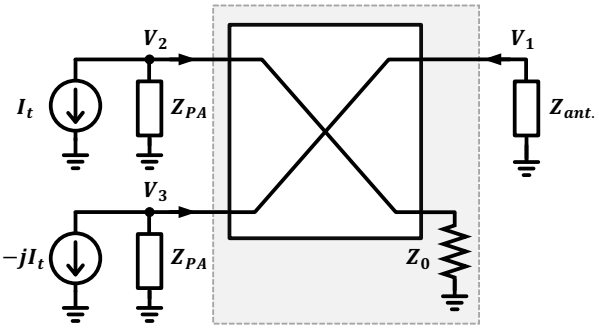


Figure 4.29: Z-parameter analysis of a balanced PA in antenna mismatch scenario assuming identical PAs.

This expression proves that the amplitude and phase mismatches are canceled, and thus, the desired output modulated signal does not contain any I/Q image component.

4.8. APPENDIX B

Fig. 4.29 shows a schematic for impedance analysis. In this context, two test current sources are applied simultaneously to both PA ports to obtain the related Z-impedance matrix. We assume an ideal Z_0 resistor terminates the isolation port to simplify the calculations. Consequently, the combiner can be considered as a three ports network and, therefore, the S-parameter and Z-parameter matrixes are squeezed to [117]

$$S = \begin{bmatrix} 0 & j & 1 \\ j & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix}, \tag{4.13}$$

$$Z = Z_0 \begin{bmatrix} 1 & -j\sqrt{2} & \sqrt{2} \\ -j\sqrt{2} & 0 & -j \\ \sqrt{2} & -j & 2 \end{bmatrix}. \tag{4.14}$$

Applying KCL analysis at the three ports, the impedance equations can be calculated by solving the following

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = Z_0 \begin{bmatrix} 1 & -j\sqrt{2} & \sqrt{2} \\ -j\sqrt{2} & 0 & -j \\ \sqrt{2} & -j & 2 \end{bmatrix} \begin{bmatrix} -\frac{V_1}{Z_{ant.}} \\ -I_t - \frac{V_2}{Z_{PA}} \\ jI_t - \frac{V_3}{Z_{PA}} \end{bmatrix}. \tag{4.15}$$

Hence, the impedances driven by two PAs are calculated as

$$\begin{aligned} Z_{L1} &= \frac{V_2}{I_t + \frac{V_2}{Z_{PA}}} \\ &= Z_0 \frac{Z_0^2 + (Z_{ant.} - Z_{PA})\, Z_0 + 3 Z_{PA} Z_{ant.}}{3 Z_0^2 + (Z_{PA} - Z_{ant.})\, Z_0 + Z_{PA} Z_{ant.}}, \end{aligned} \tag{4.16}$$

$$
\begin{aligned}
Z_{L2} &= \frac{V_3}{-jI_t + \frac{V_3}{Z_{PA}}} \\
&= Z_0 \frac{Z_0^2 + (Z_{ant.} + 3Z_{PA})\, Z_0 - Z_{PA} Z_{ant.}}{-Z_0^2 + (Z_{PA} + 3Z_{ant.})\, Z_0 + Z_{PA} Z_{ant.}}.
\end{aligned}
\tag{4.17}
$$

5

LOAD-MODULATION-BASED IMD3 CANCELLATION FOR MM-WAVE CLASS-B CMOS PAS

This chapter presents a novel load-modulation-based third-order intermodulation distortion (IMD3) cancellation technique for class-B CMOS power amplifiers (PAs). In a class-B PA, the IMD3 generated by the third-order transconductance (g_{m3}) and the gain compression have opposite signs, and thus, they can cancel each other at specific bias and loading conditions. The proposed Doherty topology allows for the adjustment of gain compression by modulating the effective loading, facilitating IMD3 cancellation over the entire load modulation region. The proposed approach is verified using a 28GHz 40nm CMOS series-Doherty PA topology. The experimental result demonstrates 10/17dB IMD3 improvement compared to class-B/Doherty PA operation. Without using any digital predistortion, the measured EVM of the proposed technique for a 50MHz 64-QAM OFDM signal with 8.9dBm average output power is -38.7dB (1.2%), which is 5.7/11dB better than a standard class-B/Doherty PA operation.

This chapter is based on the paper published in the IEEE Microwave and Wireless Components Letters [118].

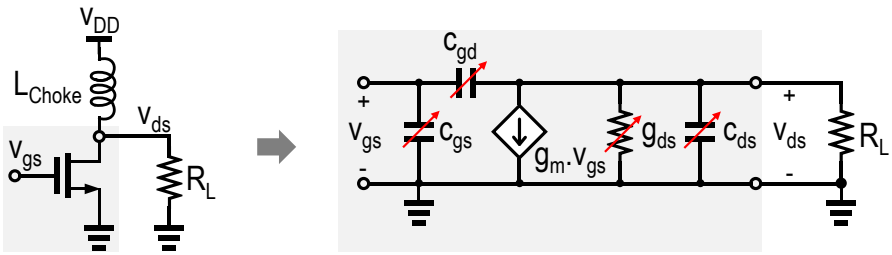


Figure 5.1: An equivalent model of a common-source PA.

5.1. INTRODUCTION

Mm-wave 5G communication systems have rapidly developed to address the market demand for high data throughput and user capacity. Their transmitters (TXs) typically employ spectrally efficient complex modulation schemes with high peak-to-average power ratios (PAPRs). However, this requires the operation of the power amplifiers (PAs) in power back-off (PBO) to fulfill the stringent linearity requirements like the adjacent channel leakage ratios (ACLRs) and error vector magnitudes (EVMs). The key design trade-off is the PA linearity and efficiency close to compression.

Since the PAs typically operate at relatively high-power levels, their actual third-order intermodulation distortion (IMD3) mechanism must be investigated under these conditions rather than in low-power operation [119]. Four dominant IMD3 contributors are present in a CMOS PA: 1) the third-order transconductance (g_{m3}), 2) the gain compression due to drain voltage clipping, 3) the voltage-dependent nonlinear parasitic capacitors (e.g., gate-source C_{gs}, gate-drain C_{gd}, and gate-bulk C_{gb}), and 4) the second-order mixing products. Enhanced second-harmonic termination [120, 121], PMOS varactor-based AM-PM compensation [122, 123], hybrid NMOS/PMOS PA structures [124–126], and transformer-based AM-PM correction [127] are proposed to improve the mm-wave PAs' linearity, deteriorated by the second-order mixing products and nonlinear capacitors. Moreover, adaptive biasing, multi-gate transistor, and antiphase [128–136] techniques are proposed for IMD3 cancellation. However, their cancellation regions are narrow and occur at low power levels, making them less suitable for PAs operating closer to compression.

In this chapter, a new load-modulation concept is presented for IMD3 cancellation in energy-efficient class-B/deep class-AB operation. In a class-B PA, the IMD3 generated by g_{m3} and gain compression have opposite signs, and thus, they can cancel each other at a specific point. This condition provides a sweet spot near the PA's peak power level. The proposed load-modulated PA topology allows dynamic adjustment of the gain compression point by modulating the load seen by the drain nodes. Consequently, this mechanism can suppress the IMD3 generated by g_{m3} over a large power back-off (PBO) range.

This chapter is organized as follows. Section 5.2 introduces the theory and principles, and the proposed load-modulation-based IMD3 cancellation technique is presented in Section 5.3. The load-modulated linear PA (LLPA) is presented in Section 5.4. Section 5.5

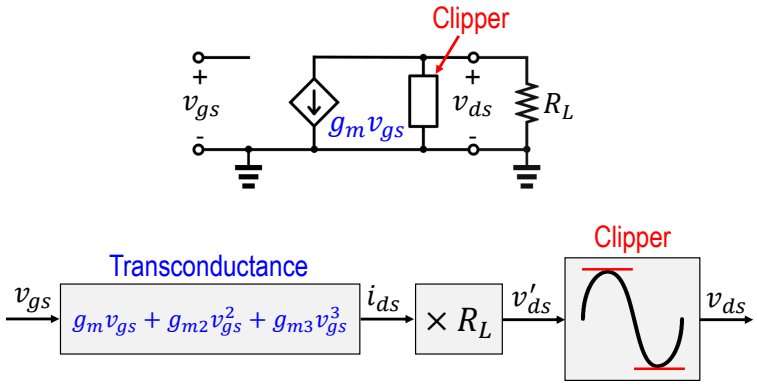


Figure 5.2: A simplified model of the common-source PA.

reports the measurement results, and Section 5.6 concludes the chapter.

5

5.2. THEORY AND PRINCIPLES

Fig. 5.1 depicts an equivalent model of a common-source PA. In a CMOS PA, the nonlinear capacitors and second harmonic distortion can be addressed effectively without affecting other IMD3 contributors. On the contrary, both g_{m3} and clipping are strongly dependent on transistor bias. It means that if we manipulate the bias voltage to improve g_{m3}, it will affect the clipping. Therefore, in this section, we omit the parasitic capacitors and focus only on the nonlinear transconductance and clipping phenomena that produce the IMD3, thus limiting the linearity.

5.2.1. IMD3 ANALYSIS: A SIMPLIFIED MATHEMATICAL MODEL

A simplified model of the common-source PA is illustrated in Fig. 5.2. It includes a nonlinear transconductance to convert the input voltage (v_{gs}) to the current (i_{ds}), which is multiplied by a load resistor ($\times R_L$) to form a current to voltage (v'_{ds}) conversion, and a clipper to model the compression. Modeling the nonlinear transconductance as a polynomial, the output IMD3 is simulated in four conditions: 1) $g_{m3} \neq 0$ and clipper is *OFF*, 2) $g_{m3} = 0$ and clipper is *ON*, 3) $g_{m3} < 0$ and clipper is *ON*, and 4) $g_{m3} > 0$ and clipper is *ON*.

The simulation results of four cases are illustrated in Fig. 5.3. As expected, the IMD3 increases by a slope of two when the clipper is *OFF*. On the other hand, applying clipping to the model with an ideal transconductance ($g_{m3} = 0$) leads to no IMD3 in the lower power levels. However, as soon as the non-distorted output voltage swing (v'_{ds}) reaches the clipping threshold, the IMD3 increases sharply. Moreover, considering negative g_{m3}, the IMD3 components of g_{m3} and clipping happened to be in-phase, thus adding up as shown in Fig. 5.3(c). On the contrary, when $g_{m3} > 0$, the IMD3 components are out-of-phase, canceling each other at a single output power level and forming an IMD3 sweet spot. As depicted in Fig. 5.3(d), at lower power levels, g_{m3} is dominant, while clipping takes the responsibility of IMD3 degradation at higher power levels.

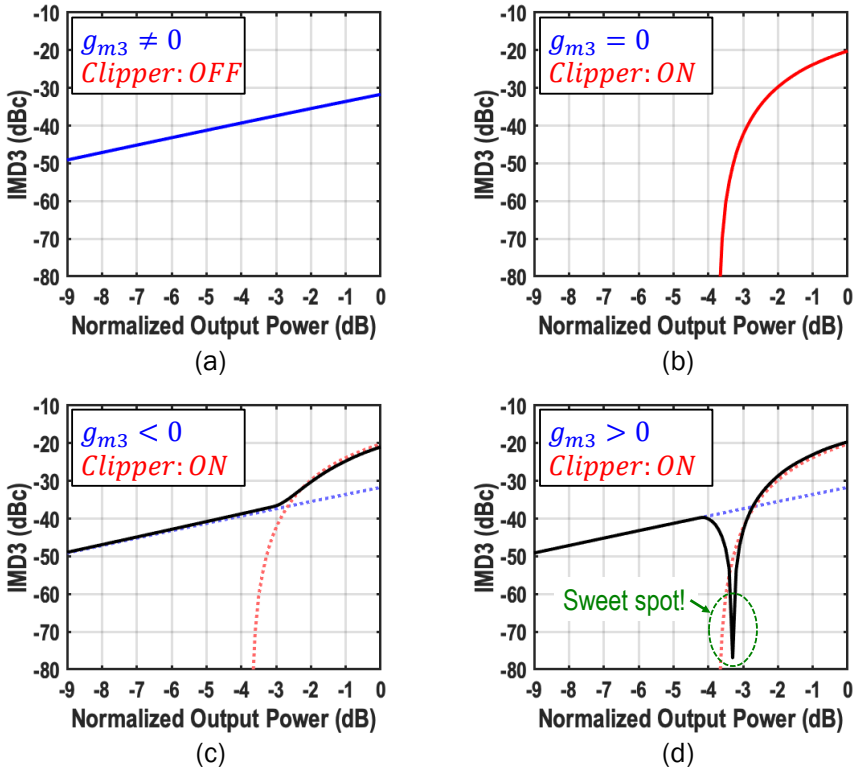


Figure 5.3: The simulated output IMD3 when (a) $g_{m3} \neq 0$ and clipper is OFF, (2) $g_{m3} = 0$ and clipper is ON, (c) $g_{m3} < 0$ and clipper is ON, and (d) $g_{m3} > 0$ and clipper is ON.

5.2.2. IMD3 ANALYSIS: A 40NM CMOS MODEL

In Fig. 5.4, a 40nm NMOS transistor's transconductance (g_m) and its first and second derivatives (g_{m2} and g_{m3}) are given versus gate bias voltage (VGS). For a highly efficient class-B PA, the bias point is chosen close to the turn-on point where g_m starts to increase, and the g_{m3} reaches its maximum value with a positive sign because of the PA's gain expansion. On the other hand, in a pure class-AB operation, the quiescent bias point at low-power operation provides low IMD3 while g_{m2} is at its maximum, entailing second-order mixing products, giving rise to higher IMD3. Furthermore, the drain-source currents are presented versus drain-source voltage (VDS) for various gate bias points. The transistor enters the triode region by decreasing VDS, resulting in gain compression and, thus, entailing an IMD3 component with a negative sign.

To gain more insight, the first-, second-, and third-order channel conductance (g_{ds}, g_{ds2}, and g_{ds3}) versus VDS for the class-B and class-AB biasing conditions are depicted in Fig. 5.5 (left). It shows that the class-AB operation introduces high IMD3 at higher power levels due to its higher bias voltage. In contrast, the class-B operation offers lower IMD3 at higher power levels as it is biased close to its turn-on region. Moreover, since

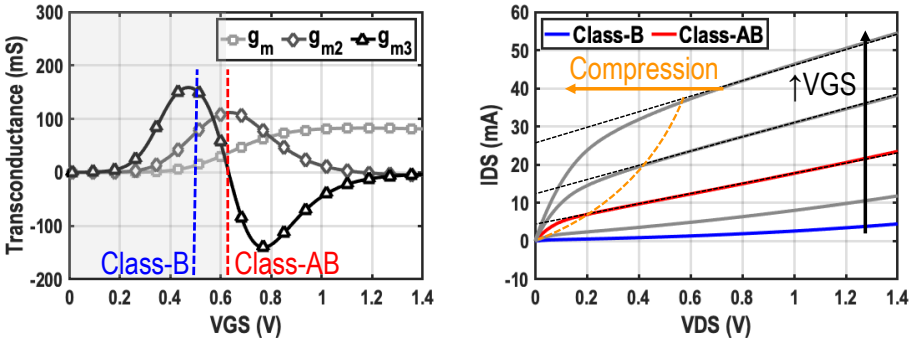


Figure 5.4: The simulated g_m, g_{m2}, and g_{m3} of a 40 nm nMOS transistor versus gate bias voltage and drain–source current versus drain–source voltage are given.

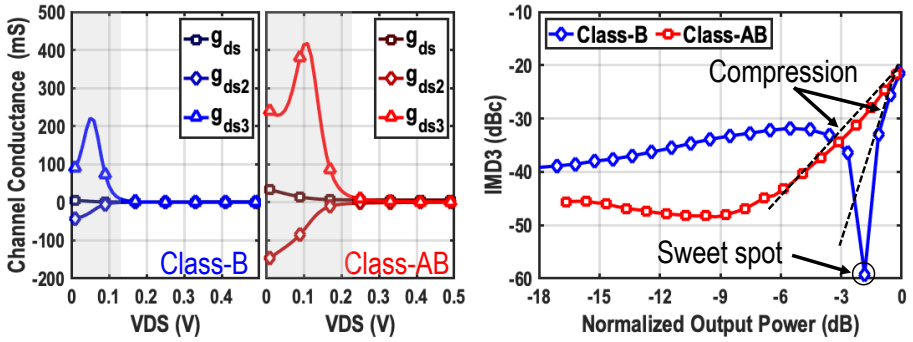


Figure 5.5: The g_{ds}, g_{ds2}, and g_{ds3} versus VDS and the two-tone simulation results of class-B and class-AB 40nm CMOS PAs.

the class-B has positive g_{m3} at lower power levels and negative g_{ds3} at higher power levels due to gain compression, moving from lower to higher power levels, an IMD3 sweet spot is expected, as shown in Fig. 5.5 (right). Nevertheless, this sweet spot is observed only at a single output power level yielding a sharp notch.

In summary, the class-B biasing condition provides low IMD3 close to its peak output power while offering high efficiency. However, its high g_{m3} leads to high small-signal IMD3. Moreover, as both mathematical and CMOS model confirmed, the IMD3 components of positive g_{m3} and gain compression maintain an IMD3 sweet spot.

5.2.3. PROPOSED LOAD-MODULATION-BASED IMD3 CANCELLATION

The cancellation should happen over a larger dynamic range to take practical advantage of the observed IMD3 sweet spot. Since the gain compression depends on the output voltage swing ($v'_{ds} = i_{ds}R_L$), the sweet spot is shifted to lower output power levels by increasing the load resistor (R_L). Fig. 5.6 demonstrates two-tone IMD3 simulations of a neutralized common-source PA for various R_L. Accordingly, if R_L is modulated dy-

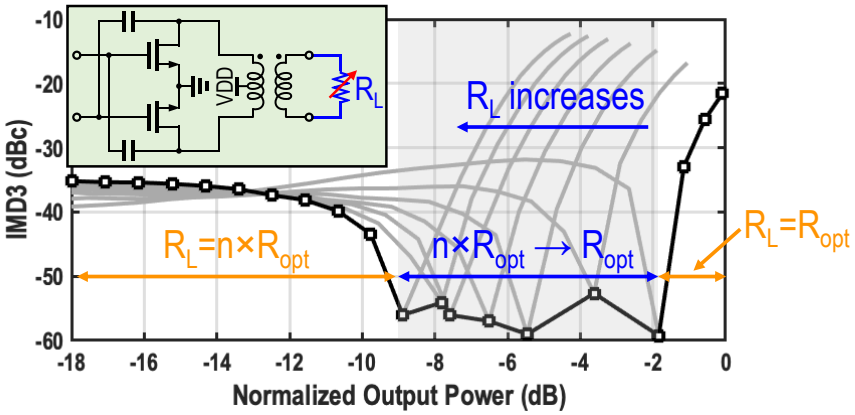


Figure 5.6: The two-tone simulations for various R_L exhibiting IMD3 sweet spot at lower output power levels.

5

namically to maintain the drain voltage swing at a region where the IMD3 component produced by clipping (g_{ds3}) cancels its counterpart generated by g_{m3}, IMD3 suppression can be achieved for a wide output power range.

5.3. PROPOSED LOAD-MODULATED LINEAR PA (LLPA)

As discussed in Chapter 3, in the load modulation PA architectures such as load-modulated balanced amplifier (LMBA) and Doherty PA (DPA), the load is modulated dynamically to maintain the drain voltage swing at a region where PA achieves its highest efficiency. The same architectures can be utilized to implement the proposed load-modulation-based IMD3 cancellation technique.

Fig. 5.7 (top) depicts parallel- and series-DPA structures that use load modulation techniques to enhance their PBO efficiency. In a DPA structure, the auxiliary PA (i_a) modulates the main PA's load (Z_m) to keep its drain voltage (v_m) at the maximum swing, maintaining the maximum drain efficiency (see Fig. 5.7, middle). Hence, the main PA works in two loading conditions: 1) the PBO region where R_L=2×R_{opt}, and 2) the load modulation region while R_L is modulated from 2×R_{opt} to R_{opt}.

Employing the same topology, the proposed load-modulated linear PA (LLPA) features a new load modulation scheme to enhance linearity. In this context, the load modulation starts sooner than a conventional DPA to keep v_m at its optimum level where the sweet spot occurs, achieving IMD3 cancellation (see Fig. 5.7, bottom). Consequently, the main PA works in three loading conditions: 1) the low-power region where R_L=2×R_{opt}, 2) the load modulation region while R_L is modulated from 2×R_{opt} to R_{opt}, and 3) the high-power region where R_L=R_{opt}. Note that the drain efficiency at PBO is degraded in this new arrangement compared to the conventional DPA to benefit the linearity. It is worth mentioning that in an ideal DPA structure, the output power and linearity are determined by the main PA, whereas the auxiliary PA only regulates the main PA's drain voltage.

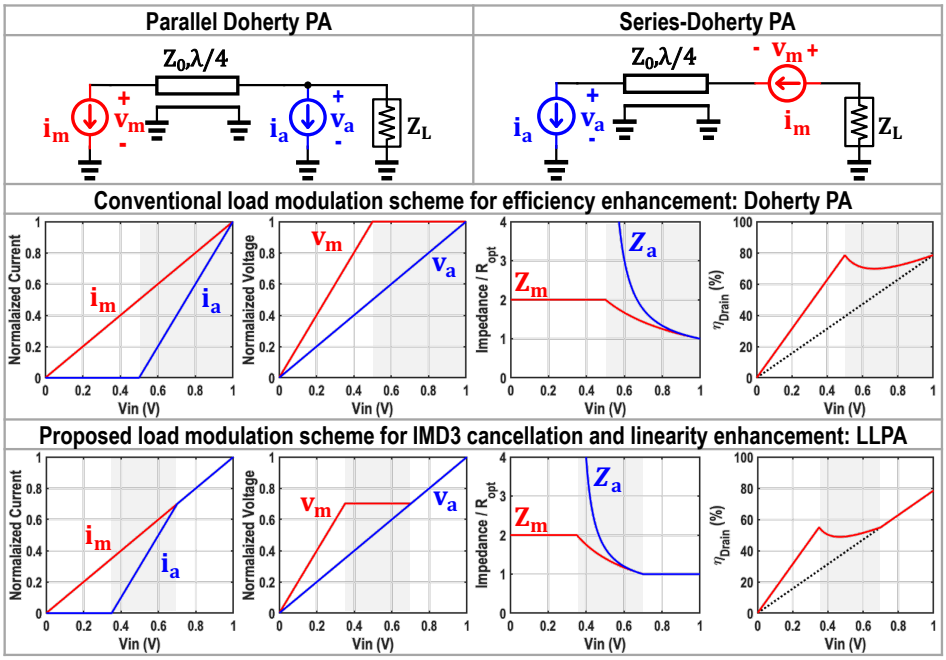


Figure 5.7: Parallel and series Doherty PAs' simplified structures (top), the load modulation scheme of conventional Doherty PA (middle), and the proposed load modulation scheme for IMD3 cancellation (bottom).

5.4. CIRCUIT IMPLEMENTATION

As proof of concept, the proposed IMD3 cancellation load modulation technique is verified using a 28GHz 40nm CMOS series-Doherty balanced PA prototype [137].

The prototype contains two identical series-Doherty PAs that are combined through a quadrature hybrid coupler, achieving more than 20dBm peak power to meet the 5G application requirements [137]. Fig. 5.8 shows the employed series-Doherty PA topology, which can be reconfigured by exploiting its (dynamic) biasing conditions to realize the proposed LLPA. Each main/auxiliary branch comprises a neutralized driver amplifier (DA), a transformer as inter-stage matching, and a neutralized common-source push-pull PA. The PAs are connected to a series-Doherty matching network (A detailed matching network design method is discussed in 3). On-chip I/Q modulators generate quadrature signals for main and auxiliary PAs. Besides, two PMOS varactors at the input of the DA and PA improve the AM-PM profile, which was mainly set by nonlinear NMOS gate capacitors [122].

Adaptive biasing circuits modulate the biases of the auxiliary branch to perform load modulation. Using the detection bias voltage of the envelope detector (V_{det}), the load modulation can be configured to operate in three modes: 1) a conventional efficiency enhancement for a DPA, 2) the proposed IMD3 cancellation (LLPA) and 3) two standard class-B PAs whose loads are always equal to R_{opt} and simply power-combined through the Doherty passive network.

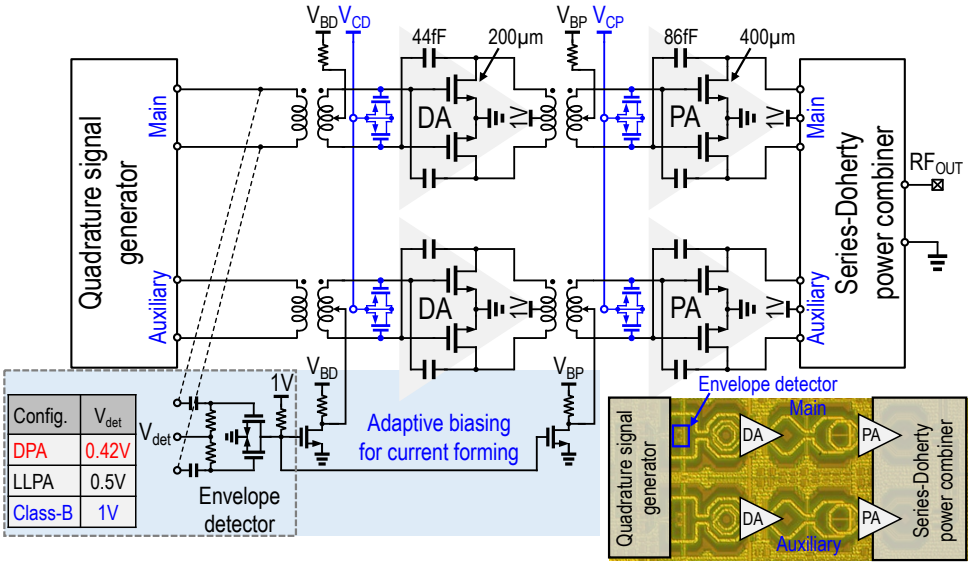


Figure 5.8: The schematic and die photo of the employed 28GHz series-Doherty PA to realize the proposed LLPA.

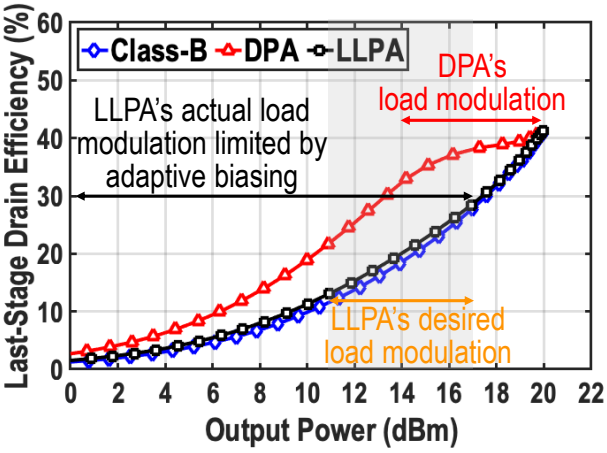


Figure 5.9: CW measurement results vs. output power.

5.5. EXPERIMENTAL RESULTS

The performance of the proposed technique is measured at 28GHz carrier frequency. The measured last-stage drain-efficiency of the LLPA (V_{det}=0.5V) is compared to the class-B PA (V_{det}=1V) and DPA (V_{det}=0.42V) operating conditions in Fig. 5.9. Note that all bias and supply voltages (except V_{det}) are kept the same for these three configurations. In this prototype, the control of the envelope detector and adaptive biasing speed

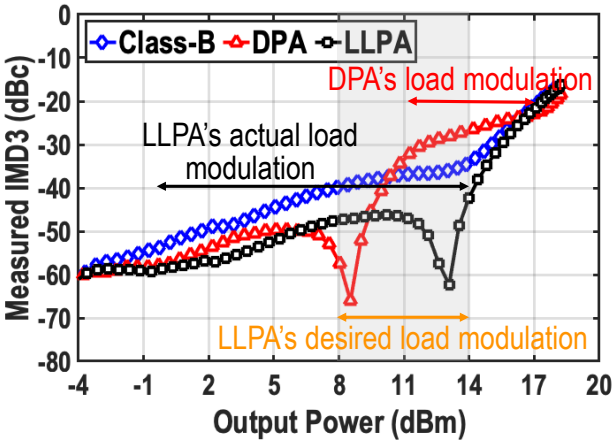


Figure 5.10: Two-tone IMD3 measurement results vs. output power.

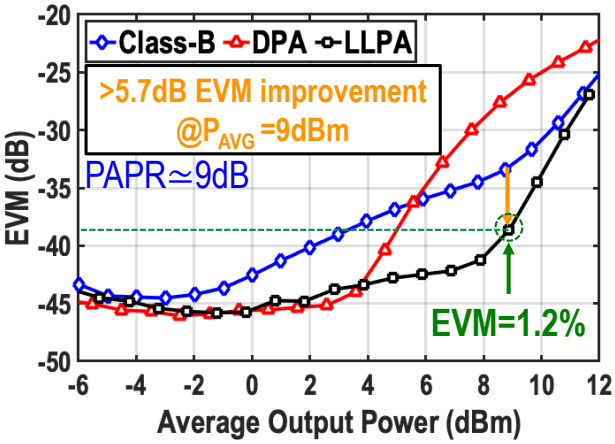


Figure 5.11: The measured EVM of a 50MHz 64-QAM OFDM versus P_{AVG}.

is somewhat limited. Therefore, the load modulation starts at a lower power level, yielding some drain efficiency degradation at deep PBO. However, in a two-tone test scenario, the LLPA exhibits >10dB IMD3 improvement over its class-B operation (Fig. 5.10). As expected, the IMD3 of DPA stays relatively high during the load modulation because the main PA operates near its compression region to achieve maximum efficiency.

The measured EVM of a 50MHz 64-QAM OFDM signal versus average output power (P_{AVG}) for three PA operating conditions are depicted in Fig. 5.11 without using any digital pre-distortion. The proposed LLPA achieves -38.7dB EVM at 8.9dBm P_{AVG}, which is 5.7/11dB lower than its class-B/DPA counterparts. Besides, the measured lower and upper side ACLRs of a 50MHz 64-QAM OFDM signal versus average output power are

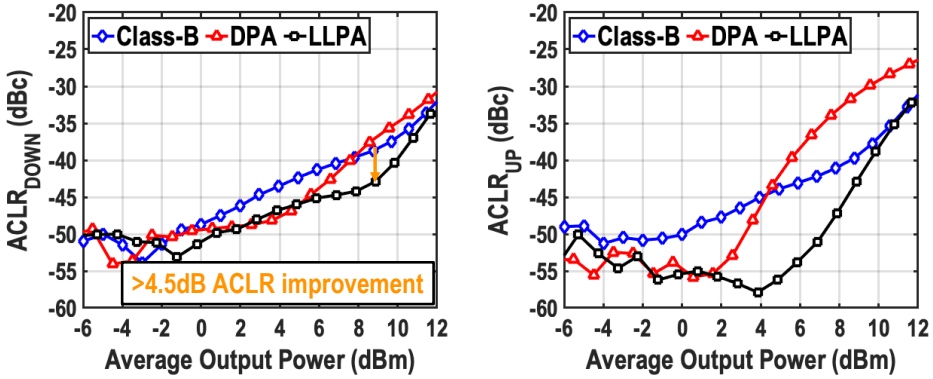


Figure 5.12: The measured $ACLR_{DOWN}$ (left) and $ACLR_{UP}$ (right) of a 50MHz 64-QAM OFDM versus P_{AVG}.

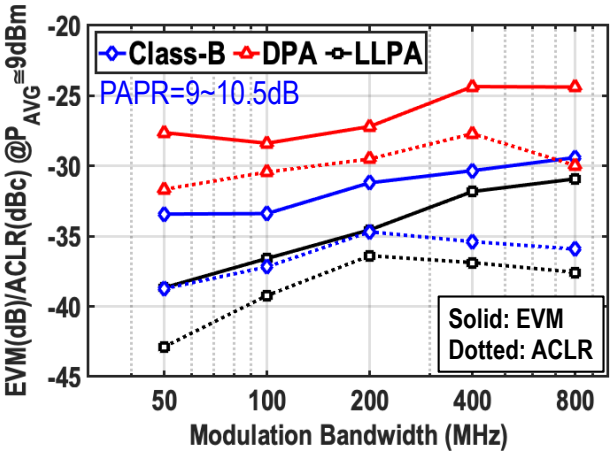


Figure 5.13: The measured EVM (solid) and ACLR (dotted) of the 64-QAM OFDM signals at 9dBm P_{AVG}.

exhibited in Fig. 5.12. Similar to EVM, the measured ACLR of LLPA is improved by 4.5dB and 11dB compared to that of class-B and DPA, respectively.

Moreover, the measured EVM and ACLR for various modulation bandwidths when P_{AVG}=9dBm are illustrated in Fig. 5.13. Since the IMD3 produced by g_{m3} and gain compression are static non-linearity, the proposed technique improves the EVM more effectively for the lower modulation bandwidths, where the dynamic non-idealities such as memory effect are not dominant. Nonetheless, the proposed LLPA offers better EVM and ACLR even at modulation bandwidth as high as 800MHz.

Furthermore, the measured P_{AVG} and average drain efficiency (η_{AVG}) are demonstrated for various modulation bandwidths when EVM=3% (Fig. 5.14). Note that EVM=3% is required for supporting a 256-QAM OFDM signal. The measurement shows that the proposed LLPA achieves the highest P_{AVG} and η_{AVG} for a specified EVM. Namely,

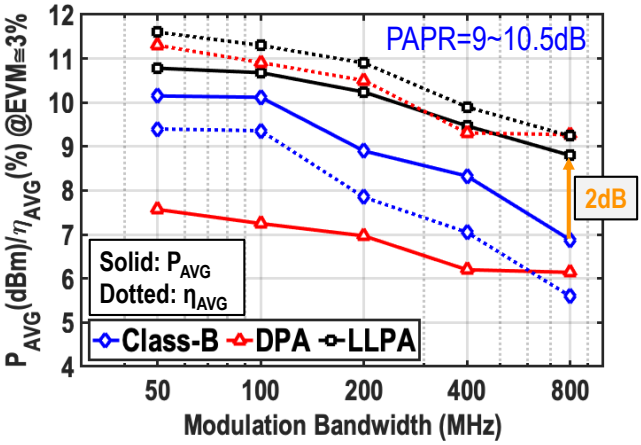


Figure 5.14: The measured P_{AVG} (solid) and η_{AVG} (dotted) when EVM=3% for 64-QAM OFDM signals.

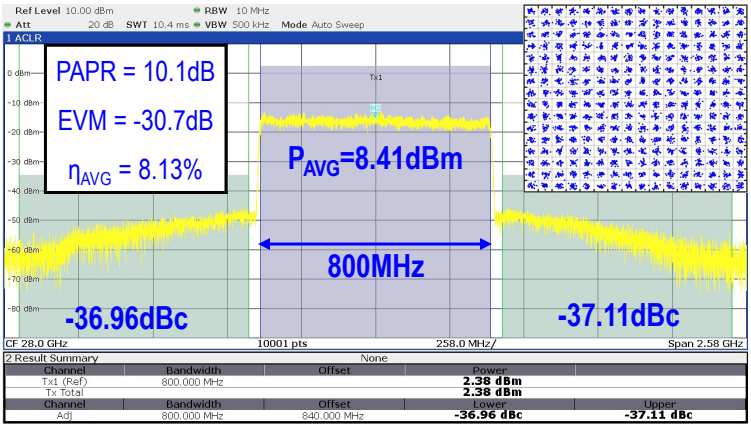


Figure 5.15: The measured spectrum and constellation of an 800MHz 256-QAM OFDM signal.

for the 800MHz modulated signal, LLPA offers 2dB higher P_{AVG} compared to the class-B configuration. Moreover, the measured spectrum and constellation of an 800MHz 256-QAM OFDM signal with 8.41dBm P_{AVG} is exhibited in Fig. 5.15, offering -30.7dB EVM and -37dBc ACLR. The state-of-the-art performance of our LLPA is summarized in Table 5.1 and compared to the prior art.

5.6. CONCLUSION

This chapter presents a load-modulation-based IMD3 cancellation technique for class-B CMOS PAs. It maintains the drain voltage swing at a region where the IMD3 component produced by gain compression cancels its counterpart generated by g_{m3}. The proposed solution is verified using a 28GHz 40nm CMOS series-Doherty balanced PA pro-

Table 5.1: CMOS mm-Wave Linear PAs Performance Comparison

	This work		Park IMS 2016 [2]	Vigilante RFIC 2017 [4]	Li IMS 2021 [6]	Ali ISSCC 2018 [9]	Choi LMWC 2020 [10]
Linearization Technique	Load-modulation-based IMD3 cancellation		2nd harmonic termination	Varactor-based AM-PM compensation	NMOS/PMOS power combining	Transformer based AM-PM correction	Three-stage antiphase
Technology	40nm CMOS		28nm CMOS	28nm CMOS	45nm SOI	65nm CMOS	65nm CMOS
Supply (V)	1		2.2	0.9	1.1	1.1	1
Freq. (GHz)	28		28	43	55	28	25
P_{SAT} (dBm)	20.1		19.8	16.6	16.3	15.6	17.3
η_{PEAK} (%)	40.6		43.3 (PAE)	24.2 (PAE)	35.4 (PAE)	41 (PAE)	32 (PAE)
Modulation scheme	64-QAM OFDM	256-QAM OFDM	64-QAM WLAN	64-QAM (at 34GHz)	64-QAM CP-OFDM	64-QAM	64-QAM WLAN
Modulation bandwidth (MHz)	50	800	80	675	800	340	20
PAPR (dB)	8.9	10.1	10.8	8.3	9.8	NR	10.55
EVM_{RMS} (dB)	-38.7 (1.2%)	-30.7 (2.92%)	-27.5	-25	-23.2	-26.4	-25
ACLR (dBc)	-42.9	-36.96	NR	-30.2	-26.4	-30	NR
P_{AVG} (dBm)	8.9	8.41	10.97	8.9	8	9.8	10.2
η_{AVG} (%)	9.46	8.13	17.3 (PAE)	4.4 (PAE)	8.1 (PAE)	18.2 (PAE)	6.8 (PAE)

totype. The experimental result demonstrates >10dB IMD3 improvement compared to a class-B PA. The measured EVM/ACLR of the proposed approach for a 50MHz 64-QAM OFDM signal with 8.9dBm average power are -38.7dB/-42.9dBc, respectively, which are 5.7dB/4.5dB better than the class-B configuration.

6

A CHAIN-WEAVER BALANCED POWER AMPLIFIER WITH AN EMBEDDED IMPEDANCE/POWER SENSOR

This chapter introduces an N-Way chain-weaver balanced power amplifier (PA) for millimeter-wave (mm-wave) phased-array transmitters (TXs). Taking advantage of the proposed combining network, an embedded impedance/power sensor is implemented, which can be utilized for output power regulation, built-in self-test, and load-based performance optimization. The proposed PA architecture offers linearity and gain robustness under the antenna's frequency/time-dependent voltage standing wave ratio (VSWR). In the event of impedance mismatch, the proposed PA provides N different loads equally distributed on the VSWR circle. Consequently, the performance of the PAs is the average of N PAs with N different loads, which makes this structure VSWR resilient. As a proof-of-concept, an eight-way chain-weaver balanced PA is realized in 40nm bulk CMOS technology, and it delivers 25.19dBm P_{SAT} with 16.19% PAE. The proposed PA supports a 2GHz 64-QAM OFDM signal with 16dBm average power, achieving -25dB error vector magnitude (EVM). The average EVM is better than -30.3dB without digital pre-distortion for an "800MHz 256-QAM OFDM" signal while generating an average output power of 12.17dBm. The performance of the PA is also evaluated under 1.5:1 to 3:1 VSWR conditions. The measured small-signal gain variation under VSWR 3:1 is ±0.7dB. Moreover, assuming any frequency/time-dependent loading condition within the VSWR 3:1 circle, the proposed chain-weaver BPA achieves <2.8° AM-PM over 3GHz bandwidth. Besides, the embedded impedance/power sensor accuracy outperforms the state-of-the-art. The proposed impedance sensor can measure VSWR 3:1 by maximum angle and magnitude errors of 12.3°and 0.106, respectively.

This chapter is based on the paper published in the IEEE Journal of Solid-State Circuits [138].

6.1. INTRODUCTION

Power amplifiers (PAs) are one of the crucial parts of the millimeter-wave (mm-wave) 5G transmitters (TXs), as they usually define the TX linearity, reliability, and efficiency. Taking advantage of the mm-wave phased-array architecture empowers 5G TXs to achieve the required equivalent isotropic radiated power (EIRP) with a reasonable average output power levels, e.g., 9dBm for backhaul and 15dBm for handset applications [18]. On the other hand, they typically employ spectrally efficient complex modulation schemes with high peak-to-average-power ratios (PAPRs), e.g., 11dB [4]. Besides, in the hybrid/analog beamforming architectures, the TX signal reaches the PA's input with a low power level due to losses of preceding stages, including power splitters and phase shifters [11]. Therefore, the PA must provide a high gain and peak output power to achieve the required average EIRP.

Moreover, the TX must satisfy the ever-tightening linearity specifications of the 5G systems, verified by the error vector magnitude (EVM). Among all noise and nonlinearity contributors of an mm-wave TX, the PA typically owns most of the EVM budget, as it must handle a large signal while directly interfacing with the antenna [88]. Hence, several mm-wave linear PAs have been introduced to address the 5G EVM specifications [25, 73–77, 118, 120–122, 124–126, 139–141]. Nevertheless, the critical challenge is achieving the required gain, power, and EVM and maintaining them over the voltage standing wave ratio (VSWR) provided by the antenna and its connection [8]. Fig. 6.1(a) exhibits the simulated gain variation of a single-branch PA ($\Gamma_{OUT} = -4dB$) for VSWR<3:1. It shows more than 5dB gain variation, while only 1.249dB comes from load mismatch loss ($1 - |\Gamma_L|^2$). Furthermore, assuming no memory effect, the EVM of a PA can be directly determined by its amplitude-to-amplitude (AM-AM) and amplitude-to-phase (AM-PM) distortions. Fig. 6.1(b) demonstrates the measured input 1dB compression point (iP_{1dB}) and AM-PM of a 40nm CMOS linear PA [142] at 28.5GHz under VSWR of 3:1. It shows more than 5dB iP_{1dB} variation over various VSWR angles, while its AM-PM at input power<iP_{1dB} fluctuates between -3.7° to 5°.

Since the mm-wave 5G TXs must support modulation bandwidths up to 1.4GHz, the antenna impedance can vary significantly over such a large bandwidth [143]. This dependency becomes more complex when considering a time-varying VSWR caused by the beam-angle-dependent element-to-element mutual coupling of the phased-array TX and environmental changes [19–21, 23, 144]. This time and frequency-dependent VSWR deteriorates PA gain-flatness, output 1dB compression point (oP_{1dB}), AM-AM, AM-PM, and reliability. The gain-flatness correction consumes the link budget, while the PA needs to be over-dimensioned to satisfy the required EIRP, linearity, and reliability over the signal bandwidth to handle the worst-case VSWR scenario.

Active load-pulling and reconfigurable matching networks are introduced to address the VSWR issue [48, 104, 106]. However, since the PA can be tuned only for a specific antenna impedance (i.e., at a chosen frequency), reconfigurable matching networks do not offer frequency-dependent VSWR compensation. A conventional solution for a VSWR-resilient PA is employing an isolator at its output. Unfortunately, due to the area constraint of the phased-array transceivers, an integrated isolator would not be a viable solution. Moreover, despite the development of integrated state-of-the-art mm-waves isolators [64, 65, 142], they yield area overhead, demonstrate high TX-to-antenna loss (>1.8

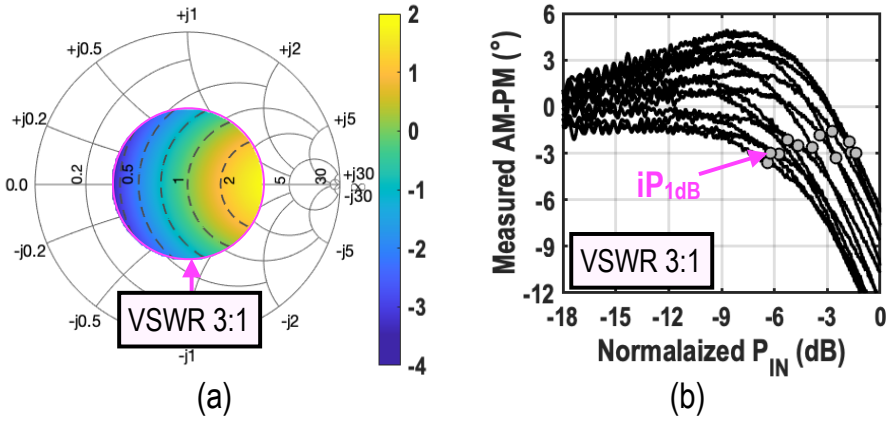


Figure 6.1: (a) The simulated gain variation of a single-branch PA with $\Gamma_{OUT} = -4dB$. (b) The measured iP_{1dB} and AM-PM of a 40nm CMOS linear PA [142] at 28.5GHz under VSWR of 3:1 with various VSWR angles.

dB), and require extra power consumption to generate their quadrature clocks. Additionally, a VSWR resilient impedance/power sensor is an essential part of such a PA to regulate gain, beam pattern, and EIRP [145–148].

On the other hand, balanced PAs (BPAs) provide inherent VSWR resilience by relying on the cancellation of the reflected wave [57]. This article introduces the chain-weaver balanced PA architecture [149] extending the conventional BPA's linearity, gain, and power resilience under a significant frequency and time-dependent VSWR. The proposed mm-wave PA features: 1) a four stages eight-way power combined Class-AB PA achieving high output power, gain, and linearity, 2) a chain-weaver balanced power combiner for VSWR resilience, and 3) an embedded impedance/power sensor.

This chapter is organized as follows. Section 6.2 discusses phased-array link system considerations and requirements for PA designing. The proposed chain-weaver BPA architecture is introduced in Section 6.3. Section 6.4 presents the proposed embedded impedance/power sensor. Section 6.5elaborates on circuit implementation details of the chain-weaver BPA prototype fabricated in the 40nm bulk CMOS technology. Section 6.6 presents the experimental results of the chain-weaver PA, while the measurement results of the impedance/power sensor are discussed in Section 6.7. Lastly, we conclude our work in Section 6.8.

6.2. SYSTEM CONSIDERATIONS AND REQUIREMENTS

In this Section, we discuss the PA design considerations when the optimization goal is the communication link power consumption, not PAE. Fig. 6.2(a) demonstrates a simplified phased-array link supporting up to 1.4GHz modulation bandwidth as the front-end component in the TX beamforming IC, the PAs face the impedance presented by the antenna arrays. As depicted, due to different connection lengths, the PAs see unequal frequency-dependent load impedance and connection loss. Additionally, the beam-angle-dependent element-to-element mutual coupling adds a time-dependent factor to the VSWR experienced by the PAs. Furthermore, human body proximity and environ-

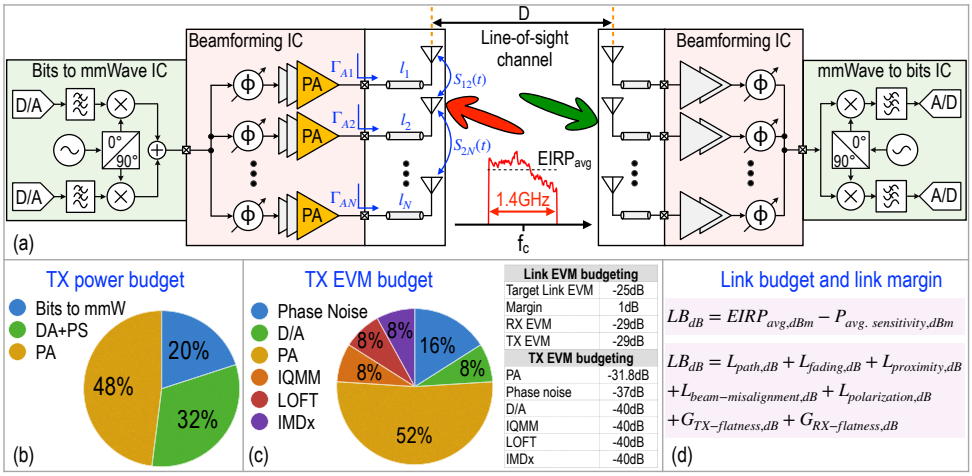


Figure 6.2: (a) A simplified phased-array link supporting up to 1.4GHz modulation bandwidth. The PAs share TX's (b) power and (c) EVM budgets. (d) Link budget calculation taking into account the TX/RX gain flatness.

mental changes, although at a lower rate, affect the impedance seen by the PAs.

As depicted in Fig. 6.1, VSWR variation influences the gain, output compression power levels, and linearity. Therefore, frequency-dependent VSWR leads to gain, power, and EVM deviation over frequency within the modulation bandwidth. This imposes many design challenges through the link and increases total power consumption. For instance, the PA must deliver an average output power (P_{AVG}) to support the specified EIRP. Hence, the required peak power (P_{Peak}) in the presence of VSWR can be calculated as

$$P_{Peak} = P_{AVG} + PAPR + \Delta P, \tag{6.1}$$

where ΔP represents the difference between the worst-case (wc) and 50Ω peak power ($P_{Peak-wc} - P_{Peak-50\Omega}$) for all possible VSWR condition. Assuming an ideal class B PA, $\Delta P = 1dB$ degrades the average PAE by ×0.8. Fig. 6.2(b) depicts an example power consumption budget of a phased-array TX, introducing the PAs as the dominant power consumer. This power consumption budget is estimated based on information reported in [150–152], assuming beam-forming IC consists of 16 beam-forming elements and PAs can deliver 20dBm peak power with 30% efficiency with a class-B-like efficiency curve. Although a highly efficient PA architecture can optimize the power budget [59, 60, 153–155], a VSWR-resilient PA will prevent the need for over-designing, yielding a reduced power consumption.

In general, EVM budgeting can significantly affect the power consumption budget, thus the total power consumption. Eq.6.2 can estimate the overall EVM of the TX

$$EVM_{TX} = \sqrt{EVM_{D/A}^2 + EVM_{UC}^2 + EVM_{IMDx}^2 + EVM_{PA}^2}, \tag{6.2}$$

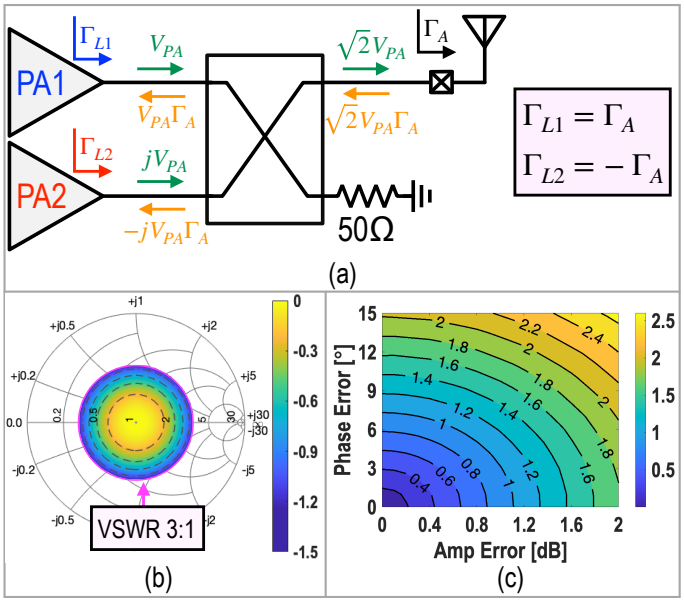


Figure 6.3: (a) The simplified block diagram of the balanced PA and its forward and reflected waves assuming matched PA units ($\Gamma_{PA} = 0$). (b) Gain of the balanced PA assuming ideal QHC. (c) gain variation of the balanced PA over VSWR 3:1 circle versus amplitude and phase error of the QHC.

and

$$EVM_{UC} = \sqrt{EVM_{P.N}^2 + EVM_{IQMM}^2 + EVM_{LOFT}^2}, \tag{6.3}$$

where $EVM_{D/A}$, EVM_{UC}, EVM_{IMDx}, and EVM_{PA} are the EVM degraded by quantization noise, up-conversion, odd/even order distortions, and the PA non-linearity, respectively. Also, the up-conversion EVM contribution includes $EVM_{P.N.}$, EVM_{IQMM}, EVM_{LOFT}, which are contributions of phase noise, I/Q modulation imbalance (IQMM), and LO feed through (LOFT), respectively.

Targeting -25dB EVM with 1dB margin and assuming an equal contribution for RX and TX, Fig. 6.2(c) exhibits a simplified EVM budget example of the TX calculated based on performance reported in [150–152, 156–158]. Here, we assume -37dB phase noise contribution and -40dB for IQMM, LOFT, quantization noise, and odd/even order distortions. The most significant portion of the TX EVM budget is given to the PA as it usually bottlenecks in TX's linearity and power consumption. Furthermore, as shown in Fig. 6.1(b), VSWR significantly influences PA EVM. This feature enforces the choice of less efficient PA operation, exploiting more linear biasing conditions and over-designing. Additionally, the PA might require a larger EVM budget, thus tightening the other blocks' linearity specifications and increasing the total power consumption.

Lastly, the link budget calculation is presented in Fig. 6.2(d), considering the TX/RX gain flatness. The frequency-dependent VSWR results in a frequency-dependent gain and EVM, which requires a higher EVM to satisfy the link budget. Therefore, over-designing at the link level is typically essential to address the required link budget,

imposing higher link power consumption.

6.3. CHAIN-WEAVER BALANCED POWER AMPLIFIER

This section discusses an N-way combining solution that can provide inherent resilience against frequency and time-dependent VSWR.

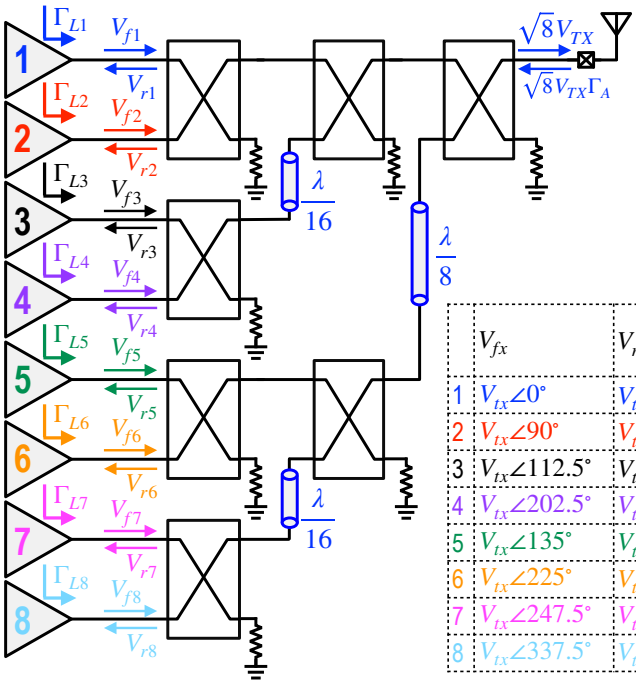
6.3.1. CONVENTIONAL BALANCED PA

Balanced PAs (BPAs) provide inherent VSWR resilience by relying on the cancellation of the reflected wave [67, 68, 88, 159]. It consists of two PAs combined by an isolated quadrature combiner. The quadrature combiner can be implemented with a 2-to-1 Wilkinson power combiner, where one of the PAs is connected to the combiner by a $\lambda/4$ transmission line (TLs) [159]. An alternative quadrature combiner is, as depicted in Fig. 6.3(a), a quadrature-hybrid coupler (QHC). The forward and reflected waves shown in Fig. 6.3(a) imply the reflection coefficient seen by the PAs is 180 degrees out of phase. Here, the PAs are considered as matched ports for simplification. Therefore, any reflected waves from the antenna do not influence the forward power of the PAs and, consequently, that of the BPA. Nonetheless, as discussed in [88], the BPA provides broadband output matching independent from PAs' impedance. This output matching alleviates the gain variation under the frequency-dependent VSWR. In Fig. 6.3(b), the gain variation of a BPA under VSWR is demonstrated, which is only <1.249dB due to mismatch loss of the antenna ($1\text{-}|\Gamma|^2$). However, as shown in Fig. 6.3(c), the gain deviation of the BPA over a VSWR circle heavily depends on the QHC amplitude and phase error.

6.3.2. CHAIN-WEAVER BALANCED PA

Moving on a VSWR circle with 1° increment, a single-branch PA sees 360 different loading conditions leading to performance variation. BPA, on the other hand, provides 180 different loading conditions for its PAs as one sees the inverted load of the other. Additionally, in this 180 loading condition, the overall performance is the average of two PAs with opposite loads, leading to a more robust performance over VSWR angles. To further extend the VSWR resilience of the BPA, we proposed the chain-weaver BPA. The goal is to introduce an N-way power combiner, which offers $\frac{360}{N}$ different loading conditions for N PAs.

The proposed N-way chain-weaver BPA is demonstrated in Fig. 6.4, where N=8. The chain-weaver BPA consists of eight equally weighted PAs combined in three stages. In the first stage, four QHCs are employed as 2-to-1 isolated quadrature power combiners, where two $\lambda/16$ TLs are added to the output of two of them, providing 22.5° phase shift for both forwards and reflected signals. The second stage comprises two QHCs and one $\lambda/8$ TL at the output of one of them for a 45° phase shift. Lastly, the third stage is a QHC directly connected to the antenna port. In this combining structure, the $\lambda/16$ and $\lambda/8$ TLs provide a unique phase shift, with a 22.5° increment, from each PA to the antenna port. As presented in Fig. 6.4, these unique phase shifts must be included in the forward signals for combining constructively at the antenna port. In the antenna load mismatch event, the reflected wave from the antenna travels back and reaches each PA with the



	V_{fx}	V_{rx}	$\Gamma_{Lx} = \frac{V_{rx}}{V_{fx}}$
1	$V_{tx}\angle 0°$	$V_{tx}\Gamma_A\angle 0°$	$\Gamma_A\angle 0°$
2	$V_{tx}\angle 90°$	$V_{tx}\Gamma_A\angle -90°$	$\Gamma_A\angle -180°$
3	$V_{tx}\angle 112.5°$	$V_{tx}\Gamma_A\angle -112.5°$	$\Gamma_A\angle -225°$
4	$V_{tx}\angle 202.5°$	$V_{tx}\Gamma_A\angle -202.5°$	$\Gamma_A\angle -45°$
5	$V_{tx}\angle 135°$	$V_{tx}\Gamma_A\angle -135°$	$\Gamma_A\angle 90°$
6	$V_{tx}\angle 225°$	$V_{tx}\Gamma_A\angle -225°$	$\Gamma_A\angle -90°$
7	$V_{tx}\angle 247.5°$	$V_{tx}\Gamma_A\angle -247.5°$	$\Gamma_A\angle -135°$
8	$V_{tx}\angle 337.5°$	$V_{tx}\Gamma_A\angle -337.5°$	$\Gamma_A\angle 45°$

Figure 6.4: The simplified block diagram of an eight-way balanced PA and its forward and reflected waves assuming matched PA units ($\Gamma_{PA} = 0$).

same phase shift. Since the combining gain from the PAs to the antenna is identical, all PAs see the same reflection coefficient magnitude. However, owing to the phase shift with a 22.5° increment, the reflection coefficient seen by each PA has a unique angle with a $\frac{360°}{8} = 45°$ increment as depicted in Fig. 6.4. Therefore, assuming lossless QHCs, this structure distributes the PAs' load like a chain-dotted circle on the VSWR circle with a 45° distance.

Fig. 6.5 demonstrates the loading conditions for VSWR 3:1 and three VSWR angles. In a conventional BPA, the PAs experience both the actual and inverted antenna impedance. Still, the loading conditions are different in these three VSWR angles, leading to linearity degradation. In the proposed chain-weaver BPA, however, only the places of the PAs are shifted in the chain-dotted circle, resulting in the same overall loading conditions. As such, assuming identical unit PAs, the gain, oP_{1dB}, and linearity of the overall structure are equal for these three VSWR angles.

Thus far, the PAs are considered an ideal matched signal port with fixed forward power for simplification. However, as discussed in [88], the impedance seen by the PAs is a function of their impedance. Assuming Γ_{PA} and Γ_A as the reflection coefficient of

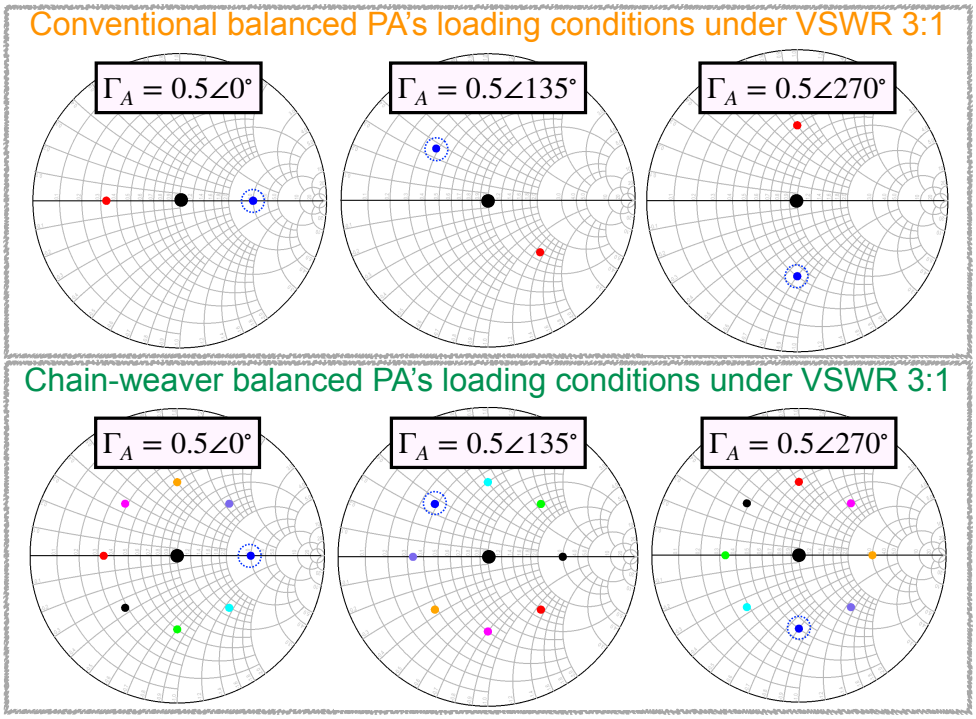


Figure 6.5: Loading condition of the conventional balanced PA and eighth-way chain weaver PA under VSWR 3:1.

the PAs and antenna, respectively, the load seen by eight PAs are as follows

$$\begin{aligned}
\Gamma_{L1} &= \frac{\Gamma_A\angle 0°}{1+\Gamma_{PA}\Gamma_A\angle 0°}, \Gamma_{L2} = \frac{\Gamma_A\angle -180°}{1+\Gamma_{PA}\Gamma_A\angle -180°}, \\
\Gamma_{L3} &= \frac{\Gamma_A\angle -225°}{1+\Gamma_{PA}\Gamma_A\angle -225°}, \Gamma_{L4} = \frac{\Gamma_A\angle -45°}{1+\Gamma_{PA}\Gamma_A\angle -45°}, \\
\Gamma_{L5} &= \frac{\Gamma_A\angle -270°}{1+\Gamma_{PA}\Gamma_A\angle -270°}, \Gamma_{L6} = \frac{\Gamma_A\angle -90°}{1+\Gamma_{PA}\Gamma_A\angle -90°}, \\
\Gamma_{L7} &= \frac{\Gamma_A\angle -135°}{1+\Gamma_{PA}\Gamma_A\angle -135°}, \Gamma_{L8} = \frac{\Gamma_A\angle -335°}{1+\Gamma_{PA}\Gamma_A\angle -335°}.
\end{aligned} \tag{6.4}$$

Moreover, since the PAs are not matched, the reflected signal from the antenna will reflect and, eventually, in the steady state, will be absorbed in the first stage QHCs' termination resistor. The absorbed signal's magnitude (V_{term}) can be calculated as

$$V_{term} = \sqrt{2}V_{tx}|\Gamma_A||IL_t|^2|IL_{QHC1}||\Gamma_{PA}|, \tag{6.5}$$

where IL_t and IL_{QHC1} are the total insertion loss of the chain-weaver power combiner and the insertion loss of the first stage's QHC, respectively. Therefore, these four termination resistors' reliability criteria must be satisfied for the maximum possible VSWR. As

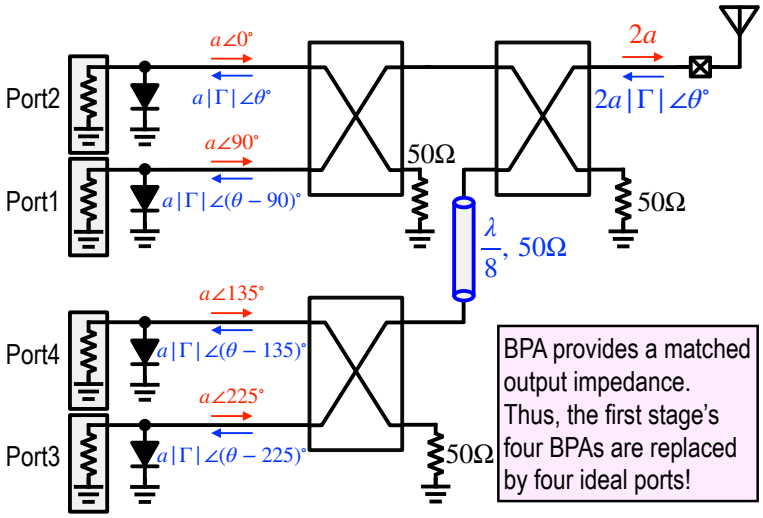


Figure 6.6: The simplified schematic of the embedded VSWR resilient impedance/power sensor.

6

the first stage provides matched output, thus completely absorbing the reflected power, the second and third-stage termination resistors' signal is zero. However, this is only true when assuming no in-phase quadrature mismatch (IQMM) for the QHCs. In practice, even with the matched load, part of the power will be directed to the termination resistors due to the IQMM, which is discussed in Section 6.9.

Note that a four-way Wilkinson-based power combiner/splitter with a phase shift of 45° increment is implemented in [159]. However, it is not easily scalable due to its unbalanced and asymmetrical structure.

6.4. EMBEDDED IMPEDANCE/POWER SENSOR

Fig. 6.6 unveils the simplified schematic of the embedded VSWR resilient impedance/power sensor. Since the first stage BPAs' output impedance is matched to the characteristic impedance of its QHC (Z_0=50Ω) [88], the first stage's BPAs are considered ideal power ports. It means that the forward wave at each port is independent of the reflected wave. As shown, an RMS or peak detector can be used at each port to measure the combined voltage of the forward (V_f) and reflected (V_r) waves ($V_i^2 = |V_f + V_r|^2$). Since the port impedance and the characteristic impedance of the following QHC are 50Ω, the combined voltage represents the combined power accordingly. Assuming an antenna reflection coefficient with magnitude and angle of $|\Gamma|$ and θ, respectively, and lossless QHCs and TL, the forward and reflected waves at four ports are presented in Fig. 6.6.

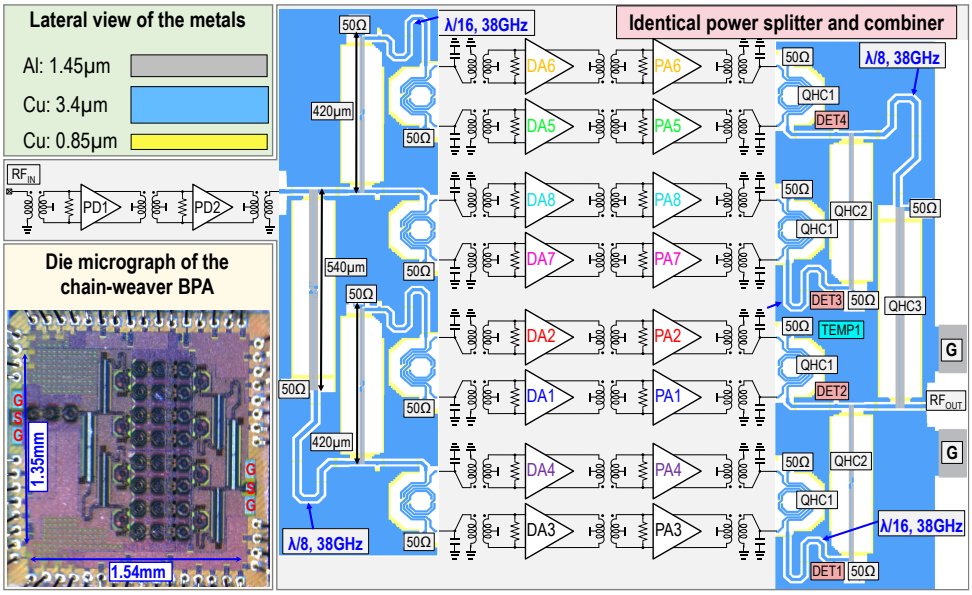


Figure 6.7: A detailed schematic and die photo of the proposed eight-way chain-weaver balanced PA.

Hence, the voltage at each port can be calculated as follows

$$\begin{aligned} V_1^2 &= a^2(1+|\Gamma|^2-2|\Gamma|\cos\theta),\\ V_2^2 &= a^2(1+|\Gamma|^2+2|\Gamma|\cos\theta),\\ V_3^2 &= a^2(1+|\Gamma|^2-2|\Gamma|\sin\theta),\\ V_4^2 &= a^2(1+|\Gamma|^2+2|\Gamma|\sin\theta). \end{aligned} \tag{6.6}$$

Please note that in the conventional BPA, due to the 90° phase increment, only two of the above equations, V_1^2 and V_2^2, can be achieved, which is not sufficient for calculating impedance and power. Thanks to the chain-weaver BPA's $\lambda/8$ TL, four equations are available to calculate three unknown parameters ($|\Gamma|$, θ, and a). Although only three equations are required to calculate the unknown variables, we would calculate the impedance and power using all four voltages to minimize the effect of limited accuracy and dynamic range of the utilized RMS or peak detectors. Therefore, assuming lossless passives, the angle and magnitude of the antenna can be calculated as

$$\theta = \tan^{-1}\frac{V_3^2-V_4^2}{V_2^2-V_1^2} \tag{6.7}$$

$$|\Gamma| = \frac{V_1^2+V_2^2}{V_1^2-V_2^2}\cos\theta - \sqrt{\left(\frac{V_1^2+V_2^2}{V_1^2-V_2^2}\cos\theta\right)^2-1}. \tag{6.8}$$

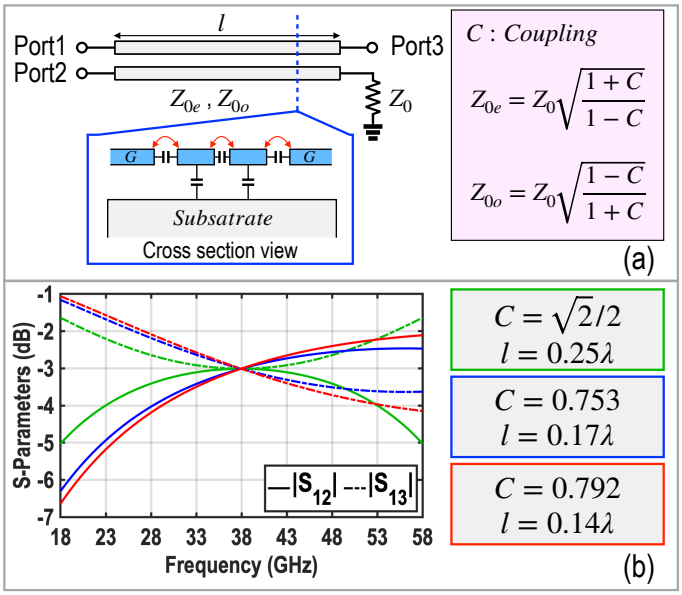


Figure 6.8: (a) The coupled-line-based QHC and its cross-section view. (b) The simulated $|S_{12}|$ and $|S_{13}|$ of the coupled-line-based QHCs with different couplings.

Additionally, the delivered power to the antenna can be expressed as

$$P_{Sense} = \frac{(1-|\Gamma|^2)2a^2}{Z_0} = \frac{1-|\Gamma|^2}{1+|\Gamma|^2}\sum_{i=1}^{4} V_i^2. \tag{6.9}$$

Thus far, the passives are considered ideal and lossless. However, the loss of the QHCs and the TL, as well as the magnitude and phase deviation of these four combining paths, affect the accuracy of the calculation. For instance, the reflected wave at the port can be derived as

$$V_{r1} = (\sum_{i=1}^{4} V_{fi}S_{5i})S_{15}|\Gamma|\angle\theta, \tag{6.10}$$

where V_{fi} is the forward wave of port i, and S_{ji} represents the scattering parameters assuming the antenna as the fifth port. In this work, we assume an equal insertion loss in four combining paths without any magnitude and phase mismatch within them. Therefore, we use Eq. (6.7), Eq. (6.8), and Eq. (6.9) to calculate the antenna impedance and output power and apply a constant coefficient correction factor for taking into account the insertion loss. This further implies that using all four equations of Eq. (6.6) can alleviate the inaccuracies.

6.5. CIRCUIT IMPLEMENTATION

The proposed eight-way chain-weaver BPA is realized in 40nm bulk CMOS technology by occupying 2.08mm^2 core area. Fig. 6.7 demonstrates a detailed schematic view and

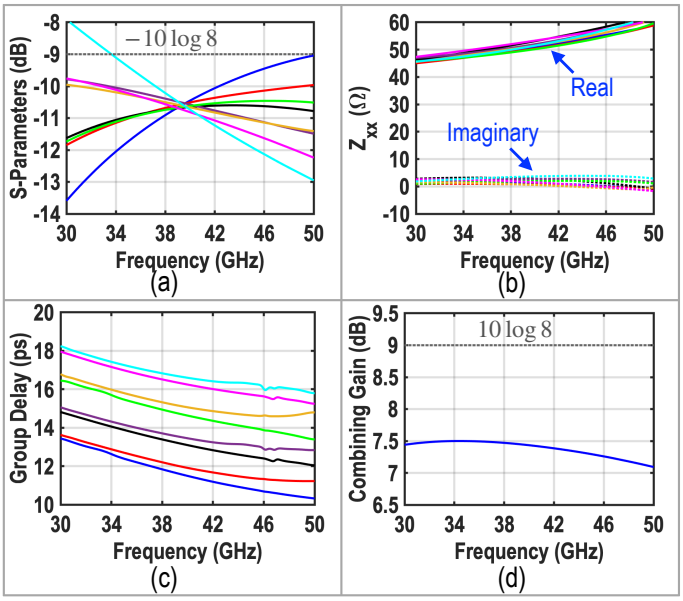


Figure 6.9: (a) The simulated s-parameter components ($|S_{9n}|$) of the output (Port9) to each PAs (Port1-to-8). (b) The real and imaginary part of the impedance seen by the PAs versus carrier frequency. (c) Simulated group delay from each PA to the output. (d) The combining gain of the proposed 8-to-1 power combiner. The output balun loss of the PAs is excluded in these simulation results.

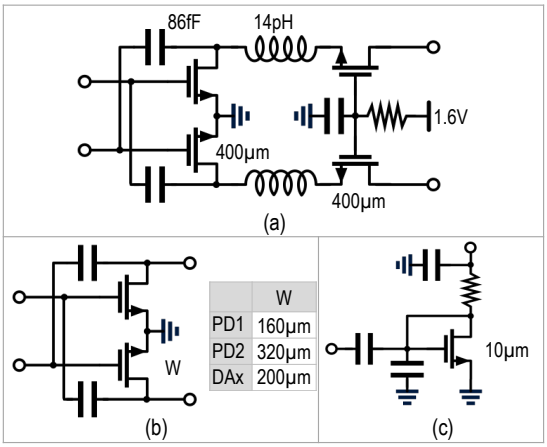


Figure 6.10: The schematic of (a) the PA, (b) the driving amplifier and pre-drivers, and (c) the RMS detector.

the die micrograph of the proposed chain-weaver BPA. Starting from the RF_{IN} port, two common-source pre-drivers (PDs) stages are employed to deliver the required high-power gain. Then, the amplified signal is split by a 1-to-8 splitter, a 180° rotated version of the output power combiner. The first stage of the 8-to-1 chain-weaver

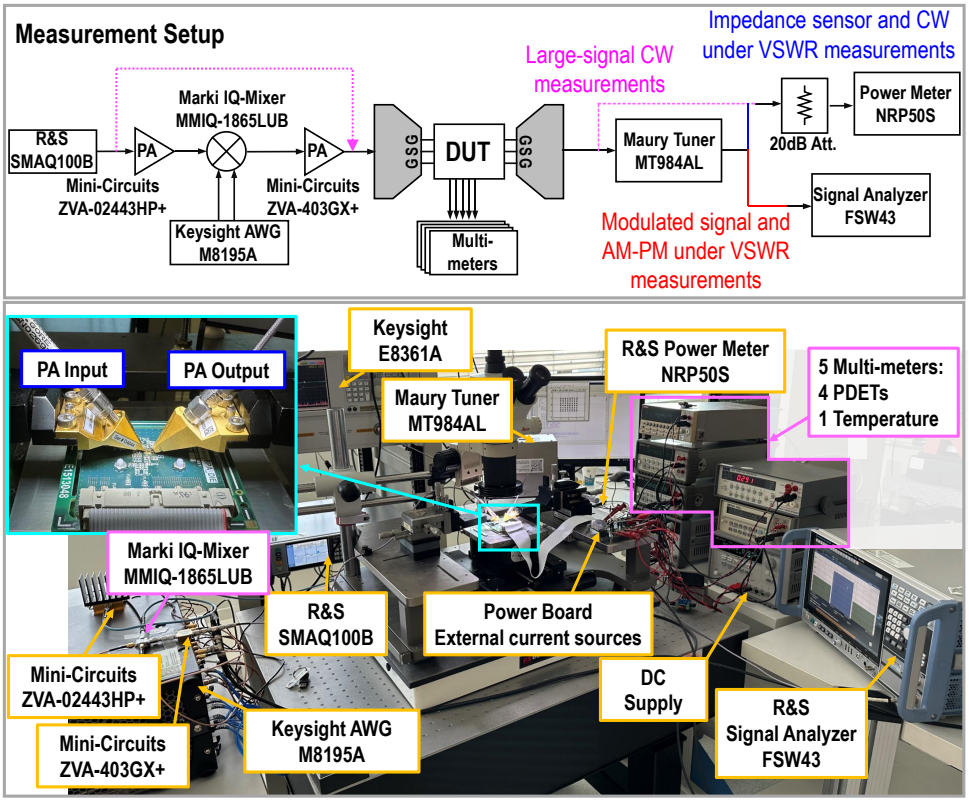


Figure 6.11: Simplified CW and modulation measurement setups.

combiner comprises four identical QHCs (QHC1), forming four balanced PAs. QHC1 is implemented by a compact transformer-based structure for tight floor planning [88]. Besides, two $\lambda/16$ coplanar TLs connect the second and fourth QHCs' output to the second combining stage, forming the required 22.5° phase shift. Here, the reflection wave is absorbed in the termination resistors of the first stages' QHCs. As such, their reliability for the worst-case VSWR condition must be satisfied for a maximum value achieved from (6.5).

The second stage consists of two coupled-line QHCs (QHC2) and a $\lambda/8$ coplanar TL for 45° phase shifting. The last stage is another coupled-line QHC (QHC3) directly connected to the antenna port. Fig. 6.8(a) a coupled-line QHC and its simplified cross-section view. The even (Z_{0e}) and odd (Z_{0o}) impedance of the coupled line must satisfy the shown equations for the desired coupling (C) and characteristic impedance Z_0. A $\lambda/4$ coupled-coupled line with $C = \sqrt{2}/2$ is considered as a conventional coupled-line QHC. However, as depicted in Fig. 6.8(b), a higher coupling factor can be employed to decrease the required length in the cost of bandwidth. QHC2 is implemented with 5μm and 1μm spacing to maximize the coupling (0.792), thus minimizing the length (420μm).

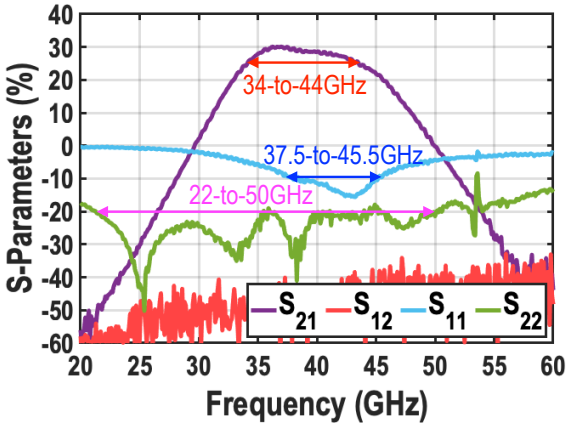


Figure 6.12: S-parameter measurement results of the proposed chain-weaver balanced PA.

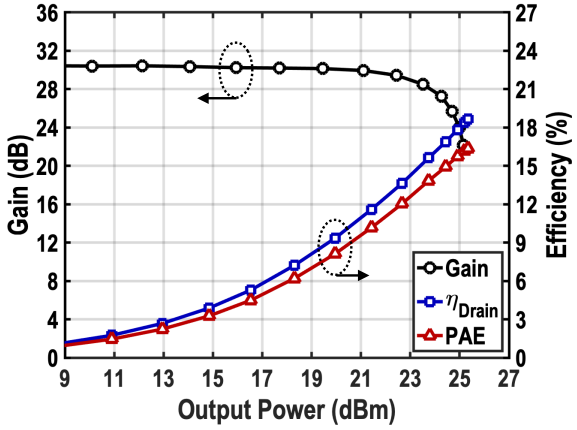


Figure 6.13: Large-signal CW measurement results at 37GHz.

Even though the aluminum layer is used to increase the current handling of the QHCs, a wider width (10μm) is chosen for the last QHC to address the reliability of the peak current at the worst-case VSWR. This feature leads to a lower coupling (0.753) and, thus, a longer length (540μm) than QHC2.

Fig. 6.9 exhibits the simulated performance of the proposed 8-to-1 power combiner excluding the Baluns. The S-parameter components of the output to each PA are demonstrated in Fig. 6.9(a). Since the characteristic impedance of all QHCs and TLs are 50Ω, assuming a 50Ω output load, the combiner provides a broadband 50Ω loading condition for the PAs as shown in Fig. 6.9(b). Moreover, the simulated group delay from each PA to the output is plotted in Fig. 6.9(c). Since QHC as a 2-to-1 combiner has an identical group delay, the pairs connected to the QHC1s have almost equal group delay. The group delay is separated by almost 1.64ps, equal to 22.5° phase shift at 38GHz. Lastly, the

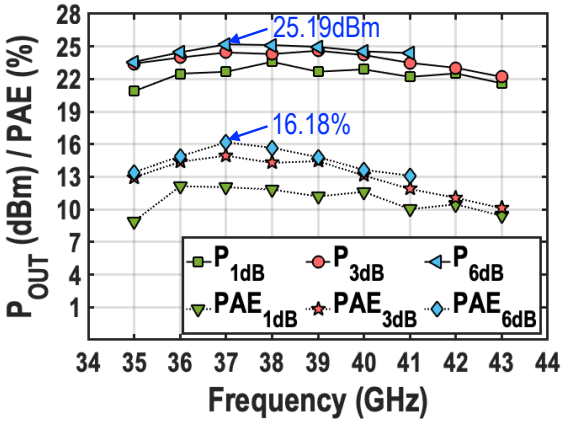


Figure 6.14: The measured output power and PAE at 1dB, 3dB, and 6dB compression point.

combining gain of the proposed 8-to-1 power combiner is depicted in Fig. 6.9(d), which is 1.5-1.9dB less than $10\log 8$.

The eight PA units comprise a common-source drive amplifier (DA) and a cascode PA. As shown in Fig. 6.10(a), two series inductors (14pH) are utilized to improve PAE and gain [72]. Additionally, the common-source pair is neutralized in all amplifiers to improve odd mode stability and boost power gain (see Fig. 6.10(b)). Also, double-tuned transformers are designed as input, inter-stage, and output-matching networks to cover the targeted bandwidth. Also, four RMS detectors (DETs) are employed at the input of the second stage for impedance/power sensing. As depicted in Fig. 6.10(c), each DET comprises a capacitive coupler and a diode-connected NMOS biased at the weak inversion region with an external current source [69, 86].

6.6. MEASUREMENTS OF THE CHAIN-WEAVER BALANCED PA

All measurements are performed using a high-frequency probe station. The DC supplies, bias voltages, and RMS detector pads are wire-bonded directly to an FR4 printed circuit board (PCB). Fig. 6.11 exhibits the continuous wave (CW) and modulated signal measurement setups. In this work, 2V supply voltage is used for the PAs and 1V for the driver and pre-driver amplifiers. A Maury MT984AL load tuner is used for the VSWR measurement. The tuner is characterized at the tip of the probe. The insertion losses of the probes, cables, and the directional coupler are measured and de-embedded. The tuner loss variation as a function of VSWR at all operating frequencies is extracted and de-embedded.

6.6.1. 50Ω LOAD MEASUREMENTS

The small-signal S-parameter performance is measured using the Keysight E8361A network analyzer. As Fig. 6.12 demonstrates, the PA achieves 10 GHz small-signal BW_{3dB}, while its S_{22} is better than -20dB in the 22-to-50GHz band. The PA offers 29.9dB small-signal gain at 37 GHz.

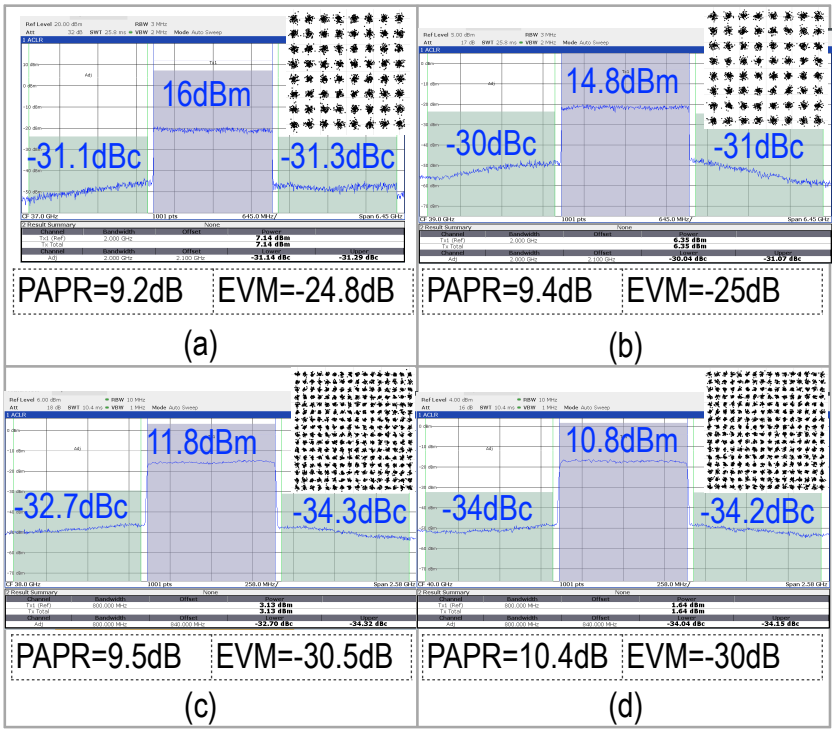


Figure 6.15: The measured constellation and spectra of a 64-QAM OFDM signal with 2GHz modulation bandwidth at (a) 37GHz and (b) 39GHz. Also, the measured constellation and spectrum of a 256-QAM OFDM signal with 800MHz modulation bandwidth at (c) 38GHz and (d) 40GHz.

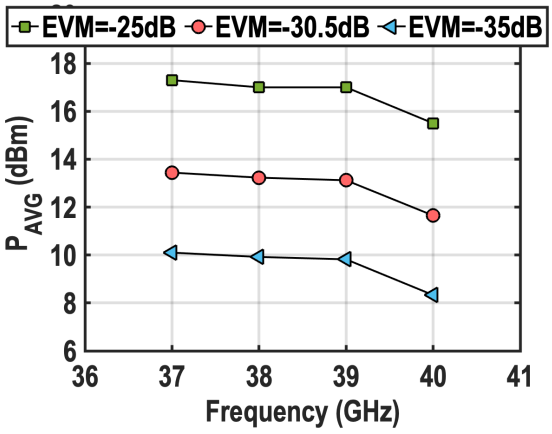


Figure 6.16: The average power of a 64-QAM OFDM signal with 100MHz modulation bandwidth versus carrier frequency when the measured EVMs are -25dB, -30.5dB, and -35 dB.

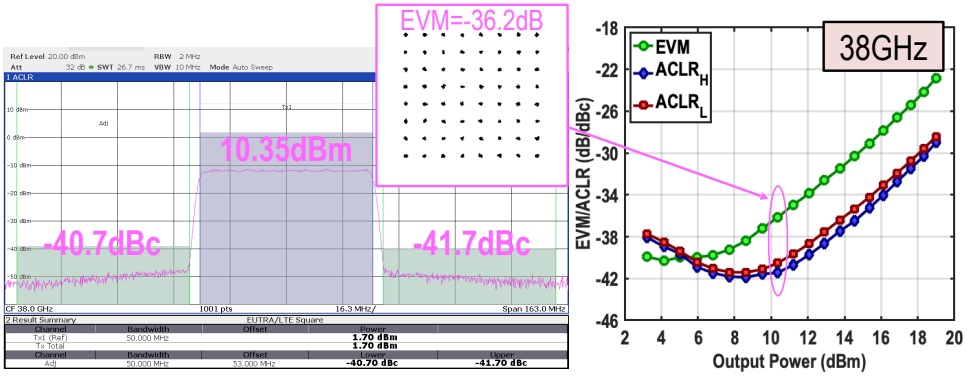


Figure 6.17: Measured EVM/ACLRs versus average power at 38 GHz for a 50MHz 64-QAM OFDM signal.

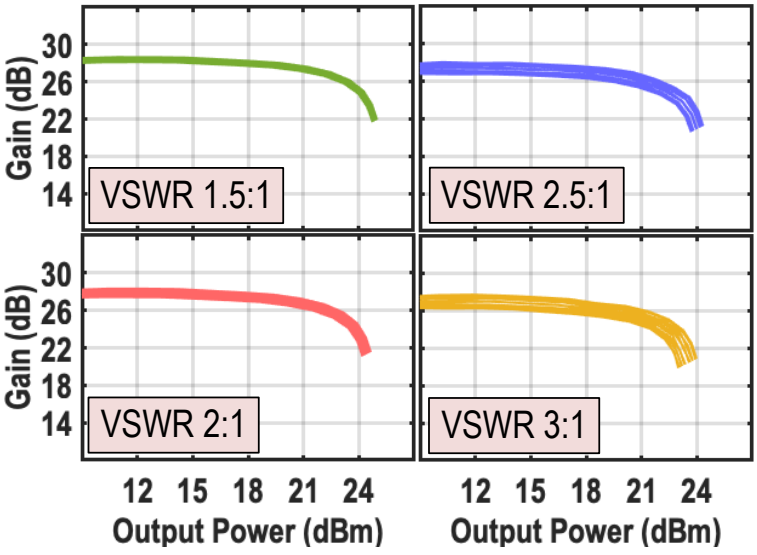


Figure 6.18: The measured gain versus output power under VSWR at 37GHz.

The large signal CW measurement results at 37GHz are reported in Fig. 6.13, where the PA achieves a saturated power of 25.19dBm and PAE of 16.18%. Moreover, as shown in Fig. 6.14, the PA provides more than 22 dBm P_{1dB} over the 36-to-42GHz band.

Wideband modulated signals such as "64-QAM OFDM" and "256-QAM OFDM" verify the PA dynamic performance. Fig. 6.15(a-b) exhibit measured constellations and spectrums of a 2 GHz "64-QAM OFDM" signal at 37 GHz and 39 GHz carrier frequencies. Without digital pre-distortion (DPD), the PA achieves almost -25 dB EVM with 16dBm and 14.8dBm average power at 37GHz and 39GHz, respectively. The PA supports 800MHz "256-QAM OFDM" signals with EVM≅-30.5dB and average output powers of

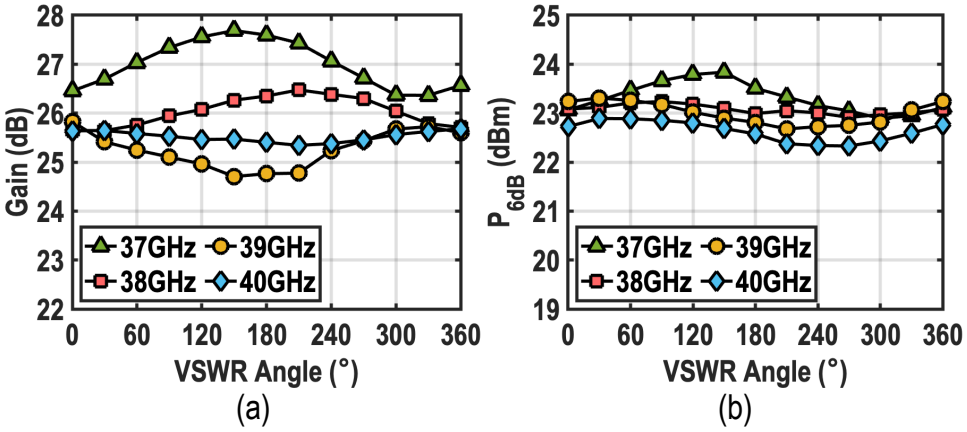


Figure 6.19: (a) gain and (b) saturated power variation under VSWR 3:1.

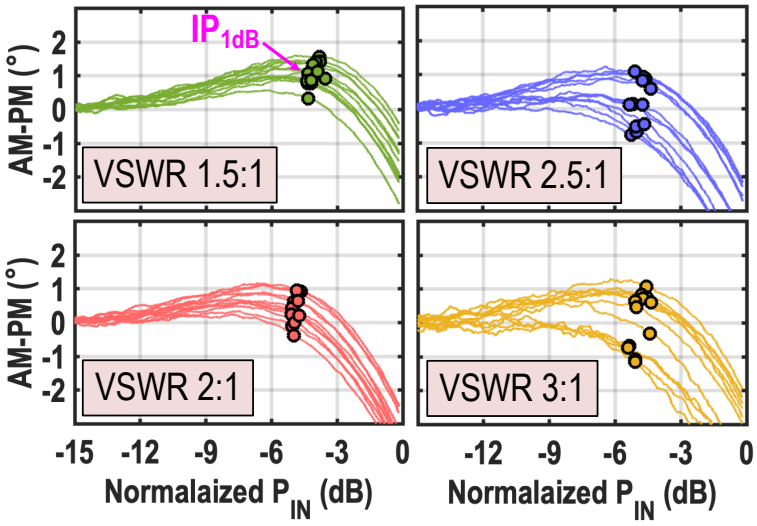


Figure 6.20: The measured AM-PM versus output power under VSWR at 37GHz.

11.8dBm and 10.8dBm at 38GHz and 40GHz, respectively.

The average power of a 100MHz "64-QAM OFDM" signal versus carrier frequency is shown in Fig. 6.16 for EVM of -25dB, -30.5dB, and -35 dB. Besides, Fig. 6.17 demonstrates the measured EVM/ACLRs of a 50MHz "64-QAM OFDM" signal versus the average power at 38 GHz.

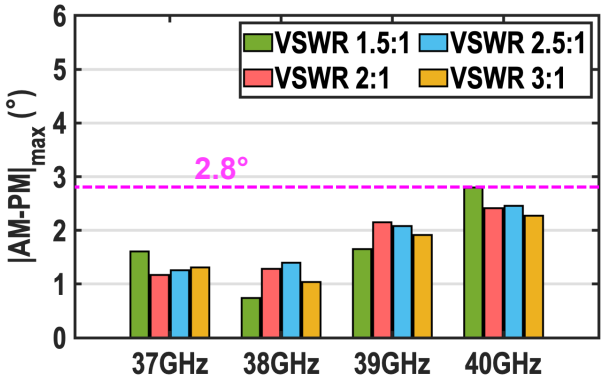


Figure 6.21: The measured AM-PM deviation under VSWR 1.5:1 to 3:1 in the 37-to-40GHz band.

Table 6.1: Silicon-Based mm-Wave PAs Performance Comparison

			Mm-Wave 5G PAs				Efficiency Enhanced PAs/TXs				
Parameter	**This Work**		Zeng ISSCC 2023	Wang ISSCC 2020	Ahn RFIC 2020	Dasgupta RFIC 2019	Qunaj ISSCC 2021	Pashaeifar JSSC 2021	Mannem ISSCC 2020	Chappidi VLSI 19	Zhu ISSCC 2024
Architecture	**Chain-Weaver Eight-Way Balanced PA**		Two-Stage PA with Feedback Linearity	Compensated Distributed Balun	Eight-Way Power Combiner	Four-way DAT based Combiner	Doherty-Like LMBA	TX with Doherty Balanced PA	Reconfigurable Doherty PA	Broadband Doherty PA	Seven-Way LMBA
Technology	**40nm CMOS**		28nm CMOS	45nm SOI	65nm CMOS	65nm CMOS	28nm CMOS	40nm CMOS	45nm SOI	65nm CMOS	65nm CMOS
Core Area (mm^2)	**2.08**		106	0.21	0.25	0.945	1.44 (Die size)	1.38	1.18	1.35 (Die size)	2.2
Supply (V)	**1 (PDs + DA), 2 (PA)**		0.9, 1.8	2	NR	2.2	1	1	1, 2	1.1	1
Frequency (GHz)	**35 to 43**		19.7 to 43.8	25.8 to 43.4	28	39	36	24 to 30	39	26 to 42	27.8 to 38.3
Gain (dB)	**29.9 (37GHz)**		20.5	18.9 (37GHz)	15.9	38	18	21.8 (TX gain)	12.4*	13.5*	16.1 (38GHz)
P_{1dB} (dBm)	**22.67 (37GHz)**		17.6 (37GHz)	18.9 (37GHz)	22	21.5	19.6	20	20.2	19.2 (33GHz)	20 (38GHz)
P_{sat} (dBm)	**25.19 (37GHz)**		19.3 (37GHz)	20 (37GHz)	23.2	26	22.6	NA	20.8	19.6 (33GHz)	24.1 (38GHz)
PAEsat (%)	**16.18 (37GHz)**		27	38.7 (37GHz)	33.5	26.6	32	31	33.3	24 (33GHz)	28.8 (38GHz)
S22 (dB)	**<-20**		-3.5~-4*	-1*	-5.8	-19*	-12*	-22.2	-9*	NA	<-20
Modulation Bandwidth (GHz)	2	0.8	0.2	0.8	0.1	0.05	3	0.8	0.5	2	0.75
Modulation	**OFDM 64-QAM**	**OFDM 256-QAM**	OFDM 64-QAM	OFDM 64-QAM	256-QAM	OFDM 64-QAM	64-QAM	OFDM 64-QAM	64-QAM	OFDM 64-QAM	64-QAM
EVM_{rms} (dB)	**-25**	**-30.3**	-25.1 (37GHz)	-25.1	-31.2	-32*	-25.1	-27.1	-22.9	-24 (37GHz)	-26.1 (38GHz)
ACLR (dBc)	**-30.7**	**-33.3**	-24.1 (37GHz)	-27.8	-30	-33	NA	-32	-25.4	-25 (37GHz)	-31.1 (38GHz)
P_{avg} (dBm)	**16**	**12.17**	8.7 (37GHz)	10.2	18.2	14.7	15.5	8.4	12.2	10.2 (37GHz)	19.2 (38GHz)
PAEavg (%)	**4.1**	**1.93**	5.4 (37GHz)	13.6	17.6	NA	20	10.8#	16.1	9.8 (37GHz)	18.2 (38GHz)
VSWR	**1.5:1 to 3:1 @37 to 40GHz**		NA	NA	NA	NA	NA	3:1 @27 to 28GHz	3:1	4:1	NA
Gain Deviation (dB)	**0.7**		NA	NA	NA	NA	NA	0.65	0.9~1.3*	NA	NA
P_{1dB} Deviation (dB)	**0.79**		NA	NA	NA	NA	NA	NA	0.3~0.4*	~1*	NA
AM-PM_{max} (o)	**2.80**		NA	NA	NA	NA	NA	NA	NA	NA	NA

*Graphically estimated #PA drain efficiency.

6.6.2. VSWR MEASURMENTS

As discussed in Section 6.2, linearity, gain, and output power robustness under load mismatch are crucial in mm-wave phased-array systems. The VSWR resilience of the proposed PA is evaluated by measuring its AM-PM and large-signal performance under VSWR. The Maury tuner was characterized at the probe tip, and its calibration was done as described in [147]. Since the angle of the load provided by the tuner varies considerably even in bandwidth as narrow as 50MHz, the wideband modulation performance under VSWR will not accurately determine the resilience of the PA. Therefore, we report the linearity, gain, and output power variation under various VSWR conditions at different carrier frequencies to ensure that the PA supports wideband modulation signals under any VSWR condition.

Fig. 6.18 demonstrates the measured gain versus output power under various VSWR

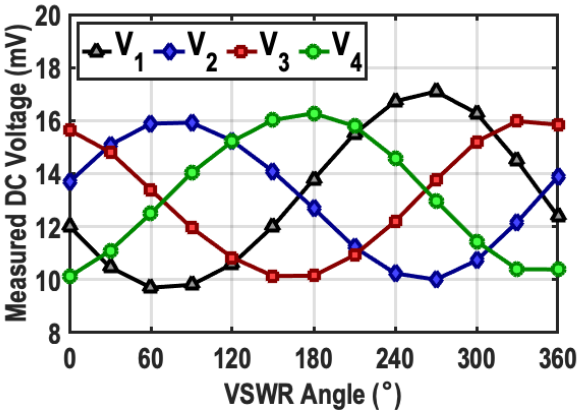


Figure 6.22: The raw measured RMS voltages at 40GHz and 16dBm output power.

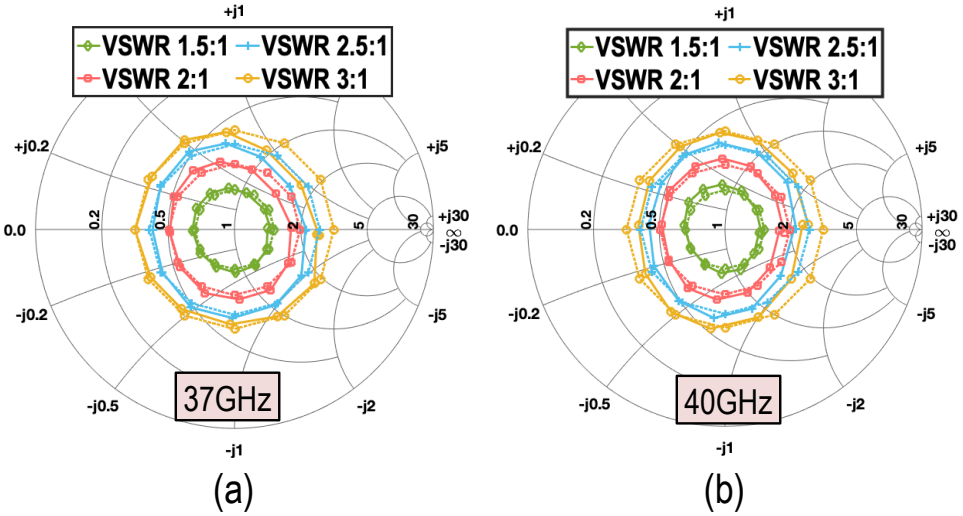


Figure 6.23: The measured load reflection coefficients (solid line) and the tuner's configured load (dashed line).

at 37GHz. The small-signal gain variation under VSWR 3:1 is ±0.7dB. The gain and saturated power of the PA in the 37-to-40GHz band are depicted in Fig. 6.19. Please note that the measured gain and power include 1.249dB reflection loss $(1-|\Gamma|^2)$.

Moreover, Fig. 6.20 exhibits the measured AM-PM under various VSWR at 37GHz. The normalized input 1dB compression point power deviation is also shown in Fig. 6.20. Compared with the measured AM-PM shown in Fig. 6.1(b), the proposed chain-weaver balanced PA provides a robust linearity performance under VSWR. Lately, the measured AM-PM deviations under various VSWR in the 37-to-40GHz band are summarized in Fig. 6.21. It shows that in a 3GHz bandwidth, the PA offers AM-PM<2.8°for any loading

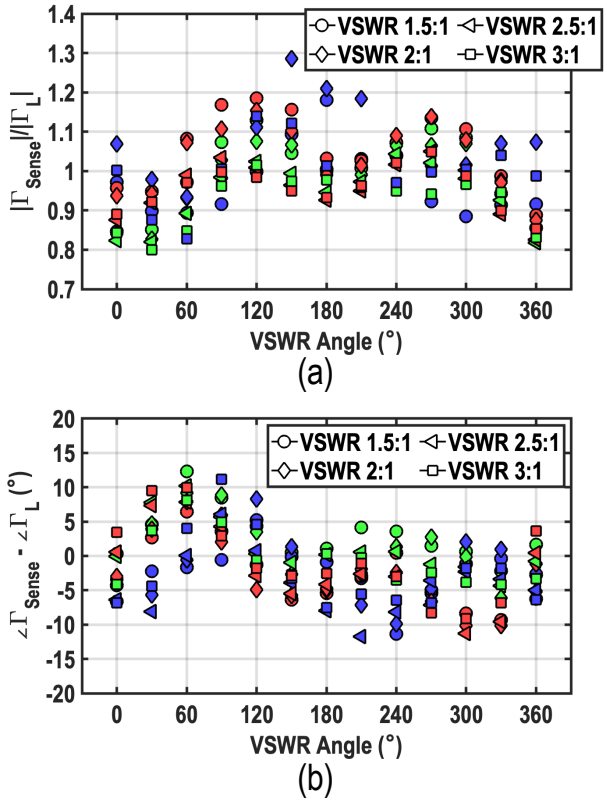


Figure 6.24: The measured load (a) magnitude and (b) angle errors at 37GHz (green), 38GHz (blue), and 40GHz (red).

condition in the VSWR 3:1 circle. Table 6.1 summarizes the measured performance of the proposed chain-weaver BPA.

6.7. MEASUREMENTS OF THE IMPEDANCE/POWER SENSOR

The performance of the embedded impedance/power sensor is evaluated under VSWR. As mentioned, the measured voltage is not equal due to insertion loss mismatches, non-ideal output matching, parasitics at the output pad, or rms detector mismatch. Therefore, one-time calibration is required. First, the outputs of the rms detectors are measured while PA delivers a CW signal to a matched load (50Ω). We then equalized them to have the same values for all four detectors in the matched loading condition. Further, fixed magnitude and phase correction factors are applied at each carrier frequency to address the insertion loss and phase misalignment. Additionally, the coupling ratio of the rms detectors must be de-embedded for the actual power sensing. Fig. 6.22 shows the measured raw data at 40GHz and 16dBm output power under VSWR 3:1. As expected from (6.6), the measured rms voltages (V_{1-4}^2) vary with ~90° phase difference. To calcu-

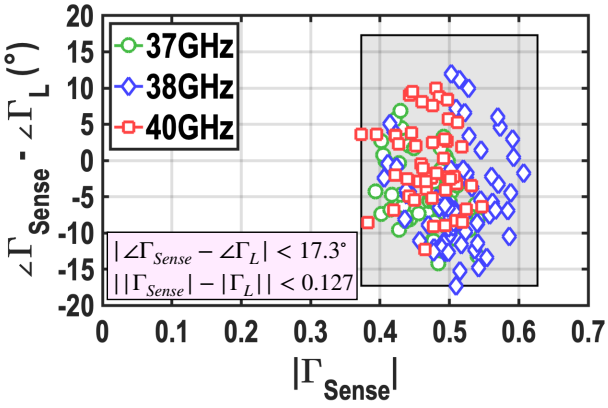


Figure 6.25: The measured $\angle\Gamma_{Error}$ versus $|\Gamma_{Sense}|$ for VSWR 3:1 (VSWR angle=0:30:360°) at five different output powers with 2dB step.

late the magnitude ($|\Gamma_{Sense}|$) and angle ($\angle\Gamma_{Sense}$) of the load using (6.7) and (6.8), a fixed correction coefficient is used for all VSWRs and signal power levels.

Fig. 6.23 compares the measured load reflection coefficients (solid line) with the tuner's configured load (dashed line). To show the accuracy of the impedance sensor, the magnitude and angle error of the measured impedance are demonstrated in Fig. 6.24. We define the magnitude and angle error as

$$M_{Error} = \frac{|\Gamma_{Sense}|}{|\Gamma_L|}, \tag{6.11}$$

$$\angle\Gamma_{Error} = \angle\Gamma_{Sense} - \angle\Gamma_L, \tag{6.12}$$

where Γ_L the load provided by the tuner and Γ_{Sense} is the load measured by the impedance sensor. The magnitude error is evaluated by its ratio rather than its difference to ensure reasonably high accuracy for all VSWR conditions. Fig. 6.24(a) shows the maximum error occurs at 38GHz for VSWR 2:1 and 150° (M_{Error} =1.286), while the maximum angle error observed at 37GHz for VSWR 1.5:1 at 60° ($\angle\Gamma_{Error}$ =12.3°).

Thus far, the impedance sensor accuracy has been examined at one output power level. However, since the impedance of the PA can change by its output power, it may impact the accuracy of the impedance sensor. Therefore, the measured $|\Gamma_{Sense}|$ and $\angle\Gamma_{Error}$ for VSWR 3:1 (VSWR angle=0:30:360°) at five different output powers with 2dB step are depicted in Fig. 6.25. It shows the impedance sensor can measure VSWR 3:1 by maximum angle and magnitude errors of 17.3°and 0.127, respectively.

As explained in Section 6.4, the output power can be calculated using (6.9). We first measured the output power for a 50Ω matched load. Fig. 6.26 exhibits the measured output power using the embedded power sensor and its error ($P_{OUT} - P_{Sense}$) versus the output power (P_{OUT}) measured by an external power meter. The power sensor is calibrated one time at 18dBm output power. The power sensing error under VSWR at different carrier frequencies is also demonstrated in Fig. 6.27. The maximum error is -1.092dB, which occurs at 38GHz.

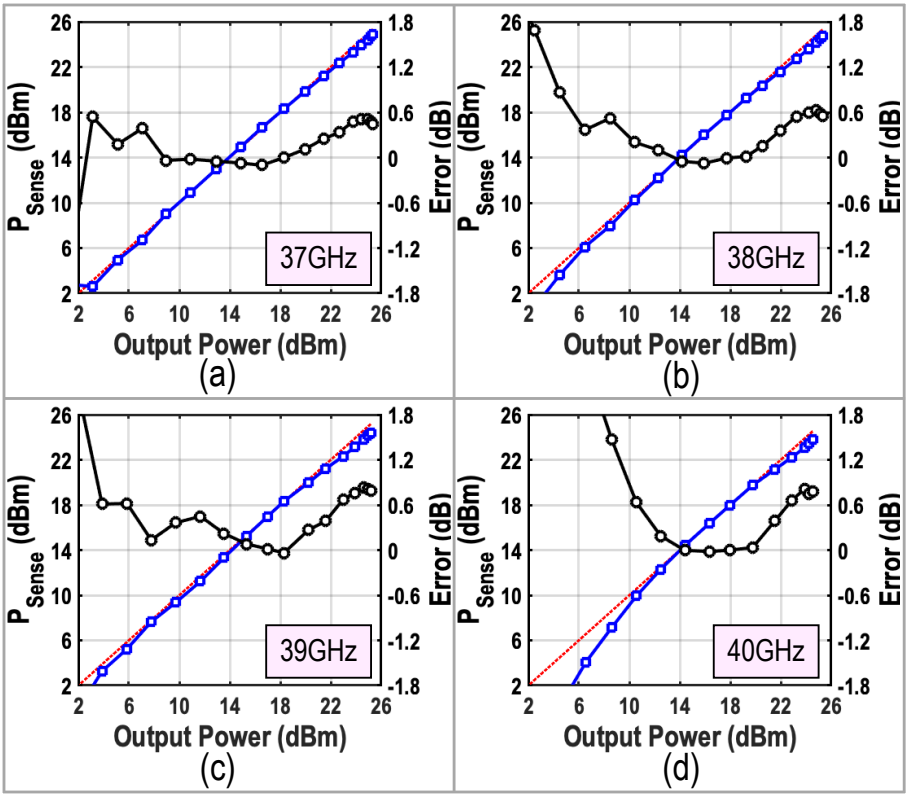


Figure 6.26: The measured output power using the embedded power sensor and its error ($P_{OUT} - P_{Sense}$) at (a) 37GHz, (b) 38GHz, (c) 39GHz, and (d) 40GHz.

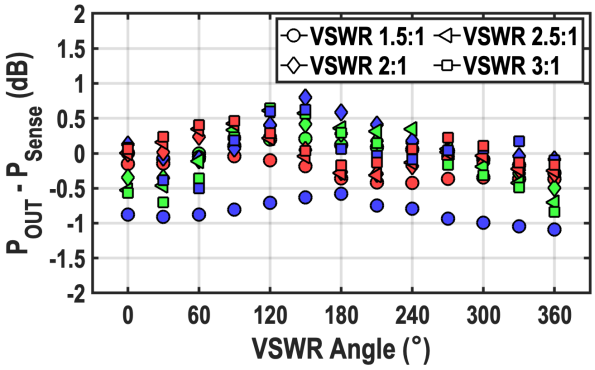


Figure 6.27: The power sensing error under VSWR at 37GHz (green), 38GHz (blue), and 40GHz (red).

6.8. CONCLUSION

This chapter presented an N-way chain-weaver balanced power amplifier for mm-wave phased-array TXs. The proposed PA architecture offers linearity and gains

Table 6.2: Impedance Sensors Performance Comparison

Parameter	This Work	Mm-Wave/RF Impedance Sensors			
		Munzer ISSCC 2022	Zhang ISSCC 2021	Munzer MWCL 2021	Lu ISSCC 2017
Technology	**40nm CMOS**	45nm SOI	22nm SOI	45nm SOI	40nm CMOS
VSWR	**1.5:1 to 3:1**	3	3	3	3
Frequency (GHz)	**37 to 40**	27 to 41	28	38	2.4
$\lvert 20\log\frac{\lvert\Gamma_{Sense}\rvert}{\lvert\Gamma_L\rvert}\rvert (dB)$	**2.14**	2.38 (Estimated)	NA	3.38	1.87 (Estimated)
$\lvert\lvert\Gamma_{Sense}\rvert - \lvert\Gamma_L\rvert\rvert$	**0.106**	0.149 (37GHz)	0.14	0.238	0.1
$\lvert\angle\Gamma_{Sense} - \angle\Gamma_L\rvert (^\circ)$	**12.3**	18.72 (37GHz)	33	28.9	18

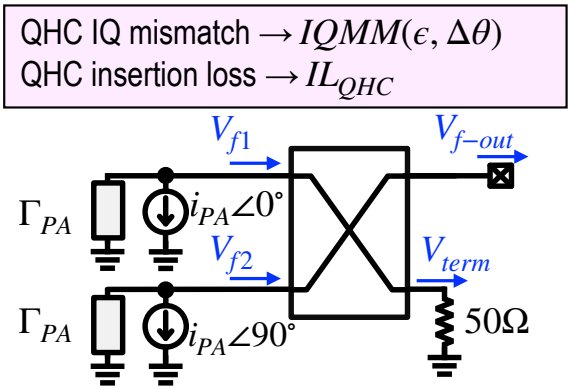


Figure 6.28: A simplified BPA operating in the presence of QHC IQ mismatch.

robustness under frequency/time-dependent VSWR, while it comprises an embedded impedance/power sensor. In the event of VSWR, the proposed PA provides N different loads distributed on the VSWR circle with equal angle distance. An eight-way chain-weaver balanced PA is realized in 40nm bulk CMOS technology as a proof-of-concept. The proposed PA supports a 2GHz 64-QAM OFDM signal with 16dBm average power. Assuming any frequency/time-dependent loading condition within the VSWR 3:1 circle, the proposed chain-weaver BPA achieves <2.8° AM-PM over 3GHz BW. Finally, as compared in Table 6.2 the proposed embedded impedance/power sensor accuracy surpasses the best-in-class companions.

6.9. APPENDIX A

Assuming no IQMM in the QHC, a perfect reflected signal cancellation was considered in Sections 6.3 and 6.3. However, the IQMM of the QHC can lead to additional combining power loss, power leaking into the termination resistors, and non-perfect output matching, which can introduce gain variation and degrade the accuracy of the proposed

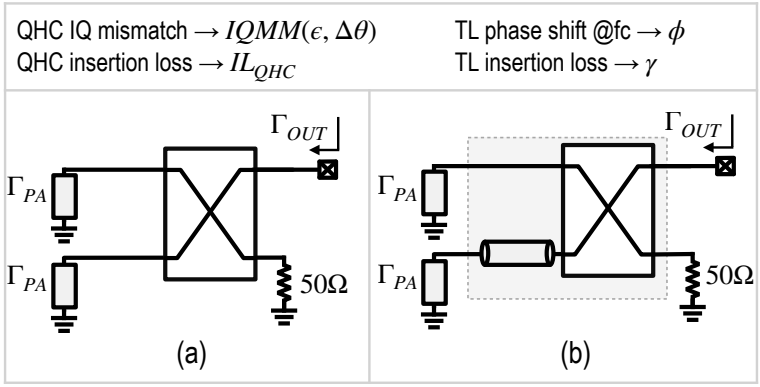


Figure 6.29: (a) A simplified BPA representing the first stage of the chain-weaver PA, and (b) a BPA with an additional TL representing the second and third stages of the chain-weaver PA.

impedance/power sensor.

Fig. 6.28 depicts a simplified conventional BPA assuming a QHC with ϵ and $\Delta\theta$ as its amplitude and phase errors, respectively. Following the same notation as Fig. 6.4, we have $V_{f1} = V_{tx}\angle 0^\circ$ and $V_{f2} = V_{tx}\angle 90^\circ$. Therefore, the output forward signal and the termination resistor voltage can be obtained by

$$V_{f-out} = V_{tx}.IL_{QHC}.\sqrt{1+\frac{2(1+\epsilon)\cos\Delta\theta}{1+(1+\epsilon)^2}}, \tag{6.13}$$

$$V_{term} = V_{tx}.IL_{QHC}.\sqrt{1-\frac{2(1+\epsilon)\cos\Delta\theta}{1+(1+\epsilon)^2}}, \tag{6.14}$$

where IL_{QHC} is the insertion loss of the QHC. Therefore, contrary to the reliability criteria posed by VSWR for the first-stage termination resistors, the reliability of the second and third stages are more at risk due to higher power levels. Hence, all termination resistors' reliability must be satisfied for the maximum possible amplitude/phase errors and peak power.

An imperfect QHC deteriorates the reflected signal cancellation in a BPA and, as a result, degrades the output matching condition. In a conventional BPA as exhibited in Fig. 6.29(a), the output reflection coefficient (Γ_{OUT}) can be calculated as

$$|\Gamma_{OUT}| = \frac{\sqrt{1+(1+\epsilon)^4-2(1+\epsilon)^2\cos 2\Delta\theta}}{1+(1+\epsilon)^2}|\Gamma_{PA}|.|IL_{QHC}|^2, \tag{6.15}$$

which explains the gain variation illustrated in Fig. 6.3(c).

To extend this analysis to the proposed chain-weaver PA, we need to consider added TLs insertion losses and phase shifts, as shown in Fig. 6.29(b). Assuming TL phase shift

and insertion loss are ϕ and γ, respectively, the output reflection coefficient can be calculated as

$$|\Gamma_{OUT}| = \frac{\sqrt{1+\hat{\gamma}^4 - 2\hat{\gamma}^2 \cos 2\Delta\hat{\theta}}}{1+\hat{\gamma}^2} |\Gamma_{PA}|.|IL_{QHC}|^2, \tag{6.16}$$

where $\hat{\gamma} = \gamma(1+\epsilon)$ and $\Delta\hat{\theta} = \Delta\theta + \phi$. Now, by replacing $|\Gamma_{PA}|$ in the above equation with an expression from the previous formula and considering $\phi = 22.5°$, we can obtain the output reflection coefficient of the second stage. Likewise, the calculated coefficient can be employed in (6.16) again, this time considering $\phi = 45°$, to obtain the output coefficient of the eight-way chain-weaver PA.

7

A MM-WAVE POWER AMPLIFIER WITH AN INTEGRATED ISOLATOR/CIRCULATOR/RECEIVER

This chapter presents a reconfigurable mm-wave fully integrated frequency division duplex (FDD) frontend that comprises a power amplifier (PA) and an integrated nonreciprocal ultra-compact isolator/circulator/receiver (RX). The realized circulator is based on a ring quarter-wave transmission line topology with adjusted characteristic impedances, improving transmitter (TX)-to-antenna insertion loss and TX-to-RX isolation. The circulator's nonreciprocal gyrator features an AND-gate switching-based N-path filter while acting as a mixer-first RX. The circulator can be reconfigured into an isolator by activating cross-coupled negative resistors. This compared N-path filter-based circulator/isolator occupies only 0.38mm^2. Over a 27.1-to-31.1GHz band, the realized frontend offers >20dB TX-to-RX isolation while its measured TX-to-antenna insertion loss is 1.7~2.2dB. The RX path tolerates the PA's blocker signal, achieving 5dBm in-band and 13dBm out-of-band B_{1dB}. The PA delivers 15.15dBm peak output power with 33% drain efficiency. The functionality of the proposed FDD frontend is evaluated by simultaneous TX/RX operation with 400MHz TX/RX modulation bandwidth and 400MHz channel spacing. The measured AM-PM of the realized PA with the integrated isolator shows relatively high VSWR resilience at the lower power level and less robustness against VSWR around its peak output power. The frontend prototype occupies only 0.7mm^2, including circulator, PA, quadrature hybrid coupler LO generators, and baseband circuits.

Part of this chapter is published in 2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) [142].

7.1. INTRODUCTION

Millimeter-wave (mm-wave) bands accommodate various high-throughput communication and high-resolution sensing systems, such as 60GHz Wi-Fi (IEEE 802.11ad and IEEE 802.11ay standards) [160–162] and automotive radar [163–165]. Owing to silicon technology scaling, mm-wave phased-array systems enable the development of satellite communication and fifth-generation (5G) cellular wireless networks to address the demand for high data throughput and low latency. In addition to allocating wide channel bandwidth at mm-wave frequencies, dual orthogonal polarization further increases channel capacity and enhances spectral efficiency. Nevertheless, their shorter wavelength leads to lower penetrability and higher free-space path loss, thus limited coverage [7].

Beamforming architectures address the required link budget while reducing interference and increasing link security [11]. However, the directional and line-of-sight connections make the link even more susceptible to small obstacles, degrading the distance and mobility support. Moreover, mm-wave dual-polarized phased-array systems pose stringent requirements on the transceiver's (TRX) performance specifications, power consumption, and, most importantly, the occupied silicon area.

The ongoing 5G new radio (NR) frequency range two (FR2) standard has utilized mm-wave bands (e.g., 24.25-29.5GHz, 37-43.5GHz, and 47.2-48GHz), while the time division duplex (TDD) ensures channel reciprocity. Although industry and research groups have vastly developed the 5G NR system and shown promising performance in supporting multi-Gbit/s data rate [150, 166–168], its coverage range must be improved. In addition to TDD, full-duplex systems such as frequency division duplex (FDD) and single-frequency full-duplex (SF-FD) recently gained momentum, envisioning more innovative and revolutionary link protocol design [169–171]. Considering the stringent area restriction of the phased array structures, implementing the frontend with appropriate duplexing and band-pass filtering to support the FDD and SF-FD systems at mm-wave frequencies is very challenging.

Employing separate antennas for the transmitter (TX) and the receiver (RX) provides sufficient isolation in full-duplex systems at the cost of a larger form factor [172]. Electrically balanced duplexer (EBD) and its counterparts, such as hybrid coupler and Wilkinson combiner, offer a high TX-to-RX isolation for a single-antenna system and occupy a reasonably low area [173–176]. However, they still suffer from 3-dB loss at TX and RX paths. Magnetic-free CMOS circulators have recently been presented at RF and mm-wave bands for SF-FD links [64, 177–180]. As illustrated in Fig. 7.1(a), apart from the circulator's isolation, which is crucial to prevent the receiver from saturation, further self-interference cancellation (SIC) is required. Nonetheless, achieving high SIC in a practical phased array system considering process, voltage, and temperature (PVT) variations and mutual coupling issues if the closely spaced antenna arrays is a daunting task. Moreover, state-of-the-art mm-wave CMOS circulators are still relatively large for phased-array systems and introduce a high loss comparable to EBDs and hybrid couplers.

Fig. 7.1(b) depicts an FDD TRX frontend utilizing a circulator as the duplexer. In contrast to SF-FD, the TX signal acts as an out-of-band (OOB) blocker and, hence, demands a sharp band-pass filter (BPF). Because implementing integrated compact BPF is not feasible at mm-wave, standalone mixer-first RX architectures and active BPFs have

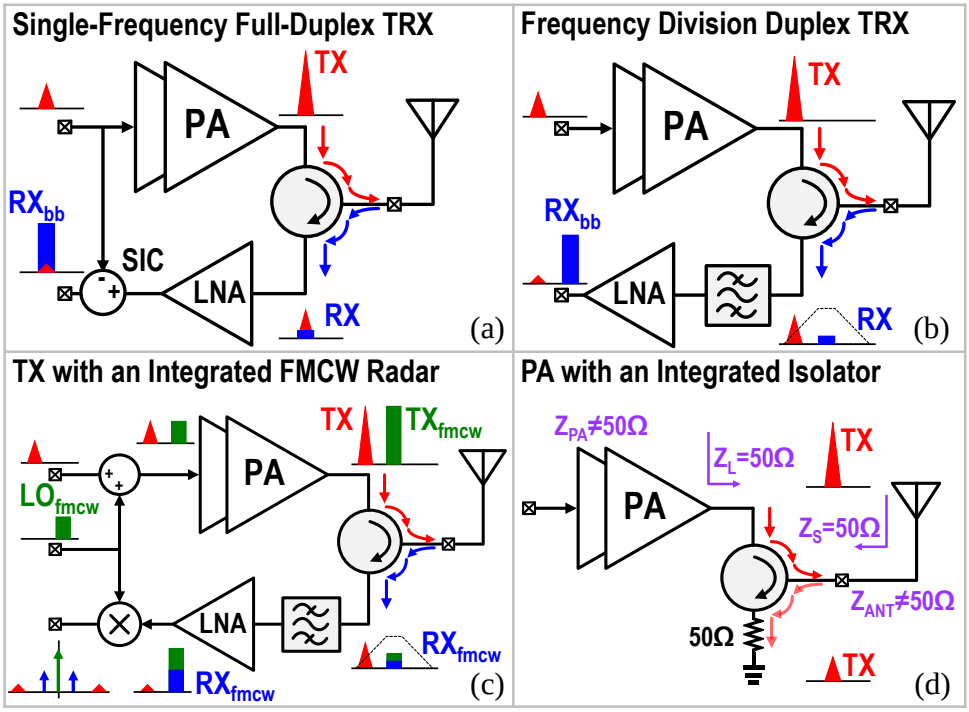


Figure 7.1: A simplified form of the possible applications employing the mm-wave integrated circulator/isolator: (a) SF-FD TRX front-end, (b) FDD TRX front-end, (c) TX Front-end with an integrated FMCW radar for background sensing, and (d) a PA with an integrated isolator.

gained significant research attention [181–184]. In [169], an E-band Backhaul-on-glass FDD module comprising TRX, PAs, and diplexer is introduced. However, due to its significant form factor, the FDD module is not scalable in a phased array system to enhance the link budget.

Moreover, employing a circulator as the duplexer fulfills the requirements of both the SF-FD and FDD systems, opening the path to new applications. Single-antenna frequency-modulated continuous-wave (FMCW) radars require a full-duplex front-end to transmit the continuous-wave (CW) frequency ramp while receiving the reflected signal from targets. [185] introduces a signal processing pipeline to extract distance from reflected orthogonal frequency division multiplexing (OFDM) communications signals. However, beamforming directs the TX OFDM signal to the desired RX, so using the reflected signal for real-time 3-D sensing is not feasible. Besides, the TDD architecture of the conventional 5G FR2 forces a separate antenna radar structure. An alternative architecture is illustrated in Fig. 7.1(c), where the TX operates alongside an FMCW radar at different carrier frequencies. In this context, the RX should tolerate both IB and OOB blockers demanding to support SF-FD and FDD simultaneously. This can pave the way for environmental intelligence and intelligent beam steering.

In addition to the full-duplex TRX operation, the integrated circulator can be reconfigured to an isolator. As depicted in Fig. 7.1(d), despite the impedance of the power amplifier (PA) and antenna, the isolator simultaneously provides matched sourcing impedance for the antenna and optimum loading conditions for the PA. This is opposed to the balanced amplifiers [88, 149] and the reconfigurable matching networks [48, 104, 106], which only provide matched loading conditions to the antenna or the PA.

This chapter demonstrates the feasibility and implementation of two separate solutions for mm-wave phased array systems. First, we elaborate on our recently published compact single-antenna mm-wave full-duplex frontend [142] capable of operating as an FDD frontend, supporting simultaneous transmit and receive (STAR) FDD communication with up to 400MHz modulation bandwidth. Second, we reconfigure the chip to a VSWR-resilient PA with an integrated isolator. The proposed reconfigurable architecture features: 1) an mm-wave N-path filter as a nonreciprocal gyrator that simultaneously functions as a blocker tolerant RX, 2) a compact differential ring quadrature transmission lines topology with adjusted characteristic impedances to improve the TX-to-antenna insertion loss (IL_{TX}), RX gain (G_{RX}), and TX-to-RX isolation, 3) an integrated push-pull PA directly connected to the proposed circulator/isolator, and 4) embedded negative resistors to reconfigure the frontend to an integrated isolator.

This chapter is organized as follows. Section 7.2 presents the system requirements and analysis. The proposed circulator/isolator architecture is given in Section 7.3, where we proposed a pass-transistor-based AND-gate switching to realize an N-path filter at mm-wave frequencies. Section 7.4 elaborates on the circuit implementation details of the 40-nm bulk CMOS technology prototype. Section 7.5 presents the experimental results of the FDD frontend, and Section 7.6 reports the measurement results of the integrated isolator. Finally, this chapter is concluded in Section 7.7.

7.2. MM-WAVE FULL-DUPLEX TRX SYSTEM LEVEL DESIGN AND TRADE-OFFS

This Section discusses system design specifications and trade-offs for an mm-wave phased-array full-duplex link.

7.2.1. LINK BUDGET CALCULATIONS

In a conventional single-input single-output (SISO) link, the link budget (LB) can be calculated as

$$LB_{SISO,dB} + LM_{dB} = P_{TX,dBm} + 2 \times G_{A,dBi} - P_{S-RX,dBm} \tag{7.1}$$

where $P_{TX,dBm}$ and $P_{S-RX,dBm}$ are TX signal power and RX sensitivity of a TRX element, respectively. $G_{A,dBi}$ is antenna gain and LM_{dB} is link margin. As mentioned, modern communication systems aim to support multi-Gb/s data throughput by allocating wider bandwidth, which means a higher RX noise floor. They also employ high-order complex modulation schemes, requiring a higher signal-to-noise ratio (SNR). As a result, the RX sensitivity ($P_{S-RX,dBm} = -174\,\text{dBm/Hz} + 10\log BW_{Hz} + NF_{dB} + SNR_{dB}$) increases, thus, the link budget decreases. As such, mm-wave bands are inevitable in accommodating signals with large modulation bandwidth. This attribute raises two more issues:

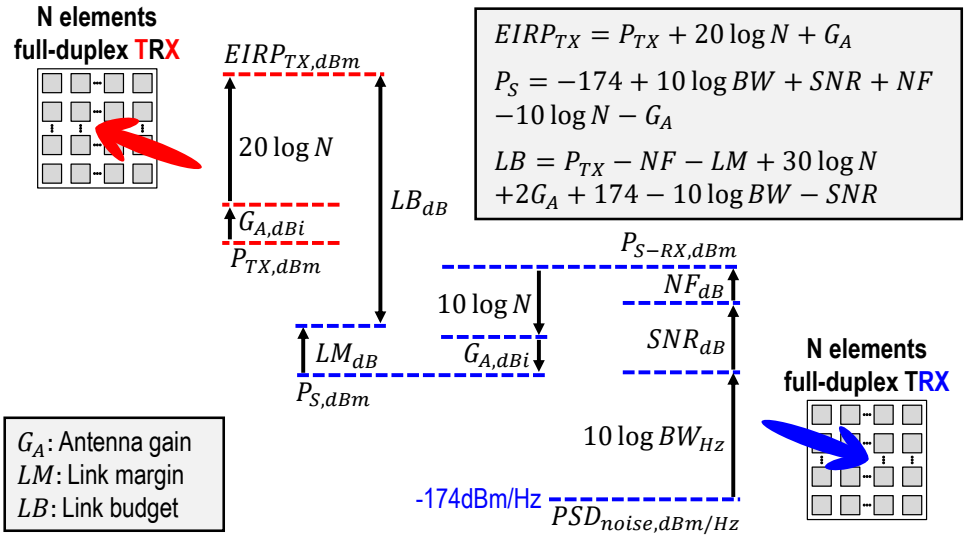


Figure 7.2: The link budget calculation of a full-duplex link employing two N-elements phased-array TRXs.

1) higher free-space path loss and 2) lower TX output power due to technology limitations at such frequency bands. In summary, modern communications systems demand a higher link budget to address higher free-space path loss, while their link budget suffers from high RX sensitivity and limited TX output power. To address these challenges, as exhibited in Fig. 7.2, an N elements phased array link offers $30\log N$ link budget improvement.

As an example of a short-range link, e.g., $d = 100$ m line-of-sight, we assume two 64 elements TRXs employing a 400MHz 64-QAM OFDM scheme (requiring $SNR_{dB} = 25dB$) at 28GHz carrier frequency. Considering 4 dBi antenna gain ($G_{A,dBi}$) and 10 dB link margin (LM_{dB}), $P_{TX,dBm} - NF_{dB} > -13.79$ dBm is required to address path loss of a 100 m long link.

7.2.2. ISOLATION AND LINEARITY REQUIREMENTS

As depicted in Fig. 7.1 (a-b), the TX signal interferes with the RX as they operate simultaneously in a single antenna full-duplex radio. Mitigating RX sensitivity degradation caused by TX signal enforces stringent specifications for duplexer (e.g., a circulator) isolation and RX linearity. Moreover, an SC-FD system employs SIC along with the circulator's TX-to-RX isolation (ISO) to ensure that the TX signal and its distortions are well below the RX noise floor. Therefore, as discussed in [177], ISO+SIC must be less than $P_{TX,dBm} - NF_{dB} + 174dBm/Hz - 10\log BW_{Hz}$. However, in a phased array system with the same RX and TX beam direction, since the TX interferers are combined coherently alongside the RX signals, the required ISO+SIC can be calculated as

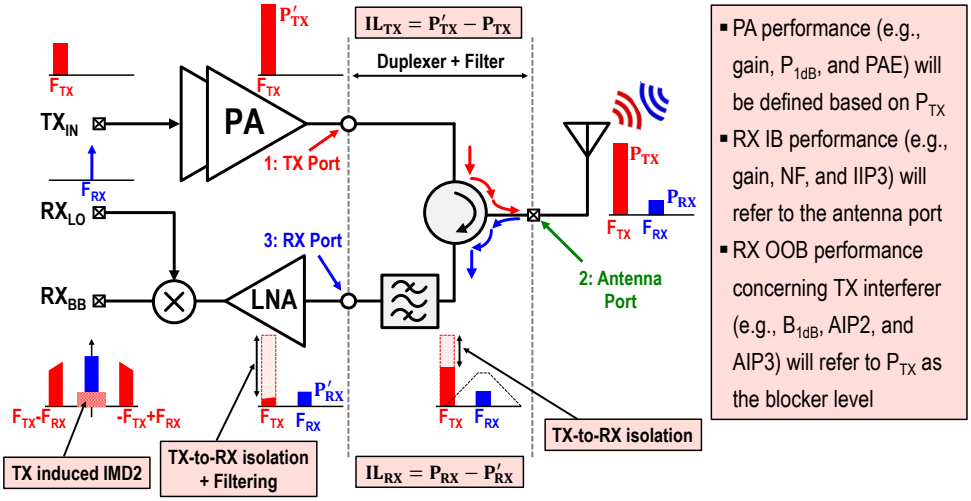


Figure 7.3: The TX-induced second-order distortion mechanism in the fully integrated FDD TRX.

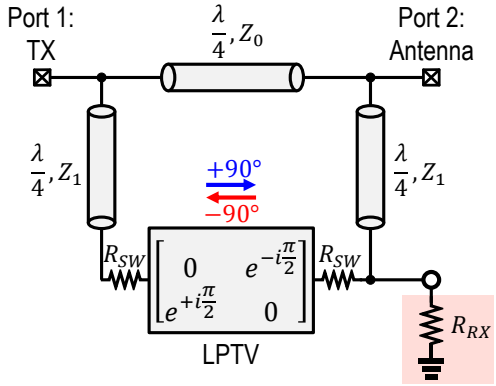
$$ISO + SIC > P_{TX,dBm} - NF_{dB} + 174\,\text{dBm} - 10\log BW_{RX,Hz} + 10\log N - 10\log\frac{BW_{TX,Hz}}{BW_{RX,Hz}}, \tag{7.2}$$

where $BW_{TX,Hz}$ and $BW_{RX,Hz}$ are TX and RX signals modulation bandwidths, respectively. Assuming ISO=20dB and 400MHz RX/TX modulation bandwidth, SIC>72.21dB is required for the design as mentioned earlier example. Nevertheless, extending SC-FD phased-array systems requires higher SIC, which is practically hard considering PVT variations and mutual coupling.

Moreover, the dual-polarization feature introduces another interferer due to the antenna's limited horizontal-vertical (H-V) isolation (e.g., 20dB). Therefore, canceling perpendicular polarization's TX signal leakage is inevitable, making the system even more complex. Therefore, even though SC-FD link architecture offers the highest spectrum efficiency, it is not readily extendable to dual-polarization massive-MIMO systems.

Similarly, a conventional single-antenna FDD system demands high duplexer isolation. For instance, third-generation (3G) wireless systems require >50dB duplexer isolation, where the duplexer handles 15V signal swing to support $P_{TX,dBm} = 24dBm$ [174]. Such a duplexer adds high loss ($\sim 2-3dB$) at both RX and TX paths [186], degrading TX efficiency and RX sensitivity. However, in the modern phased array systems, since the $P_{TX,dBm}$ is lower and the RX sensitivity level is higher, the requirement on a single RX element's duplexer isolation and linearity could be relaxed, enabling fully integrated mm-wave wideband full-duplex links.

As depicted in Fig. 7.1 (b), in the RX path of an FDD system, the channel select filters to suppress the TX signal as well as any other interferers, e.g., mutual coupling and orthogonal-polarization signals to prevent RX amplifiers from saturation. Therefore, unlike SC-FD systems, a dual-polarization phased array FDD system does not entail an-



Nonreciprocal phase-response technique	Two-port N-path filter [xx]	Nonreciprocal Delay [xx]
Compact die area	✓	✗
mm-wave operation	✗	✓
TX-to-antenna loss	✗	✗
Down-conversion	✓	✗

Figure 7.4: The magnetic-free CMOS circulators [64, 177].

other interferer cancellation loop but compels more stringent out-of-band (OOB) interferer rejection.

Even though the TX signal occupies another frequency band, its noise and distortion levels must stay well below the RX noise floor. This imposes a stringent requirement on RX linearity and its OOB interferer tolerance specifications, such as input 1dB compression point (IP_{1dB}), input third-order intercept point (IIP_3), and, for a direct conversion RX architecture, input second order intercept point (IIP_2).

A conventional FDD system considers the TX, RX, and duplexer components individually each with their own specifications. On the contrary, this work aims to study the design of a fully integrated frontend, including the duplexer. Therefore, we redefine the TRX specifications based on the antenna port's signal levels, as shown in Fig. 7.3. We defined antenna-port referred third-order intercept point (AIP_3) and antenna-port referred second-order intercept point (AIP_2) to address TX-induced distortions. Thus, the AIP_2 specification can be calculated as

$$\begin{aligned} AIP_2 > {} & 2P_{TX} - NF + 174dBm - 10\log BW_{RX} \\ & + 10\log N - 10\log\frac{2BW_{TX}}{BW_{RX}} - 3dB. \end{aligned} \tag{7.3}$$

Note that, in practice, specifying the required distortion and noise levels needs complex system-level calculations. Nevertheless, these simplified equations help determine trade-offs and making the right design choices.

7.3. PROPOSED MM-WAVE CIRCULATOR/ISOLATOR ARCHITECTURE

As depicted in Fig. 7.4, the magnetic-free CMOS circulators comprise a circle of three quarter-wave transmission lines (QTLs) and a nonreciprocal linear periodic time-variant (LPTV) circuit. LPTV provides a +90° phase shift in one direction and a -90° phase shift

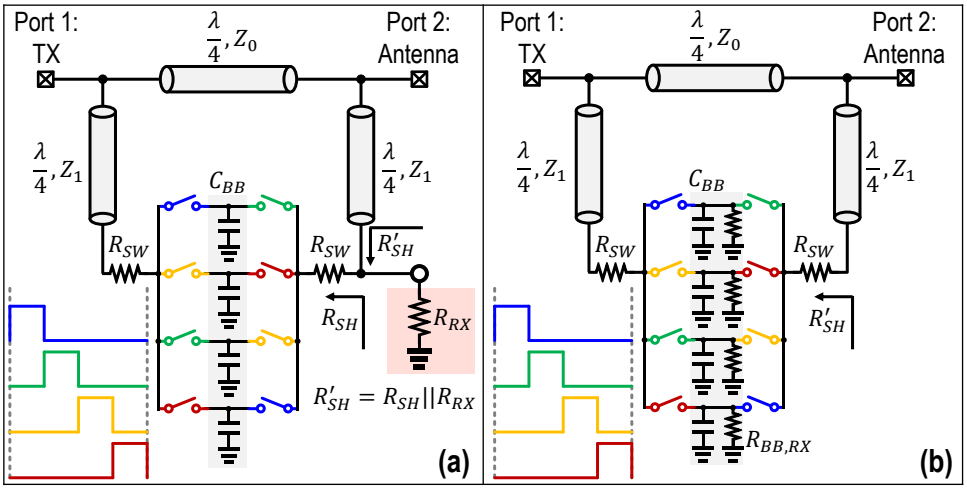


Figure 7.5: The magnetic-free CMOS circulators utilizing an N-path filter as LPTV and termination resistor placed at (a) RX port, and (b) baseband.

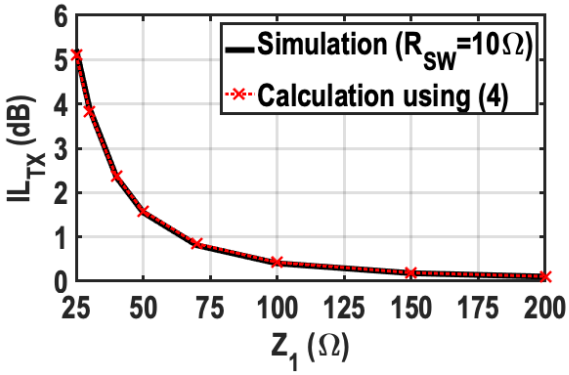


Figure 7.6: Simulated and calculated IL_{TX} versus Z_1 while $Z_0 = 50\Omega$.

in the opposite direction, leading to wave propagation only in one direction. The LPTV component can be implemented either by a two-port N-path filter or a nonreciprocal delay. N-path filters occupy a small die area and contain an embedded down-conversion path [178]. However, they are unpractical at the mm-wave frequencies as generating and amplifying the nonoverlapping clocks of the N-path filter is challenging. Therefore, a nonreciprocal delay technique has been exploited to extend the operational frequency of the CMOS circulators to mm-wave in the cost of occupying a relatively large area [64]. Nevertheless, both LPTV solutions introduce a high IL_{TX}, basically caused by the switches' impedance (R_{SW}), and heavily depends on the employed technology node.

To mitigate this undesired loss, we proposed a noncontinuous QTL characteristic

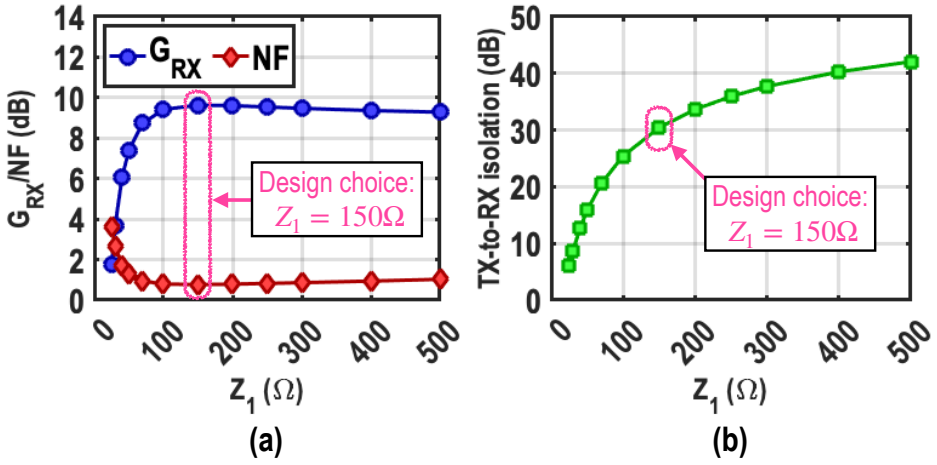


Figure 7.7: Simulated (a) G_{RX}, NF, and (b) TX-to-RX isolation versus Z_1 values while $Z_0 = 50\Omega$ and $C_{BB} = 500fF$.

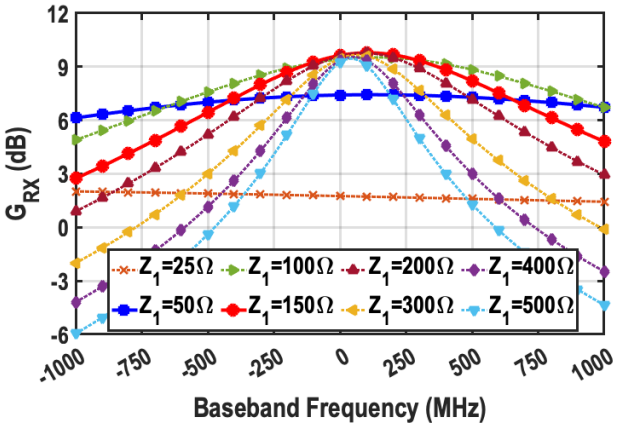
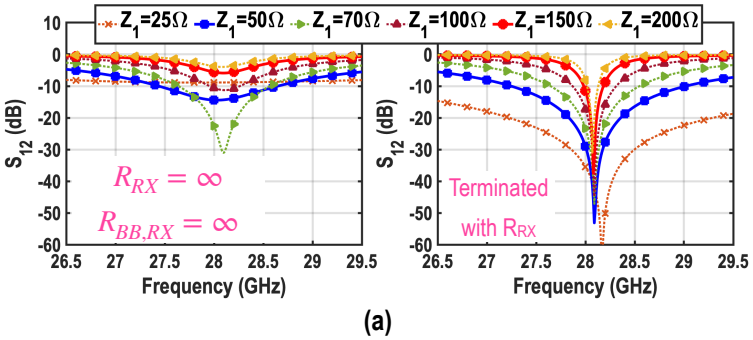


Figure 7.8: Simulated G_{RX} versus baseband frequency for various Z_1 values while $Z_0 = 50\Omega$ and $C_{BB} = 500fF$.

impedance to have a degree of freedom for optimizing IL_{TX}. As depicted in Fig. 7.4, the QTL impedance of the direct path is Z_0, which defines the impedance of the circulator, while the impedance of two other QTLs (Z_1) is chosen to be greater than Z_0. As discussed in [177], the IL_{TX} is mainly determined by R_{SW} independent from the employed LPTV structure and its configuration. The IL_{TX} can be calculated as follows

$$IL_{TX} = \frac{1}{S_{21}} = 1 + \frac{Z_0 R_{SW}}{Z_1^2}. \tag{7.4}$$

As can be inferred from (7.4), selecting a larger Z_1 decreases the IL_{TX}.



(a)

Values of R_{RX} **OR** R_{BB} required to terminate the clockwise propagating waves						
Z_1	25Ω	50Ω	70Ω	100Ω	150Ω	200Ω
R_{RX}	19Ω	162Ω	-1.6kΩ	-290Ω	-248Ω	-267Ω
$R_{BB,RX}$	54Ω	590Ω	-7.2kΩ	-1.15kΩ	-980Ω	-1.06kΩ

(b)

Figure 7.9: (a) The simulated S_{12} without (left) and with (right) R_{RX} termination for various Z_1 values while $Z_0 = 50\Omega$, $C_{BB} = 500fF$, and $R_{BB,RX} = \infty$. (b) The resistor values required for R_{RX} or $R_{BB,RX}$ for terminating the reflected wave from the antenna port when the PA port is excited (clockwise propagating waves).

As exhibited in Fig. 7.5(a), the two-port N-path filter is chosen in this work to benefit from its embedded down-converter and compact die area. Considering $Z_0 = 50\Omega$ and $R_{SW} = 10\Omega$, Fig. 7.6 shows the simulation results with ideal switches reasonably match the calculated IL_{TX} using (7.4).

Since the N-path filter down-converts the RX signal, in the full-duplex frontend mode of operation, the actual RX port of the circulator is left open ($R_{RX} = \infty$, see Fig. 7.5(a)) [178]. Therefore, assuming an infinitive number of paths ($N \rightarrow \infty$) and using a relatively higher impedance value for Z_1 compared to Z_0, the desired RX signal arrives with a higher voltage amplitude at the baseband, benefiting the conversion gain (G_{RX}) and NF. However, due to the finite number of paths ($N = 4$), the impedance presented by the N-path filter (R_{SH}) is limited. Thus, the G_{RX} and NF improvements are not persistent and slightly degrade at greater Z_1 values. Utilizing $R_{SW} = 10\Omega$ and $C_{BB} = 500fF$, the simulation results with ideal switches are demonstrated in Fig. 7.7, which confirms the substantial improvement of G_{RX}, NF, and TX-to-RX isolation. As shown, $Z_1 = 150\Omega$ is chosen in this design to maximize G_{RX} and TX-to-RX isolation and minimize IL_{TX} and NF. Nevertheless, to achieve the mentioned benefit, the giveaway is bandwidth. Fig. 7.8 depicts G_{RX} versus baseband frequency for various Z_1, where utilizing greater Z_1 narrows the bandwidth.

Moreover, as $R_{RX} = \infty$ in the full-duplex configuration, the RX signal passes through the nonreciprocal N-path filter in this structure and is eventually absorbed in the TX port termination [178]. Therefore, a termination resistor R_{RX} must be employed at the RX port to reconfigure the proposed circulator to an isolator. Incorporating with R_{SH}, the termination resistor must provide a matching condition for the clockwise propa-

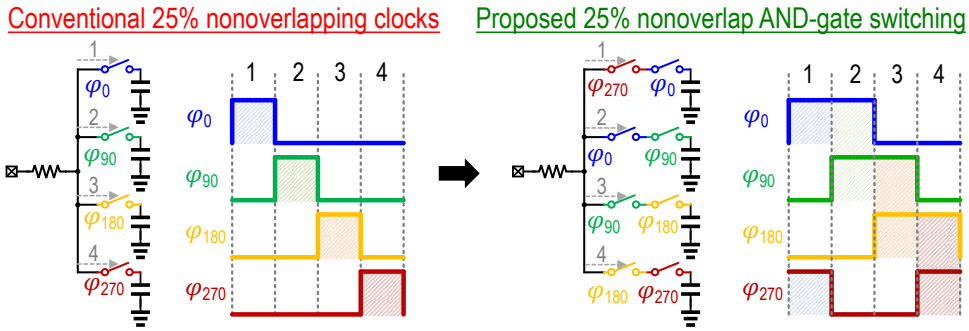


Figure 7.10: The AND-gate switching N-path filter's principles.

gating waves, thus establishing reverse isolation from the antenna port to the TX port. Assuming matching conditions at TX and antenna ports, the following condition must be satisfied for the termination resistor

$$R_{SH}||R_{RX} = \frac{R_{SH} \times |R_{RX}|}{R_{SH} + R_{RX}} = \frac{Z_1^2}{Z_0}. \tag{7.5}$$

Fig. 7.9 (a) demonstrates the simulated S_{12} (Port 1: TX and port 2: antenna) without (left) and with (right) R_{RX} termination resistor, and reveals three observations. 1) Even without a termination resistor, reverse isolation is achieved when $Z_1 = 70\Omega$. 2) the bandwidth of the reverse isolation, achieved by termination, decreases when it becomes greater Z_1. 3) As shown in Fig. 7.9 (b), a positive termination resistor is utilized for $Z_1 < 70\Omega$, while a negative resistor is required to satisfy the termination condition when $Z_1 \geq 70\Omega$.

Moreover, Fig. 7.5 (b) shows that the clockwise wave can be terminated with the baseband resistors ($R_{BB,RX}$). As reported in Fig. 7.9 (b), the required baseband resistors are larger than RF termination, and their parasitics can be absorbed in the baseband capacitors (C_{BB}).

7.3.1. N-PATH FILTER DESIGN

As mentioned, the nonreciprocal LPTV circuit is implemented as two back-to-back N-path filters to benefit from their compact area, which is crucial for phased array systems. In a conventional N-path filter, e.g., a four-path filter, nonoverlapping 25% LO clocks are required to diminish the charge sharing of switches, providing high-Q filtering. Obviously, generating and amplifying 25% LO clocks requires very broadband circuits, which is not feasible at the mm-wave frequencies. In [187], a quadrature mixer topology is introduced to avoid generating 25% LO clocks for SAW-less GPS applications. Although it simplified the LO generation circuitry, its overall performance does not advance the conventional 25% LO quadrature mixer at GPS operational frequency. We proposed an N-path filter structure with pass-transistor-based AND-gate switches driven by quadrature 50% LO clocks to achieve the nonoverlapping operation at the mm-wave frequencies. In this context, as exhibited in Fig. 7.10, each path's capacitor is connected to the

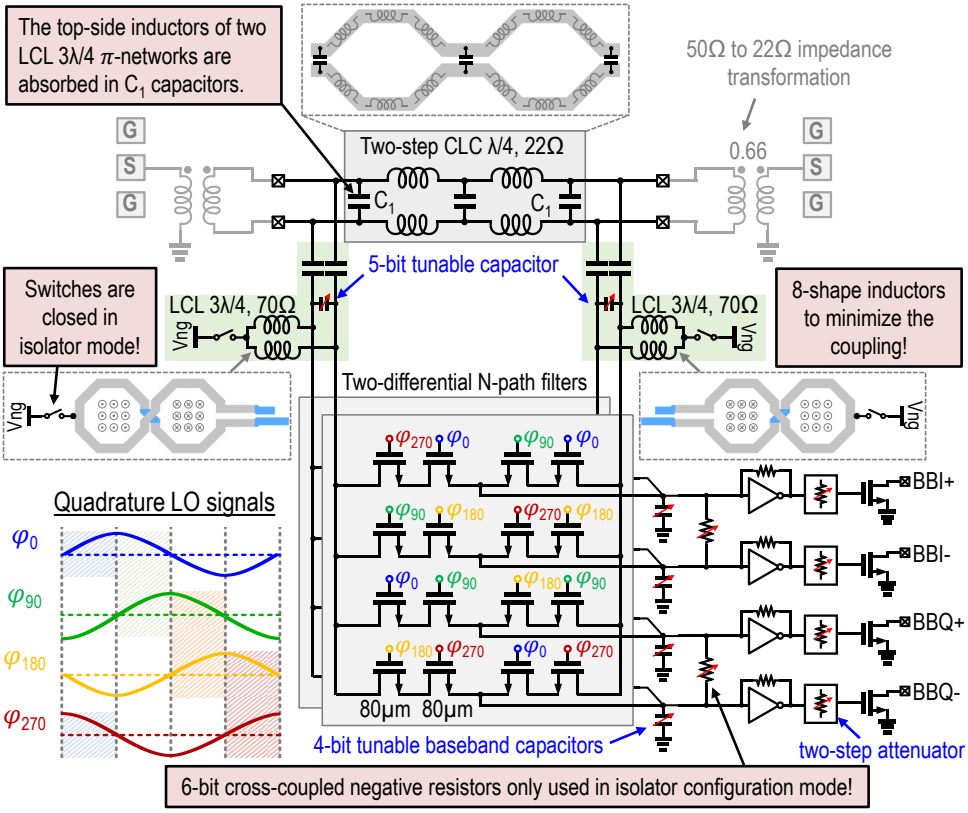


Figure 7.11: The schematic of the proposed circulator/isolator.

shared RF node when both switches are ON, replicating bitwise AND-gate operation and resembling 25% nonoverlap switching. The switches can be driven by sinusoidal LO signals, which enables utilizing inductors to resonate out the parasitic capacitors of the switches.

7.3.2. DESIGN CHOICES

As mentioned, this paper intends to study the feasibility of implementing two separate structures. Therefore, the design choices are made to address the requirements of both architectures instead of optimizing one's performance. Unlike the nonreciprocal delay, which can be implemented only in differential, the N-path filter can be implemented single-ended or differential. We chose differential to place the circulator between PA and Balun. Hence, the Z_0 is smaller (22Ω instead of 50Ω), thus, the inductors are smaller. Moreover, the power handling of the circulator/isolator is higher in the differential mode, and it can be scaled further by reducing Z_0. To increase output power, we need to decrease the PA's required optimum load (R_{opt}), which scales power handling accordingly. Nonetheless, the differential structure offers less conversion gain and NF in the FDD

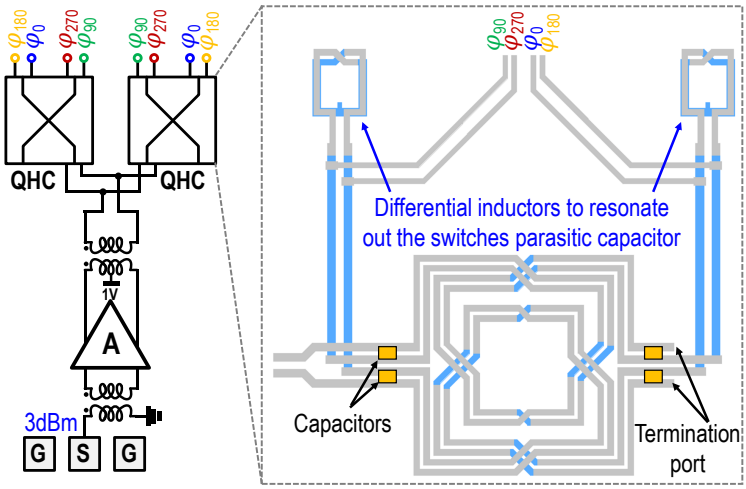


Figure 7.12: The schematic of quadrature LO generator and the 2D layout view of the implemented QHC.

frontend configuration. Its performance also suffers from step-down impedance and Balun loss. The required $P_{TX} - NF > -13.79dBm$ can be achieved since the power handling is higher. Additionally, the differential structure possibly offers a higher AIP2.

7.4. CIRCUIT IMPLEMENTATION

Fig. 7.11 demonstrates a detailed schematic of the proposed mm-wave circulator/isolator featuring two back-to-back AND-gate switching N-path filters. A two-step lumped-element CLC π-network is employed to realize the circulator's PA-to-antenna QTL. Its equivalent impedance Z_0 is set to 22Ω to match R_{opt} as integrated into a PA's matching network. Two 70Ω LCL π-networks are utilized to form the circulator's remaining QTLs. They connect the TX and antenna ports to the LPTV circuit and perform DC blocking. Here, the LCL's top side inductors are absorbed in C_1. Accordingly, the proposed LPTV circuit is implemented by two-differential N-path filters (Fig. 7.10), whose switches are realized by NMOS transistors with relatively large channel width (80μm) to minimize their ON-resistance (R_{SW}). The parasitic capacitors of the switches are resonated out by two differential inductors, which are combined with LCL's bottom-side inductors. Additionally, two 5-bit tunable capacitors are employed to adjust the resonance frequency. As depicted, the inductors are implemented with an 8-shape to minimize the unwanted couplings, thus enabling a compact layout.

The down-converted baseband signals are amplified by self-bias inverter-based transconductance amplifiers and their subsequent open-drain NMOS transistors. A two-step attenuator is implemented in each baseband path, providing possible attenuations of 8-dB and 16-dB. Besides, 4-bit tunable capacitors are utilized in the baseband to control the RX bandwidth slightly.

As discussed, negative resistors are utilized in the baseband to provide matching conditions for the clockwise propagating waves in the isolator configuration. The negative

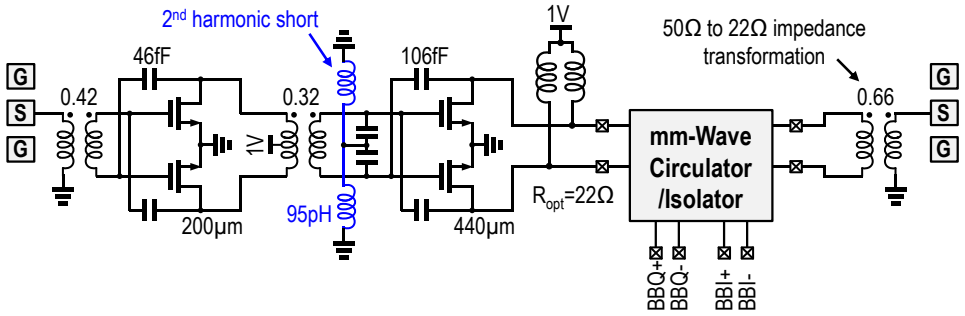


Figure 7.13: The schematic of the proposed PA with an integrated circulator/isolator.

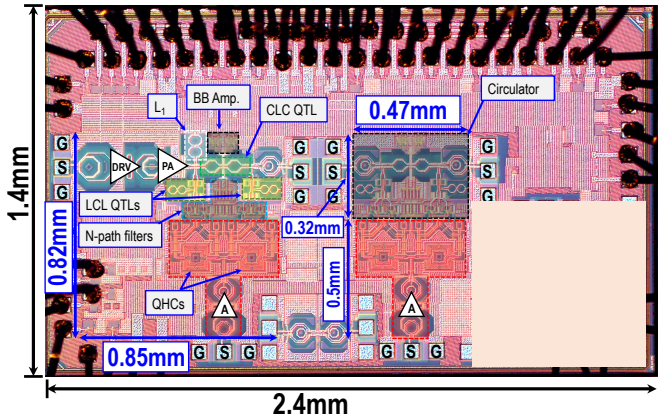


Figure 7.14: Die micrograph of the proposed PA with an integrated circulator/isolator.

resistors are implemented using 6-bit switchable cross-coupled NMOS transistors. Their supply voltage (V_{ng}) is provided from the center tap of the 8-shape inductors. Note that the center tap is open when the circulator configuration is employed.

Fig. 7.12 exhibits the implemented quadrature LO generator. Two differential transformer-based quadrature hybrid couplers (QHCs) generate the mm-wave sinusoidal quadrature LO clocks. Two differential inductors are used to resonate out the parasitic capacitors of the N-path filter's switches. Moreover, a neutralized common-source input amplifier provides the required LO power level of QHCs.

Fig. 7.13 demonstrates the schematic of the proposed PA with an integrated circulator/isolator. The circulator/isolator is located between the PA and the output balun. A neutralized common-source push-pull PA is designed with input second harmonic short condition to boost its linearity. Besides, an 8-shape symmetrical inductor resonates out the parasitic capacitors of the PA and provides its DC feed. Finally, a neutralized common-source pre-driver is implemented to drive its following PA.

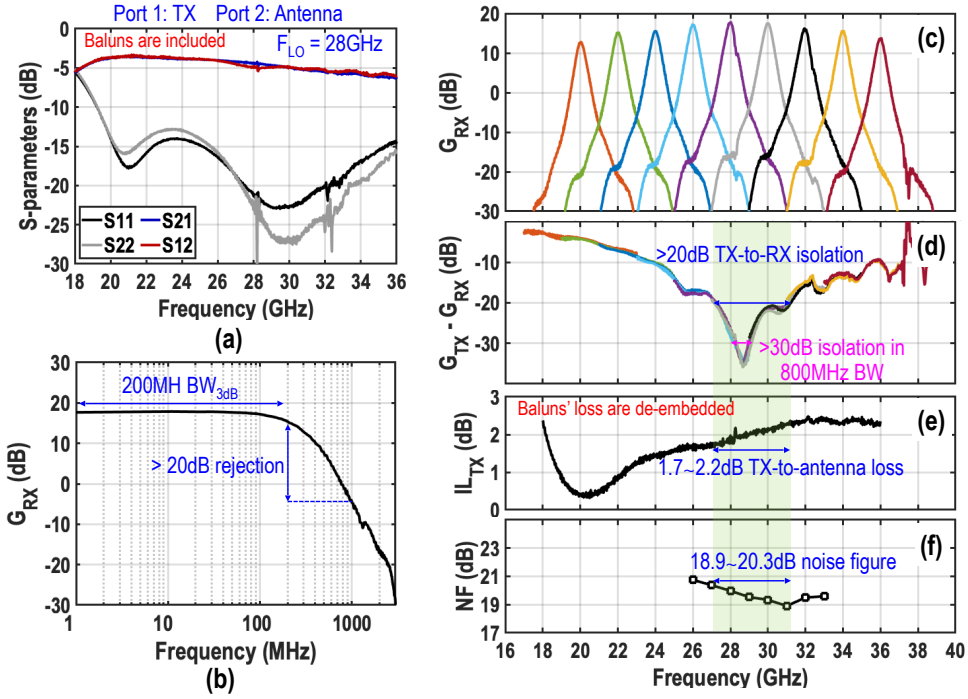


Figure 7.15: The measured (a) Small-signal s-parameter, (b) RX gain versus baseband frequency, (c) RX-gain at various LO frequencies, (d) TX-to-RX isolation, (e) noise figure, and (f) TX-to-antenna insertion loss over the 20-to-36GHz band.

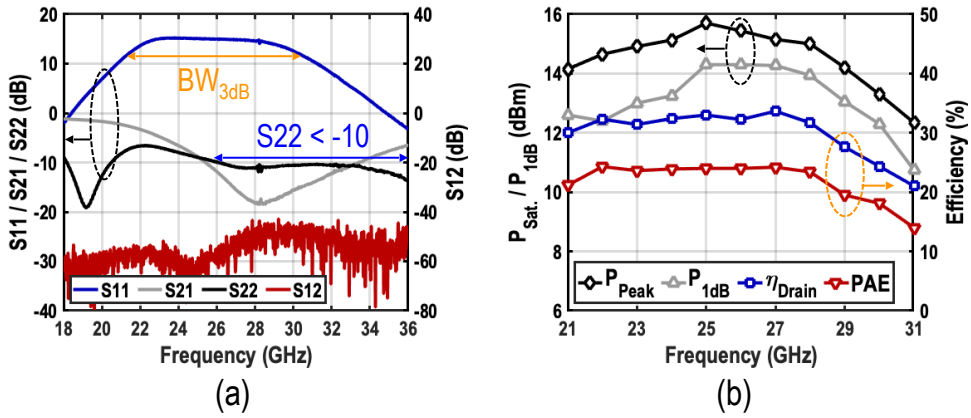


Figure 7.16: (a) Small-signal s-parameter and (b) large-signal CW measurement results of the TX path.

7.5. MEASUREMENT RESULTS–PART I: "A FDD TRX FRONT-END"

Fig. 7.14 exhibits the die micrograph of the mm-wave PA with an integrated circulator/isolator and the standalone mm-wave circulator/isolator. The chip is fabricated

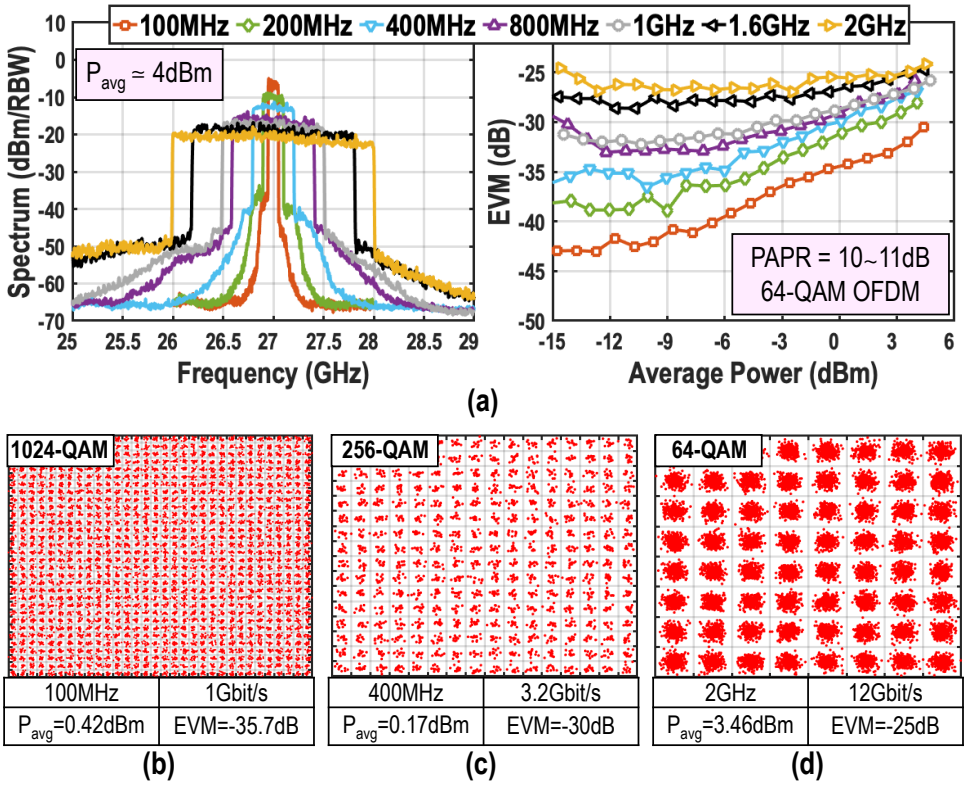


Figure 7.17: (a) The 64-QAM OFDM signals spectrum and EVM versus output power of the TX path for various modulation bandwidths. The measured constellations of (b) 1024-QAM, (c) 256-QAM, and (d) 64-QAM OFDM signals.

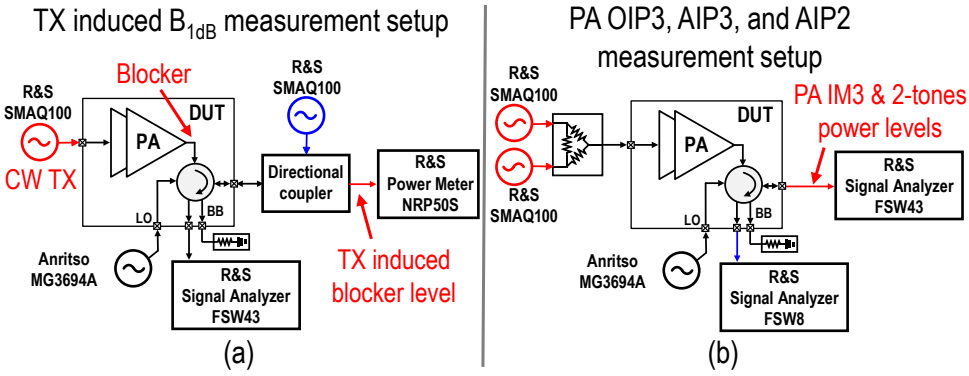


Figure 7.18: The measurement setup for (a) TX induced B_{1dB} and (b) OIP3 of the PA and antenna-port referred IP2/IP3 measurements.

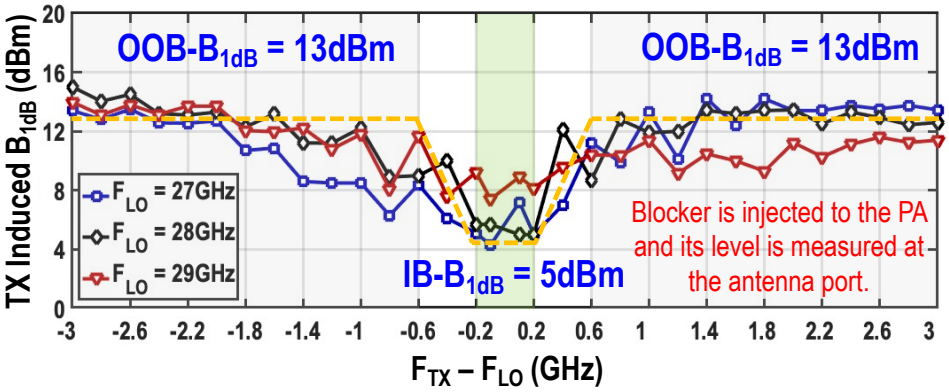


Figure 7.19: The measured TX induced B_{1dB} at various carrier frequencies.

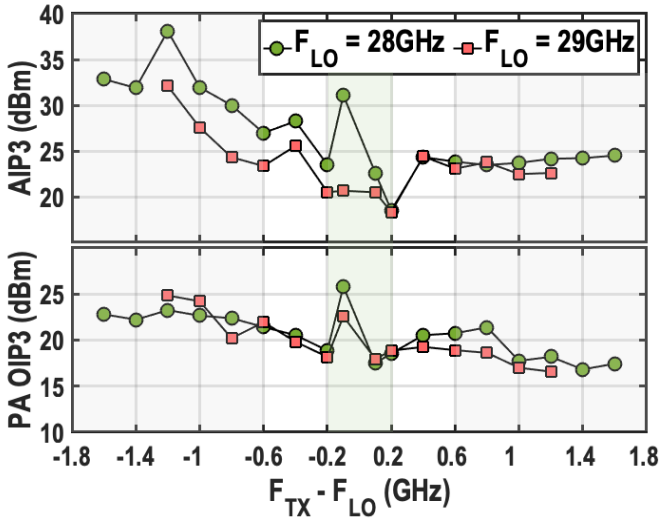


Figure 7.20: The measured PA OIP3 and FDD front-end AIP3.

in 40-nm bulk CMOS technology. The core area occupied by the proposed circulator/isolator, its LO generators, and baluns is 0.38mm^2, while the PA with an integrated circulator/isolator occupies 0.7mm^2. All measurements are performed using a high-frequency probe station. The DC supplies, bias voltages, digital control signals, and RX baseband signals are wire-bonded directly to an FR4 printed circuit board (PCB). This work uses a 1-V supply voltage for the pre-driver, PA, and LO amplifier, while 1.4-V is used for baseband self-biased transconductances. This section presents the measurement results for the circulator/RX configuration to support the mm-wave FDD frontend. Note that the cross-coupled negative resistors are off in this configuration, and the switches at the circulator's 8-shape inductors' center tap are open.

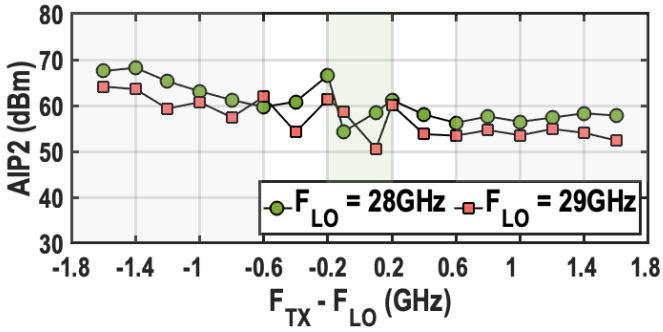


Figure 7.21: The measured FDD front-end AIP2.

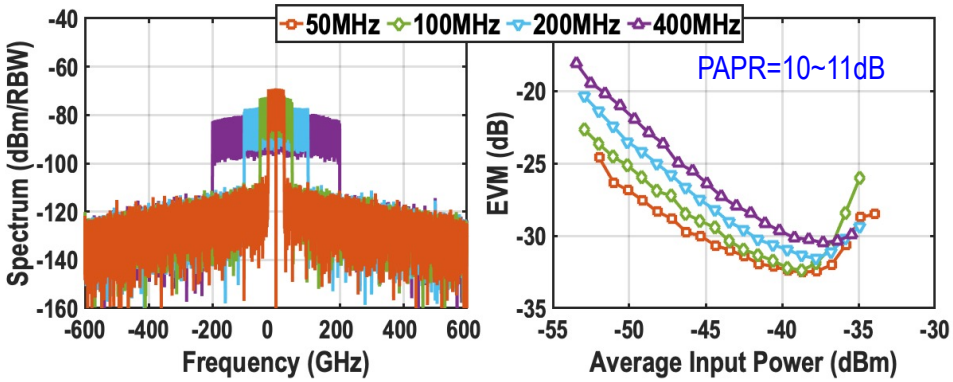


Figure 7.22: The OFDM signal measurement results of the RX path.

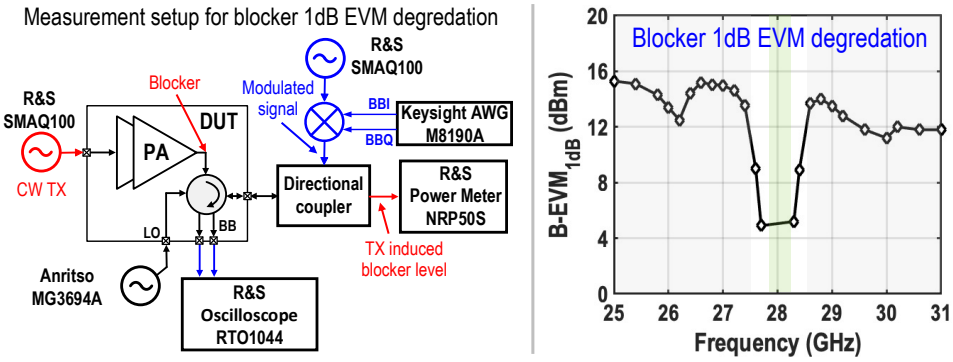


Figure 7.23: The RX EVM degradation under the OOB CW TX blocker measurement setup and results.

7.5.1. CIRCULATOR PERFORMANCE

Fig. 7.15 exhibits the s-parameter measurement results of the circulator, including its baluns' loss. The RX achieves 400 MHz 3 dB bandwidth (BW_{3dB}) with 18 dB gain and

20 dB rejection at 1 GHz spacing away from the carrier frequency. Moreover, the circulator is widely tunable over a 22-to-36GHz band trade-off, which exists in a 30 dB TX-to-RX isolation in an 800 MHz bandwidth. It also offers >20 dB isolation within the 27.1-to-31.1 GHz band. The measured IL_{TX} is 1.7~2.2 dB, and the noise figure (NF) is 18.9~20.3 dB in the same band. Note that the measured NF includes the insertion-loss/NF of the circulator and the mixer-first down conversion path. Nonetheless, its NF is limited mainly by the impedance transformation ratio of the balun ($50\,\Omega \rightarrow 22\,\Omega$) and the double-balanced passive down-conversion mixer's topology. Therefore, there is a trade-off between PA power handling and RX's NF. Here, we prioritized the PA power handling for the benefit of the isolator configuration. Nevertheless, employing more advanced technology nodes that offer lower switching impedance with much lower parasitic capacitors can improve RX performance and IL_{TX}, thus increasing TRX's link budget.

7.5.2. TX PERFORMANCE

Fig. 7.16 demonstrates the small-signal and large-signal performance of the TX path. The s-parameter measurement results show that the integrated PA offers almost 10 GHz BW_{3dB} with 15.4 dB small-signal gain. Owing to the relatively low measured IL_{TX}, the PA achieves 15.15 dBm peak power at the antenna port with 33%/24.2% drain-efficiency/PAE. Its P_{1dB} also exceeds 14 dBm. The spectrum and EVM of the modulated 64-QAM OFDM signals with various modulation bandwidths, up to 2GHz, are depicted in Fig. 7.17. Additionally, the measured constellations of 1024-QAM, 256-QAM, and 64-QAM OFDM signals are shown, achieving up to 12Gbit/s data rate which is limited by measurement instruments.

7.5.3. RX PERFORMANCE

As illustrated in Fig. 7.18 (a), RX gain compression under a large blocker is measured when the CW blocker signal is applied to the PA, and its power is measured and reported at the antenna port. The measured TX induced B_{1dB} at various carrier frequencies are demonstrated in Fig. 7.19, where the frontend achieves better than 5dBm IB TX induced B_{1dB} while its OOB TX induced B_{1dB} is 13 dBm, confirming its capability to support FD and FDD TRX operations. Additionally, OIP3 of the PA and AIP2/AIP3 of the fully integrated FDD frontend are measured using the measurement setups shown in Fig. 7.18 (b). Fig. 7.20 presents the measured PA OIP3 and FDD frontend AIP3. A class-AB biasing condition is employed to diminish PA's OIP3 contribution to AIP3, while the second harmonic is shorted at PA input. Furthermore, the measured AIP2 is depicted in Fig. 7.21. As discussed, the FDD frontend may require a higher OOB AIP2, depending on the modulation bandwidth and number of antennas. Hence, a better layout practice, an improved ground and supply isolation, and an IIP2 calibration can potentially improve AIP2.

Moreover, Fig. 7.22 exhibits a 64-QAM OFDM spectrum and EVM with modulation bandwidths up to 400MHz. The RX EVM degradation under the OOB CW TX blocker is also measured. In this case, the level of CW TX blocker causing 1 dB degradation in EVM of a 400 MHz OFDM is measured as shown in Fig. 7.23. As a result, the proposed frontend can support FDD. However, for FD applications, an additional SIC is required.

Lastly, Fig. 7.24 demonstrates full FDD measurement results, where a -35 dBm 400 MHz 64-QAM OFDM RX signal at 28GHz carrier frequency is injected to the antenna

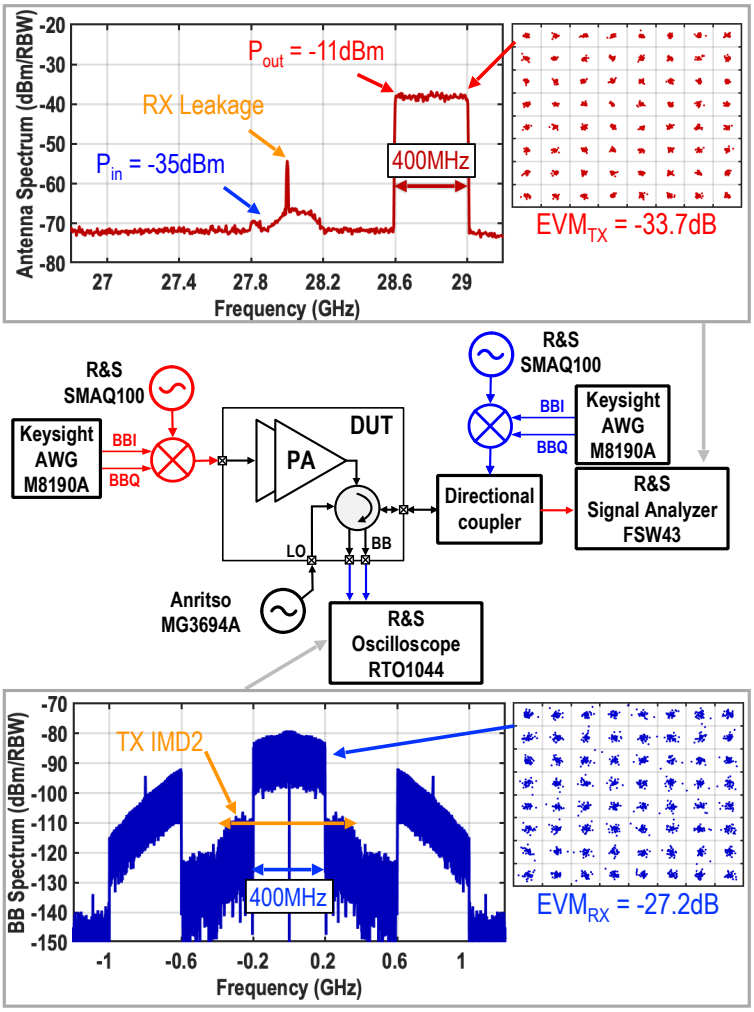


Figure 7.24: A full simultaneously transmit and receive FDD measurement results. A -35dBm 400MHz 64-QAM OFDM RX signal at 28GHz carrier frequency is injected into the antenna port through a directional coupler. Simultaneously, a -11dBm 400MHz 64-QAM OFDM TX signal at 28.8GHz carrier frequency is delivered to the antenna port by the PA.

port, while a -11 dBm 400 MHz 64-QAM OFDM TX signal at 28.8GHz carrier frequency is delivered to the antenna port. Note that TX IMD2 limits the PA's output power and requires further IIP2 calibration. The baseband spectrum shows >40dB TX suppression owing to TX-to-RX isolation of the circulator and suppression of the N-path filter down-converter.

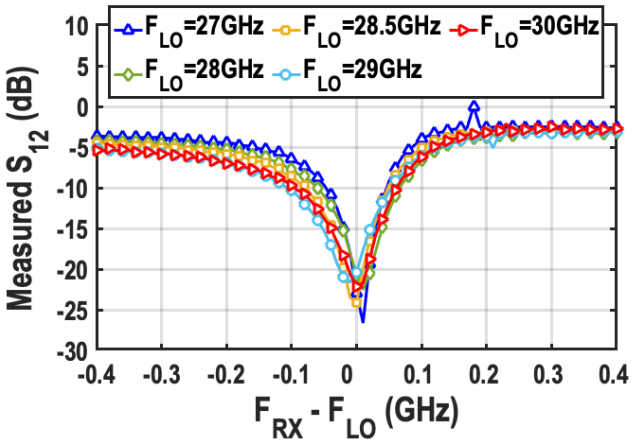


Figure 7.25: The measured S_{12} of the stand-alone isolator while cross-coupled negative resistors are on.

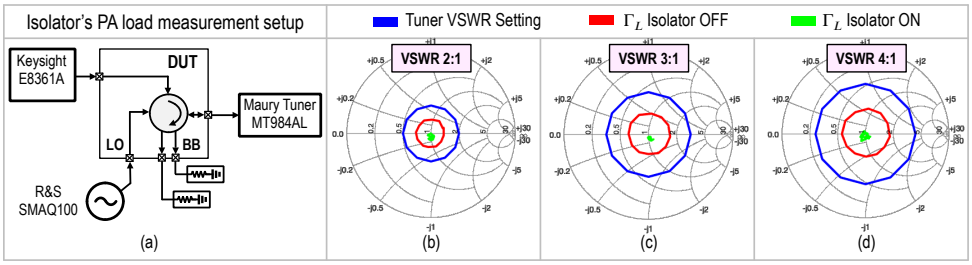


Figure 7.26: (a) The simplified measurement setup. The measured load provided by the isolator for (b) VSWR 2:1, (c) VSWR 3:1, and (d) VSWR 4:1.

7.6. MEASUREMENT RESULTS–PART II: "A VSWR RESILIENT POWER AMPLIFIER"

This section presents the measurement results of the isolator configuration, where the switches at the circulator's 8-shape inductors' center tap are connected to a 0.7-V supply. Using 6-bit control settings, a fraction of cross-coupled negative resistors turn on to achieve reverse isolation in the isolator. As we expected, Fig. 7.15 (a) shows that in the standalone circulator configuration, S_{12} is almost equal to S_{21}, achieving no reverse isolation. In contrary, Fig. 7.25 reports the measured S_{12} of the stand-alone isolator configuration, showing >15dB reverse isolation. This reverse isolation is necessary to provide optimum loading conditions for the PA independent from the actual antenna load.

Fig. 7.26 (a) presents the simplified setup used to measure the load provided by the isolator for the PA. Fig. 7.26 (b-d) exhibits the measured load at 28.5 GHz, where the blue line is the VSWR of the antenna provided by the load tuner, the red line is the load seen by the PA when the isolator is off, and the green line is the load seen by the PA when the isolator is on. The measurement results confirm that the isolator can always provide a

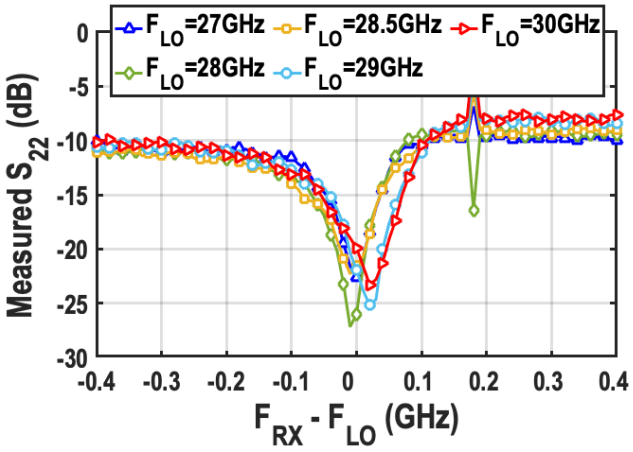


Figure 7.27: The measured S_{22} of the PA with the integrated isolator while cross-coupled negative resistors are on.

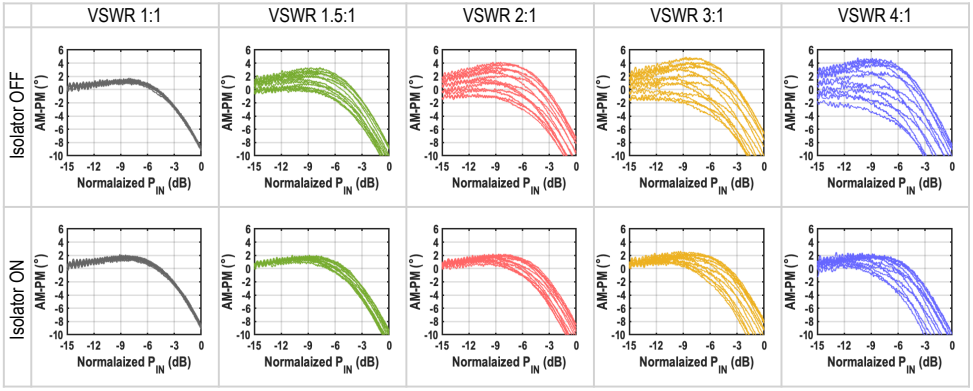


Figure 7.28: The measured AM-PM distortions of the PA with and without isolator's contribution.

perfect optimum load for the PA even for voltage standing wave ratios (VSWR) 4:1. Note that the radius of the red circle is smaller than the antenna VSWR circle owing to the loss of the balun and the circulator/isolator.

Furthermore, the PA with the integrated isolator is evaluated. As shown in Fig. 7.16 (a), S_{22} of the PA in the FDD frontend configuration is around 10 dB. However, since the signal injected from the antenna port is absorbed in the isolation configuration, S_{22} is expected to be improved. Fig. 7.27 exhibits the measured S_{22} of the PA when a fraction of the cross-coupled negative resistors are on. As shown in Fig. 7.9, a narrow band S_{12} and consequently a narrow band S_{22} was expected as we chose a larger Z_1 value compared to Z_0. Nonetheless, the bandwidth can be improved by selecting a smaller Z_1 in the cost of higher $\mathrm{IL_{TX}}$.

Lastly, we measured the amplitude-to-phase (AM–PM) distortions of the PA versus

Table 7.1: Silicon-Based mm-Wave PAs Performance Comparison

		Nonreciprocal Circulators / RXs			Blocker Tolerant RX / Filter			FD/FDD TRX	
Parameter	**This Work**	Reiskarimian ISSCC 2017	Dinc ISSCC 2017	Garg ISSCC 2021	Boynton RFIC 2020	Song RFIC 2020	Hari RFIC 2021	Mondal ISSCC'19	Shahramian RFIC'22
Architecture	PA with an integrated N-path filter based isolator/circulator/RX	N-path filter based circulator RX	Circulator with nonreciprocal delay	FD circulator RX with SIC	Series mixer-first RX	Mixer-first RX with passive Elliptic LPF	Reflection-mode N-path filter	Separate antenna TRX	FDD Module-on-glass TRX
Technology	40nm CMOS	65nm CMOS	45nm SOI	45nm SOI	65nm CMOS	65nm CMOS	45nm SOI	65nm CMOS	130nm SiGe
Core Area (mm²)	0.7 (FD/FDD front-end), 0.38 (Circulator RX)	0.94	2.16	4.54	NR	0.63	2.25 (Die)	0.48 (Single channel)	12.4 (Die) 1040 (Module)
Supply (V)	1 (PA + LO), 1.4 (BB)	2.4	NR	NR	NR	1.2	1→1.3	1	3.3
Frequency (GHz)	TX: 21-31, RX: 22-36	0.61-0.975	22.7-27.3	25.5-27.75	9-31	21-29	6-31	28 & 37	71-76 & 81-86
G_{RX} (dB)	18	28	-3.2 (Ant. to RX)	16.1	40	3-6	-6 @28GHz*	16.1 & 10.9	72
RX BW_{3dB} (MHz)	400	20	NA	800	NR	500	1-1.22GHz	500	4000
NF (dB)	18.9–20.4	6.3	3.3–4.4 (without RX)	5.8	12.5–17	12–14.5	18.5 @28GHz*	6.2 & 7.0	6.6-7.9 & 7.2-8.4
IB IIP3 (dBm)	2.8	-18.4	NA	NR	NR	NR	6.3	NR	>0 (?)
OOB IIP3 (dBm)	15 (ΔF/BW=1.5)	15.4 (ΔF=500MHz)	NA	NR	21*	NR	20 (ΔF/BW=1)	NR	NR
IB B_{1dB} (dBm)	5†	NR	NA	11.5 (with SIC)	-45*	-6	-8*	NR	NR
OOB B_{1dB} (dBm)	13† (ΔF/BW=1.5)	NR	NA	NR	-6→4	3.4 (ΔF/BW=2)	4.4 (ΔF/BW=1)	NR	NR
TX-to-antenna insertion loss (dB)	1.8 @ 28GHz	1.8	3.3	3.1	NA	NA	NA	NA	2.5-3*
TX-to-RX isolation (dB)	>30 (28.3-29.1GHz) >20 (27.1-31.1GHz)	26* / 40 (with Bal. Network)	>18.5	53 (with SIC)	NA	NA	NA	NA	>40
P_{DC} (mW)	LO buffer: 89 Baseband: 19.9	108	78.4	RX: 88 SIC: 23.5	72→162	22.8	146-384	37.6 (Single channel)	RX#: 2000 TX#: 3200

*Graphically estimated †Blocker signal is applied to the PA, and its level is measured at the antenna port #Single supply including LDOs, configuration and calibration functions.

load VSWR. Fig. 7.28 compares the measured AM-PM distortions of the PA with and without the isolator's contribution. Note that we reported 12 measurement results for VSWR 1:1 to show the repeatability of the measurements. As demonstrated, the isolator provides a relatively high VSWR resiliency at the lower powers. However, moving towards peak power, the AM-PM improvement degraded due to the saturation of the switches. As such, the voltage swing at the N-path filter nodes can be reduced by choosing a smaller Z_1 in the cost of higher IL_{TX}.

Table 7.1 summarizes the measured results of the proposed mm-wave frontend and compares it with that of the state-of-the-art in three different modes of operation, namely, non-reciprocal circulators/RXs, blocker tolerant RX/filters, and FD/FDD frontend. To the best of the author's knowledge, the realized prototype is the first reconfigurable fully integrated mm-wave FDD frontend featuring integrated PA, isolation, circulator, and receiver.

7.7. CONCLUSION

This chapter features a fully integrated mm-wave FDD frontend, comprising a two-stage PA, an integrated circulator as the duplexer, and a mixer-first RX implemented as a part of the circulator. The proposed circulator/isolator is realized by utilizing an advanced ring quarter-wave transmission line topology with adjusted characteristic impedances to improve TX-to-antenna insertion loss and TX-to-RX isolation at the cost of a narrower bandwidth. The implemented circuitlator's LPTV circuit consists of an AND-gate switching-based N-path filter, enabling a mixer-first RX operation. As a proof of concept, a configurable prototype chip is realized in 40-nm bulk CMOS whose circulator occupies only 0.38 mm^2 core area thanks to the ultra-compact N-path filter structure.

Including its isolator's loss, the PA delivers 15.15 dBm peak output power with 33% drain efficiency. The realized frontend prototype occupies only 0.7mm^2, including circulator, PA, quadrature hybrid coupler LO generators, and baseband circuits. The functionality of the proposed FDD frontend is evaluated by a STAR measurement with 400 MHz TX/RX modulation bandwidth and channel spacing. Moreover, the PA with the integrated isolator showed a significant VSWR resiliency at the lower power level. However, its robustness against VSWR was degraded around its peak output power.

8

CONCLUSION

8.1. THESIS OUTCOME

In this dissertation, our goal was to present novel TX/PA architectures designed to align with the essential key performance indicators (KPIs) of mm-wave phased-array transceivers, taking into account their practical challenges. Our aim was to leverage the opportunities presented by mm-wave technology while minimizing the need for tuning and calibration of phased-array TXs.

Achieving high power back-off (PBO) efficiency in Power Amplifiers (PAs) is a KPI for mm-wave 5G transmitters (TX). Therefore, our first objective is to develop a wideband Doherty PA that can achieve near-ideal 6dB PBO efficiency enhancement. Building on this, we extend the load modulation concept of the Doherty PA, not just for efficiency gains but also to enhance linearity. This leads to the introduction of a load-modulation-based architecture designed to cancel third-order intermodulation distortion (IMD3), addressing the stringent linearity requirements of 5G systems.

Another significant challenge in phased-array PA design is managing the time-varying voltage standing wave ratio (VSWR) caused by mutual coupling between antenna elements. Our second objective is to improve PA KPIs such as PBO efficiency and output power while ensuring stable performance under varying VSWR conditions. We introduce a novel N-way balanced power combiner to achieve higher output power and enhance the VSWR resilience of balanced amplifiers. Additionally, by utilizing a balanced amplifier structure, we ensure that the proposed Doherty PA maintains its performance even under load mismatch. The integration of a quadrature hybrid coupler enables the implementation of a second image-rejection stage in the direct upconversion TX architecture, effectively maximizing the image-rejection ratio and eliminating the need for I/Q mismatch calibration.

While low- and mid-band 5G standards employ both Time Division Duplexing (TDD) and Frequency Division Duplexing (FDD), only TDD has been considered for high-band systems. This thesis explores alternative duplexing methods, including FDD, which separates transmission and reception into different frequency bands, and Single-Frequency

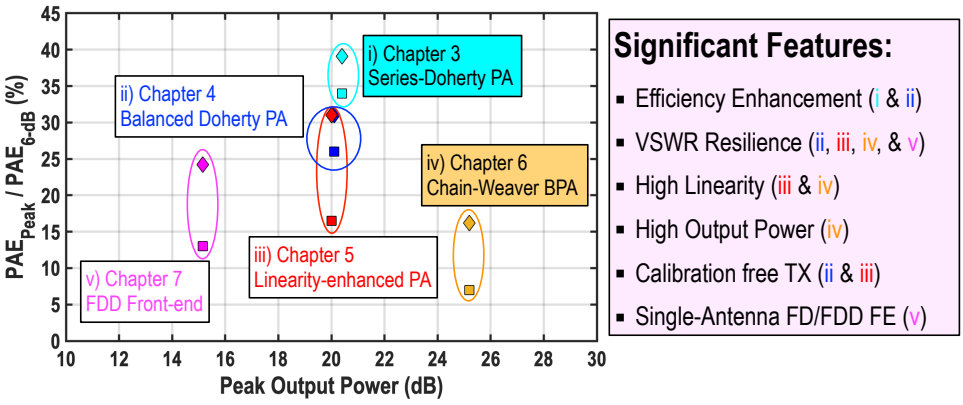


Figure 8.1: Peak and 6dB power back-off PAE of five distinct TX frontend solutions operating at the 24-to-42GHz band presented in this thesis.

Full-Duplex (SF-FD), which allows both operations on the same frequency.

Illustrated in Fig. 8.1, we outlined five distinct TX frontend approaches providing peak output power ranging from 15 to 25.2dBm, effectively tackling critical KPIs like linearity, VSWR resilience, and efficiency. Our contribution to advancing mm-wave TX frontend technology can be summarized as follows.

- A wideband series-Doherty PA to achieve close to ideal (2x compared to a class-B PA efficient curve) 6-dB PBO efficiency (Chapters 3, 4, 5);
- Implementation and test of the post-silicon inter-stage passive validation approach to evaluate the mm-wave chip prototypes (Chapter 3);
- An efficiency-enhanced balanced PA for addressing the load sensitivity of the efficiency enhancement PA architectures (Chapter 4);
- Design, implementation, and validation of a mm-wave double-quadrature direct upconverter with inherently high image-rejection ratio (Chapter 4);
- The introduction of the load-modulation based IMD3 cancellation technique (Chapter 5);
- The pioneering of an N-way Chain-Weaver Balanced PA with embedded power and impedance sensor (Chapter 6);
- Proposing an mm-wave N-path filter structure and ring quarter-wave transmission line topology with adjusted characteristic impedance for realizing an ultra-compact low-loss CMOS circulator (Chapter 7);
- Design, implementation, and full-scale experimental validation of the first fully integrated FDD TRX front-end (Chapter 7);
- Design, implementation, and testing of the first PA with integrated isolator (Chapter 7).

8.2. CONCLUSION AND CONTRIBUTIONS TO THE STATE-OF-THE-ART

The wideband series-Doherty PA introduced in **Chapter 3** represents a significant advancement in mm-wave 5G transmitter design, particularly in terms of efficiency and bandwidth. Unlike traditional parallel-Doherty PAs, which often suffer from limited bandwidth and efficiency degradation at PBO, the proposed series-Doherty PA architecture employs a two-step impedance inverting-based combiner that maintains high efficiency across a broad frequency range. Experimental results demonstrate that this PA achieves superior 6dB PBO efficiency outperforming state-of-the-art. Compared to traditional Doherty PAs, which typically operate efficiently over a narrow bandwidth, our design offers a more versatile solution that is well-suited for the wideband requirements of modern mm-wave systems, thereby pushing the boundaries of current PA technology and setting a new benchmark for future designs.

In **Chapter 4**, the proposed balanced TX architecture, incorporating a double-quadrature direct upconverter and a Doherty-balanced PA, delivers substantial improvements in both linearity and efficiency for mm-wave phased-array systems. The double-quadrature architecture stands out by significantly reducing in-band distortion and enhancing spectral purity, addressing key limitations found in traditional TX designs without requiring any calibration. Simultaneously, the balanced Doherty PA structure enhances system robustness, particularly in handling VSWR variations, which are critical in phased-array applications. Unlike conventional efficiency enhancement approaches that often struggle to maintain performance under varying load conditions, the integration of series-Doherty PA with a balanced PA framework provides a superior solution that maintains high efficiency and linearity across a wide range of operating conditions. This work contributions set a new standard by achieving excellence in both efficiency and linearity without relying on any calibration and tuning, paving the way for more reliable and high-performance mm-wave 5G systems.

Chapter 5 presents a novel approach to improving linearity in class-B CMOS PAs for mm-wave applications through load-modulation-based IMD3 cancellation. By carefully optimizing the biasing and load conditions, the proposed technique effectively cancels out IMD3 components, which are typically a significant challenge in conventional class-B PAs, particularly at higher frequencies. This advancement allows for superior linearity without sacrificing efficiency, a balance that is often difficult to achieve in traditional PA designs. When compared to state-of-the-art linearization techniques, which often require complex circuitry or sacrifice efficiency, this method provides a simpler and more power-efficient solution. The resulting PA design not only meets but exceeds the linearity requirements for mm-wave 5G systems, offering a significant improvement over existing solutions.

In **Chapter 6**, the development of the N-Way Chain-Weaver Balanced PA introduces an architecture that enhances the performance and reliability of mm-wave phased-array TXs. This balanced PA integrates an embedded impedance and power sensor, allowing real-time monitoring and adjustment to optimize output power and maintain consistent performance under varying VSWR conditions. The Chain-Weaver architecture extends the traditional balanced PS's VSWR resilience, ensuring robust operation across a wide range of scenarios. When compared to state-of-the-art PA designs, this approach offers superior resilience and adaptability, marking a significant advancement in PA technology for mm-wave applications. The combination of improved VSWR resilience, real-time performance optimization, and high output power positions this architecture as a leading solution for next-generation 5G systems, addressing key challenges in phased-array deployment.

Chapter 7 introduces a fully integrated FDD transceiver front-end and a PA with an embedded isolator, advancing the state-of-the-art in mm-wave 5G communication systems. The proposed transceiver front-end leverages a novel CMOS circulator architecture, providing effective isolation between transmission and reception paths while maintaining a compact and scalable design. The integration of the PA with the isolator further enhances system performance by minimizing signal interference and ensuring stable operation across a wide range of operating conditions. Unlike traditional FDD systems that rely on bulky and costly off-chip components, this integrated solution of-

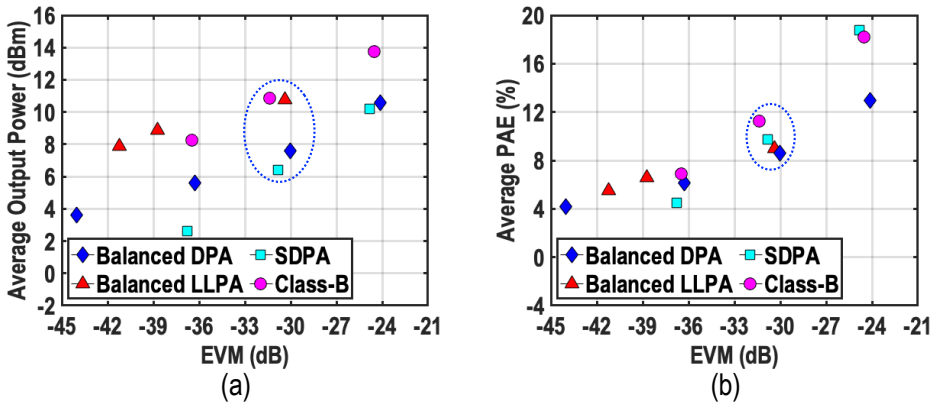


Figure 8.2: Comparision of measured average (a) output power and (b) PAE of four PA configurations while supporting a 64-QAM OFDM with 9 to 10dB PAPR.

fers a more efficient and cost-effective approach, significantly reducing the overall footprint and complexity. When compared to existing transceiver designs, this architecture stands out for its high level of integration, improved isolation, and scalability, setting a new benchmark for fully integrated mm-wave solutions in next-generation 5G applications.

8.2.1. DOES EFFICIENCY-ENHANCEMENT LEAD TO THE HIGHEST SYSTEM EFFICIENCY?

As discussed in Chapter 3, while the Doherty PA achieves efficiency enhancement, it also introduces inherent amplitude-to-amplitude (AM-AM) and amplitude-to-phase (AM-PM) distortions. These distortions impact the PA's average efficiency because a certain Error Vector Magnitude (EVM) must be maintained, necessitating operation at deep power back-off (PBO) to meet the required EVM. In contrast, although a linear PA does not benefit from efficiency enhancement, its superior EVM performance allows it to satisfy the required EVM at a higher average power, resulting in relatively high average efficiency.

Figure 8.2 compares the output power and average efficiency versus EVM for four PA architectures: 1) a balanced Doherty PA (Balanced DPA), 2) a balanced load-modulated linear PA (Balanced LLPA), 3) a series-Doherty PA (SDPA), and 4) a class-B PA. Targeting an EVM of -30.5dB, Fig 8.2(a) demonstrates that the linear PAs provide 2-3dB higher average output power compared to their Doherty counterparts while maintaining comparable average PAE. **This suggests that although Doherty PAs offer superior PBO efficiency, linear PAs deliver better overall performance when low EVM is required. It also indicates that to maximize TX system efficiency, a Doherty PA should be paired with digital pre-distortion (DPD).**

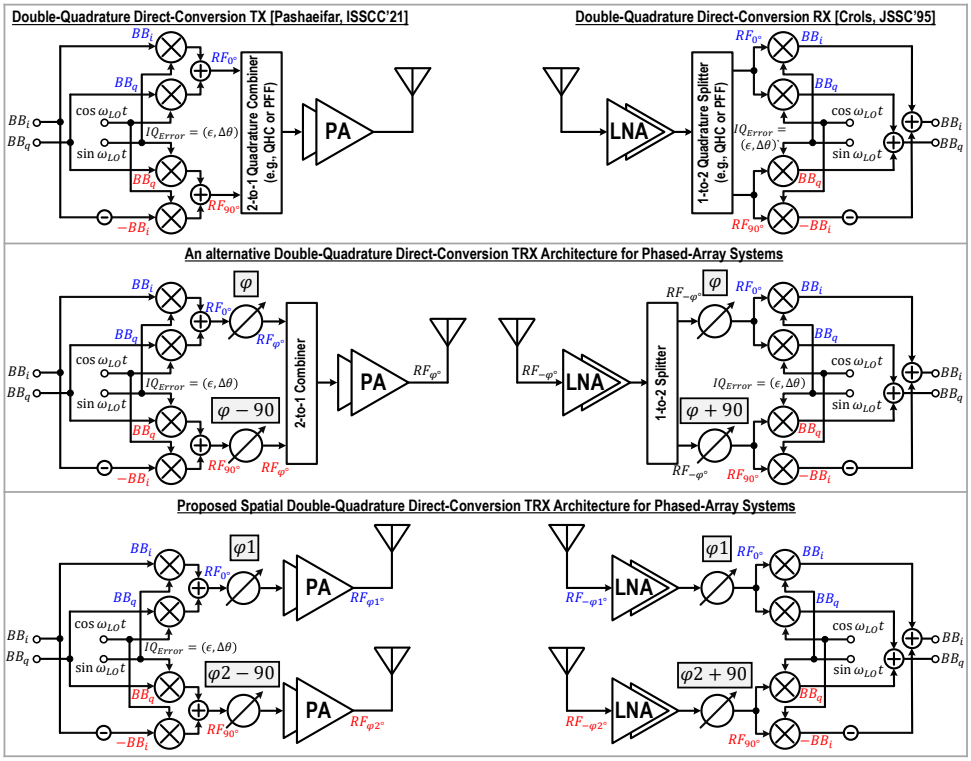


Figure 8.3: Conventional double-quadrature TRX and proposed spatial double-quadrature TRX architectures.

8.3. SUGGESTIONS FOR FUTURE DEVELOPMENTS

The research presented introduces various TX frontend architectures characterized by their high efficiency, linearity, and resilience to VSWR. Additionally, it lays the foundation for future studies to advance mm-wave phased-array systems.

- The AM-AM/AM-PM performance of the load-modulated Doherty PA for broadband operation is analyzed in Chapter 3. Since AM-PM degradation across frequencies is foreseeable, restoring linearity involves integrating a tunable element into the matching network to fine-tune the resonating frequency. Additionally, CMOS Doherty PAs often grapple with notable memory effects stemming from adaptive biasing circuits, presenting two key challenges: 1) mismatch between adaptive biasing delay and main path group delay, and 2) asymmetric rising and falling bias voltage shapes from the adaptive biasing circuit. Hence, employing a wideband adaptive biasing circuit with symmetric output transitions can significantly enhance DPA linearity and bolster EVM when handling signals with wide modulation bandwidths.

- As mentioned in Chapter 1, novel mm-wave phased-array TRX architectures can be introduced to improve the performances, such as security [13], SNR,

and I/Q mismatch by over-the-air (OTA) combining the signals. In this context, we propose extending the double-quadrature architecture to spatial double-quadrature TRX. The conventional double-quadrature TX (see Chapter 4) and RX architecture (depicted in Fig. 8.3 top) require two I/Q de-/modulators for down/up converting RF_{0° and RF_{90°, along with a quadrature splitter/combiner, which poses a drawback. As an alternative (illustrated in Fig. 8.3 middle), the quadrature splitter/combiner can be replaced by its in-phase counterpart, while the $\pm 90^\circ$ phase shift is applied by the phase shifter. Finally, achieving in-phase splitting/combining spatially, as shown in Fig. 8.3 (bottom), enables the proposed spatial double-quadrature TRX architecture. This architecture can support hybrid-beamforming where RF_{0° can be connected to half of the beamforming elements while RF_{90° is connected to the other half. Notably, spatial double-quadrature TRX requires no additional circuits, as RF_{90° can be generated by swapping the baseband connections, and $\pm 90^\circ$ can be applied as a constant phase shift in the second half of the beamforming elements. Therefore, utilizing existing circuits with slight reconfiguration, the second I/Q mismatch rejection of spatial double-quadrature TRX comes with no power and area overhead.

- In Chapter 5, a load-modulation-based IMD3 cancellation technique is introduced, leading to a notable 5.7dB improvement in EVM. However, the limitations of the analog adaptive biasing circuit prevented us from fully exploiting the technique's benefits. Conversely, digital and mixed-signal TXs/PAs provide complete control over the auxiliary path's current, making them an ideal architecture for implementing this technique.

- Chapter 7 delves into the potential of phased-array mm-wave FDD systems, highlighting their promise through the notably reduced gap between TX blocker level and RX sensitivity level compared to conventional FDD systems. Nevertheless, due to its double-balanced mixer-first RX structure, the suggested fully integrated FDD frontend grapples with a high noise figure. By incorporating the proposed adjusted characteristic impedance transmission line ring with a nonreciprocal delay as the nonreciprocal linear periodic time-variant circuit, broader band operation with enhanced TX and RX performance can be achieved. Moreover, integrating an LNA in the RX path can significantly enhance the RX noise figure.

BIBLIOGRAPHY

[1] Erik Ekudden. "1.4 5G Drives Exponential Increase in Processing Needs Across all Industries". In: *2023 IEEE International Solid-State Circuits Conference (ISSCC)*. 2023, pp. 33–35. DOI: 10.1109/ISSCC42615.2023.10067359.

[2] Lip-Bu Tan. "1.4 Fueling Semiconductor Innovation and Entrepreneurship in the Next Decade". In: *2024 IEEE International Solid-State Circuits Conference (ISSCC)*. Vol. 67. 2024, pp. 29–33. DOI: 10.1109/ISSCC49657.2024.10454565.

[3] A. M. Niknejad, S. Thyagarajan, E. Alon, Y. Wang, and C. Hull. "A circuit designer's guide to 5G mm-wave". In: *2015 IEEE Custom Integrated Circuits Conference (CICC)*. Sept. 2015, pp. 1–8. DOI: 10.1109/CICC.2015.7338410.

[4] T. Tuovinen, N. Tervo, and A. Pärssinen. "Analyzing 5G RF System Performance and Relation to Link Budget for Directive MIMO". In: *IEEE Transactions on Antennas and Propagation* 65.12 (Dec. 2017), pp. 6636–6645. ISSN: 1558-2221. DOI: 10.1109/TAP.2017.2756848.

[5] M. Shafi, A. F. Molisch, P. J. Smith, T. Haustein, P. Zhu, P. De Silva, F. Tufvesson, A. Benjebbour, and G. Wunder. "5G: A Tutorial Overview of Standards, Trials, Challenges, Deployment, and Practice". In: *IEEE Journal on Selected Areas in Communications* 35.6 (June 2017), pp. 1201–1221. ISSN: 1558-0008. DOI: 10.1109/JSAC.2017.2692307.

[6] N. Kouzayha, Z. Dawy, J. G. Andrews, and H. ElSawy. "Joint Downlink/Uplink RF Wake-Up Solution for IoT Over Cellular Networks". In: *IEEE Transactions on Wireless Communications* 17.3 (Mar. 2018), pp. 1574–1588. ISSN: 1536-1276. DOI: 10.1109/TWC.2017.2781696.

[7] S. A. Busari, K. M. S. Huq, S. Mumtaz, L. Dai, and J. Rodriguez. "Millimeter-Wave Massive MIMO Communication for Future Wireless Systems: A Survey". In: *IEEE Communications Surveys Tutorials* 20.2 (Secondquarter 2018), pp. 836–869. ISSN: 1553-877X. DOI: 10.1109/COMST.2017.2787460.

[8] Hua Wang, Peter M. Asbeck, and Christian Fager. "Millimeter-Wave Power Amplifier Integrated Circuits for High Dynamic Range Signals". In: *IEEE Journal of Microwaves* 1.1 (2021), pp. 299–316. DOI: 10.1109/JMW.2020.3035897.

[9] H. Hashemi. "Millimeter-wave power amplifiers transmitters". In: *2017 IEEE Custom Integrated Circuits Conference (CICC)*. Apr. 2017, pp. 1–8. DOI: 10.1109/CICC.2017.7993691.

[10] Qualcomm Technologies, Inc. *"Spectrum for 4G and 5G"*. Dec. 2017.

[11] B. Sadhu, Y. Tousi, J. Hallin, S. Sahl, S. K. Reynolds, Ö. Renström, K. Sjögren, O. Haapalahti, N. Mazor, B. Bokinge, G. Weibull, H. Bengtsson, A. Carlinger, E. Westesson, J. -E. Thillberg, L. Rexberg, M. Yeck, X. Gu, M. Ferriss, D. Liu, D. Friedman, and A. Valdes-Garcia. "A 28-GHz 32-Element TRX Phased-Array IC With Concurrent Dual-Polarized Operation and Orthogonal Phase and Gain Control for 5G Communications". In: *IEEE Journal of Solid-State Circuits* 52.12 (Dec. 2017), pp. 3373–3391. ISSN: 1558-173X. DOI: 10.1109/JSSC.2017.2766211.

[12] H. T. Nguyen, T. Chi, S. Li, and H. Wang. "A Linear High-Efficiency Millimeter-Wave CMOS Doherty Radiator Leveraging Multi-Feed On-Antenna Active Load Modulation". In: *IEEE Journal of Solid-State Circuits* 53.12 (Dec. 2018), pp. 3587–3598. ISSN: 1558-173X. DOI: 10.1109/JSSC.2018.2880186.

[13] Naga Sasikanth Mannem, Tzu-Yuan Huang, Elham Erfani, Sensen Li, David Munzer, Matthieu R. Bloch, and Hua Wang. "A 25–34-GHz Eight-Element MIMO Transmitter for Keyless High Throughput Directionally Secure Communication". In: *IEEE Journal of Solid-State Circuits* 57.5 (2022), pp. 1244–1256. DOI: 10.1109/JSSC.2021.3135481.

[14] A. Hajimiri, A. Komijani, A. Natarajan, R. Chunara, X. Guan, and H. Hashemi. "Phased array systems in silicon". In: *IEEE Communications Magazine* 42.8 (2004), pp. 122–130. DOI: 10.1109/MCOM.2004.1321403.

[15] A. Natarajan, A. Komijani, and A. Hajimiri. "A fully integrated 24-GHz phased-array transmitter in CMOS". In: *IEEE Journal of Solid-State Circuits* 40.12 (Dec. 2005), pp. 2502–2514. ISSN: 1558-173X. DOI: 10.1109/JSSC.2005.857420.

[16] Bodhisatwa Sadhu, Yahya Tousi, Joakim Hallin, Stefan Sahl, Scott Reynolds, Örjan Renström, Kristoffer Sjögren, Olov Haapalahti, Nadav Mazor, Bo Bokinge, Gustaf Weibull, Håkan Bengtsson, Anders Carlinger, Eric Westesson, Jan-Erik Thillberg, Leonard Rexberg, Mark Yeck, Xiaoxiong Gu, Daniel Friedman, and Alberto Valdes-Garcia. "7.2 A 28GHz 32-element phased-array transceiver IC with concurrent dual polarized beams and 1.4 degree beam-steering resolution for 5G communication". In: *2017 IEEE International Solid-State Circuits Conference (ISSCC)*. 2017, pp. 128–129. DOI: 10.1109/ISSCC.2017.7870294.

[17] Thomas Cameron. "RF Technology for the 5G Millimeter Wave Radio". In: *Analog Devices Inc.* (2016).

[18] Peter M. Asbeck, Narek Rostomyan, Mustafa Özen, Bagher Rabet, and Jefy A. Jayamon. "Power Amplifiers for mm-Wave 5G Applications: Technology Comparisons and CMOS-SOI Demonstration Circuits". In: *IEEE Transactions on Microwave Theory and Techniques* 67.7 (2019), pp. 3099–3109. DOI: 10.1109/TMTT.2019.2896047.

[19] F. M. Barradas, P. M. Tomé, J. M. Gomes, T. R. Cunha, P. M. Cabral, and J. C. Pedro. "Power, Linearity, and Efficiency Prediction for MIMO Arrays With Antenna Coupling". In: *IEEE Transactions on Microwave Theory and Techniques* 65.12 (Dec. 2017), pp. 5284–5297. ISSN: 1557-9670. DOI: 10.1109/TMTT.2017.2766067.

[20] S. K. Dhar, A. Abdelhafiz, M. Aziz, M. Helaoui, and F. M. Ghannouchi. "A Reflection-Aware Unified Modeling and Linearization Approach for Power Amplifier Under Mismatch and Mutual Coupling". In: *IEEE Transactions on Microwave Theory and Techniques* 66.9 (Sept. 2018), pp. 4147–4157. ISSN: 1557-9670. DOI: 10.1109/TMTT.2018.2859959.

[21] X. Chen, S. Zhang, and Q. Li. "A Review of Mutual Coupling in MIMO Systems". In: *IEEE Access* 6 (2018), pp. 24706–24719. ISSN: 2169-3536. DOI: 10.1109/ACCESS.2018.2830653.

[22] C. Fager, T. Eriksson, F. Barradas, K. Hausmair, T. Cunha, and J. C. Pedro. "Linearity and Efficiency in 5G Transmitters: New Techniques for Analyzing Efficiency, Linearity, and Linearization in a 5G Active Antenna Transmitter Context". In: *IEEE Microwave Magazine* 20.5 (May 2019), pp. 35–49. ISSN: 1557-9581. DOI: 10.1109/MMM.2019.2898020.

[23] X. Chen, M. Abdullah, Q. Li, J. Li, A. Zhang, and T. Svensson. "Characterizations of Mutual Coupling Effects on Switch-Based Phased Array Antennas for 5G Millimeter-Wave Mobile Communications". In: *IEEE Access* 7 (2019), pp. 31376–31384. ISSN: 2169-3536. DOI: 10.1109/ACCESS.2019.2902951.

[24] Steve Cripps. *RF Power Amplifiers for Wireless Communications, Second Edition*. 2006.

[25] Fei Wang and Hua Wang. "A Broadband Linear Ultra-Compact mm-Wave Power Amplifier With Distributed-Balun Output Network: Analysis and Design". In: *IEEE Journal of Solid-State Circuits* 56.8 (2021), pp. 2308–2323. DOI: 10.1109/JSSC.2021.3078485.

[26] Seyed Yahya Mortazavi and Kwang-Jin Koh. "Integrated Inverse Class-F Silicon Power Amplifiers for High Power Efficiency at Microwave and mm-Wave". In: *IEEE Journal of Solid-State Circuits* 51.10 (2016), pp. 2420–2434. DOI: 10.1109/JSSC.2016.2588470.

[27] Sheikh Nijam Ali, Pawan Agarwal, Shahriar Mirabbasi, and Deukhyoun Heo. "A 42–46.4% PAE continuous class-F power amplifier with Cgd neutralization at 26–34 GHz in 65 nm CMOS for 5G applications". In: *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. 2017, pp. 212–215. DOI: 10.1109/RFIC.2017.7969055.

[28] Tso-Wei Li and Hua Wang. "A Continuous-Mode 23.5-41GHz Hybrid Class-F/F-l Power Amplifier with 46% Peak PAE for 5G Massive MIMO Applications". In: *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. 2018, pp. 220–230. DOI: 10.1109/RFIC.2018.8429030.

[29] Tso-Wei Li, Ming-Yu Huang, and Hua Wang. "A continuous-mode harmonically tuned 19-to-29.5GHz ultra-linear PA supporting 18Gb/s at 18.4% modulation PAE and 43.5% peak PAE". In: *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*. 2018, pp. 410–412. DOI: 10.1109/ISSCC.2018.8310358.

[30] Tso-Wei Li, Min-Yu Huang, and Hua Wang. “Millimeter-Wave Continuous-Mode Power Amplifier for 5G MIMO Applications”. In: *IEEE Transactions on Microwave Theory and Techniques* 67.7 (2019), pp. 3088–3098. DOI: 10.1109/TMTT.2019.2906592.

[31] Edgar Felipe Garay, David Joseph Munzer, and Hua Wang. “26.3 A mm-Wave Power Amplifier for 5G Communication Using a Dual-Drive Topology Exhibiting a Maximum PAE of 50% and Maximum DE of 60% at 30GHz”. In: *2021 IEEE International Solid- State Circuits Conference (ISSCC)*. Vol. 64. 2021, pp. 258–260. DOI: 10.1109/ISSCC42613.2021.9365830.

[32] Muhammad Hassan, Lawrence E. Larson, Vincent W. Leung, and Peter M. Asbeck. “A Combined Series-Parallel Hybrid Envelope Amplifier for Envelope Tracking Mobile Terminal RF Power Amplifier Applications”. In: *IEEE Journal of Solid-State Circuits* 47.5 (2012), pp. 1185–1198. DOI: 10.1109/JSSC.2012.2184639.

[33] Jooseung Kim, Dongsu Kim, Yunsung Cho, Daehyun Kang, Byungjoon Park, Kyunghoon Moon, and Bumman Kim. “Analysis of Envelope-Tracking Power Amplifier Using Mathematical Modeling”. In: *IEEE Transactions on Microwave Theory and Techniques* 62.6 (2014), pp. 1352–1362. DOI: 10.1109/TMTT.2014.2321356.

[34] Ji-Seon Paek, Dongsu Kim, Jae-Yeol Han, Younghwan Choo, Jun-Suk Bang, Seungchan Park, Jongbeom Baek, Takahiro Nomiyama, Ik-Hwan Kim, and Jongwoo Lee. “Efficient RF-PA Two-Chip Supply Modulator Architecture for 4G LTE and 5G NR Dual-Connectivity RF Front End”. In: *IEEE Journal of Solid-State Circuits* 57.4 (2022), pp. 1075–1089. DOI: 10.1109/JSSC.2022.3144771.

[35] F.H. Raab, P. Asbeck, S. Cripps, P.B. Kenington, Z.B. Popovic, N. Pothecary, J.F. Sevic, and N.O. Sokal. “Power amplifiers and transmitters for RF and microwave”. In: *IEEE Transactions on Microwave Theory and Techniques* 50.3 (2002), pp. 814–826. DOI: 10.1109/22.989965.

[36] D. Zhao, S. Kulkarni, and P. Reynaert. “A 60-GHz Outphasing Transmitter in 40-nm CMOS”. In: *IEEE Journal of Solid-State Circuits* 47.12 (Dec. 2012), pp. 3172–3183. ISSN: 1558-173X. DOI: 10.1109/JSSC.2012.2216692.

[37] S. Li, T. Chi, J. Park, H. T. Nguyen, and H. Wang. “A 28-GHz Flip-Chip Packaged Chireix Transmitter With On-Antenna Outphasing Active Load Modulation”. In: *IEEE Journal of Solid-State Circuits* 54.5 (May 2019), pp. 1243–1253. ISSN: 1558-173X. DOI: 10.1109/JSSC.2019.2898112.

[38] Kang Ning, Yihao Fang, Navid Hosseinzadeh, and James F. Buckwalter. “A 30-GHz CMOS SOI Outphasing Power Amplifier With Current Mode Combining for High Backoff Efficiency and Constant Envelope Operation”. In: *IEEE Journal of Solid-State Circuits* 55.5 (2020), pp. 1411–1421. DOI: 10.1109/JSSC.2019.2949255.

[39] S. Li, M. Y. Huang, D. Jung, T. -Y. Huang, and H. Wang. “A MM-Wave Current-Mode Inverse Outphasing Transmitter Front-End: A Circuit Duality of Conventional Voltage-Mode Outphasing”. In: *IEEE Journal of Solid-State Circuits* (2020), pp. 1–1. ISSN: 1558-173X. DOI: 10.1109/JSSC.2020.3038882.

[40] Bagher Rabet and Peter M. Asbeck. “A 28 GHz Single-Input Linear Chireix (SILC) Power Amplifier in 130 nm SiGe Technology”. In: *IEEE Journal of Solid-State Circuits* 55.6 (2020), pp. 1482–1490. DOI: 10.1109/JSSC.2020.2967542.

[41] Daniel J. Shepphard, Jeffrey Powell, and Steve C. Cripps. “An Efficient Broadband Reconfigurable Power Amplifier Using Active Load Modulation”. In: *IEEE Microwave and Wireless Components Letters* 26.6 (2016), pp. 443–445. DOI: 10.1109/LMWC.2016.2559503.

[42] Chandrakanth R Chappidi, Tushar Sharma, Zheng Liu, and Kaushik Sengupta. “Load Modulated Balanced mm-Wave CMOS PA with Integrated Linearity Enhancement for 5G applications”. In: *2020 IEEE/MTT-S International Microwave Symposium (IMS)*. 2020, pp. 1101–1104. DOI: 10.1109/IMS30576.2020.9224038.

[43] Valdrin Qunaj and Patrick Reynaert. “A Ka-Band Doherty-Like LMBA for High-Speed Wireless Communication in 28-nm CMOS”. In: *IEEE Journal of Solid-State Circuits* 56.12 (2021), pp. 3694–3703. DOI: 10.1109/JSSC.2021.3110168.

[44] Roberto Quaglia, Jingzhou Pang, Steve C. Cripps, and Anding Zhu. “Load-Modulated Balanced Amplifier: From First Invention to Recent Development”. In: *IEEE Microwave Magazine* 23.12 (2022), pp. 60–70. DOI: 10.1109/MMM.2022.3203940.

[45] Jiaxing Sun, Feng Lin, Houjun Sun, Wenhua Chen, and Renato Negra. “Broadband Three-Stage Pseudoload Modulated Balanced Amplifier With Power Back-Off Efficiency Enhancement”. In: *IEEE Transactions on Microwave Theory and Techniques* 70.5 (2022), pp. 2710–2722. DOI: 10.1109/TMTT.2022.3162867.

[46] Amir Agah, Hayg-Taniel Dabag, Bassel Hanafi, Peter M. Asbeck, James F. Buckwalter, and Lawrence E. Larson. “Active Millimeter-Wave Phase-Shift Doherty Power Amplifier in 45-nm SOI CMOS”. In: *IEEE Journal of Solid-State Circuits* 48.10 (2013), pp. 2338–2350. DOI: 10.1109/JSSC.2013.2269854.

[47] N. Rostomyan, M. Özen, and P. Asbeck. “28 GHz Doherty Power Amplifier in CMOS SOI With 28% Back-Off PAE”. In: *IEEE Microwave and Wireless Components Letters* 28.5 (May 2018), pp. 446–448. ISSN: 1558-1764. DOI: 10.1109/LMWC.2018.2813882.

[48] C. R. Chappidi, X. Wu, and K. Sengupta. “Simultaneously Broadband and Back-Off Efficient mm-Wave PAs: A Multi-Port Network Synthesis Approach”. In: *IEEE Journal of Solid-State Circuits* 53.9 (Sept. 2018), pp. 2543–2559. ISSN: 1558-173X. DOI: 10.1109/JSSC.2018.2841977.

[49] E. Kaymaksut, D. Zhao, and P. Reynaert. “Transformer-Based Doherty Power Amplifiers for mm-Wave Applications in 40-nm CMOS”. In: *IEEE Transactions on Microwave Theory and Techniques* 63.4 (Apr. 2015), pp. 1186–1192. ISSN: 1557-9670. DOI: 10.1109/TMTT.2015.2409255.

[50] Yen-Chih Chen, Yu-Hsuan Lin, Jung-Lin Lin, and Huei Wang. “A Ka-Band Transformer-Based Doherty Power Amplifier for Multi-Gb/s Application in 90-nm CMOS”. In: *IEEE Microwave and Wireless Components Letters* 28.12 (2018), pp. 1134–1136. DOI: 10.1109/LMWC.2018.2878133.

[51] F. Wang, T. Li, S. Hu, and H. Wang. “A Super-Resolution Mixed-Signal Doherty Power Amplifier for Simultaneous Linearity and Efficiency Enhancement”. In: *IEEE Journal of Solid-State Circuits* 54.12 (Dec. 2019), pp. 3421–3436. ISSN: 1558-173X. DOI: 10.1109/JSSC.2019.2937435.

[52] S. Hu, F. Wang, and H. Wang. “A 28-/37-/39-GHz Linear Doherty Power Amplifier in Silicon for 5G Applications”. In: *IEEE Journal of Solid-State Circuits* 54.6 (June 2019), pp. 1586–1599. ISSN: 1558-173X. DOI: 10.1109/JSSC.2019.2902307.

[53] Z. Zong, X. Tang, K. Khalaf, D. Yan, G. Mangraviti, J. Nguyen, Y. Liu, and P. Wambacq. “A 28-GHz SOI-CMOS Doherty Power Amplifier With a Compact Transformer-Based Output Combiner”. In: *IEEE Transactions on Microwave Theory and Techniques* (2021), pp. 1–1. ISSN: 1557-9670. DOI: 10.1109/TMTT.2021.3064022.

[54] Seokhyeon Kim, Hyun-Chul Park, Daehyun Kang, Donggyu Minn, and Sung-Gi Yang. “A 24.5–29.5GHz Broadband Parallel-to-Series Combined Compact Doherty Power Amplifier in 28-nm Bulk CMOS for 5G Applications”. In: *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. 2021, pp. 171–174. DOI: 10.1109/RFIC51843.2021.9490410.

[55] H. T. Nguyen and H. Wang. “A Coupler-Based Differential mm-Wave Doherty Power Amplifier With Impedance Inverting and Scaling Baluns”. In: *IEEE Journal of Solid-State Circuits* 55.5 (May 2020), pp. 1212–1223. ISSN: 1558-173X. DOI: 10.1109/JSSC.2020.2970708.

[56] T. -Y. Huang, N. S. Mannem, S. Li, D. Jung, M. -Y. Huang, and H. Wang. “26.1 A 26-to-60GHz Continuous Coupler-Doherty Linear Power Amplifier for Over-An-Octave Back-Off Efficiency Enhancement”. In: *2021 IEEE International Solid-State Circuits Conference (ISSCC)*. Vol. 64. Feb. 2021, pp. 354–356. DOI: 10.1109/ISSCC42613.2021.9365858.

[57] M. Pashaeifar, L. C. N. de Vreede, and M. S. Alavi. “14.4 A 24-to-30GHz Double-Quadrature Direct-Upconversion Transmitter with Mutual-Coupling-Resilient Series-Doherty Balanced PA for 5G MIMO Arrays”. In: *2021 IEEE International Solid- State Circuits Conference (ISSCC)*. Vol. 64. Feb. 2021, pp. 223–225. DOI: 10.1109/ISSCC42613.2021.9365776.

[58] Shohei Imai, Kenji Mukai, Satoshi Tanaka, and Hiroshi Okabe. “Bandwidth Optimization of Doherty Power Amplifier Based on Source Converters for 5G Mobile Handsets”. In: *IEEE Transactions on Microwave Theory and Techniques* 70.1 (2022), pp. 813–826. DOI: 10.1109/TMTT.2021.3124302.

[59] Masoud Pashaeifar, Anil K. Kumaran, Mohammadreza Beikmirza, Leo C.N. de Vreede, and Morteza S. Alavi. “A 24-to-32GHz series-Doherty PA with two-step impedance inverting power combiner achieving 20.4dBm Psat and 38%/34% PAE at Psat/6dB PBO for 5G applications”. In: *2021 IEEE Asian Solid-State Circuits Conference (A-SSCC)*. 2021, pp. 1–3. DOI: 10.1109/A-SSCC53895.2021.9634772.

[60] Fei Wang and Hua Wang. “A High-Power Broadband Multi-Primary DAT-Based Doherty Power Amplifier for mm-Wave 5G Applications”. In: *IEEE Journal of Solid-State Circuits* 56.6 (2021), pp. 1668–1681. DOI: 10.1109/JSSC.2021.3070800.

[61] Mohsen Mortazavi, Yiyu Shen, Dieuwert Mul, Leo C. N. de Vreede, Marco Spirito, and Masoud Babaie. “A Four-Way Series Doherty Digital Polar Transmitter at mm-Wave Frequencies”. In: *IEEE Journal of Solid-State Circuits* (2022), pp. 1–1. DOI: 10.1109/JSSC.2021.3133861.

[62] Xingcun Li, Wenhua Chen, Shuyang Li, Huibo Wu, Xiang Yi, Ruonan Han, and Zhenghe Feng. “A 110-to-130GHz SiGe BiCMOS Doherty Power Amplifier With Slotline-Based Power-Combining Technique Achieving >22dBm Saturated Output Power and >10% Power Back-off Efficiency”. In: *2022 IEEE International Solid- State Circuits Conference (ISSCC)*. Vol. 65. 2022, pp. 316–318. DOI: 10.1109/ISSCC42614.2022.9731552.

[63] Zonglin Ma, Kaixue Ma, Keping Wang, and Fanyi Meng. “A 28GHz Compact 3-Way Transformer-Based Parallel-Series Doherty Power Amplifier With 20.4%/14.2% PAE at 6-/12-dB Power Back-off and 25.5dBm PSAT in 55nm Bulk CMOS”. In: *2022 IEEE International Solid- State Circuits Conference (ISSCC)*. Vol. 65. 2022, pp. 320–322. DOI: 10.1109/ISSCC42614.2022.9731564.

[64] Tolga Dinc, Aravind Nagulu, and Harish Krishnaswamy. “A Millimeter-Wave Non-Magnetic Passive SOI CMOS Circulator Based on Spatio-Temporal Conductivity Modulation”. In: *IEEE Journal of Solid-State Circuits* 52.12 (2017), pp. 3276–3292. DOI: 10.1109/JSSC.2017.2759422.

[65] Aravind Nagulu and Harish Krishnaswamy. “28.5 Non-Magnetic 60GHz SOI CMOS Circulator Based on Loss/Dispersion-Engineered Switched Bandpass Filters”. In: *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*. 2019, 446–448. DOI: 10.1109/ISSCC.2019.8662467.

[66] Robin Garg, Sanket Jain, Paul Dania, and Arun Natarajan. “14.3 A 26GHz Full-Duplex Circulator Receiver with 53dB/400MHz(40dB/800MHz) Self-Interference Cancellation for mm-Wave Repeaters”. In: *2021 IEEE International Solid- State Circuits Conference (ISSCC)*. Vol. 64. 2021, 222–224. DOI: 10.1109/ISSCC42613.2021.9365979.

[67] F. Torres, M. De Matos, A. Cathelin, and E. Kerhervé. “A 31 GHz 2-Stage Reconfigurable Balanced Power Amplifier with 32.6dB Power Gain, 25.5% PAEmax and 17.9dBm Psat in 28nm FD-SOI CMOS”. In: *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. June 2018, pp. 236–239. DOI: 10.1109/RFIC.2018.8429009.

[68] S. Shahramian, M. J. Holyoak, A. Singh, and Y. Baeyens. “A Fully Integrated 384-Element, 16-Tile, *W* -Band Phased Array With Self-Alignment and Self-Test”. In: *IEEE Journal of Solid-State Circuits* 54.9 (Sept. 2019), pp. 2419–2434. ISSN: 1558-173X. DOI: 10.1109/JSSC.2019.2928694.

[69] Masoud Pashaeifar, Leo C. N. de Vreede, and Morteza S. Alavi. “A Millimeter-Wave CMOS Series-Doherty Power Amplifier With Post-Silicon Inter-Stage Passive Validation”. In: *IEEE Journal of Solid-State Circuits* 57.10 (2022), pp. 2999–3013. DOI: 10.1109/JSSC.2022.3175685.

[70] E. G. Larsson, O. Edfors, F. Tufvesson, and T. L. Marzetta. “Massive MIMO for next generation wireless systems”. In: *IEEE Communications Magazine* 52.2 (Feb. 2014), pp. 186–195. ISSN: 1558-1896. DOI: 10.1109/MCOM.2014.6736761.

[71] I. Ahmed, H. Khammari, A. Shahid, A. Musa, K. S. Kim, E. De Poorter, and I. Moerman. “A Survey on Hybrid Beamforming Techniques in 5G: Architecture and System Model Perspectives”. In: *IEEE Communications Surveys Tutorials* 20.4 (Fourthquarter 2018), pp. 3060–3097. ISSN: 1553-877X. DOI: 10.1109/COMST.2018.2843719.

[72] Hayg-Taniel Dabag, Bassel Hanafi, Fatih Golcuk, Amir Agah, James F. Buckwalter, and Peter M. Asbeck. “Analysis and Design of Stacked-FET Millimeter-Wave Power Amplifiers”. In: *IEEE Transactions on Microwave Theory and Techniques* 61.4 (2013), pp. 1543–1556. DOI: 10.1109/TMTT.2013.2247698.

[73] D. Zhao and P. Reynaert. “A 40-nm CMOS E-Band 4-Way Power Amplifier With Neutralized Bootstrapped Cascode Amplifier and Optimum Passive Circuits”. In: *IEEE Transactions on Microwave Theory and Techniques* 63.12 (Dec. 2015), pp. 4083–4089. ISSN: 1557-9670. DOI: 10.1109/TMTT.2015.2496341.

[74] S. Shakib, M. Elkholy, J. Dunworth, V. Aparin, and K. Entesari. “2.7 A wideband 28GHz power amplifier supporting 8×100MHz carrier aggregation for 5G in 40nm CMOS”. In: *2017 IEEE International Solid-State Circuits Conference (ISSCC)*. Feb. 2017, pp. 44–45. DOI: 10.1109/ISSCC.2017.7870252.

[75] W. Huang, J. Lin, Y. Lin, and H. Wang. “A K-Band Power Amplifier with 26-dBm Output Power and 34% PAE with Novel Inductance-based Neutralization in 90-nm CMOS”. In: *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. June 2018, pp. 228–231. DOI: 10.1109/RFIC.2018.8428973.

[76] C. Wu, Y. Lin, Y. Hsiao, C. Chou, Y. Wu, and H. Wang. “Design of a 60-GHz High-Output Power Stacked- FET Power Amplifier Using Transformer-Based Voltage-Type Power Combining in 65-nm CMOS”. In: *IEEE Transactions on Microwave Theory and Techniques* 66.10 (Oct. 2018), pp. 4595–4607. ISSN: 1557-9670. DOI: 10.1109/TMTT.2018.2859980.

[77] D. Manente, F. Padovan, D. Seebacher, M. Bassi, and A. Bevilacqua. “A 28-GHz Stacked Power Amplifier with 20.7-dBm Output P1dB in 28-nm Bulk CMOS”. In: *IEEE Solid-State Circuits Letters* 3 (2020), pp. 170–173. ISSN: 2573-9603. DOI: 10.1109/LSSC.2020.3009973.

[78] Dixian Zhao and Patrick Reynaert. “A 60-GHz Dual-Mode Class AB Power Amplifier in 40-nm CMOS”. In: *IEEE Journal of Solid-State Circuits* 48.10 (2013), pp. 2323–2337. DOI: 10.1109/JSSC.2013.2275662.

[79] W.H. Doherty. “A New High Efficiency Power Amplifier for Modulated Waves”. In: *Proceedings of the Institute of Radio Engineers* 24.9 (1936), pp. 1163–1182. DOI: 10.1109/JRPROC.1936.228468.

[80] Luca Piazzon, Rocco Giofrè, Roberto Quaglia, Vittorio Camarchia, Marco Pirola, Paolo Colantonio, Franco Giannini, and Giovanni Ghione. "Effect of Load Modulation on Phase Distortion in Doherty Power Amplifiers". In: *IEEE Microwave and Wireless Components Letters* 24.7 (2014), pp. 505–507. DOI: 10.1109/LMWC.2014.2316507.

[81] Xiaohu Fang, Arthur Chung, and Slim Boumaiza. "Linearity-Enhanced Doherty Power Amplifier Using Output Combining Network With Predefined AM–PM Characteristics". In: *IEEE Transactions on Microwave Theory and Techniques* 67.1 (2019), pp. 195–204. DOI: 10.1109/TMTT.2018.2870830.

[82] J.R. Long. "Monolithic transformers for silicon RF IC design". In: *IEEE Journal of Solid-State Circuits* 35.9 (2000), pp. 1368–1382. DOI: 10.1109/4.868049.

[83] I. Aoki, S.D. Kee, D.B. Rutledge, and A. Hajimiri. "Distributed active transformer-a new power-combining and impedance-transformation technique". In: *IEEE Transactions on Microwave Theory and Techniques* 50.1 (2002), pp. 316–331. DOI: 10.1109/22.981284.

[84] Siva V. Thyagarajan, Ali M. Niknejad, and Christopher D. Hull. "A 60 GHz Drain-Source Neutralized Wideband Linear Power Amplifier in 28 nm CMOS". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 61.8 (2014), pp. 2253–2262. DOI: 10.1109/TCSI.2014.2333682.

[85] M. Vigilante and P. Reynaert. "A Wideband Class-AB Power Amplifier With 29–57-GHz AM–PM Compensation in 0.9-V 28-nm Bulk CMOS". In: *IEEE Journal of Solid-State Circuits* 53.5 (May 2018), pp. 1288–1301. ISSN: 1558-173X. DOI: 10.1109/JSSC.2017.2778275.

[86] S. Kshattry, W. Choi, C. Yu, and K. O. Kenneth. "Compact Diode Connected MOSFET Detector for On-Chip Millimeter-Wave Voltage Measurements". In: *IEEE Microwave and Wireless Components Letters* 26.5 (May 2016), pp. 349–351. ISSN: 1558-1764. DOI: 10.1109/LMWC.2016.2548365.

[87] Marco Vigilante and Patrick Reynaert. "On the Design of Wideband Transformer-Based Fourth Order Matching Networks for *E* -Band Receivers in 28-nm CMOS". In: *IEEE Journal of Solid-State Circuits* 52.8 (2017), pp. 2071–2082. DOI: 10.1109/JSSC.2017.2690864.

[88] Masoud Pashaeifar, Leo C. N. de Vreede, and Morteza S. Alavi. "A Millimeter-Wave Mutual-Coupling-Resilient Double-Quadrature Transmitter for 5G Applications". In: *IEEE Journal of Solid-State Circuits* 56.12 (2021), pp. 3784–3798. DOI: 10.1109/JSSC.2021.3111126.

[89] S. Kshattry, C.-K. Yu, C.-L. Wu, Y. Yun, C. Lee, C.-Y. Cha, W.-Y. Choi, N. Preisler, and K. K. O. "High-Impedance, Broadband and Compact RMS Detectors for On-Chip Measurements of Millimeter Wave Voltages for Built-In Self-Testing and Debugging". In: *2020 IEEE 20th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*. 2020, pp. 22–25. DOI: 10.1109/SIRF46766.2020.9040184.

[90] A.M. Cowley and H.O. Sorensen. "Quantitative Comparison of Solid-State Microwave Detectors". In: *IEEE Transactions on Microwave Theory and Techniques* 14.12 (1966), pp. 588–602. DOI: 10.1109/TMTT.1966.1126337.

[91] Chikuang Yu, Chieh-Lin Wu, Sandeep Kshattry, Yang-Hun Yun, Choong-Yul Cha, Hisashi Shichijo, and Kenneth K. O. “Compact, High Impedance and Wide Bandwidth Detectors for Characterization of Millimeter Wave Performance”. In: *IEEE Journal of Solid-State Circuits* 47.10 (2012), pp. 2335–2343. DOI: 10.1109/JSSC.2012.2219155.

[92] B. Yang, Z. Yu, J. Lan, R. Zhang, J. Zhou, and W. Hong. “Digital Beamforming-Based Massive MIMO Transceiver for 5G Millimeter-Wave Communications”. In: *IEEE Transactions on Microwave Theory and Techniques* 66.7 (July 2018), pp. 3403–3418. ISSN: 1557-9670. DOI: 10.1109/TMTT.2018.2829702.

[93] A. K. Gupta and J. F. Buckwalter. “Linearity Considerations for Low-EVM, Millimeter-Wave Direct-Conversion Modulators”. In: *IEEE Transactions on Microwave Theory and Techniques* 60.10 (Oct. 2012), pp. 3272–3285. ISSN: 1557-9670. DOI: 10.1109/TMTT.2012.2209435.

[94] D. Zhao and P. Reynaert. “A 40 nm CMOS E-Band Transmitter With Compact and Symmetrical Layout Floor-Plans”. In: *IEEE Journal of Solid-State Circuits* 50.11 (Nov. 2015), pp. 2560–2571. ISSN: 1558-173X. DOI: 10.1109/JSSC.2015.2456918.

[95] P. Wu, A. K. Gupta, and J. F. Buckwalter. “A Dual-Band Millimeter-Wave Direct-Conversion Transmitter With Quadrature Error Correction”. In: *IEEE Transactions on Microwave Theory and Techniques* 62.12 (Dec. 2014), pp. 3118–3130. ISSN: 1557-9670. DOI: 10.1109/TMTT.2014.2362123.

[96] R. Wu, R. Minami, Y. Tsukui, S. Kawai, Y. Seo, S. Sato, K. Kimura, S. Kondo, T. Ueno, N. Fajri, S. Maki, N. Nagashima, Y. Takeuchi, T. Yamaguchi, A. Musa, K. K. Tokgoz, T. Siriburanon, B. Liu, Y. Wang, J. Pang, N. Li, M. Miyahara, K. Okada, and A. Matsuzawa. “64-QAM 60-GHz CMOS Transceivers for IEEE 802.11ad/ay”. In: *IEEE Journal of Solid-State Circuits* 52.11 (Nov. 2017), pp. 2871–2891. ISSN: 1558-173X. DOI: 10.1109/JSSC.2017.2740264.

[97] H. Kim, B. Park, S. Song, T. Moon, S. Kim, J. Kim, J. Chang, and Y. Ho. “A 28-GHz CMOS Direct Conversion Transceiver With Packaged 2 × 4 Antenna Array for 5G Cellular System”. In: *IEEE Journal of Solid-State Circuits* 53.5 (May 2018), pp. 1245–1259. ISSN: 1558-173X. DOI: 10.1109/JSSC.2018.2817606.

[98] F. Piri, M. Bassi, N. R. Lacaita, A. Mazzanti, and F. Svelto. “A PVT-Tolerant >40-dB IRR, 44% Fractional-Bandwidth Ultra-Wideband mm-Wave Quadrature LO Generator for 5G Networks in 55-nm CMOS”. In: *IEEE Journal of Solid-State Circuits* 53.12 (Dec. 2018), pp. 3576–3586. ISSN: 1558-173X. DOI: 10.1109/JSSC.2018.2878819.

[99] J. Pang, S. Maki, S. Kawai, N. Nagashima, Y. Seo, M. Dome, H. Kato, M. Katsuragi, K. Kimura, S. Kondo, Y. Terashima, H. Liu, T. Siriburanon, A. Tharayil Narayanan, N. Fajri, T. Kaneko, T. Yoshioka, B. Liu, Y. Wang, R. Wu, N. Li, K. K. Tokgoz, M. Miyahara, A. Shirane, and K. Okada. “A 50.1-Gb/s 60-GHz CMOS Transceiver for IEEE 802.11ay With Calibration of LO Feedthrough and I/Q Imbalance”. In: *IEEE Journal of Solid-State Circuits* 54.5 (May 2019), pp. 1375–1390. ISSN: 1558-173X. DOI: 10.1109/JSSC.2018.2886338.

[100] F. Piri, E. Rahimi, M. Bassi, F. Svelto, and A. Mazzanti. "70–90-GHz Self-Tuned Polyphase Filter for Wideband I/Q LO Generation in a 55-nm BiCMOS Transmitter". In: *IEEE Solid-State Circuits Letters* 2.9 (Sept. 2019), pp. 155–158. ISSN: 2573-9603. DOI: 10.1109/LSSC.2019.2930361.

[101] A. Rezola, J. F. Sevillano, D. del Río, B. Martín, I. Gurutzeaga, I. Vélez, and R. Berenguer. "Temperature-Dependent I/Q Imbalance Compensation in Ultra-Wideband Millimeter-Wave Multi-Gigabit Transmitters". In: *IEEE Transactions on Microwave Theory and Techniques* 68.1 (Jan. 2020), pp. 340–352. ISSN: 1557-9670. DOI: 10.1109/TMTT.2019.2943335.

[102] D. Zhao and P. Reynaert. "An E-Band Power Amplifier With Broadband Parallel-Series Power Combiner in 40-nm CMOS". In: *IEEE Transactions on Microwave Theory and Techniques* 63.2 (Feb. 2015), pp. 683–690. ISSN: 1557-9670. DOI: 10.1109/TMTT.2014.2379277.

[103] H. T. Nguyen, S. Li, and H. Wang. "4.6 A mm-Wave 3-Way Linear Doherty Radiator with Multi Antenna Coupling and On-Antenna Current-Scaling Series Combiner for Deep Power Back-Off Efficiency Enhancement". In: *2019 IEEE International Solid- State Circuits Conference - (ISSCC)*. Feb. 2019, pp. 84–86. DOI: 10.1109/ISSCC.2019.8662500.

[104] N. S. Mannem, M. -Y. Huang, T. -Y. Huang, and H. Wang. "A Reconfigurable Hybrid Series/Parallel Doherty Power Amplifier With Antenna VSWR Resilient Performance for MIMO Arrays". In: *IEEE Journal of Solid-State Circuits* 55.12 (Dec. 2020), pp. 3335–3348. ISSN: 1558-173X. DOI: 10.1109/JSSC.2020.3022617.

[105] F. Wang and H. Wang. "24.1 A 24-to-30GHz Watt-Level Broadband Linear Doherty Power Amplifier with Multi-Primary Distributed-Active-Transformer Power-Combining Supporting 5G NR FR2 64-QAM with >19dBm Average Pout and >19% Average PAE". In: *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*. Feb. 2020, pp. 362–364. DOI: 10.1109/ISSCC19947.2020.9063146.

[106] S. M. Bowers, K. Sengupta, K. Dasgupta, B. D. Parker, and A. Hajimiri. "Integrated Self-Healing for mm-Wave Power Amplifiers". In: *IEEE Transactions on Microwave Theory and Techniques* 61.3 (Mar. 2013), pp. 1301–1315. ISSN: 1557-9670. DOI: 10.1109/TMTT.2013.2243750.

[107] C. R. Chappidi, T. Sharma, and K. Sengupta. "Multi-port Active Load Pulling for mm-Wave 5G Power Amplifiers: Bandwidth, Back-Off Efficiency, and VSWR Tolerance". In: *IEEE Transactions on Microwave Theory and Techniques* 68.7 (July 2020), pp. 2998–3016. ISSN: 1557-9670. DOI: 10.1109/TMTT.2020.2977342.

[108] S. Kulkarni, D. Zhao, and P. Reynaert. "Design of an Optimal Layout Polyphase Filter for Millimeter-Wave Quadrature LO Generation". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 60.4 (Apr. 2013), pp. 202–206. ISSN: 1558-3791. DOI: 10.1109/TCSII.2013.2251946.

[109] J. S. Park and H. Wang. "A Transformer-Based Poly-Phase Network for Ultra-Broadband Quadrature Signal Generation". In: *IEEE Transactions on Microwave Theory and Techniques* 63.12 (Dec. 2015), pp. 4444–4457. ISSN: 1557-9670. DOI: 10.1109/TMTT.2015.2496187.

[110] M. Huang, T. Chi, S. Li, T. Huang, and H. Wang. “A 24.5–43.5-GHz Ultra-Compact CMOS Receiver Front End With Calibration-Free Instantaneous Full-Band Image Rejection for Multiband 5G Massive MIMO”. In: *IEEE Journal of Solid-State Circuits* 55.5 (May 2020), pp. 1177–1186. ISSN: 1558-173X. DOI: 10.1109/JSSC.2019.2959495.

[111] J. Crols and M. S. J. Steyaert. “A single-chip 900 MHz CMOS receiver front-end with a high performance low-IF topology”. In: *IEEE Journal of Solid-State Circuits* 30.12 (Dec. 1995), pp. 1483–1492. ISSN: 1558-173X. DOI: 10.1109/4.482196.

[112] J. C. Rudell, J. -. Ou, T. B. Cho, G. Chien, F. Brianti, J. A. Weldon, and P. R. Gray. “A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications”. In: *IEEE Journal of Solid-State Circuits* 32.12 (Dec. 1997), pp. 2071–2088. ISSN: 1558-173X. DOI: 10.1109/4.643665.

[113] B. Razavi. *RF Microelectronics*. Communications Engineering & Emerging Technology Series from Ted Rappaport. Pearson Education, 2011. ISBN: 9780132901055. URL: https://books.google.nl/books?id=zTnD1RgHbbkC.

[114] H. Jeon, Y. Park, Y. Huang, J. Kim, K. Lee, C. Lee, and J. S. Kenney. “A Triple-Mode Balanced Linear CMOS Power Amplifier Using a Switched-Quadrature Coupler”. In: *IEEE Journal of Solid-State Circuits* 47.9 (2012), pp. 2019–2032. DOI: 10.1109/JSSC.2012.2193510.

[115] G. Nikandish, R. B. Staszewski, and A. Zhu. “Breaking the Bandwidth Limit: A Review of Broadband Doherty Power Amplifier Design for 5G”. In: *IEEE Microwave Magazine* 21.4 (Apr. 2020), pp. 57–75. ISSN: 1557-9581. DOI: 10.1109/MMM.2019.2963607.

[116] H. Gao, K. Ying, M. K. Matters-Kammerer, P. Harpe, Q. Ma, A. van Roermund, and P. Baltus. “A 48–61 GHz LNA in 40-nm CMOS with 3.6 dB minimum NF employing a metal slotting method”. In: *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. May 2016, pp. 154–157. DOI: 10.1109/RFIC.2016.7508274.

[117] G. Gonzalez. *Microwave Transistor Amplifiers: Analysis and Design*. Prentice Hall, 1997. ISBN: 9780132543354.

[118] Masoud Pashaeifar, Leo C. N. de Vreede, and Morteza S. Alavi. “Load-Modulation-Based IMD3 Cancellation for Millimeter-Wave Class-B CMOS Power Amplifiers Achieving EVM <1.2%”. In: *IEEE Microwave and Wireless Components Letters* 32.6 (2022), pp. 716–719. DOI: 10.1109/LMWC.2022.3166257.

[119] C. Fager, J.C. Pedro, N.B. de Carvalho, H. Zirath, F. Fortes, and M.J. Rosario. “A comprehensive analysis of IMD behavior in RF CMOS power amplifiers”. In: *IEEE Journal of Solid-State Circuits* 39.1 (2004), pp. 24–34. DOI: 10.1109/JSSC.2003.820860.

[120] Byungjoon Park, Daechul Jeong, Jooseung Kim, Yunsung Cho, Kyunghoon Moon, and Bumman Kim. “Highly linear CMOS power amplifier for mm-wave applications”. In: *2016 IEEE MTT-S International Microwave Symposium (IMS)*. 2016, pp. 1–3. DOI: 10.1109/MWSYM.2016.7540024.

[121] H.-C. Park, D. Kang, S. M. Lee, B. Park, K. Kim, J. Lee, Y. Aoki, Y. Yoon, S. Lee, D. Lee, D. Kwon, S. Kim, J. Kim, W. Lee, C. Kim, S. Park, J. Park, B. Suh, J. Jang, M. Kim, D. Minn, I. Park, S. Kim, K. Min, J. Park, S. Jeon, A.-S. Ryu, Y. Cho, S. T. Choi, K. H. An, Y. Kim, J. H. Lee, J. Son, and S.-G. Yang. "4.1 A 39GHz-Band CMOS 16-Channel Phased-Array Transceiver IC with a Companion Dual-Stream IF Transceiver IC for 5G NR Base-Station Applications". In: *2020 IEEE International Solid- State Circuits Conference - (ISSCC)*. 2020, pp. 76–78. DOI: 10.1109/ISSCC19947.2020.9063006.

[122] Marco Vigilante and Patrick Reynaert. "A 29-to-57GHz AM-PM compensated class-AB power amplifier for 5G phased arrays in 0.9V 28nm bulk CMOS". In: *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. 2017, pp. 116–119. DOI: 10.1109/RFIC.2017.7969031.

[123] Masoud Pashaeifar, Leo C. N. de Vreede, and Morteza S. Alavi. "14.4 A 24-to-30GHz Double-Quadrature Direct-Upconversion Transmitter with Mutual-Coupling-Resilient Series-Doherty Balanced PA for 5G MIMO Arrays". In: *2021 IEEE International Solid- State Circuits Conference (ISSCC)*. Vol. 64. 2021, pp. 223–225. DOI: 10.1109/ISSCC42613.2021.9365776.

[124] Tso-Wei Li, Sensen Li, Hossein Miri Lavasani, and Hua Wang. "A V-Band Doubly Hybrid NMOS/PMOS Four-Way Distributed-Active-Transformer Power Amplifier for Nonlinearity Cancellation and Joint Linearity/Efficiency Optimization". In: *2021 IEEE MTT-S International Microwave Symposium (IMS)*. 2021, pp. 382–385. DOI: 10.1109/IMS19712.2021.9575016.

[125] Shailesh Kulkarni and Patrick Reynaert. "A 60-GHz Power Amplifier With AM–PM Distortion Cancellation in 40-nm CMOS". In: *IEEE Transactions on Microwave Theory and Techniques* 64.7 (2016), pp. 2284–2291. DOI: 10.1109/TMTT.2016.2574866.

[126] Mohammed Abdulaziz, Halil Volkan Hünerli, Koen Buisman, and Christian Fager. "Improvement of AM–PM in a 33-GHz CMOS SOI Power Amplifier Using pMOS Neutralization". In: *IEEE Microwave and Wireless Components Letters* 29.12 (2019), pp. 798–801. DOI: 10.1109/LMWC.2019.2948763.

[127] Sheikh Nijam Ali, Pawan Agarwal, Joe Baylon, Srinivasan Gopal, Luke Renaud, and Deukhyoun Heo. "A 28GHz 41%-PAE linear CMOS power amplifier using a transformer-based AM-PM distortion-correction technique for 5G phased arrays". In: *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*. 2018, pp. 406–408. DOI: 10.1109/ISSCC.2018.8310356.

[128] Han-Woong Choi, Sunkyu Choi, and Choul-Young Kim. "A 25-GHz Power Amplifier Using Three-Stage Antiphase Linearization in Bulk 65-nm CMOS Technology". In: *IEEE Microwave and Wireless Components Letters* 30.5 (2020), pp. 489–491. DOI: 10.1109/LMWC.2020.2984949.

[129] Sangsu Jin, Byungjoon Park, Kyunghoon Moon, Myeongju Kwon, and Bumman Kim. "Linearization of CMOS Cascode Power Amplifiers Through Adaptive Bias Control". In: *IEEE Transactions on Microwave Theory and Techniques* 61.12 (2013), pp. 4534–4543. DOI: 10.1109/TMTT.2013.2288206.

[130] Gwangsik Cho, Jinseok Park, and Songcheol Hong. “A 25.5-dB Peak Gain F -Band Power Amplifier With an Adaptive Built-In Linearizer”. In: *IEEE Microwave and Wireless Components Letters* 30.1 (2020), pp. 106–108. DOI: 10.1109/LMWC.2019.2954217.

[131] Wonho Lee, Jongho Yoo, and Songcheol Hong. “A 28-GHz CMOS Power Amplifier Linearized by Dynamic Conductance Control and Body Carrier Injection”. In: *IEEE Microwave and Wireless Components Letters* 31.9 (2021), pp. 1071–1074. DOI: 10.1109/LMWC.2021.3083284.

[132] Taehwan Joo, Bonhoon Koo, and Songcheol Hong. “A WLAN RF CMOS PA With Large-Signal MGTR Method”. In: *IEEE Transactions on Microwave Theory and Techniques* 61.3 (2013), pp. 1272–1279. DOI: 10.1109/TMTT.2013.2244228.

[133] Jonghoon Park, Changhyun Lee, Jinho Yoo, and Changkun Park. “A CMOS Antiphase Power Amplifier With an MGTR Technique for Mobile Applications”. In: *IEEE Transactions on Microwave Theory and Techniques* 65.11 (2017), pp. 4645–4656. DOI: 10.1109/TMTT.2017.2709304.

[134] Doohwan Jung, Huan Zhao, and Hua Wang. “A CMOS Highly Linear Doherty Power Amplifier With Multigated Transistors”. In: *IEEE Transactions on Microwave Theory and Techniques* 67.5 (2019), pp. 1883–1891. DOI: 10.1109/TMTT.2019.2899596.

[135] Hyunjin Ahn, Ilku Nam, and Ockgoo Lee. “A 28-GHz Highly Efficient CMOS Power Amplifier Using a Compact Symmetrical 8-Way Parallel-Parallel Power Combiner with IMD3 Cancellation Method”. In: *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. 2020, pp. 187–190. DOI: 10.1109/RFIC49505.2020.9218411.

[136] Jonghoon Park, Changhyun Lee, and Changkun Park. “A Quad-Band CMOS Linear Power Amplifier for EDGE Applications Using an Anti-Phase Method to Enhance its Linearity”. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 64.4 (2017), pp. 765–776. DOI: 10.1109/TCSI.2016.2620559.

[137] Masoud Pashaeifar, Leo C. N. de Vreede, and Morteza S. Alavi. “A Millimeter-Wave Mutual-Coupling-Resilient Double-Quadrature Transmitter for 5G Applications”. In: *IEEE Journal of Solid-State Circuits* 56.12 (2021), pp. 3784–3798. DOI: 10.1109/JSSC.2021.3111126.

[138] Masoud Pashaeifar, Anil Kumar Kumaran, Leo C. N. de Vreede, and Morteza S. Alavi. “A Chain-Weaver Balanced Power Amplifier With an Embedded Impedance/Power Sensor”. In: *IEEE Journal of Solid-State Circuits* (2024), pp. 1–14. DOI: 10.1109/JSSC.2024.3453213.

[139] Eric C. Wagner and Gabriel M. Rebeiz. “An 8-Way Combined E-Band Power Amplifier with 24 dBm Psat and 12% PAE in 0.12 μm SiGe”. In: *2018 IEEE/MTT-S International Microwave Symposium - IMS*. 2018, pp. 1342–1344. DOI: 10.1109/MWSYM.2018.8439443.

[140] Hyunjin Ahn, Ilku Nam, and Ockgoo Lee. “A 28-GHz Highly Efficient CMOS Power Amplifier Using a Compact Symmetrical 8-Way Parallel-Parallel Power Combiner with IMD3 Cancellation Method”. In: *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. 2020, pp. 187–190. DOI: 10.1109/RFIC49505.2020.9218411.

[141] Weisen Zeng, Li Gao, Ningzheng Sun, Hongtao Xu, Quan Xue, and Xiuyin Zhang. “25.2 A 19.7-to-43.8GHz Power Amplifier with Broadband Linearization Technique in 28nm Bulk CMOS”. In: *2023 IEEE International Solid-State Circuits Conference (ISSCC)*. 2023, pp. 372–374. DOI: 10.1109/ISSCC42615.2023.10067840.

[142] Masoud Pashaeifar, Leo C.N. De Vreede, and Morteza S. Alavi. “A Millimeter-Wave Front-End for FD/FDD Transceivers Featuring an Embedded PA and an N-Path Filter Based Circulator Receiver”. In: *2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. 2022, pp. 11–14. DOI: 10.1109/RFIC54546.2022.9863209.

[143] Parastoo Taghikhani, Koen Buisman, and Christian Fager. “Hybrid Beamforming Transmitter Modeling for Millimeter-Wave MIMO Applications”. In: *IEEE Transactions on Microwave Theory and Techniques* 68.11 (2020), pp. 4740–4752. DOI: 10.1109/TMTT.2020.2995657.

[144] Christian Fager, Thomas Eriksson, Filipe Barradas, Katharina Hausmair, Telmo Cunha, and Jose Carlos Pedro. “Linearity and Efficiency in 5G Transmitters: New Techniques for Analyzing Efficiency, Linearity, and Linearization in a 5G Active Antenna Transmitter Context”. In: *IEEE Microwave Magazine* 20.5 (2019), pp. 35–49. DOI: 10.1109/MMM.2019.2898020.

[145] Yang Zhang, Giovanni Mangraviti, Johan Nguyen, Zhiwei Zong, and Piet Wambacq. “26.4 A Reflection-Coefficient Sensor for 28GHz Beamforming Transmitters in 22nm FD-SOI CMOS”. In: *2021 IEEE International Solid-State Circuits Conference (ISSCC)*. Vol. 64. 2021, pp. 360–362. DOI: 10.1109/ISSCC42613.2021.9366018.

[146] David Munzer, Naga Sasikanth Mannem, Edgar Felipe Garay, and Hua Wang. “Single-Ended Quadrature Coupler-Based VSWR Resilient Joint mm-Wave True Power Detector and Impedance Sensor”. In: *IEEE Transactions on Microwave Theory and Techniques* 70.5 (2022), pp. 2802–2814. DOI: 10.1109/TMTT.2022.3149538.

[147] David Munzer, Naga Sasikanth Mannem, Jeongseok Lee, and Hua Wang. “Broadband mm-Wave Current/Voltage Sensing-Based VSWR-Resilient True Power/Impedance Sensor Supporting Single-Ended Antenna Interfaces”. In: *IEEE Journal of Solid-State Circuits* 58.6 (2023), pp. 1535–1551. DOI: 10.1109/JSSC.2022.3211935.

[148] Edward Liu, David Munzer, Jeongseok Lee, and Hua Wang. “32.10 A Compact Broadband VSWR-Resilient True-Power-and-Gain Sensor with Dynamic-Range Compensation for Phased-Array Applications”. In: *2024 IEEE International Solid-State Circuits Conference (ISSCC)*. Vol. 67. 2024, pp. 538–540. DOI: 10.1109/ISSCC49657.2024.10454458.

[149] M. Pashaeifar, A. K. Kumaran, L. C. N. de Vreede, and M. S. Alavi. “32.7 A 25.2dBm P_{SAT}, 35-to-43GHz VSWR-Resilient Chain-Weaver Eight-Way Balanced PA with an Embedded Impedance/Power Sensor”. In: *2024 IEEE International Solid- State Circuits Conference (ISSCC)*, pp. 1–3.

[150] H.-C. Park, D. Kang, S. M. Lee, B. Park, K. Kim, J. Lee, Y. Aoki, Y. Yoon, S. Lee, D. Lee, D. Kwon, S. Kim, J. Kim, W. Lee, C. Kim, S. Park, J. Park, B. Suh, J. Jang, M. Kim, D. Minn, I. Park, S. Kim, K. Min, J. Park, S. Jeon, A.-S. Ryu, Y. Cho, S. T. Choi, K. H. An, Y. Kim, J. H. Lee, J. Son, and S.-G. Yang. “A 39GHz-Band CMOS 16-Channel Phased-Array Transceiver IC with a Companion Dual-Stream IF Transceiver IC for 5G NR Base-Station Applications”. In: *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*, pp. 76–78. DOI: 10.1109/ISSCC19947.2020.9063006.

[151] Ashutosh Verma, Venu Bhagavatula, Amitoj Singh, Wanghua Wu, Hariharan Nagarajan, Pak-Kim Lau, Xiaohua Yu, Omar Elsayed, Ajaypat Jain, Anirban Sarkar, Fan Zhang, Che-Chun Kuo, Patrick McElwee, Pei-Yuan Chiang, Chengkai Guo, Zhanjun Bai, Tienyu Chang, Abishek Mann, Andreas Rydin, Xingliang Zhao, Jeiyoung Lee, Daeyoung Yoon, Chih-Wei Yao, Siuchuang Ivan Lu, Sang Won Son, and Thomas B. Cho. “A 16-Channel, 28/39GHz Dual-Polarized 5G FR2 Phased-Array Transceiver IC with a Quad-Stream IF Transceiver Supporting Non-Contiguous Carrier Aggregation up to 1.6GHz BW”. In: *2022 IEEE International Solid-State Circuits Conference (ISSCC)*. Vol. 65. 2022, pp. 1–3. DOI: 10.1109/ISSCC42614.2022.9731664.

[152] Hong-Teuk Kim, Byoung-Sun Park, Seong-Sik Song, Tak-Su Moon, So-Hyeong Kim, Jong-Moon Kim, Ji-Young Chang, and Yo-Chul Ho. “A 28-GHz CMOS Direct Conversion Transceiver With Packaged 2 × 4 Antenna Array for 5G Cellular System”. In: *IEEE Journal of Solid-State Circuits* 53.5 (2018), pp. 1245–1259. DOI: 10.1109/JSSC.2018.2817606.

[153] Hansik Oh, Seungwon Park, Jooseok Lee, Seungjae Baek, Joonho Jung, Taewan Kim, Jinhyun Kim, Woojae Lee, Jae-Hong Park, Kihyun Kim, Dong-Hyun Lee, Sangho Lee, Jeong Ho Lee, Ji Hoon Kim, Younghwan Kim, Sangyong Park, Bohee Suh, Soyoung Oh, Dongsoo Lee, Sehyug Jeon, Juho Son, and Sung-Gi Yang. “32.2 A 24.25-to-29.5GHz Extremely Compact Doherty Power Amplifier with Differential-Breaking Phase Offset Achieving 23.7% PAEavg for 5G Base-Station Transceivers”. In: *2024 IEEE International Solid-State Circuits Conference (ISSCC)*. Vol. 67. 2024, pp. 522–524. DOI: 10.1109/ISSCC49657.2024.10454406.

[154] Wei Zhu, Jiazhi Ying, Long Chen, Jian Zhang, Guanshen Lv, Xiangjie Yi, Zhiqiang Zhao, Zunxiang Wang, Yan Wang, Wenhua Chen, and Houjun Sun. “32.8 A 27.8-to-38.7GHz Load-Modulated Balanced Power Amplifier with Scalable 7-to-1 Load-Modulated Power-Combine Network Achieving 27.2dBm Output Power and 28.8%/23.2%/16.3%/11.9% Peak/6/9/12dB Back-Off Efficiency”. In: *2024 IEEE International Solid-State Circuits Conference (ISSCC)*. Vol. 67. 2024, pp. 534–536. DOI: 10.1109/ISSCC49657.2024.10454540.

[155] Anil Kumar Kumaran, Masoud Pashaeifar, Mats Alexanderson, Leonardus Cornelis Nicolaas de Vreede, and Morteza S. Alavi. "A Single-Supply Balun-First Three-Way mm-Wave Doherty PA". In: *IEEE Transactions on Microwave Theory and Techniques* (2024), pp. 1–16. DOI: 10.1109/TMTT.2024.3365697.

[156] J. D. Dunworth, A. Homayoun, B-H. Ku, Y-C. Ou, K. Chakraborty, G. Liu, T. Segoria, J. Lerdworatawee, J. W. Park, H-C. Park, H. Hedayati, D. Lu, P. Monat, K. Douglas, and V. Aparin. "A 28GHz Bulk-CMOS dual-polarization phased-array transceiver with 24 channels for 5G user and basestation equipment". In: *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*. 2018, pp. 70–72. DOI: 10.1109/ISSCC.2018.8310188.

[157] Yusheng Yin, Berktug Ustundag, Kerim Kibaroglu, Mustafa Sayginer, and Gabriel M. Rebeiz. "Wideband 23.5–29.5-GHz Phased Arrays for Multistandard 5G Applications and Carrier Aggregation". In: *IEEE Transactions on Microwave Theory and Techniques* 69.1 (2021), pp. 235–247. DOI: 10.1109/TMTT.2020.3024217.

[158] Yun Wang, Rui Wu, Jian Pang, Dongwon You, Ashbir Aviat Fadila, Rattanan Saengchan, Xi Fu, Daiki Matsumoto, Takeshi Nakamura, Ryo Kubozoe, Masaru Kawabuchi, Bangan Liu, Haosheng Zhang, Junjun Qiu, Hanli Liu, Naoki Oshima, Keiichi Motoi, Shinichi Hori, Kazuaki Kunihiro, Tomoya Kaneko, Atsushi Shirane, and Kenichi Okada. "A 39-GHz 64-Element Phased-Array Transceiver With Built-In Phase and Amplitude Calibrations for Large-Array 5G NR in 65-nm CMOS". In: *IEEE Journal of Solid-State Circuits* 55.5 (2020), pp. 1249–1269. DOI: 10.1109/JSSC.2020.2980509.

[159] Ali M. Darwish, Amr A. Ibrahim, Joe X. Qiu, Edward Viveiros, and H. Alfred Hung. "A Broadband 1-to-N Power Divider/Combiner With Isolation and Reflection Cancellation". In: *IEEE Transactions on Microwave Theory and Techniques* 63.7 (2015), pp. 2253–2263. DOI: 10.1109/TMTT.2015.2431690.

[160] Michael Boers, Bagher Afshar, Iason Vassiliou, Saikat Sarkar, Sean T. Nicolson, Ehsan Adabi, Bevin George Perumana, Theodoros Chalvatzis, Spyros Kavvadias, Padmanava Sen, Wei Liat Chan, Alvin Hsing-Ting Yu, Ali Parsa, Med Nariman, Seunghwan Yoon, Alfred Grau Besoli, Chryssoula A. Kyriazidou, Gerasimos Zochios, Jesus A. Castaneda, Tirdad Sowlati, Maryam Rofougaran, and Ahmadreza Rofougaran. "A 16TX/16RX 60 GHz 802.11ad Chipset With Single Coaxial Interface and Polarization Diversity". In: *IEEE Journal of Solid-State Circuits* 49.12 (2014), pp. 3031–3045. DOI: 10.1109/JSSC.2014.2356462.

[161] Alexander Tomkins, Alan Poon, Eric Juntunen, Ahmed El-Gabaly, Grigori Temkine, Yat-Loong To, Craig Farnsworth, Arash Tabibiazar, Mohammad Fakharzadeh, Saman Jafarlou, Ahmed Abdellatif, Hatem Tawfik, Brad Lynch, Mihai Tazlauanu, and Ronald Glibbery. "A 60 GHz, 802.11ad/WiGig-Compliant Transceiver for Infrastructure and Mobile Applications in 130 nm SiGe BiCMOS". In: *IEEE Journal of Solid-State Circuits* 50.10 (2015), pp. 2239–2255. DOI: 10.1109/JSSC.2015.2436900.

[162] Bodhisatwa Sadhu, Alberto Valdes-Garcia, Jean-Olivier Plouchart, Herschel Ainspan, Arpit K. Gupta, Mark Ferriss, Mark Yeck, Mihai Sanduleanu, Xiaoxiong Gu, Christian W. Baks, Duixian Liu, and Daniel Friedman. "A 250-mW 60-GHz CMOS Transceiver SoC Integrated With a Four-Element AiP Providing Broad Angular Link Coverage". In: *IEEE Journal of Solid-State Circuits* 55.6 (2020), pp. 1516–1529. DOI: 10.1109/JSSC.2019.2943918.

[163] Davide Guermandi, Qixian Shi, Andy Dewilde, Veerle Derudder, Ubaid Ahmad, Annachiara Spagnolo, Ilja Ocket, André Bourdoux, Piet Wambacq, Jan Craninckx, and Wim Van Thillo. "A 79-GHz 2 × 2 MIMO PMCW Radar SoC in 28-nm CMOS". In: *IEEE Journal of Solid-State Circuits* 52.10 (2017), pp. 2613–2626. DOI: 10.1109/JSSC.2017.2723499.

[164] Milad Kalantari, Wang Li, Hossein Shirinabadi, Ali Fotowat-Ahmady, and C. Patrick Yue. "A W-Band Single-Antenna FMCW Radar Transceiver With Adaptive Leakage Cancellation". In: *IEEE Journal of Solid-State Circuits* 56.6 (2021), pp. 1655–1667. DOI: 10.1109/JSSC.2020.3032677.

[165] Tolga Dinc, Sachin Kalia, Siraj Akhtar, Baher Haroun, Benjamin Cook, and Swaminathan Sankaran. "High-Efficiency Class-E Power Amplifiers for mmWave Radar Sensors: Design and Implementation". In: *IEEE Journal of Solid-State Circuits* 57.5 (2022), pp. 1291–1299. DOI: 10.1109/JSSC.2022.3147723.

[166] Ashutosh Verma, Venu Bhagavatula, Amitoj Singh, Wanghua Wu, Hariharan Nagarajan, Pak-Kim Lau, Xiaohua Yu, Omar Elsayed, Ajaypat Jain, Anirban Sarkar, Fan Zhang, Che-Chun Kuo, Patrick McElwee, Pei-Yuan Chiang, Chengkai Guo, Zhanjun Bai, Tienyu Chang, Abishek Mann, Andreas Rydin, Xingliang Zhao, Jeiyoung Lee, Daeyoung Yoon, Chih-Wei Yao, Siuchuang Ivan Lu, Sang Won Son, and Thomas B. Cho. "A 16-Channel, 28/39GHz Dual-Polarized 5G FR2 Phased-Array Transceiver IC with a Quad-Stream IF Transceiver Supporting Non-Contiguous Carrier Aggregation up to 1.6GHz BW". In: *2022 IEEE International Solid-State Circuits Conference (ISSCC)*. Vol. 65. 2022, pp. 1–3. DOI: 10.1109/ISSCC42614.2022.9731664.

[167] Bodhisatwa Sadhu, Arun Paidimarri, Duixian Liu, Mark Yeck, Caglar Ozdag, Yujiro Tojo, Wooram Lee, Kevin Xiaoxiong Gu, Jean-Olivier Plouchart, Christian W. Baks, Yusuke Uemichi, Sudipto Chakraborty, Yo Yamaguchi, Ning Guan, and Alberto Valdes-Garcia. "A 24–30-GHz 256-Element Dual-Polarized 5G Phased Array Using Fast On-Chip Beam Calculators and Magnetoelectric Dipole Antennas". In: *IEEE Journal of Solid-State Circuits* 57.12 (2022), pp. 3599–3616. DOI: 10.1109/JSSC.2022.3204807.

[168] J. D. Dunworth, A. Homayoun, B-H. Ku, Y-C. Ou, K. Chakraborty, G. Liu, T. Segoria, J. Lerdworatawee, J. W. Park, H-C. Park, H. Hedayati, D. Lu, P. Monat, K. Douglas, and V. Aparin. "A 28GHz Bulk-CMOS dual-polarization phased-array transceiver with 24 channels for 5G user and basestation equipment". In: *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*. 2018, pp. 70–72. DOI: 10.1109/ISSCC.2018.8310188.

[169] Shahriar Shahramian, Michael Holyoak, Mike Zierdt, Mustafa Sayginer, Joe Weiner, Amit Singh, and Yves Baeyens. “An All-Silicon E-Band Backhaul-on-Glass Frequency Division Duplex Module with >24dBm PSAT & 8dB NF”. In: *2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. 2022, pp. 59–62. DOI: 10.1109/RFIC54546.2022.9863150.

[170] Susnata Mondal, Rahul Singh, and Jeyanandh Paramesh. “21.3 A Reconfigurable Bidirectional 28/37/39GHz Front-End Supporting MIMO-TDD, Carrier Aggregation TDD and FDD/Full-Duplex with Self-Interference Cancellation in Digital and Fully Connected Hybrid Beamformers”. In: *IEEE ISSCC*. 2019, pp. 348–350. DOI: 10.1109/ISSCC.2019.8662468.

[171] Robin Garg, Sanket Jain, Paul Dania, and Arun Natarajan. “14.3 A 26GHz Full-Duplex Circulator Receiver with 53dB/400MHz(40dB/800MHz) Self-Interference Cancellation for mm-Wave Repeaters”. In: *IEEE ISSCC*. Vol. 64. 2021, pp. 222–224. DOI: 10.1109/ISSCC42613.2021.9365979.

[172] Susnata Mondal and Jeyanandh Paramesh. “Power-Efficient Design Techniques for mm-Wave Hybrid/Digital FDD/Full-Duplex MIMO Transceivers”. In: *IEEE Journal of Solid-State Circuits* 55.8 (2020), pp. 2011–2026. DOI: 10.1109/JSSC.2020.2987691.

[173] B. van Liempd, J. Craninckx, R. Singh, P. Reynaert, S. Malotaux, and J.R. Long. “A Dual-Notch +27dBm Tx-Power Electrical-Balance Duplexer”. In: *ESSCIRC 2014 - 40th European Solid State Circuits Conference (ESSCIRC)*. 2014, pp. 463–466. DOI: 10.1109/ESSCIRC.2014.6942122.

[174] Gengzhen Qi, Barend van Liempd, Pui-In Mak, Rui P. Martins, and Jan Craninckx. “A SAW-Less Tunable RF Front End for FDD and IBFD Combining an Electrical-Balance Duplexer and a Switched-LC N-Path LNA”. In: *IEEE Journal of Solid-State Circuits* 53.5 (2018), pp. 1431–1442. DOI: 10.1109/JSSC.2018.2791477.

[175] Kejian Shi, Hooman Darabi, and Asad A. Abidi. “Design and Analysis of an Electrical Balance Duplexer With Independent and Concurrent Dual-Band TX-RX Isolation”. In: *IEEE Journal of Solid-State Circuits* 57.5 (2022), pp. 1385–1396. DOI: 10.1109/JSSC.2021.3135509.

[176] Jun Hwang, Dongho Yoo, and Byung-Wook Min. “Compact mm-Wave Ultra-Wideband and Low-Noise Phase Alternately Distributed Quasi-Circulators”. In: *IEEE Journal of Solid-State Circuits* 59.5 (2024), pp. 1351–1360. DOI: 10.1109/JSSC.2024.3358338.

[177] Negar Reiskarimian, Jin Zhou, and Harish Krishnaswamy. “A CMOS Passive LPTV Nonmagnetic Circulator and Its Application in a Full-Duplex Receiver”. In: *IEEE Journal of Solid-State Circuits* 52.5 (2017), pp. 1358–1372. DOI: 10.1109/JSSC.2017.2647924.

[178] Negar Reiskarimian, Mahmood Baraani Dastjerdi, Jin Zhou, and Harish Krishnaswamy. “Analysis and Design of Commutation-Based Circulator-Receivers for Integrated Full-Duplex Wireless”. In: *IEEE Journal of Solid-State Circuits* 53.8 (2018), pp. 2190–2201. DOI: 10.1109/JSSC.2018.2828827.

[179] Mahmood Baraani Dastjerdi, Sanket Jain, Negar Reiskarimian, Arun Natarajan, and Harish Krishnaswamy. "Analysis and Design of a Full-Duplex Two-Element MIMO Circulator-Receiver With High TX Power Handling Exploiting MIMO RF and Shared-Delay Baseband Self-Interference Cancellation". In: *IEEE Journal of Solid-State Circuits* 54.12 (2019), pp. 3525–3540. DOI: 10.1109/JSSC.2019.2945303.

[180] Negar Reiskarimian, Mohammad Khorshidian, and Harish Krishnaswamy. "Inductorless, Widely Tunable N-Path Shekel Circulators Based on Harmonic Engineering". In: *IEEE Journal of Solid-State Circuits* 56.5 (2021), pp. 1425–1437. DOI: 10.1109/JSSC.2021.3063383.

[181] Pingyue Song and Hossein Hashemi. "mm-Wave Mixer-First Receiver with Passive Elliptic Low-pass Filter". In: *IEEE RFIC*. 2020, pp. 271–274. DOI: 10.1109/RFIC49505.2020.9218288.

[182] Sandeep Hari, Cody J. Ellington, and Brian A. Floyd. "A 6-31 GHz Tunable Reflection-Mode N-Path Filter". In: *IEEE RFIC*. 2021, pp. 143–146. DOI: 10.1109/RFIC51843.2021.9490492.

[183] Zachariah G Boynton and Alyosha Molnar. "A 9-31GHz 65nm CMOS Down-Converter with >4dBm OOB B1dB". In: *IEEE RFIC*. 2020, pp. 279–282. DOI: 10.1109/RFIC49505.2020.9218432.

[184] Ce Yang, Shiyu Su, and Mike Shuo-Wei Chen. "Millimeter-Wave Receiver With Non-Uniform Time-Approximation Filter". In: *IEEE Journal of Solid-State Circuits* 58.5 (2023), pp. 1201–1211. DOI: 10.1109/JSSC.2023.3243044.

[185] Junfeng Guan, Arun Paidimarri, Alberto Valdes-Garcia, and Bodhisatwa Sadhu. "3-D Imaging Using Millimeter-Wave 5G Signal Reflections". In: *IEEE Transactions on Microwave Theory and Techniques* 69.6 (2021), pp. 2936–2948. DOI: 10.1109/TMTT.2021.3077896.

[186] Yuan-Ching Lien, Eric A. M. Klumperink, Bernard Tenbroek, Jon Strange, and Bram Nauta. "Enhanced-Selectivity High-Linearity Low-Noise Mixer-First Receiver With Complex Pole Pair Due to Capacitive Positive Feedback". In: *IEEE Journal of Solid-State Circuits* 53.5 (2018), pp. 1348–1360. DOI: 10.1109/JSSC.2018.2791490.

[187] Osamu Ikeuchi, Nobuo Saito, and Bram Nauta. "Quadrature sampling mixer topology for SAW-Less GPS receivers in 0.18μm CMOS". In: *Symposium on VLSI Circuits*. 2010, pp. 177–178. DOI: 10.1109/VLSIC.2010.5560309.

List of Acronyms

2G Second-generation
5G Fifth-generation
ACLR Adjacent Channel Leakage Ratios
AIP2 Antenna-port Referred Input Power 2nd Order
AIP3 Antenna-port Referred Input Power 3rd Order
AM-AM Amplitude-to-Amplitude Distortions
AM-PM Amplitude-to-Phase Distortions
AWG Arbitrary-Wave Generator
BB Baseband
BER Bit Error Rate
BPA Balanced Power Amplifier
BPF Band-Pass Filter
BPSK Binary Phase-Shift Keying
BW Bandwidth
CC Component Carrier
CMOS Complementary Metal-Oxide-Semiconductor
CW Continuous Wave
DA Drive Amplifier
DAC Digital-to-Analog Converter
DPA Doherty Power Amplifier
DPD Digital Pre-Distortion
DSP Digital Signal Processing
DUC Direct Up-Conversion
EBD Electrically Balanced Duplexer
EIRP Equivalent Isotropically Radiated Power
ET Envelope Tracking
EVM Error Vector Magnitude
FDD Frequency Division Duplex
FMCW Frequency-Modulated Continuous-Wave
FR2 Frequency Range 2
IB Inband
IC Integrated Circuit
IMD Intermodulation Distortion
IMD3 Intermodulation Distortion 3rd Order
IIP2 Input Intercept Point 2nd Order
IIP3 Input Intercept Point 3rd Order
IoT Internet-of-things
I/Q In-phase and Quadrature

IQMM In-phase and Quadrature Mismatch
IRR Image Rejection Ratio
KPI Key Performance Indicator
LLPA Load-Modulated Linear Power Amplifier
LM Link Margin
LMBA Load-Modulated Balanced Amplifiers
LNA Low Noise Amplifier
LO Local Oscillator
LOFT Local Oscillator Feedthrough
LOS Line of Sight
LPTV Linear Periodic Time-Variant
MAPL Maximum Allowable Path Loss
MC Monte Carlo
m-MIMO massive Multi-Input Multi-Output
mm-wave Millimeter Wave
NF Noise Figure
NR New Radio
OFDM Orthogonal Frequency-Division Multiplexing
OIP3 Output Intercept Point 3rd Order
OOB Out-of-Band
OP_{1dB} Output 1dB Compression Point
OTA Over-the-Air
PA Power Amplifier
PAE Power-Added Efficiency
PAPR Peak-to-Average Power Ratio
PBO Power Back-Off
PCB Printed Circuit Board
PDPA Parallel-Doherty Power Amplifier
PSIV Post-Silicon Inter-Stage Passive Validation
PVT Process, Voltage, and Temperature
QAM Quadrature Amplitude Modulation
QHC Quadrature Hybrid Coupler
QPSK Quadrature Phase-Shift Keying
QTL Quarter-wave Transmission Line
RF Radio Frequency
RMS Root Mean Square
RX Receiver
SDPA Series-Doherty Power Amplifier
SF-FD Single-Frequency Full-Duplex
SFDR Spurious-Free Dynamic Range
SIC Self-Interference Cancellation
SISO Single-Input Single-Output
SNR Signal-to-Noise Ratio
SSB Single-Sideband
STAR Simultaneous Transmit and Receive

TDD Time Division Duplexing
TL Transmission Line
TRX Transceiver
TX Transmitter
VCO Voltage-Controlled Oscillator
VGA Variable Gain Amplifier
VSWR Voltage Standing Wave Ratio
wc Worst-Case

LIST OF FIGURES

LIST OF TABLES

SUMMARY

The availability of millimeter-wave (mm-wave) communication systems is a key enabler in developing the fifth generation (5G) mobile networks that offer higher data throughput, lower network latency, and improved link robustness. Namely, they take advantage of mm-wave phased arrays to empower 5G communication systems that establish directional links with large bandwidths between the base station and user equipment. Despite this huge potential, mm-wave 5G has several natural disadvantages. The shorter wavelength of mm-wave signals results in lower penetrability, higher free-space path loss, and susceptibility to atmospheric attenuation, limiting network coverage. Additionally, 5G systems, offering high data throughput, require the use of complex modulation signals and, as such, need to handle large amplitude variations, complicating achieving high energy efficiency. Furthermore, their increased receiver noise lowers the sensitivity and link budget, while their use of Nanometer CMOS technology limits their transmit power and efficiency, impacting system reliability and thermal management.

Unlike digital processors, whose performance and efficiency improve with semiconductor technology scaling, the performance of analog/RF front ends mainly relies on circuit and system architecture innovations. Luckily, operating at mm-wave frequencies unlocks new opportunities, and an approach using those can exceed initial expectations. In this context, this dissertation introduces a series of innovative designs and techniques enhancing the performance and efficiency of power amplifiers (PAs) and transceivers for 5G mm-wave systems.

Chapter 3 unveils a two-step impedance inverting-based series-Doherty combiner with a compact design and broadband load modulation, along with a detailed design framework derived from 5G specifications. The chapter also explores the linearity limitations of Doherty Power Amplifiers, particularly the AM-AM/AM-PM distortions caused by load modulation, and introduces a post-silicon inter-stage passive validation approach to improve prototype evaluation. The proposed series-Doherty PA achieves state-of-the art performance across the 24-to-30GHz band.

Chapter 4 presents a broadband TX solution tailored for 5Gmm-wave phased-array systems, featuring a double-quadrature direct upconverter and a series-Doherty balanced PA. This PA structure is designed for enhanced efficiency, delivering 20dBm output power and improving power back-off efficiency in the presence of voltage standing wave ratio (VSWR) conditions induced by the mutual antenna coupling in phased arrays. This TX architecture also boasts the image rejection ratio and superior uncalibrated local oscillator feedthrough suppression due to its symmetric layout and meticulous design considerations.

Chapter 5 introduces a load-modulation-based IMD3 cancellation technique for class-B CMOS PAs, which significantly reduces intermodulation distortion, provides enhanced error-vector magnitude (EVM), and improved adjacent channel leakage ratio (ACLR) for a 50MHz 64-QAM OFDM signal.

Chapters 6 and **7** discuss innovative PA designs for mm-wave phased-array systems. **Chapter 6** introduces an N-way chain-weaver balanced PA designed to maintain linearity and gain under varying VSWR conditions, featuring an embedded impedance/power sensor. This PA architecture is demonstrated to support a 2GHz 64- QAM OFDM signal with high accuracy and minimal AM-PM distortion across a 3GHz bandwidth.

Chapter 7, in conclusion, presents a fully integrated mm-wave FDD transceiver front-end with a two-stage PA and an integrated circulator functioning as a duplexer. This is the first PA with an integrated isolator to enhance VSWR resilience. The chapter details the compact design and efficient performance of this front-end, which occupies only $0.7 mm^2$ and is VSWR resilient.

SAMENVATTING

De beschikbaarheid van millimetergolf (mm-wave) communicatiesystemen wordt als een belangrijke voorwaarde beschouwd in de ontwikkeling van de vijfde generatie (5G) mobiele netwerken, welke hogere datasnelheden, kortere responsetijden en een verbeterde netwerkbetrouwbaarheid mogelijk maken. Door gebruik te maken van "mm-wave Phase-Array" antennes kunnen 5G-communicatiesystemen namelijk directionele links met een grote bandbreedte tot stand brengen tussen het basisstation en de gebruikersapparatuur. Ondanks dit enorme potentieel hebben 5G mm-wave systemen ook een aantal natuurlijke nadelen. Het gebruik van een kortere golflengte resulteert namelijk in een geringere doordringbaarheid van gebouwen, hogere propagatie verliezen in de vrije ruimte en gevoeligheid voor atmosferische verzwakking die de dekking van een mm-wave 5G netwerk beperken. Deze systemen hebben te maken met een verhoogd ruisniveau in hun ontvangers, wat leidt tot een lagere gevoeligheid en dus geringere netwerkdekking. Het gebruik van complex-gemoduleerde signalen met grote amplitude variaties bemoeilijkt verder het energiezuinig maken van deze systemen. Terwijl de gebruikte nanometer-CMOS technologie voor hun implementatie aanleiding geeft tot beperkingen in zendvermogen en -efficiëntie, welke van invloed zijn op de systeem betrouwbaarheid en de thermisch eigenschappen.

In tegenstelling tot digitale applicaties, zoals rekenprocessoren, waarvan de prestaties en efficiëntie aanzienlijk verbeteren met de vooruitgang in halfgeleidertechnologie, zijn de prestatie van analoge/RF zenders en ontvangers voornamelijk afhankelijk van innovaties in hun schakelingen en systeemarchitectuur. Gelukkig geeft werken op mm-golf frequenties ook nieuwe mogelijkheden en kan een aanpak die hier gebruik van maakt de oorspronkelijke verwachtingen overtreffen. In deze context introduceert dit proefschrift een reeks innovatieve ontwerpen en technieken gericht op het verbeteren van de prestaties en efficiëntie van eindversterkers (PA's) en zend/ontvangers voor 5G mm-wave systemen.

Hoofdstuk 3 introduceert een breedbandige twee-stap-impedantie-inverterende serie-Doherty combiner, samen met zijn ontwerpkader welke is afgeleid van 5G specificaties. Dit hoofdstuk onderzoekt ook de lineariteit beperkingen van de Doherty Power Amplifier, met name de AM-AM/AMPM-vervorming veroorzaakt door de load-modulatie. Een passieve vermogenssensor wordt geïntroduceerd om de post-silicium validatie/evaluatie van prototypes te verbeteren. De voorgestelde serie-Doherty PA bereikt "state-of-the-art" prestaties in de 24-30 GHz band.

Hoofdstuk 4 presenteert een breedband TX-oplossing voor 5G mm-wave Phased-Array systemen, met een dubbel-kwadratuur-upconverter en een serie-Doherty gebalanceerde PA. Deze PA-structuur is ontworpen voor hoge efficiëntie, levert 20dBm uitgangsvermogen en verbetert de efficiëntie in aanwezigheid van VSWR-condities (Voltage Standing Wave Ratio) welke worden veroorzaakt door de onderlinge koppeling van de antennes in een Phased-Array systeem. De TX-architectuur heeft ook een hoge spiegel-

frequentie onderdrukkingsverhouding en een superieure niet gekalibreerde onderdrukking van het signaal van de lokale oscillator dankzij een zorgvuldig ontwerp en symmetrische IC-layout.

Hoofdstuk 5 introduceert een impedantie-modulatie gebaseerde intermodulatie-onderdrukkingstechniek voor klasse-B CMOS PA's, welke de vervorming (IM3), de foutvectormagnitude (EVM) en de aangrenzend kanaal signaal/lek verhouding (ACLR) aanzienlijk verbeterd voor een 50 MHz 64-QAM OFDM-signaal.

De hoofdstukken 6 en **7** behandelen innovatieve PA-ontwerpen voor mm-wave Phased-Array systemen. **Hoofdstuk 6** introduceert een N-way Chain-Weaver gebalanceerde PA met ingebouwde impedantie/vermogenssensors, ontworpen om de lineariteit en versterking te behouden onder variërende VSWR-conditie. Er wordt aangetoond dat deze PA-architectuur een 2GHz 64-QAM OFDM-signaal met hoge nauwkeurigheid en minimale AM-PM-vervorming ondersteunt over een bandbreedte van 3GHz.

Hoofdstuk 7 presenteert tenslotte een volledig geïntegreerd mm-wave frequentie-domein-gescheiden (FDD) zend/ontvanger front-end met een tweetraps PA en een geïntegreerde circulator die als duplexer functioneert. Dit is de eerste realisatie van een PA met een geïntegreerde isolator om de VSWR-bestendigheid te verbeteren. Het hoofdstuk beschrijft het compacte ontwerp en de efficiëntie prestaties van dit front-end, dat slechts 0,7 mm2 in beslag neemt en VSWR-bestendig is.

LIST OF PUBLICATIONS

Journals:

- **M. Pashaeifar**, A. K. Kumaran, L. C. N. de Vreede, and M. S. Alavi, "A Chain-Weaver Balanced Power Amplifier with an Embedded Impedance/Power Sensor," in *IEEE Journal of Solid-State Circuits (Early access)*, pp. 1-14, 2024. (*Special ISSCC issue*)

- **M. Pashaeifar**, L. C. N. de Vreede, and M. S. Alavi, "A Millimeter-Wave CMOS Series-Doherty Power Amplifier With Post-Silicon Inter-Stage Passive Validation," in *IEEE Journal of Solid-State Circuits*, vol. 57, no. 10, pp. 2999-3013, Oct. 2022. (*Special A-SSCC issue*)

- **M. Pashaeifar**, L. C. N. de Vreede, and M. S. Alavi, "A Millimeter-Wave Mutual-Coupling-Resilient Double-Quadrature Transmitter for 5G Applications," in *IEEE Journal of Solid-State Circuits*, vol. 56, no. 12, pp. 3784-3798, Dec. 2021. (*Special ISSCC issue*)

- **M. Pashaeifar**, L. C. N. de Vreede, and M. S. Alavi, "Load-Modulation-Based IMD3 Cancellation for Millimeter-Wave Class-B CMOS Power Amplifiers Achieving EVM < 1.2%," in *IEEE Microwave and Wireless Components Letters*, vol. 32, no. 6, pp. 716-719, June 2022. (*Special IMS issue*)

- **M. Pashaeifar**, L. C. N. de Vreede, and M. S. Alavi, "A Millimeter-Wave Power Amplifier with an Integrated CMOS Isolator/Circulator/Receiver," in *IEEE Journal of Solid-State Circuits*, *under review.*

- A. K. Kumaran, **M. Pashaeifar**, M. Alexanderson, L. C. N. de Vreede, and M. S. Alavi, "A Single-Supply Balun-First Three-Way mm-Wave Doherty PA," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 72, no. 5, pp. 2757-2772, May 2024. (*Special RFIC issue*)

Conferences:

- **M. Pashaeifar**, A. K. Kumaran, L. C. N. de Vreede and M. S. Alavi, "32.7 A 25.2dBm P_{SAT}, 35-to-43GHz VSWR-Resilient Chain-Weaver Eight-Way Balanced PA with an Embedded Impedance/Power Sensor," *2024 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2024, pp. 532-534.

- **M. Pashaeifar**, L. C. N. de Vreede, and M. S. Alavi, "14.4 A 24-to-30GHz Double-Quadrature Direct-Upconversion Transmitter with Mutual-Coupling-Resilient Series-Doherty Balanced PA for 5G MIMO Arrays," *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2021, pp. 223-225.

- **M. Pashaeifar**, A. K. Kumaran, M. Beikmirza, L. C. N. de Vreede and M. S. Alavi, "A 24-to-32GHz series-Doherty PA with two-step impedance inverting power combiner achieving 20.4dBm Psat and 38%/34% PAE at Psat/6dB PBO for 5G applications," *2021 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Busan, Korea, Republic of, 2021, pp. 1-3.

- **M. Pashaeifar**, L. C. N. De Vreede and M. S. Alavi, "A Millimeter-Wave Front-End for FD/FDD Transceivers Featuring an Embedded PA and an N-Path Filter Based Circulator Receiver," *2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Denver, CO, USA, 2022, pp. 11-14.

- **M. Pashaeifar**, , L. C. N. de Vreede, and M. S. Alavi, "Load-Modulation-Based IMD3 Cancellation for Millimeter-Wave Class-B CMOS Power Amplifiers Achieving EVM < 1.2%," 2022 *IEEE/MTT-S International Microwave Symposium-IMS 2022*, Denver, CO, USA, 2022. (*Best student paper candidate*)

- A. K. Kumaran, **M. Pashaeifar**, H. M. Nemati, L. C. N. de Vreede and M. S. Alavi, "A 26GHz Balun-First Three-Way Doherty PA in 40nm CMOS with 20.7 dBm Psat and 20dB Power Gain," *2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Diego, CA, USA, 2023, pp. 189-192.

- A. K. Kumaran, **M. Pashaeifar**, M. D'Avino, L. C. N. de Vreede and M. S. Alavi, "On-Chip Output Stage Design for a Continuous Class-F Power Amplifier," *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, Daegu, Korea, 2021, pp. 1-5.

ACKNOWLEDGEMENTS

As I approach the conclusion of this long and challenging chapter of my life, I find myself filled with a mixture of delight and, if you can believe it, a tinge of sadness. My PhD journey has been marked by incredible moments, and I have had the privilege of learning from and sharing this path with many remarkable individuals. I would like to take this opportunity to express my sincere gratitude to those who have been an integral part of my academic and personal growth.

First and foremost, I extend my deepest appreciation to Dr. Morteza Alavi, my co-promoter and advisor. From the very beginning, you placed your trust in my passion for research, even though my experience in RFIC design was limited. You gave me the freedom to explore and encouraged me to chart my own course, always offering unwavering support without ever imposing your ideas or opinions. Your ability to recognize potential, even when I was unsure of my own capabilities, was one of the greatest gifts anyone could have given me.

I vividly remember, just a few days before my first tape-out, you asked if I wanted to attempt a second chip. Three days later, when you returned, you were surprised to see that I had already made a draft layout. Your support during that time, especially extending the deadline to allow me to finish my second chip in just 10 days, meant the world to me. It was a testament to your belief in me and your commitment to pushing me beyond what I thought was possible.

Your guidance has always been focused on helping me become the best version of myself, not only as a researcher but also as an individual. One moment stands out in particular—when we had to withdraw my second ISSCC submission. It was one of the most difficult and frustrating moments of my academic career, but your calm reassurance and unwavering support helped me navigate that disappointment with grace and integrity. You taught me that success is not only about achieving results but about the strength of character we demonstrate in the face of setbacks.

Throughout this journey, you have been more than an academic advisor—you have been a mentor in every sense of the word. I consider myself incredibly fortunate, not only because of your technical brilliance but because of the kindness and understanding you've shown me time and again. Your influence extends far beyond the lab; you have shaped the way I approach challenges, how I lead, and how I persevere.

Thank you, Morteza, for everything. Your guidance, support, and belief in me have truly shaped my PhD journey in ways I will never forget.

I would also like to express my heartfelt gratitude to my PhD promoter, Prof. Leo de Vreede. As the head of our group, you generously accepted me as a PhD student and have supported me throughout the past six years. I will never forget the moment during my first chip measurement when I was struggling with the VSWR measurement due to the lack of a tuner. Despite the challenge, you patiently listened to my concerns and, within

just two days, you found a solution that turned out to be one of the pivotal moments of my academic journey.

Your feedback has consistently elevated our work, helping us move from good to excellent. Like Morteza, you never imposed your views, always allowing me the space to pursue my own ideas and forge my own path. Your guidance has been invaluable, and I am deeply thankful for your mentorship and support.

My appreciation is also extended to my Ph.D. committee members, Prof. Wang, Prof. Nauta, Prof. Wambacq, Prof. Smolders, Prof. Makinwa, and Prof. Serdijn. Thank you for reviewing my Ph.D. dissertation and providing insightful comments. Also, I would like to express our gratitude to Marcel Geurts, Domine Leenaerts, Paul Mattheijssen, Jawad Qureshi, and Mustafa Acar from NXP Semiconductors.

My Ph.D. would not have been completed without the help and support of several experts. First, I am grateful to Atef Akhnoukh, who patiently assisted Ph.D. students during the tape-out phases; second, to Zu Yao Chang, who precisely wire-bonded my chips and miraculously saved my first chip after it was damaged during measurement, just one week before the ISSCC deadline; third, to Antoon Frehe, whose exceptional support with hardware and software greatly facilitated the tape-out process; and last, but not least, to Dr. Juan Bueno, who provided invaluable support during measurements, especially for my last chip, where time was limited. Thank you all. I would also like to acknowledge our wonderful group secretary, Marion de Vlieger. Thank you very much, Marion, for smoothly coordinating all the numerous requests I constantly sent your way.

My PhD journey didn't truly begin on June 5, 2018, at TU Delft, but almost four years earlier at the University of Tehran. I had the privilege of working under the supervision of Dr. Mehdi Kamal and Prof. Ali Afzali-Kusha, and I am deeply grateful for your unwavering support and for teaching me how to conduct high-quality research. During the final stage of my PhD, when I was on the verge of quitting, your understanding and encouragement were invaluable, and for that, I will always be indebted to you. I would also like to express my heartfelt thanks to Prof. Massoud Pedram for his insightful feedback, thoughtful comments, and constant encouragement. I am proud to have had the opportunity to collaborate with such an exceptional team.

Additionally, I want to extend my appreciation to Dr. Masoud Babaei for his invaluable help, feedback, and support throughout my PhD. Your wisdom and advice have been indispensable, and I am especially grateful for the time you took out of your busy schedule to offer honest and constructive feedback. Your kindness and generosity will always be remembered.

A special thank you goes to the remarkable Dr. Marco Spirito. Your insightful and helpful comments, particularly in relation to measurement techniques, have been immensely valuable. Beyond your technical expertise, your kindness, charm, and thoughtfulness made working together a pleasure. Our technical discussions were both enjoyable and enlightening—your brilliance shines through in everything you do.

I would like to express my deep gratitude to my dear friends, Milad Kalami and Dr. Milad Kalantari. You introduced me to the elegance and beauty of RF, which ultimately led me to change my field of study. Our 40-minute online discussion on Doherty Power Amplifiers remains the most productive time of my professional life, during which I gained a deep understanding of the Doherty PA principles. You are, without a doubt,

the most brilliant engineers I have ever had the pleasure of working with.

Now that I am so close to finishing my Ph.D. study, I cannot resist thinking about my M.Sc. advisor Dr. Shahin Jafarabadi Ashtiani who started me on this path. I had never before felt the joy that I did in his lectures for the course of Analog CMOS Integrated Circuits.

My appreciation is also forwarded to Mohsen Mortazavi, Mohammad Ali Montazerolghaem, Mohammadreza Beikmirza, Milad Mehrpoo, Mohsen Hashemi, Nasim Bakhshaee, and Nawaf Almotairi for very nice professional, political, and personal discussions. I must send my gratitude to my friends and colleagues in ELCA: Gagan Singh, Anil Kumar Kumaran, Michele Squillante, Ehsan Shokrolahzadeh, Jun Feng, Rob Bootsman, Zhong Gao, Jingchu He, Dieuwert Mul, Richard Coesoij, Visweswaran Karunanithi, Maneesh Verma, Satoushi Malotaux, Carmine De Martino, Luca Galatro, Yiyu Shen, Yue Chen, Ronaldo Martins da Ponte, Alessandro Urso, Kambiz Nanbakhsh, Linghan Zhang, Ferry Musters, and Amitava Giri.

My appreciation is forwarded to my friends from the Iranian community in the Netherlands: Maryam and Milad, Nasim and Mohsen, Bahar and Mohammad Ali, Maryam and Amin, Boshra and Mohammadreza, Negin and Mohsen, Romina and Amir Hossein, Bahar and Milad, Zahra and Mojtaba, Samira and Amir Arsalan, Motahareh, and Mahdi. My appreciation also to my friends from Iran: Amir Hossein, Doctor Mohammadreza, Mahmoud (Aye Azad), Arash and Mahtab, and all members of "*Joke 2 New*" group.

I want to express the depths of my love and gratitude to my incredible parents, Maman and Baba. Your sacrifices, love, kindness, and unwavering support have been invaluable throughout my life. I owe everything to you. To my little sister, Mahsa, thank you for always standing by me with your love and kindness. I wish you and dear José a lifetime filled with happiness and joy.

I also wish to extend my gratitude to my wonderful parents-in-law, Laya and Ali, for their kindness, love, and continuous support. Thank you to Maryam, Shahriar, and our beautiful Anisa, as well as, of course, Samira.

Mahsa, my love, beyond and above all, I am endlessly grateful to you, my dearest. This entire journey began with you—my greatest supporter, my best friend, and my wisest adviser. Your love, kindness, wisdom, and simply your presence have given me the strength to endure and thrive throughout this long journey.

We've been through so much together, including postponing our wedding, which was eventually canceled due to the pandemic. During those challenging times, you became my greatest comfort—always there with unwavering support, no matter how difficult things got. You stood by me through endless nights and weekends of work, always understanding the demands of my PhD, never once faltering in your patience, love, and encouragement.

I know how many sacrifices you've made for me and I will be forever grateful for everything. I couldn't have done this without you by my side, and every achievement in this journey is as much yours as it is mine.

Masoud Pashaeifar
Munich, September 2024

About the Author

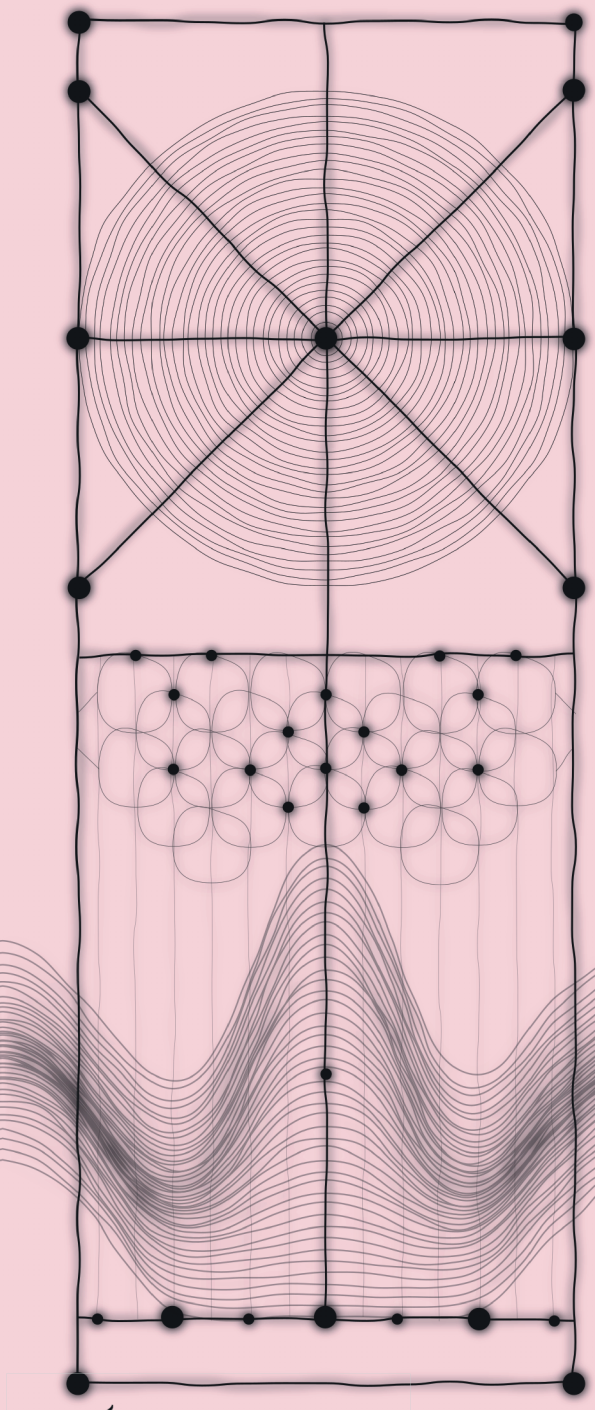
Masoud Pashaeifar received the B.Sc. degree from the Shahid Bahonar University of Kerman, Kerman, Iran, in 2011, and the M.Sc. degree in circuits and systems from the University of Tehran, Tehran, Iran, in 2013. He was the Head of the Hardware Research Group at Bakhtar Communication Company, Tehran, Iran, from 2014 to 2018. In 2018, he joined the Delft University of Technology, Delft, The Netherlands, as a PhD candidate. He has been with Apple Inc., Munich, Germany, since September 2022. His research interests include RF/mm-wave/sub-THz transceivers.

Mr. Pashaeifar received the IEEE Solid-State Circuits Society (SSCS) Predoctoral Achievement Award for 2021–2022. He serves as a Reviewer for the IEEE Journal of Solid-State Circuits, the IEEE Solid-State Circuits Letters, and the IEEE Transactions on Circuits and Systems–I: Regular Papers.

The Art of Connections!

As the digital and physical worlds become increasingly intertwined, the demands on communication systems continue to grow. At the heart of this evolution lies a quest not just for faster connections but for more intelligent, efficient, and adaptable technologies. In our pursuit of progress, we find ourselves constantly balancing the challenges of innovation with the desire for seamless connectivity.

This work explores the frontiers of communication, where invisible waves carry the lifeblood of our connected world. It is a journey into the science of transmission, the art of precision, and the ever-present need to push the boundaries of what is possible. In doing so, we shape the future of how we communicate, interact, and live in a world defined by information.



TU Delft

ISBN 978-94-6384-638-7