A Single-Stage Bias-Flip Regulating Rectifier With Fully Digital Duty-Cycle-Based MPPT for Piezoelectric Energy Harvesting

Yue, Xinling; Du, Sijun

DOI
10.1109/JSSC.2024.3495232

Publication date
2024

Document Version
Final published version

Published in
IEEE Journal of Solid-State Circuits

A Single-Stage Bias-Flip Regulating Rectifier With Fully Digital Duty-Cycle-Based MPPT for Piezoelectric Energy Harvesting

Xinling Yue, *Graduate Student Member, IEEE*, and Sijun Du, *Senior Member, IEEE*

***Abstract*— Piezoelectric energy harvesting (PEH) has been considered a promising solution for replacing conventional batteries to power wireless sensors. A complete PEH system typically includes three stages: ac–dc rectification, maximum power point tracking (MPPT), and output voltage regulation to power the load circuits. Unfortunately, most prior works focus only on the first one or two stages. A few employ three, but unfortunately, they are in cascaded stages, which results in cascaded power efficiency loss. This article proposes a single-stage bias-flip MPPT regulating rectifier (BMRR), which integrates the active bias-flip rectification, MPPT, and output voltage regulation into one stage. The proposed BMRR transfers energy from the piezoelectric transducer (PT) directly to the output capacitor by employing fewer switches, removing the conventional bridge rectifier, and eliminating cascaded energy loss. In addition, the design was implemented in a fully digital fast-MPPT technique based on an improved duty-cycle-based (DCB) algorithm to let the PT voltage jump to the maximum power point (MPP) in only one step. The proposed BMRR rectifier was fabricated in a 180-nm BCD process. The measured results show 930% power enhancement compared to a full bridge rectifier (FBR) and 92.5% end-to-end (E2E) efficiency.**

***Index Terms*— Duty-cycle-based (DCB) maximum power point tracking (MPPT), energy harvesting, MPPT, MPPT regulating rectifier, piezoelectric energy harvester, regulation, single-stage rectifier.**

I. Introduction

In THE era of the Internet of Things (IoT), a diverse array of wireless sensors is emerging to bridge the gap between the physical world and the digital realm. While conventional batteries have long served as the primary power source for these sensors, they come with several limitations, including limited lifespans, large system sizes, high maintenance costs, and harsh environmental conditions. In response, energy harvesting has garnered considerable attention as a promising alternative. This approach involves harvesting energy from ambient sources in the surrounding environment and converting it into electrical energy [1], [2], [3], [4], [5], [6], [7], [8], [9]. Vibration energy harvesting stands out among the various energy sources due to its versatility, high energy density, low frequency, and scalability.

Received 18 June 2024; revised 19 October 2024; accepted 5 November 2024. Date of publication 19 November 2024; date of current version 26 February 2025. This article was approved by Associate Editor Shaolan Li. This work was supported by the Dutch Research Council (NWO) under Grant 2022/TTW/01250918. *(Corresponding author: Sijun Du.)*

The authors are with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: sijun.du@tudelft.nl).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2024.3495232.

Digital Object Identifier 10.1109/JSSC.2024.3495232

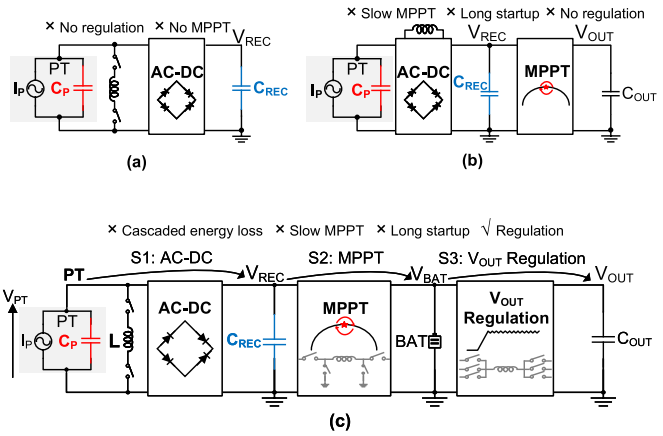


Fig. 1. Conventional one-stage [1], two-stage [10], and three-stage rectifiers for PEH. (a) Conventional one-stage ac–dc rectifier. (b) Conventional two-stage ac–dc + MPPT. (c) Conventional three-stage topology (S1→S2→S3).

Piezoelectric energy harvesting (PEH) uses a piezoelectric transducer (PT) to convert vibration energy into electrical energy. When the PT is vibration at its resonance, it can be represented as an ac current source I_P parallel to a capacitor C_P, as illustrated in Fig. 1. Due to the ac nature of PTs, an ac–dc rectifier is typically employed [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21]. Among rectifiers, a full bridge rectifier (FBR) is commonly used for its simplicity. However, FBRs suffer from low output power efficiency as the PT voltage reverses polarity at every zero-crossing moment of I_P, leading to charge loss. To address this issue, a bias-flip ac–dc rectifier was proposed, incorporating an inductor to aid PT flipping by forming an RLC oscillation loop, as depicted in Fig. 1(a) [1], [15], [21].

The power output from an synchronized switch harvesting on inductor (SSHI) rectifier is determined by several factors: the characteristics of the piezoelectric material, the properties of the excitation source, and the efficiency of the rectifier's flipping mechanism. Despite these parameters being initially fixed, the output power fluctuates with changes in the rectifier output voltage, V_{REC}. As V_{REC} increases from low to high, the output power rises to a peak and then declines, where the peak is called the maximum power point (MPP). Importantly, variations in the excitation source or bias-flipping efficiency cause shifts in this MPP, where the bias-flipping efficiency refers to the efficiency of PT voltage after bias-flipping over the voltage before flipping. To pinpoint the rectifier operating at this MPP, a technique called MPP tracking (MPPT) is required as

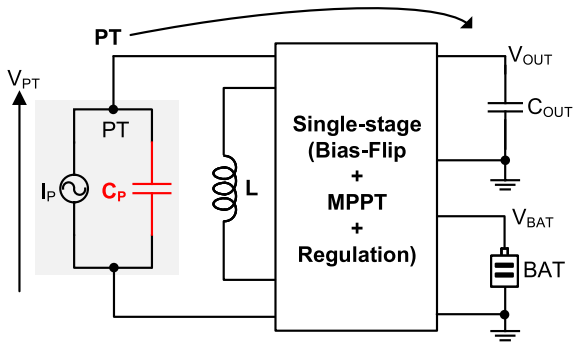


Fig. 2. Conceptual architecture of the proposed single-stage BMRR.

an additional stage following the rectifier. Many conventional MPPT techniques have been investigated, such as perturb and observe (P&O) [22], [23], fractional open-circuit voltage (FOCV) [6], [12], and sense and set [24]. However, most of them require an additional rectified capacitor for system operation. Fig. 1(b) illustrates a two-stage system cascading the bias-flipping rectification and MPPT stages. However, this setup exhibits extended startup times and sluggish MPPT due to a large C_{REC} and lacks output regulation.

To directly power the electronic loads, output regulation is also needed in a complete PEH system, as depicted in Fig. 1(c), which consists of three stages: a bias-flip ac–dc rectifier, an MPPT block, and an output voltage regulation stage. Energy transfer from the PT to the output capacitor C_{OUT} occurs following ac–dc rectification, MPPT, and output regulation, inevitably subject to cascaded energy loss [25].

This article proposes a single-stage bias-flip MPPT regulating rectifier (BMRR), integrating active bias-flipping rectification, MPPT, and output voltage regulation into a single-stage [26], as illustrated in Fig. 2. The proposed BMRR offers several advantages over previous designs.

1) *Simplified Topology:* By consolidating three essential functions into a single stage, the BMRR utilizes fewer switches, eliminating the need for a conventional bridge rectifier and C_{REC} for MPPT.
2) *Reduced Energy Loss:* Energy transfer from the PT to C_{OUT} is accomplished in one stage, eliminating cascaded energy loss.
3) *Efficient MPPT:* The BMRR employs a fast-MPPT technique based on an improved duty-cycle-based (DCB) algorithm [10], enabling the PT voltage (V_{PT}) to rapidly reach the MPP in one step.
4) *Digital MPPT Implementation:* A fully digital MPPT approach enhances higher accuracy and energy efficiency compared to its analog predecessor.

By integrating these advancements, the proposed BMRR represents a significant leap forward in the efficiency and performance of PEH systems.

II. Power Efficiency Analysis

In this section, the power conversion efficiency (PCE) of a conventional three-stage system and the proposed single-stage system are derived and compared.

A. Conventional Three-Stage Systems

When deriving the PCE of a conventional three-stage PEH system, the architecture of the three cascaded stages shown in Fig. 1(c) is used. This architecture consists of three power stages: an ac–dc bias-flip rectifier, an MPPT block, and an output regulator. Three storage elements are connected to the outputs of the three stages: C_{REC}, BAT, and C_{OUT}. When the PT is vibrating, the current source can be expressed as

$$I_P = I_0 \times \sin(\omega t) \tag{1}$$

where ω is the vibration excitation frequency. Therefore, the charge generated in a half-period is

$$Q_T = \int_0^{\frac{T}{2}} I_0 \sin(\omega t) dt = \frac{2I_0}{\omega}. \tag{2}$$

If the PT is disconnected from the rectifier and in an open circuit, the zero-to-peak open-circuit voltage amplitude (V_{OC}) is expressed by

$$V_{\mathrm{OC}} = \frac{1}{2} \times \frac{Q_T}{C_P} = \frac{I_0}{\omega C_P}. \tag{3}$$

In a conventional three-stage rectifier, in the first stage, an SSHI rectifier is used to flip PT voltage, where V_F can express the flipped voltage [27]

$$V_F = (V_{\mathrm{REC}} + 2V_D) \times e^{\frac{-\pi}{\sqrt{\frac{4L}{R^2C_P}-1}}} = (V_{\mathrm{REC}} + 2V_D)\eta_F \tag{4}$$

where V_D is the forward voltage drop of a diode in an FBR, and $\eta_F = e^{(-\pi/((4L/R^2C_P)-1)^{1/2})}$ is the flipping efficiency, with L as the inductance and R as the total resistance in the RLC loop. The voltage loss (V_L) after flipping can be written as

$$V_L = (V_{\mathrm{REC}} + 2V_D) \times (1 - \eta_F). \tag{5}$$

Hence, the charge flowing into C_{REC} is

$$Q_{\mathrm{SSHI}} = Q_T - C_P \times V_L = C_P(2V_{\mathrm{OC}} - V_L). \tag{6}$$

The input power flowing into the rectifier is expressed by

$$P_{\mathrm{IN,REC}} = 2f_P C_P (V_{\mathrm{REC}} + 2V_D)(2V_{\mathrm{OC}} - V_L). \tag{7}$$

While the ideal rectifier output power transferred to the rectified capacitor C_{REC} is

$$P_{\mathrm{OUT,REC}} = 2f_P C_P V_{\mathrm{REC}}(2V_{\mathrm{OC}} - V_L). \tag{8}$$

Therefore, the ac-to-dc PCE of a conventional bias-flip rectifier, noted as η_{REC}, can be expressed as

$$\begin{aligned} \eta_{\mathrm{REC}} &= \frac{P_{\mathrm{OUT,REC}}}{P_{\mathrm{IN,REC}}} \\ &= \frac{2f_P C_P V_{\mathrm{REC}}(2V_{\mathrm{OC}} - V_L)}{2f_P C_P (V_{\mathrm{REC}} + 2V_D)(2V_{\mathrm{OC}} - V_L)} \\ &= \frac{V_{\mathrm{REC}}}{V_{\mathrm{REC}} + 2V_D}. \end{aligned} \tag{9}$$

In the second stage, the charge stored in C_{REC} is transferred to BAT using a typical buck-boost dc–dc converter. In the third stage, the energy stored in BAT is transferred to a regulated output capacitor, C_{OUT}, through another buck-boost dc–dc converter. The PCE of a buck-boost converter depends on many factors, including the voltage conversion ratio (VCR), loop resistance, switching frequency, inductors, and so on. For most

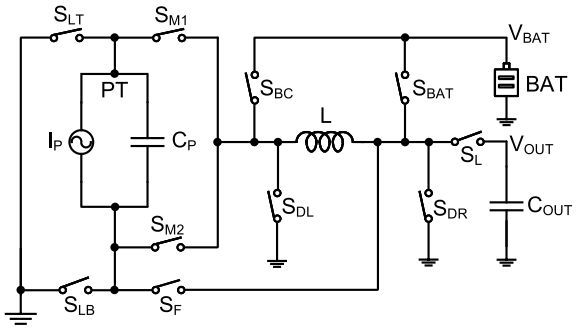


Fig. 3. Power-stage topology of the proposed BMRR.

well-designed inductor-based CMOS buck-boost converters, the PCE is usually between 90% and 95%. To simplify our calculations and focus only on the PCE of the system level, it is assumed that the two buck-boost converters in the second and third stages in Fig. 1(c) have the same efficiency, noted as η_{DCDC}.

Therefore, the end-to-end (E2E) efficiency ($\eta_{\mathrm{E2E-conv}}$) of a conventional three-stage architecture is given as

$$\begin{aligned}\eta_{\mathrm{E2E-conv}} &= \eta_{\mathrm{REC}} \times \eta_{\mathrm{DCDC}} \times \eta_{\mathrm{DCDC}} \times \eta_{\mathrm{MPPT}} \\ &= \frac{V_{\mathrm{REC}} \times \eta_{\mathrm{DCDC}}^2 \times \eta_{\mathrm{MPPT}}}{V_{\mathrm{REC}} + 2V_D} \end{aligned} \tag{10}$$

where η_{MPPT} is the MPPT efficiency. This efficiency depends on how well the real-time V_{REC} tracks the actual MPP voltage, V_{MPP}, where $V_{\mathrm{MPP}} = (V_{\mathrm{OC}}/(1-\eta_F)) - V_D$ according to [4]. For a well-designed MPPT block making the V_{REC} tracking V_{MPP} very well with a small ripple, η_{MPPT} can be very close to 1. Hence, (10) can be approximated as the following if we assume $\eta_{\mathrm{MPPT}} \approx 1$ while $V_{\mathrm{REC}} = V_{\mathrm{MPP}}$:

$$\eta_{\mathrm{E2E-conv}} \approx \frac{V_{\mathrm{MPP}} \times \eta_{\mathrm{DCDC}}^2}{V_{\mathrm{MPP}} + 2V_D}. \tag{11}$$

B. Proposed Single-Stage BMRR

As shown in the conceptual architecture of the proposed BMRR in Fig. 2, which eliminates the FBR, C_{REC}, and cascaded dc–dc conversion losses. The topology of the proposed BMRR is shown in Fig. 3; its operation will be detailed in Section III, while this section is focused on the PCE analysis. The BAT serves as an energy reservoir. The proposed BMRR extracts the energy from the PT to the output capacitor, C_{OUT}, in only one dc–dc conversion stage, without an FBR. Similar to buck-boost converters used in the conventional three-stage system, there are also only two power switches in one conduction path in the BMRR. Hence, the PCE of the dc–dc conversion in the BMRR is at the same level as the PCE of a typical buck-boost converter used in conventional systems, previously noted as η_{DCDC}. Assuming the MPPT efficiency is very close to 1, the E2E PCE of the proposed BMRR is written as

$$\begin{aligned}\eta_{\mathrm{E2E-prop}} &= \eta_{\mathrm{DCDC}} \times \eta_{\mathrm{MPPT}} \\ &\approx \eta_{\mathrm{DCDC}}. \end{aligned} \tag{12}$$

Therefore, based on (11) and (12), a comparison between the E2E PCE of the proposed BMRR and the conventional three-stage system is made and expressed as below

$$\frac{\eta_{\mathrm{E2E-conv}}}{\eta_{\mathrm{E2E-prop}}} = \frac{V_{\mathrm{MPP}} \times \eta_{\mathrm{DCDC}}}{V_{\mathrm{MPP}} + 2V_D}. \tag{13}$$

Since η_{DCDC} is always less than 1, it is evident that the E2E PCE of the proposed BMRR is always higher than that of a conventional three-stage system. The PCE difference can be significant if V_{MPP} is low, such that a considerable amount of energy is wasted in the diodes due to V_D in a conventional three-stage system.

III. System Architecture

Fig. 3 shows the power-stage topology of the proposed BMRR, which consists of ten power switches, an inductor, an output capacitor C_{OUT}, and an energy reservoir (BAT). The PT voltage flipping and energy transfer phases are controlled by the corresponding operating modes of these switches, as illustrated in Fig. 4.

At the zero-crossing moment of I_P, V_{PT} is flipped by the inductor in mode (a) by closing S_{M1} and S_F in Fig. 4. The power transfer involves two cases, determined by the relationship between the PT-generated power (P_{PT}) and load-consumed power (P_{LOAD}). When $P_{\mathrm{PT}} \leq P_{\mathrm{LOAD}}$, C_{OUT} can be charged directly by the PT in modes (b) or (c), depending on PT polarity. Each mode of (b) and (c) includes two subphases. The red path is to energize the inductor, where the energy is dumped from PT to the inductor. In the second step (blue path), the energy is discharged from the inductor to the output capacitor C_{OUT}.

When $P_{\mathrm{PT}} > P_{\mathrm{LOAD}}$, part of the PT-generated energy goes into BAT in modes (d) and (e), depending on the PT polarity, to regulate V_{OUT}. Every mode involves two steps operated in a red path (inductor-charging) and followed by a blue path (inductor-discharging). If the PT-generated power is insufficient to power the load-consumed power, the stored energy in BAT will also be used to charge the output capacitor C_{OUT} to regulate V_{OUT} in mode (f).

Fig. 5 compares the PT waveform (V_{PT}) between a conventional work (top) and the proposed BMRR (bottom). In conventional works, V_{PT} is gradually converged to the optimum voltage (V_{MPP}), corresponding to the MPP by a DCB MPPT technique in [13]. The DCB MPPT points out the relationship between the MPPT efficiency (η_{MPPT}) and the rectifier's cut-off duty cycle (D_{CO}) in a half-vibration period, where the MPPT efficiency refers to the current output power (P_{OUT}) over the maximum output power (P_{Max}), ($\eta_{\mathrm{MPPT}} = (P_{\mathrm{OUT}}/P_{\mathrm{Max}})$). The relationship between the MPPT efficiency (η_{MPPT}) and the rectifier's cut-off duty cycle can be expressed by $\eta_{\mathrm{MPPT}} = 1 - \cos^2(\pi \times D_{\mathrm{CO}})$. The MPP can be tracked by regulating D_{CO} at 50%, corresponding to V_{PT} regulated at V_{MPP}.

The DCB MPPT in [13] necessitates the use of a rectified capacitor (C_{REC}) to track output power variations and maintain it at the MPP. Unfortunately, C_{REC} is typically at the microfarad level, resulting in prolonged startup times, as depicted in Fig. 5 (top left). When V_{REC} is low, the rectifier's cut-off duty cycle is small and gradually converges to 50% over an extended startup period along with the increase of V_{REC}. When

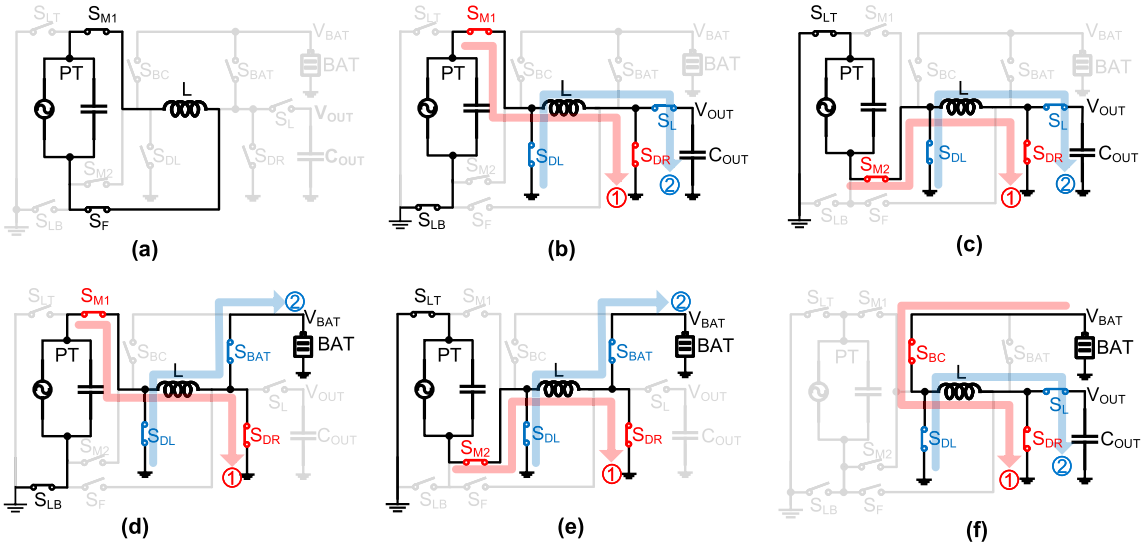


Fig. 4. Operation modes and current flowing paths of the proposed BMRR. (a) V_{PT} flipping. (b) $V_{PT} > 0$, energy: PT $\rightarrow$ C_{OUT}. (c) $V_{PT} < 0$, energy: PT $\rightarrow$ C_{OUT}. (d) $V_{PT} > 0$, energy: PT $\rightarrow$ BAT. (e) $V_{PT} < 0$, energy: PT $\rightarrow$ BAT. (f) Energy: BAT $\rightarrow$ C_{OUT}.

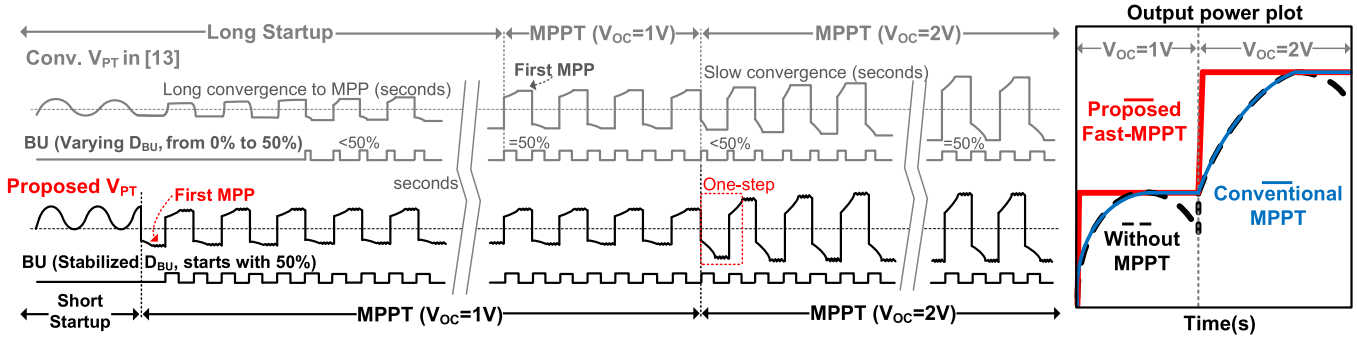


Fig. 5. PT voltage (V_{PT}) of a conventional bias-flip rectifier and the proposed BMRR (left); output power of the proposed BMRR, conventional SSHI with MPPT, and conventional SSHI with no MPPT (right).

external excitation level changes, such as the open-circuit voltage V_{OC} increasing from 1 to 2 V, the duty cycle becomes smaller than 50% since V_{REC} is still at the previous V_{MPP} corresponding to $V_{OC} = 1$ V. A considerable time is needed to charge V_{REC} to the new V_{MPP}.

To achieve short startup and fast convergence under variable excitation, this design proposes a stabilized DCB MPPT technique, which temporarily puts the PT in an open circuit to let V_{PT} directly climb to the MPP within half vibration period, rather than waiting many periods in conventional DCB designs. The V_{PT} waveform of the proposed BMRR is shown in Fig. 5 (bottom). The capacitor C_{REC} is removed from the proposed BMRR, guaranteeing a fast MPPT convergence. The proposed system starts by directly regulating the duty cycle of the PT voltage build-up (BU) time to a fixed value of 50%, indicating that the first MPP is achieved from the beginning and the system always works at MPP. Even if the external excitation abruptly changes from 1 to 2 V, the proposed rectifier shows a very fast response and works at the new MPP in the next half period.

Correspondingly, the output power plot versus time is shown on the right. Without MPPT, the output power rises to the top and goes down. The plot of the conventional MPPT technique tracks the MPP along with the power plot "No MPPT" and then keeps the power at MPP. However, the proposed BMRR quickly forces the output power to the MPP, which does not require tracking the naturally varying output power.

Fig. 6 shows the system architecture of the proposed BMRR, which consists of a power stage with ten power switches described earlier, a bias-flip rectification control block, a fully digital fast-MPPT block, a V_{OUT} regulation block, a startup block, switch control blocks, and level shifters. During startup, to find 50% V_{PT} BU duty cycle (D_{BU}) for MPP, the vibration period (T_0) is sampled first. V_P is connected to a comparator, with V_N connected to the ground, to calculate the vibration period during the startup time (T_0) with a digital counter. After finding T_0, the first flipping moment of V_{PT} can be determined at $T_0/2$ in the next period. After flipping, the MPPT block allows V_{PT} to build up for another $T_0/4$ (corresponding to $D_{BU} = 50\%$) to climb to its first MPP voltage.

When V_{PT} reaches the MPP, the MPP voltage V_{MPP} is sampled, and V_{PT} starts being regulated at this voltage. As V_{PT} starts moving away from the MPP (C_P started being discharged), the BU signal, BU, goes high, indicating that V_{PT} needs to be flipped and build up again in an opposite polarity

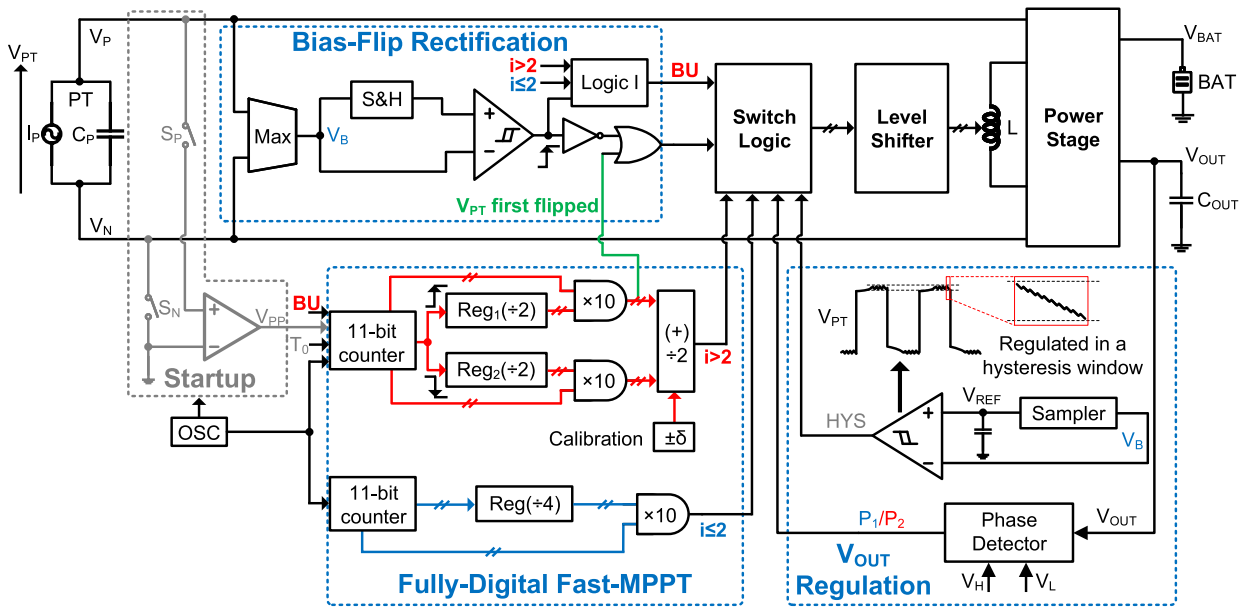


Fig. 6. System architecture of the proposed single-stage BMRR.

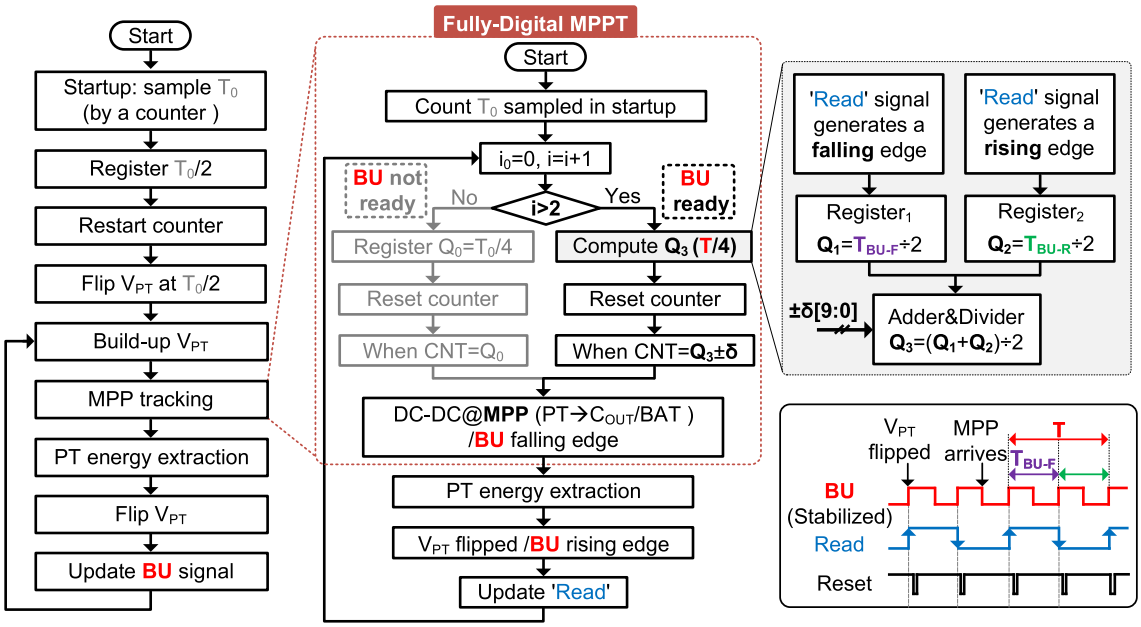


Fig. 7. Operation flowchart of the proposed system.

toward the next MPP. After another $T_0/4$, BU goes low, and V_{PT} reaches the MPP again. To maintain efficient MPPT, a new vibration period (T) is digitally sampled and updated at every rising edge of BU. The periodically refreshed T is used to find $T/4$ to determine the next BU time of V_{PT} (or ON time of the BU signal) to let it build up directly to the MPP after it is flipped. The reason for letting V_{PT} build-up for exactly $T/4$ is based on the $D_{BU} = 50\%$ rule of the DCB MPPT algorithm [13]. Since BU is only available after the first flipping, the $T/4$ time for the first two MPPs is calculated from T_0. From the third MPP, a real-time T is measured for each vibration period and refreshed at each rising edge of BU.

The V_{OUT} regulation block uses a hysteresis window, set by V_H and V_L, to regulate V_{OUT}. There are three modes to charge C_{OUT}: modes (b)–(d). A phase detector decides which mode to use and generates control signals, depending on the power level and PT polarity. Finally, digital signals generated by the bias-flip rectification, MPPT, and V_{OUT} regulation blocks are fed into the switch logic block to drive the power stage after level shifters.

The system flowchart is shown in Fig. 7. The left flowchart illustrates the system-level operations. The system commences with sampling the vibration period, followed by three subsequent steps: PT voltage bias-flipping, MPPT, and energy

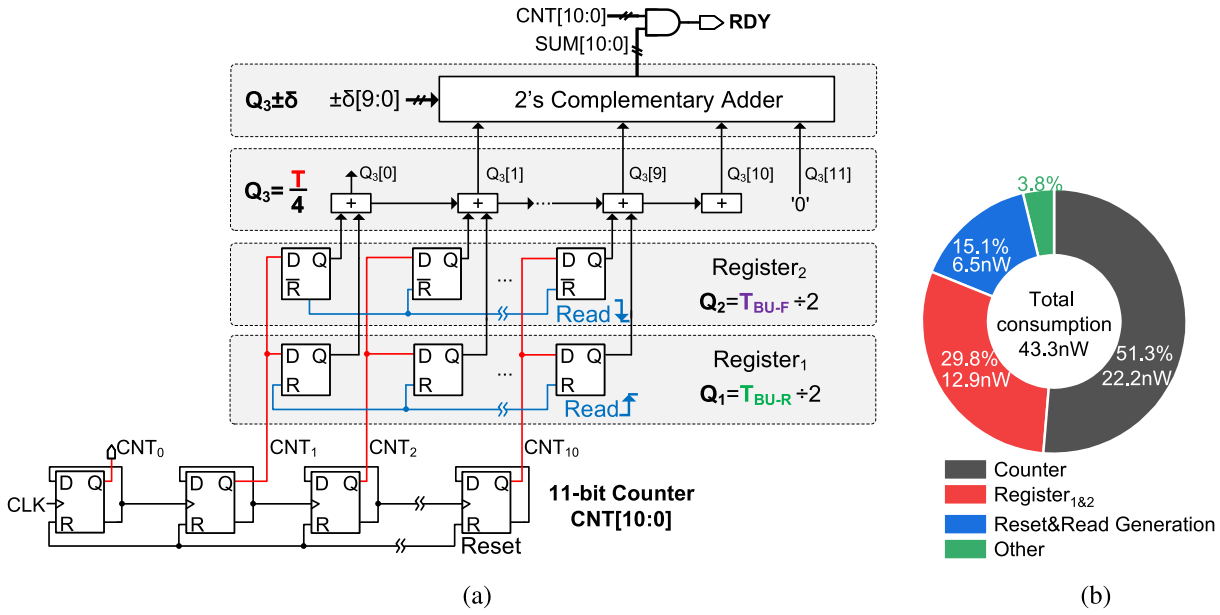


Fig. 8. Fully digital MPPT of the proposed stabilized DCB MPPT technique. (a) Fully digital MPPT circuit implementation. (b) MPPT block power consumption.

extraction. The detailed MPPT operations are shown in the middle, where the first two MPPs are found through the left path when the BU signal is not ready. Upon reaching a steady state, the MPP is tracked via the right path when BU is ready. Fig. 7 (right) shows the procedure for determining the 50% duty cycle, as referenced in Fig. 6. The bottom right shows the waveform of the BU, Read, and Reset signals. In the steady operations, the rising edge of BU corresponds to the PT voltage flipping moment, while its falling edge signifies the arrival of the MPP.

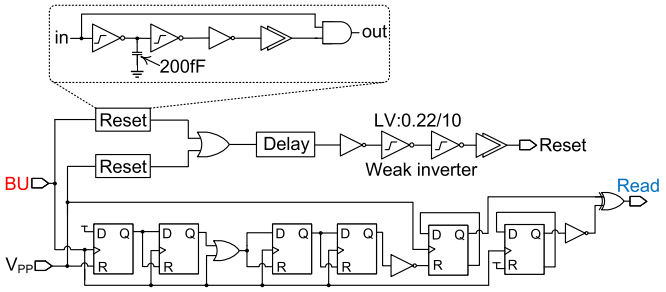


Fig. 9. Digital MPPT control block for generating Reset and Read signals.

IV. Circuit Implementation

Fig. 8(a) shows the circuit implementation of the fully digital MPPT to find $T/4$ as the BU time of V_{PT} to achieve $D_{BU} = 50\%$. To determine $T/4$ first, an 11-bit counter CNT[10:0] continuously counts the clock (CLK) cycles within each BU period. The counter is driven by an on-chip generated clock of 50 kHz. The counter is reset at every BU rising edge, and its 1-bit-right-shifted (halved) output is alternatively stored in two registers, Q_1 and Q_2. Then, Q_1 and Q_2 are averaged to obtain $T/4$. The averaging operation of two adjacent BU periods, stored in Q_1 and Q_2, is to remove the error between them and obtain an accurate $T/4$. The final $T/4$ can be externally adjusted by a 10-bit signal δ[9:0] (in the range of $[-512, 511]$) through a 2's complementary adder to manually stabilize D_{BU} in a wide range from 15% to 75%. This calibration ability allows the system performance to be measured when it works in non-MPP conditions. By employing a fully digital MPPT technique, the whole MPPT block consumes only 43.3 nW as shown in Fig. 8(b), where the counter occupies the largest proportion.

Fig. 9 shows the circuit implementation responsible for generating the counter control signals featured in Fig. 8. This configuration directs the V_{PP} and BU signals into the reset block and D-flip-flops, where V_{PP} is the result of comparing V_P and V_N during the startup state shown in Fig. 6. These components collaborate to yield the final Reset and Read signals, pivotal for regulating the counter operation outlined in Fig. 8. The Read signal undergoes updates upon the occurrence of a rising edge in the BU signal. Conversely, after reading the registered clocks, the Reset signal is triggered. The reset block's specifications are outlined at the top of the diagram. The weak inverters are characterized by a width-to-length (W/L) ratio of 0.22/10 μm.

Fig. 10 shows the V_{OUT} regulation block, which is crucial in determining the energy flow directions in the system. The logic controls, depicted on the left side of the diagram, produce outputs that dictate the energy flow paths of the system. In the switch logic section, the top two paths signify the energy flow from the battery (BAT) to the output capacitor C_{OUT}, while the middle paths represent the energy flow from the PT to the BAT. The bottom paths depict the energy transfer from the PT to C_{OUT}. After passing through the level shifters, the output signals drive the switches in the power stage.

The input signals, P_1 and P_2, indicate whether V_{OUT} reaches its hysteresis lower boundary, V_L, or higher boundary,

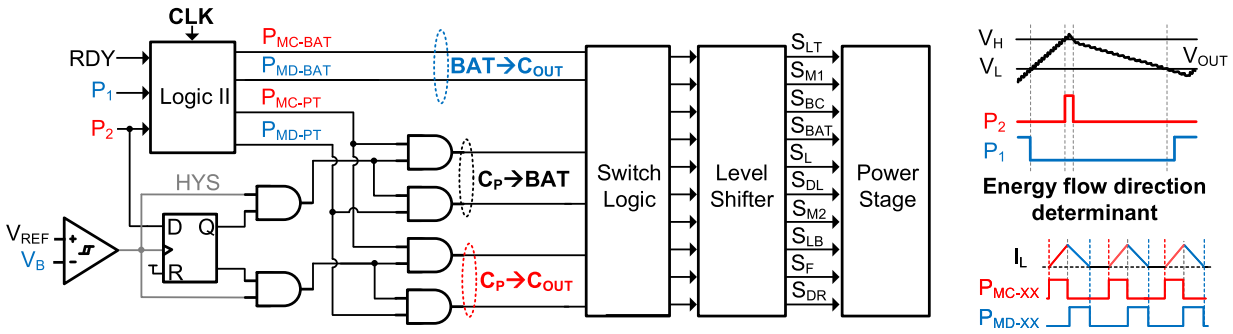


Fig. 10. Output regulation block of the proposed single-stage rectifier.

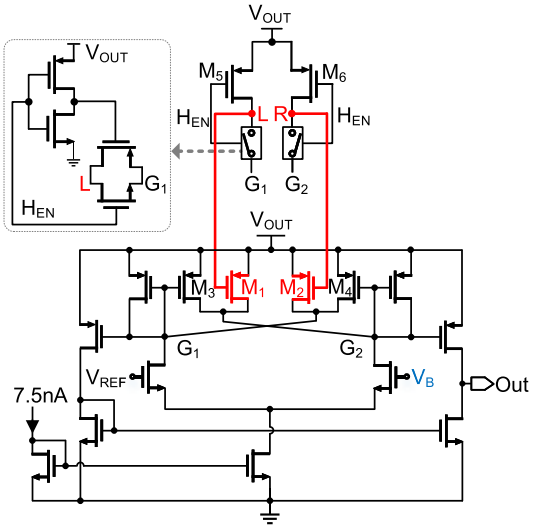


Fig. 11. Hysteresis comparator for PT voltage regulation.

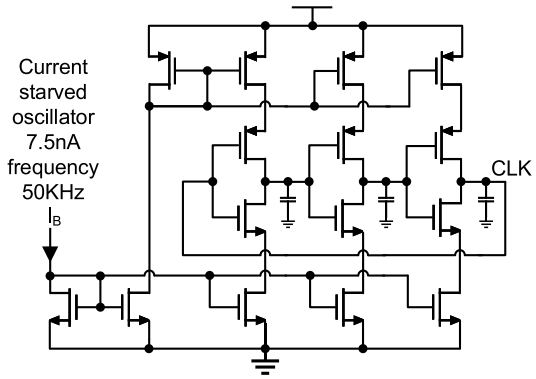
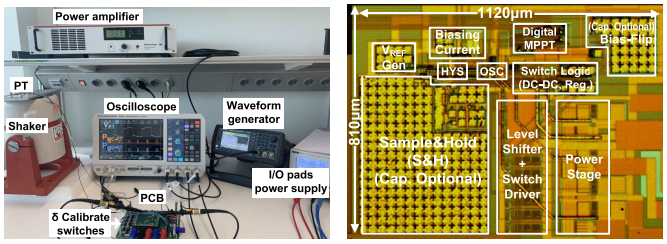


Fig. 12. On-chip oscillator for generating a 50-kHz clock.



(a) (b)

Fig. 13. Experimental setup and chip microphotograph. (a) Measurement setup. (b) Chip micrograph.

V_H, respectively. When P_2 is high, V_{OUT} does not need to be charged, and the PT energy goes into BAT; otherwise, PT-generated energy is transferred into C_{OUT}. When P_1 is high, it indicates that PT-harvested power is too low to sustain the load, so BAT is engaged to charge V_{OUT} until it reaches V_H. The HYS signal generated by a hysteresis comparator in Fig. 11 assists in determining where the PT-generated energy flows. The signals P_1, P_2, and RDY are used to generate inductor-charging phases, P_{MC-XX} (either P_{MC-PT} or P_{MC-BAT}), and inductor-discharging phases P_{MD-XX} (either P_{MD-PT} or P_{MD-BAT}), to drive the switch matrix for power transfer operations. The RDY signal indicates whether the MPP arrives.

Fig. 11 presents the detailed circuits of the hysteresis comparator, which is crucial in regulating the PT voltage. The ratio between the widths of transistors (M_1 and M_2) and (M_3 and M_4) determines the hysteresis window. The PMOS pair (M_5 and M_6) at the top serves to calibrate the ratio in a wide range. When H_{EN} is high, M_5 and M_6 are OFF, resulting in a smaller window. Otherwise, M_5 and M_6 are connected in series with M_1 and M_2, respectively, leading to a larger window. Fig. 12 shows a current-starved on-chip oscillator. Its output, CLK, of 50 kHz is provided to the counters to count the vibration period and determine the MPP. The biasing current is 7.5 nA, and the total consumed power is around 67.5 nW.

V. Measurement Results

Fig. 13 shows the measurement setup and chip micrograph. The chip was fabricated in a 180-nm BCD process. The active chip area is 0.91 mm^2. Two commercial PTs are used in the measurements to validate the operations of the proposed system better. The two PTs are S129-H5FR-1803YB and S128-J1FR-1808YB, with inherent capacitors 23 and 116 nF, and the resonance frequencies of 133 and 120 Hz, respectively. The employed BAT is SEIKO MS621FE with a voltage range between 3 and 3.5 V.

Fig. 14 shows the waveform of V_{PT} and V_{PP} in the very first several vibration periods after excitation starts. Initially, the vibration period T_0 is examined for the first several free oscillations of V_{PT}. After T_0 is sampled and determined, the first flipping moment of the PT voltage occurs after $T_0/2$ in the following period. After another $T_0/4$ period, the MPP arrives, and dc–dc conversion starts operating to regulate the

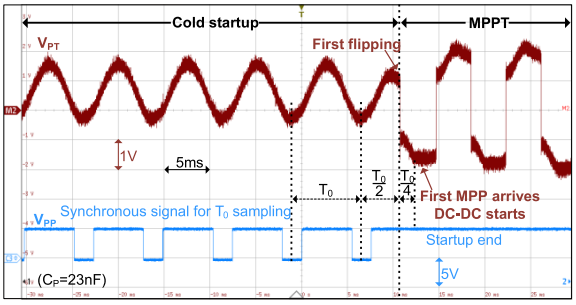


Fig. 14. Measured PT voltage waveform during startup.

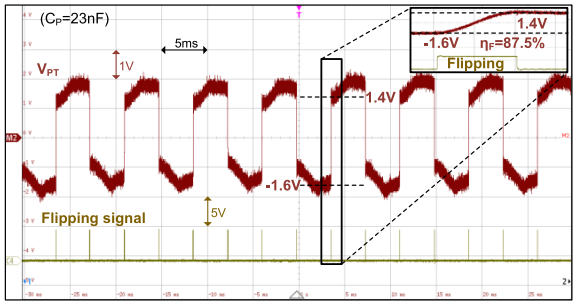


Fig. 15. Measured PT voltage waveform during the steady state.

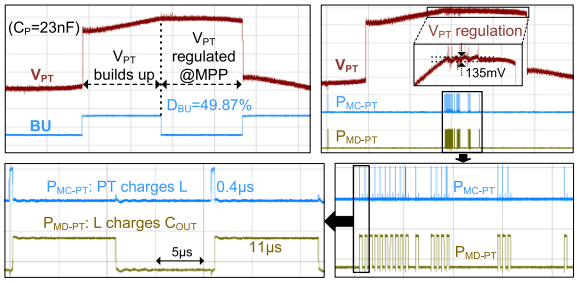


Fig. 16. Zoom-in waveform of the PT voltage and related control phases.

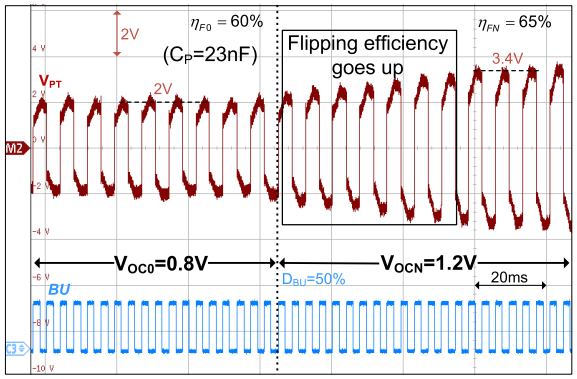


Fig. 17. System transient waveform of the PT voltage and BU signals under different external excitation levels.

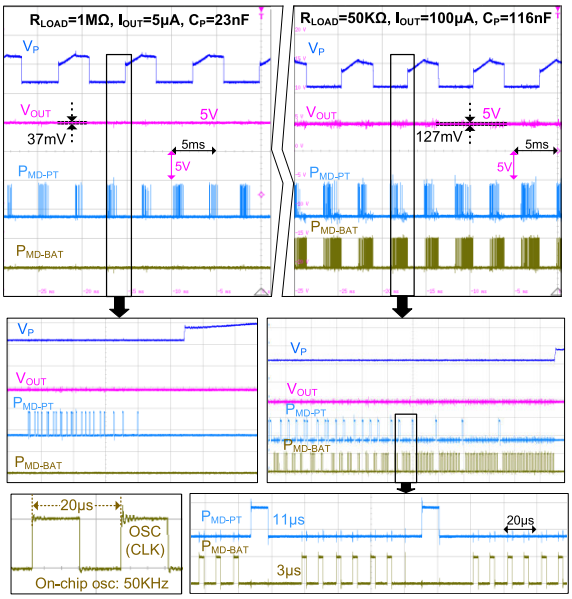


Fig. 18. Measured V_{OUT} regulation in different loading conditions.

PT voltage, indicating the finishing of the startup period. As shown in Fig. 14, the startup period consists of only five vibration periods. This period could potentially be optimized to as few as two periods. Once the startup period is complete, the system transitions into a stable operating state, maintaining V_{PT} regulation and bias-flipping.

Fig. 15 shows the PT voltage, V_{PT}, and the flipping signal during the steady state. The zoomed-in figure at the top-right displays the behavior of the PT voltage during a flipping moment. During this time, the PT voltage is flipped from −1.6 to 1.4 V, representing an 87.5% voltage flipping efficiency.

Fig. 16 provides a detailed view of the PT voltage during both the BU and regulation periods. The waveform shows a measured BU duty cycle, D_{BU}, of approximately 49.87%. Fig. 16 (right) shows the control phases, P_{MC-PT} and P_{MD-PT}. P_{MC-PT} represents the phase during which the charge is transferred from the PT to energize the inductor, while P_{MD-PT} shows the inductor-discharging phase.

Fig. 17 shows the waveform of PT voltage V_{PT} and BU. The proposed system was designed to achieve MPPT in response to changes in external excitation levels. Initially, the open-circuit voltage (V_{OC}) of the PT is 0.8 V and the flipping efficiency is 60%, corresponding to an MPP voltage V_{MPP} of around 2 V. When V_{OC} increases to 1.2 V, the flipping efficiency rises to 65% in the steady state since the higher gate-driving voltage reduces the switch resistance in the bias-flip loop. It can be observed that the duty cycle of BU is anchored to 50% to automatically regulate V_{PT} toward the new V_{MPP} of around 3.4 V.

Fig. 18 shows the waveform of V_P, V_{OUT}, P_{MD-PT}, and P_{MD-BAT} under different load conditions. P_{MD-PT} and P_{MD-BAT} represent the inductor-discharging phases from the PT and the BAT, respectively. Fig. 18 (left) shows that when the load resistance is 1 MΩ, the system maintains an output voltage of 5 V with a small ripple of 37 mV and a load current of 5 μA. In contrast, Fig. 18 (right) shows the waveform in a heavier load condition with a load resistance of 50 kΩ, which results in a larger maximum output voltage ripple of 127 mV. The zoomed-in waveform on the bottom reveals that P_{MD-PT} and P_{MD-BAT} lasts 11 and 3 μs, respectively. The output of the on-chip 50-kHz oscillator is shown at the bottom left.

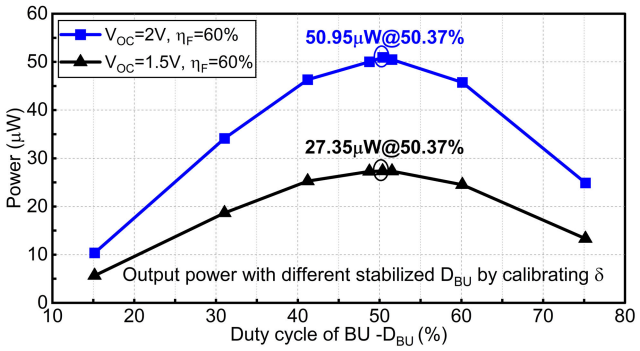


Fig. 19. Output power versus D_{BU} for different voltages V_{OC}.

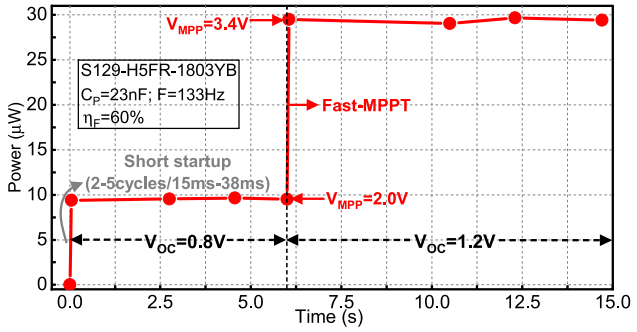


Fig. 20. Output power versus the time with increasing V_{OC}.

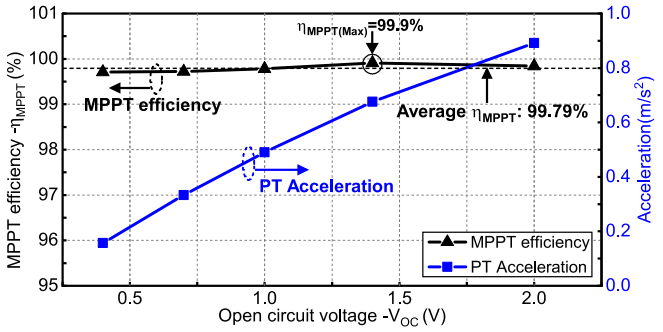


Fig. 21. MPPT efficiency and excitation acceleration levels over V_{OC}.

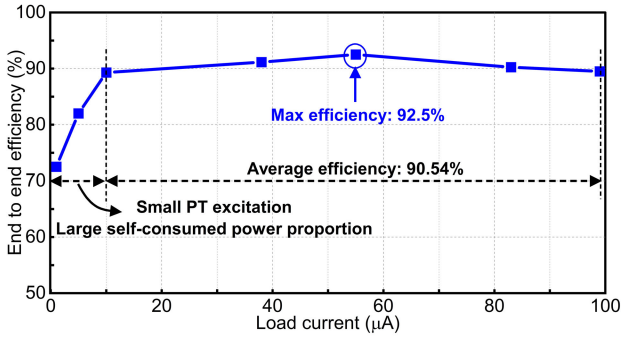


Fig. 22. E2E efficiency with different load currents.

Fig. 19 presents the relationship between output power and the BU signal duty cycle, D_{BU}, for the proposed BMRR under different open-circuit voltages V_{OC}. Fig. 19 aims to determine the optimum duty cycle for maximum power output, with V_{OC} at 1.5 and 2 V, both exhibiting the same voltage flipping efficiency of 60%. This data was acquired by manually configuring the external signal δ[9:0] to stabilize D_{BU} at a specific value in a broad range from 15% to 75%, as detailed in Fig. 8. The results prove that for different V_{OC} values, the optimum D_{BU} for achieving maximum output power is around 50%, which matches the theory of the DCB MPPT algorithm.

Fig. 20 shows the output power of the proposed BMRR over 15 s of time starting from a static PT with V_{OC} changed in the middle, similar to the phenomenon shown in Fig. 17. The measurements demonstrate the effectiveness of the fast-MPPT technique. Initially, following the startup phase, the output power swiftly rises to 10 μW within a timeframe of 15–38 ms (2–5 vibration periods). This rapid increase is attributed to the implementation of the proposed fast-MPPT technique. Subsequently, when the open-circuit voltage transitions from 0.8 to 1.2 V, the output power undergoes a significant surge from 10 to 30 μW rapidly. This rapid power increase underscores the responsiveness and efficiency of the BMRR rectifier in adapting to changes in the external environment, thereby maximizing power extraction from the energy source.

Fig. 21 exhibits the measured MPPT efficiency and acceleration level as a function of the open-circuit voltage V_{OC}. The data reveals remarkable efficiency metrics, with a maximum MPPT efficiency reaching an impressive 99.9%, while the average MPPT efficiency stands at 99.79% in a wide range of V_{OC} from 0.4 to 2 V. These results underscore the efficacy of the fully digital MPPT design. The chip leverages a 180-nm BCD process featuring CMOS transistors with a maximum rating of 5 V. The acceleration measurements complement these efficiency figures, with the minimum acceleration level at 0.2 m/s^2 corresponding to V_{OC} of 0.4 V, and the maximum acceleration measured at 0.9 m/s^2 corresponding to V_{OC} of 2.0 V. Such performance metrics highlight the robustness and versatility of the chip design in adapting to varying operating conditions while consistently achieving high levels of efficiency.

Fig. 22 provides the measured E2E efficiency of the proposed BMRR for various load currents. Notably, the measurements indicate a peak E2E efficiency of 92.5% with the load current at 55 μA. The system achieves an average efficiency of 90.54% in a wide range of load current from 10 to 100 μA. The E2E efficiency tends to be relatively low at lower load current due to a relatively higher proportion of self-consumed power. These results underscore the efficacy of the proposed single-stage BMRR in achieving high E2E efficiency from the energy harvester to the load.

Fig. 23 depicts the figure of merit (FOM) concerning flipping efficiency, where the FOM is defined as the ratio of the extracted power with the proposed BMRR to that of an FBR. With flipping efficiency ranging from 60% to 87.5% by changing the off-chip inductance, the FOM exhibits corresponding variations from 5× to 9.3×. Therefore, the BMRR achieves the energy extraction enhancement of up to 9.3× compared to an FBR.

Table I provides performance comparisons between the proposed BMRR and prior works. Unlike most previous

TABLE I
PERFORMANCE COMPARISON WITH PRIOR WORKS

	JSSC'17 [25]	ISSCC'20 [28]	AICSP'22 [29]	ISSCC'22 [30]	JSSC'23 [21]	JSSC'23 [10]	**This work**
Technology	350 nm	600 nm	180 nm	180 nm	180 nm	180 nm	180 nm
Energy	Electromagnetic	Piezoelectric	Piezoelectric	Triboelectric	Piezoelectric	Piezoelectric	**Piezoelectric**
Frequency	64.4Hz/109Hz	56Hz	120Hz	250Hz	130Hz	230Hz	**133Hz/120Hz**
C_P	No	24nF	15nF	120pF	100nF	42nF	**23nF/116nF**
Technique	NVC	SECE	Recycling SL	MCS-BF	ES-SSHI	SSHI	**BMRR**
Dimension	1.3 mm^2	14 mm^2	0.275 mm^2	5.9 mm^2	1.21 mm^2	0.47 mm^2	**0.91mm^2**
η_F	No	No	70%*	69%	91%/84%	82%	**87.5%**
Inductor	No	220 µH	100 µH	10mH	10 µH	120H	220 µH
FBR Required?	Yes	Yes	No	Yes	No	Yes	**No**
Cold Start?	Yes(5 s)	Yes(4 s)	No	N/R	No	No	**Yes(15ms)**
C_{REC} Existed?	Yes	No	No	Yes	Yes	Yes	**No**
MPPT	CAC	P&O	No	No	No	DCB	**Stabilized DCB**
MPPT Circuit	Analog	Analog&Digital	N/R	N/R	N/R	Analog	**Digital**
MPPT Eff.	91%	N/R	N/R	N/R	N/R	98%	**99.9%**
Reg. V_{OUT}	2.2V	No	No	No	No	No	**5V**
Features	Rec.+MPPT+Reg.	Rec.+MPPT	Rec.	Rec.	Rec.	Rec.+MPPT	**Rec.+MPPT+Reg.**
Cascaded No.	3	2 (No Reg.)	1 (Rec. only)	1 (Rec. only)	1 (Rec. only)	2 (No Reg.)	**1**
E2E PCE	90%	94%(No Reg.)	76%(Rec. only)	70.7%(Rec. only)	N/R	N/R	**92.5%(Overall)**
FOM (P_{IC}/P_{FBR})	1×	3.28×	2.5×−12×	3.14×	11.7×−6.4×	7.38×	**9.3×**

*: Estimated. N/R: Not reported.

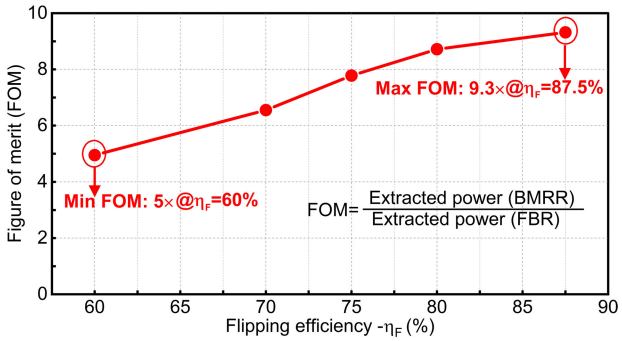


Fig. 23. Power extraction enhancement compared to an FBR.

approaches focusing on improving the performance of either the rectifier stage or the MPPT stage, the BMRR is focused on global optimization to achieve high E2E efficiency by integrating bias-flip rectification, MPPT, and output regulation in only one stage. Its MPPT algorithm, based on stabilized DCB, achieves one-step MPPT. Measured results show a maximum output E2E efficiency of 92.5% and power extraction enhancement of 9.3× compared to an FBR with near-zero diode voltage drop, highlighting its superior performance in PEH systems.

VI. CONCLUSION

This article proposes a single-stage BMRR for PEH. The proposed system integrates bias-flip rectification, MPPT, and output regulation in only one stage, eliminating intermediate stages and minimizing energy loss. The proposed fully digital MPPT technique is based on a stabilized 50% DCB method, which ensures that MPPT is achieved shortly after the system starts operating, typically within several vibration cycles. The proposed architecture removes the conventional rectified capacitor, guaranteeing a one-step MPPT and short startup. Thanks to the single-stage BMRR, the energy extraction performance is enhanced by 9.3× compared to an FBR, and a 92.5% E2E efficiency is achieved.

REFERENCES

[1] Y. K. Ramadass and A. P. Chandrakasan, "An efficient piezoelectric energy harvesting interface circuit using a bias-flip rectifier and shared inductor," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 189–204, Jan. 2010.

[2] D. A. Sanchez, J. Leicht, E. Jodka, E. Fazel, and Y. Manoli, "A 4μw-to-1mw parallel-sshi rectifier for piezoelectric energy harvesting of periodic and shock excitations with inductor sharing, cold start-up and up to 681% power extraction improvement," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jul. 2016, pp. 366–367.

[3] Z. Chen, M.-K. Law, P.-I. Mak, W.-H. Ki, and R. P. Martins, "Fully integrated inductor-less flipping-capacitor rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3168–3180, Dec. 2017.

[4] S. Du, Y. Jia, C. Zhao, G. A. J. Amaratunga, and A. A. Seshia, "A fully integrated split-electrode SSHC rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1733–1743, Jun. 2019.

[5] X. Yue and S. Du, "A synchronized switch harvesting rectifier with reusable storage capacitors for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 58, no. 9, pp. 2597–2606, Sep. 2023.

[6] M. Shim, J. Kim, J. Jeong, S. Park, and C. Kim, "Self-powered 30μW to 10 mW piezoelectric energy harvesting system with 9.09 ms/V maximum power point tracking time," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2367–2379, Oct. 2015.

[7] X. Wang et al., "Configurable hybrid energy synchronous extraction interface with serial stack resonance for multi-source energy harvesting," *IEEE J. Solid-State Circuits*, vol. 58, no. 2, pp. 451–461, Feb. 2023.

[8] D. Maurath, P. F. Becker, D. Spreemann, and Y. Manoli, "Efficient energy harvesting with electromagnetic energy transducers using active low-voltage rectification and maximum power point tracking," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1369–1380, Jun. 2012.

[9] K.-S. Yoon, S.-W. Hong, and G.-H. Cho, "Double pile-up resonance energy harvesting circuit for piezoelectric and thermoelectric materials," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1049–1060, Apr. 2018.

[10] X. Yue, S. Javvaji, Z. Tang, K. A. A. Makinwa, and S. Du, "A bias-flip rectifier with duty-cycle-based mppt for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 59, no. 6, pp. 1771–1781, Jun. 2024.

[11] E. E. Aktakka and K. Najafi, "A micro inertial energy harvesting platform with self-supplied power management circuit for autonomous wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 49, no. 9, pp. 2017–2029, Sep. 2014.

[12] Z. Chen, M.-K. Law, P.-I. Mak, X. Zeng, and R. P. Martins, "Piezoelectric energy-harvesting interface using split-phase flipping-capacitor rectifier with capacitor reuse for input power adaptation," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2106–2117, Aug. 2020.

[13] X. Yue, S. Javvaji, Z. Tang, K. A. A. Makinwa, and S. Du, "A bias-flip rectifier with a duty-cycle-based MPPT algorithm for piezoelectric energy harvesting with 98% peak MPPT efficiency and 738% energy-extraction enhancement," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 442–444.

[14] N. J. Guilar, R. Amirtharajah, and P. J. Hurst, "A full-wave rectifier with integrated peak selection for multiple electrode piezoelectric energy harvesters," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 240–246, Jan. 2009.

[15] S. Javvaji, V. Singhal, V. Menezes, R. Chauhan, and S. Pavan, "Analysis and design of a multi-step bias-flip rectifier for piezoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2590–2600, Sep. 2019.

[16] X. Yue and S. Du, "Voltage flip efficiency optimization of SSHC rectifiers for piezoelectric energy harvesting," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2021, pp. 1–5.

[17] A. Morel et al., "Fast-convergence self-adjusting SECE circuit with tunable short-circuit duration exhibiting 368% bandwidth improvement," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 222–225, 2020.

[18] D. A. Sanchez, J. Leicht, F. Hagedorn, E. Jodka, E. Fazel, and Y. Manoli, "A parallel-SSHI rectifier for piezoelectric energy harvesting of periodic and shock excitations," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2867–2879, Dec. 2016.

[19] S. Sankar, P.-H. Chen, and M. S. Baghini, "An efficient inductive rectifier based piezo-energy harvesting using recursive pre-charge and accumulation operation," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2404–2417, Aug. 2022.

[20] X. Yue, J. Mo, Z. Chen, S. Vollebregt, G. Zhang, and S. Du, "A fully integrated sequential synchronized switch harvesting on capacitors rectifier based on split- electrode for piezoelectric energy harvesting," *IEEE Trans. Power Electron.*, vol. 39, no. 6, pp. 7643–7653, Jun. 2024.

[21] Y.-W. Jeong, S.-J. Lee, and S.-U. Shin, "A scalable N-step equally split SSHI rectifier for piezoelectric energy harvesting with low-Q inductor," *IEEE J. Solid-State Circuits*, vol. 58, no. 12, pp. 3519–3529, Dec. 2023.

[22] S. Li, A. Roy, and B. H. Calhoun, "A piezoelectric energy-harvesting system with parallel-SSHI rectifier and integrated MPPT achieving 417% energy-extraction improvement and 97% tracking efficiency," in *Proc. Symp. VLSI Circuits*, Jun. 2019, pp. C324–C325.

[23] S. Bandyopadhyay and A. P. Chandrakasan, "Platform architecture for solar, thermal, and vibration energy combining with MPPT and single inductor," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2199–2215, Sep. 2012.

[24] Y. Peng et al., "An efficient piezoelectric energy harvesting interface circuit using a sense-and-set rectifier," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3348–3361, Dec. 2019.

[25] J. Leicht and Y. Manoli, "A 2.6 μW–1.2 mW autonomous electromagnetic vibration energy harvester interface IC with conduction-angle-controlled MPPT and up to 95% efficiency," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2448–2462, Sep. 2017.

[26] X. Yue and S. Du, "A single-stage bias-flip regulating rectifier with fully-digital fast-MPPT for piezoelectric energy harvesting achieving 9.3X power enhancement and 92.5% end-to-end efficiency," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2024, pp. 1–2.

[27] S. Du, Y. Jia, C. Zhao, G. A. J. Amaratunga, and A. A. Seshia, "A nail-size piezoelectric energy harvesting system integrating a MEMS transducer and a CMOS SSHI circuit," *IEEE Sensors J.*, vol. 20, no. 1, pp. 277–285, Jan. 2020.

[28] A. Morel et al., "Self-tunable phase-shifted SECE piezoelectric energy-harvesting IC with a 30nW MPPT achieving 446% energy-bandwidth improvement and 94% efficiency," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 488–490.

[29] S. Yang and G. A. Rincón-Mora, "Recycling piezoelectric switch-inductor charger," *Anal. Integr. Circuits Signal Process.*, vol. 113, no. 3, pp. 403–414, Dec. 2022.

[30] J. Lee, S.-H. Lee, G.-G. Kang, J.-H. Kim, G.-H. Cho, and H.-S. Kim, "A triboelectric energy-harvesting interface with scalable multi-chip-stacked bias-flip and daisy-chained synchronous signaling techniques," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3825–3839, Dec. 2022.

Xinling Yue (Graduate Student Member, IEEE) is currently pursuing the Ph.D. degree in microelectronics with the Electronic Instrumentation Laboratory, Delft University of Technology, Delft, The Netherlands.

She joined the Electronic Instrumentation Laboratory, Delft University of Technology, in December 2020. Her current research interests are energy-efficient power management integrated circuits and systems, which include energy harvesting, rectifiers, dc/dc converters, and maximum power point tracking techniques.

Ms. Yue received the Best Student Paper Award at the 2022 IEEE International Conference on Electronics Circuits and Systems (ICECS), the Student Travel Grant Awards at the 2022 IEEE International Symposium on Circuits and Systems (ISCAS), and the 2023 ISSCC and the 2023–2024 SSCS Predoctoral Achievement Award.

Sijun Du (Senior Member, IEEE) received the B.Eng. degree (Hons.) in electrical engineering from University Pierre and Marie Curie (UPMC), Paris, France, in 2011, the M.Sc. degree (Hons.) in electrical and electronic engineering from Imperial College London, London, U.K., in 2012, and the Ph.D. degree in electrical engineering from the University of Cambridge, Cambridge, U.K., in January 2018.

He was with the Laboratoire d'Informatique de Paris 6 (LIP6), University Pierre and Marie Curie, and then was an IC Engineer in Shanghai, China, from 2012 to 2014. He was a Summer Engineer Intern at Qualcomm Technology Inc., San Diego, CA, USA, in 2016. He was a Post-Doctoral Researcher with the Department of Electrical Engineering and Computer Sciences (EECS), University of California at Berkeley, Berkeley, CA, USA, from 2018 to 2020. In 2020, he joined the Department of Microelectronics, Delft University of Technology (TU Delft), Delft, The Netherlands, as an Assistant Professor. His current research is focused on energy-efficient integrated circuits and systems, including power management integrated circuits (PMIC), energy harvesting, wireless power transfer, and dc/dc converters used in the Internet-of-Things (IoT) wireless sensors, wearable electronics, and biomedical devices.

Dr. Du received the Dutch Research Council (NWO) Talent Program VENI Grant in the 2021 round. He was a co-recipient of the Best Student Paper Award at the IEEE International Conference on Electronics Circuits and Systems (ICECS) 2022. He serves as the IEEE ICECS Subcommittee Chair in 2022 and 2024, has been serving as an IEEE ISSCC Student Research Preview (SRP) Committee Member since 2023, and serves as the IEEE ISCAS Subcommittee Chair in 2025.