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η-ρ Pareto Design of a Balancing Converter for Bipolar DC Grids

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***Abstract*—This article provides the design procedure of a $\pm$350 V series resonant balancing converter for bipolar DC grids. The process creates a η-ρ Pareto front to design a 3 kW converter with natural convection cooling.**

***Index Terms*—DC-DC Converter, Resonant power conversion, DC Grids, Modulation, Zero voltage switching, Soft-switching converters, Pareto Front.**

I. Introduction

Bipolar DC grids offer a range of advantages over their unipolar counterparts, as extensively documented in recent studies [1], [2]. These benefits include but are not limited to, increased power flow capacity, reduced insulation voltage stresses, and the availability of more voltage levels [3]–[5]. Despite these advantages, bipolar DC grids face significant challenges, particularly when different loads are connected across the poles and the neutral. This can lead to an imbalance in the grid, resulting in discrepancies in pole-to-neutral voltages. Such imbalances pose risks of equipment tripping and can instigate unwanted current flow through the neutral conductor, consequently elevating the system's power losses. To mitigate these issues, it's imperative to integrate specialized converters with balancing functions. These converters are critical in maintaining grid stability, ensuring operational reliability, and optimizing performance.

The series resonant balancing converter is a topology that, to date, has received limited detailed exploration in the academic literature. While its application has been noted in fields such as capacitor balancing in multilevel converters [6], [7], its potential for balancing bipolar DC grids remains largely untapped. This topology is particularly appealing for use in bipolar DC power grids due to the small size of its passive components, a benefit arising from its inherent resonant nature. Additionally, the modulation scheme employed in this topology enables zero voltage switching (ZVS) turn-on of all switches across the fully designed load range, a feature that enhances operational efficiency and longevity. Despite these promising aspects, there is a notable gap in the literature regarding this converter's realistic design and comprehensive analysis, especially in the context of bipolar DC grids. Our paper delves into these converters' detailed design and practical implementation to address this gap. Utilizing $\eta - \rho$ Pareto front analysis with real-world components, we highlight the converter's crucial role in effectively managing the unique challenges posed by bipolar DC grids, thereby underscoring its potential as a transformative technology in this domain.

The remainder of this article is systematically organized as follows: Section II offers a concise overview of the converter's operating principles. This includes detailed discussions on the power flow dynamics relative to the switching frequency and the computation of resonant inductor currents critical for ensuring the ZVS turn-on of all switches. Following this, Section III delves into the converter's design methodology. This section comprehensively addresses the selection criteria for the primary components of the converter and elucidates the methodology employed for calculating losses in various components. This foundational knowledge paves the way for constructing the η-ρ Pareto front, showcasing a spectrum of potential converter designs. Subsequently, Section IV presents a detailed analysis of the Pareto front, highlighting all viable design options. The digest culminates with Section V, which not only concludes the article but also sets the stage for the full-length article, offering insights into the broader implications and applications of the research findings.

II. Converter Operation

The operational principles of the converter under discussion are well-established in the literature and have been thoroughly explicated in sources such as [8], [9]. As depicted in Fig. 1, the converter's topology comprises four switches ($\mathrm{S_1}$-$\mathrm{S_4}$), a resonant inductor (L_r), a resonant capacitor (C_r), and two DC link capacitors ($\mathrm{C_1}$ and $\mathrm{C_2}$). The dynamic states of the converter, including the current through L_r and the voltage across C_r, are illustrated in Fig. 1.

In Capacitive Phase Shift (Cap PS) mode, as shown in Fig. 1, the converter facilitates ZVS turn-on across the entire load range. This operational mode is segmented into four distinct switching states: SW1, SW2, SW3, and SW4, as detailed in Fig. 1.

Achieving ZVS turn-on necessitates that the currents at switching moments (t_0 to t_4) are adequate to charge and discharge the output capacitance ($\mathrm{C_{oss}}$) of the switches being

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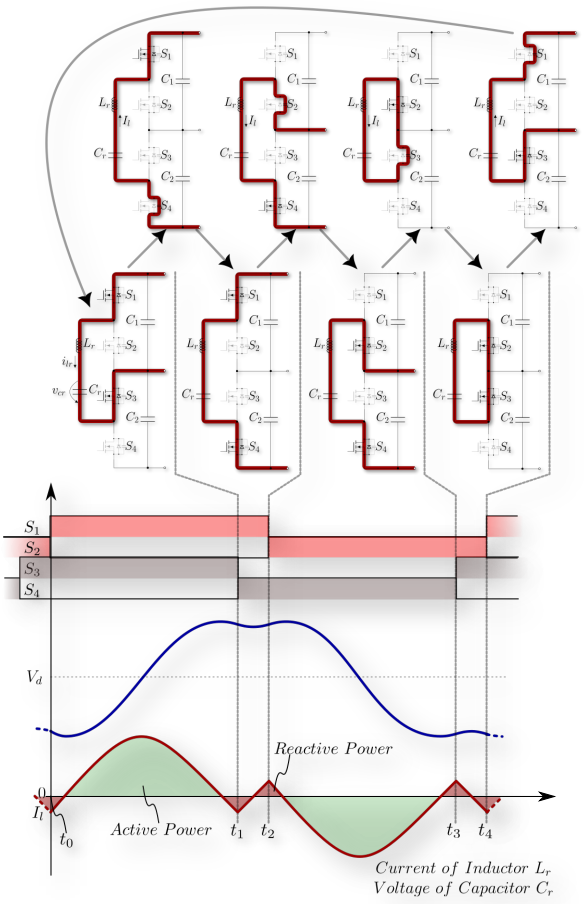

Fig. 1. Illustration of ZVS turn-on of the switches along with the switching states of the converter.

turned off and on, respectively. The minimum current required for ZVS turn-on is expressed as:

$$I_{min,ZVS} = V_d \sqrt{\frac{8}{3}\frac{C_{oss,tr}}{L_r}} \tag{1}$$

where V_d is the pole-to-neutral voltage of the grid, and $C_{oss,tr}$ represents the time-related output capacitance of the switches.

Astute observers will note that both the current waveform and power flow are influenced by the switching frequency and the phase shift between the upper (S_1, S_2) and lower (S_3, S_4) half-bridges. However, it has been demonstrated in [10] that minimizing L_r reduces the dependency of power flow on phase shift. Hence, its power flow can be changed by only manipulating the switching frequency as given by:

$$P_o = 2 f_{sw} C_r V_L \left[\frac{V_L}{2} - \sqrt{\left(\frac{V_L}{2}\right)^2 - I_l^2 Z_0^2} - tan\left(\frac{\omega_0}{4 f_{sw}}\right) I_l V_L Z_0 \right]. \tag{2}$$

Interestingly, for the particular case of soft switching constraints in this application, the maximum power flow is related to the characteristic impedance of the resonant tank. The maximum power flow is calculated with a phase shift that is just enough to achieve the minimum soft switching inductor current. The maximum power flow at that current is approximated by:

$$P_{o,max} \approx \frac{V_d^2}{2\pi Z_0} \tag{3}$$

where Z_0 is the characteristic impedance of the resonant tank.

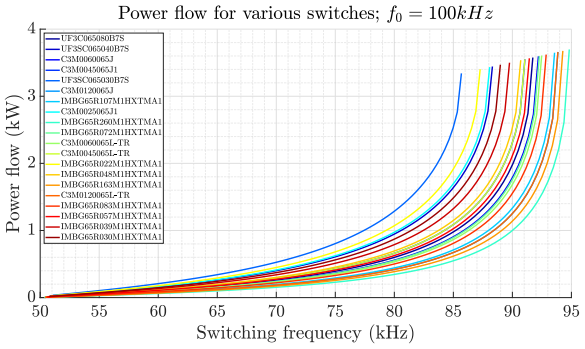

Fig. 2. Variation of power flow concerning switching frequency for various switches at a resonant frequency of 100 kHz.

For the switches used in this study, the power flow relative to the switching frequency is illustrated in Fig. 2. It is important to note that the value of I_{l0} is set as dictated by (1). Due to varying C_{oss} values, the I_{l0} differs for each switch.

III. Converter Design

The procedure for creating a η-ρ (efficiency-density) Pareto front for a converter design is comprehensive and systematic, consisting of two key steps:

1) Component selection methodology: This step involves selecting the major distinct components of the converter, focusing on using real-world components for which volume information is readily available. This approach ensures that the Pareto front is grounded in real-world applicability.
2) Calculation of losses in components: Calculating losses in the converter components is a critical step involving a detailed analysis of various loss mechanisms. This includes the switch conduction losses, which are incurred due to the resistance of the switch when it is in its 'on' state. Additionally, switch turn-off losses are considered, occurring during the transition of the switch from the 'on' state to the 'off' state. Furthermore, the losses in the resonant inductor, both in its core material and copper conductor, are accounted for. Lastly, the resonant capacitor losses of the capacitor used in the resonant circuit are also included in this comprehensive loss analysis.

Each loss component must be quantified to understand its impact on the converter's efficiency and power density. This detailed loss analysis is crucial for accurately positioning each design on the η-ρ Pareto front, providing valuable insights for optimizing converter designs.

A. Semicondutor switches

In this section, the methodology for selecting the switches is given. The calculation of various loss components in the switches follows this.

1) Component selection: Surface-mount device (SMD) type MOSFET switches are employed in pursuit of a compact and aesthetically pleasing design. The half-bridge configuration of the converter, incorporating pairs S_1 & S_2 or S_3 & S_4, is depicted in Fig. 3.

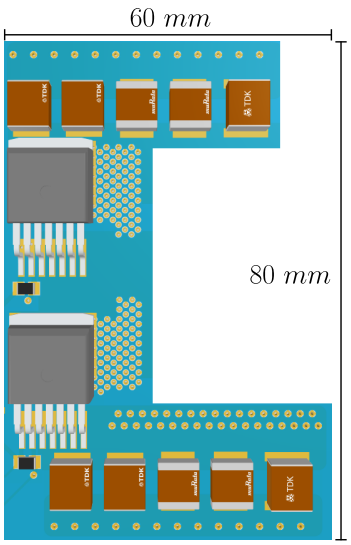

Fig. 3. Half bridge configuration of the designed converter.

This design strategically places all components on the top layer of the PCB, enhancing both functionality and aesthetics. Thermal vias are incorporated to manage heat effectively. These vias facilitate heat dissipation from the MOSFET switches to a heatsink attached beneath the PCB. Additionally, the capacitors illustrated in Fig. 3 serve as decoupling capacitors, critical for maintaining stable voltage levels and minimizing noise in the circuit.

2) Switch conduction losses: To determine the conduction losses in the switch, it is essential to determine the current's RMS value in one cycle. The conduction losses at the highest power flow point define the Pareto front. An example of the switch current in one cycle is shown in Fig. 4.

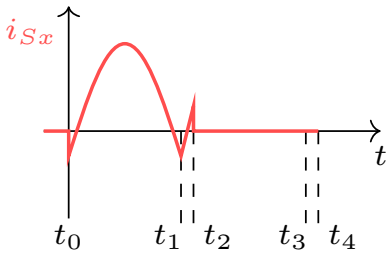

Fig. 4. Example of current flowing through the switches.

Using the converter in the Cap PS mode ensures that the RMS value of current in all the switches at a particular operating point is the same. This is a benefit of using this operating mode. The switch current can be decomposed into different Fourier coefficients. These coefficients can be used to find the rms current through the switches. The conduction losses then are estimated using (4)

$$P_{cond} = I_{rms}^2 R_{ds,on} \tag{4}$$

where, $R_{ds,on}$ is the drain to source resistance of the switch.

3) Switch turn-off losses: As discussed above, the converter is operated such that when the grid is balanced, the currents at the switching instances are the same for any particular switch. This current is given by (1). Furthermore, the turn-on losses are different due to the ZVS turn-on of all the switches. The switch turn-off losses are calculated using the method in [11].

B. Resonant Inductor

This study explores a range of resonant frequencies from 60kHz to 120kHz. Consequently, the inductance value of the resonant inductor varies with each resonant frequency and the associated maximum power flow level. The following sections outline the methodology for selecting and designing the resonant inductor.

1) Component Selection: For the core of the resonant inductor, this work exclusively considers PQ cores from Ferroxcube. The physical characteristics of these cores limit the feasibility of combining multiple cores to form a larger one, thereby reducing the number of viable inductor combinations. Given the design considerations for switching frequencies between 60-120 kHz and available data [12].

Regarding conductors, litz wire is chosen for the resonant inductor's winding. A comprehensive wire database was compiled using specifications from a litz wire manufacturer's website [13]. For every feasible core size, only those litz wires were chosen for which the calculated number of turns can fit in the winding window.

2) Losses: The losses in the resonant inductor significantly impact the overall efficiency of the converter. Due to the non-sinusoidal nature of the inductor current waveform, as depicted in Fig. 1, the iGSE method is employed to calculate the core losses [14].

Fourier analysis estimates copper losses and determines the RMS currents at different harmonic frequencies. Dowell's equation is then applied to ascertain the litz wire resistance up to the 10th harmonic of the resonant frequency. Detailed methodologies for calculating copper losses are discussed in [14], [15].

C. Resonant capacitor

The value of the resonant capacitor is dependent upon the resonant frequency (f_r) and characteristic impedance (Z_0) of the resonant tank. For a given maximum power flow and input voltage, the value of the characteristic impedance can be found by rearranging (3). The resonant capacitor's value is found using (5).

$$C_r = \frac{1}{2\pi f_r Z_0} \tag{5}$$

1) Component selection: The resonant capacitors used in this application are ceramic capacitors with C0G dielectric material.

2) Losses: The C0G dielectric is known for its high purity and low tolerance [16]. Hence, the ESR of these capacitors is very low [17]. On top of this, as C0G dielectric capacitors are not available with very high values, several of them are connected in parallel to achieve a suitable capacitance value. For example, nine C0G capacitors of 33 nF are connected in parallel to achieve a value of 297 nF. This further reduces the ESR value to less than 1 $\mathrm{m\Omega}$ in the operating frequency range [18]. Therefore, the losses in the resonant capacitors are neglected due to their low ESR.

D. Heatsink

1) Component selection: Selecting an appropriate heatsink for a design involves careful consideration of several critical characteristics to ensure optimal thermal management. Firstly, the attachment method is paramount; the heatsink should be specifically designed for attachment to the underside of the PCB. It must be compatible with a thermally insulating adhesive to provide secure mounting and ensure electrical isolation. Secondly, size constraints play a crucial role. The heatsink's dimensions should not exceed a maximum area of 100mm by 100mm, a limitation that is essential for ensuring compatibility with the available space and the overarching design of the PCB. Lastly, the thermal resistance specification for natural convection is a key factor. Since natural convection is the primary mode of heat dissipation, selecting heatsinks with well-defined thermal resistance data from the manufacturer for natural convection is critical. This specific data is indispensable for accurately evaluating the heatsink's effectiveness in dissipating heat within the intended operational environment.

By adhering to these specific criteria, the chosen heatsink will be well-suited for the thermal demands of the design while also conforming to the physical and operational constraints of the PCB layout. An example of the heatsink attachment method is shown in Fig. 5.

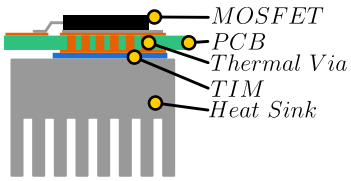

Fig. 5. Application of heatsink in the considered designs.

2) Temperature rise calculation: In this study, selecting an appropriate heatsink is crucial to ensure that the MOSFET junction temperature remains below a certain threshold, especially under high power flow conditions. Heatsinks are chosen for a maximum power flow of 3 kW, based on their ability to limit the switch junction temperature to 120 $^{\circ}\mathrm{C}$. This consideration is vital for reducing thermal cycling and enhancing the reliability of the semiconductor switches, as emphasized in [19].

To determine the steady-state junction temperature of the selected MOSFET, we refer to the thermal circuit depicted in Fig. 6. The ambient temperature is assumed to be 25 $^{\circ}\mathrm{C}$. Within this circuit, R_{jc} represents the junction-to-case thermal resistance, while R_{via} indicates the resistance offered by the thermal vias, which, according to existing literature, is about 8 $^{\circ}\mathrm{C\,W^{-1}}$ [20]. Additionally, R_{tim} signifies the thermal resistance of the thermal interface material, which in our design is considered to be a constant at 0.3 $^{\circ}\mathrm{C\,W^{-1}}$. Finally, R_{hs} represents the thermal resistance of the heatsink under natural convection conditions.

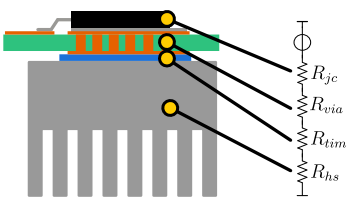

Fig. 6. Heat dissipation circuit considered for calculating the junction temperature of the MOSFET.

By applying this thermal resistance circuit model, we can accurately calculate the junction temperature of the switch using (6).

$$T_j = (P_{loss,cond} + P_{loss,off})(R_{jc} + R_{via} + R_{tim} + R_{hs}) + 25 \tag{6}$$

IV. Results

This study adopted a methodical approach to select various components for the series-resonant balancing converter from the Digikey website. This selection process was crucial in estimating the converter's approximate volume. The design space for all the major parameters and components of the converter are summarized in Table I.

By applying our loss calculation methodology, we determined the efficiency at the point of maximum power flow for all feasible converter designs. This analysis yielded two critical datasets: efficiency (η) and volumetric power density (ρ), which were instrumental in constructing the Pareto front for a 3 kW series-resonant balancing converter, as illustrated in Fig. 9.

Observations from Fig. 7 reveal that the data points representing feasible designs on the Pareto map are discrete. This discreteness can be attributed to utilizing real-world components in the converter design, which inherently exhibit discrete changes in volume. Notably, the analysis indicates that the feasible designs can achieve efficiencies as high as 98.6% and volumetric power densities reaching up to 6.4 kW/l. It is, however, important to note that these high levels of power density are achieved with a marginal trade-off in efficiency. This nuanced balance between efficiency and power density is critical in understanding the design and performance trade-offs in developing advanced converters for future bipolar DC grids.

TABLE I
DESIGN SEARCH SPACE FOR THE CONVERTER.

Component	Selection criteria/chosen value
MOSFETs	• Should be SMD component • Rated at 650 V • Commercially available • Bottom side cooled • Components shown in Fig. 2
Resonant frequency	60, ..., 120 kHz
Characteristic impedance	5 (kept constant for benchmarking designs)
DC Link Capacitor	• Voltage range: 400 - 500 V • Capacitance range: 40 - 80 µF
Resonant inductor core	• Shape: PQ • Sizes: 2016 to 5050 • Material: 3C95
Resonant inductor conductor	• Cross section area: 1 - 2.5 mm^2 • Litz wire
Heatsinks	• Natural convection • Thermal resistance: $\leq 3\ K\,W^{-1}$ • Length: ≤ 100 mm • Width: ≤ 160 mm • Height: ≤ 50 mm
MOSFET junction temperature limit	120 °C

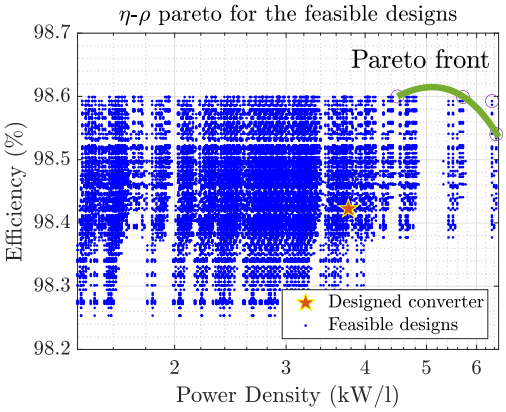

Fig. 7. $\eta - \rho$ Pareto front created with the analysis.

The designed converter prototype is shown in Fig. 8. Table II presents the selected components for designing the converter.

The converter was tested with various load powers. Fig. 9 shows the resulting efficiency data. It should be noted that the peak efficiency of the converter is more than 99% at a load power of around 900 W. However, at peak power of 3 kW, the efficiency decreases to around 98%. However, according to the loss model, the efficiency should be around 98.4%. Several factors lead to this discrepancy. These factors are listed below.

- The $R_{ds,on}$ of switches generally increases with the rise in junction temperature. At peak power, the algorithm assumes that the $R_{ds,on}$ does not change. However, the resistance should be considered higher than the nominal value, thus leading to higher losses.

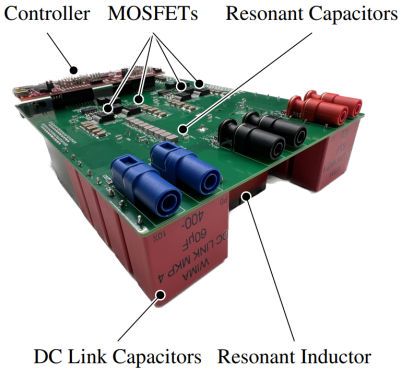

Fig. 8. Prototype of the designed converter.

TABLE II
PARAMETERS OF THE DESIGNED CONVERTER PROTOTYPE.

Parameter	Value
MOSFET part number	C3M0025065J1
DC link capacitors	4 x 60 µF
DC link capacitor part number	DCP4G056007GD4KSSD
Resonant frequency	100 kHz
Resonant capacitor	9 x 33 nF
Resonant capacitor part number	CGA9Q1C0G3A333J280KC
Resonant inductor	8.6 µH
Core size	PQ 5050
Number of turns	11
Conductor area	2.3755 mm^2
Power stage volume	4 x 42480 mm^3
Controller board volume	165000 mm^3

- For calculating the loss in the resonant inductor, Steinmetz coefficients are used, which are usually not accurate at higher power and with non-sinusoidal waveforms. This leads to further discrepancies between the calculated and measured losses.

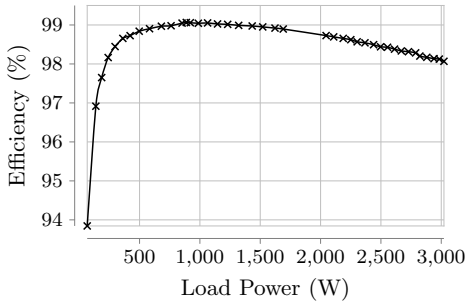

Fig. 9. Measured efficiency of the converter with respect to the power flow.

V. CONCLUSION

In this article, we present a comprehensive methodology for selecting and designing a series-resonant balancing converter. The discussion begins by elucidating the operating principles of the converter, providing a critical foundation for the subsequent component selection process. We then delve into detailed methodologies for choosing the key components

of the converter, an essential step in ensuring its optimal performance.

To complement this, we explore the methods used for calculating the losses within the converter, a pivotal aspect in evaluating its efficiency. Leveraging a meticulously compiled component database sourced from Digikey.com, we construct a Pareto front representing the feasible designs for a 3 kW converter. The Pareto front analysis reveals promising outcomes; the converter demonstrates an exceptional efficiency of up to 98.6% and a remarkable volumetric power density of 6.4 kW/l.

These findings underscore the potential of the series-resonant balancing converter as a significant contributor to the evolving landscape of bipolar DC grids. The converter's high efficiency and power density make it a compelling choice for future bipolar DC power grid applications, promising enhanced performance and reliability.

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