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LOW TEMPERATURE PUREB TECHNOLOGY FOR CMOS COMPATIBLE PHOTODETECTORS

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In this thesis, conventional high temperature (HT, 700 °C) PureB technology is optimized in order to fabricate detectors with improved key parameters such as the spatial uniformity of the responsivity. A novel technology for low temperature (LT, 400 °C) boron deposition is developed providing a uniform, smooth, closed LT boron layer. This technology is successfully employed to create near-ideal LT PureB (pure boron) diodes with low, deep-junction-like saturation currents which make it possible to fully integrate LT PureB photodiodes together with electronic interface circuits and other sensors on a single chip. In this way, smart sensor systems or even CCD or CMOS UV imagers can be realized.

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To my parents
To my lovely wife, Fereshteh

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Chapter 1

Introduction

1.1 Application challenges

In the last years we have witnessed an increase in the demand for both high performance ultraviolet and low energy electron detectors. Such detectors are used in high tech applications such as optical lithography and electron microscopy; medical imaging; protein analysis and DNA sequencing; forensic analysis; disinfection and decontamination; space observation; etc.

To meet these demands, a new silicon detector technology has been proposed by DIMES (TU Delft) called "PureB" technology. It is based on chemical vapor deposition of pure boron on silicon and has been successfully applied for fabricating extremely shallow, i.e. less than 10 nm deep, silicon p^+n junction diodes for a number of leading edge device applications. With PureB technology, at a nominal temperature of 700 °C, a nm-thin amorphous boron layer is deposited on silicon while simultaneously an effective p^+ delta-doping of the silicon surface is realized. Detectors produced in this way have demonstrated an impressive performance for low penetration depth beams such as vacuum ultraviolet (VUV) radiation and low energy electrons (< 1 keV). Comparisons of PureB technology to state-of-the-art Si-based UV and electron detectors are presented in Table 1.1 and Table 1.2, respectively.

Near ideal[1], low leakage current, highly sensitive, radiation-hard diode characteristics are demonstrated. Moreover, the fact that the boron deposition is conformal and highly selective to Si makes PureB technology an attractive

[1] Diode ideality factor, $n \approx 1$

candidate for creating junctions on silicon nanowires and advanced CMOS transistors including a source/drain in p-type FinFETs. The impressive properties of PureB devices have made this technology become commercially available very quickly as EUV photodetectors for ASML EUV litho tools and electron detectors for FEI scanning electron microscopy (SEM) systems.

However these PureB detectors still suffer from a non-uniformity of the boron layer leading to spatial non-uniformity of the detector responsivity. Moreover, the PureB technology is not CMOS compatible due to the relatively high boron deposition temperature, and hence it cannot be integrated in a standard CMOS process to produce high performance ultraviolet and low energy electron image sensors.

1.2 Main question

The main questions of the reported research work are: how to improve the PureB technology such that better spatial uniformity of the detector responsivity is achieved and how to make the technology CMOS compatible.

1.3 Potential solutions

To answer these questions, first optimization of the conventional 700 °C PureB technology is needed to fabricate detectors, with improved key parameters such as the spatial uniformity of the responsivity. This can be achieved by studying the deposition kinetics and the deposition chamber characteristics of the boron deposition from diborane (B_2H_6) along with investigating the pattern dependency and the loading effects as sources of layer non-uniformity.

The second step is to modify the PureB technology such that it becomes applicable at temperatures lower than 500 °C without deteriorating the detector characteristics, which will make the technology completely CMOS compatible and part of standard IC/CMOS processes.

1.4 Objectives

The objectives of this thesis are to find the best answer to the main question presented above by: proposing an advanced version of the PureB

technology; demonstrating an excellent performance of the detectors produced by this technology; and proving that the modified PureB technology is CMOS compatible.

Table 1.1: Performance overview of representative commercially available Si-based UV detectors compared to the PureB UV photodetector.

Detector	*ETH PtSi-nSi*	*IRD AXUV*	*IRD SXUV* [a]	*IRD UVG*	*Hamamatsu (S5226)*	PureB[b]
Junction type	**Schottky**		**n-on-p**		**p-on-n**	**p-on-n**
EUV sensitivity (A/W)@13.5nm	~ 0.2 [c]	~ 0.265	~ 0.23	Unknown	Unknown	0.267
Stability under EUV	Unknown[d]	Not stable	Good[e]	Unknown	Unknown	Δ ~ 3%[f]
VUV sensitivity (A/W)@193nm	~ 0.03	~ 0.1	~ 0.01	~ 0.137	~ 0.1	0.102
VUV sensitivity (A/W)@157nm	~ 0.02	~ 0.1	< 0.01	Unknown	Unknown	0.123
VUV sensitivity (A/W)@121nm	≤ 0.02	Unknown	< 0.01	< 0.05	Unknown	0.116
Stability under DUV/VUV	Δ ~ 2%	Not stable	Un-known	Δ ~ 10%	Not stable	Δ ~ 4%
References	[1, 2]	[1, 3-5]	[4, 5]	[1, 3]	[1]	[6]

a. SXUV: Si-based n-on-p junction photodiodes with nitride metal silicide front window.
b. Data are based on as-deposited PureB photodetectors without any post-processing thermal annealing.
c. Value from measurement at PTB [6].
d. Stability proven only in the VUV range [1].
e. No more information is given in the ref.
f. Δ: reduction in responsivity based on the data reported in the mentioned references.

Table 1.2: Performance overview of representative commercially available, research-reported Si-based electron detectors compared to PureB electron detector.

Detector	Commercial BSE	Commercial vCD	Delta doped e2V CCD 97	PureB BSE
Electron signal gain[a] @ 1 KeV	~ 46	~ 126	~ 112	213
Electron signal gain @ 500 eV	~ 18	~ 52	~ 47	102
Electron signal gain @ 200 eV	Unknown	Unknown	~ 13	34
Stability	Δ ~ 5%	Δ ~ 5%	Unknown	Δ ~ 4%
References	[7, 8]	[7, 8]	[9]	[10]

a. Electron signal gain, Gph, is defined as I_{ph}/I_{beam}, where I_{ph} is the output current of the photodiode and I_{beam} is the current of the incident electron beam, assuming a negligible dark current.

1.5 Organization of the thesis

Fig. 1.1 represents the basic structure of this thesis. The content of the chapters is as follows:

In Chapter 2, an overview of the conventional boron CVD technology performed at 700 °C is presented. Application of this technology is overviewed in the state-of-the-art ultraviolet (UV) photodetectors and low energy electron detectors. The superior electrical and optical performances of these devices are reviewed together with some of the drawbacks, limitations and imperfections, which are the points of improvement in this thesis.

In Chapter 3, in order to achieve better control of the boron deposition, an analytical kinetic model is proposed to describe the deposition kinetics and the deposition chamber characteristics that determine the boron deposition rate from diborane (B_2H_6) over the wafer.

In Chapter 4, the conventional boron deposition is optimized to provide uniform and reliable deposition of 2-nm-thick boron layers, with thickness variations of only a few angstroms. To solve the boron layer uniformity problem, in this chapter, the loading effect and the pattern dependency are investigated and identified as sources of layer non-uniformity.

In Chapter 5, an improved technology for low temperature (LT, 400 °C) boron deposition is presented providing a uniform, smooth, closed LT boron layer. The temperature dependency of the kinetics of boron deposition on patterned Si/SiO_2 surfaces in the temperature range from 700 °C to 400 °C is discussed in this chapter.

In Chapter 6 it is demonstrated how the new knowledge presented in Chapters 3, 4 and 5 is employed to fabricate high performance PureB detectors particularly for low penetration photon/electron beam detection. First, Section 6.1 presents the fabrication process of high responsivity, high stability PureB photodiodes with a 2-3 nm-thick boron top layer using an optimized conventional (700 °C) boron deposition. Then, in Section 6.2, it is shown that the LT boron depositions performed at 400 °C can be used to create p^+n photodiodes with nm-thin boron layer windows and near-theoretical sensitivity for irradiation with either UV light or low energy electrons down to 200 eV, with negligible optical or electrical degradation.

Lastly, in Chapter 7 the conclusions of the presented research work are drawn and suggestions are made for future work.

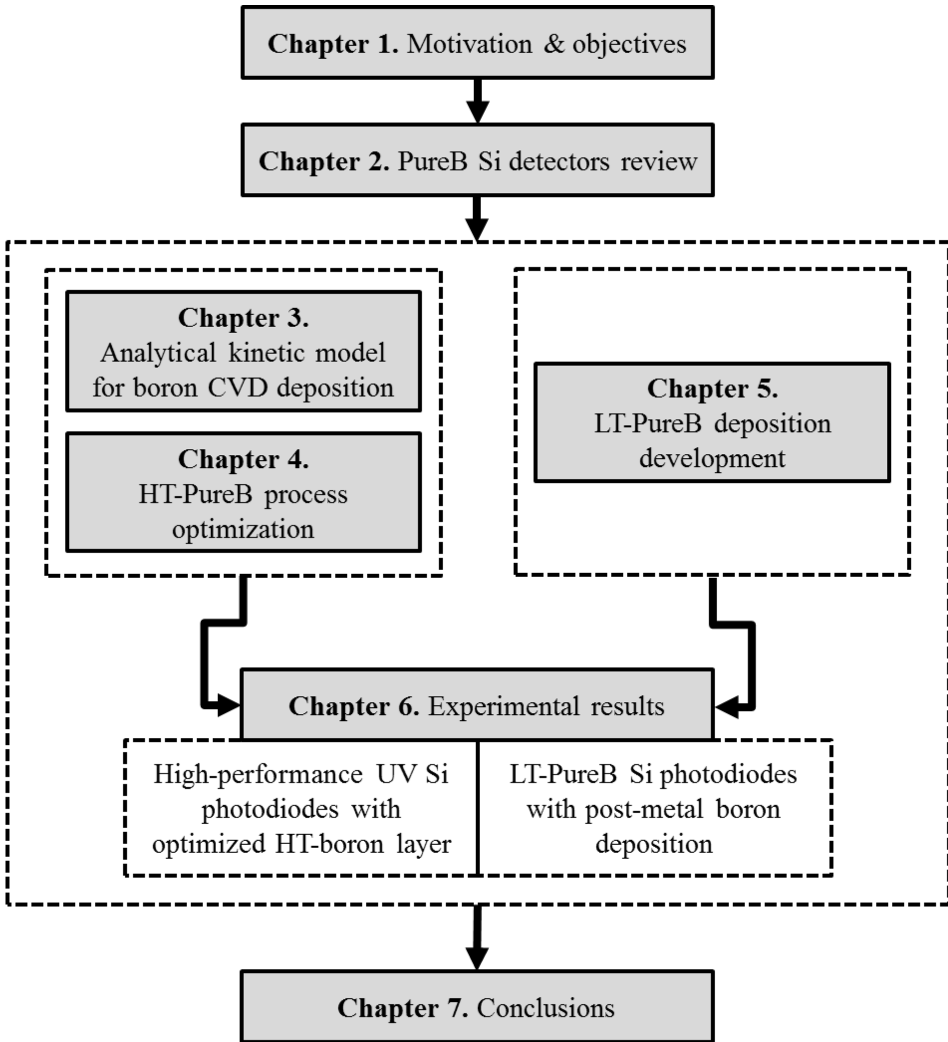


Fig. 1.1: Basic structure of this thesis.

Chapter 2

PureB silicon-based detectors

In this chapter, an overview of the conventional pure boron (PureB) CVD technology performed at 700 °C is presented. Application of this technology in state-of-the-art ultraviolet (UV) photodetectors and low energy electron detectors is also reviewed. The superior electrical and optical performances of these devices are reviewed together with some of the drawbacks, limitations and imperfections, which are the points of improvement in this thesis. It will be shown, based on the knowledge provided in this thesis, that the current PureB technology can be optimized in order to fabricate superior performance PureB detectors, particularly for low penetration photon/electron beam detection.

In Section 2.1 a short introduction is given. In Section 2.2 the existing PureB detector production technology is presented. In Section 2.3 the electrical and optical properties of the PureB detectors are discussed. Section 2.4 reveals the drawbacks and limitations of the state-of-the-art PureB detectors. The conclusions are in Section 2.5.

2.1 Introduction

For several years now, source/drain formation for CMOS devices has been the main driving force behind the development of novel doping technologies targeting nm-shallow, ultra-abrupt, and highly doped junctions with damage-free properties. Likewise, there are also many other *pn*-junction-based devices beyond the Bipolar/CMOS scenario that also can profit from advances in doping technology, such as silicon-based detectors particularly for low penetration photon/electron beam detection. Here the focus has been on detectors that have become very successful boron deposition applications.

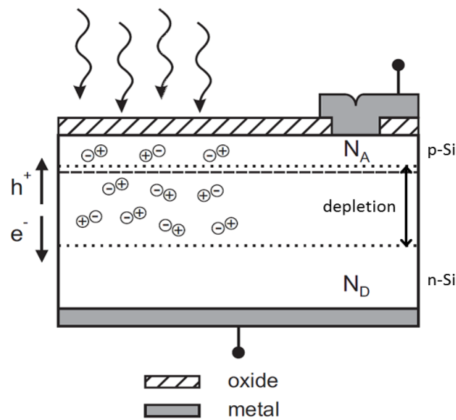


Fig. 2.1: Schematic cross-section of a conventional p^+n photodiode.

Schematic cross-section of a conventional p^+n photodiode is shown in Fig. 2.1. Although concepts of these devices are well known [11], their performance has so far been limited by manufacturability and design tradeoffs.

Photodiodes also count on the depletion region of a *pn* junction and on the resulting electric field in order to separate electron-hole pairs generated by the incident radiation and to collect holes and electrons at the anode and cathode, respectively. Nevertheless, photogenerated carriers are also formed in the quasi-neutral top diffused junction. In fact, the intensity of the radiation and thus the carrier generation rate inside the device decreases exponentially from the surface with a characteristic length, i.e. the penetration depth, defined as the reciprocal of the absorption coefficient at the incident radiation wavelength. Therefore, an extremely ultrashallow junction will be instrumental in minimizing the carrier loss in the quasi-neutral region, since electron-hole pairs can recombine before being collected at the electrodes and most of the photogeneration occurs in the space-charge region [11, 12]. This becomes crucial in applications designed for low penetration beam detection such as VUV light and less than 1 KeV electrons where the penetration depth in silicon and also other solid materials is less than 10 nm [13-15].

Based on these considerations, a Schottky diode would appear to be the most efficient solution for these kinds of devices, since it gives an ideal abrupt junction and the depletion already starts from the surface [2]. On the other hand, since such devices generally operate in reverse bias conditions, *pn* junction configurations are preferred to Schottky contacts because the I-V characteristics

of the former have lower current levels. Moreover, photodiodes with low 'dark current', i.e. current without irradiation, can have a greater signal-to-noise ratio and be more sensitive to weak radiation intensities [11, 12]. The subsequent influence on optical performance will be discussed below.

Although ultrashallow and abrupt p^+ doping profiles are available, the reduction in the junction depth should also be supplemented with higher doping efficiency, otherwise the I-V characteristics will be influenced in a less favorable way [16, 17]. In fact, the resulting junction will not suppress the injection of minority carriers from the substrate, and the diode current will be high. Doping techniques, such as implantation or CVD epitaxial growth, are not suitable [18]. In the former case, in fact, besides the unavoidably broadening of either the p^+ profile or the background n-type doping distribution, the depletion region might be affected by reduced carrier lifetime due to lattice damage. This will generally increase the generation recombination leakage current and, in particular, the loss of photogenerated carriers in devices for radiation detection. CVD depositions can provide nm-thick Si layers with abrupt doping transitions; however, low temperature processing, which is required, for instance, in photodiode implementations, cannot provide high enough efficiency for boron doping due to limited solid solubility [18, 19].

Regarding the detector application, recent years have witnessed a significant growing interest in the development and fabrication of highly sensitive, stable detectors particularly for low penetration photon/electron beam detection such as vacuum UV (VUV) wavelengths (λ = 200-10 nm) down to soft X-rays (λ = 10-0.1 nm), and electrons of less than 1 KeV [20-24]. This has been mainly driven by advances in lithography equipment, since several sensors are used to evaluate and optimize imaging performance as position sensing and beam intensity monitoring.

For many of these applications, the radiation-sensitive area is exposed to high photon flux doses and is generally affected by either surface or bulk contamination. These harsh conditions readily deteriorate the optical performance and limit the lifetime of the device itself. Therefore, ruggedness and long term stability when exposed to high radiance and aggressive environments are two of the essential key features for detector applications in the VUV spectral range, alongside extreme requirements for excellent reliability, high and spatially uniform sensitivity, wide dynamic range, high linearity, and low noise (i.e. low dark current) [22, 25, 26].

Solutions for UV radiation detection are generally offered by silicon-based devices, which are inherently responsive to a broadband radiation extending from the near infrared region wavelengths (≤ 1 μm) down to soft X-rays ($\lambda \sim 1$ nm) [27, 28]. Moreover, they have attractive characteristics in terms of accuracy and prediction of optical efficiency [29]. Although III-V wide bandgap semiconductors, like gallium nitride (GaN), aluminum nitride (AlN), aluminum gallium nitride (AlGaN), have been recently considered as promising candidates mainly due to their radiation hardness [30-32], they still face lower sensitivity and many processing issues compared to more mature and cost effective Si technologies. Even their intrinsic solar blindness, i.e. a good UV/visible response ratio, can be feasibly achieved for silicon devices. In fact, it has been demonstrated that integration of a thin film of a suitable filtering material directly on the exposed surface is fully compatible and makes selective response to a much narrower band possible [33]. Fig. 2.2 [34, 35] shows a classification diagram of the existing UV photodetectors together with key arguments (*in italics*) which lead to the conclusion that silicon photodetectors are the superior option.

Regarding the device structure, documented methods of producing reliable UV detectors involve mainly planar diffused silicon *pn* junctions, either p^+n [36] or n^+p [37], and Schottky diodes [38]. Nevertheless, natural inversion layer photodiodes result in low yield due to poor process control of the indirect method of forming the surface depletion and conductive top layer. As stated above, diffusion-type photodiodes have lower dark current. In addition, they are much more sensitive than Schottky-type photodiodes either on Si or III-N compounds, especially at deep ultraviolet (DUV) wavelengths (120-200 nm). The limited radiation sensitivity of Schottky diodes might be due to a combination of several factors, which are mainly dependent on the specific photodiode technology, such as high reflection and absorption losses in the front metal contact, lower surface electric field, and higher surface recombination. On the other hand, the presence of a metallic front-layer has been demonstrated to provide a more stable performance under heavy radiation exposure [39]. Similar ruggedness has been reported for metal-silicide windows on p^+n junction diodes [40, 41].

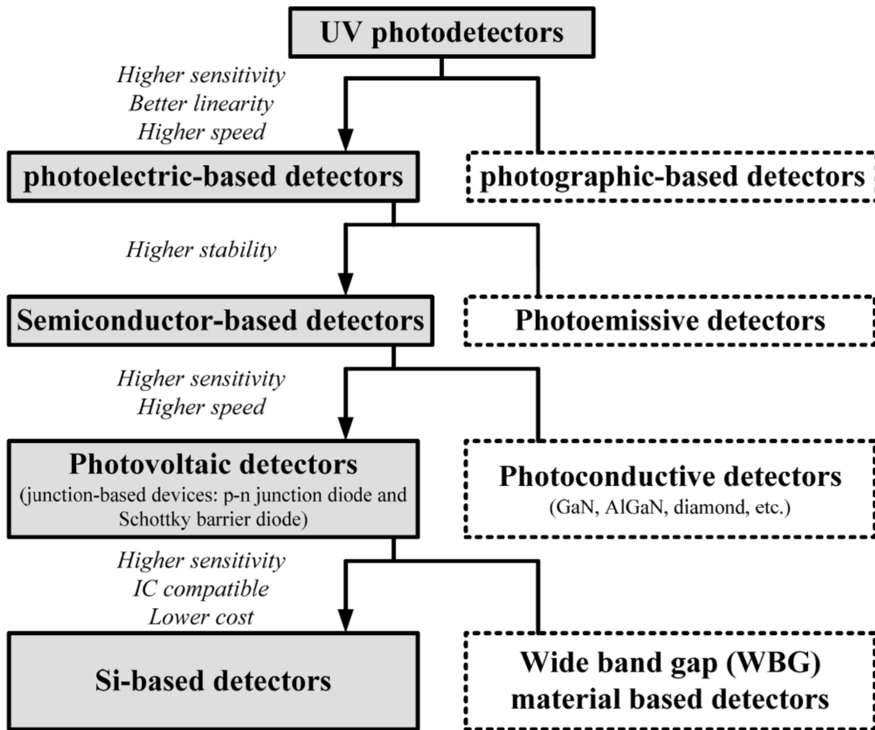


Fig. 2.2: Classification of solid state UV photodetectors [34, 35].

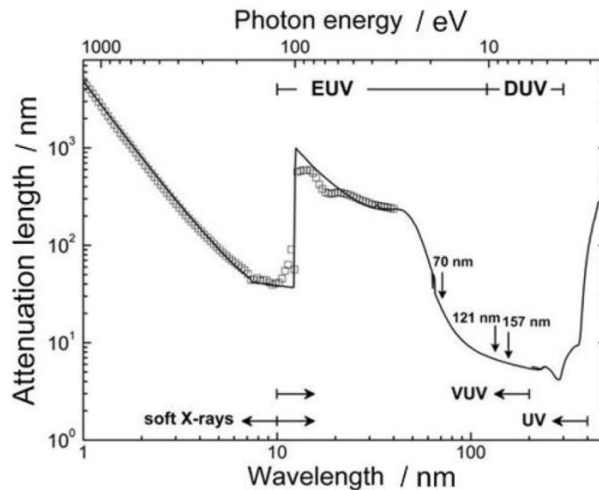


Fig. 2.3: Attenuation length (penetration depth) in Si as a function of the radiation wavelength in the UV/soft X-ray spectral range; solid line after [15], square symbols after [13, 42].

Moreover, for planar diffused diodes, the spectral sensitivity to UV radiation is also dependent on the Si absorption coefficient, since the attenuation length (penetration depth) of UV photons into silicon approaches values lower than 10 nm in the wavelength range of 100-350 nm, as shown in Fig. 2.3.

In particular, a minimum of ~ 5 nm is reached at the DUV wavelengths of applicative interest, such as λ = 157 nm and λ = 193 nm. Therefore, to optimize the optical conversion efficiency the uppermost edge of the depletion region should be within this distance. However, commercial *np* junction diodes simply rely more on both the built-in electric field induced by the gradient of the n^+ diffused doping profile and the formation of junctions shallower than the diffusion length of the minority carriers. The latter requirement is quite straightforward to realize, since the diffusion length of the holes is about 0.4 μm or higher are reported for n^+ doping levels of about 10^{18}-10^{19} cm^{-3}. Most of the built-in electric field is also induced by steep dopant pile-ups that are intentionally formed during thermal growth of the SiO_2 coating layers. In fact, *n*-type species, such as arsenic and phosphorus, segregate at the Si/SiO_2 interface [37]. In contrast, for boron profiles an opposite segregation mechanism does not allow for tailoring of the electric field in this manner, and thus the carrier collection efficiency is poorer than the n^+p implementation. Furthermore, the presence of positive charges in the anti-reflection oxide coating can induce further carrier losses in the p^+ front region, since the resulting electric field will hinder the carrier collection. For these reasons, n^+p photodiodes have been generally preferred over p^+n junctions, as they are claimed to be inherently more stable than boron-diffused devices in the UV spectral range [43]. However, one could easily argue that the n^+ surface peak would be too strictly dependent on the presence of the SiO_2 front-layer, which can be a cause of either radiation absorption at short wavelengths or radiation-induced degradation.

On the other hand, the ability to form extremely ultrashallow, highly doped, completely damage-free junctions can maximize the optical performance up to the theoretical limits for even p^+n photodiodes, as in the case of boron deposition. In fact, the reduced junction depth would significantly increase the percentage of carriers generated in the depletion region. At the same time, the electric field induced by the high doping concentration gradient would efficiently separate any further electron-hole pairs created in the shallow diffused area, since it would not be confined within the space-charge region, but it would extend to the surface [11]. The high doping concentration can have the

additional advantage of being able to screen any influence of oxide charges when anti-reflection coating layers are needed. Moreover, the enhancement of carrier collection by such doping-induced electric fields strongly prevents any recombination of photogenerated carriers at the Si surface or Si/SiO_2 interface, since minority carriers would be in the presence of recombination traps for a negligible time.

In conclusion the pure boron (PureB) CVD deposition technology is demonstrated to be a reliable solution for the formation of the highly doped, completely damage-free, ultrashallow (i.e. less than 10 nm), p^+ junction needed in the aforementioned advanced detectors particularly for low penetration photon/electron beam detection. In the following section, conventional PureB technology implemented at 700 °C is briefly reviewed together with application of this technology in the state-of-the-art ultraviolet (UV) photodetectors and low energy electron detectors.

2.2 Conventional PureB CVD technology

Conventional boron CVD technology is implemented at temperatures from 500 °C to 800 °C. It was developed at the DIMES (Delft Institute of Microelectronics and Nanotechnology) facilities of TU Delft [44, 45]. Detectors for some commercial applications, such as EUV photodetectors for ASML EUV litho tools and electron detectors for FEI SEM systems, were fabricated using a "high temperature (HT)" (700 °C) CVD process [20-22, 24, 28, 46-53].

In this section we shall give a short overview of this detector technology. For more details readers are referred to the thesis of M. Popadic [18] and F. Sarubbi [19], where extensive research has been reported on characterization of the PureB technology, generally using the 700 °C CVD process.

Processing conditions and pure boron properties

For the PureB CVD process, diborane (B_2H_6) is used as the precursor gas with a doping concentration of 0.2% at a typical flow rate of 490 sccm (standard cubic centimeters per minute), while hydrogen (H_2) is used as a carrier gas with a typical flow rate of 20 slm (standard liters per minute) and also for the dilution of the doping source [19]. These deposition chamber conditions have proven to be particularly ideal for several reasons. First, at temperatures higher than 700 °C the boron layer will not be built up due to increased B-desorption and

significant boron silicide formation. Second, for much lower diborane concentrations, for example 0.02%, the deposition rate goes from the nm-per-minute range to hour-long rates, while for higher concentrations (e.g. 2%), tens of nanometers are deposited per minute and the deposition loses one of its otherwise attractive properties: selective deposition on Si with respect to silicon oxide.

Deposition can be performed at either atmospheric (ATM) or reduced ambient pressures. Rotation of the sample during the deposition can provide a homogeneous gas distribution profile and prevent gas depletion phenomena significantly (details in Section 3.6.1). For a given temperature, ambient pressure and diborane concentration, the boron coverage on the Si surface and the doping of the crystalline silicon substrate is controlled by varying the deposition time.

The samples were *ex-situ* prepared for boron deposition as described in Appendix A. As an extra measure to assure an oxygen-free surface, *in-situ* cleaning is performed for the wafers destined for a HT boron deposition by baking in H_2 at 800 °C for 4 min prior to the deposition cycle [45].

A high-resolution Transmission Electron Microscope (HRTEM) image of a boron layer is shown in Fig. 2.4 for a temperature of 700 °C, 10-min deposition time at a constant pressure, diborane and carrier gas flow rate conditions of ATM pressure, 490 sccm and 20 slm, respectively, for which a constant deposition rate is obtained for depositions longer than 2 min (see Fig. 2.5). The process has a very distinct starting process for deposition of B on bare Si before it proceeds with deposition of B on B as will be described later in Section 3.4.

During the thermal decomposition of diborane, the high gas-source injection (490 sccm) causes boron atoms to readily segregate on the bare silicon surface in amorphous phase, thus forming a boron layer. In addition, at such temperature significant presents of B content at the Si interface induces boron atoms to initiate a reaction with the silicon in a boron-silicon phase [54]. Thus a boron silicide B_xSi_y layer is also formed at the deposition temp. > 500 °C, which here is seen as a roughening of the c-Si surface.

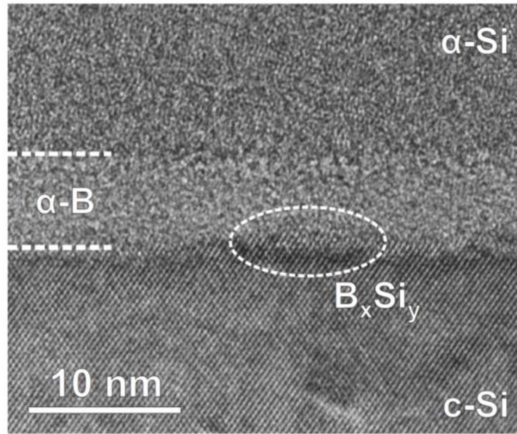


Fig. 2.4: High resolution TEM image of a boron layer (α-B) formed after a 10-min B2H6 exposure at 700 °C. The sample was covered with a physical layer deposition (PVD) of α-Si as a contrasting layer [45].

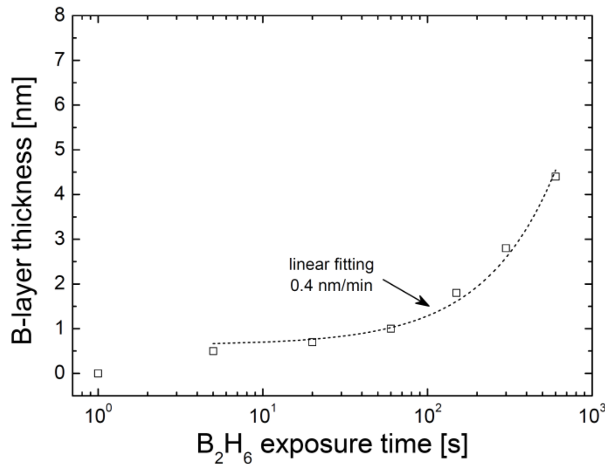


Fig. 2.5: Thickness of the boron layer (deposited at ASMI Epsilon one and measured by ellipsometry) as a function of deposition time at a pressure of 760 torr, temperature of 700 °C, and gas flow rate of 490 sccm [45].

The deposition rate, i.e. boron thickness values can be extracted from ellipsometry measurements by modelling the refractive index of the boron stack as 3.2, a value that was calibrated by a TEM analysis of the boron layer. The resulting deposition rate of 0.4 nm/min compares well with the rate found previously in [45] from SIMS analysis, but ellipsometry has the advantage of being a quick, non-destructive, in-line measurement technique that appears to be

applicable down to nm thickness of the boron layer (Fig. 2.5). The measured layer thickness includes both boron and a boron/silicon transition layers on top of the c-Si wafer, the ratio of which varies with the deposition temperature set for B_2H_6 dissociation.

The effective B-doping and junction depth in the underlying c-Si are determined by the solid solubility at deposition temperatures and duration of the thermal diffusion/boron deposition. For standard 700 °C deposition in photodiode fabrication on n-Si substrates, the obtained doping regarding the solid solubility of boron in bulk silicon is ~2×10^{19} cm^{-3} and diffuses only nanometers away from the surface even for 30-min long depositions [48]. This is also shown in the simulations of Fig. 2.6, where the doping profiles at 700 °C with different exposure times are presented.

The simulations were performed without implementing a point defect model because previous works had shown that no detectable transient enhanced diffusion (TED) or boron enhanced diffusion (BED) effects are active during the deposition process or subsequent annealing steps. Thus it is expected that the doping profile is determined by the thermal diffusivity and solid solubility at the given temperature [17].

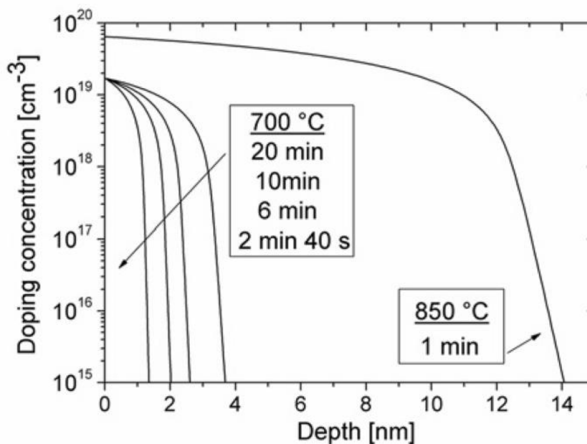


Fig. 2.6: Simulations of boron doping profiles achieved by drive-in from a constant boron surface doping set at the solid solubility of the boron in Si. An annealing temperature of either 700 °C or 850 °C is applied with different drive-in times [53]. Performed with the software Synopsys Taurus TSUPREM [55, 56]

For a substrate doping of 10^{15} cm^{-3}, the simulations predict junction depths of 1.4 nm, 2.0 nm, 2.6 nm, and 3.7 nm for deposition times of 2 min 40 s, 6 min, 10 min, and 20 min, respectively. Although this is extremely shallow, a reasonable (not extremely high) sheet resistance in the 10 kΩ/sq range is still obtained [17]. In this way, a highly doped, ultrashallow junction is formed in a tunable manner, which means that it can be designed for specific applications by trading off the properties such as the junction depth, boron layer thickness, c-Si doping level, layer resistivity, etc. An additional advantage of forming $p^{+}n$ diodes using boron deposition at 700 °C is the experimentally proven fact that the deposition location is restricted by high selectivity in terms of the oxide openings in the Si wafer, since the boron layer deposits exclusively on the oxide-free silicon surfaces. An example of the resulting diode I-V characteristics for different deposition times and temperatures, including the case for which no boron is deposited, is shown in Fig. 2.7. As can be seen, all diodes show near-ideal behavior with ideality factors lower than ~ 1.02, which is in accordance with the conclusion that the boron deposition process does not introduce any defects that cause significant leakage currents. Furthermore, at both deposition temperatures, increasing the boron deposition time leads to a decrease in the saturation current, for which a transition is seen from the high current Schottky diode case to a low current $p^{+}n$ diode characteristic.

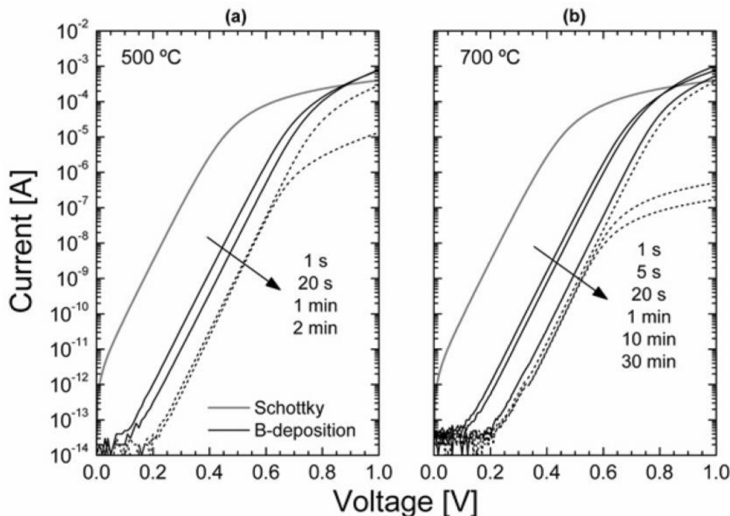


Fig. 2.7: Diode I-V characteristics for various deposition times at either (a) 500 °C or (b) 700 °C. The anode area is (2×1) μm^2. For comparison, the I-V curve of a Schottky diode is also included [45].

As a brief overview of the conventional boron layer deposited at 700 °C, the following can be considered attractive properties of this layer:

1- Formation of an effective highly doped ultrashallow p^+n junction in a tunable manner;
2- Layer formation selective to Si/SiO_2 surfaces for deposition at 700°C;
3- Constant deposition rate, which gives linear relation between thickness versus deposition time;
4- Totally damage-free junction formation, i.e. no detectable transient enhanced diffusion (TED) or boron enhanced diffusion (BED) defects are active during the deposition process or subsequent annealing steps;
5- Ideal p^+n diode behaviors ($n \approx 1.02$);
6- Effective suppression of minority carrier injection from the substrate even for nm-thick deposited boron layers, i.e. low saturation currents of boron deposited p^+n diodes;
7- Natural diffusion barrier layer between Si and pure Al layers–a prerequisite for front entrance window formation in nm low penetration depth radiation detectors;
8- Stability in the vacuum environment, and under harsh irradiation.

The impressive aforementioned properties of the boron layer make this technology an attractive process for fabricating detectors which can detect low penetration depth beams. In the Section 2.3 we shall discuss the electrical and optical properties of the PureB devices, while the main performance drawbacks and limitations will be discussed in Section 2.4 with some examples.

2.3 PureB detector properties

In this section a short overview of the properties of the state-of-the-art PureB silicon-based detectors for applications in the ultraviolet (UV) spectral range and also for low energy electron detection are given, together with a brief comparison to other commercially available devices. The advantages of the state-of-the-art PureB UV photodiodes and electron detectors are highlighted.

2.3.1 **Electrical characterization**

PureB UV photodetectors

The PureB technology has been successfully applied in the fabrication of planar p^+n photodiodes for radiation detection throughout the UV spectral range i.e. extreme/deep/vacuum ultraviolet (EUV/DUV/VUV). The impressive properties of the PureB devices made this technology quickly commercially available.

Fig. 2.8 shows a basic structure of the PureB UV photodetector, which can also be seen in more detail as the final result of the PureB process flow described in Appendix B.

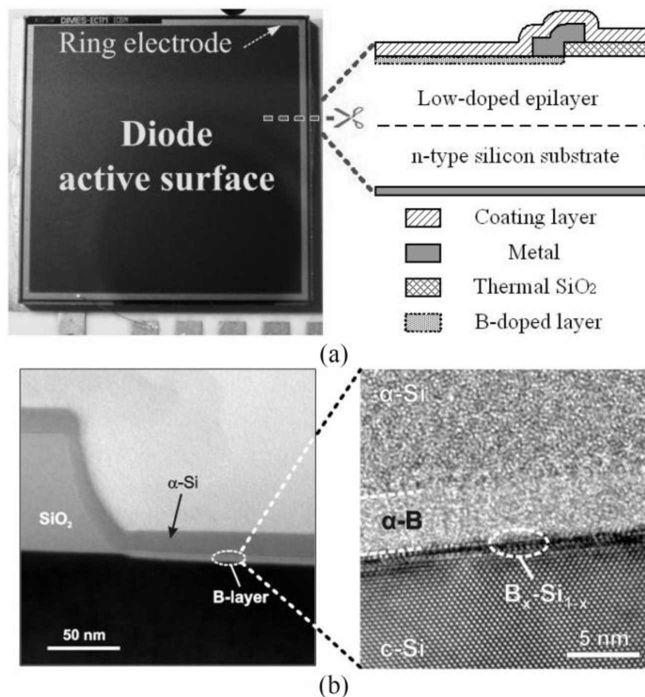


Fig. 2.8: (a) Photo and cross-section of fabricated PureB diodes (1×1 cm^2) [53]; (b) TEM images of a 10-min boron deposition on a Si(100) substrate. The sample was covered with 20 nm of PVD α-Si for the TEM analysis. The figure is reproduced from [44, 45, 52].

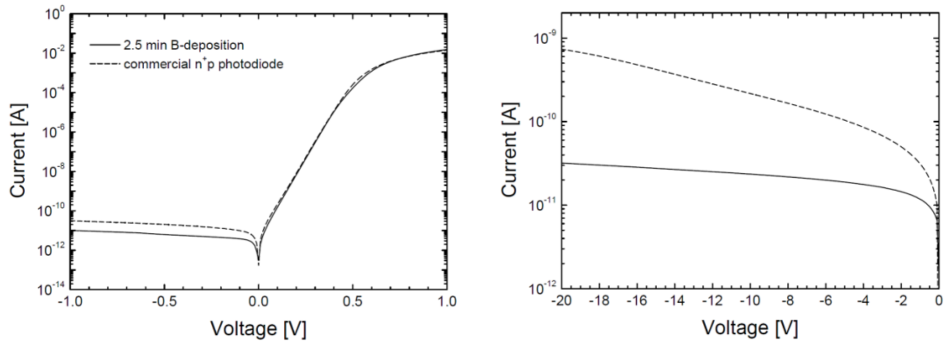


Fig. 2.9: (Left) I-V characteristics and (right) reverse I-V characteristics of a 6-min as-deposited B-diode compared to a state-of-the-art n^+p photodiode. The active area is 10.75 mm^2 [19].

In Fig. 2.8b, TEM images are shown of a 10-min boron layer deposited on a Si(100) substrate. As indicated in the images, this technique offers the advantage complete boron coverage over Si surfaces.

Fig. 2.9 shows the I-V characteristics of a 6-min PureB diode in comparison to a commercial n^+p photodiode [19]. An excellent electrical performance is achieved in terms of low dark current (< 50 pA at a reverse bias voltage of 20 V) and ideal behavior for such a large diode active area (10.75 mm^2). In fact, the voltage dependence on the dark current for the state-of-the-art device reveals that the generation effects dominate, while the PureB diodes benefit from both the high carrier lifetime semiconductor material in the depletion region and negligible surface generation recombination (g-r) over the entire active area. This also emphasizes that this technology delivers a defect-free p^+n ultrashallow junction. Furthermore, PureB diodes can uphold a very high breakdown voltage. Extremely low dark current of ~1 pA, for a diode with a (300×300) µm^2 junction area, is observed at a reverse bias voltage as high as -40 V [23, 26].

To verify the response time, the dynamic performance of the PureB photodetector with an 11 mm^2 circular shaped active area was experimentally evaluated. Experimental results are presented in Fig. 2.10. It can be seen that the measured time constants are similar even when the light spot has different sizes and locations [53, 57]. The time constant extracted from the measurement is about 98 ns.

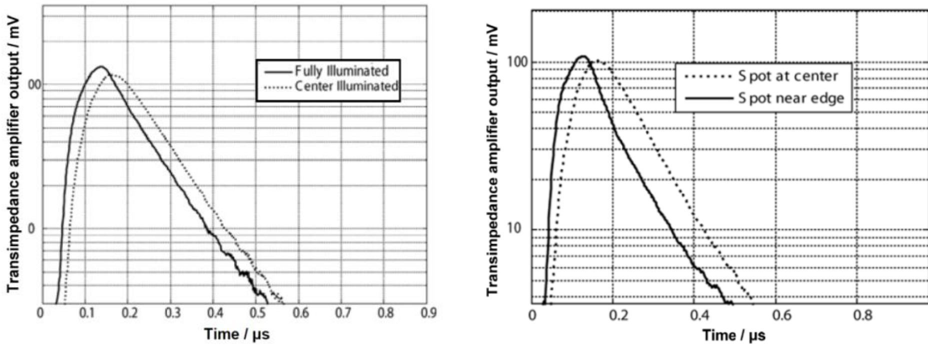


Fig. 2.10: Measured photodiode response to a pulse radiation input (right) when the illuminated area sizes are different, and (left) when the illuminated spot positions are different [53, 57].

The response time of the PureB diodes is limited by R_s and C_j. Therefore, with smaller values for R_s and C_j, a higher operational speed can be achieved. The junction capacitance can be adjusted by varying the thickness of the low doped epi-layer and the doping profile (see the fabrication process in Appendix B). However, technology and production cost limitations need to be considered when optimizing the process in this direction. Subsequently, what remains to be considered is the reduction of R_s. Post-thermal processing (i.e. thermal annealing/drive-in) after boron deposition can be used for optimizing the R_s. As can be seen in Table 2.1 and Fig. 2.11, by controlling the junction depth in the range from a few nanometers to hundreds of nanometers, the R_s can be adjusted correspondingly.

Table 2.1: Simulated junction depth versus post-thermal annealing recipes.

Post-thermal annealing	Simulated junction depth[a]
No annealing	< 5 nm
10 min @ 800 °C	~ 20 nm
30 min @ 850 °C	> 30 nm
20 min @ 900 °C	~ 150 nm

[a] The simulations were performed with Taurus TSUPREM-4™ [56].

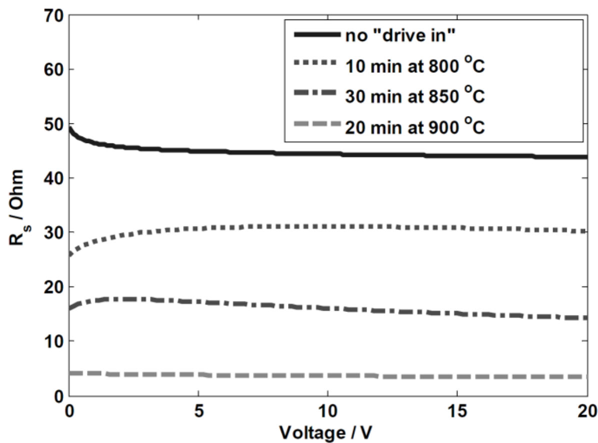


Fig. 2.11: Measured PureB diode series resistance with different post-thermal annealing recipes versus reverse bias voltage (the R_s is measured by an impedance analyzer at 1 MHz.) [53].

PureB electron detectors

The basic PureB detector fabrication process is described in Appendix B. Here we shall briefly discuss two different diode designs as shown in Fig. 2.12. The cross-section of two adjusted detector segments is also shown in Fig. 2.13. For more details, readers are referred to [10].

In Fig. 2.12, design (a) presents a PureB backscattered electron (BSE) detector with a diameter of 8 mm located inside a 10 mm × 10 mm die. This detector is composed of eight segments that are joined in different combinations during operation in Scanning Electron Microscope (SEM) systems [21, 48, 49]. One example is the concentric backscattered (CBS) mode, where eight segments are grouped in four concentric rings as shown in Fig. 2.12b. Design (b) is also used for electron detection with a total detector diameter of 19 mm located inside a 20 mm × 20 mm die. This detector consists of six symmetric sectors as shown in Fig. 2.12c.

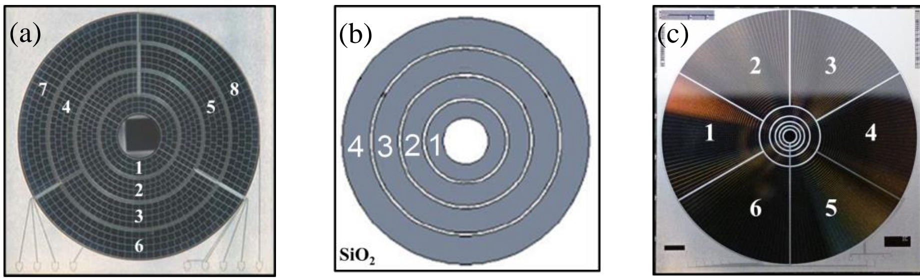


Fig. 2.12: (a) Photograph of the PureB BSE detector with eight segments [21]. (b) CBS combination of the PureB BSE detector segments in four concentric rings [21]. (c) Photograph of another PureB electron detector with six symmetric sectors. *Photograph in Fig 2.12c is provided by Iszgro Diodes BV.*

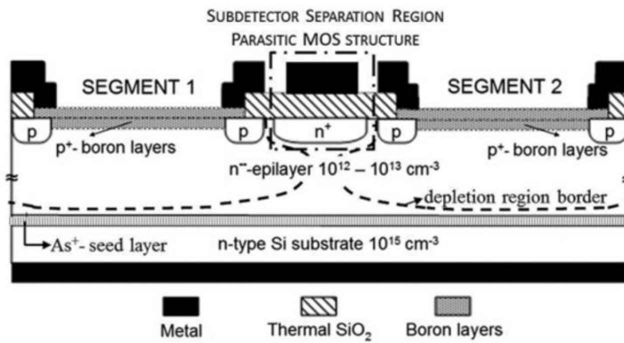


Fig. 2.13: Cross-section of adjacent diode segments of the PureB detector, indicating the separation region between them [21].

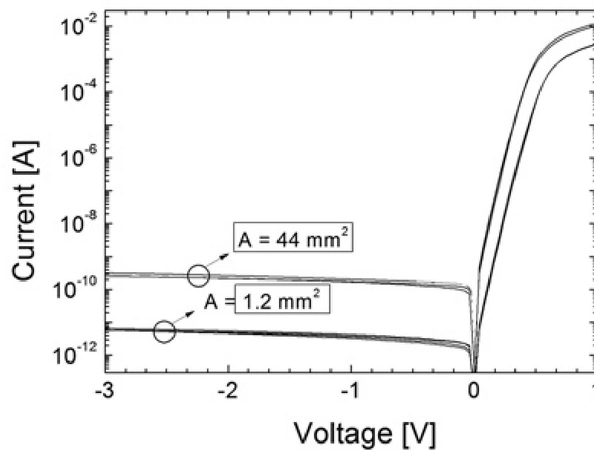


Fig. 2.14: Measured I-V characteristics of two photodiode segments of a PureB electron detector with a 1.8-nm-thick boron layer at different positions on the wafer with active anode areas of 44 mm^2 and 1.2 mm^2 [21].

Next, the performance evaluation is limited to the PureB BSE detector while both detectors are used to investigate the boron layer non-uniformities. Fig. 2.14 shows the measured I-V characteristics of two photodiode segments of the PureB electron detector shown in Fig. 2.12a. As can be seen in this figure, the photodiodes demonstrate an ideal behavior ($n \approx 1$), with the low dark current level corresponding to their active anode area, i.e. ~ 50 pA and ~ 0.2 nA for 1.2 mm^2 and 44 mm^2 active anode area respectively at -1 V bias.

To test the electrical stability of the PureB electron detectors during electron irradiation, the I-V characteristics of samples on a single wafer were monitored for several different exposures. The characteristics across the wafer before exposure are given in the wafer map in Fig. 2.15, where the values of the dark current recorded at 2.5 V reverse bias are shown along with the corresponding ideality factors [48].

An average dark current density of 0.595 pA/mm^2 was found with a standard deviation of only 0.089 pA/mm^2 across the wafer. The small spread in values is evidence that the boron layer provides a good Si coverage on all dies over the entire wafer, even for a boron layer thickness of only 1.8 nm. The overall behavior is ideal with a very narrow spread of the ideality factors of 1.02 ± 0.01 over the wafer. Subsequently, to evaluate the dark current stability of PureB photodiodes, the dark current was then measured after exposing the unbiased devices for 10 min to electrons with energies of 1 keV to 25 keV in the Philips XL50 SEM in scanning mode.

The I-V characteristics of the diodes exposed to 25 keV electrons (in the center) are shown in Fig. 2.16. As can be seen in this figure, the exposure in the center of the device did not modify the dark current, indicating that the boron layer junction is not degraded by electrons with energies up to 25 keV.

			58.2 1.03		52 1.03		
		50.9 1.02		49.1 1.03			
	54.5 1.02		63.2 1.00		62.3 1.01		63.4 1.02
55.7 1.02		48.9 1.03		45.1 1.02		45.3 1.02	
	46.7 1.03		46.4 1.02		42.7 1.00		59.8 1.02
		41.4 1.01		44 1.00		54.2 1.02	
	44.1 1.01		43.3 1.01		41.8 1.01		
		57.5 1.03		38.5 1.01			

Fig. 2.15: Over-the-wafer measurements of the dark current in pA at a 2.5 V reverse bias (upper number), and an ideality factor *n* (lower number) for the non-irradiated PureB electron detector with a 1.8-nm-thick boron layer [48].

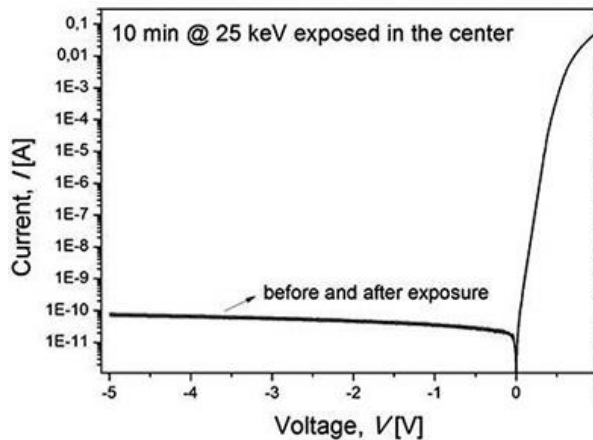


Fig. 2.16: The I-V characteristics of a photodiode before and after a 10-min electron irradiation at 25 keV when exposed in the center [48].

2.3.2 Optical characterization

PureB UV photodetector in the EUV spectral range

Fig. 2.17 presents the measured EUV responsivity of the PureB photodetectors with and without the post-thermal processing steps as described in Table 2.2 [24, 29, 51, 58]. In the figure a commercial n^+p photodiode with a 9-nm TiSi front window (IRD SXUV) and the theoretically attainable values for an ideal Si-based photodetector, are included for comparison [6].

Table 2.2: Description of the PureB photodetectors for EUV measurements in Fig. 2.17

Boron dep. time	Post processing steps		
	LPCVD oxide	*Thermal annealing*	*Other processes*
6 min	---	---	---
6 min	---	1 min @ 850 °C	300nm B-doped CVD Si
30 min	300 nm	20min @ 900 °C	Remove oxide/boron layer

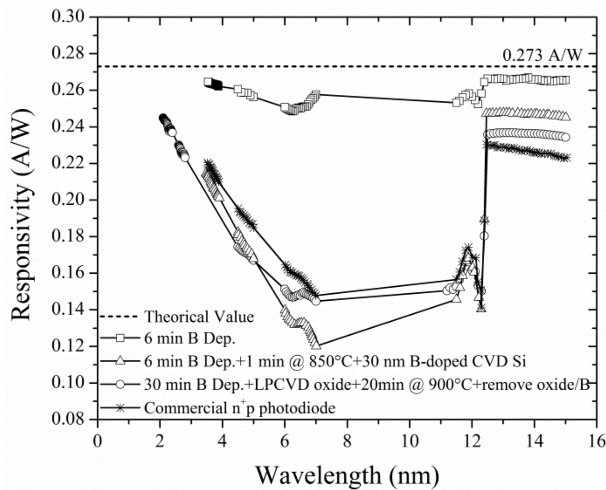


Fig. 2.17: Measured EUV spectral responsivity of PureB photodetectors described in Table 2.2. A commercial n^+p photodiode (IRD SXUV) and the theoretically attainable values for an ideal Si-based photodetector (dashed line) are also included for comparison [24, 29, 51, 58].

The photodetectors were characterized in three wavelength ranges: from 11.5 nm to 15 nm, which also includes the Si-L edge at 12.4 nm (100 eV); a range around the boron edge at 6.6 nm (188 eV); and above and below the carbon edge at 4.4 nm (284 eV).

The responsivity of as-deposited PureB photodetectors at the 13.5-nm wavelength measured is about 0.265 A/W, which is very close to that of an ideal lossless system (0.273 A/W, dashed line in Fig. 2.17) [24, 29, 51, 58]. This again confirms that the boron deposition process can provide ultrashallow, high quality, damage-free p^+-doped active surface layers which can minimize any quantum efficiency loss due to either recombination of photo generated carriers or absorption in the front window. This value dropped to 0.247 A/W (~ 7% drop) and 0.236 A/W (~ 11% drop) for the samples with the post-thermal processing step after boron deposition, i.e. *in-situ* annealing of 1 min 850 °C and 20 min 900 °C, respectively.

PureB UV photodetectors in the DUV/VUV spectral range

Fig. 2.18 shows the responsivity of a PureB photodetector compared with other commercially available state-of-the-art photodetectors in the DUV/VUV spectral range (wavelengths from 100 nm to 220 nm) [3, 38, 39, 52, 59]. This PureB photodetector was fabricated by a 6-min boron deposition which roughly formed a 2-3 nm boron coverage and less than 10 nm junction depth. The measured responsivity is in the order of 0.1 A/W or higher [59].

Moreover, as shown in Fig. 2.19, the VUV radiation is also absorbed intensively in the nm-thin boron layer. Compared to a 4-nm boron-covered PureB photodetector, the responsivity of a similar PureB photodetector with 12 nm of boron coverage shows a drop of more than 50% (from 0.09 A/W to less than 0.04 A/W at 193 nm). This confirms that the presence of any pre-absorption layers—e.g. a nm-thin boron layer, B-doped region or boron-silicide (B_xSi_y) layer, even ultra-thin—can act as a “dead-layer” and greatly reduce the photo response of the photodiode.

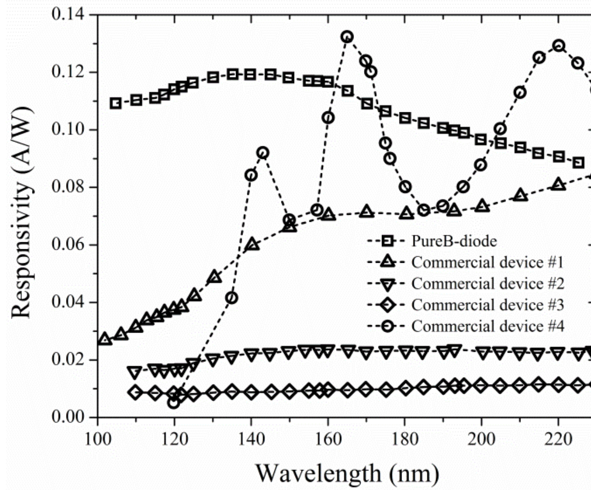


Fig. 2.18: Measured responsivity of PureB photodetectors in the DUV/VUV spectral range, compared with other state-of-the-art Si-based photodetectors. The measured B-photodetectors were fabricated at DIMES (junction depth: < 10 nm; boron layer: ~2 nm, measured by ellipsometry). The commercial devices labeled #1 to #4 are a SPD p^+n junction photodiode; an ETH PtSi-Schottky photodiode; an IRD SXUV n^+p junction photodiode; and an IRD UVG n^+p junction photodiode, respectively. [3, 38, 39, 52, 59]

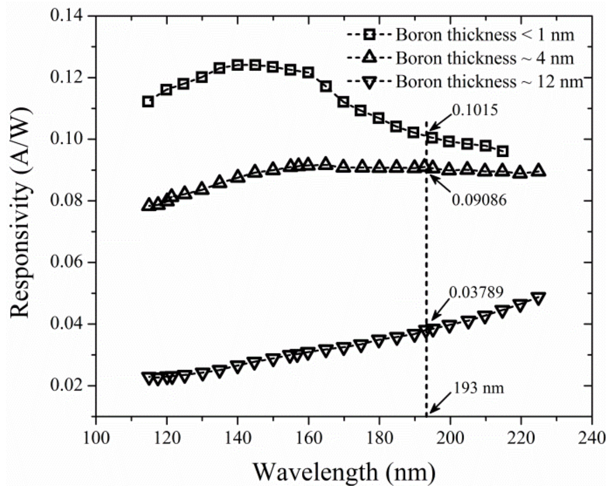


Fig. 2.19: Measured VUV/DUV responsivity of PureB photodetectors with different boron thicknesses on the diode's surface. The measured diode was fabricated at DIMES (boron thickness was measured by ellipsometry) [59].

PureB electron detectors

In Fig. 2.20 the relative electron signal gain is plotted as a function of the energy of the incident electron beam for PureB BSE detectors with 1.8-nm and 5-nm-thick boron layers, as indicated by P1.8B and P5B, respectively [48]. The electron signal gain, G_{ph}, is defined as I_{ph}/I_{beam}, where I_{ph} is the output current of the photodiode and I_{beam} is the current of the incident electron beam, assuming a negligible dark current. The other PureB electron detectors with different cap layers are also included in Fig. 2.20 for comparison. As can be seen at energies below 5 keV, there is a significant decrease in gain that follows the thickness of the layers covering the active Si region, while relative gain values of about 97% are reached for all the samples at energies around 10 keV. The influence of the inactive dead layers is clearly visible in this figure.

In Fig. 2.21, the PureB BSE detector with a 1.8-nm-thick boron layer (P1.8B) is compared to two commercially available detectors: a backscattered electron (BSE) detector and a “low Voltage high Contrast Detector” (vCD) detector, that are both currently used in SEM systems [48]. With such a thin front entrance window of only a 1.8-nm-thick boron layer, the PureB BSE detector achieves 60% of the theoretical gain value at 500 eV electron beam energy as compared to 14% for the BSE detector and 40% for the vCD detector [8].

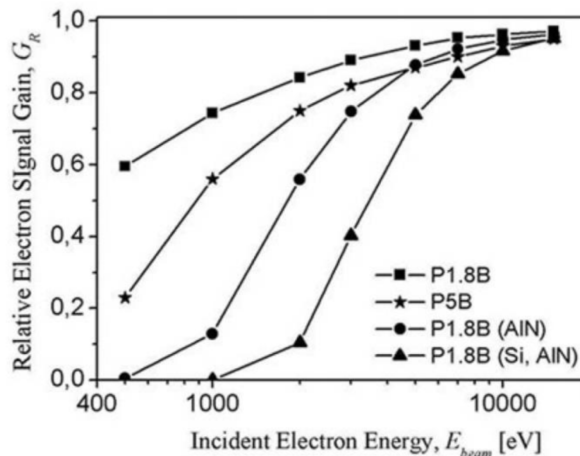


Fig. 2.20: Measured relative electron signal gain for the PureB electron detectors with only a boron layer entrance and other capping layers [48].

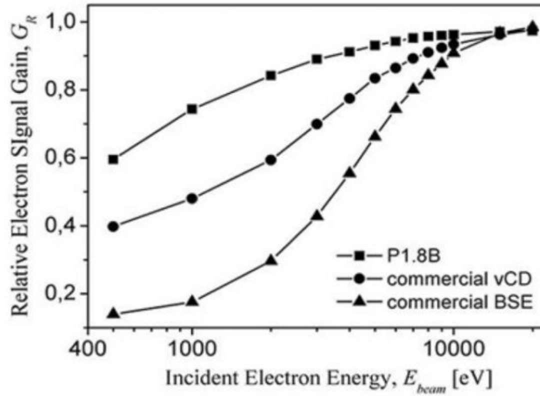


Fig. 2.21: Measured relative electron signal gain for the PureB BSE detector with a 1.8–nm-thick boron layer (P1.8B) and two commercially available photodiodes: a backscattered electron detector (BSE) and a low Voltage high Contrast Detector (vCD) [48].

Similarly, at 1 keV the gain reaches 74% of the theoretical value, which corresponds to an improvement of 4.1 and 1.5 times over the BSE and vCD detectors, respectively. A significant performance advantage is maintained up to almost 10 keV, at which point they all tend towards the 97% level. For higher energies, the electrons (as reported in [14]) will start to travel so deep into the Si that a much wider depletion region, i.e., a much more lightly doped Si, is needed to detect all of the incoming beam.

The electron detection efficiency of the PureB BSE detector (P1.8B) is measured as shown in Fig. 2.21 by employing the following equation (Eq. 2.1) in a SEM system using the electron gun as the source of electrons [21]. The measurement setup is described in more detail in [60].

$$\text{Detected Electrons /Incident Electrons} = \frac{I_{\text{ph}} - I_{\text{dark}}}{I_{\text{beam}}} \tag{2.1}$$

I_{ph} is the output current of the photodiode at 3 V reverse bias and is measured with an external picoampmeter during exposure of the device. I_{beam} is the input current determined for each measurement by directing the electron beam onto a Faraday cup. I_{dark} is the photodiode dark current, which can be neglected for electron energies above 1 keV in view of the fact that the value is typically a thousand times lower than the I_{ph}. Sub-keV electrons, on the other hand, generate a current comparable to the dark current of the diode, where the energy detection threshold depends on the dark current level.

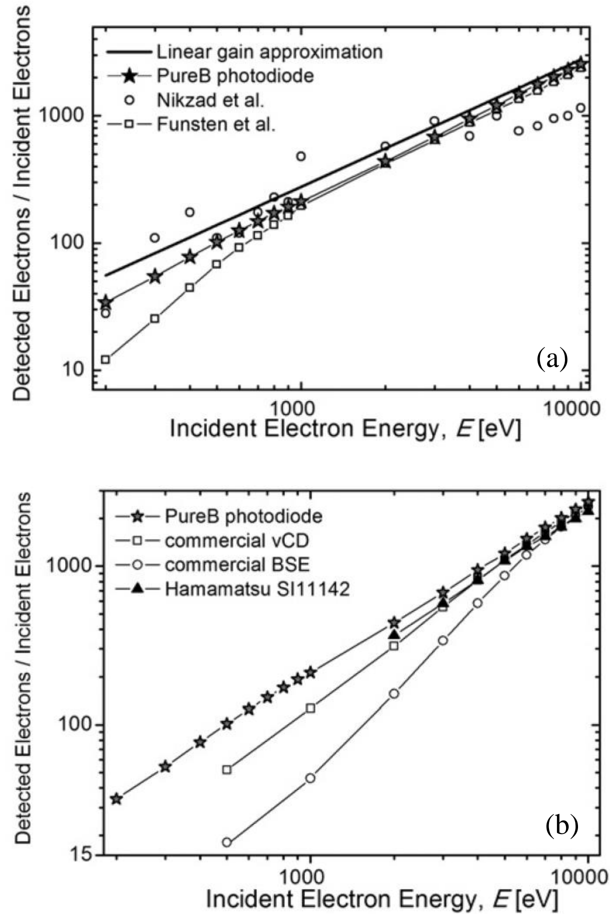


Fig. 2.22: Measured electron gain of the PureB BSE detector (P1.8B) compared to: (a) the data reported by Nikzad et al. [61], Funsten et al. [62], and theoretical electron gain; and (b) a commercially available BSE detector, a low Voltage high Contrast Detector (vCD), and a Hamamatsu SI11142 electron detector [21].

The theoretical electron gain is indicated in Fig. 2.22a by a solid line, which shows that the PureB BSE detector (P1.8B) clearly follows the theoretical trend. The gain reaches 92% of the theoretical value at 10 keV, 87.5% at 5 keV, 73% at 1 keV, and an unprecedented 60% at the lowest energy of 200 eV. Compared to the other electron detectors reported in the literature and also added to the graph, the PureB BSE detector shows a record high performance with reliable energy dependence. Moreover, when compared to commercial implementations of backscattered electron detectors (BSE) and low Voltage high Contrast Detectors (vCDs) as in Fig. 2.22b, the PureB BSE detector is clearly superior in

terms of detection efficiency. Several points are also added for the latest Hamamatsu SI11142 BSE detector, but the supplied data is only for energies above 2 keV [63]. At 2 keV, the PureB BSE detector performs at 80% of the theoretical efficiency, while this is somewhat lower at 65% for the SI11142.

2.4 Drawbacks and limitations of state-of-the-art PureB detectors

Besides the impressive aforementioned properties of the PureB UV and low energy electron (photo)detectors, there are some important drawbacks that affect the performance of these devices, which will be discussed next.

2.4.1 Boron layer thickness non-uniformity

As we will discuss in detail in Chapter 4, the conventional HT boron layer (deposited at 700 °C) is subjected to undesirable boron layer thickness non-uniformity as can be clearly seen in the Fig. 2.23, where the 2D map of the boron layer relative thickness variation of the (10×10) mm^2 VUV photodiode and PureB electron detectors is given. These non-uniformities observed are similar to those found for selective epitaxial growth (SEG) of Si and SiGe layers [64-66]. As can be seen in the Fig. 2.23, the boron layer is thicker when it is adjusted to a larger oxide area. These non-uniformities introduce some imperfections to the performance of the PureB detectors especially when they are employed for low penetration beam detection.

2.4.2 Non-uniformity of the response

As shown in Fig. 2.19 and Fig. 2.20, the VUV radiation and low energy electrons (less than 1 KeV) are absorbed intensively in the nm-thin boron layer, which makes the responsivity of the PureB detectors very sensitive to any sub-nanometer variation of the boron layer thickness. Hence, the DUV/VUV responsivity measurements and the low energy electron measurements can be used as a good indicator of the uniformity of the boron thickness on the photodiode surface. Fig. 2.24 presents the responsivity uniformity of PureB photodetectors across the active region in two directions (vertical and lateral)

with different nominal boron layer thicknesses, exposed to VUV light at a 193-nm wavelength [53].

Obviously, a better uniformity is achieved when the boron layer is thinner. However, as we will mention next, boron coverage that is too thin may lead to incomplete boron layer coverage that reduces the reliability of the boron layer as a protective barrier, increasing the probability of oxidation of the diode surface and potentially affecting the performance stability of the photodiodes.

Similar non-uniformity of the PureB detectors can also be seen in Fig. 2.23 by measuring the output current (I_{ph}) when they are exposed to low energy electrons. These non-uniformities are unacceptable especially for the applications which demand a uniform response over the entire active region, such as the aforementioned UV and electron detectors.

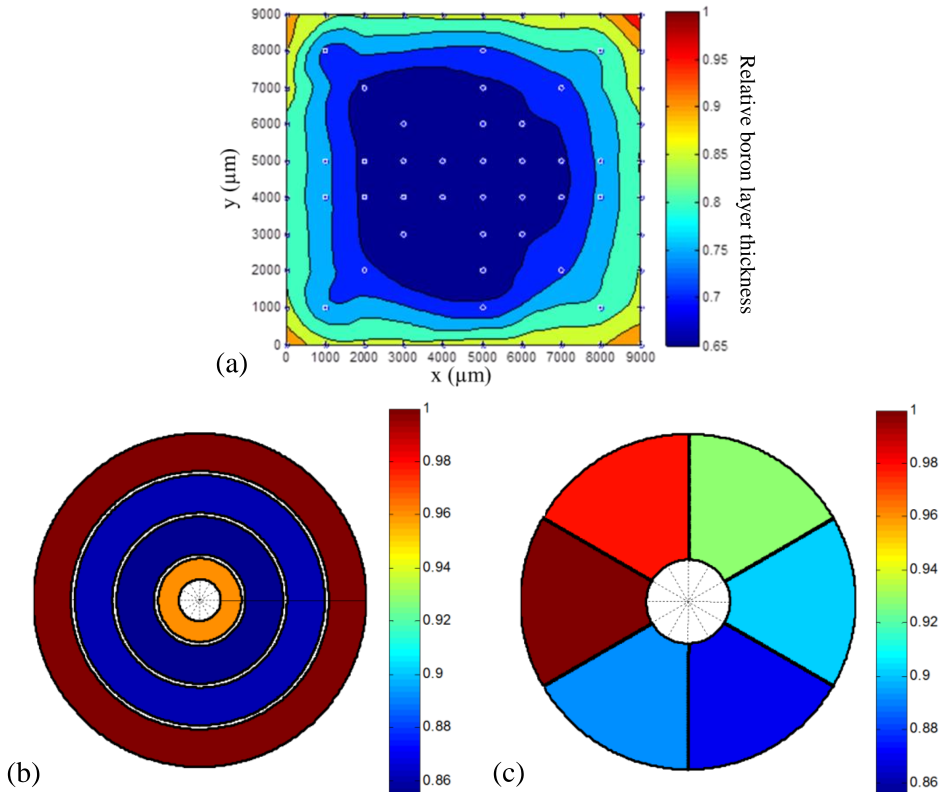


Fig. 2.23: 2D map of boron layer relative thickness: (a) over the entire active area of a large (10×10) mm^2 VUV photodiode; (b) and (c) of the two different designs of the electron detectors. The contour plots are extracted from 1 keV E-beam measurements [60].

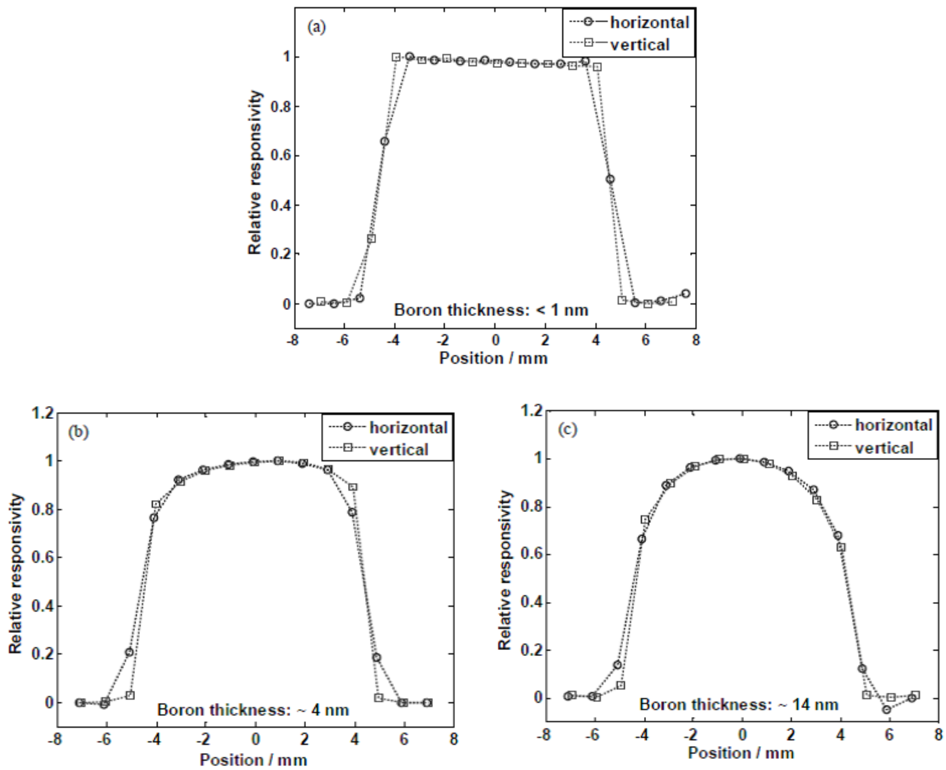


Fig. 2.24: Responsivity uniformity of PureB photodiodes with a (1×1) cm^2 anode area, at a 193-nm wavelength. The boron layer thickness was measured by ellipsometry [53].

2.4.3 Reliability of the boron layer as an aluminum barrier

Fig. 2.25 shows SEM images of the silicon surface after boron deposition followed by pure Al deposition, alloying at 400 °C, and selective removal of the aluminum [48]. This SEM inspection is sufficient to conclude that a longer deposition is instrumental in forming a uniform and continuous boron film that functions as a reliable barrier layer. Therefore this imposes a trade-off between the maximum detection efficiency and spatial uniformity, i.e. boron layer that is as thin as possible, and the reliability of the boron layer coverage of the Si surface, i.e. a barrier layer for spiking between Si and pure Al. This limitation can be exacerbated when there is a significant non-uniformity of the boron layer over the entire wafer, and even inside a single die between different

segments/sectors, as can be seen in Fig. 2.23. This variation, in some cases, can be in the range of few nanometers, which is not acceptable for low penetration beam detection, as we discussed above.

2.4.4 Surface presence of undesired oxide amounts

Optical and physical measurement results confirm the presence of an undesired amount of oxide components on the surface of the tested PureB photodiode samples, when thin boron coverage is formed. Table 2.3 presents the ellipsometry-measured oxide components on the photodiode surface of the fabricated PureB photodiode. The results also show that the oxide presence tends to be lower with increased boron layer thickness. A similar result was found with an X-ray Photoelectron Spectroscopy (XPS) measurement: the SiO_x component was measured on the surface of photodiode #2, which is shown in Table 2.3. Since no boron oxide was detected on the diode surface by the XPS test, we can conclude that the boron layer itself is not oxidized after boron deposition.

The UV optical measurement results also show the presence of an "oxygen" element in the surface layer stack of PureB photodiodes. For example, as illustrated in Fig. 2.26, a measured EUV responsivity undulation around the oxygen absorption edge ($\lambda \approx 2.3$ nm) indicates an oxide component on the surface of photodiode #2 and photodiode #3 (presented in Table 2.3) [52]. However, the undulation is too small to determine the exact oxide content.

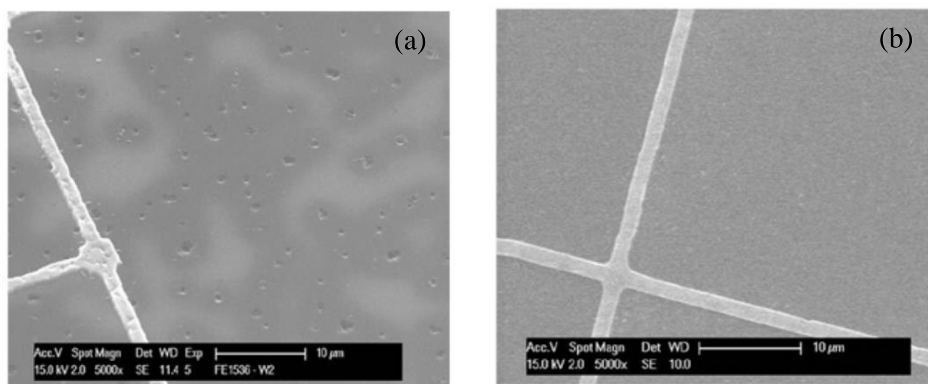


Fig. 2.25: SEM images of the silicon surface for the sample with a boron layer thickness of (a) around 1 nm and (b) 4 nm, after pure Al deposition, alloying at 400 °C, and selective removal of the Al [48].

Table 2.3: Measured by ellipsometry presence of oxide in the surface layer stack of PureB photodiodes with different boron thicknesses.

Photodiode	Boron layer thickness (nm)	Measured oxide thickness (nm)
#1	< 1 nm	5 ~ 6 nm
#2	4 nm	3 nm
#3	12 nm	1 ~ 1.5 nm
#4	14 nm	< 1 nm
#5	15 nm	No measurable oxide

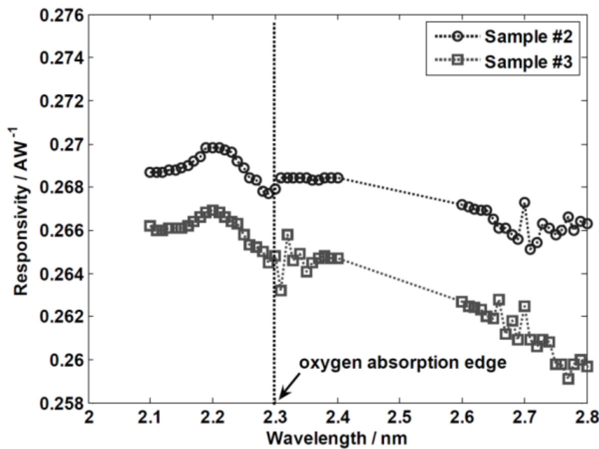


Fig. 2.26: Monitored responsivity undulation around the oxygen absorption edge (λ ≈ 2.3 nm) of PureB photodiodes for photodiode #2 and photodiode #3, which are presented in Table 2.3 [52].

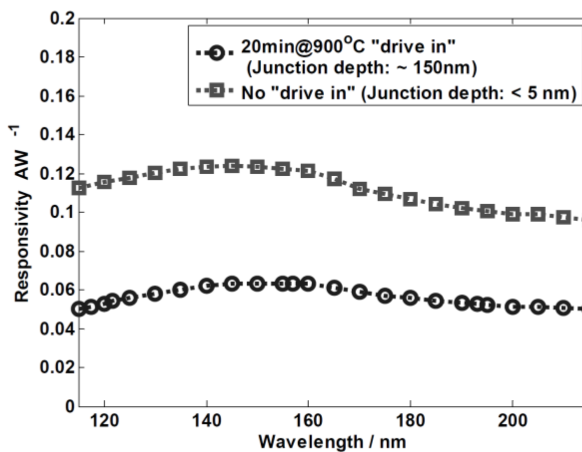


Fig. 2.27: Responsivity of PureB photodiodes with different junction depths obtained with annealing step after boron deposition [52, 67].

2.4.5 Poor tolerance to post-deposition thermal steps

As discussed above, the responsivity of the conventional PureB photodiodes is deteriorated by the extra thermal processing steps such as the annealing (drive-in) step. Such extra thermal processing can be necessary, for example, to reduce the photodiode series resistance [68] from the as-deposited 10 kΩ/sq to a few hundred Ω/sq, or to make the integration in a front-end CMOS process flow feasible. The reduced responsivity can be seen in the EUV responsivity shown in Fig. 2.17, as well as VUV response of Fig. 2.27 where the EUV/VUV response for PureB photodiodes with and without the *in-situ* annealing step is presented [52, 67].

2.4.6 Stability of conventional PureB photodetectors

As shown in Fig. 2.28, PureB photodetectors with lower parasitic surface oxide content show better optical performance stability [52, 53]. The samples correspond to the samples presented in Table 2.3.

Fig. 2.29 shows the measured VUV responsivity degradation of PureB photodetectors with and without the post-thermal processing step [53]. As can be seen, the as-deposited PureB photodiode (junction depth < 10 nm) demonstrates better stability, ~ 40%, than the sample with a deeper junction with 20-min annealing at 800 °C (junction depth > 30 nm). The same phenomenon has also been observed in the EUV spectral range.

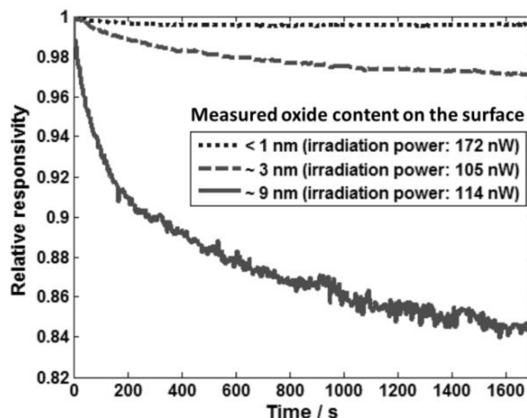


Fig. 2.28: Monitored responsivity degradation of conventional PureB photodetectors with varying parasitic oxide content on the surface as presented in Table 2.3, at a 121-nm wavelength. The oxide content was measured by ellipsometry on PureB photodiodes with a (1×1) cm^2 active area, and is expressed as a thickness in nanometers [52, 53].

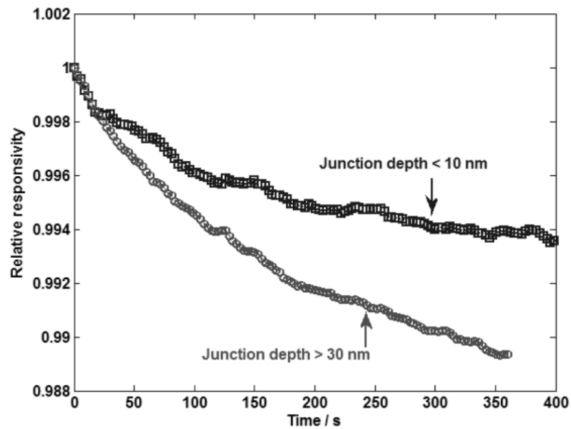


Fig. 2.29: Monitored responsivity degradation at 70-nm wavelengths of two conventional PureB photodiodes with and without 20-min annealing at 800 °C as a post-thermal processing step [53]. Photodiode with deeper junction shows ~ 1.1% responsivity drop in 400 sec exposure.

2.4.7 CMOS compatibility

As discussed above, conventional PureB technology is employed to fabricate state-of-the-art PureB UV photodiodes. Therefore due to the relatively high temperature of the deposition (500 °C – 700 °C) of this technology, at the moment it is difficult to fully integrate it in standard IC/CMOS processes. However, this technology has an inherent potential to achieve standard IC/CMOS compatibility if a reliable boron deposition process can be developed at a lower temperature (LT), for example at 400 °C, which could provide a device performance similar to the ones based on the conventional 700 °C PureB process. This gives a chance to fully integrate the LT PureB photodiodes together with electronic interface circuits and other sensors on a single chip. In this way, smart sensor systems or even CCD or CMOS UV imagers can be realized.

As a result of this thesis, a novel technology for boron deposition at low temperature (400 °C) deposition processes has been developed. This technology will be presented in Chapter 5. By employing this technology, a DUV/VUV/low energy electron Si photodiode has been fabricated which is presented in Section 6.2.

2.5 Summary

In this chapter a short overview of the state-of-the-art PureB Si-based detectors, with applications in the ultraviolet (UV) spectral range and also for low energy electron detection, are given together with a brief performance comparison with the other commercial available devices. It has been found that PureB detectors demonstrate a superior performance with respect to sensitivity, stability, simplicity, and cost. Due to the impressive properties of PureB detectors, this technology was made commercially available for lithography machines and SEM systems. Based on the reported state-of-the-art PureB UV photodiodes and PureB electron detectors, their advantages and drawbacks are evaluated.

From the discussion in this chapter it can also be concluded that an improvement of the PureB technology is required in two aspects:

- First, regarding the optical performance, particularly the spatial non-uniformity of the response to low energy beams, the current conventional HT PureB technology needs to be optimized. Such non-uniformity is unacceptable, especially for applications demanding a uniform response over the entire active region, such as the aforementioned UV and electron detectors.
- Second, the current PureB technology is limited to the deposition temperature range from 500 °C to 800 °C, which makes this technology incompatible to standard CMOS processes.

To solve the above-mentioned problems, in this thesis the loading effect and the pattern dependency of the HT boron deposition is investigated and an analytical kinetic model is developed to predict the deposition intensity. Altogether, with adjusting some process and layout parameters, the existing technology is optimized to deliver a significantly improved PureB detector performance, as described in Chapter 4.

It has been shown that a CVD of boron on silicon can be realized at temperatures lower than 500 °C. A low temperature pure boron (LT PureB) CVD process at 400 °C is proposed and implemented, which provides PureB detectors with the same electrical and optical properties as the ones produced with the HT PureB process, as described in Chapter 5.

Chapter 3

An analytical kinetic model for boron CVD deposition

In this chapter, an analytical kinetic model is proposed which describes the deposition kinetics and the deposition chamber characteristics that determine the pure boron (PureB) deposition rate from diborane (B_2H_6) over the wafer. In addition to the theoretical considerations, the operation of two different reactor types of ASM Epsilon One and 2000 are experimentally studied. The proposed model is shown to be potent enough to predict the rate of boron deposition on non-rotating bare silicon wafers for both reactors. This is very useful for transferring recipes from one reactor to the other.

This model takes into consideration most important factors: i.e. the gas phase diffusion mechanism of the diborane species through the stationary boundary layer over the wafer, the gas phase processes and the related surface reactions. To develop the model, the actual parabolic gas velocity and temperature gradient profiles in the reactor which were calculated theoretically and also simulated with the commercial FLUENT® software is applied. In the following sections the derivation of the analytical kinetic model is discussed in detail.

3.1 Definition of the reactor system

In order to achieve better control of the boron deposition from diborane (B_2H_6) and a better understanding of the associated kinetics, the deposition mechanism and growth characteristics need to be described. A CVD process involves several steps essentially composed of the reactant transfer in the gas

phase and the chemical reactions at the substrate surface [69]. Therefore, the presented investigation considers fundamental aspects of the chemical thermodynamics, the transport phenomena in the gas phase, as well as the chemical kinetics of the deposition reaction.

Various theories have been proposed to describe the transport phenomena in CVD reactors [70-78]. Most of these theories model the epitaxial growth of Si and SiGe layers, and they can be divided into two main groups. The first group includes models that have been developed based on the boundary layer theory and only consider the physical diffusion effects [70, 77]. The second group encompasses models that consider the surface reactions [71-76, 78]. Since in CVD reactors the boundary layer is stationary or, at most, moving slowly, the input value of the partial pressure of the reactants cannot be upheld throughout the chamber. Moreover, the design of the chamber (the height and width of the chamber, the size of the susceptor, etc.) can also have an influence on the deposition and the final deposition/growth-rate of the layer. For modeling that is detailed enough to be predictive, it is necessary to consider both the physical phenomena and the reaction processes in relation to the specific reactor design. The lack of modeling that takes both aspects into account meant it was necessary to empirically calibrate each type of reactor with respect to the deposition rate.

In Fig. 3.1 a schematic illustration is shown of the chemical and physical CVD chamber geometry that we use in our model. The experimental work on which the modeling is based was performed in two different systems: the ASM Epsilon One and 2000, which have two different reactor designs. In the model, the reactor height, h, is constant and approximately equal to 22 mm, and the width, b, is much larger than h. The aspect ratio, $h/b \approx 0.085$, is therefore so small that we can consider this reactor to be a two-dimensional system with sufficient accuracy. In these systems, the susceptor[1], lies at the bottom of the chamber as shown schematically in Fig. 3.1 and Fig. 3.2. The susceptor is heated up and held at a deposition temperature, T_s, by an assembly of lamps. This heat is transferred to the gas flowing over the susceptor, whereas the temperature of the upper wall (T_w) is much cooler than the susceptor; we have assumed its temperature to be T_0. Moreover, we have assumed that the inlet

[1] where the wafer placed on (see Fig. 3.2)

temperature of the gases is room temperature. Therefore, a large temperature gradient exists over the height of the reactor. This is visualized by FLUENT® simulations in the following section.

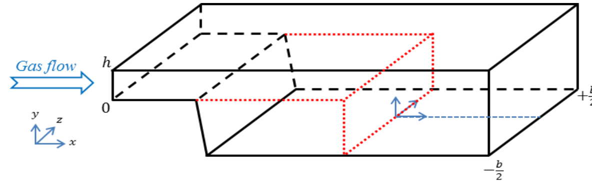


Fig. 3.1: Schematic illustration of the CVD reactor geometry used for modelling purposes. The red-dotted line represents the susceptor. More details are shown in Fig. 3.2.

Deposition conditions are chosen for which the reactant (B_2H_6) concentrations can be assumed to be much smaller than the concentration of the carrier gas (H_2). From this it follows that the gas flow and temperature profiles are completely determined by the physical constants of the carrier gas. The overall flow velocity and temperature gradients are chosen in such a way that the Reynolds number, Re, satisfies the condition for laminar flow in the reactor [79]. However, at the same time the velocity is chosen just high enough for the transport in the flow direction to be completely dominated by forced flow; i.e., we neglect diffusion along the axes of the reactor system. These effects will, however, be discussed later in connection with the experimental results presented in Section 3.6. End effects in flow and temperature are not taken into account so the profiles of the velocity and temperature are fully developed.

The starting point for developing a mathematical model for the chemical and physical behavior of the CVD process is an expression for the temperature, T, and velocity profile for a fully developed flow which can be calculated by solving the equation for energy conservation, the continuity equation and the equation of motion for the carrier gas:

$$c_g \rho_g u_x \frac{\partial T}{\partial x} = \frac{\partial}{\partial x}\left(\mathrm{k}_0 T^{\beta} \frac{\partial T}{\partial x}\right) = 0 \tag{3.1}$$

$$\frac{\partial}{\partial y}\left(\mu_0 T^{\gamma} \frac{\partial u_x}{\partial y}\right) = \text{constant} \tag{3.2}$$

Here, $u_x(y)$, x, y, c_g, ρ_g, $\mu_0 T^{\gamma}$, and $k_0 T^{\beta}$ are: the gas velocity profile, axial position in the direction of the gas flow, vertical position perpendicular to the direction of the gas flow, heat capacity of the carrier gas at constant pressure, density of the carrier gas, temperature-dependent thermal conductivity, and dynamic viscosity of the carrier gas, respectively. The constants β and γ are approximately equal to 0.7 [80, 81].

The solution of Eqs. (3.1) and (3.2) leads to a distorted parabola with a maximum shifted towards the colder part of the reactor for the gas velocity profile, $u_x(y)$, and a gradually decreasing temperature above the susceptor for the temperature profile, $T(y)$, (Eq. 3.3), which are confirmed by the simulation presented in Section 3.2.

$$T(y) = \left[T_s^{1+\beta} - \left(T_s^{1+\beta} - T_w^{1+\beta}\right)\frac{y}{h}\right]^{\frac{1}{1+\beta}} \tag{3.3}$$

T_s and T_w are the temperatures of the susceptor and upper wall, respectively.

Consequently, the velocity of the gas molecules deviates at the gas boundaries where there is a vertical diffusion of the gas molecules. This effect was also considered in the implementation of the model. Lastly we assume that adsorption of the gas phase species only occurs on the substrate placed on the hot susceptor and not on the cold upper wall of the reactor. A balance between adsorption and subsequent deposition is established to produce the boron layer and/or doping of the substrate.

3.2 Simulation of the EPI reactor

In this section, for better understanding of the chamber parameters, the gas flow and the heat transfer in the ASM Epsilon 2000 CVD reactor which was defined in the previous section, are numerically simulated by using the Gambit software and the commercial CFD package of FLUENT© for boron depositions at 700°C with different reactor conditions, i.e. the atmospheric (ATM) pressure, susceptor rotation speeds of 0 rpm, 10 rpm, 20 rpm and 35 rpm (rotation per minute), and gas flow rates of 25 slm, 20 slm and 15 slm (standard liters per minute) [82]. The results of this simulation are employed to develop an analytical kinetic model to predict the deposition rate of boron layers.

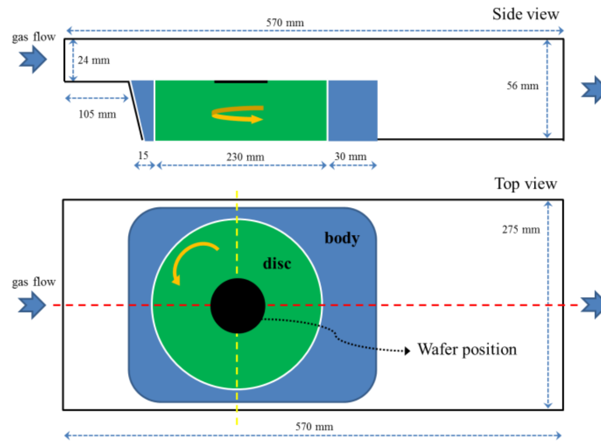


Fig. 3.2: Schematic of the ASM Epsilon 2000 CVD reactor geometry.

In Fig. 3.2 a schematic illustration is shown of the ASM Epsilon 2000 CVD reactor which is used in the simulation geometry, along with its dimensions.

The susceptor consists of two parts: a susceptor disc and a body. The wafer is placed in a pocket located at the middle of the susceptor disc and is rotated at a given speed depending on the recipe. The body is the stationary part of the susceptor around the disc. The susceptor is heated up and held at deposition temperature by an assembly of lamps from top and bottom. Part of this heat is transferred to the gas flowing over the susceptor, while the temperature of the upper wall is much cooler than the susceptor. Moreover, we have assumed that the gases have a room inlet temperature. The deposition conditions are chosen such that the reactant (B_2H_6) concentrations can be assumed to be much smaller than the concentration of the carrier gas (H_2). From this it follows that the gas flow and the temperature profiles are completely determined by the physical constants of the carrier gas.

Numerical simulation

The mathematical model for the simulations can be described by the governing three-dimensional (3D) partial differential equations: the equation of conservation of mass (continuity equation) (3.4); of momentum (Navier-Stokes equation) (3.5); and of energy (3.6):

$$\nabla . \vec{u} = 0 \tag{3.4}$$

$$\rho_0\left(\frac{\partial\vec{u}}{\partial t}+\vec{u}.\nabla\vec{u}\right)=-\nabla p+\mu\nabla^2\vec{u}+\rho\vec{g} \tag{3.5}$$

$$\rho_0 C_\mathrm{p}\left(\frac{\partial T}{\partial t}+\vec{u}.\nabla T\right)=k\nabla^2 T \tag{3.6}$$

where $\vec{u}$ is the velocity vector. p, T, t and g represent: the pressure, temperature, time and an external force, respectively. Physical properties such as density (ρ), viscosity (μ), heat capacity (C_p), and thermal conductivity (k) are defined for hydrogen. Subscript 0 denotes the reference state. The buoyancy force is calculated by the Boussinesq approximation with the volume expansion coefficient (β) calculated from the ideal gas law, as follows:

$$\rho=\rho_0\big(1-\beta(T-T_0)\big) \tag{3.7}$$

Simulations were performed using GAMBIT and FLUENT© software [83]. The 3D geometry of Fig. 3.2 was first modeled in GAMBIT and meshed using the Cooper Scheme as an unstructured 3D meshing tool. The results can be seen in Fig. 3.3 with, in total, 180049 Hexahedral cells in the 3D domain.

Then the CFD package of FLUENT© was used to solve the equations for the steady-state case and compute the results. The SIMPLE algorithm was used as a solver. The first-order upwind differencing scheme was used to discretize momentum and energy terms and the convergence criterion of 1×10^{-5} for continuity and velocity components, and of 1×10^{-6} for energy, which are considered to be satisfactory.

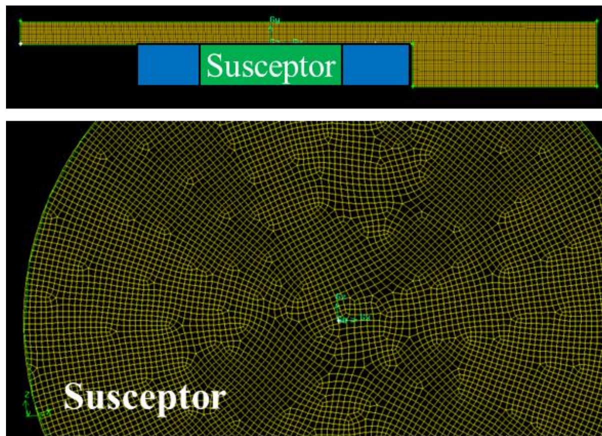


Fig. 3.3: 2D meshed structure of reactor geometry (top) side view and (bottom) susceptor disc.

Simulations were then performed using boundary condition of Eq 3.10 (Section 3.3) and for a susceptor temperature of 700°C with different disc rotating speeds of 0 rpm, 10 rpm, 20 rpm and 35 rpm and gas flow rates of 25 slm, 20 slm and 10 slm, which correspond to velocities of 6.1 cm/s, 5.1 cm/s and 3.8 cm/s, respectively. In order to establish the efficacy of the susceptor system, full 3D simulations are carried out.

Results and discussion

The uniformity of the boron layer deposited by this CVD reactor depends, on the one hand, on the uniform distribution of the substrate temperature, and on the other hand, on the flow velocity pattern uniformity near the substrate. Fig. 3.4 shows temperature distributions inside the reactor for different gas flow (slm) and susceptor rotation speed (rpm) conditions as specified in the figure. The distributions presented in (a), (b) and (c) are 3D illustrations and 2D cross-sections of the middle plans in the direction of the gas flow and perpendicular to the gas flow, respectively.

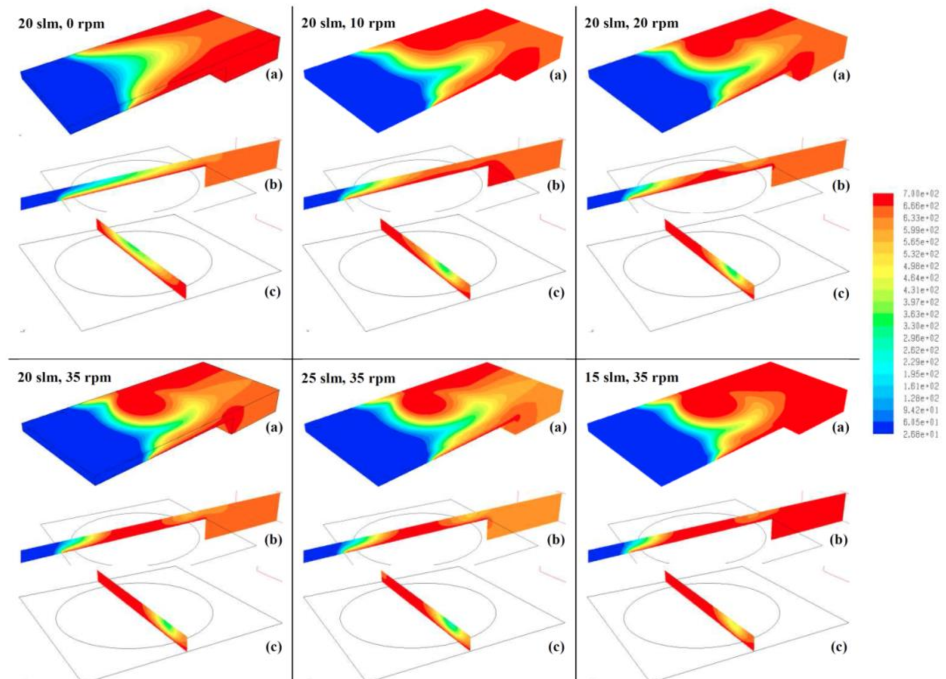


Fig. 3.4: (a) 3D and 2D middle plane, (b) in the direction of gas flow, and (c) perpendicular to the direction of the gas flow of the temperature distribution inside the reactor for different slm and rpm conditions, as indicated in the figure.

At zero rpm (stationary susceptor) a thermal boundary layer created over the susceptor is clearly visible ("20 slm, 0 rpm" b and c in Fig. 3.4). Under this condition the temperature profile is also symmetrical in the perpendicular plan to the gas flow with a vertical gradient, as can be seen in Fig. 3.4 "20 slm, 0 rpm" (c). This condition is not desired due to a very narrow thermal boundary layer, with the temperature of deposition over the susceptor significantly limiting the number of active precursors for deposition. By rotating the susceptor the temperature distribution becomes increasingly more uniform, allowing for the thermal boundary layer to expand vertically over the susceptor where the wafer is located. This can be seen by comparing the thermal distributions of Fig. 3.4 with different rpms at the same slm. It can be concluded that the temperature distribution becomes more homogenous at higher susceptor rotation speeds.

Fig. 3.5 shows the gas flow profiles determined by 3D numerical simulations for different rpms and slms as indicated in the figure. It can be seen that at zero rotation, the gas flow is laminar and dominated by forced convection. Rotation of the susceptor disc causes a gas rotation due to the frictional force between them and makes a cylindrical disturbance. This disturbance somehow facilitates the transportation of the reactant precursors to the substrate while at the same time introducing a gas velocity gradient over the substrate, as can be seen in the counter plots presented in Fig. 3.5 (b) and (c). This gradient is increased with rising susceptor rotation speed. The direction of the gas rotation and velocity gradient is clearly visible in Fig. 3.6 where the gas velocity vectors are presented. Besides cylindrical disturbance, the gas flow is still laminar and flows with forced convection. Therefore the intermingling due to free convection can be negligible. The return flow of heated gas occurring at the leading edge of the hot susceptor is also visible in all cases in Fig. 3.5. Gas phase diffusion inside the reactor is investigated in [84]. Investigating the images given in Fig. 3.5 results in the conclusion that the gas velocity over the susceptor disc is mainly defined by rpm, while the gas flow (slm) can control the height of the stagnant gas phase boundary layer, as described in [84]. Both these parameters have an impact on the uniformity of the boron deposition.

In conclusion, this section investigated temperature distributions and gas velocity profiles inside the reactor for different conditions. It has been found that the gas flow (slm) controls the height of the stagnant boundary layer, and rotating the susceptor disc provides more homogenous temperature distribution

while causing an increase in the gas velocity gradient over the susceptor. This in turn can cause non-uniform deposition.

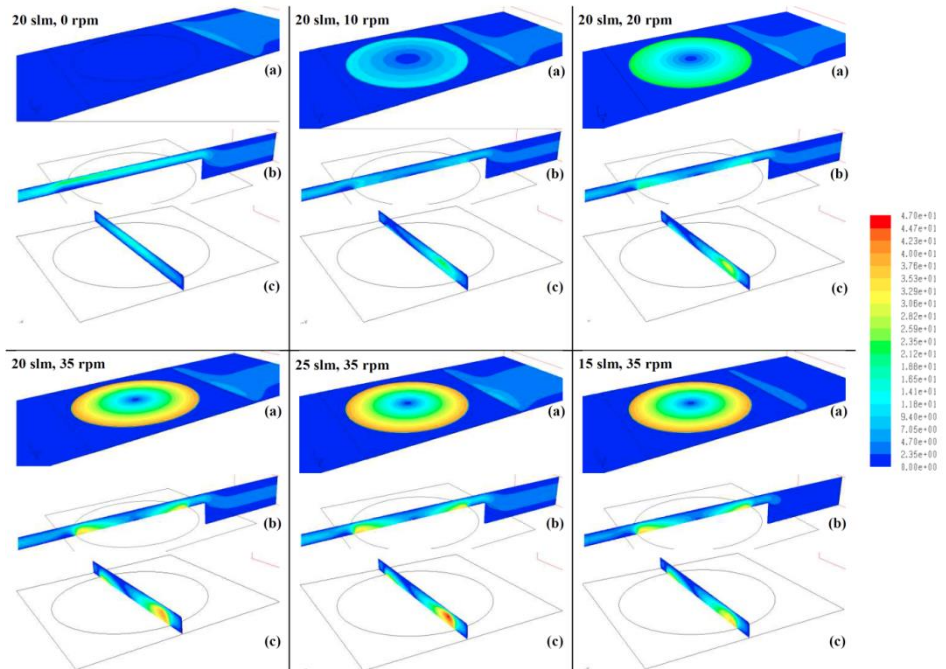


Fig. 3.5: (a) 3D and 2D middle plane, (b) in the direction of gas flow, and (c) perpendicular to the direction of the gas flow, of the gas velocity profiles inside the reactor, for different slm and rpm conditions, as indicated in figure.

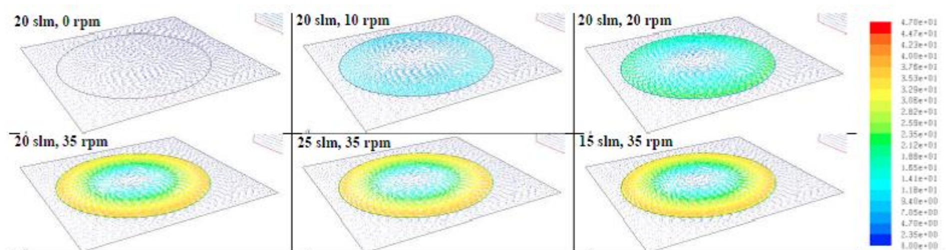


Fig. 3.6: Gas velocity vectors for different slm and rpm conditions, as indicated in figure.

3.3 Concentration profile model

In this section a model is developed for the concentration profile of the reactant species when the deposition is controlled by diffusion of the reactants through a laminar flow inside the horizontal chamber of the ASM Epsilon One CVD reactor. In this case the deposition process is limited by mass transport in the gas phase. The main idea of the model is to develop the concentration profile by taking into account the diffusion mechanism of the diborane species through the stationary boundary layer over the wafer and by applying the actual parabolic gas velocity and temperature gradient profiles inside the 2D reactor system.

In the following discussions, the gas flow is considered to be laminar and dominated by forced convection. This implies that intermingling due to free convection can be neglected. Return flow of heated gas may occur at the leading edge of the hot susceptor [85]. This is due to buoyancy forces caused by the expansion of the cold gases which hit the hot elements. This effect, which introduces additional mixing and memory effects, is also neglected in the present model.

Isothermal system

First we consider a system with a constant temperature, in which the active component rapidly decomposes at the susceptor, $y = 0$, for all axial flow positions $x \geq 0$ (Fig. 3.1and Fig. 3.7). Therefore, the concentration of the reactant species at $y = 0$ is zero across the entire decomposition zone. The transport of material towards the susceptor in the y-direction goes entirely via gas phase diffusion (laminar flow through the stationary boundary layer over the susceptor).

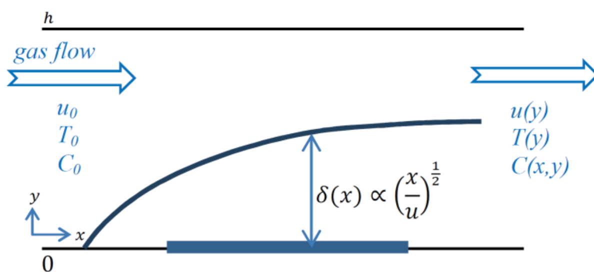


Fig. 3.7: Schematic illustration of a clasical boundary layer and reactor conditions over the susceptor.

The equation for mass conservation for this case is:

$$u(y)\frac{\partial C(x,y)}{\partial x} = D\frac{\partial^2 C(x,y)}{\partial y^2} \tag{3.8}$$

where C and D are the concentration profiles and the gas phase diffusion coefficient of the active component in the carrier gas, respectively. $u(y)$ is an expression for the parabolic velocity profile found by solving Eqs. (3.1 and 3.2) in the reactor chamber and is given by:

$$u(y) = 4u_0\left(\frac{y}{h} - \frac{y^2}{h^2}\right) \tag{3.9}$$

Equation (3.8) is difficult to solve for a parabolic velocity profile. Therefore, the problem is first solved for a constant flow velocity. Thereafter the influence of a parabolic flow profile on the obtained results is evaluated. For the case of a constant flow velocity (u_0) the problem can be solved analytically for the boundary conditions:

$$\begin{cases} C(x,0) = 0, & \text{for all } x \geq 0 \quad (3.10a) \\ \left.\dfrac{\partial C(x,y)}{\partial y}\right|_{y=h} = 0, & \text{for all } x \geq 0 \quad (3.10b) \\ C(0,y) = C_0, & \text{for all } 0 < y \leq h \quad (3.10c) \end{cases}$$

The second condition (Eq. 3.10b) is an expression of the fact that no mass transport is possible through the upper wall of the reactor. Following [86](24), the above problem can be solved, giving:

$$C(x,y) = \frac{4C_0}{\pi}\sum_{m=0}^{\infty}\left\{\begin{matrix} \dfrac{1}{(2m+1)}\sin\left(\dfrac{(2m+1)\pi}{2h}y\right) \\ \times\, exp\left[\dfrac{-(2m+1)^2\pi^2 D}{4h^2 u_0}x\right] \end{matrix}\right\} \tag{3.11}$$

In this equation, m is a summation integer.

In Fig. 3.8, concentration profiles at different positions, x, i.e., h^2u_0/D, have been drawn as calculated from Eq. (3.11). For small values of x the solution of Eq. (3.11) is equivalent to an error function for diffusion in a semi-

infinite medium. This holds until the concentration at $y = h$ falls significantly below C_0. For the following analysis the critical concentration for this to happen is defined as $0.99C_0$ (see Fig. 3.9).

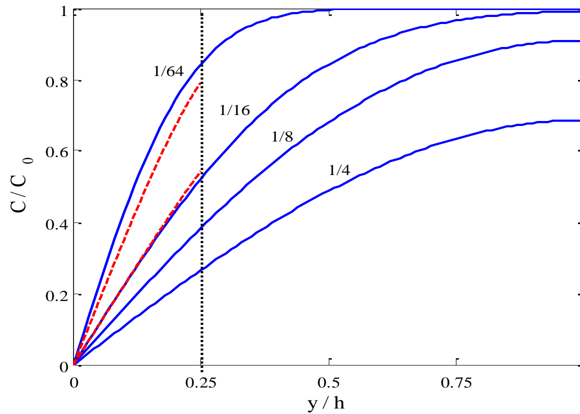


Fig. 3.8: Normalized concentrations calculated as a function of the axial position x in units of $\frac{h^2 u_0}{D}$, which is indicated along each curve. Solid line: concentration as a function of position above the susceptor in an isothermal cell with a capturing boundary at $y = 0$, for a constant gas velocity and temperature. Dashed line: concentration profile for $x_0 = \frac{h^2 u_0}{64D}$ and $x_0 = \frac{h^2 u_0}{16D}$ after correction for the linear velocity profile. Parameter of the figure is the axial position, x in $\frac{h^2 u_0}{D}$.

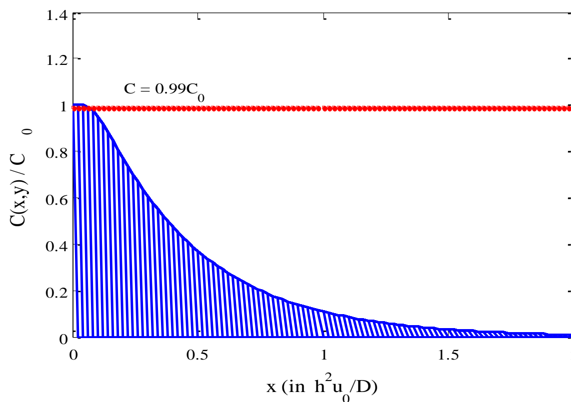


Fig. 3.9: Normalized concentration found from Eq. (3.11) versus axial position, x in $\frac{h^2 u_0}{D}$. The entrance length, x_0, where the $C(x,y) = 0.99C_0$, is also indicated.

The axial distance x_0 at which the concentration at $y = h$ reaches this value can be calculated from Eq. (3.11) as:

$$x_0 = \frac{h^2 u_0}{16D} \tag{3.12}$$

It appears that for higher values of x, only the first term in the summation of Eq. (3.11) has to be considered, as the series converges very rapidly. For these values of $x > x_0$:

$$C(x, y) = \frac{4C_0}{\pi} \sin\left(\frac{\pi y}{2h}\right) \exp\left(\frac{-\pi^2 D}{4h^2 u_0} x\right) \tag{3.13}$$

In Eq. (3.13), the gas phase depletion in the flow direction is represented by the exponential term. This equation also shows that the concentration profiles as a function of y have the same form for all values of $x > x_0$, as determined by the sine function. Therefore, the distance x_0 can be considered an entrance length for the concentration profile to develop in the reactor cell. For $x \leq x_0$ the concentration profile has to build up and is the same as in a semi-infinite medium; for $x > x_0$ the concentration profile has developed and remains the same form for all of x.

Solutions for the development region $x \leq x_0$ in a linear flow profile

Fig. 3.8 shows that in the development region $x \leq x_0$ the largest drop in concentration occurs in a relatively thin layer above the susceptor. Therefore, for calculation of the mass flux at $y = 0$, this part of the reactor represents the region of main interest. In Fig. 3.8, it can be seen that the main concentration drop occurs between $y = 0$ and $y = h/4$. In order to solve Eq. (3.8) in a more realistic way than the plug velocity approach given above, the parabolic velocity profile can be substituted by a linear velocity distribution, i.e.:

$$u(y) = 3.4u_0\left(\frac{y}{h}\right) \tag{3.14}$$

This is on the average correct to within ~ 10% in the relevant range $0 \leq y \leq h/4$ as illustrated by Fig. 3.10.

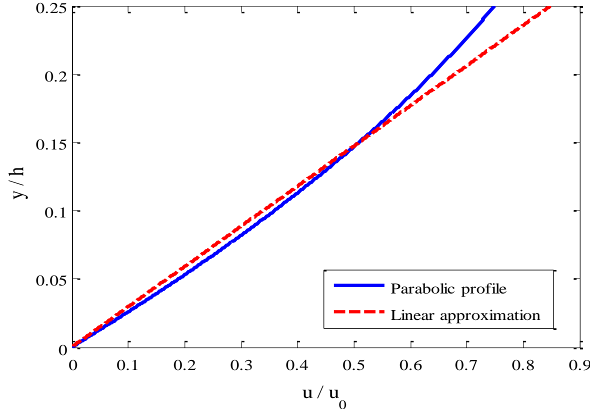


Fig. 3.10: Parabolic flow profile for $x_0 = \frac{h^2 u_0}{16D}$ (solid line) and linear velocity approximation (dashed line) as a function of y for $0 \leq y \leq h/4$.

According to [87], solving a diffusion problem in a semi-infinite system with a capturing boundary at $y = 0$ leads to the linear velocity profile given by:

$$\frac{C(x,y)}{C_0} = 1 - \frac{\int_\beta^\infty \exp(-\theta^3)\, d\theta}{\Gamma(\frac{4}{3})} \tag{3.15a}$$

where:

$$\beta = y\left(0.38\frac{u_0}{Dhx}\right)^{1/3} \tag{3.15b}$$

Here, θ is an integration parameter and Γ is the well-known gamma function. The concentration profiles given by Eq. (3.15a) do not differ strongly from those given by Eq. (3.11), but can be regarded as a refinement of the model. This is illustrated in Fig. 3.8 for $x_0 = \frac{h^2 u_0}{64D}$ and $x_0 = \frac{h^2 u_0}{16D}$ in the interval $0 \leq y \leq h/4$. Using Fick's law, the mass flux at $y = 0$ is given by:

$$F_m(x) = -D\left[\frac{\partial C(x,y)}{\partial y}\right]_{y=0} \tag{3.16a}$$

By using Eq. (11a) this now becomes:

$$F_m(x) = 0.81DC_0\left(\frac{Dhx}{u_0}\right)^{-1/3} \tag{3.16b}$$

As mentioned in [88] and indicated by the classical boundary layer theory—which equates the stationary boundary layer and mass flux over the susceptor, $F_m(x) = DC_0/\delta(x)$ and $\delta(x) = \left(\frac{\mu x}{\rho u}\right)^{\frac{1}{2}}$, respectively—the factor $\frac{1}{0.81}\left(\frac{Dhx}{u_0}\right)^{\frac{1}{3}}$ in Eq. (3.16b) can be considered the effective boundary layer thickness, $\delta_{eff}(x)$. The error in the mass flux given in Eq. (3.16b) introduced by the linear velocity profile is small (~ 3%) due to the power 1/3 of u_0. The mass flux follows a 1/3 power in x and u as a consequence of the linear velocity approximation.

Since the active component is only consumed at $y = 0$ (over the susceptor), the average concentration at $x = x_0$, $\bar{C}(x_0)$ can now be calculated on the basis of the total amount of material that has disappeared as follows:

$$\int_0^{x_0} F_m(x)dx = hu_0[C_0 - \bar{C}(x_0)] \tag{3.17a}$$

Solving this equation gives:

$$\bar{C}(x_0) = 0.81C_0 \tag{3.17b}$$

Using this and Eqs. (3.12) and (3.16b) we obtain for the mass flux at $x = x_0$ and $y = 0$:

$$F_m(x_0) = 2.52\frac{D\bar{C}(x_0)}{h} \tag{3.18}$$

Solutions for the depletion region $x > x_0$

Since the concentration profiles for values of any x larger than the entrance length are of the same form (this will remain true for any velocity function which is constant in x), Eq. (3.18) can be generalized by applying symmetry considerations:

$$F_m(x) = 2.52\frac{D\bar{C}(x)}{h} \tag{3.19}$$

The mass flux balance between the supply by forced flow and deposition at $y = 0$ for each x is now given by:

$$-hu_0\frac{\partial\bar{C}(x)}{\partial x} = 2.52\frac{\bar{C}(x)}{h} \tag{3.20}$$

Integration of this equation with respect to x from x_0 to x and with respect to $C(x)$ from $0.81C_0$ to $C(x)$ gives:

$$\bar{C}(x) = 0.81C_0 exp\left[\frac{-2.52D(x-x_0)}{h^2u_0}\right] \tag{3.21}$$

Then the concentration profiles at $y = 0$ can be calculated from Eq. (3.21). Rearranging and including Eq. (3.12) yields:

$$\bar{C}(x) = 0.692C_0 exp\left[\frac{-2.52D}{h^2u_0}x\right] \tag{3.22}$$

This is the average concentration profile of the reactants over the susceptor with a linear velocity profile. This will be used for developing the final deposition rate model for boron layer deposition.

3.4 Surface reaction mechanisms of the boron CVD deposition

In this section the surface reaction mechanisms are investigated to determine the activation energies of the pure boron (PureB) layer deposition at temperatures from 350 ℃ to 850 ℃. In the following sections, the experimental data presented here and the extracted activation energies will be applied as an input for developing the analytical kinetic model, which describes the deposition kinetics and the deposition chamber characteristics. These determine the deposition rates of boron layers on any uniform and non-uniform patterned silicon wafer.

The deposition was performed in a commercial Si/SiGe epitaxial reactor by exposing the Si surface to diborane (B_2H_6). At 700 ºC, in the first few seconds of exposure, the boron atoms interact with the Si surface sites to quickly build up something like an atomic layer plane [45, 89]. Upon further deposition the boron coverage readily exceeds one monolayer (1 ML). After this the boron atoms is deposited on a full boron surface, which is a process that has a much slower, well-controlled deposition rate. In the past it has been shown that less than 2-nm-thick layers can be deposited with good reliability and uniformity with a suitable adjustment of the deposition parameters such as deposition time, temperature, partial pressures and flow rates [88]. At lower temperatures the carrier gas has a large influence on the ability to create the first full boron coverage of the Si. Nevertheless, by first creating a full boron coverage at 700 ºC which is smooth and uniform, and then proceeding with the low temperature depositions, the boron-on-boron activation energies could be determined over the entire temperature range. The deposition behavior was also studied for a carrier gas of either H_2 or N_2. The latter can be considered to be an inert gas below about 800 ºC.

The overall chemical reaction describing the diborane deposition is quite simple and given by:

$$B_2H_6(g) \longrightarrow 2B(s) + 3H_2(g) \qquad [R3.23]$$

where (g) indicates the gas phase and (s) the solid phase. However, the individual reactions leading to this final result are quite complicated.

Several studies have been published on reactions between B hydrides and either Si(100) or boron surfaces [90-93]. The possible gas phase chemical reactions are very complex and include the formation of several high order boranes (B_3H_7, B_4H_{10} and B_5H_{11}). The work of T.P. Fehlner *et al.* [94-96], A.B. Baylis *et al.* [97] and G.W. Mappes *et al.* [98] specifically investigate the formation of solid boron from diborane and conclude that the dominant boron hydride gas phase species is BH_3. Modeling studies of the intentional doping of Si thin films using B_2H_6 as a dopant source gas, have also indicated that the primary gas phase reaction pathways are the decomposition of B_2H_6 into BH_3 and the subsequent recombination to again form B_2H_6 [91, 99-103], as shown in reaction [R3.24]. This assumption is also supported by computational studies that show that the unimolecular decomposition and recombination reactions are the energetically favorable reaction pathways [99, 104].

$B_2H_6(g) \longrightarrow 2BH_3(g)$ [R3.24]

As F. Sarubbi *et al.* mention [44, 45], in the first seconds of the silicon surface being exposed to diborane at 700 °C, the coverage of the deposited layer can grow to exceed 1 ML. After this phase, the boron atoms are deposited on a closed boron surface. At each stage of the deposition, the silicon or boron surface has many dangling bonds, some of which will be terminated with hydrogen atoms. When BH_3 molecules interact with these bonds, there are several possible reactions. With one precursor involved and four types of surface sites: H-terminated Si/B sites and H-free Si/B sites; there are four heterogeneous reactions that must be considered. The most probable reactions, from the point of view of thermodynamics and kinetics, are listed in Table 3.1. In the notation, H_Si, H_B are the silicon and boron atoms with H-terminated dangling bonds, and $\circ$ Si, $\circ$ B are the silicon and boron atoms with free dangling bonds, respectively. The perception that these are the most probable reactions is supported by silicon doping studies which have indicated that BH_3 is the active gas species that initially adsorbs on open surface sites [91, 99-103]. The BH_3 molecule will impinge upon the growth surface (silicon/boron) and form an activated BH_2-site complex.

The released atomic hydrogen in reactions [R3.25] and [R3.27] reacts *in-situ* with the H-terminated Si/B surface sites with the following possible surface reactions [105, 106]:

The forward direction of reactions ([R3.29] and [R3.30]) releases the hydrogen from the surface and decreases the H surface coverage. The presence of hydrogen gas can suppress this reaction. The reverse direction represents the reaction of molecular hydrogen with the surface. These two processes are illustrated in Fig. 3.11.

Table 3.1: Possible heterogeneous reactions involved in boron layer deposition with a B_2H_6 precursor.

Reaction no.	BH_3 reaction with	Reaction
[R3.25]	H-free Si surface sites	$BH_3(g) + \circ\, Si(s) \longrightarrow H_2B_Si(s) + H(g)$
[R3.26]	H-terminated Si surface sites	$BH_3(g) + H_Si(s) \longrightarrow H_2B_Si(s) + H_2(g)$
[R3.27]	H-free B surface sites	$BH_3(g) + \circ\, B(s) \longrightarrow H_2B_B(s) + H(g)$
[R3.28]	H-terminated B surface sites	$BH_3(g) + H_B(s) \longrightarrow H_2B_B(s) + H_2(g)$

$$\mathrm{H(g) + H_Si(s) \leftrightarrows H_2(g) + \circ\, Si(s)} \qquad [R3.29]$$

$$\mathrm{H(g) + H_B(s) \leftrightarrows H_2(g) + \circ\, B(s)} \qquad [R3.30]$$

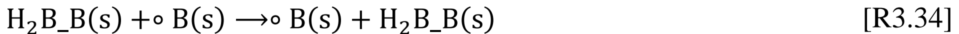
In the deposited layer there are some possible cross-linked reactions [107, 108] between two adjacent Si-H and B-H bonds (Fig. 3.11):

$$\mathrm{H_Si(s) + H_Si(s) \leftrightarrows Si_Si(s) + H_2(g)} \qquad [R3.31]$$

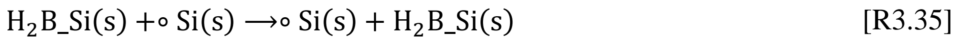
$$\mathrm{H_B(s) + H_B(s) \leftrightarrows B_B(s) + H_2(g)} \qquad [R3.32]$$

$$\mathrm{H_B(s) + H_Si(s) \leftrightarrows B_Si(s) + H_2(g)} \qquad [R3.33]$$

In addition, there are a few other possible reactions, like migration of the attached boron atoms along the surface (e.g. migration of deposited boron atoms along a boron-covered surface, [R3.34] and [R3.35]) and/or boron diffusion into the silicon substrate as a dopant, [R3.36] (see Fig. 3.11):



$$\mathrm{H_2B_B(s) + \circ\, B(s) \longrightarrow \circ\, B(s) + H_2B_B(s)} \qquad [R3.34]$$



$$\mathrm{H_2B_Si(s) + \circ\, Si(s) \longrightarrow \circ\, Si(s) + H_2B_Si(s)} \qquad [R3.35]$$

$$\mathrm{Si_B(s) \longrightarrow \circ\, Si(s) + B\ (diffused)} \qquad [R3.36]$$

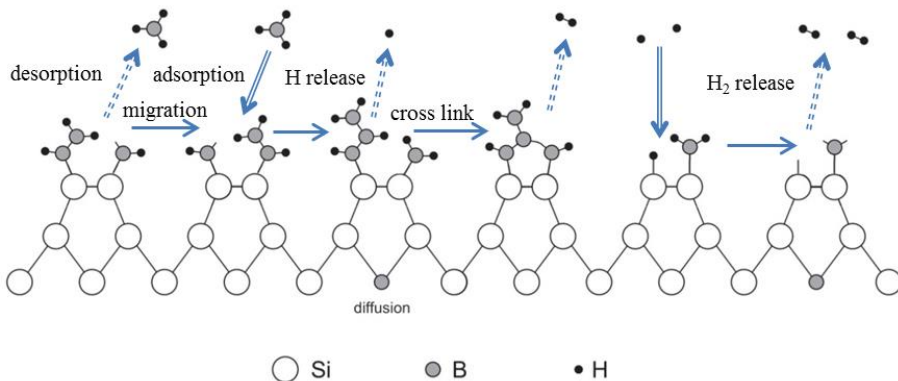


Fig. 3.11: Some of the possible secondary reactions when a Si surface is exposed to B_2H_6.

Theoretically the above nine reactions (reactions [R3.25] to [R3.33]) are all reversible. However, the diborane is thermodynamically unstable [95, 109] whereas the deposited boron layer is stable. This was confirmed by an experiment where the boron was deposited at 700 °C on a bare wafer and left in a H_2 atmosphere for time intervals varying from a couple of hours to several days. The boron layer thickness was monitored; the thickness was unchanged with only few percentage roughness change which confirms that there was no change over time. This means that in the temperature range 400 °C to 700 °C no etching and/or desorption reaction of the deposited layer with H_2 should be expected. Therefore, the reverse direction of reactions [R3.25] to [R3.28] can be neglected while reactions [R3.29] and [R3.30] must be taken into account. For reactions [R3.26] and [R3.28], two Si-H/B-H bonds must be broken, and only one Si-H/B-H bond must be broken for reactions [R3.25] and [R3.27]. Thus the activation energies of reactions [R3.26] and [R3.28] must be higher than those of reactions [R3.25] and [R3.27] so that:

$$E_a^{[R4]} > E_a^{[R3]}$$

and

$$E_a^{[R6]} > E_a^{[R5]}$$

Assuming that the lowest energy path will dominate, it can be concluded that the boron deposition on either silicon or boron surface will be governed largely by reactions [R3.25] and [R3.27].

Applying the same reasoning to reactions [R3.29] to [R3.32] gives:

$$E_a^{[R9]} > E_a^{[R7]}$$

and

$$E_a^{[R10]} > E_a^{[R8]}$$

Furthermore, we assume that the surface bonded hydrogen atoms are swept away by reactions [R3.29] and [R3.30] for silicon or boron surfaces, unless there are not enough free hydrogen atoms. This is considered to be the case, because the deposition of one BH_3 molecule produces two surface bonded hydrogen atoms but only one free hydrogen atom (reactions [R3.25] and [R3.27]).

The experiments were carried out in the ASM Epsilon 2000 Si/SiGe epitaxial reactor. The reactor has a large SiC susceptor which was heated up to the deposition temperature by a cross-array of lamps above and below the deposition chamber. The readout and control of the temperature was performed by one master thermo-couple at the center and three slaves at the front, rear and side of the susceptor that were found to be constant to within ± 0.5 °C. As a carrier gas, either pure H_2 or pure N_2 was used, with a water and oxygen content below the ppm level and a total flow rate of 20 slm (standard liters per minute). For deposition of the boron layer, diborane gas was used with several different input partial pressures. When H_2 was used as a carrier gas, naturally, the diborane was diluted in H_2. When N_2 was used as a carrier gas, the content of H_2 was less than 2% of the main gas flow. All experiments were performed at atmospheric pressure. Bare Si (100) 100 mm wafers with a thickness of 500-550 μm were used.

The samples were *ex-situ* prepared for boron deposition as described in Appendix A. In the deposition chamber, a 4-min H-bake was performed at 800 °C. The layer thickness was measured in-line using ellipsometry which has an acceptable accuracy and good repeatability for smooth layers [88]. To obtain smooth layers in all cases where the boron-on-boron deposition rate was to be determined, the initial deposition was performed at 700ºC. At this temperature, a complete (monolayer) B-coverage of the Si was readily achieved [45]. Subsequently, a series of thicker layers were deposited at the temperature to be investigated. The sheet resistance of some of the boron layers was determined by using the method described by F. Sarubbi *et al.* [45].

In Fig. 3.12 Arrhenius plots of the deposition rate (DR) of the boron layers is shown for two different diborane partial pressures P_{high} = 3.39 mtorr and P_{low} = 1.7 mtorr. For H_2 carrier gas and high partial pressure, three linear regions are clearly discerned, while for low partial pressure, only two regions are seen. In the latter case, for temperatures below approximately 400 °C, there is no measurable deposition. In the case of N_2 carrier gas with the high diborane partial pressure, the curve shows two linear regions, one below and the other above 700 °C.

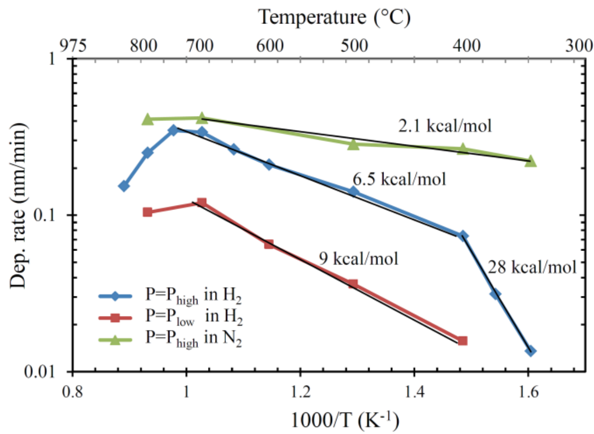


Fig. 3.12: Deposition rate (DR) of boron layers on B-covered Si as a function of temperature for different diborane partial pressures (P_{high} = 3.39 mtorr, P_{low} = 1.7 mtorr) and a carrier gas of either H_2 or N_2. The values are an average of 21 measurements taken across each wafer. The extracted activation energies in the linear regions are indicated.

In each linear region of the curves in Fig. 3.12, the deposition rate (DR) can be expressed by the Arrhenius equation:

$$\mathrm{DR(T)} = A\exp(\frac{-E_a}{RT}) \qquad (3.37)$$

where A, E_a, R and T are the frequency factor, the activation energy, the gas constant of the substrate, and the deposition temperature, respectively. The extracted activation energies of the boron deposition in each linear region are indicated in Fig. 3.12. For the deposition in H_2 and T ≤ 400 °C, the activation energy was found to be 28 kcal/mol. In this region the forward direction of reactions [R3.29] and [R3.30] are not dominant. Therefore, less hydrogen is released from the surface and most of the surface sites are terminated by hydrogen. As a consequence, the deposited boron layer is initially discontinuous and for longer deposition times a lumpy layer is created. This is supported by the ellipsometry measurements listed in Table 3.2 for boron layers deposited on a smooth boron layer pre-deposited at 700°C. This first layer has a roughness < 0.2 nm while the low temperature layers have a higher roughness. For the temperature range from 400 °C to 700 °C, the activation energy is found to be 6.5 kcal/mol. In this region the deposition of the boron layer is mainly

controlled by reactions [R3.25] and [R3.27]. Since reactions [R3.29] and [R3.30] are predominantly in the forward direction, the surface hydrogen is swept away by these reactions. Then the surface H coverage is very low, and accordingly the deposited boron layer in this temperature region is very smooth and uniform as confirmed by the ellipsometry measurements in Table 3.2. At temperatures above 700 °C, the deposition rate decreases with increasing temperature. This is largely due to a rise in the desorption of boron atoms from the surface (reverse direction of reactions [R3.25] to [R3.28]). Moreover, more boron can be lost from the surface by diffusion into the silicon substrate as given by reaction [R3.36]. In Fig. 3.13 measured sheet resistance values are plotted as a function of the deposition temperature. The values decrease with temperature with a very significant drop starting around 750°C where the boron diffusion constant in Si increases significantly. F. Sarubbi *et al.* [17] have shown that the boron layer has very high resistivity. The sheet resistance at these deposition temperatures is determined by the doping of the Si that is limited by the deposition time and the boron solid solubility in Si.

In the case of deposition in N_2, there is no hydrogen to suppress the forward direction of the reactions [R3.29] and [R3.30]. Therefore the activation energy is low with a value found to be 2.1 kcal/mol. This value is determined by the actual BH_3 reactions with Si and B surface sites.

All in all, it can be concluded that the boron deposition occurs through four main mechanisms: (a) direct B deposition by decomposition of BH_3 at free Si/B sites ([R3.25] to [R3.28]), (b) the intermediate reaction of atomic hydrogen with the H-terminated Si/B surface sites to release H_2 and create free Si/B sites ([R3.29] and [R3.30]), (c) post-deposition reactions by cross-linked processes accompanied with H_2 split-off ([R3.31] to [R3.33]), and (d) B desorption from the surface (reverse of [R3.25] to [R3.28]). Process (c) is associated with the decomposition of bulk H-Si and H-B bonds to give H_2 evolution, as has been observed in annealing experiments such as the one reported by J.A. McMillan and E.M. Peterson for a-Si:H-thin film treatments [110]. During the deposition, all four mechanisms (a), (b), (c) and (d) occur simultaneously. At the lower temperatures, (b) and (c) proceed slower than (a), and a hydrogenated layer may form near the surface. At the more moderate temperatures there is a better balance between the three steps (a), (b) and (c). Process (d) becomes dominant at high temperatures and the deposition rate decreases significantly.

Table 3.2: Boron layer roughness extracted from ellipsometry measurements, for a layer deposited in H_2 onto a smooth boron layer pre-deposited at 700 °C. This first layer has a roughness of < 0.2 nm.

	Temperature range (°C)		
	T < 400 °C	400°C ≤ T ≤ 700°C	T >700°C
Measured roughness (nm)	0.6 - 0.9	0.2 - 0.5	0.4 - 0.7

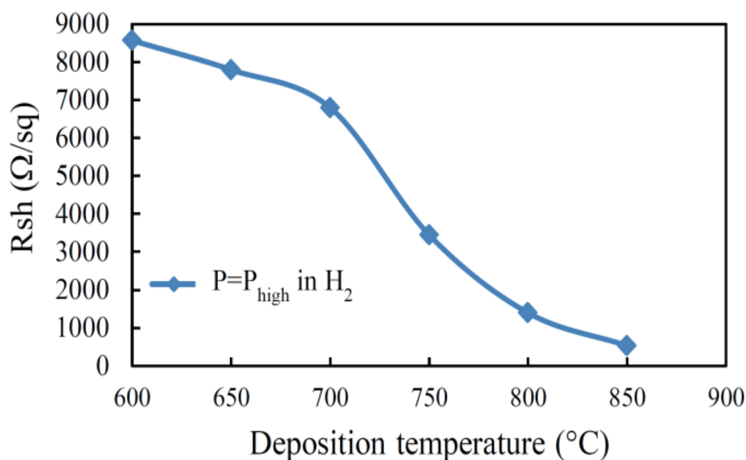


Fig. 3.13: Measured sheet resistance at different deposition temperatures for the diborane partial pressure, P_{high} = 3.39 mtorr.

The comparison between H_2 and N_2 carrier gases given in Fig. 3.12 shows that the presence of H_2 inhibits the deposition, i.e., reactions [R3.25] to [R3.32] are suppressed in the forward direction. Therefore, it can be concluded that for the inert carrier gas N_2 the deposition rate is determined by the rate of desorption of hydrogen being supplied by the precursor gas B_2H_6.

In conclusion, it has been shown that based on the presented results, the CVD behavior of boron on silicon from diborane to form boron layers can be understood in terms of the detailed reaction mechanisms involving BH_3 and H reactions with either Si or B surfaces. Desorption of H from surface bonds is essential for obtaining smooth layers with high deposition rates. Therefore, at 400 ºC, the highest rate of ~0.3 nm/min is found with a N_2 rather than H_2 carrier gas. The latter prevents deposition at temperatures below 400 ºC if the B_2H_6

partial pressure is too low. Activation energies have been determined in three distinguishable regions that each can be related to the dominance of a different chemical reaction mechanism: for H_2 as carrier gas 28 kcal/mol is found below 400 ºC and 6.5 kcal/mol from 400 ºC to 700 ºC; for N_2 as carrier gas the activation energy is found to be 2.1 kcal/mol for all deposition temperatures below 700 ºC. These activation energies will be used as an input for an analytical kinetic model developed in the next section.

3.5 Modeling of the active precursor flux over the surface

For a gas-solid heterogeneous unimolecular elementary reaction, there are two essential conditions needed for reactant molecules to deposit onto the substrate:

(i) The reactant molecules must be activated.

(ii) The reactant molecules must interact with the substrate.

The Meng Tao method of modeling the growth rate of the CVD deposition of Si from silane [76] is presented here as a basis for the approach taken for the boron case. In Tao's model, the impinging reactant molecules on the Si surface are attached to the dangling bonds. By applying the Maxwell distribution function in unit time, the number of the reactant molecules (dΓ) which interact with a unit area of the substrate with kinetic energy between E_K and (E_K +dE_K) can be thus estimated to be:

$$d\Gamma = 8\pi N_R \left(\frac{1}{2\pi m_R kT}\right)^{\frac{3}{2}} m_R E_k \exp\left(-\frac{E_k}{\mathrm{k}T}\right) dE_k \tag{3.38}$$

where N_R is the number of reactant molecules in a unit volume of the gas phase, m_R is the mass of a reactant molecule, and the k is Boltzmann's constant at the deposition temperature. Integrating the formula from E_A (deposition activation energy) to + ∞, the number of the activated reactant molecules which strike a unit area of the substrate in one unit of time is given by:

$$\Gamma = \frac{N_R}{(2\pi m_R kT)^{\frac{1}{2}}} (E_A + \mathrm{k}T) \exp\left(-\frac{E_A}{\mathrm{k}T}\right) \tag{3.39}$$

Thus the activated flux of a precursor, i.e., the number of precursor species that decomposes upon collision with the substrate is:

$$f_R^S = \frac{P_R^S}{(2\pi m_R \mathrm{k}T)^{\frac{1}{2}}}(\frac{E_A}{\mathrm{k}T} + 1)\exp\left(-\frac{E_A}{\mathrm{k}T}\right) \tag{3.40}$$

where P_R^S is the partial pressure of the reactant at the surface of the substrate, and E_A is the activation energy of the heterogeneous reaction, assuming a perfect gas for which $P = N\mathrm{k}T$.

Surface reaction mechanisms of diborane, B_2H_6, on the Si/B surfaces were investigated in Section 3.4. Hence in the gas phase, B_2H_6 undergoes homogeneous decomposition by reaction [R3.24]. Following this section, BH_3 adsorption brings H to the surface, which affects the surface H coverage and hence the deposition rate. With one precursor involved and four types of surface sites, H-terminated Si and B sites and H-free Si and B sites, there are four heterogeneous reactions to consider (reactions [R3.25] to [R3.28]) with the notation of $f_{\mathrm{BH_3-on-Si}}$, $f_{\mathrm{BH_3-on-HSi}}$, $f_{\mathrm{BH_3-on-B}}$, and $f_{\mathrm{BH_3-on-HB}}$ respectively. Then the total B-flux over the substrate surface can be expressed as the sum of the above-mentioned four fluxes.

On the other hand, the activation energies for reactions on H-terminated Si/B surface sites are larger than H-free sites. Thus these fluxes can be neglected as compared to those on H-free Si/B surface sites. As an example, the activation energy of SiH_4 adsorption on H-free Si sites is ~30 kcal/mol [111], whereas that on H-terminated Si sites is ~51 kcal/mol [112]. It is reasonable to assume that the situation for the deposition of BH_3 would show a similar trend. Under this assumption, the total surface B flux can be expressed as:

$$\begin{aligned} f_{\mathrm{B}}^S &= f_{\mathrm{BH_3-on-Si}}^S + f_{\mathrm{BH_3-on-HSi}}^S + f_{\mathrm{BH_3-on-B}}^S + f_{\mathrm{BH_3-on-HB}}^S \\ &\approx f_{\mathrm{BH_3-on-Si}}^S + f_{\mathrm{BH_3-on-B}}^S \end{aligned} \tag{3.41}$$

Based on Eq. 3.40, we can write the equation for the primary surface B flux as:

$$f_{\mathrm{B}}^{S} \approx \eta_1(1-\gamma)\left(1-\theta_{\mathrm{H(Si)}}\right)\frac{P_{\mathrm{BH_3}}^{S}}{\left(2\pi m_{\mathrm{BH_3}}\mathrm{k}T\right)^{\frac{1}{2}}}\times \left(\frac{E_{\mathrm{BH_3-on-Si}}}{\mathrm{k}T}+1\right)\exp\left(-\frac{E_{\mathrm{BH_3-on-Si}}}{\mathrm{k}T}\right)+ \eta_2\gamma\left(1-\theta_{\mathrm{H(B)}}\right)\frac{P_{\mathrm{BH_3}}^{S}}{\left(2\pi m_{\mathrm{BH_3}}\mathrm{k}T\right)^{\frac{1}{2}}}\times \left(\frac{E_{\mathrm{BH_3-on-B}}}{\mathrm{k}T}+1\right)\exp\left(-\frac{E_{\mathrm{BH_3-on-B}}}{\mathrm{k}T}\right) \tag{3.42}$$

In these equations, $\theta_{\mathrm{H(Si)}}$ and $\theta_{\mathrm{H(B)}}$ are the ratio of H-terminated Si sites to all Si sites and the ratio of H-terminated boron surface sites to all boron surface sites, respectively. The $P_{\mathrm{BH_3}}^{S}$ and $m_{\mathrm{BH_3}}$ are the BH_3 partial pressure at the substrate surface, and molecular mass of BH_3, respectively. The $E_{\mathrm{BH_3-on-Si}}$ and $E_{\mathrm{BH_3-on-B}}$ are the activation energies unique to the particular reaction ([R3.25], [R3.27]). The γ is the ratio of boron surface sites to all surface sites and is calculated as [B]/N_0, where [B] is the B concentration and N_0 the atomic density of the boron layer, which is 5.0×10^{22} atoms/cm^3 at Si surfaces and 1.3×10^{23} atoms/cm^3 at B surfaces [113]. Also η *is* a unit less constant.

As described in Section 3.4, at the early stages of deposition, such as sub-min deposition times, boron atoms are deposited and interact to cover the silicon surface with an atomic-layer plane, while the boron coverage can also grow to exceed one monolayer (1 ML). Thus the boron deposition can be divided into the two stages. In the first stage a monolayer coverage of boron atoms on the Si surface is being built up, and in the second stage the boron atoms are deposited on a surface fully covered with boron atoms. Here only the second stage is modeled. Then the activated boron flux on the B surface is reduced to $f_{\mathrm{B}}^{S} \approx f_{\mathrm{BH_3-on-B}}^{S}$ and expressed as:

$$f_{\mathrm{B}}^{S} \approx \eta\gamma\left(1-\theta_{\mathrm{H(B)}}\right)\frac{P_{\mathrm{BH_3}}^{S}}{\left(2\pi m_{\mathrm{BH_3}}\mathrm{k}T\right)^{\frac{1}{2}}}\times \left(\frac{E_{\mathrm{BH_3-on-B}}}{\mathrm{k}T}+1\right)\exp\left(-\frac{E_{\mathrm{BH_3-on-B}}}{\mathrm{k}T}\right) \tag{3.43}$$

3.6 Description of the experiments

Experiments were carried out in two systems: the ASM Epsilon One and 2000, which have a quartz reactor with a rectangular cross-section. In Table 3.3 the main parameters describing the present experimental conditions are given. These reactors have a large SiC susceptor which is heated up to the deposition temperature by a cross-array of lamps above and below the deposition chamber. The readout and control of the temperature are performed by one master thermo-couple at the center and three slaves at the front, rear and side of the susceptor, which was found to be kept at a constant temperature within ± 0.5 °C.

For deposition of the boron layer, diborane was used as a gas source with different input partial pressures from 1.7 mtorr to 3.39 mtorr. Pure H_2 was used as a carrier gas with a water and oxygen content below the ppm level with variable flow rates between 5 slm and 20 slm (standard liters per minute). All depositions were performed at 700 °C and atmospheric pressure (ATM) over 100 mm non-rotating bare Si (100) wafers with a thickness of 500 μm to 550 μm. Also we found that the substrate type (orientation, resistivity and doping type) did not influence the deposition rate significantly.

The samples were *ex-situ* prepared for boron deposition as described in Appendix A. As an extra measure to assure an oxygen-free surface, a 4-min H-bake at 800 °C was performed before the deposition [45]. The layer thickness was measured in-line using ellipsometry which has an acceptable accuracy and good repeatability for smooth layers [88]. The inlet region before the deposition zone (see Fig. 3.2) is around 15 cm for our reactors, which was calculated to be long enough to allow the velocity profile to be established [114]. The hot zone suited for reaction/deposition is 25 cm in length. For the experimental data, the position $x = 0$ defines the leading edge of the wafer on the hot susceptor.

Table 3.3: Main parameters describing the experimental conditions for both the Epsilon One and Epsilon 2000.

EPI	*h (mm)*	*h/b*	u_0 *min*	u_0 *max*	$P_{B_2H_6}$ *min*	$P_{B_2H_6}$ *max*
One	22	0.085	10 slm	20 slm	1.7 mtorr	3.39 mtorr
2000	24	0.089				

3.6.1 Application of the theoretical model to the CVD process

It is a generally accepted fact that the CVD deposition of boron using diborane with hydrogen carrier gas is limited by gas phase diffusion of BH_3 molecules through the stationary boundary layer over the wafer (e.g., [88]). Diborane is known to decompose in H_2 at temperatures above 200 °C - 300 °C [95]. Furthermore it can be observed from Fig. 3.4 or more clearly from Fig. 3.14, which it is only in a narrow region close to the susceptor where the gases are heated to the deposition temperature. Therefore the assumption that B_2H_6 molecules decompose just over the susceptor is acceptable. The upper wall of the chamber is not heated with lamps so the decomposition will not take place at this cold wall (see Fig. 3.14).

From the evidence presented above, it can be concluded that under forced laminar flow conditions, the theoretical model discussed in the previous section should be applicable to the present systems. As far as we know, no measurements are available for the diffusivity of BH_3 in H_2, so in the present analysis the diffusion coefficients for the undecomposed BH_3 molecule are used.

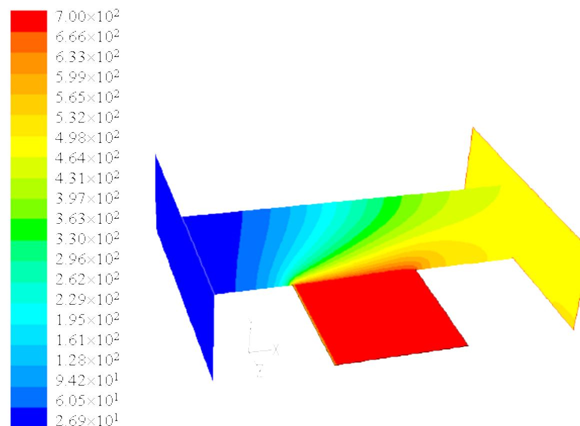


Fig. 3.14: Temperature distribution for an ASM Epsilon One CVD reactor as simulated by commercial FLUENT© software with the total pressure at ATM. To simplify the simulation, H_2 is considered to be the main gas flowing over the susceptor. The susceptor is heated up by an assembly of lamps to the deposition temperature (here 700 °C). This heat is then transferred to the flowing gas [82]. More simulation conditions can be seen in Fig. 3.4.

From [115], it can be found that the diffusion coefficient for BH_3 with M = 13.84 g/mol, is approximately 0.77 cm^2/s at 273 K and 1 ATM in H_2. Then following this reference, this value can be extrapolated to a temperature of 973 K (~ 700 °C) by using this empirical equation:

$$\frac{D_{\mathrm{BH_3}}^{T_1}}{D_{\mathrm{BH_3}}^{T_2}} = \left[\frac{1}{2}\left(\frac{T_1}{T_2} + 1\right)\right]^{1.65} \tag{3.44}$$

Then the physical constant for BH_3 in H_2 at 1 ATM and 700 °C is:

$$D_{\mathrm{BH_3}}^{700\,°\mathrm{C}}(\mathrm{H_2}) = 3\ \frac{\mathrm{cm^2}}{\mathrm{s}} \tag{3.45}$$

Since these diffusion coefficients vary approximately with the square root of the reduced molecular mass of the diffusing molecules, only small differences for the diffusion of the various possible diborane species are expected.

In Section 3.4, the activation energies of the reaction/deposition of the boron layers is found to be 6.5 $kcal.mol^{-1}$ for moderate temperatures between 400 °C to 700 °C and 28 $kcal.mol^{-1}$ for lower temperatures (lower than 400 °C).

3.7 Results and discussion

In this section an analytical model is established to describe the deposition kinetics and the deposition chamber characteristics that determine the deposition rate over the wafer. The predictive capabilities of the model have been verified by experiments, performed at 700 ºC in different ASM CVD reactors [116].

A bare clean silicon wafer is loaded into the reactor and placed on a non-rotating susceptor in the way that the primary flat of the wafer is located perpendicular to the direction of the gas flow as shown schematically in Fig. 3.15.

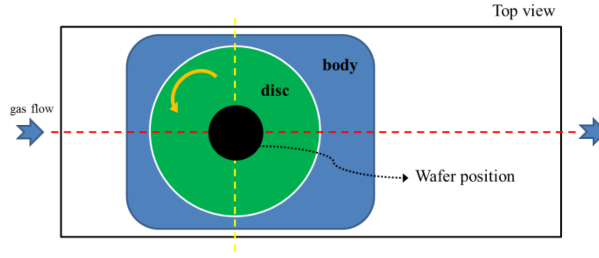


Fig. 3.15: Schematic top view of the reactor indicating the susceptor and position of a wafer inside the reactor.

Therefore the classical boundary layer and reactor conditions over the susceptor as shown in Fig. 3.7 are applicable for the bare non-rotating wafer as well as the average concentration profile of the reactants over the susceptor with the linear velocity profile of Eq. (3.22). With Eqs. (3.22) and (3.43) and using the ideal gas law in a very thin layer over the susceptor, the final equation for the total activated B flux over the susceptor ($y = 0$) is obtained as:

$$f_{\mathrm{B}}(x) \approx 0.264\eta\gamma\left(1-\theta_{\mathrm{H(B)}}\right)\frac{P_{\mathrm{BH_3}}}{\left(\mathrm{m_{BH_3}}\mathrm{k}T\right)^{\frac{1}{2}}}\times \left(\frac{E_{\mathrm{BH_3-on-B}}}{\mathrm{k}T}+1\right)\exp\left(-\frac{E_{\mathrm{BH_3-on-B}}}{\mathrm{k}T}\right)\exp\left(-\frac{2.52D}{h^2u_0}x\right) \tag{3.46}$$

In this equation, the $P_{\mathrm{BH_3}}$ is the input partial pressure of the $\mathrm{BH_3}$ and the $E_{\mathrm{BH_3-on-B}}$ is the unique activation energy of the boron CVD deposition, as already discussed in this chapter.

If the density of the deposited boron layer is ρ_{B}, and the mass of the pure boron atoms in the layer is M, the number of boron atoms in a unit volume of the boron layer is:

$$N_0 = \frac{\rho_{\mathrm{B}}}{M} \tag{3.47}$$

From the equations given above, the deposition rate, DR, of the boron layer deposited in a CVD system by using B_2H_6 over a bare non-rotating silicon wafer can be calculated as $\frac{f_{\mathrm{B}}(x)}{N_0}$ yielding:

$$\mathrm{DR}_{\mathrm{BnR}}^{\mathrm{B}}(x) = 0.264\eta\gamma\beta_1\beta_2 P_{\mathrm{BH}_3} \times \exp\left(-\frac{2.52D}{h^2 u_0}x\right) \tag{3.48}$$

where:

$$\beta_1 = \frac{1}{N_0}\frac{\left(1-\theta_{\mathrm{H(B)}}\right)}{\left(m_{\mathrm{BH}_3}\mathrm{k}T\right)^{\frac{1}{2}}}$$

and:

$$\beta_2 = \left(\frac{E_{\mathrm{BH}_3\mathrm{-on-B}}}{\mathrm{k}T}+1\right)\exp\left(-\frac{E_{\mathrm{BH}_3\mathrm{-on-B}}}{\mathrm{k}T}\right)$$

In Fig. 3.16 several experimental results are compared to model predictions. It should be noted that parameter fitting was performed for the ASM Epsilon One. The boron deposition rates are extracted as a function of (a) the axial position, x, for different gas flow and diborane partial pressure conditions, (b) gas flow over the susceptor, and (c) input diborane partial pressure including curves for two different axial positions. By only adjusting the reactor/process parameters, this model was also successfully transferred from the ASM Epsilon One to the Epsilon 2000 reactor, which has completely different reactor conditions. The experimental results and model predictions for the Epsilon 2000 are also shown in Fig. 3.16a. In fact, this model is capable of predicting the deposition rate on any 2D uniform or non-uniformly patterned wafer such as those used for advanced device fabrication. The very small, less than 5%, deviation between the experimental results and model prediction is plausibly related to the lateral diffusion of the diborane molecules, which becomes more evident at lower gas flows and diborane partial pressures.

It can be seen that the data calculated on the basis of this model fit well with the experimental results and have been very useful not only in the development of uniform boron layers with little pattern dependence, but also in the transferring of recipes from one reactor to the other.

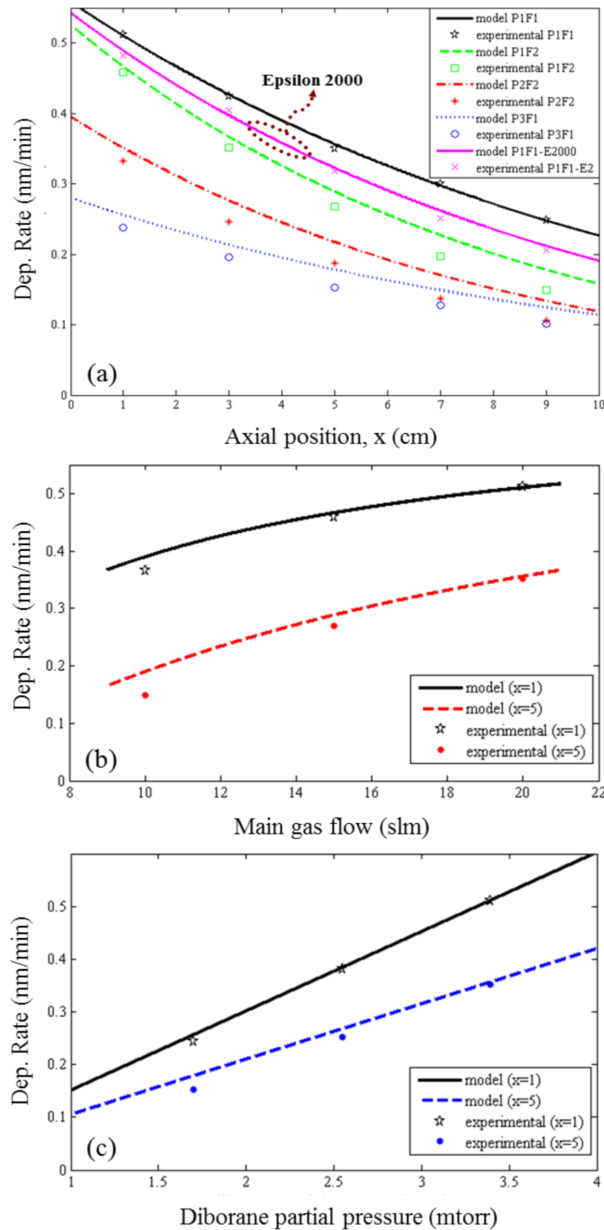


Fig. 3.16: Model and experimental results for the boron deposition rate as a function of (a) an axial position, *x*, (b) main gas flow over the susceptor, and (c) diborane partial pressure. The applied diborane partial pressures were 3.39, 2.55 and 1.7 mtorr given by P_1, P_2 and P_3, respectively. Furthermore the applied gas flows were 20, 15 and 10 slm given by F_1, F_2 and F_3, respectively. All experiments were performed at atmospheric pressure [116].

Remarks on validity of the model for laminar flow and influence of axial and lateral diffusion of diborane species

Equation (3.48) for the deposition rate in a laminar flow system is, in principle, only valid for the two-dimensional case of two semi-infinite parallel plates. A cell with a rectangular cross-section can also be considered as a two-dimensional system if the following requirements are fulfilled. First, the lateral concentration gradients should be small so as to minimize the diffusion in this direction. Secondly, the gas flow velocity must be constant in the lateral direction. Finally, free convective movements that can cause differences in the supply of reactant components laterally should be of no consequence [75].

To examine this, boron deposition rates were also studied as a function of the lateral position, z, on the wafer. We found that upon decreasing the diborane partial pressure and/or gas flow rate during the deposition, the axial and lateral homogeneity are disturbed, as can be seen in Fig. 3.17. This phenomenon can be attributed to axial and lateral diffusion of the diborane species due to the lateral concentration gradients and lateral gas velocity profile. However, in our case this is not considerable. From this we infer that lateral diffusion effects will, at least in the deposition region, not play an important role. On the other hand, the gas velocity can be calculated as a function of lateral position, z, using an empirical expression derived by Holmes and Vermeulen [117] as shown in Fig. 3.18. The results are shown in this figure for the four different rectangular reactor cells with a comparison to the reactor we used in this experiment. The shapes of the velocity profiles strongly depend on the aspect ratio, h/b, of the reactor.

It can be seen that in our reactor, the gas velocity is constant to within 80% of the total reactor width. There is a minor influence as can be seen by the deposition rates in Fig. 3.17. Therefore, it is concluded that the lateral distribution of deposition rates is determined by the lateral profile of the forced flow velocity in these low R_a number systems. This implies that free convective motions are not important. Giling's holographic experiments [118] showed that isotherms are perfectly parallel to the susceptor, and that gas flow patterns are very stable under the present conditions. From this it was concluded that in the part of the cell where flow and temperature profiles are developed, free convective motions are not important. From the present work it can be found that if free convective motions are present, they do not affect mass transport by diffusion and forced flow under low R_a number conditions. Therefore, when

considering the deposition rate distributions in our situation, the flow may be assumed to be effectively forced laminar.

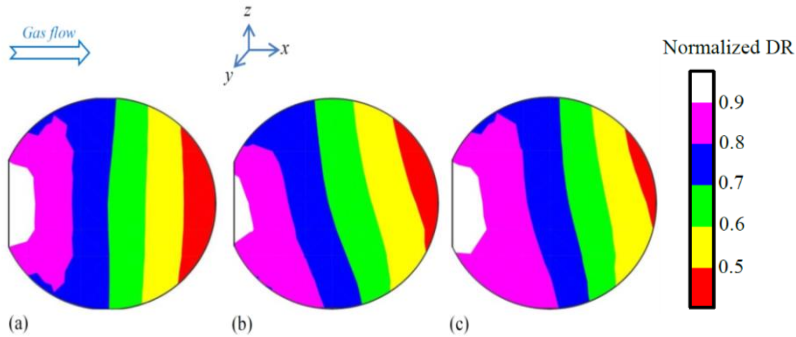


Fig. 3.17: 2D contour plots of the normalized boron deposition rate over a non-rotating wafer for (a) P_1F_1, (b) P_1F_3 and (c) P_3F_1 conditions. Here P_1 and P_3 are 3.39 mtorr and 1.7 mtorr, while F_1 and F_3 are 20 slm and 10 slm, respectively.

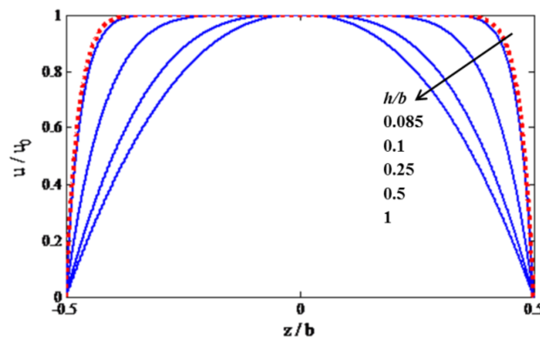


Fig. 3.18: Lateral distribution of gas velocity at a specific height above the susceptor for the h/b ratios 0.085, 0.1, 0.25, 0.5 and 1, according to [117].

3.8 Summary

In this chapter, surface reaction mechanisms are investigated to determine the activation energies of pure boron (PureB) layer deposition at temperatures from 350 ºC to 850 ºC. For better understanding of the chamber parameters, the gas flow and the heat transfer in the ASM Epsilon 2000 CVD reactor are numerically simulated by using commercial CFD software. The results are employed to develop an analytical model to describe the deposition kinetics and the deposition chamber characteristics. These determine the deposition rate of boron layers over the wafer. This model is based on a wide range of input parameters, such as: initial diborane partial pressure, total gas flow, axial position on the wafer, deposition temperature, activation energy of the diborane deposition, surface H-coverage, and reactor dimensions. By only adjusting these reactor process parameters, this model is also successfully transferred from the ASM Epsilon One to the Epsilon 2000 reactor which has completely different reactor conditions.

It can be concluded that the data calculated on the basis of this model fit well with the experimental results. The very small, less than 5%, deviation between experimental results and the model prediction is plausibly related to the lateral diffusion of the diborane molecules, which becomes more evident at lower gas flows and diborane partial pressures. The influence of axial and lateral diffusion of diborane species and the validity of the model for laminar flow in the real CVD process is clarified. In fact, this model is capable of predicting the deposition rate on any 2D uniform or non-uniformly patterned wafers, such as those used for advanced device fabrication. The model has been very useful both in the development of uniform boron layers with minimal pattern dependence and in the transferring of recipes from one reactor to the other. As a result, the deposition of 2-nm-thick boron layers with thickness variations of only a few angstroms is now performed as the standard for a variety of process wafer conditions, as will be described in detail in Chapter 4.

Chapter 4

Optimization of conventional high temperature boron deposition

In Chapter 2, the impressive properties of the state-of-the-art PureB UV and low energy electron detectors are reviewed. Also some of the important drawbacks that affect the performance of these devices are discussed. From the discussion in Chapter 2 it is concluded that an improvement in PureB technology is highly required in two aspects: (i) reducing the deposition temperature below 500 °C, which will make this technology compatible with standard CMOS processes (this issue is addressed in Chapter 5, where a novel technology for low temperature (LT, 400 °C) boron deposition is developed); (ii) improving the spatial uniformity of responsivity mainly related to the boron layer thickness uniformity, especially for applications demanding a uniform response over the entire active region.

To solve the boron layer uniformity problem, in this chapter the loading effect and the pattern dependency of high temperature (HT, 700 °C) boron deposition are investigated and identified as sources of layer non-uniformity.

Since investigating the loading effect and pattern dependency requires studying the thickness variation, first, some thickness evaluation measurement techniques are discussed together with their advantages and limitations regarding the uniformity monitoring. Furthermore, an end-of-line resistance measurement technique is introduced as a nondestructive and accurate means of monitoring the boron uniformity with fine resolution. Then the non-uniformity of the boron layer and its impact on the device performance are discussed. The pattern dependency and local loading effect of the HT boron deposition are studied as sources of layer non-uniformity. Lastly, based on all discussions, by

using the kinetic model developed in Chapter 3, recommendations for depositing a uniform 2-nm-thick boron layer are made.

Altogether, it will be shown that the optimized HT boron deposition process provides uniform and reliable deposition of 2-nm-thick boron layers, with only thickness variation of a few angstroms. Basically, this improved process can be applied without changing the existing designs, as in most cases the desired optimization can be achieved only by modifying the chamber and the process parameters. This property of the new process makes it very interesting and easy to use for existing layouts. The process proposed in this chapter is employed to fabricate high performance PureB detectors, particularly for low penetration photon/electron beam detection. The results will be presented in Chapter 6.

4.1 Thickness and uniformity evaluation techniques

In this section, several techniques for thickness and uniformity evaluation of the deposited layer are explored as well as vertical resistance measurement technique is introduced as a means of monitoring the boron uniformity.

The VUV and E-beam sensitivity measurements are preferred methods for monitoring the boron layer thickness. Both VUV light (10 nm - 200nm) and electrons with less than 1-keV of energy have an extremely small penetration depth of less than 10 nm not only in silicon, but in practically all other solid state materials. This can be seen in Fig. 2.3 (Chapter 2) and Fig. 4.1, where the attenuation length of (V)UV light and the path length of electron beam in silicon are shown respectively.

Therefore the response of detectors with only a boron layer front entrance window to these radiation sources can be very sensitive to any thickness variations of the boron layer, even in the angstrom range, as can be seen in Fig. 2.19 and Fig. 2.20 (Chapter 2). Hence these two measurements can be used as a very accurate method to study the boron layer uniformity. The layer uniformity is extracted by monitoring the induced photo/electron current of the detector during the scanning of its surface with a small area beam. Thus, for accurate and reliable results, a good quality detector is needed for the measurements. Therefore the measurements cannot be done only for deposited boron on silicon substrate. This circumstance is a limiting point of using these kinds of measurements as in-line measurement techniques for uniformity monitoring.

The High Resolution Transmission Electron Microscope (HRTEM) is the other ultimate testing technique. The HRTEM image provides very accurate cross-sectional information such as two-dimensional projection of the crystal structure, as well as layer stack thickness with angstrom accuracy, as can be seen in Fig. 2.4 (Chapter 2). However this technique needs some preparation steps before imaging which make it costly, time consuming, complex and destructive, and also prevents the use of this technique for any in-line uniformity monitoring.

Another technique that can be used, with certain limitations, for determining the layer thickness is Secondary Ion Mass Spectrometry (SIMS) measurement. This technique is used to determine the elemental, isotopic, or molecular composition of the surface to a depth of 1 to 2 nm and can be a very sensitive surface analysis technique. However for thickness monitoring, in this measurement, the density of a deposited layer is very important and can be a limiting point when this value is unknown or varies with the deposition conditions. Also this measurement is not sensitive to the surface roughness. Additionally, the SIMS measurement is time consuming, complex, and destructive measurement, which also makes this technique impractical for in-line uniformity monitoring.

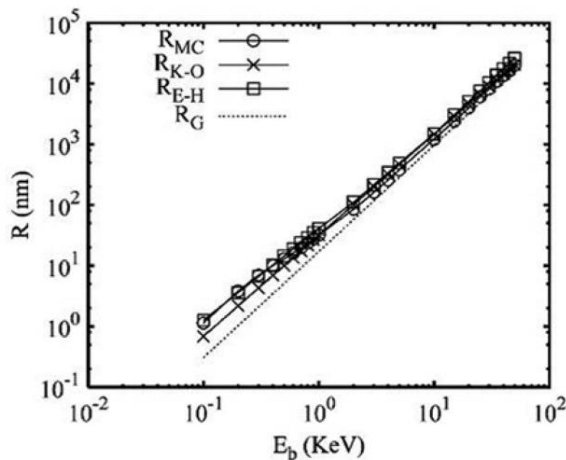


Fig. 4.1: Penetration depth in Si versus electron range for Silicon. RMC is from Monte Carlo simulation [14]. See Fig. 2.3 in Chapter 2 for attenuation length of UV photons into silicon.

The other useful, handy technique is ellipsometry measurement. Ellipsometry measures a change in polarization as light is reflected by, or transmitted through, a material structure. The polarization depends on the optical properties and the thickness of the individual materials. Normally, for our experiments at DIMES, an ellipsometry measurement is employed after boron deposition to monitor the boron thickness on a millimeter-large surfaces. This technique has the advantage of being not only a quick, non-destructive and repeatable measurement technique that can be used for in-line boron layer thickness monitoring, but also a calibration tool of the deposition parameters. However it needs an ellipsometry model. This model was prepared at DIMES and calibrated for HRTEM images. The measurements give consistent results in the case of 700 °C deposition, while, due to the increased roughness of the layers for lower temperature depositions, the ellipsometry becomes inaccurate; the roughness should not be more than the thickness [119, 120]. Examples are given in Table 4.1 where the values are extracted from ellipsometry measurements.

In Fig. 4.2, past ellipsometry measurements of boron layer thicknesses are plotted and used to determine the boron deposition rate at 700°C. The deposition rate is shown to be constant, at about 0.4 nm/min, which is a function of deposition time repeated over time. Moreover, this deposition rate is the same as reported by F. Sarubbi in [45], where the values were determined on the basis of HRTEM images.

In Fig. 4.3 an overview is given of the statistical results of the boron layer thickness with 6-min boron deposition at 700 °C for six different runs during the last two years. Dispersion values were calculated as the ratio between the standard deviation and the thickness mean value. These low dispersion values highlight the exceptional reproducibility of the boron deposition process over time.

Nevertheless, this technique has limited resolution, it does not provide information about the layer thickness close to the perimeter of large windows, and it cannot be applied to micron-sized windows. Therefore a quick and simple measurement technique is highly demanded as a non-destructive, in-line means of monitoring the boron layer thickness uniformity regardless of the deposition temperature. Therefore, an alternative measurement technique is proposed: an end-of-line resistance measurement.

Table 4.1: Ellipsometry measurement of thickness and roughness of boron layers deposited at different temperatures.

Boron	Dep. temp				
	700°C	600°C	500°C	450°C	400°C
Dep. time (min)	10	10	16	20	60
Thickness (nm)	3.74	3.21	3.14	1.77	1.62
Roughness (nm)	0.38	0.81	1.23	2.64	3.73

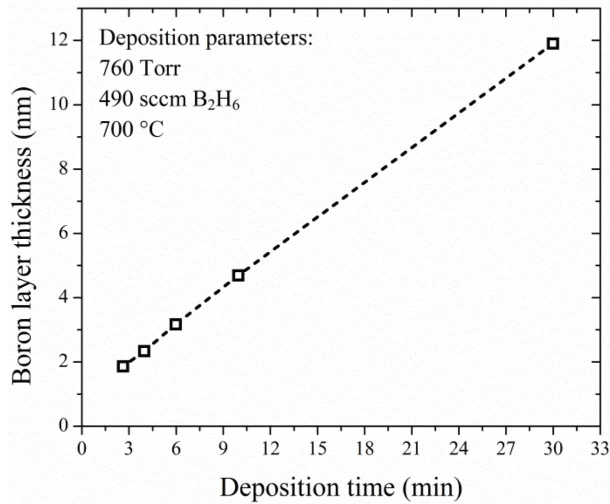


Fig. 4.2: The boron layer thickness as a function of B_2H_6 exposure times at 700 °C.

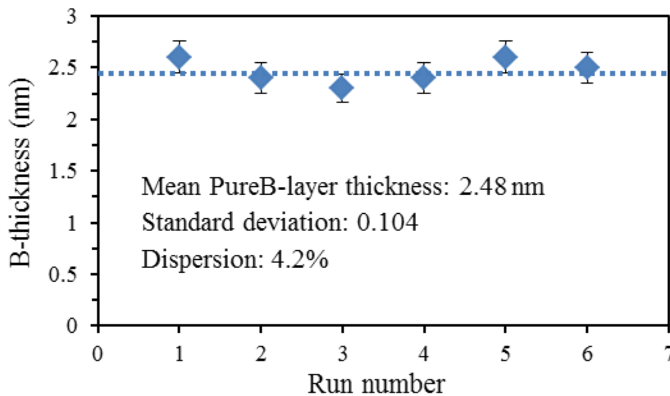


Fig. 4.3: Reproducibility of boron layer deposited at 700 °C for 6 min over different six runs.

4.1.1 End-of-line resistance measurement

Dedicated structures are designed for resistance measurement to monitor the thickness variations in nm-thin boron layers deposited on Si for detector applications where the angstrom level thickness variations have an impact on the performances, as described previously in Chapter 2. In millimeter-large windows, a fine resolution is achieved with the metal contact arrays patterned directly on the boron layer. For micron-sized windows Kelvin structures provide a sensitive solution.

a. Test methodology and structure design

With the goal of mapping the thickness variations, due to loading effects for all window sizes, we have examined two types of resistance measurement structures. One involves a direct resistance measurement and is suited for mapping the thickness over millimeter-large windows. The other uses a Kelvin contact resistance test structure to measure the resistance through the boron layer, when deposited in small windows.

<u>Large Si openings</u>

For large-area windows, arrays of aluminum contacts are directly patterned on the boron surface in the manner illustrated schematically in Fig. 4.4.

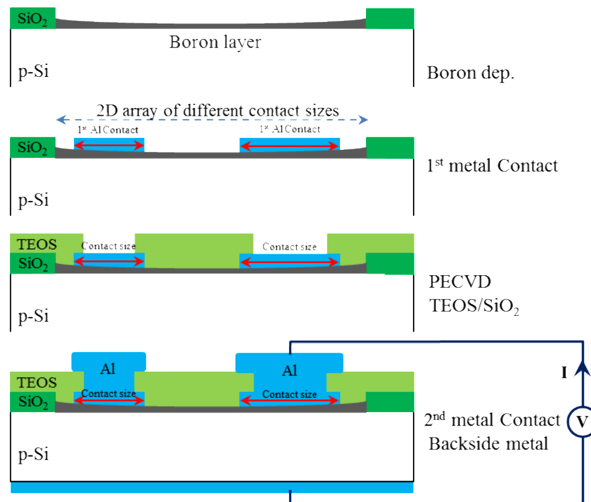


Fig. 4.4: Basic process flow for fabricating arrays of contacts on large boron-coated windows with the Si.

The boron makes ohmic contact with the p-Si substrate and the Al patterning on the boron layer is possible by selectively etching the Al to the boron with diluted HF (see Appendix B) [121]. Direct I-V measurements can then be performed through each contact to the back of the wafer as shown in the schematic. Since the boron layer resistivity is high, the resistance through it will dominate the measurement even for nm-thin layers. In the examples given here the windows are (20×20) mm^2 in area and they are patterned with arrays of 190×190 contacts with areas of: (4×4) µm^2, (6×6) µm^2, (8×8) µm^2 or (10×10) µm^2, evenly distributed over the boron surface. For these large windows, ellipsometry was also used to calibrate the layer thickness directly after deposition.

Micron-sized Si openings

For micron-sized windows, the cross-bridge Kelvin resistance (CBKR) structure shown in Fig. 4.5 is employed. It is designed to accurately measure contact resistance values down to at least 10^{-7} Ωcm^2 [122]. The structure has five contact openings: B, C, D, E and F, with areas of $l \times l$, $l \times 2$µm, $l \times 2$µm, $l \times 3$µm, $l \times 3$µm, respectively, where l is the length of the contact window B to be measured, i.e., 2 µm, 4 µm, 6 µm or 10 µm. In this design, also the other contacts C, D, E and F are exposed to the boron deposition. This will increase the series resistance through the diffusion taps to the contact B without directly influencing the otherwise currentless measurement. Nevertheless, when this series resistance becomes very large it can limit the current that can pass through the contact B, thus the possible voltage drop over B can become too low to be measured accurately. This may occur for MΩ (megaohm) large contact resistances. In this case the measured contact resistance, R_{meas}, is the resistance over the boron layer R_{boron} given by:

$$R_{\text{meas}} = R_{\text{boron}} = \frac{V_{34}}{I_{12}} = \rho_{\text{boron}} \frac{Th_{\text{boron}}}{A_{\text{B}}} \tag{4.1}$$

where ρ_{boron} is the resistivity and Th_{boron} is the thickness of the deposited boron layer for a square contact window with an area of $A_{\text{B}} = l^2$. V_{34} and I_{12} are as indicated in Fig. 4.5.

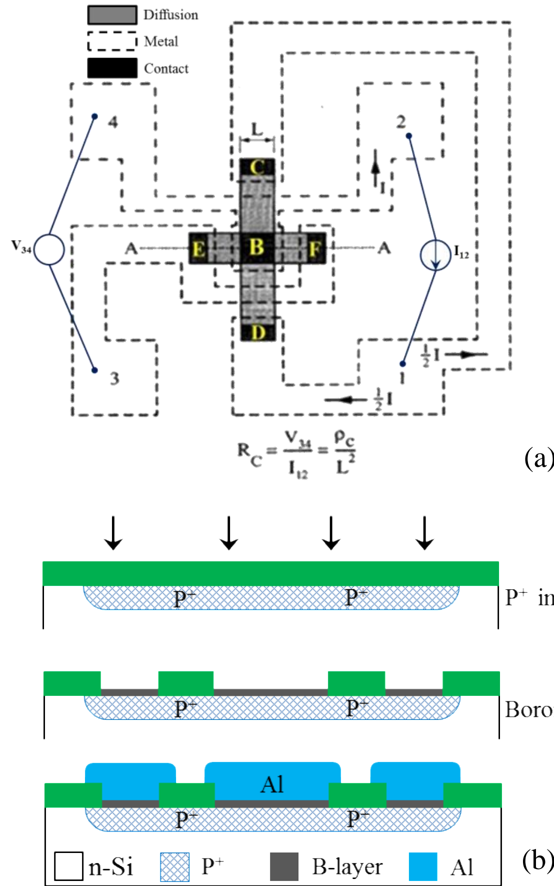


Fig. 4.5: (a) Layout of the cross-bridge Kelvin structure and (b) a schematic of the corresponding cross-section through the line A–A'.

b. Test structure fabrication

The devices are fabricated on 100-mm (4-inch), 2-5 Ωcm, n-type Si (100) substrates. A 220-nm-thick thermal oxide is grown on the wafers and patterned by wet etching in BHF. The boron layers of interest can be deposited in the temperature range from 400 °C to 700 °C. In this experiment depositions on the mm-large and the µm-sized windows are performed in the ASMI Epsilon 2000 and Epsilon One CVD reactor systems, respectively, at temperatures of either 700 °C or 450 °C. Deposition details were previously described in Chapter 2. In this thesis, the HT boron deposition is performed in the Epsilon 2000 reactor system at 700 °C.

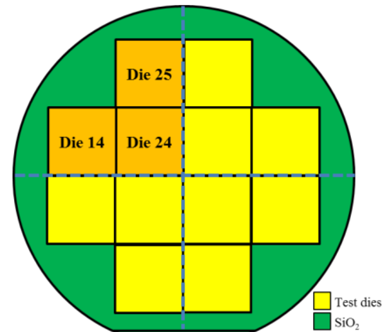


Fig. 4.6: Wafer-level layout of 20-mm-large dies.

Samples were *ex-situ* prepared for boron deposition as described in Appendix A. The important precaution that must be taken into account for deposition at 450 °C is that for this deposition there was no *in-situ* baking step and the wafers were directly loaded into the reactor at a deposition temperature of either 450 °C or 400 °C. The lack of *in-situ* baking makes the HF dip with Marangoni drying a very crucial step. Wafers must be loaded immediately into the N_2-purged load lock of the reactor to prevent any native oxide formation.

For the experiments on the mm-large windows, two deposition times, either 12 min or 19 min, are used to achieve boron layers thicker than 3 nm. The layout of the dies on the wafer in this case is shown in Fig. 4.6. There are 12 (20×20) mm^2 dies, and because of the rotation of the wafer during the boron deposition, the wafer can be divided into experimentally equal quarters as indicated in the figure, each quarter containing 3 dies of which we will examine 14, 24, 25 at the top right of the wafer. Dies 14 and 25 are near the edge and surrounded on two sides by large areas of oxide. In contrast, die 24 is surrounded by the large silicon areas of the other dies and is close to an oxide area only in one corner.

c. Results and discussion

Ellipsometry can be used for large windows to calibrate the boron layer thickness directly after deposition. From comparison with TEM images it becomes clear that ellipsometry gives an accurate thickness value for HT layers but not for lower temperature deposited layers (< 700 °C). At low temperatures the roughness of the layers increases as the deposition temperature decreases, and the ellipsometry seriously underestimates the thickness while overestimating the roughness, as can be seen from the values listed in Table 4.1.

The ellipsometry results of a scan made over the middle of the dies in a horizontal direction are shown in Fig. 4.7 for the HT deposition times of 12 min and 19 min. This scan shows that the thickness is largest when the surrounding oxide areas are large. This is in accordance with the loading effects and will be described later in this chapter in Section 4.4.

Fig. 4.8 shows the corresponding resistance of the 12-min and 19-min HT deposited boron layer, as measured on (10×10) μm^2 and (4×4) μm^2 contacts, for the same three dies (i.e. 14, 24 and 25) in Fig. 4.6. Fig. 4.9 shows the 2D contour mapping of the normalized resistance of the HT boron layer over these 3 dies for a 19-min deposition. The (4×4) μm^2 contacts are measured in arrays of 19×19 contacts in total. The increase in thickness near large oxide areas due to the loading effect is clearly visible and displays the same trend but with a much finer resolution.

The boron deposition has an incubation time that depends on the deposition parameters. Thus the thickness is not proportional to the deposition time, but the constant deposition rate means that the differential resistance between two different depositions is proportional to the differential deposition time. This is substantiated by Fig. 4.10, where over 1500 measurements on the dies treated in Fig. 4.8 and Fig. 4.9 have been compiled. For each of the four different contact sizes of (4×4) μm^2, (6×6) μm^2, (8×8) μm^2 and (10×10) μm^2, the differential resistance is linearly proportional to the differential deposition time. The same relationship is achieved over three consecutive runs and over the wafers. Therefore, for the CVD reactor conditions used in this experiment, the boron layer resistivity can be determined with high accuracy and is found to be 650 Ωcm. The extracted resistivity is also consistent and not dependent on contact size. Hereafter this linear graph can be used for translating measured resistance to the boron layer thickness and vice versa.

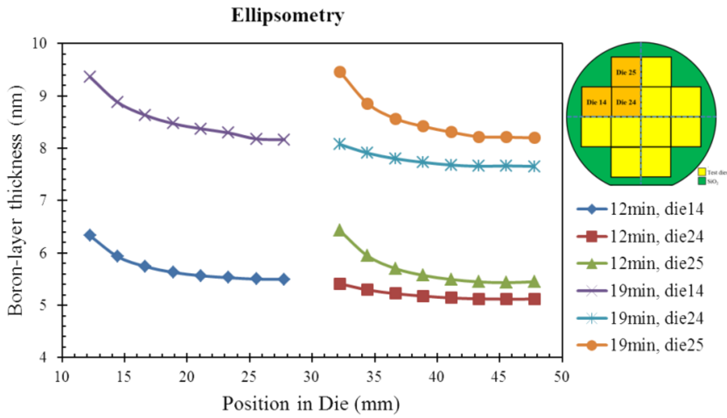


Fig. 4.7: HT boron layer thickness as a function of position in three (20×20) mm^2 dies and for a deposition time of either 12 min or 19 min, as extracted from ellipsometry measurements. The layout of the dies on the wafer is shown on the right.

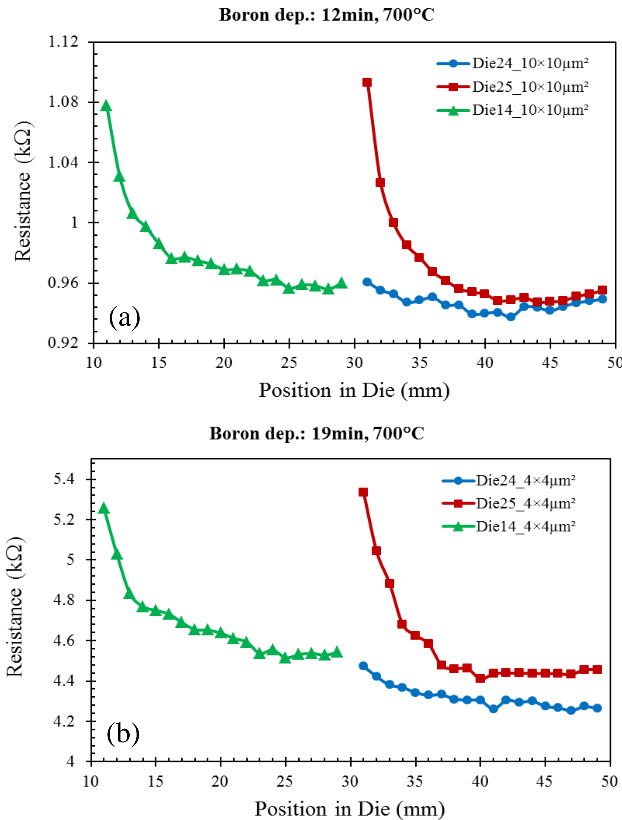


Fig. 4.8: Resistance measured on (10×10) µm2 (a) and (4×4) µm2 (b) contacts filled with the HT boron layer, over the same three dies as shown in Fig. 4.6.

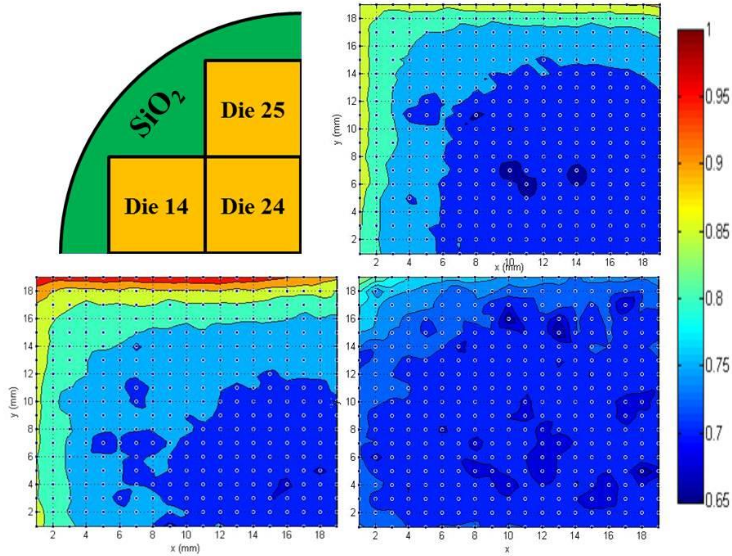


Fig. 4.9: 2D contour mapping of the normalized resistance of the HT boron layer over the 3 dies 14, 24 and 25, shown in the top left side of the figure; for a 19 min deposition measured on arrays of 19×19 contacts with size of (4×4) μm^2.

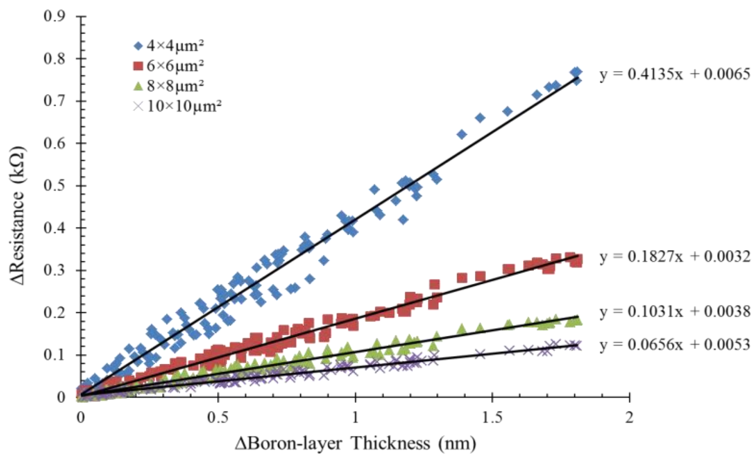


Fig. 4.10: The differential resistance of a HT boron layer as a function of differential thickness for over 1500 measurements of 6 different dies over the wafer for the 4 different contact sizes.

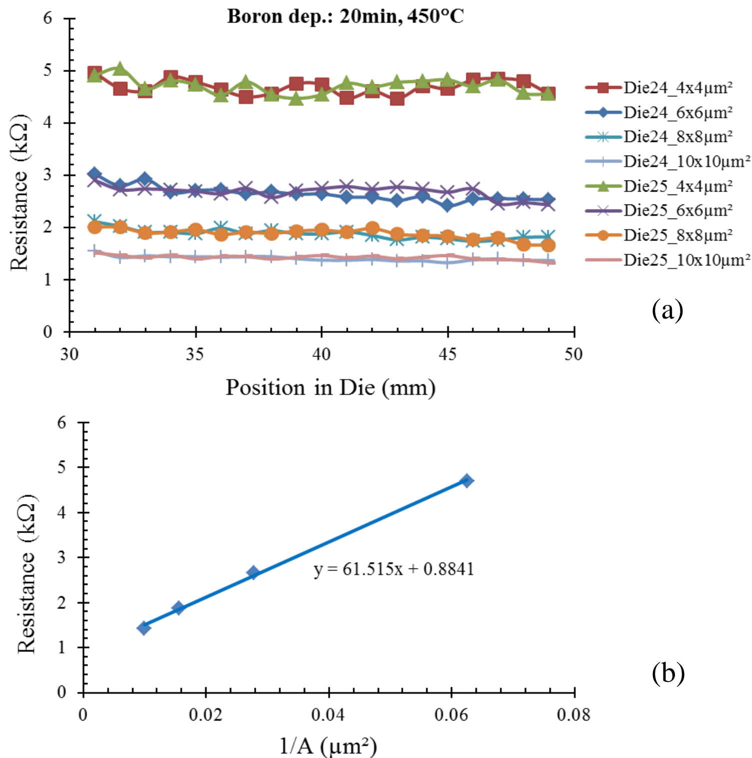


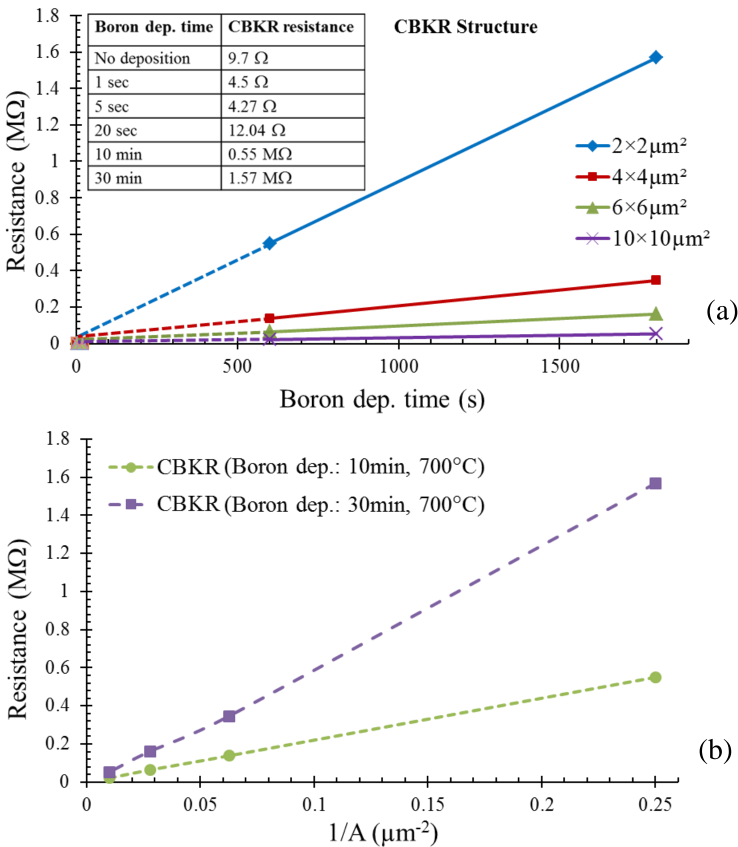
Fig. 4.11: Resistance of a 450 °C LT boron layer for 4 contact sizes, for dies 24 and 25 shown in Fig. 4.6, as a function of either (a) the position on the die or (b) the contact area.

For lower temperature deposition, it could be expected that the resistance measurement would be unreliable either because of poor adhesion of the Al metallization due to the rough surface or because of pin holes that could create low resistive paths. However, as shown in Fig. 4.11 the resistance displays high linearity with respect to contact sizes, which indicates that the high roughness of the layer does not inhibit a reliable resistance measurement. From the mapping over the large windows it is clear that there are no significant loading effects in this situation. This confirms earlier results indicating that loading effects are so small in low temperature depositions (< 450 °C) that the boron layer is deposited with the same thickness over the entire surface [123].

In the experiments with μm-sized windows, the HT (700 °C) boron layer was deposited in the ASMI Epsilon One system, which is only reserved for standard Si/SiGe depositions with different deposition times of 1 s, 5 s, 20 s, 10

min and 30 min, in several CBKR structures of Fig. 4.5, with B contact sizes of (2×2) μm^2, (4×4) μm^2, (6×6) μm^2 and (10×10) μm^2. Fig. 4.12 shows the extracted resistance versus boron deposition time, along with the contact size.

The contact resistance for the 2-min-long deposition time is plotted as a function of the contact area showing that it scales with the inverse value of the area in both cases. This means that for this set of small contacts, the boron thickness is the same even though the surrounding oxide area is quite different from device to device. This lack of sensitivity to loading effects confirms our proposed theory that the high mobility of boron atoms on both the oxide and silicon will eliminate thickness differences in this situation. This part will be discussed later in this chapter.



Boron dep. time	CBKR resistance
No deposition	9.7 Ω
1 sec	4.5 Ω
5 sec	4.27 Ω
20 sec	12.04 Ω
10 min	0.55 MΩ
30 min	1.57 MΩ

Fig. 4.12: Kelvin measurements of the resistance in small windows as a function of (a) boron deposition time and (b) the contact area (A). The inserted table gives the resistance in the (2×2) μm^2 contact windows.

The table included in Fig. 4.12a gives the resistance values for (2×2) μm^2 windows as a function of the boron deposition time. For the second shortest deposition time (5 s), the measured contact resistance first decreases before it starts to show an increase at the 20-s exposure time. A boron thickness for such a short exposure cannot be determined by ellipsometry. The Kelvin resistance measurement structure, on the other hand, is seen to be very sensitive to very small changes in the surface, i.e., boron and Si interface. The initial drop in resistance is perhaps due to an increased boron surface doping. The value only starts to increase after a complete boron layer is formed. This is, in first instance, a thin tunneling layer with a comparably much lower resistance than the thick layers.

The Kelvin resistance measurement of the two thickest boron layers was high enough to be measured reliably even by direct I-V measurement through the diffusion taps. Both resistance measurements gave the same result. From these values a boron resistivity of ~ 10^4 Ωcm could be extracted. This deviates strongly from the 650 Ωcm found for the Epsilon 2000 depositions. A plausible explanation is that the conditions in the two reactor systems that were used are so different with respect to background contamination that this gives a different doping/conductivity of the boron semi-metal material. From the general application of the equipment, it is expected that the Epsilon 2000 is much more contaminated than the Epsilon One, particularly with arsenic and Ge.

d. Summary

It can be summarized that with the applications presented in this section, end-of-line resistance measurements have been shown to be suitable as a non-destructive means of monitoring boron layer uniformity, as well as critical properties of the layer. This method is then used for the uniformity study presented next in this chapter.

The linear relation between measured resistance and boron thickness regardless of contact size provides a handy tool to measure thickness, while the fine resolution of the measurements makes it very useful for monitoring boron layer uniformity. Importantly, it must be taken into account that for this deposition technique it is not possible to assume a unique resistivity value even for otherwise similar deposition parameters due to dependency of the resistivity to the contamination background of the reactor. Therefore, resistance measurement cannot directly replace ellipsometry as a means of determining the

layer thickness. However, within one series of deposition, the resistivity of the layer appears to be uniform both over the wafer and from run to run. This means that by using a reactor with an unknown contamination background or in the case of changing any of the chamber conditions, first a resistivity measurement calibration is needed to find the boron layer resistivity for the new situation. Thereafter it is possible to use a direct resistance measurement method for thickness measurements as well as uniformity monitoring. For the HT process (standard deposition at 700 °C), which provides smooth layers, the deposition rate can be found with ellipsometry. The resistance measurements give a means of determining thickness distributions in windows where complex pattern dependencies have a large but unpredictable effect on the thickness. For deposited HT boron in the millimeter-large and micron-sized Si openings, deposition equipment-dependent resistivity values were found: 650 Ωcm in the more contamination-prone system and ~ 10^4 Ωcm in the other ultra clean one. This suggests that a doping of the boron layer could be the origin of a large drop in resistivity. In contrast to ellipsometry, the Kelvin measurement structures give the possibility of monitoring the boron deposition in micron-sized Si openings. The measurements confirmed that local loading effects will not determine the layer thickness in such small windows for HT deposition that is characterized by a high boron mobility along the wafer surfaces. This will be discussed later in this chapter in detail.

For lower temperature deposition, the layers are too rough for reliable interpretation of the ellipsometry measurements. However, despite this roughness, the direct resistance measurements are shown here to enable reliable monitoring of the relative layer thickness. The measurements confirm that there are no significant local loading effects as expected, since the boron mobility along the wafer surface is very small at such low deposition temperatures.

All in all, for all types of layers deposited in the temperature range of 400°C to 700 °C, the resistance measurements give a means of monitoring thickness variations with high resolution in both large and small windows on the silicon.

These measurements are used later to study the local loading effects of boron deposition on a micro-scale, where the diffusion length of boron atoms over silicon/boron surfaces is investigated. This value defines the maximum travel distance and/or time before boron atoms are deposited as a boron layer or desorbed from the surface to the gaseous phase.

4.2 Identification of the non-uniformity of the HT boron layer

The first step for optimization of the HT boron deposition process is to identify the non-uniformity of the boron layer, which is discussed in this section and the next.

As previously discussed, the very low penetration depth of VUV light and low energy electrons (less than 1 KeV) in solid materials makes these measurements a good indicator of the boron layer thickness uniformity on the diode surface. As an example, Fig. 4.13 presents the scan of the relative responsivity uniformity to a 121-nm light across the middle of three (10×10) mm^2 photodetectors, with non-optimized boron layer uniformity, for a thickness of: < 1 nm; 4 nm; and 14 nm. The detector principle is described in Chapter 2.

For this wavelength the attenuation length in silicon/boron is only 7 nm. So for the thicker layers, the non-uniformity due to the loading effects becomes very visible and almost cuts the responsivity at the edge of the photoactive anode area in half. This is the limiting point when a uniform responsivity is required over the entire active region of detectors, e.g. photodetectors for lithography machines.

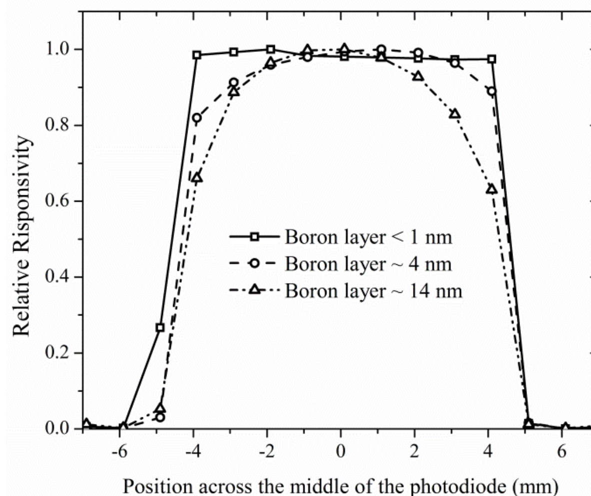


Fig. 4.13: Measured relative responsivity across the middle of 3 (10×10) mm^2 photodiodes with non-optimized boron layer uniformity, for a thickness of < 1 nm, 4 nm and 14 nm, respectively, and exposure to 121 nm light.

The sample with a 4-nm-thick boron layer was also used to determine the relative electron signal gain by using a low energy electron beam (LEEB) setup, as described in [60]. Fig. 4.14 shows a 2D contour plot of boron layer thickness uniformity and a 3D surface plot of the LEEB relative responsivity through the active area of a large (10×10) mm^2 detector extracted from 1 keV E-beam measurements.

First of all, it can be seen that the results, particularly in this case, are quite similar for different directions. Secondly it can be deduced that the boron layer thickness is almost symmetrical across the square window while it is not uniform. The boron layer is thinner in the middle, thicker at the edges where it is adjacent to oxide on the one side, and it is thickest at the corners of the window where it is adjacent to oxide on two sides. The responsivity graph, on the other hand, follows a reverse trend of the thickness uniformity. Therefore it can be concluded that the layer non-uniformity is related to oxide areas near the Si opening. The geometrical symmetry of the results is due to the symmetry of the design and the uniform oxide areas around the active area.

The same kind of design related symmetry can also be seen in Fig. 4.15a but not in Fig. 4.15b, where another kind of non-uniformity can be identified for segmented layouts, e.g. layouts presented in Fig. 2.12, when the coverage of the boron layer in different segments is not uniform. Fig. 4.15 presents a 2D map of boron layer thickness uniformity of two different designs of the electron detector, as extracted from 1 keV LEEB measurements.

In conclusion, the non-uniformity of the responsivity to low penetration beams such as VUV light, and less than 1 KeV electrons, are identified in association with boron thickness variations, which are related to the pattern dependency and local loading effect during the boron deposition. These two effects are mainly dependent on layout and process parameters.

In the following sections, first the device performance challenges that have risen from the non-uniformity of the boron layer will be discussed. Then a study of the pattern dependency and the local loading effects will be presented.

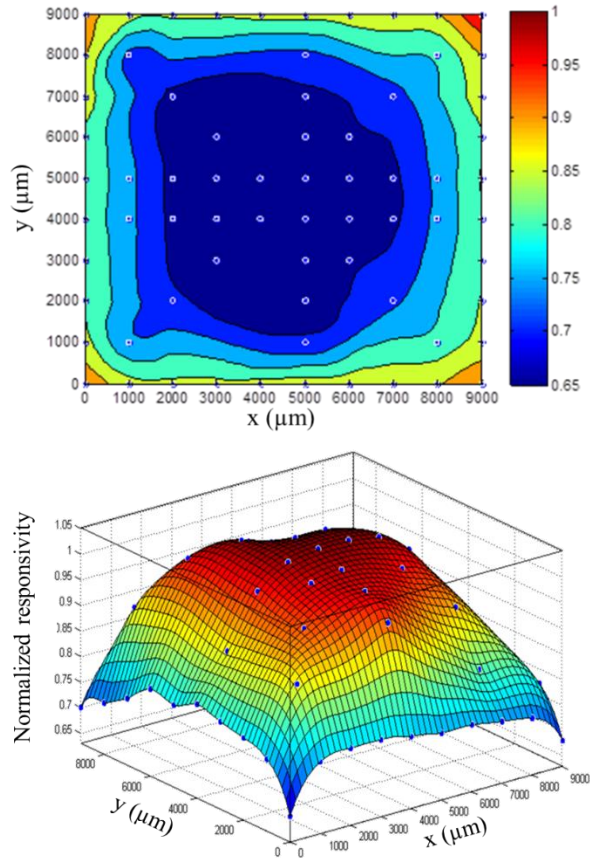


Fig. 4.14: (Top) 2D map of boron thickness uniformity and (bottom) 3D surface plot of the LEEB relative responsivity over the entire active area of a (10×10) mm^2 photodiode extracted from 1 keV E-beam measurements [60].

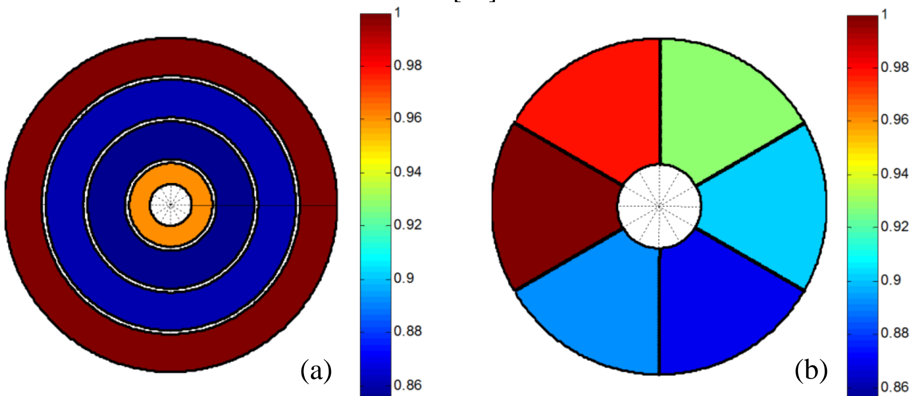


Fig. 4.15: 2D map of boron thickness uniformity of two different designs of the electron detectors. The contour plots are extracted from 1 keV LEEB measurements.

4.3 Effect of the boron layer non-uniformity on device performance

In this section, the consequences of the non-uniformity of the boron layer on the device performance are discussed.

The first consequence, as was indicated above, is the detector responsivity. Uniformity of the boron layer is a main factor for uniformity of the detector responsivity, especially to low penetration depth beams. The attenuation length of these beams in silicon and boron is only a few nanometers. Thus, to obtain higher responsivity, the thinnest possible boron layer that can be deposited uniformly over the entire active region of the diode is a high aspiration.

Photodetectors designed for lithography machines are one of the applications that demand high uniformity of the responsivity over the entire detector area. In this application, the uniformity is a key requirement because any undesired non-uniformity can degrade the accuracy of the machine, which is not acceptable. This is a real challenging point where, for example, the VUV responsivity presents a high non-uniformity as can be seen in Fig. 4.13 and Fig. 4.14. The non-uniformity of the responsivity was identified with a direct correlation to the boron thickness uniformity over the active region.

Another challenge being raised when segmented detectors, such as those used for electron detection in SEM systems, are considered. The example is shown and described in Fig. 2.12 (in Chapter 2) where the detector segments are configured in Concentric-Back-Scattered (CBS) mode and segments are grouped in 4 concentric rings. The SEM systems employ two contrast mechanisms for the imaging of the specimen: topographical contrast and material contrast. Typically, the material contrast (atomic number Z) corresponds to the sum of the recorded signals from all the detector segments, while the topography is obtained by subtracting the signals thus producing the so-called “shadowing” images [124]. In this situation, uniform coverage of the boron layer over all segments and/or rings is a key point when thickness variation of this layer is identified as a source of responsivity variations. However, it has been found that the boron coverage is not uniform, as shown in Fig. 4.15. The outermost and innermost segments have a thicker boron layer, compared to the inner segment, due to adjacency to an oxide area. The SEM images of uncoated pollen sample taken from each segment is also shown in Fig. 4.16 [21].

It can be seen that the signal contrasts of the outermost and innermost rings are somewhat weaker than the contrasts obtained for the inner rings. This is in resemblance to the boron thickness in correspondence to the rings as presented in Fig. 4.15. Thus it can be concluded that besides the difference in the angle of incident for these rings which causes differences in signal contrasts, non-uniform coverage of the boron layer over the 4 rings of the detector might also in-part, play a role. Another example can be taken from the design shown in Fig. 2.12c. A similar non-uniform coverage of the boron layer can be seen in Fig. 4.15b where the thickness variation of about ~ 0.5 nm can be detected between different sectors of a die which is not acceptable for very high accuracy applications.

Therefore, before any attempt to improve the detector performance, it is crucial to study the source of the boron layer non-uniformity and to try to minimize it. In the next sections, pattern dependency and local loading effect of the HT boron deposition are studied as potential sources of non-uniformity. Methods are proposed for achieving uniform 2-nm-thick boron layer deposition.

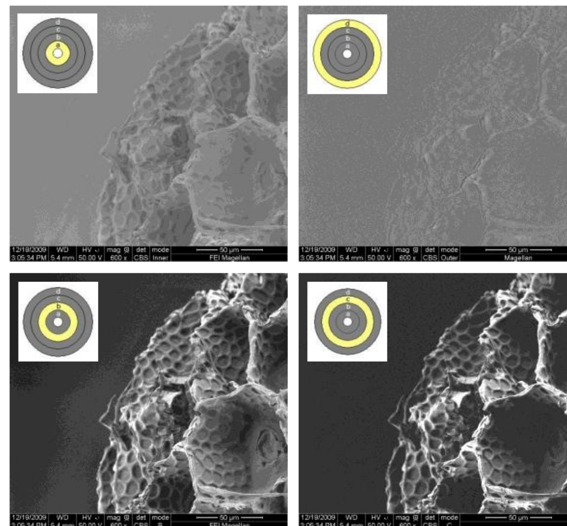


Fig. 4.16: Uncoated pollen sample imaged at 50 eV landing energy for each segment in Concentric Back-Scattered mode, as showed in the inset [21].

4.4 Sources of boron layer thickness non-uniformity

The boron deposition is susceptible to loading effects and pattern dependency due to the selectivity of the deposition between the Si and SiO_2 surfaces at higher temperatures like 700 °C. Besides this, the recipe and layout parameters can also act as a source of non-uniformity by either introducing and/or enhancing it. The recipe parameters can be: the deposition temperature, the diborane gas distribution, and the gas flow profile over the wafer. The gas flow profile and temperature distribution is investigated for different wafer rotations by CFD simulation in Chapter 3.

The layout parameters can be: (i) the total ratio of the silicon to oxide areas, also called the global oxide ratio (GOR: area of SiO_2/wafer); (ii) the local ratio of the Si opening to nearby oxide region, referred to as the local oxide ratio (LOR: local area of SiO_2/Si). Regarding the size of the opening window, as in Fig. 4.14, we can see that more non-uniformity occurs for centimeter-large openings.

In this section, pattern dependency and the local loading effect of the HT boron deposition are investigated. Experiments have been conducted to identify the impact of the recipe and layout parameters on these two effects in order to control and minimize them. The local loading effect is studied at the macro-scale where the impact of the local oxide areas on the boron layer thickness at the middle of the millimeter-large openings is considered, and an empirical model is employed to describe this effect. The local loading effect is also investigated at the micro-scale where the layer profile inside the opening is studied. As a result of this study, the diffusion length of boron atoms at deposition temperatures 700 °C, 500 °C and 400 °C, over the silicon or boron surfaces, is extracted as the maximum distance that boron atoms can travel along these surfaces before deposition on the substrate or desorption to the main gas stream occurs at these temperatures.

At the end, on basis of the knowledge obtained in this and previous chapters, some methods are proposed for depositing a uniform 2-nm-thick HT boron layer with thickness variations of only a few angstroms.

4.4.1 Pattern dependency of the boron deposition

In this section the pattern dependency of the boron deposition is studied for different Si opening window sizes and distributions. The loading effects

observed are similar to those found for selective epitaxial growth (SEG) of Si and SiGe layers [64-66]. Differences in the deposition rate of the deposited layers are correlated to both the Si/SiO_2 surface ratio over the wafer as a global effect, and the size of the windows in relation to the pattern of the surrounding oxide areas as a local effect (details in Section 4.4). This pattern dependency must be taken into account when applying the boron deposition to devices where the boron layer thickness is critical, e.g., in photodiodes for detecting DUV/VUV light [53] and electrons with energies below 1 keV [21]. Significant non-uniformity can be found when the window dimensions are in the millimeter range or higher (for example see Fig. 2.23 in Chapter 2). Here we focus on determining the global effects on large area windows by using measurement techniques such as SIMS and ellipsometry. Several methods have already been proposed to decrease the pattern dependency and/or the loading effect for the SEG of Si and SiGe [89, 125-127]. However, to the best of our knowledge, this is the first reported effort to research the reproducibility and the pattern dependency of boron depositions, including the loading effects. An optimization of the deposition parameters is performed for 700 ºC (HT) depositions, at either atmospheric (ATM) pressure or 60 torr, with respect to uniformity over the wafer with and without a patterned oxide coverage. As a result, deposition procedures are proposed for achieving a well-controlled deposition rate with very low pattern dependency.

The experimental part of this work was performed on 100-mm 2-5Ωcm n-type Si (100) substrates [119]. A 220-nm-thick thermal oxide was grown on some wafers and patterned by wet etching in BHF. The HT boron deposition was performed at 700 ºC in an ASM Epsilon 2000 CVD reactor as described earlier in Chapter 2.

Eight samples in four groups with different pattern sizes and different oxide coverage ratios (OCR) were used in this study to investigate pattern dependency, as presented in Table 4.2. The oxide coverage ratio can be defined here as the ratio of the oxide masked area to the entire surface area of the wafer:

$$\mathrm{OCR} = \frac{S_{\mathrm{SiO_2}}}{S_{\mathrm{wafer}}} \tag{4.2}$$

Ellipsometry measurements were used to measure the thickness of the deposited boron layer at the middle of millimeter- to centimeter-sized windows in SiO_2. For wafers without any oxide coverage the measurement was performed in the middle of the wafer.

Table 4.2: Description of the samples.

Sample	OCR (%)	Window area (mm^2)	Comment
SW-58	58	43.7	and many small windows
SW-71	71	7.68	and many small windows
6LW-80	80	50, 75, 100, 200, 300, 400	6 window sizes
4LW-80	80	100, 200, 300, 400	large windows of different sizes
14LW-80	80	100	fourteen windows
LW-SiOpen	71	100, 81	27 dies
LW-Oxide	72	81	27 dies
LW-SiDies	75	81	24 dies

The influence of the deposition parameters defined in the recipe (i.e. pressure, temperature and gas flow), and the structural parameters presented in the layout (i.e. aperture size, oxide coverage ratio), on the pattern dependency and/or loading effects of the boron layers, is a complicated issue since the parameters can be interdependent. Ideally, a deposition should be completely independent of the size/geometry of the openings. However, in reality, many effects play a role due to the non-uniform gas consumption over different window sizes and different lateral gas diffusion because of global and local loading effects. The exact origin of the pattern dependency is a complex combination of chemical, kinetic, and thermal factors, which are evaluated here in a systematic experimental study.

Effect of oxide coverage and window size

In order to investigate the effect of the: (i) silicon opening size and (ii) the oxide coverage on the wafer (OCR) on the boron thickness uniformity, the deposition rate is compared for samples SW-58, SW-71 and 6LW-80. In Fig. 4.17 the dependency is plotted as a function of OCR for wafers with different patterns. As the oxide coverage ratio goes from 0 to 80%, the deposition rate increases to about 85%.

Also plotted in Fig. 4.17 is the deposition rate as a function of the window size for the same OCR. All measurements were performed on wafer 6LW-80, which means that there was no influence from global effects. Due to a loading effect, the deposition rate increased as the feature size of the Si windows decreased. These results demonstrate the general trend that the deposition rate

will increase as the area covered by oxide increases globally, as well as in the direct vicinity of an opening to Si. These trends are related to the selective nature of the deposition and are also well known from the selective silicon epitaxy [65, 66].

CVD deposition on blanket wafers may be described using the classical boundary layer theory [128]. In this theory, a laminar gas stream is flowing over the wafer. Due to the frictional force between the gas stream and the stationary susceptor/substrate, a stagnant/low velocity boundary layer arises. Therefore the main gas transport mechanism through this boundary layer is diffusion. With the reaction of the reactant species with the surface atoms and subsequent deposition, the boundary layer will become depleted if the net deposition reaction is faster than the diffusion. Over this boundary layer, the gas is assumed to be well mixed and moving at a constant speed, *u*. To determine the thickness of this boundary layer, the balance of the frictional and accelerating forces on a gas element yields a boundary layer thickness, δ, as a function of the position, *x*, over the susceptor/substrate: $\delta(x)=A(\mu x/u)^{1/2}$, where μ is the gas kinematic viscosity and A is a constant. However, the thickness of this boundary layer is not easy to calculate precisely. Several unknown parameters are involved.

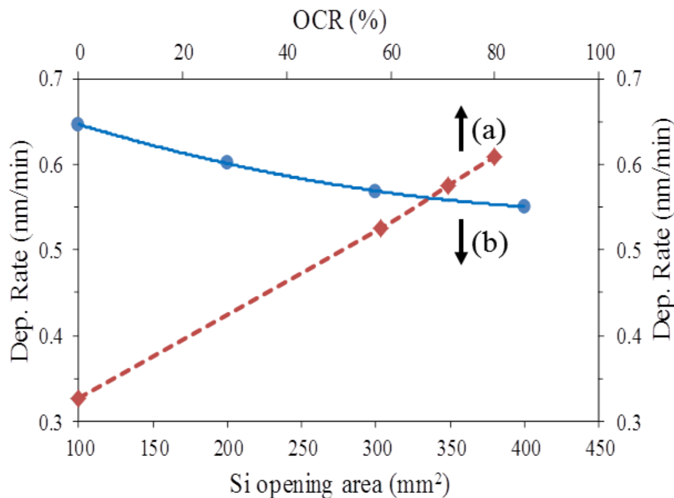


Fig. 4.17: Deposition rate of the boron layer as a function of: (a) the oxide coverage ratio (dashed line) for a wafer with no oxide for samples SW-58, SW-71 and 6LW-80, and (b) the area of the individual oxide windows to Si for sample 6LW-80, i.e., with a constant OCR of 80% (solid line).

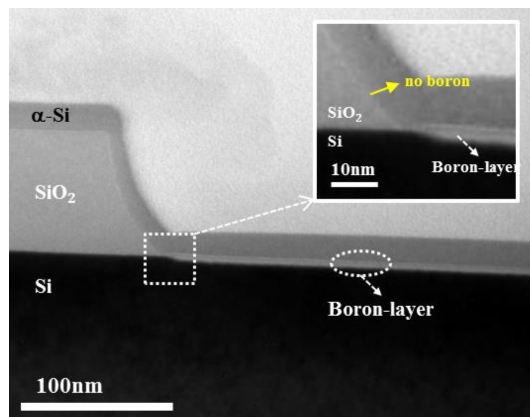


Fig. 4.18: TEM image of a boron layer directly formed in a contact window during a 6-min B_2H_6 exposure at 700 °C.

For example, the kinematic viscosity and the gas velocity are highly dependent on the actual gas temperature, which can be significantly different from the susceptor temperature. This is typical for lamp-heated cold wall reactors, where the temperature is controlled by thermocouples located in the susceptor. A rough approximation of the magnitude of this boundary layer yields values in the centimeter range. This means that the reactant species have to diffuse vertically within a range of centimeters. However, diffusion will also occur laterally if there are any concentration gradients over the wafer (which is the case for selective deposition on substrates with varying window sizes). This implies that the gas phase depletion gradient may be significant (in the centimeter range) both vertically and laterally.

In the case of boron depositions, it was found that no boron is deposited on the flat or beveled SiO_2 surfaces, as confirmed by the TEM image in Fig. 4.18. Therefore, the boron atoms on the oxide are floating and move around on the surface thus creating higher concentration boron atoms that will give a higher lateral diffusion on a patterned wafer surface than on a bare-Si wafer. Consequently there is an increase of the probability of the boron atoms sticking to the Si surface of the open windows. In this way an increase of the amount of oxide area around the window will result in an increase of the boron layer thickness on the silicon surface of the window.

Impact of deposition parameters on pattern dependency

A series of reports on the SEG of Si and SiGe have shown that the pattern dependency can be reduced by tuning the growth parameters [89, 125-127]. Here the boron layer was deposited at both atmospheric pressure (ATM) and 60 torr, on several patterned wafers with ~80% OCR and opening areas of 100 mm^2, 200 mm^2, 300 mm^2 and 400 mm^2. Deposition was performed with different diborane partial pressures and main gas flows, where P_1 (F_1) was the maximum diborane partial pressure (main flow), and P_2 (F_2) and P_3 (F_3) were 75% and 50% of the maximum values, respectively. The boron deposition rate is shown in Fig. 4.19 as a function of these parameters. In each figure the corresponding deposition rate for bare wafers is also shown. The results show a reduction in the pattern dependency with decreasing diborane partial pressure as well as the main gas flow (Fig. 4.19a and b). Moreover, no significant improvement in the pattern dependency was observed when decreasing the total pressure from ATM to 60 torr, see Fig. 4.19c.

In order to verify the effect of the deposition parameters and the surrounded oxide areas on the pattern dependency and/or deposition rate of boron, the pattern which is shown in Fig. 4.20 (samples 14LW-80) was designed. The boron was deposited over this pattern where 14 oxide windows to the silicon, each (1×1) cm^2 in size, are positioned so that the surrounding oxide area is different in each case. This gives different loading effects and therefore different boron deposition rates.

In Fig. 4.21 the results are shown for different diborane partial pressures and main gas flow combinations. As can be seen in this figure, e.g., dies no. 3 and 5 have a higher deposition rate due to the larger amount of adjacent oxide area and die no. 11 has a lower value because it is located near two other dies and close to the edge of the wafer with less surrounded oxide area. The large variations become very small when the diborane partial pressure and main gas flow are low. However, as seen in Fig. 4.21b, the deposition rate variation is not significantly changed by reducing the total pressure from ATM to 60 torr.

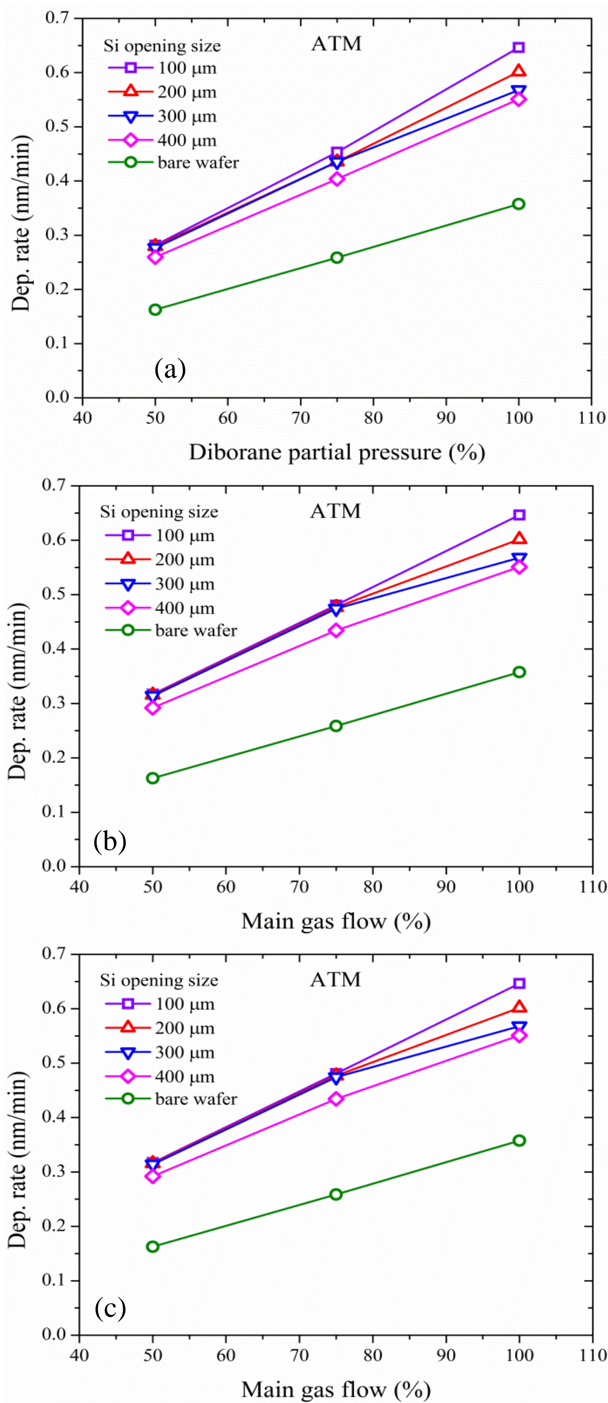


Fig. 4.19: The boron deposition rate as a function of: (a) diborane partial pressure, (b) main gas flow at atmospheric pressure, and (c) diborane partial pressure at 60 torr, for different window sizes as well as for a bare Si wafer.

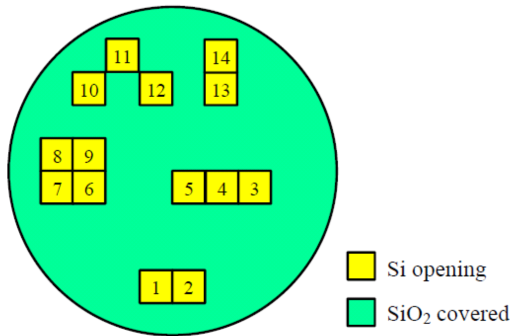


Fig. 4.20: Patterning of samples 14LW-80.

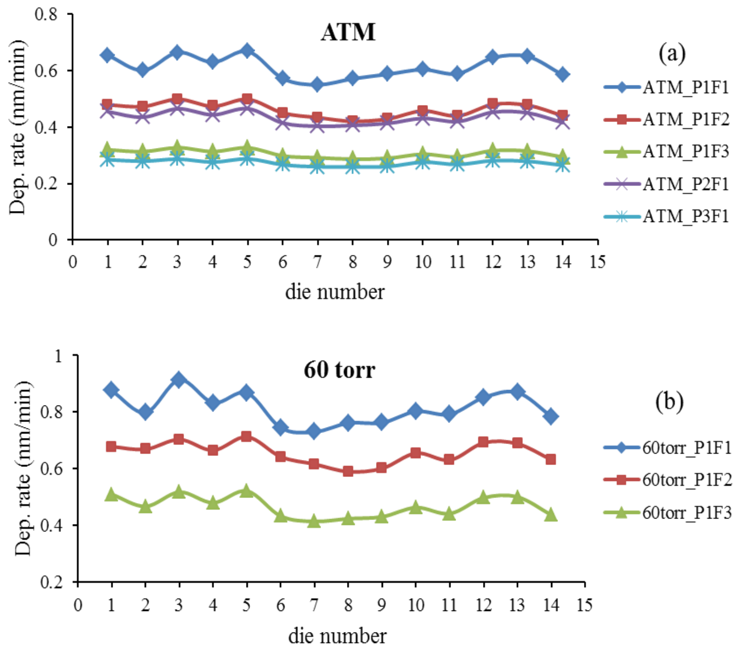


Fig. 4.21: Boron deposition rate plotted against the die number for a wafer patterned with 14 (1×1) cm^2 dies as in the wafer layout of Fig. 4.20, for different deposition parameters at: (a) atmospheric pressure and (b) 60 torr pressure. Here, P_1 (F_1) is the maximum diborane partial pressure (main gas flow), and P_2 (F_2) and P_3 (F_3) are 75% and 50% of the maximum values, respectively.

These results show that for atmospheric pressure, the deposition rate for maximum diborane partial pressure and maximum main flow (P_1F_1) varies the most due to a high pattern dependency and/or loading effect from the surrounding oxide areas. However, with a decrease in the diborane partial pressure or the main flow (i.e. P_1F_2, P_1F_3, P_2F_1, and P_3F_1) this effect is mitigated, which results in all dies with not only any adjacent oxide areas, but also with a different width (e.g. dies no. 6, 7, 8 and 9 together), having the same deposition rate. At the same time the total deposition rate is decreased, as would be expected. This experiment shows that it is possible to adjust the deposition parameters so that the loading effect of the oxide areas can be regulated to give a uniform and equally thick boron layer in all dies of a patterned wafer.

Impact of the wafer layout on layer uniformity

As already discussed, the layer uniformity depends on the loading effects and the surrounding oxide areas. This means that the larger the surrounding oxide area is at the deposition site, the thicker the boron layer is. As a result, a special wafer layout can provide better layer uniformity, and eventually higher device performance.

Therefore an experiment was done with three distinct wafer layouts of RG, RM and CDE as described below and shown in Fig. 4.22, all of which correspond to the circular detector geometry shown in Fig. 2.12 in Chapter 2 with a (10×10) mm^2 die size.

1- Regular wafer layout (RG): standard wafer layout used for exposure of the process wafers. It can be divided in two parts: main part and surplus margin. All dies are located in the main part as indicated by the solid red line in Fig. 4.22. This part is surrounded by a surplus margin which is not used for device fabrication purposes, and is usually covered with oxide (Fig. 4.22a).
2- Remove Margin wafer layout (RM): RG layout with the oxide of the surplus margin etched away (see Fig. 4.22b).
3- Continuous Dies to the Edge wafer layout (CDE): the surplus margin of the RG layout is patterned by the same mask which is used to expose the main wafer area, as shown in Fig. 4.22c.

The boron layer is deposited in all three of these wafer layouts under the same deposition condition (6 min, 700 °C). The layer thickness is measured by the ellipsometry technique in different positions along the wafer at the middle of the circular openings (as indicated by dashed blue line in Fig. 4.22). The results are shown in Fig. 4.23.

It can be seen from the boron layer thickness measurements that the middle dies in the RG layout have a lower boron deposition rate than the edge dies. The loading effect is the cause of the huge amount of oxide at the surplus margin of the wafer that supplies additional boron to the outer dies, thus creating die-to-die thickness variations [119, 129]. Therefore, the surplus margin oxide is removed in the RM layout. However, this does not improve the layer uniformity since in this case the outer dies have a lower deposition rate compared to the central dies, due to "consumption" of boron at the large Si areas of the surplus margin [119, 129]. To achieve an optimized loading/consumption effect of the surplus margin area at the middle of the wafer, the same oxide-etch mask design is applied for the surplus margin area as for the main wafer area, as shown in the CDE layout in Fig. 4.22c. This guarantees that all the dies have the same loading effect and, consequently, the same boron deposition rate is obtained, as shown in Fig. 4.23.

The situation is further complicated by the fact that the oxide openings of electron detectors are typically segmented (e.g. 2D contour plots given in Fig. 4.15 based on the designs of Fig. 2.12 in Chapter 2). Since it is a key point that all the segments have the same performance, for this reason it is crucial to deposit the same and uniform boron layer inside each segment. To investigate this, the wafer layouts of the RG and CDE were used with the detector geometry of Fig. 2.12c, with a (20×20) mm^2 die size. The boron was deposited (6 min, 700 °C) and the layer thickness was measured by ellipsometry. The results are shown in Fig. 4.24 and Fig. 4.25. In these figures the solid red and dashed blue lines show both the boundary of the main dies, and the test dies measured for boron layer thickness, respectively. The table included in the figures shows the statistics of the ellipsometry measurements of the deposited boron layer.

As can be seen in Fig. 4.24 there is an enormous thickness variation inside the segmented dies (~ 0.5 nm) and also between segments of the inner dies and outer dies (up to 1 nm). These thickness variations are not acceptable especially for low penetration beam applications where a reliable and uniform 2-nm-thick

boron layer is needed with only 10% acceptable thickness variation. Fig. 4.25 shows much less thickness variation for the CDE layout of only 4 angstroms throughout the wafer.

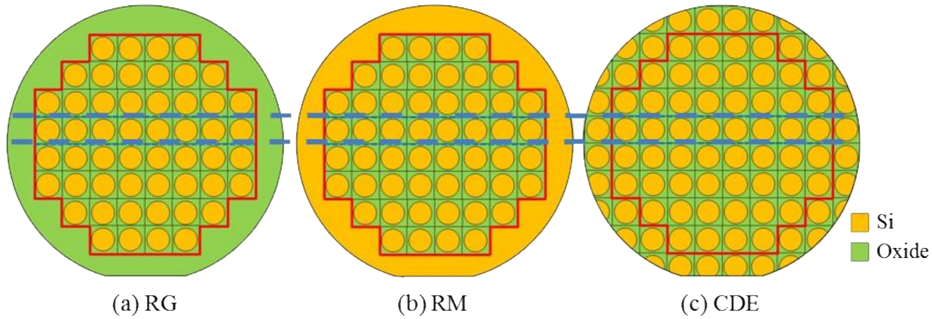


Fig. 4.22: Different wafer level designs of the oxide-etch mask: (a) Regular layout (RG), (b) Remove Margin layout (RM), and (c) Continuous Dies to Edge layout (CDE). The red line shows the boundary of the main dies, and the dashed blue lines mark the test dies for which the boron layer thickness is measured.

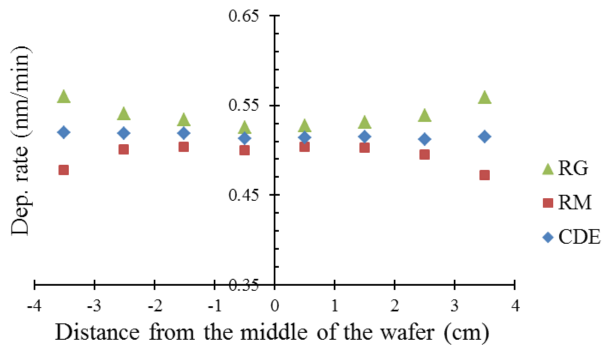
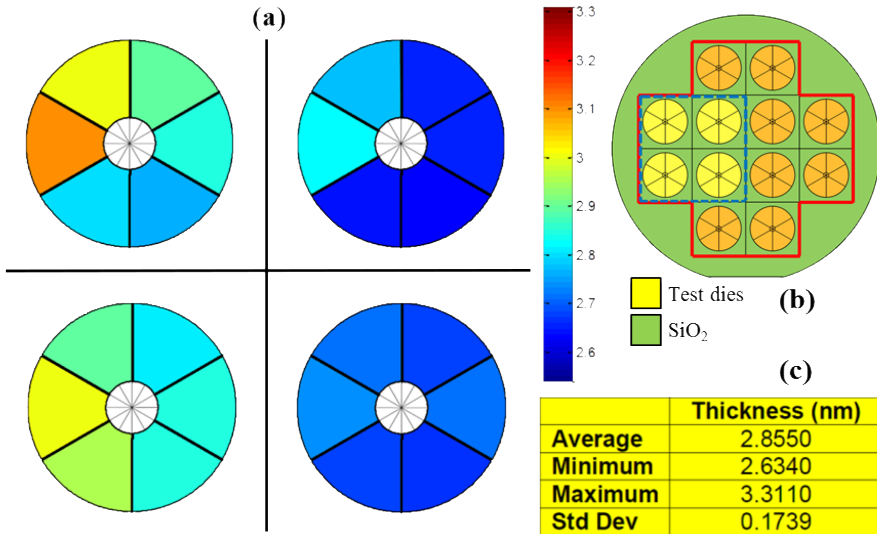
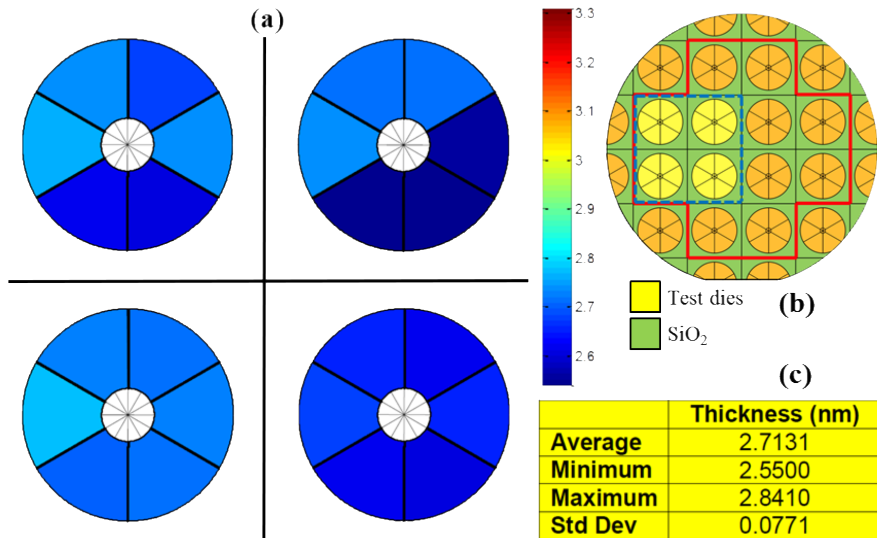


Fig. 4.23: The boron deposition rate versus distance from the middle of the wafer for the RG, RM and CDE layouts of Fig. 4.22 at 700 °C.



	Thickness (nm)
Average	2.8550
Minimum	2.6340
Maximum	3.3110
Std Dev	0.1739

Fig. 4.24: (a) 2D contour plot of boron layer thickness for the RG wafer layout over the segmented electron detector geometry of Fig. 2.12c; (b) the Regular wafer layout (RG) where the red line shows the boundary of the main dies, and the dashed blue line marks the test dies for which the boron layer thickness is measured; and (c) statistics of the ellipsometry measurements of the deposited boron layer.



	Thickness (nm)
Average	2.7131
Minimum	2.5500
Maximum	2.8410
Std Dev	0.0771

Fig. 4.25: (a) 2D contour plot of the boron layer thickness for the CDE wafer layout over the segmented electron detector geometry of Fig. 2.12c; (b) CDE wafer layout where the red line shows the boundary of the main dies, and the dashed blue line marks the test dies for which the boron layer thickness is measured; and (c) statistics of the ellipsometry measurements of the deposited boron layer.

It can be concluded that the wafer layout has an impact on the final boron layer uniformity over the wafer. The presented results prove that the CDE wafer layout guarantees a similar loading effect for all dies, resulting in a similar boron deposition rate. It is finally shown that by: (i) using a CDE layout instead of a RG layout, (ii) optimizing the boron deposition parameters, and (iii) considering additional optimization methods (as will be discussed next), it becomes possible to deposit a reliable, uniform, reproducible 2-nm-thick boron layer with only thickness variations of a few angstroms over the patterned wafer.

Verification of the gas depletion in the boundary layer

As discussed previously, the windows to the Si consume the diborane species and cause gas depletion inside the boundary layer over the windows. Therefore the diborane species have to diffuse through the stationary boundary layer width from the main gas stream to reach the surface of the wafer, which is schematically illustrated in Fig. 4.26. As already shown, the boron atoms cannot stick onto the oxide areas, and because of this the boron concentration is increased over these areas. When the lateral gas diffusion is increased, it creates a local boundary layer over each opening, as is shown by the yellow arrows in the Fig. 4.26.

Generally, many different windows with different distances from each other are found on each die or wafer, and the deposition rate will also be influenced by the proximity to neighboring windows. This can be placed in relation to the width of the opening windows, W_{Si}, and width of the oxide, W_{ox}, separating the windows. This situation is shown schematically in Fig. 4.27.

To verify the boundary layer thickness and the range of gas depletion in the boundary layer, boron was deposited on wafers patterned as shown in Fig. 4.28. Three wafers were processed with the area designated as the “reference” area and filled in different ways:

LW-SiOpen: one big window to the Si,
LW-Oxide: covered by oxide,
LW-SiDies: three (10×10) mm^2 dies are opened as separated windows to the Si.

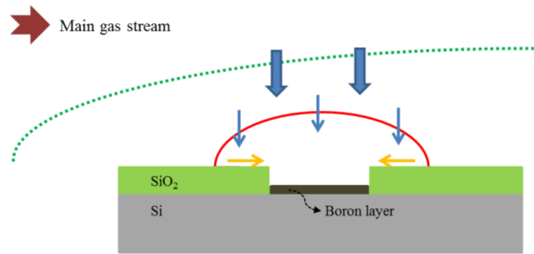


Fig. 4.26: Schematic illustration of the local boundary layer over a window to Si due to the lateral diffusion of the boron species.

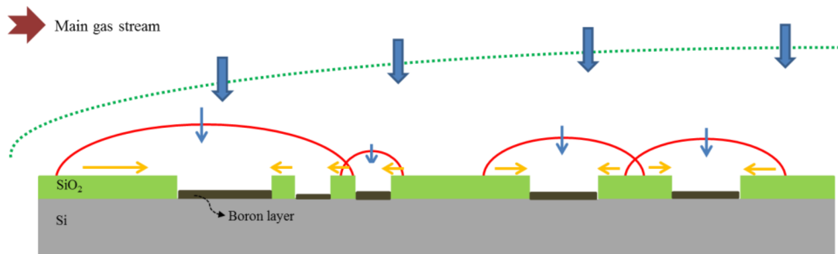


Fig. 4.27: Schematic illustration of the local boundary layers and their impact on the final boron layer thickness for a die design where equal windows or oxide separation sizes result in different thicknesses.

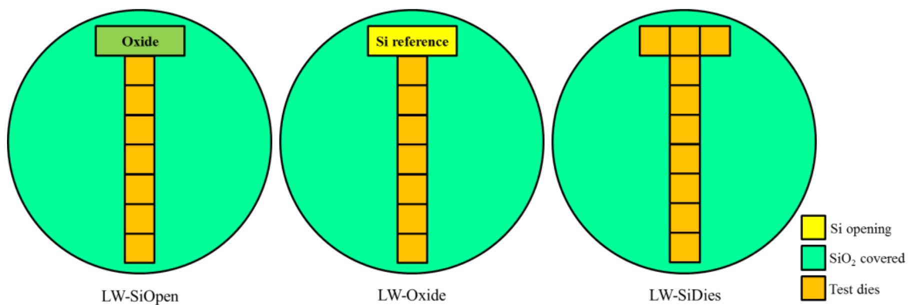


Fig. 4.28: Patterning of wafers where the “reference” area is filled in different ways for samples LW-SiOpen, LW-Oxide and LW-SiDies.

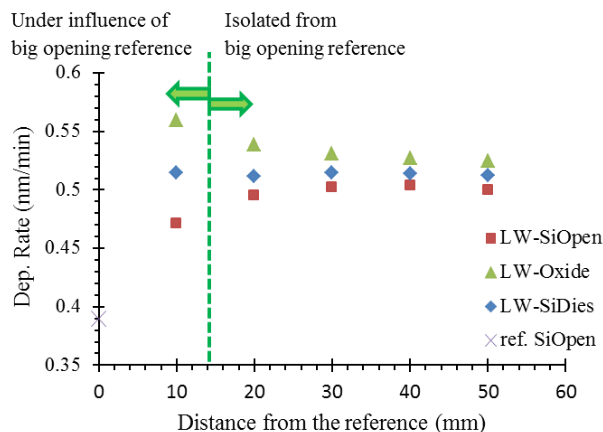


Fig. 4.29: Deposition rate of boron in a row of five (1×1) cm^2 test dies adjacent to a (3×1) cm^2 die placed as the "reference" area shown in Fig. 4.28, for three different fillings of this area as defined for the samples LW-SiOpen, LW-Oxide and LW-SiDies. The deposition rate in the "Si reference" area for sample LW-SiOpen is included for comparison.

If the dominant transport mechanism is diffusion and the boundary layer thickness is in the order of centimeters, then the extent of gas depletion from a large opening should also be in the order of centimeters. Fig. 4.29 shows the deposition rate of boron in the (10×10) mm^2 Si openings at different distances from the "reference" area for the three samples. For comparison, the boron deposition rate in the "reference" area for sample LW-SiOpen is included. The curve for design LW-SiOpen reveals two distinct regions. Close to the reference area, the smaller openings have a low deposition rate which is lower than that of the dies that are further away and not impacted by the depletion volume of the large reference opening, as schematically indicated in Fig. 4.27. In this volume, a significant portion of the gas molecules is consumed by this large opening, and the diborane available for the surrounding dies is reduced. As the distance is increased, the deposition rate is also increased until saturation is reached at a distance of around 1-1.5 cm.

The curve for the LW-Oxide design also has two distinct regions. In this design the "reference" is covered by the oxide. The loading effect of this oxide area increases the deposition rate of the closest open dies. It can also be deduced that the gas-phase diffusion length of boron atoms on the oxide area should be around 1-1.5 cm, which is about 1-1.5 times the Si opening width. From Fig. 4.29 it can be deduced that when the "reference" area is patterned with

separated open dies of the same area as the five dies forming the monitoring row, then the dies do not have a distinguishable impact on each other. All in all, it can be concluded that considering the fact that the smaller openings display the same deposition behavior as the nearby larger opening, any micro-loading effects are minimal. In other words, there is no dependence on the opening size, but the local Si coverage is very important. It should be noted that the uniformity of the deposition over a blanket wafer under these deposition conditions was checked and the non-uniformity was less than 2%. Therefore the distribution of the boron layer thickness over these test wafers supports the picture of the deposition and associated pattern dependency of boron CVD deposition as illustrated by Fig. 4.27.

To summarize, it has been demonstrated that the deposition rate of boron layer can vary over the wafer depending on the Si opening size and OCR of the mask design as well as wafer layout. The higher the OCR is, the higher the deposition rate will be, and the deposition rate also increases as the size of the windows to the Si decreases. This has been explained in terms of the gas depletion of the diborane species in the stationary and/or local boundary layer. The results show a reduction in the pattern dependency with decreasing diborane partial pressure as well as main gas flow. Moreover, no significant improvement in the pattern dependency was observed when decreasing the total pressure from ATM to 60 torr. Thus, conditions were found that can be used together with the CDE layout instead of the RG layout, that make it possible to control pattern dependency and loading effects to such a degree that the 2-nm-thick boron layer used in existing applications can be deposited uniformly with variations in thickness of only a few angstroms.

The diffusion length of boron on the oxide surface in the order of centimeters is found to be in relation to the Si opening width. The loading effect in micron sized windows therefore will not lead to thicker layers than seen in the larger windows. This confirms the investigation results presented in Section 4.1.1, where the Kelvin resistance measurements of micron-sized Si openings showed that the high mobility of the boron atoms at 700 °C eliminate thickness differences in this particular situation.

4.4.2 Local loading effect of the boron deposition

During the boron deposition, the source of boron atoms can be divided into a vertical and a lateral component, both of which supply reactant molecules to the wafer surface available for the deposition. The lateral component is responsible for the so-called local loading effect that occurs because the boron does not deposit on oxide but diffuses along the surface. The importance of this component will depend on the patterning of the wafer (i.e. the oxide coverage ratio, window sizes and also the local W_{ox}/W_{Si} ratio or briefly the LOR) as well as the boron diffusion lengths on the oxide and silicon.

In this section the local loading effect of the boron deposition will be investigated at the macro- and micro-scale [129]. At the macro-sale the investigation is limited to the influence of the LOR on the final boron layer thickness at the middle of the millimeter-large Si opening window while the micro-scale investigates the uniformity profile of the deposited boron layer inside the opening with micrometer resolution. With the results of this investigation valuable information is extracted about the diffusion length of boron atoms along silicon and boron surfaces in the deposition temperature range of 700°C to 400°C, which presents the maximum distance that boron atoms can travel along the surface before being deposited (as a layer) or desorbed back to the main gas stream. Moreover, the results are used for developing a comprehensive model to predict the boron deposition rate on any 2D uniformly or non-uniformly patterned wafer such as those used for advanced device fabrication, as presented previously in Chapter 3.

a. Macro-scaled investigation of the local loading effect

This section discusses the lateral source of boron species which comes from the oxide-covered areas. It not only causes the local loading effect during the boron deposition, but also has an impact on the final boron layer thickness at the middle of the millimeter-large Si opening window. An empirical model is employed to describe this effect. A more detailed investigation is presented in the next section, where the micro-scaled aspects of the local loading effect is discussed.

Theoretical deposition considerations

In the reactor chamber, a mixture of gases passes over the wafer from one side to the other side. In the classical boundary layer theory a laminar gas flow over the wafer is assumed. In this situation, due to the frictional force between the gas steam and the stationary susceptor/wafer, a stagnant/low speed boundary layer is established (see Section 4.4.1) [119]. On an oxide-covered wafer, windows to the Si consume the diborane species and cause gas depletion inside the boundary layer over the open Si. Therefore, a gas phase diffusion of the diborane species is established through the width of the stationary boundary layer going from the main gas stream to the silicon and boron surfaces. There they are attracted to the dangling bonds and can be consumed. During the boron deposition, there are two boron source components: vertical and lateral, which contribute incoming reactant molecules.

Vertical component of the source of boron atoms

The boron atoms that contribute to the vertical component come directly from the main gas flow over the wafer. Therefore the vertical component is determined by monitoring the deposition on a bare wafer where no lateral diffusion exists. In this case, only the classical stationary/low speed boundary layer forms over the susceptor/wafer. This part is described in detail in Chapter 3, where the kinetic model for this vertical component is presented.

Lateral component of the source of boron atoms

The lateral component, also called a “local loading effect”, occurs due to: (i) the higher mobility of the boron atoms at higher temperatures, such as 700 °C; and (ii) boron atoms that do not deposit on oxide but will diffuse along the surface of the oxide. Consequently, there is an increase in the probability of boron atoms sticking to the silicon and boron surfaces of the open windows. In this way an increase in the amount of oxide area around a window will result in an increase in the deposited boron layer thickness. An example of the selective boron deposition in an opening to the Si can be seen in the TEM image of Fig. 4.30, and is also shown schematically in Fig. 4.31.

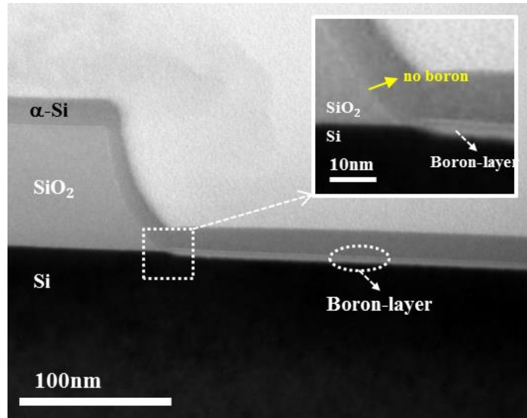


Fig. 4.30: TEM image of a boron layer deposited on an oxide opening to Si during a 6-min exposure to B_2H_6 at 700 °C.

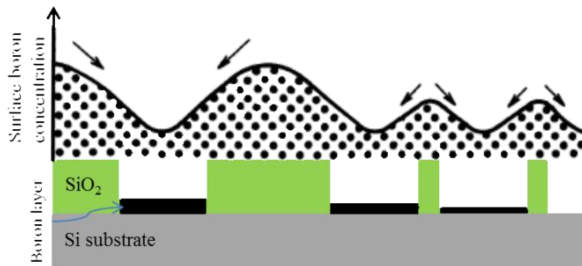


Fig. 4.31: Schematic illustration of how the boron concentration distribution over a patterned wafer is influenced by the width of the Si windows and oxide areas.

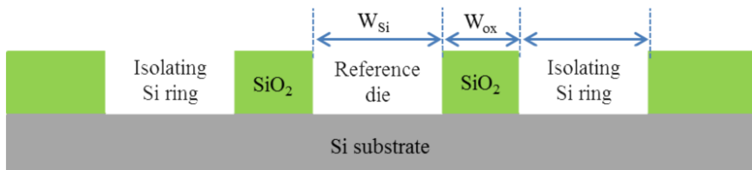


Fig. 4.32: Cross-section of the central open Si die that functions as a reference die for the boron layer thickness measurements and the surrounding rings of oxide and isolating silicon.

The local loading effect of the boron deposition at the macro-scale was studied here by measuring the layer thickness of an open reference die in the center of the wafer with a width of W_{Si}, which is surrounded by a ring of oxide with a width of W_{ox}. As shown in Fig. 4.32, this oxide ring is surrounded by an open Si ring that has the function of isolating the central reference die from other

loading effects than those supplied by this ring. In reference to the discussions in the Section 4.4.1 [119], the diffusion length of boron atoms over the oxide surfaces is in the same width range as the reference die (i.e. within range of a centimeter). Therefore, placing a 10-mm-wide isolated Si ring is enough to guard against loading effects from oxide areas on the rest of the wafer.

Here we define the local oxide ratio (LOR) as the ratio of W_{ox} to W_{Si}, and it is varied by changing the width of the oxide ring, W_{ox}. A measurement for the lateral source of boron atoms is given by the boron thickness of the reference die as a function of W_{ox} relative to the thickness $W_{ox} = 0$. The overall oxide coverage ratio (OCR) is also important for the absolute value of boron thickness, as described in Section 4.4.1 [119]. Thus, to prevent any influence on the loading effect caused by OCR-dependency of the boron deposition, all experiments were done on patterned wafers with the same OCR.

Fig. 4.33 shows the boron deposition rate versus local oxide ratio. In this figure, three regions can be distinguished: LOR < 0.1 (circular symbols); 0.1 < LOR < 1 (square symbols); and LOR > 1 (star-shaped symbols). The dashed line is calculated based on an empirical derivation (Eq. 4.3). Since the reference die and the total oxide coverage ratio were the same in all experiments, the vertical term of the source of boron was the same in all cases and the lateral term only varied with the LOR. This can be seen in Fig. 4.34, where a schematic is given of the reference die, oxide ring, isolating Si ring, vertical and lateral source of boron atoms and corresponding local-chemical boundary layer.

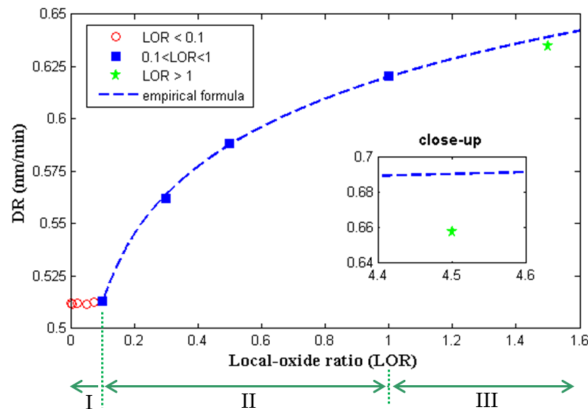


Fig. 4.33: Boron deposition rate DR versus local oxide ratio indicating three regions: LOR < 0.1 (circles); 0.1 < LOR < 1 (squares); and LOR > 1 (stars). The dashed blue line is based on Eq. (4.3). In the inset the situation for LOR ≈ 4.5 is given.

Region I: LOR < 0.1, equivalent to $\frac{W_{ox}}{W_{Si}} < \frac{1}{10}$

In this case the results show that the oxide area is too small to give measurable local loading effects (circular symbols in Fig. 4.33). This is in accordance with the fact that this narrow oxide area is adjacent to a much larger Si window so that it is completely engulfed by the depleted local chemical boundary layer over this window. Therefore, most of the available boron atoms are consumed by the large Si area. This is schematically illustrated in Fig. 4.34a.

Region II: 0.1 < LOR < 1, equivalent to $1 < \frac{W_{ox}}{W_{Si}} < \frac{1}{10}$

In this region the impact of the oxide areas can be seen from the experimental data compiled in Fig. 4.33. As the W_{ox} increases, the deposition rate increases because more boron atoms travel from the oxide to the Si region. The boron sources and the local chemical boundary layer in this situation are shown schematically in Fig. 4.34b, and the following empirical model based on expression (4.3) has been developed to describe this behavior:

$$\mathrm{DR} = 0.0468\ln\left(\frac{W_{\mathrm{ox}}}{W_{\mathrm{Si}}}\right) + 0.6202 \qquad (4.3)$$

The results of this model are included in Fig. 4.33 and indicated by the dashed line, which is seen to fit well with the experimental data. This formula can be used to model the lateral diffusion component of the boron atoms and to develop a comprehensive model to predict the boron deposition rate on any 2D uniform or non-uniformly patterned wafer.

Region III: LOR > 1, equivalent to $\frac{W_{ox}}{W_{Si}} > 1$

In this region the deposition rates rise with an increasing LOR but they no longer follow the model indicated by the dashed line in Fig. 4.33. This becomes more evident for high values of the LOR as shown by the example of LOR ≈ 4.5 in the insert (Fig. 4.33), which is the case where only the reference die at the middle of the wafer is open and the rest is covered by oxide. This shows that the increase in boron layer thickness saturates for such high values of the LOR, i.e., the diffusion across the oxide becomes limited by the diffusion length and not the presence of the Si ring. This is also supported by our previous result given in Section 4.4.1, where the diffusion length of boron atoms on oxide surfaces is

shown to be around 1-1.5 centimeter [119]. This means that the floating boron atoms over the oxide areas can travel for a certain distance and/or time before desorbing from the surface to the gaseous phase. The situations for LOR > 1 and LOR ≈ 4.5 are also shown schematically in Fig. 4.34c and d, respectively.

To summarize, in this section the local loading effect was studied for boron layer depositions on silicon in oxide windows for a wide range of local oxide ratios. It can be concluded that this effect plays an important role on the final boron layer thickness distribution. An empirical model has been employed to describe the local loading effect from oxide areas adjacent to the Si window. This model is found to be a good fit with the data for cases in which the supply of boron is not limited by the diffusion length before desorption of the boron atoms migrating along the oxide surface. This model together with the previously developed kinetic models of the deposition rate as a function of deposition parameters, give a powerful tool for predicting and controlling the boron deposition rate. These tools have been used to enable the reliable deposition of 2-nm-thick boron layers with thickness variations of only a few angstroms on any 2D uniformly or non-uniformly patterned wafer.

b. Micro-scaled investigation of the local loading effect

Here, the local loading effect of the boron deposition is investigated at the micro-scale to understand the uniformity profile of the deposited boron layer inside the oxide opening with micrometer resolution. The diffusion length of boron atoms L_B along the silicon and boron surfaces was extracted experimentally and analytically. L_B presents the average distance that boron atoms can travel along the silicon and boron surfaces before deposition or desorption to the main gas stream occurs. This parameter together with the local loading effect are the main factors causing the concave profile of the deposited layer, as will be discussed in this section. The derived analytical value of L_B was compared with the experimental data, demonstrating very good agreement. The results were then used for developing a comprehensive model to predict the boron deposition rate on any 2D uniformly or non-uniformly patterned wafer such as those used for the advanced device fabrication presented in Chapter 3.

The test structure used for this purpose is shown in Fig. 4.35. This test structure was a combination of the resistance measurement structure shown in Fig. 4.4 and a modified version of the test structure from Fig. 4.32. The modification related to Fig. 4.32 consisted of substituting the reference die with

a resistance measurement structure, W_{Si} = 20 mm. The central die was surrounded by rings of oxide W_{ox} wide and isolating silicon. The local oxide ratio ($LOR = W_{ox}/W_{si}$) was realized by changing the width of the oxide ring, W_{ox}. The resistance measurements were done using an array of 190×190 contacts over the boron layer deposited inside the die, which gave a resolution of 100 µm.

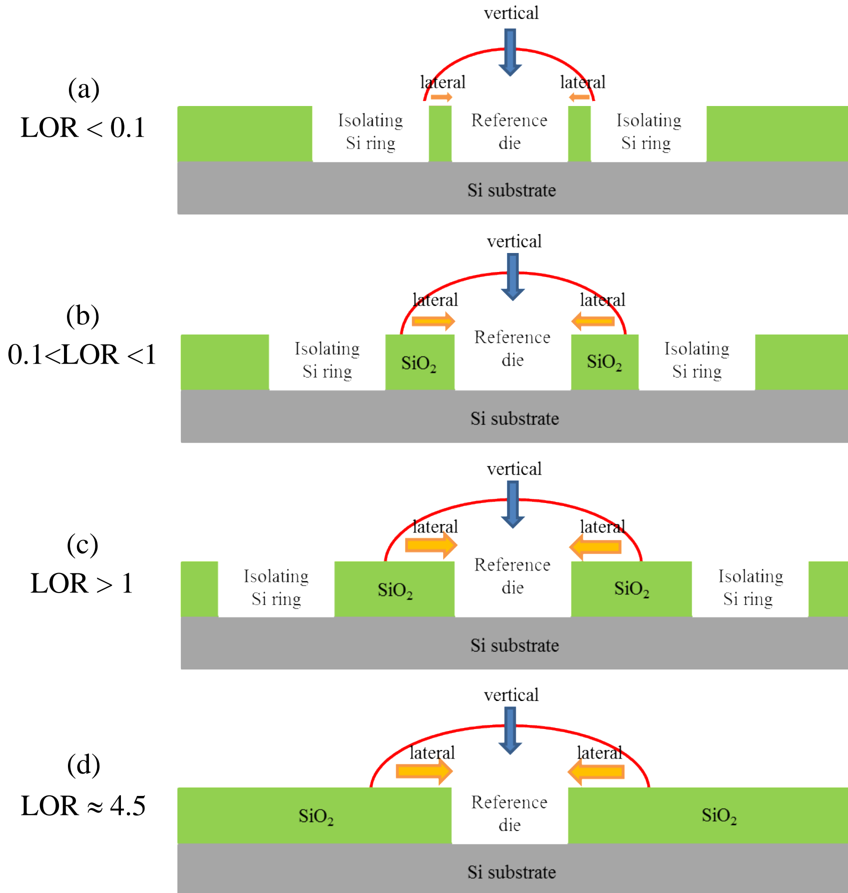


Fig. 4.34: Schematic illustration of the reference die, oxide ring, isolating Si ring, and local chemical boundary layer for (a) region I, $LOR < 0.1$; (b) region II, $0.1 < LOR < 1$; (c) region III, $LOR > 1$; and (d) region III, $LOR \approx 4.5$. The lateral and vertical components of the source of boron atoms are indicated by respectively the lateral and vertical arrows.

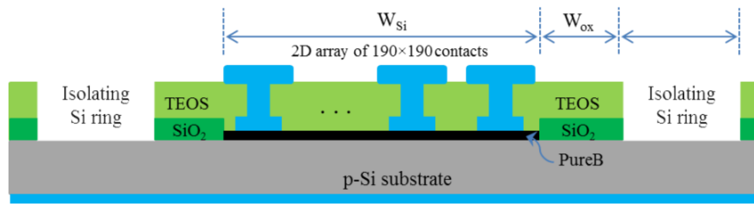


Fig. 4.35: Cross-section of the test structure used for 2D monitoring of the boron layer uniformity. The resistance measurement structure of Fig. 4.4 is located in the center and is surrounded by rings of oxide and isolating silicon.

Thereafter the measured resistance was converted into boron layer thickness by using the expressions given in Fig. 4.10, and were used for monitoring the layer profile. A linear relation between the measured resistance and the boron thickness, regardless of the contact sizes given in this figure, provides a handy tool for thickness measurements, while the fine resolution of the measurements make it very useful for 2D monitoring of the boron layer uniformity inside the opening, related to the local oxide ratio.

The 2D contour plots of the boron layer uniformity are shown in Fig. 4.36 for different LOR values: 0, 0.03, 0.06, 0.1, 0.3, 0.4, 0.5, 0.75, 1, and more than 2. The boron layer was deposited by standard 12-min deposition at 700 °C performed inside Epsilon 2000 CVD reactor as described extensively in Chapter 2. In this figure the impact of the local loading effect on the final deposited layer thickness is clearly visible as it becomes stronger for high values of the LORs (LOR > 0.1). As can be seen for LOR values less than 0.1 there is no significant thickness variation due to this narrow oxide area, while at LOR = 0.1 the overall layer thickness is increased but still no measurable non-uniformity can be seen. However the local loading effect increases considerably with increasing LOR values of more than 0.1, which causes more layer non-uniformity as can be clearly seen in Fig. 4.36. From these graphs, the gradually decreasing layer thickness from the oxide side to the middle of the window can be seen. It can be deduced that the boron thickness is almost symmetrical with respect to the center of the die. It is thinner in the middle, thicker at the edges where it is adjacent to oxide, and it is thickest at the corners of the window where it is adjacent to oxide on two sides. Upon close look at these graphs, it can be found that the diffusion length of boron atoms, L_B, is roughly ~3 mm.

To determine L_B precisely, an analytical calculation was performed. The analytical result was compared with the experimental data and the exact value of L_B was extracted.

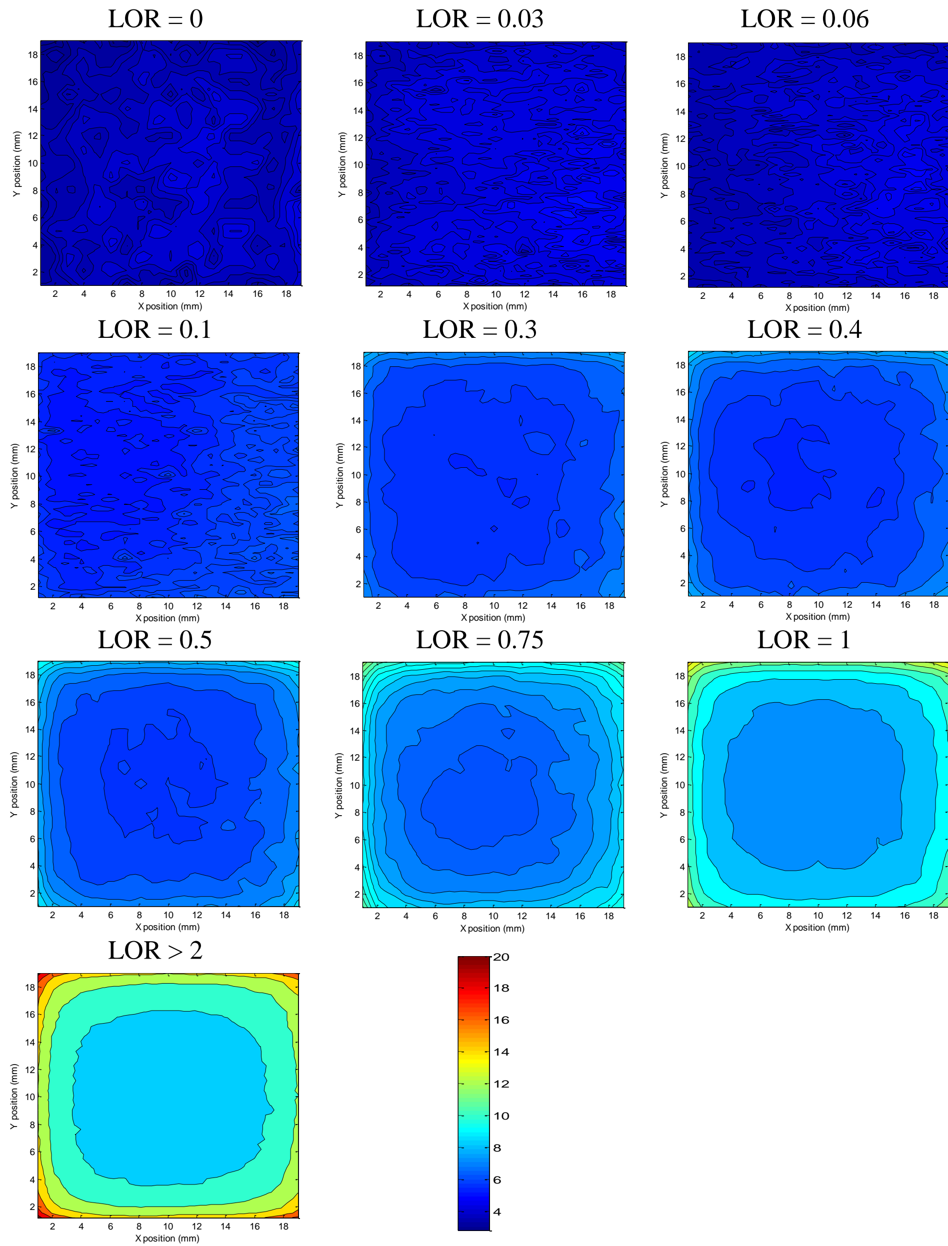


Fig. 4.36: 2D contour plot of the boron layer uniformity of the test structures in Fig. 4.35, for different local oxide ratio (LOR) values. The boron was deposited with a standard 12-min deposition at 700 °C inside an Epsilon 2000 CVD reactor [45].

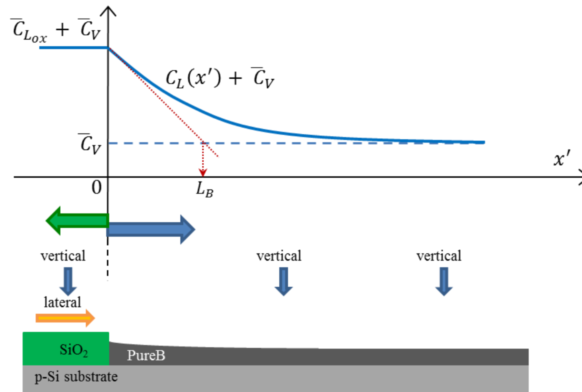


Fig. 4.37: Schematic illustration of boron concentration profiles over Si windows and oxide areas.

Fig. 4.37 shows a schematic illustration of a boron concentration profile over a semi-infinite Si window and adjusted oxide area, when there is no lateral boron reaching the other side of the Si window. In this figure, $\bar{C}_{L_{ox}}$ represents the concentration of boron atoms accumulated over the oxide area at the edge of Si opening ($x' = 0$); $\bar{C}_V$ is the concentration of boron atoms supplied by the vertical component of Eq. (3.22); and $C_L(x')$ is the lateral concentration of boron atoms to be calculated.

The lateral concentration of the boron atoms can be calculated by solving the time-independent diffusion equation in the steady state:

$$L_B{}^2 \frac{\partial^2 C_L}{\partial x'^2} - C_L = 0 \tag{4.4}$$

where L_B is the diffusion length of boron atoms, and $x' = 0$ is located at the edge between the Si opening and the oxide area, as shown in Fig. 4.37. The general solution of Eq. (4.4) is:

$$C_L(x') = k_1 \exp\left(-\frac{x'}{L_B}\right) + k_2 \exp\left(\frac{x'}{L_B}\right) \tag{4.5}$$

where k_1 and k_2 are constants to be determined based on the boundary conditions of Eq. (4.6) as schematically illustrated in Fig. 4.37.

$$\begin{cases} C_L(x' = 0) = \bar{C}_{L_{ox-si}} \\ C_L(x' = \infty) = 0 \end{cases} \tag{4.6}$$

By applying the boundary conditions (4.6) in (4.5) the lateral concentration of the boron atoms can be expressed by:

$$C_L(x') = \bar{C}_{L_{ox}} \exp\left(-\frac{x'}{\mathrm{L_B}}\right) \tag{4.7}$$

As can be seen in Fig. 4.37, the $\bar{C}_{L_{ox}}$ is the boron concentration over the oxide area at $x' = 0$ which is due to accumulation of boron atoms supplied by the main gas flow over this oxide area of width W_{ox}. Therefore it can be expressed as:

$$\bar{C}_{L_{ox}} = \int_{W_{ox}} \bar{C}_V(x_{ox}) \mathrm{d}x_{ox} \tag{4.8}$$

Solving Eq. (4.8) using Eq. (3.22) as a vertical component of concentration of boron atoms gives:

$$\bar{C}_{L_{ox}} = \frac{0.275\zeta h^2 u_0 C_0}{D} \exp\left(\frac{-12.6D}{h^2 u_0}\right) \sinh\left(\frac{2.52D}{h^2 u_0} \mathrm{W_{ox}}\right) \tag{4.9}$$

By following the derivation procedure of Eq. (3.48) in Chapter 3 and using Eqs. (4.7) and (4.9), the boron deposition rate, DR, in this case, can be expressed as:

$$DR^{\mathrm{B}}_{\mathrm{L_B}}(x) = \zeta \beta_1 \beta_2 A_2 P_{\mathrm{BH_3}} \sinh\left(\frac{2.52D}{h^2 u_0} \mathrm{W_{ox}}\right) \exp\left(-\frac{x'}{\mathrm{L_B}}\right) \tag{4.10}$$

where:

$$\beta_1 = \eta\gamma \frac{1}{N_0} \frac{\left(1 - \theta_{\mathrm{H(B)}}\right)}{\left(\mathrm{m_{BH_3}} \mathrm{k}T\right)^{\frac{1}{2}}}$$

$$\beta_2 = \left(\frac{E_{\mathrm{BH_3-on-B}}}{\mathrm{k}T} + 1\right) \exp\left(-\frac{E_{\mathrm{BH_3-on-B}}}{\mathrm{k}T}\right)$$

$$A_2 = 0.105 \times \frac{h^2 u_0}{D} \times \exp\left(\frac{-12.6D}{h^2 u_0}\right)$$

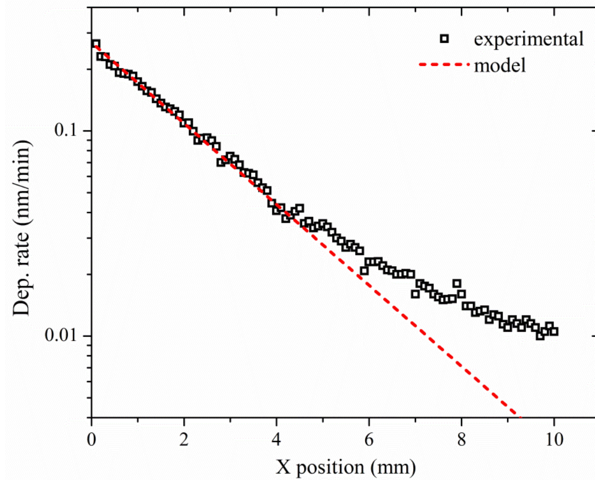


Fig. 4.38: Model and experimental results for the lateral-component-induced boron deposition rate as a function of the axial position inside the Si opening. The model values are calculated based on Eq. (4.10). The lateral component is determined by subtracting the experimental data of LOR = 0 from the experimental data of LOR = 0.3.

Therefore L_B can be extracted by plotting DR in a logarithmic scale versus the position inside the die as shown in Fig. 4.38. To remove the effect of the vertical component, the experimental data of LOR = 0 is subtracted from the experimental data of LOR = 0.3. For LOR = 0 there is no oxide ring, therefore only the vertical component was monitored. As can be seen in Fig. 4.38, the dashed line predicted by the model from Eq. (4.10) follows the experimental data satisfactorily for values of x lower than 4 mm. In this case the calculated value of L_B is 2.2 mm. The deviation of the experimental data from the model values, seen clearly for values of *x* higher than 4 mm, can be explained by the fact that a semi-infinity opening was assumed as the boundary condition of Eq. (4.6) and Fig. 4.37. In reality there is also a loading effect from the oxide area on the other side of the Si opening which causes the deviation.

The value of L_B = 2.2 mm means that the boron atoms can travel laterally along the silicon or boron surfaces for about 2.2 mm before they disappear due to deposition or desorption. Therefore it can be concluded that for $W_{Si} < L_B$, regardless of the LOR value, the local loading effect does not have any significant influence on the non-uniformity of the final layer deposited because the boron atoms can easily pass through the opening. Therefore the layer profile of these openings would be uniform with almost no thickness variations between the side and the middle of the opening. This can be seen in Fig. 4.39

where the 2D contour plot of the normalized boron thickness deposited inside the segments of the design of Fig. 2.12b in Chapter 2 is shown. In this structure the LOR > 0.1 and the concave profile cannot be seen. This figure is extracted from the LEEB [60].

At lower deposition temperatures (< 700 °C), the value of L_B drops dramatically due to a smaller amount available energy to promote the intermediate reactions of [R3.29] to [R3.36] described at Chapter 3. This can be seen in Fig. 4.40 where 2D contour plots of the normalized boron layer uniformity is shown for 500 °C and 400 °C deposited boron layers over the test structure with LOR = 0.5. The higher resolution contour plots of the closed areas with red dots in Fig. 4.40 are shown in Fig. 4.41. These contours explicitly show the non-uniformity of the profile at the edge of the window near the oxide area, where a value less than 1 mm can be extracted for L_B.

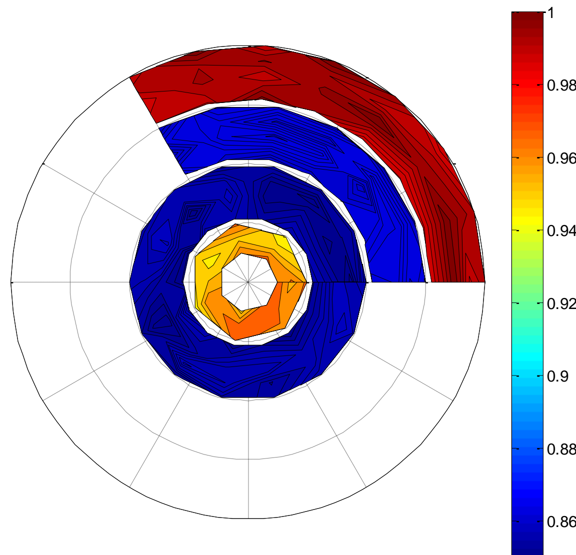


Fig. 4.39: 2D contour plot of the normalized boron thickness deposited inside the segments of the design in Fig. 2.12b.

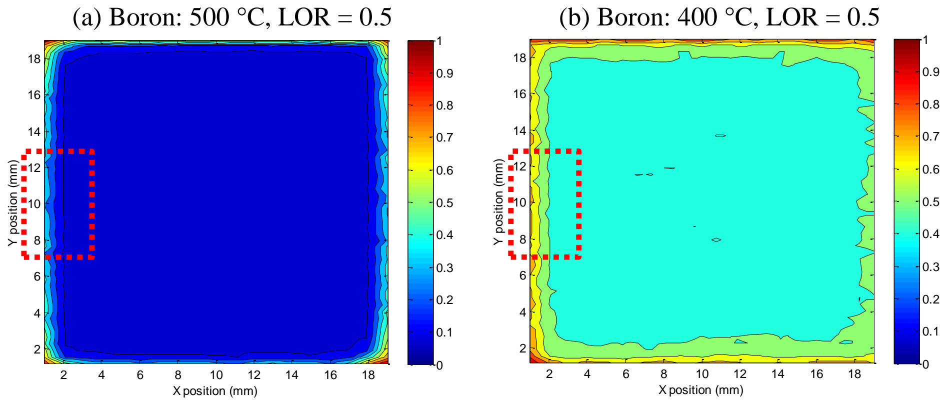


Fig. 4.40: 2D contour plots of the normalized boron layer uniformity for (a) 500 °C and (b) 400 °C deposited boron layers over the test structure with LOR = 0.5. A more detailed view of the areas surrounded with red dots is shown in Fig. 4.41.

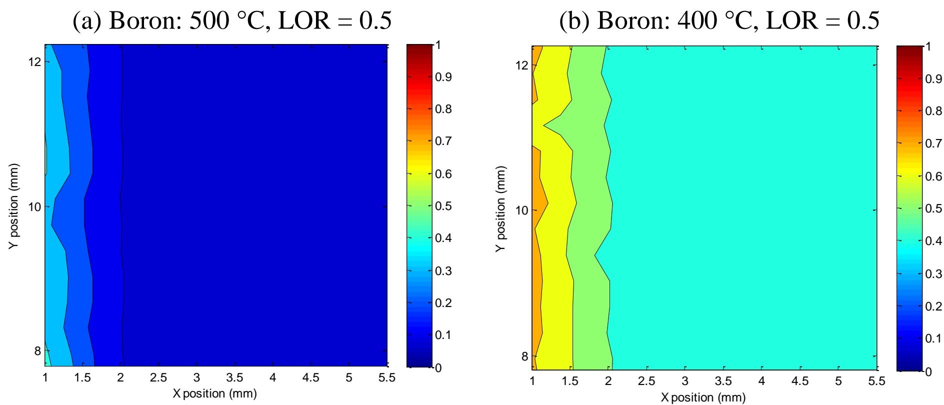


Fig. 4.41: Close-up views of the 2D contour plots given in Fig. 4.40 at the edge of the window near the oxide area.

To summarize, in this section, the local loading effect of the boron deposition was investigated in the temperature range from 700 °C to 400 °C at the micro-scale to understand the uniformity profile of the deposited boron layer inside the opening with micrometer resolution. The investigation showed that for LOR values less than 0.1 there is no significant thickness variation due to the narrow oxide area, while at LOR = 0.1 the overall layer thickness is increased but still no measurable non-uniformity can be seen. However, the local loading effect rises considerably with increasing LOR values of more than 0.1.

Valuable information about the diffusion length of the boron atoms L_B along the silicon and boron surfaces was extracted in this temperature range experimentally and analytically. L_B = 2.2 mm was calculated for boron deposition at 700 °C, while it was reduced to less than 1 mm for deposition at lower temperature (< 500 °C). It is shown that for the Si openings with $W_{Si} < L_B$, regardless of the LOR value, the local loading effect does not result in a significant non-uniformity of the final deposited layer, because the boron atoms can easily pass the opening.

Moreover, the results of this section are useful for developing a comprehensive model to predict the boron deposition rate and the profile on any 2D uniformly or non-uniformly patterned wafer such as those used for advanced device fabrication as presented previously in Chapter 3.

4.5 Recommendations for depositing a uniform 2-nm-thick boron layer

From the discussion thus far, it can be concluded that an improvement in the PureB technology is highly required, especially regarding the optical performance of these devices, i.e. spatial non-uniformity of the response to low energy beams.

To solve these problems, in this chapter, the loading effect and the pattern dependency of the HT boron deposition are investigated as a source of layer non-uniformity. In this section, methods will be proposed, which by: (i) slight modification of the process flow, (ii) adjustment of some recipe parameters, and (iii) changing the wafer layout or the die design (if necessary), give a way to control and minimize the negative effects during the deposition. The advantage of these methods is that most of them are applicable to the existing layouts without need to change the design.

The influence of the process and design parameters on the deposition rate and/or loading effects of the boron layers is a complicated issue since the parameters can be interdependent. Ideally, a deposition should be totally independent of the size/geometry of the openings and the surrounding oxide areas. However, in reality, many effects play a role due to the non-uniform gas consumption over different window sizes, and different kinds of boron atom sources, which create the global/local loading effects. Actually, the exact origin

of the non-uniformities is a complex combination of chemical, kinetic, and thermal factors.

The first recommendation originates from the results presented in Section 4.4.1 where the pattern dependency of the boron deposition was studied. It has been demonstrated that the deposition rate of boron can vary over the wafer depending on the Si opening size and OCR (oxide coverage ratio) of the mask design. The higher the OCR, the higher the deposition rate is and the deposition rate also increases as the dimensions of the windows to the Si decrease. The results presented in the aforementioned section show a reduction in the pattern dependency with decreasing diborane partial pressure and the main gas flow, which are the two main process parameters. Moreover, no significant improvement in the pattern dependency was observed with a decrease in the total pressure from ATM to 60 torr (see Fig. 4.21). Thus, it was found that 70% P_1 (or 70% F_1), where P_1 (F_1) is the maximum diborane partial pressure (main gas flow), makes it possible to control and minimize the pattern dependency and the loading effects considerably.

The second recommendation is to modify the die layout (if necessary) in order to satisfy conditions of LOR < 0.1 or $W_{Si} < L_B$ regardless of the LOR value given earlier in Section 4.4.2, where the local loading effect of the boron deposition was investigated. In both cases it was shown that there is no measurable local loading effect and no significant layer non-uniformity as can be seen in Fig. 4.36 and Fig. 4.39.

Besides this, the wafer layout also has an impact on the final boron layer uniformity over the wafer, which is the third recommendation: to control the loading effects. As discussed already in Section 4.4.1, using the CDE layout[1] instead of the RG layout[2] guarantees that all the dies have the same loading effect and, consequently, that the same boron deposition rate is obtained. Therefore by just applying this method, thickness variations of the layer were reduced from more than 1 nm to only 4 angstroms.

The above-discussed recommendations to reduce the loading effect are based on reducing the amount of additional boron atoms coming from the oxide areas (lateral source of boron atoms) by adjusting some of the process parameters such as diborane partial pressure and the main gas flow or

[1] Continuous Dies to the Edge wafer layout (Fig. 4.22c)
[2] Regular wafer layout (Fig. 4.22a)

modifying the wafer/die layout parameters. However, there is another method to reduce the surface diffusion length of boron atoms on the oxide areas. This may be achieved by introducing a polycrystalline Si seed layer to the oxide surfaces prior to the boron deposition. For example, C. Menon *et al.* also used this method for the growth of SiGe layers [127].

In fact, in this way, when depositing the seed layer, the surface diffusion length decreases, since the species adsorbed on the polycrystalline Si layer are preferably incorporated into the polycrystalline site instead of being diffused to the single crystalline opening. On the other hand, this deposited boron layer over the oxide areas can induce positive charges in the structure when they are located beneath the metal contacts/pads. This means that this method can have an impact on the performance of the PureB diode.

Altogether, it is possible to optimize the conventional HT PureB technology by only using one or more of the aforementioned methods to provide uniform and reliable deposition of 2-nm-thick HT boron layers with thickness variations of only a few angstroms. The results of this chapter will be employed to fabricate high performance PureB detectors particularly for low penetration photon/electron beam detection, as presented in Chapter 6.

4.6 Summary

In this chapter, to solve the problems addressed in Chapter 2, the pattern dependency and the loading effect of the HT boron deposition is investigated as a source of non-uniformity of the boron layer. Since these investigations need a thickness monitoring technique, the end-of-line resistance measurement is introduced as a nondestructive and accurate means of monitoring the boron layer uniformity with fine resolution.

It has been demonstrated that the deposition rate of boron can vary over the wafer depending on the Si opening size and OCR[1] of the mask design as well as the wafer layout. The deposition rate increases with a higher OCR and smaller window size to Si. This has been explained in terms of the gas depletion of the diborane species in the stationary and/or local boundary layer. The results show a reduction in the pattern dependency with a decrease in both the diborane

[1] Oxide coverage ratio

partial pressure and main gas flow. Moreover, no significant improvement in the pattern dependency was observed when decreasing the total pressure from ATM to 60 torr. Thus conditions were found, together with using a CDE layout[1] instead of a RG layout[2], which make it possible to minimize the pattern dependency and the loading effects.

The local loading effect is found to play an important role in the final boron layer thickness distribution. This effect was investigated at the macro- and the micro-scales. At the macro-sale the investigation was limited to study of the influence of the LOR[3] on the final boron layer thickness at the middle of the millimeter-large Si opening window, while at the micro-scale the target was to investigate the uniformity profile of the deposited boron layer inside the opening with micrometer resolution. An empirical and analytical model was developed to describe this effect at the macro- and micro-scales. As a result, valuable information about the diffusion length of boron atoms along the oxide and Si/B surfaces at deposition temperatures from 700 °C to 400 °C was extracted. The diffusion length of the boron atoms on the oxide surface is found to be in relation to the Si opening width, here, in the order of centimeters, which means that the loading effect in micron-sized windows will not lead to thicker layers seen in the larger windows. The diffusion length of boron atoms along the Si/B surfaces was calculated both experimentally and analytically to be about 2.2 mm and less than 1 mm for boron deposition at 700 °C and at a lower temperature (< 500 °C), respectively.

Finally, methods were proposed on the basis of the knowledge obtained in this thesis, to control and minimize the pattern dependency and the loading effect during deposition by slightly modifying the process flow, adjusting some recipe parameters and changing wafer layouts or die design (if necessary). This was accomplished to such a degree that the 2-nm-thick boron layers used in present-day applications can be deposited uniformly with variations in thickness of only a few angstroms. The results of this chapter were employed to fabricate high performance PureB detectors particularly for low penetration photon/electron beam detection, as presented in Chapter 6.

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[1] Continuous Dies to the Edge wafer layout (Fig. 4.22c)
[2] Regular wafer layout (Fig. 4.22a)
[3] Local oxide ratio (W_{ox}/W_{Si})

Chapter 5

Development of a novel low temperature (400 °C) boron deposition

Conventional PureB technology is employed to fabricate state-of-the-art PureB UV photodiodes. However, due to the relatively high temperature of boron deposition (500 °C – 700 °C), it is hard to fully integrate this technology in a standard IC/CMOS process flow.

In this chapter, a novel technology for low temperature (LT, 400 °C) boron deposition is developed providing a uniform, smooth, closed LT boron layer. This technology is successfully employed to create near-ideal LT PureB diodes with low, deep junction-like saturation currents. The low temperature deposition at 400 °C, gives a chance to fully integrate the LT PureB photodiodes together with electronic interface circuits and other sensors on a single chip. In this way, smart sensor systems or even CCD or CMOS UV imagers can be realized.

In the chapter, the temperature dependency of the kinetics of boron deposition on patterned Si/SiO_2 surfaces in the temperature range from 700 °C to 400 °C is discussed. Also, selectivity issues that arise when the boron deposition temperature is reduced from 700 °C down to 400 °C are analyzed. Some provisions are recommended to minimize the undesirable boron deposition on oxide.

The technology presented in this chapter was employed to fabricate high stability, high performance DUV/VUV/low energy electron Si photodiodes, as will be presented in Chapter 6.

5.1 Temperature dependency of boron deposition

To develop a new technology for low temperature (LT, 400 °C) boron deposition on silicon, the temperature dependency of the deposition has to be studied to understand the kinetics of boron deposition on patterned Si/SiO_2 surfaces. This study will be described in this section.

The kinetics of boron CVD deposition was investigated in Chapter 3, as well as in [116, 130]. From Eq. (3.48) it becomes clear that the deposition rate has a significant dependence on the deposition temperature as well as on the reaction leading to boron deposition [R3.23] through the intermediate reactions, ([R3.29] to [R3.36]). Therefore any change in the deposition temperature can affect the reactions and consequently can change the deposition rate and also the quality of the layer. In this section, the temperature dependency of the boron deposition will be investigated in the temperature range of 400 ºC to 700 ºC. Then LT boron deposition and the issues associated with the deposition in this temperature range will be discussed.

Under ideal conditions for HT deposition, 700 °C and 0.2% B_2H_6 concentration as described in Chapter 2, there is enough energy to facilitate reactions [R3.29] to [R3.36], which release hydrogen from the Si/B surface sites as H_2 and leave Si/B sites free for deposition [130]. Therefore, the start of the deposition will be very fast, i.e., after a few seconds of exposing the surface to diborane gas under these conditions, a monolayer of boron appears and covers the surface [17]. Fig. 5.1 shows a schematic of the deposition mechanisms for the first few monolayers of boron layers when a Si surface is exposed to B_2H_6.

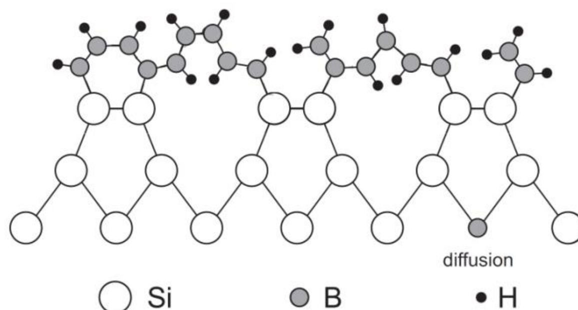

Fig. 5.1: Schematic of the first few monolayers of boron deposition when a Si surface is exposed to B_2H_6, under ideal conditions for HT deposition: 700 °C and 0.2% B_2H_6 concentration.

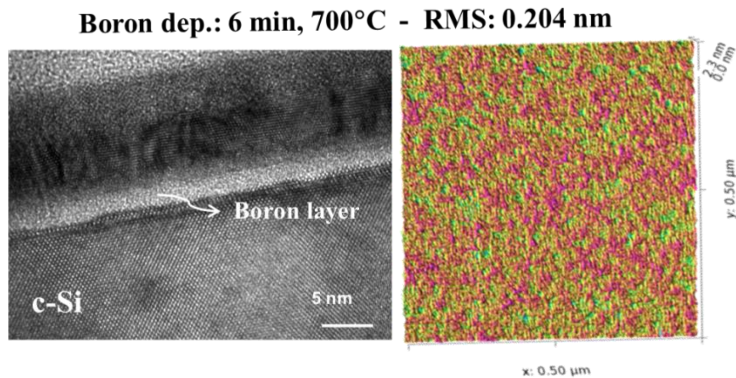

Fig. 5.2: HRTEM image (left) and atomic-force microscopy (AFM) measurement (right) of a 6-min HT deposited boron layer surface. The AFM image was taken in a (500×500) nm^2 square scanning area. This HT layer is smooth and uniform at a thickness of about 2 nm with a root-mean-square (rms) roughness value of 0.204 nm.

Then the aforementioned temperature-related reactions [R3.23] to [R3.36] progress in the forward direction leading to adsorption of boron atoms, either deposited and/or suspended, as well as migration of the boron atoms along the surface. This leads to a uniform, smooth, closed boron layer [130]. The promotion of the intermediate reactions also ensures very smooth layers with a roughness that can be around 2 angstroms as measured either by HRTEM imaging or atomic-force microscopy (AFM). This is illustrated by the analysis results shown in Fig. 5.2 for a 2-nm-thick layer.

Experiments show that by lowering the boron deposition temperature from 700 °C to 400 °C the deposition rate drops considerably from 0.4 nm/min to less than 0.01 nm/min for deposition in H_2, with a laminar gas flow of 20 slm. In this case even after a long time deposition at 400 °C there is almost no measurable layer formed and, if such a layer is deposited, it is not closed enough to make it suitable for device applications. As a result, the performance of such devices is not comparable to the ones made by conventional 700 °C boron deposition.

Several factors are responsible for this negative effect. First, by lowering the deposition temperature T for example in Eq. (3.48), the deposition rate, DR, will drop significantly. Second, at this low deposition temperature the gas phase diffusion length is very small. Lastly, the intermediate reactions that promote adsorption at 700 °C are not effective anymore. For example, due to the very

low available energy, reactions [R3.29] and [R3.30] are not promoted in the forward direction. In addition, the presence of H_2 in the reactor as a carrier gas can suppress the reaction because most of the surface sites are occupied by hydrogen that will not readily desorb at 400 °C. Consequently, the first monolayer coverage takes more time at this temperature than 700 °C. This is illustrated schematically in Fig. 5.3.

On the other hand, by switching to N_2 as a carrier gas, a much higher deposition rate of 0.25 nm/min is achieved due to the promotion of reactions [R3.29] and [R3.30] in the forward direction [130]. Thus, only lowering the temperature in the conventional 700 °C PureB recipe to 400 °C does not guarantee a promising layer deposition. Therefore for boron deposition at 400 °C a new recipe needed to be developed, which will be discussed in detail in the next section.

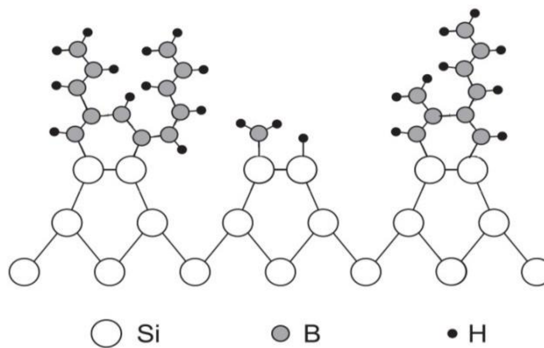

Fig. 5.3: Schematic of the deposition of the first few monolayers of boron layers for a LT deposition when a Si surface is exposed to B_2H_6.

Table 5.1: The thickness and roughness of deposited layers extracted from ellipsometry measurements, as a function of deposition temperature and time.

	Dep. temp*				
Pure Boron	700°C	600°C	500°C	450°C	400°C
Dep. time (min)	10	10	16	20	60
Thickness (nm)	3.74	3.21	3.14	1.77	1.62
Roughness (nm)	0.38	0.81	1.23	2.64	3.73

* The recipes are only different in time and temperature. Their structure is the same in all cases, even for 400 °C and the depositions were done only in H_2 ambient.

To complete the discussion about the temperature dependency of boron deposition, deposition at intermediate temperatures such as 600 °C, 500 °C and 450 °C were also investigated. Lowering the temperature lowers the gas phase diffusion coefficient and reduces the deposition rate based on Eq. (3.48). In addition, the lower temperatures mean lesser promotion of intermediate reactions [R3.29] to [R3.36] in their forward direction, so there is a higher H-coverage of the surface. Moreover, the gas phase diffusion lengths of boron atoms on both Si and oxide surfaces also decrease. Altogether, this causes the deposited layer to become increasingly rough when going from 600 °C to 500 °C and 450 °C. The properties of layers deposited on bare Si at temperatures between 700 °C to 400 °C are given in Table 5.1. The increase in roughness of the layers as the deposition temperature decreases is clearly seen.

For deposition at the lower temperatures, 450 °C and 400 °C, the ellipsometry measurement gave a roughness that is much larger than the layer average thickness, which cannot be relevant. These parameters become very dependent on the exact deposition conditions because of the absence of other intermediate reactions ([R3.29] to [R3.36]) and the fact that the gas phase diffusion lengths of boron atoms on both Si and oxide surfaces decrease.

The HRTEM image and AFM measurement of the LT deposited boron layer at 400 °C with the newly developed recipe discussed in Section 5.2 is shown in Fig. 5.4. A layer roughness of around 6 to 8 angstroms was found for a 5-nm-thick layer. In an earlier study reported in [130] as well as in Chapter 3, a smaller roughness of 3 to 4 angstroms is measured for LT deposition on a Si surface already covered with a HT deposition of boron. Therefore, it can be concluded that the inhibited removal of H from the Si surface at low temperatures plays an important role in increasing the roughness.

Next, we will discuss the process and recipe requirements needed to make the boron deposition possible at 400 °C.

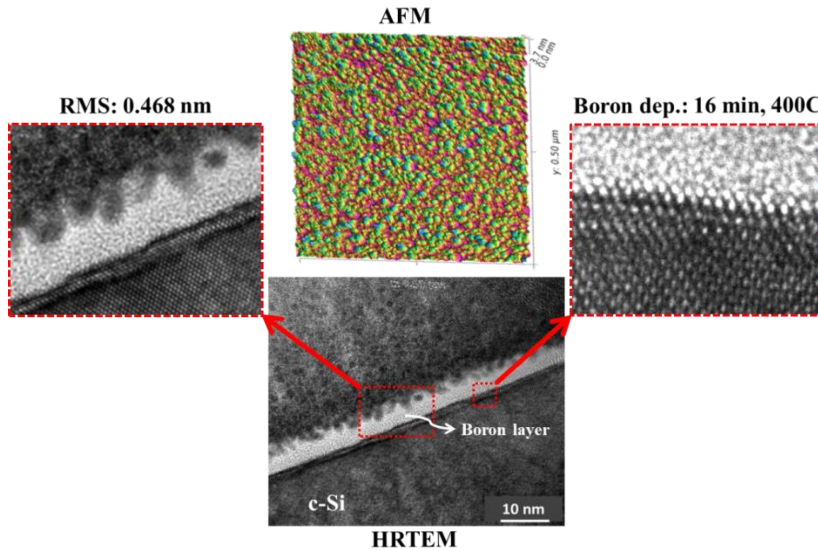

Fig. 5.4: HRTEM image (bottom) and AFM measurement (top) of a boron layer deposited at 400 °C for 16 min. The LT layer is 5-nm thick and a surface rms roughness value around 4-6 angstroms was extracted in both cases. The pictures on the left and right show a close-up of the LT boron layer surface roughness and the interface with the Si substrate, respectively.

5.2 Low temperature boron deposition at 400 °C

As already discussed in the previous section, the presence of hydrogen gas can suppress the forward direction of reactions [R3.29] and [R3.30], which are necessary to release the hydrogen from the surface and decrease the H surface coverage, as well as suppress reactions [R3.25] to [R3.33]. Therefore the deposition rate is limited by reactions [R3.29] and [R3.30]. The release of hydrogen facilitates migration of deposited boron atoms along a boron/silicon surfaces via the intermediate reactions [R3.34] to [R3.36] leading to a uniform, smooth, closed boron layer deposition. Whereas in the case of deposition in N_2, there is no hydrogen for suppressing the forward direction of the reactions [R3.25] and [R3.33], which stimulates hydrogen atoms to be released more easily from the surface and reduces the H surface coverage, leading to a higher deposition rate. However, due to the lower mobility of boron atoms in this environment, an increase in the boron layer roughness was also expected. Therefore for boron deposition at 400 °C it was necessary to start the deposition

in nitrogen to facilitate the first monolayer deposition, and then switch to a hydrogen environment to make the surface smoother and maintain the boron coverage over the entire silicon opening. This procedure can be repeated a few times as shown schematically in Fig. 5.5 to achieve a uniform, smooth and closed boron layer. Lowering the chamber pressure can also facilitate the hydrogen release from the surface and decrease the H surface coverage. Thus, deposition at a lower ambient pressure is preferable.

The HRTEM image of a LT boron layer deposited at 400 °C and a chamber pressure of 95 torr with the newly developed recipes of four and six sequences of carrier gas switching (see Fig. 5.5), are shown in Fig. 5.6. As can be seen in these images, the more switching sequences provided, the smoother the layer is.

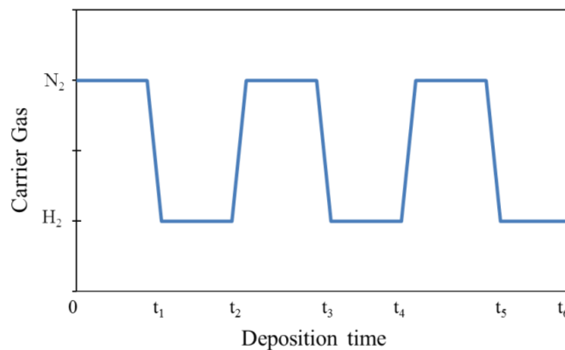

Fig. 5.5: Schematic illustration of sequences of the 400 °C PureB recipe.

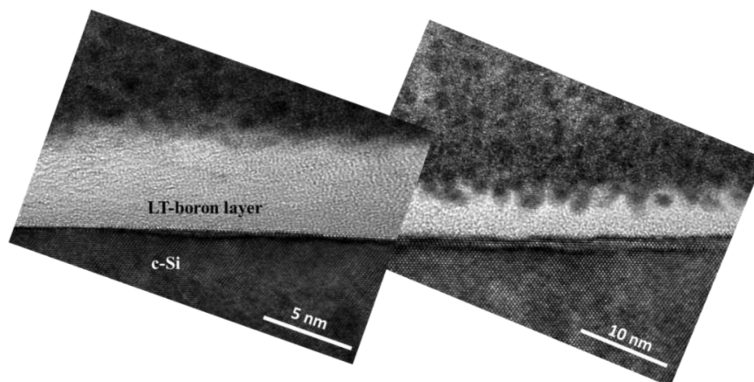

Fig. 5.6: HRTEM image of deposited LT boron layer after (left) the six, (right) and four recipe sequences. The deposition chamber pressure is 95 torr.

Besides a new recipe, some additional treatments are also needed prior to the wafers being loaded into the reactor. The first treatment is a standard *ex-situ* cleaning procedure prior to the deposition as described in Appendix A. For 400 °C deposition there was no in-situ baking step such as the one done for 700 °C deposition (see Chapter 2). Thus the wafers were directly loaded into the pre-prepared reactor at the 400 °C deposition temperature. The lack of the *in-situ* bake made the HF dip with Marangoni drying a very crucial step and the wafers had to be loaded immediately into the N_2-purged load lock of the reactor to prevent any native oxide formation.

5.3 XPS examination of the surface oxide amounts

An XPS examination was done to determine the amount of undesired surface oxide for both HT and LT PureB layers deposited at 700 °C and 400 °C, respectively. These measurements were done at the Industrial Focus Group XUV Optics, University of Twente, the Netherlands. All the measurements were done on the (1×1) cm^2 PureB photodetectors. The results are shown in the following section.

Fig. 5.7 and Fig. 5.8 show Si and B “bulk” signals, respectively. These signals, which represent the electrons that escape perpendicularly from the surface, generally come from deep inside the sample measured at detector angle of 25° for both HT and LT PureB layers. In Fig. 5.9 and Fig. 5.10 the Si and B “surface” signals measured at detector angle of 65° are shown. These signals indicate electrons that escape almost parallel to the surface which generally do not come from deep inside the sample, and which depend on the attenuation length. A clear reduction of the oxide peak can be seen in these figures which represents a lower amount of oxide at the surface as well as interface for the samples with LT boron layers.

It needs to be noted that the oxide thickness under the boron layer cannot be determined by absolute peak intensity only. This, for example, reduces when there is more boron on top (i.e. thicker boron layer). Therefore, the measurements were instead done at different detector angles from 25° to 65°.

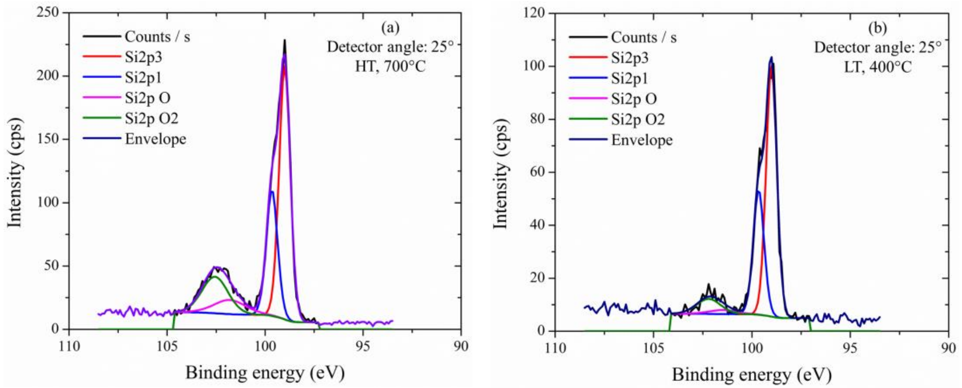

Fig. 5.7: XPS results for the Si "bulk" signal measured at a detector angel of 25° for (a) HT- and (b) LT-PureB layers. The measurements were done on the (1×1) cm^2 PureB photodetectors.

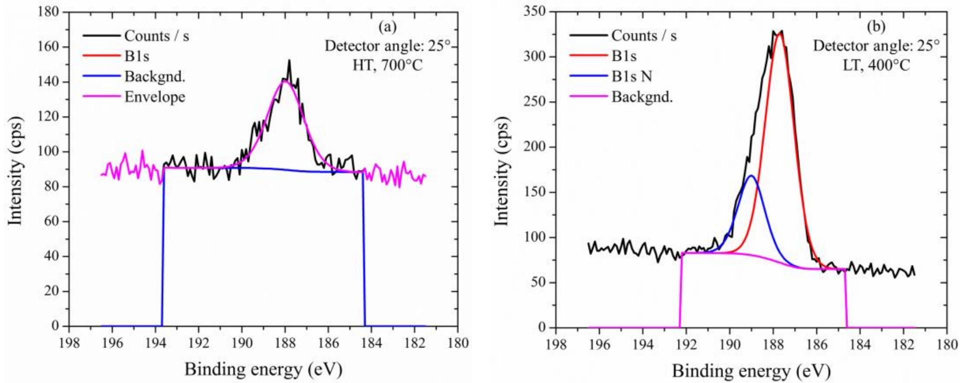

Fig. 5.8: XPS results for the B "bulk" signal measured at a detector angel of 65° for (a) HT- and (b) LT-PureB layers.

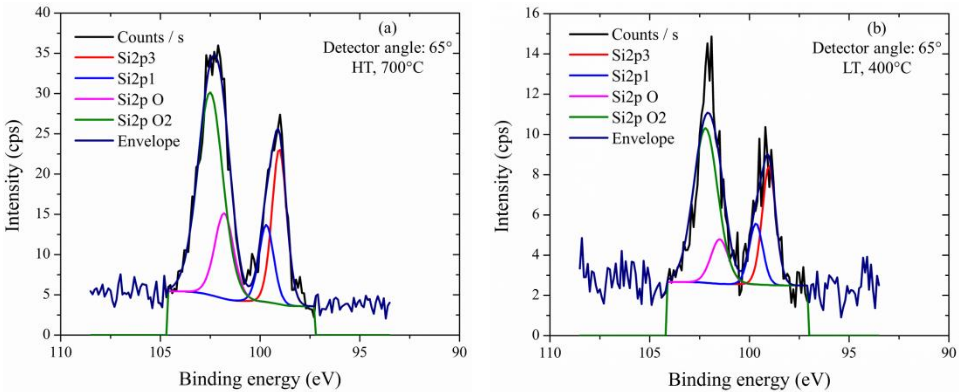

Fig. 5.9: XPS results for Si "surface" signal measured at detector angel of 65° for (a) HT- and (b) LT-PureB layers.

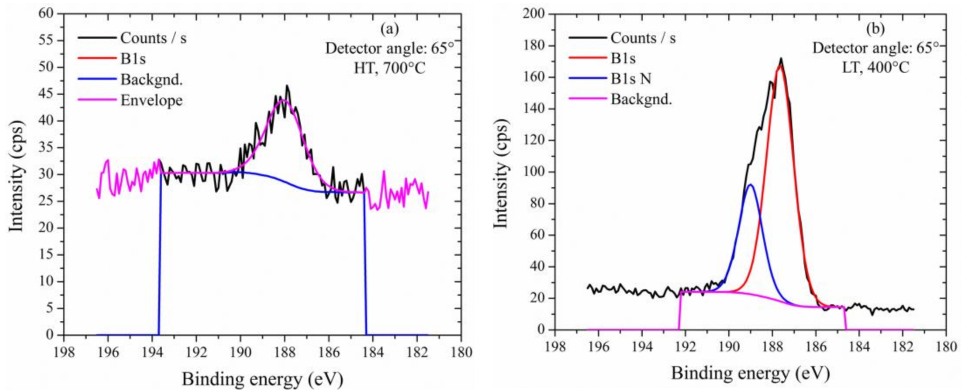

Fig. 5.10: XPS results for the B "surface" signal measured at a detector angel of 65° for (a) HT- and (b) LT-PureB layers. The measurements were done on the (1×1) cm^2 PureB photodetectors.

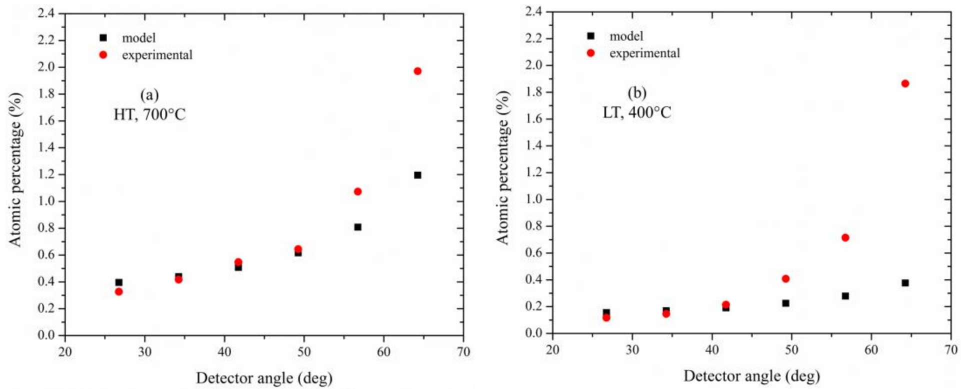

Fig. 5.11: The atomic percentage of the surface oxide as a function of the angle for (a) HT- and (b) LT-PureB layers. The measurements were done on the (1×1) cm^2 PureB photodetectors.

Table 5.2: XPS examination of the HT- and LT- boron layers.

Boron layer	**XPS**		**TEM**
	B Thickness	*Oxide Content*	*B Thickness*
LT, 400°C	3.7 nm	10%	4.5nm
HT, 700°C	1.6 nm	30%	2.5 nm

The atomic percentage of the surface oxide for both the model and experimental results as a function of the detector angle for the HT and the LT PureB samples are shown in Fig. 5.11. The atomic percentage of the surface oxide was calculated as the intensity ratio of the oxide to the elemental Si. As can be seen in this figure, the atomic percentage of the surface oxide as a function of the detector angle is fitted with an oxide thickness model for the angles below 50° and shows a 30% reduction in the amount of undesired oxide for the LT boron layers compared to the HT boron layers, as also presented in Table 5.2.

A larger discrepancy can be seen in Fig. 5.11 between the experimental and fitted data for angles wider than 50°. With these angles the signals become very weak because the Si and oxide are buried under the boron layer. Depending on the thickness of the boron layer, they can be far away from surface as can be seen by the increased difference between the LT PureB sample with a 4.5-nm boron layer and the HT PureB one with a 2.5-nm boron layer at 65°.

5.4 Issues with lowering the deposition temperature of boron layers

In this section, selectivity issues that arise when the boron deposition temperature is reduced from 700 °C to 400 °C are investigated. Some precautions are discussed to minimize the parasitic boron deposition on oxide surfaces. By taking these precautions into account, the LT boron deposition at 400 °C was successfully performed to create near-ideal diodes with low, deep junction-like saturation currents. The fabricated LT PureB photodiodes are found to be quite stable under illumination with UV light as well as low energy electrons as presented in [131] and will be discussed in Chapter 6.

5.4.1 Selectivity of the deposition to Si/SiO_2 surfaces

Considering the aforementioned temperature-related reactions [R3.23] to [R3.28] together with the fact that the gas phase diffusion length of boron atoms over oxide surfaces is in the centimeter range at this temperature [119, 129], at HT (700 °C) the boron atoms can move around easily over the oxide regions. This prevents an accumulation of the boron atoms that would give a localized

increase in the concentration over these surfaces. The higher the concentration levels, the higher the probability is of boron atoms depositing on oxide-free sites and/or defects. In the Si windows there is also a high mobility of boron atoms along the surface at this temperature with diffusion lengths in the centimeter range because the forward direction of reactions [R3.29] to [R3.36] is facilitated. All in all, these reaction mechanisms give the advantage that the deposited layers at 700 °C are completely selective to the Si surfaces regardless of the Si window size [17]. This can be seen in the HRTEM image of Fig. 5.12, where no boron deposits are observed on the flat or beveled SiO_2 surfaces.

During a LT (400 °C) deposition all the boron atoms that arrive over the oxide covered surfaces are retained there and become very limited in terms of movement. This means that the probability of desorption from the oxide-free sites and/or defects becomes much lower than in the 700 °C case and, in fact, a significant amount of boron was observed to be deposited on the oxide. This is also promoted by the longer deposition time needed to achieve a reliably closed layer because of the low deposition rate and extra thickness needed to compensate for the large amount of roughness, as can be seen in Fig. 5.3 and Fig. 5.4.

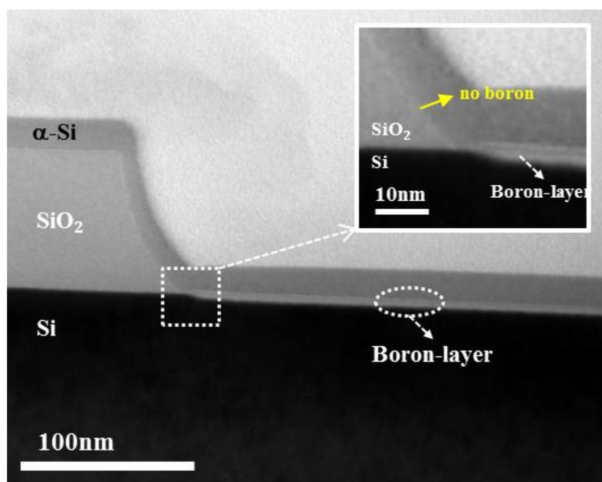

Fig. 5.12: TEM image of a HT boron layer deposited in a window with an area of (40×40) μm^2, which is small compared to the diffusion lengths of B over the Si or SiO_2; after a 6-min B_2H_6 exposure at 700 °C [17].

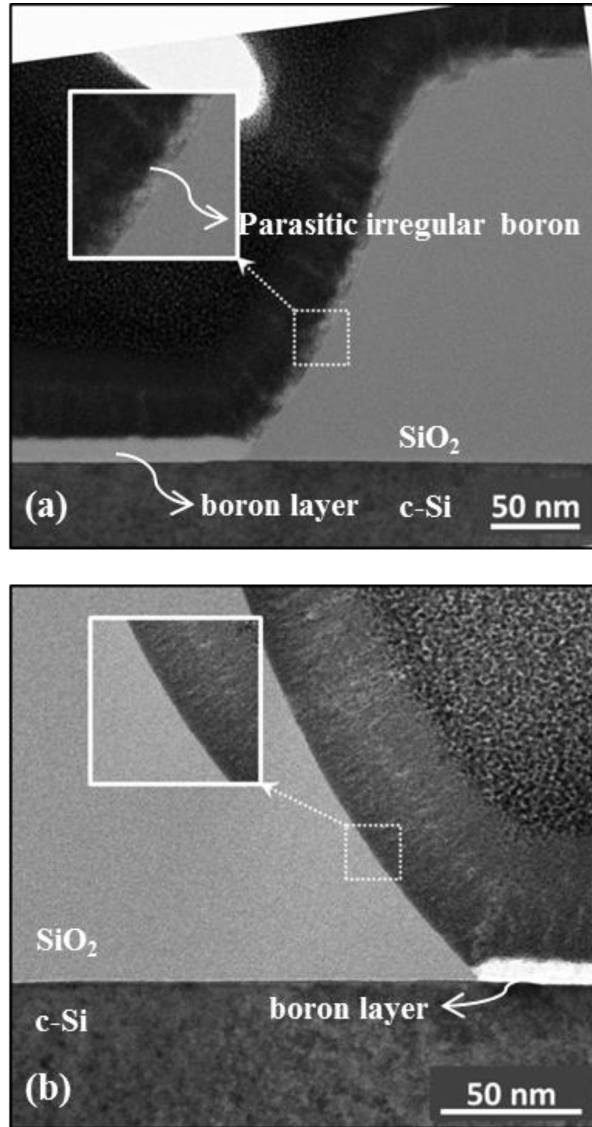

Fig. 5.13: HRTEM images of flat/beveled oxide surfaces of (a) a (40×40) μm^2 small Si window, (b) a (9×9) mm^2 large Si window for a 16-min LT deposition of boron [132].

Moreover, there is also less consumption of boron atoms during this long exposure time than that of comparable conditions at higher temperatures. Therefore, the boron concentration over the oxide surfaces can increase very significantly, which gives a much higher chance of deposition at the possible nucleation sites formed by oxide-free sites and/or defects. The first attachment of boron atoms to these sites is a process that is difficult to initiate but nevertheless possible with such high concentrations of boron atoms. The following boron atoms are much more easily attached by reaction with the initially deposited boron atoms, which results in a very rough, loosely connected layer of boron on the oxide. Examination of the HRTEM images in Fig. 5.13 reveals that such a layer appears in situations where high boron concentrations over the oxide are expected. However this is the case for micron-sized small windows surrounded by a significant amount of oxide, where the perimeter oxide wall that has been etched to form the window will readily be covered with an irregular boron deposition layer (Fig. 5.13a). This will mainly happen for depositions performed at temperatures as low as 400 °C or 450 °C. For the same deposition conditions millimeter-large windows where the local oxide to Si ratio (LOR) is small, may be found to be free of this parasitic perimeter deposition (Fig. 5.13b). This is because the desired deposition on the large Si surface decreases the boron concentration above the oxide of the perimeter.

These parasitic boron depositions on the flat/beveled oxide are unwanted and can cause problems in the subsequent processing steps. For example, the adhesion of plasma-enhanced chemical vapor deposition (PECVD) layers of TEOS-SiO_2 was seen to degrade. This is illustrated in the SEM images of Fig. 5.14. Similar adhesion issues were also witnessed in the case of physical vapor deposited (PVD) Al deposition on such surfaces. Boron depositions at 500 °C can be performed without any parasitic deposition over most oxide surfaces even at micron-sized windows. However, still for some oxide qualities this kind of unwanted parasitic deposition was observed. An example is given in Fig. 5.15b and Fig. 5.15c, where two different dies with the same layout are shown with and without adhesion issues for subsequent PECVD TEOS and PVD Al layer depositions.

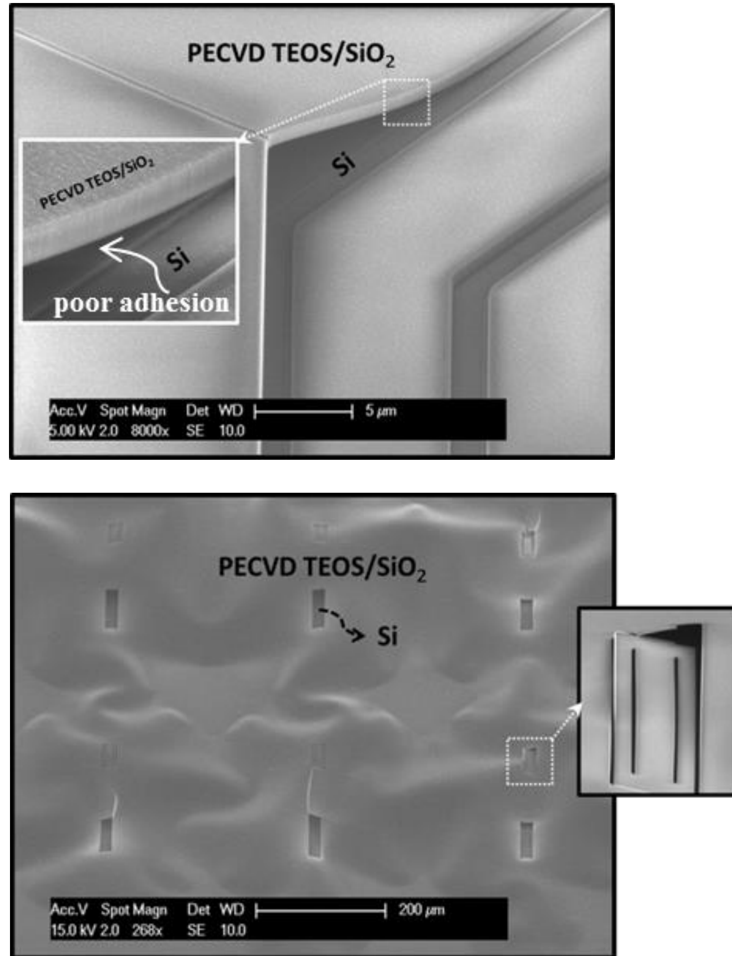

Fig. 5.14: Examples of poor adhesion of PECVD TEOS-SiO_2 as a result of parasitic boron deposition during LT deposition of boron on flat/beveled oxide surfaces near micron-sized Si windows where the LOR is high [132].

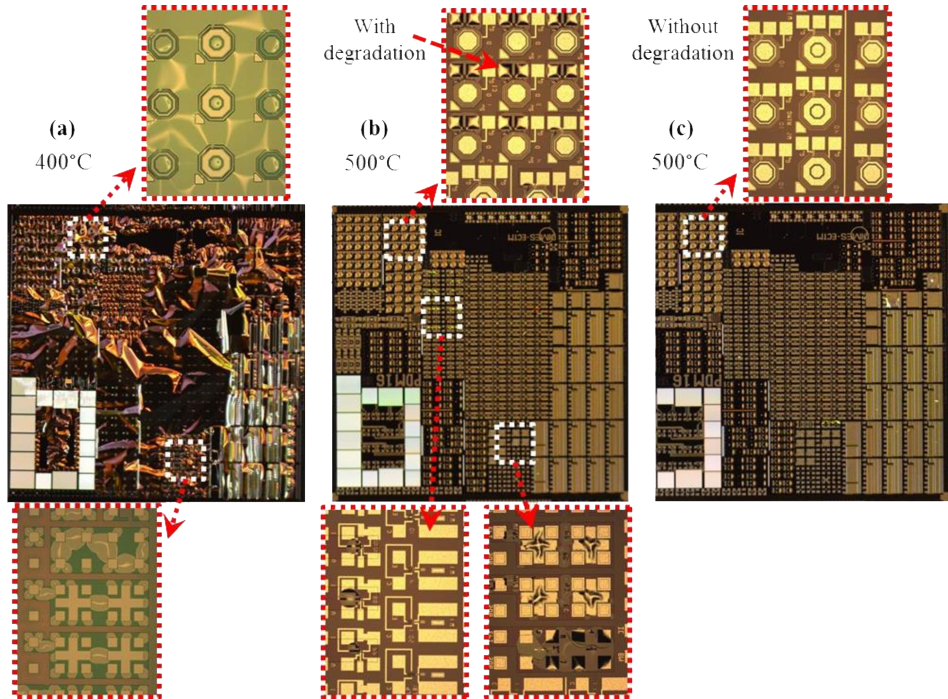

Fig. 5.15: Examples of poor adhesion and layer delamination for the same layout: (a) PECVD TEOS deposited over 400 °C boron. PVD Al deposited after PECVD TEOS deposition over 500 °C boron for two different dies on the same wafer where die. (b) Display of adhesion problems, although die (c) does not display the same adhesion problems as die (b). The insets show the zoom-in for different structures with micron-sized openings [132].

5.4.2 Precautions to minimize the parasitic boron deposition at low temperatures

There are a few precautions that can be taken to minimize the undesirable boron deposition on oxide. First, the better the oxide quality is, the lower the density will be of oxide surface-free sites and/or defects which reduce the chances of boron deposition. Second, the global/local oxide coverage ratios can be minimized in the layout of the oxide mask to reduce the accumulation of boron atoms over oxide areas. Likewise, the deposition and process parameters, like diborane partial pressure, gas flow, total deposition pressure, can be optimized to minimize the loading effects [119, 129] that otherwise will also

increase the accumulation of boron atoms over certain oxide areas, thus increasing the probability of parasitic boron deposition there. Also we have found, this poor adhesion could depend on the *ex-/in-situ* treatments before the PECVD TEOS-SiO_2 or PVD Al layers are deposited. Furthermore, the adhesion of these extra layers after boron deposition is also influenced by the exact conditions on the surface. For example, a large amount of hydrogen resides on the surface just after boron deposition and is in general known to reduce adhesion. This H coverage can be reduced by baking steps in air. An investigation of such extra treatments would have to be included in the process development when working with LT boron deposition.

By taking the aforementioned precautions into account, the LT boron deposition was successfully performed to create near-ideal diodes with low deep junction-like saturation currents.

5.5 Summary

A novel low temperature (LT, 400 °C) boron deposition technology is presented in this chapter. With this low processing temperature (400 °C), the boron layer can be deposited at the last step of the fabrication flowchart when the metal layers and implanted regions are already defined on the wafer. These can be affected by a deposition temperature of 700 °C but not 400 °C. Therefore with this LT technology, we believe that the boron deposition is fully compatible with standard IC/CMOS processes to integrate LT PureB photodiodes together with CMOS electronic interface circuits and other sensors on a single chip. In this way, smart sensor systems or even CCD or CMOS UV imagers can be realized. In Chapter 6, this technology is employed to fabricate a high stability, high performance DUV/VUV/low energy electron Si photodiode.

The temperature dependence of the kinetics of boron deposition on patterned Si/SiO_2 surfaces in the temperature range of 400 °C to 700 °C is investigated. Some selectivity issues that arise when the boron deposition temperature is reduced from 700 °C to 400 °C is discussed. This study shows that there is a large difference between the properties of the layers deposited at 400 °C and 700 °C. The latter are very smooth with a roughness of less than 2 angstroms for 2-nm-thick layers, and they deposit selectively on the Si surfaces

regardless of the Si window size. When the boron deposition temperature is brought down to 400 °C, the deposition rate drops considerably.

In the case of micron-sized small windows of silicon surrounded by large oxide areas, the oxide at the perimeter of the silicon window will be readily covered with an irregular, very rough, loosely bonded deposition of unwanted boron. However, for the same deposition conditions, millimeter-large windows may be found to be free of boron deposition due to a reduction in the amount of boron available for deposition in these regions. It has been found that the LOR[1] is one of the design parameters besides the process and chamber parameters that can be adjusted to reduce the parasitic boron deposition on oxide regions which otherwise can degrade the adhesion of subsequent depositions such as PECVD oxide or PVD Al. This must be taken into account when integrating low temperature boron process modules that, for example, could be used to add high quality (photo)diodes to fully processed CMOS wafers.

[1] Local oxide ratio

Chapter 6

Experimental results

In order to achieve better control of the boron deposition, in Chapter 3 an analytical model was proposed which described the deposition kinetics and the chamber deposition characteristics. With this model it becomes possible to predict the deposition rate of boron layers over the wafer. Chapter 4 presented optimization of the conventional high temperature (HT, 700 °C) PureB process to provide uniform and reliable deposition of 2-nm-thick HT boron layers with thickness variations of only a few angstroms. In Chapter 5 we introduced a novel process for low temperature (LT, 400 °C) boron deposition, which provides uniform, smooth, closed LT boron layers. This new process can be part of standard IC/CMOS processes.

In this chapter we demonstrate how the new knowledge presented in Chapters 3, 4 and 5 is employed to fabricate high performance PureB detectors particularly for low penetration photon/electron beam detection. First, in Section 6.1, we show how high responsivity, high stability PureB photodiodes with a 2-3 nm-thick boron top layer can be fabricated by an optimized HT PureB process, even when the boron is driven in by high temperature annealing. In Section 6.2 it is shown that the LT boron depositions performed at 400 °C can be used to create p^+n photodiodes with nm-thin boron only-beam-entrance windows and near-theoretical sensitivity for irradiation with either UV light or low energy electrons down to 200 eV, with negligible optical and electrical degradation.

6.1 High performance UV Si photodiodes with optimized HT boron layer

The high performance of the detectors is directly related to the properties of the boron layer itself. Boron layers are deposited by chemical vapor deposition on a clean Si surface conventionally at 700 ºC (HT) as described in Chapter 2. The boron layer can at the same time form both the anode region of a damage-free p^+n nanometer-shallow junction and a robust radiation front entrance window that can be as thin as 2 nm [21, 53]. At 700 ºC the deposited layer is compact and smooth with a low, well controlled deposition rate [119].

In this section all the knowledge obtained on basis of this thesis, regarding the optimization of the thickness and uniformity of the HT boron layer, is employed to fabricate high performance VUV Si photodiodes for the situation where high temperature (900 ºC) thermal processing is performed after the initial boron deposition. Such extra thermal processing can be necessary to, for example, reduce the photodiode series resistance [53] from the as-deposited 10 kΩ/sq value down to a few hundred Ω/sq, or to make integrating the PureB process in the frontend CMOS process flow feasible.

With respect to responsivity and stability for exposure to EUVV/VUV light, the best results have been achieved by compensating the boron layer for any boron loss during annealing due to boron desorption or diffusion into the Si. Besides this, the second boron deposition improves the layer uniformity and coverage. Also it maintains the monolayer of holes at the boron/Si interface to the initial high value. The responsivity obtained is much higher than what has previously been reported, because the bulk doping profiles of the driven in boron are considered [52].

6.1.1 Experimental procedure

Large 10 mm × 10 mm photodiodes with a boron-only front entrance window were fabricated as described in Appendix B. The varied deposition parameters for the photodiodes studied in this part are listed in Table 6.1. Photodiodes (PD) are named based on their deposition/process parameters as PD(annealing time, final boron layer thickness).

Table 6.1: List of photodiode fabrication specifications: annealing times for 900 ºC annealing of initial 2.2-nm boron deposition and simulated junction depth; ellipsometry measurement of thickness and roughness of boron layer after final deposition.

Photodiode type [a]	Dep. conditions		1st boron deposition			Annealing (900°C)				2nd boron deposition			Final boron layer[e]	
	Diborane Partial Pressure [b]	*Gas flow*[c]	*Dep Time*	*B. Thick.*[e] *(nm)*	*B. Rough.*[e] *(nm)*	*AN Time*	*Junction depth* [d] *(nm)*	*B. Thick. after AN* [e] *(nm)*	*B. Rough. after AN* [e] *(nm)*	*Dep Time*	*B. Thick.*[e] *(nm)*	*B. Rough.*[e] *(nm)*	*B. Thick. (nm)*	*Std Dev (48 dies)*
PD(0,2.21)	70% P_1	F_1	7'40"	2.21	0.41	0	5	---	---	---	---	---	2.21	0.055
PD(15",2.22)	70% P_1	F_1	8'	2.18	0.41	15"	23	1.91	0.87	20"	2.22	0.76	2.22	0.056
PD(30",2.29)	70% P_1	F_1	8'	2.18	0.41	30"	32	1.77	0.89	45"	2.29	0.84	2.29	0.063
PD(1',2.33)	70% P_1	F_1	8'	2.18	0.41	1'	46	1.36	0.91	1'20"	2.33	0.91	2.33	0.058
PD(5',2.39)	70% P_1	F_1	8'	2.18	0.41	5'	103	0.97	0.93	2'50"	2.39	0.98	2.39	0.065
PD(5',0)	P_1	F_1	10'	~4	---	5'	103	---	---	---	---	---	0	---
PD(20',0)	P_1	F_1	30'	~15	---	20'	206	---	---	---	---	---	0	---

[a] Photodiode: PD(annealing time, final boron layer thickness)
[b] P_1: Max diborane partial pressure, 3.39 mtorr [119].
[c] F_1: Max carrier gas flow, 20 slm [119].
[d] Simulation based data given in ref. [6, 53, 67].
[e] Based on ellipsometry measurements.

After the deposition of an initial 2.2-nm-thick boron layer, an *in-situ* annealing/drive-in at 900 ºC was performed for 15 s, 30 s, 1 min and 5 min. Optimization procedures have been developed to achieve uniformity in the angstrom range (see Chapter 4) [116, 119, 129, 130]. The importance of doing this is underlined by the photodetector active area maps shown in Fig. 6.1, where the effect of minimizing local loading effects can be clearly seen, particularly at the corners of the dies where transport of boron species from the surrounding oxide areas can significantly thicken the boron layer.

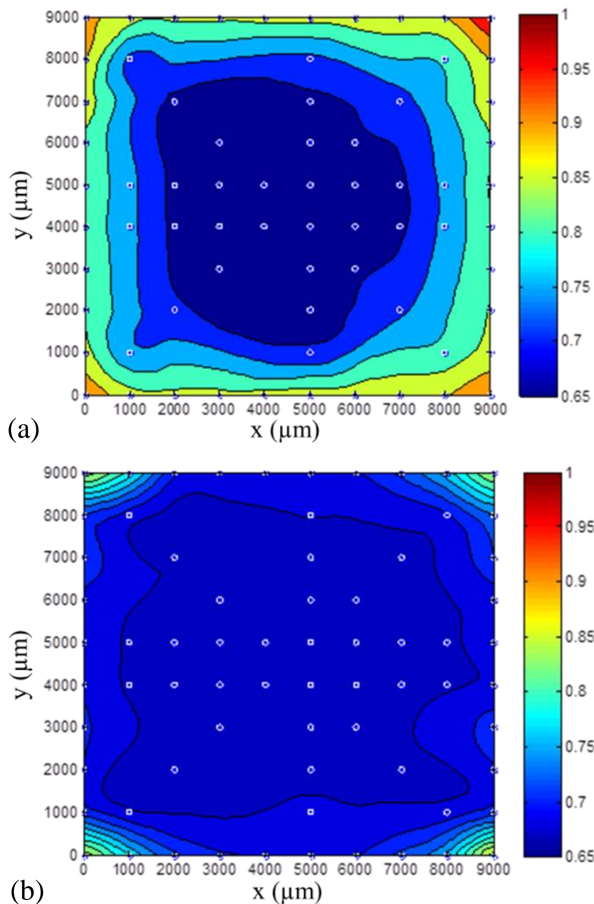

Fig. 6.1: 2D map of boron layer thickness uniformity over the 9.6×9.6 mm^2 photodetector active area extracted from 1 keV E-beam measurements [60]: (a) before and (b) after optimization of a 2.5-nm thick layer to minimize local loading effects.

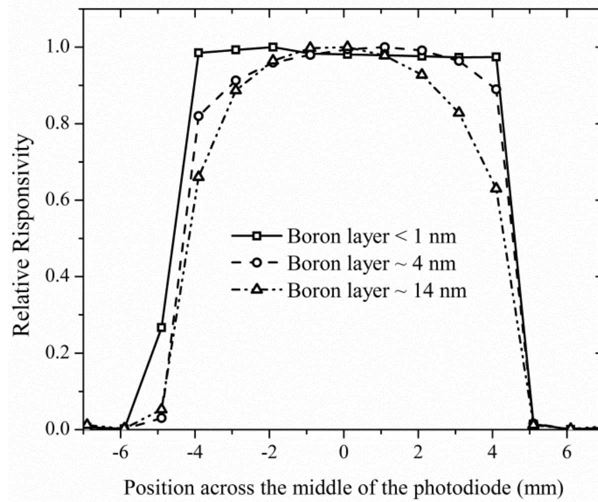

Fig. 6.2: Measured relative responsivity across the middle of three photodiodes with non-optimized boron layer uniformity, for exposure to 193 nm of light. The absolute responsivity in the middle of the three dies is 0.1 A/W, 0.09 A/W and 0.035 A/W for the < 1-nm,~ 4-nm and ~14-nm thick layers, respectively [53].

In Fig. 6.2 the responsivity to 193 nm of light is shown for a non-optimized case. For this wavelength the photon attenuation length in Si is only 7 nm, so for the thicker layers the non-uniformity due to the local loading effect becomes very visible and almost cuts the responsivity at the edge of the photoactive anode area in half.

Ellipsometry is used as a non-destructive, in-line method of monitoring the boron layer thickness. It was used here to tailor a second deposition after annealing to obtain a final layer thickness close to the initial 2.2 nm. However, as can be seen from the ellipsometry measurements listed in Table 6.1, the roughness increases with rising annealing time. This is very likely because the boron loss during annealing exposes the Si at certain points of the surface in an irregular manner. The incubation time for deposition on the Si will result in thinner boron coverage of the bare Si spots and thus a greater amount of roughness. For the PD(900,20') device, a 15-nm-thick layer was first grown, covered with 300-nm LPCVD oxide and annealed for 20 min at 900 °C. The oxide was removed along with practically all of the boron layer. This leaves the Si surface susceptible to native oxide growth and an oxide layer of about 10 nm thick is indeed verified by ellipsometry [52].

6.1.2 Electrical characterization

All the photodiodes have near ideal I-V characteristics, typical of PureB diodes [17, 49, 50, 53]. Fig. 6.3 shows across-the-wafer spread of the dark current for wafers with different thermal processing at 900 ºC, as specified in Table 6.1. The spread is small and the bulk of the dark current values lie in the 50 pA to 500 pA range, but a significant difference can be seen in some cases that can be related to the integrity of the interface. An explanation for the cause of this spread is that these devices have experienced two critical processing steps which probably cause a deterioration of the boron/silicon interface and seriously increase the spread. The first one is the anode window opening. In this step, any type of contamination left on the Si surface will prevent deposition of the boron and make spots or pinholes in the layer. The other one is the HF removal of the Al to the boron surface. Any tiny pinholes in this step may become worse if the etching is not stopped in time, resulting in oxide formation at these locations. As can be seen in Fig. 6.3, the highest dark current/spread is that of the PD(0,2.21) and PD(20',0) wafers. For the former, the junction is very close to the boron/silicon interface and the current is therefore more susceptible to interface defects. The latter, on the other hand, has a native oxide interface instead of boron directly on the Si. For the other wafers, the spread and minimum dark current values decrease as the junction depth—and p-region Gummel number—increase.

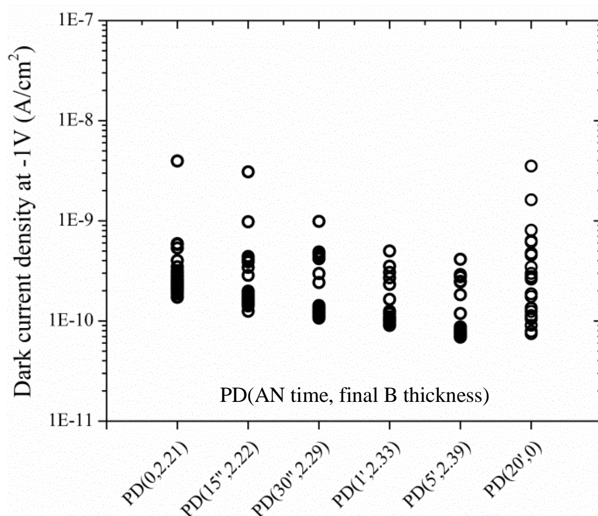

Fig. 6.3: Across-the-wafer spread of the dark current for wafers with different thermal processing at 900 ºC, as specified in Table 6.1.

Apart from this sort of process-related degradation of the electrical characteristics, the (1×1) cm^2 devices cannot be discerned on the basis of their I-V characteristics. In all cases, when no damaging process problems are encountered, the overall level of the dark currents is attractively low but presumably above the ideal value due to some small distribution of defects. The 400 °C depositions deliver similar low dark currents, as will be seen in the Section 6.2.

6.1.3 **Optical characterization**

The EUV and VUV responsivity of the photodiodes is shown in Fig. 6.5**:** and Fig. 6.5**:** respectively. For all annealed samples the responsivity is much higher than would be expected if the non-depleted p-doped region were a dead-layer.

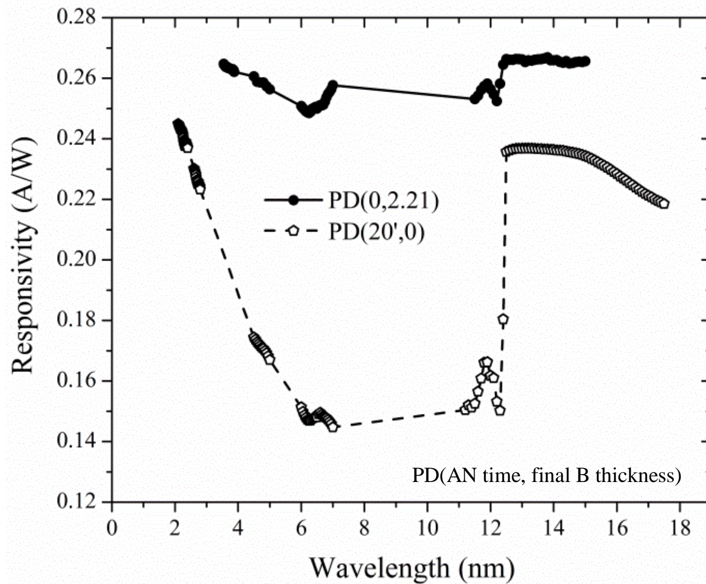

Fig. 6.4: EUV responsivity of the photodiodes with no annealing PD(0,2.21) and 20-min annealing PD(20’,0). For the latter photodiode, the lack of significant absorption at the boron edge (6.8 nm) confirms that the boron layer has been removed. The responsivity at 13.5 nm of the PD(0,2.21) sample is very close to the theoretical value of 0.273 A/W.

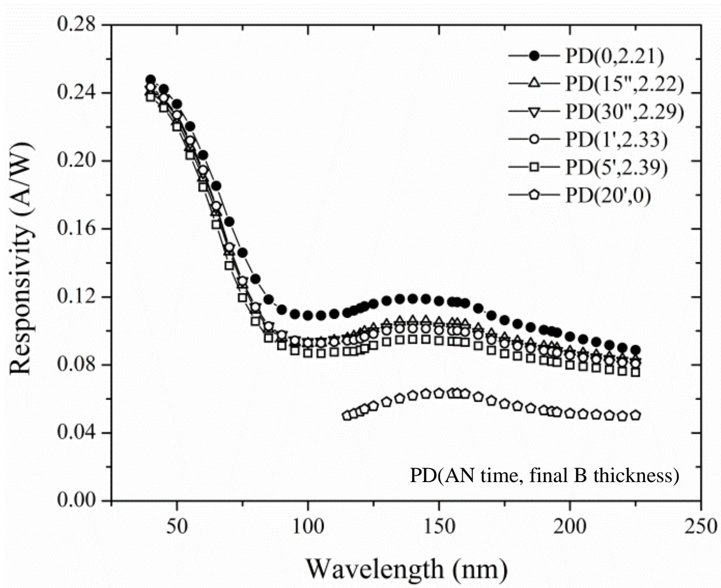

Fig. 6.5: VUV range responsivity of all the photodiodes. See their processing parameters in Table 6.1.

Table 6.2: Measured responsivity at 193 nm of light; relative drop in responsivity is given in brackets.

Photodiode type[a]	**Responsivity (A/W)**
PD(0,2.21)	0.1
PD(15”,2.22)	0.09 (10%)[b]
PD(30”,2.29)	0.089 (11%)
PD(1’,2.33)	0.088 (12%)
PD(5’,2.39)	0.082 (18%)
PD(20’,0)	0.053 (47%)

[a] PhotoDiode(annealing time, final boron layer thickness) based on Table 6.1.
[b] Relative drop in responsivity with respect to the non-annealed photodiode.

In the

Table **6.2**, the relative drop in responsivity is also given in brackets. It is evident that both types of electric fields contribute to improving the responsivity. However, without the extra hole layer and associated very high field strength at the interface, the high measured responsivity cannot be accounted for.

In Fig. 6.6**:** the across-the-die uniformity of the responsivity is shown for an exposure with 70 nm and 193 nm of light respectively with only less than 5% responsivity variation compare to 30% variation of the responsivity for non-optimized PureB samples. This uniformity is visible for the as-deposited PureB photodetector as well as the ones experiencing drive-in with different annealing times at 900 ºC, compared with the Fig. 6.2 where the responsivity to 193 nm of light is shown for a non-optimized case.

By closer look to the Fig. 6.6**:**, it can be found that for 193 nm the responsivity drops as the annealing time increases, as would be expected if the absorption in the non-depleted p^+-Si region dominates. However, for 70 nm the 15", 30"and 1' annealings show the opposite trend and it seems the absorption in the boron layer dominates. The same trend can also be found in Fig. 6.5**:** for the exposure to 40 nm and 150 nm of light. The cross-over point is at about 100 nm, as illustrated in Fig. 6.7. In the region below about 100 nm, the absorption in the boron layer becomes much stronger than at 150 nm (or 193 nm), while the attenuation in the Si decreases [68].

Although the ellipsometry measurements suggest that the final deposited boron layer thickness increases slightly for the samples with the longer annealing time which means that the boron was over deposited during the 2nd deposition. However the longer annealing time the higher roughness will be. Due to the exponential relation between light absorption and depth in the absorbing material, this higher roughness may significantly increase the amount of light reaching the Si, thus increasing the responsivity even though the junction depth in the Si is increasing.

Ellipsometry results suggest a thin oxide layer (up to few nm) on the surface of the PD(20',0) sample [52]. Above a wavelength of ~100 nm the optical characteristics of SiO_2 changes abruptly, going from being highly absorbing to transparent. The thickness can be adjusted to achieve anti-reflection for each specific wavelength. However, even when accounting for anti-reflection, the responsivity of this sample is still lower than what is

predicted if the effect of the interface hole-layer is included. As a side note it should be mentioned that it cannot be entirely excluded that the morphology of the boron layer has an effect on the reflectivity of the Si. However, the layer is considered to be so thin that any such effect would be very small.

A very important parameter for lithography applications is the stability. It is tested here by the long time exposures specified in Fig. 6.8. The photodiodes with a complete boron coverage show good stability while the PD(20',0) with oxide coverage degrades considerably, confirming the robust nature of the boron layer with respect to charging and photo-generated interface traps.

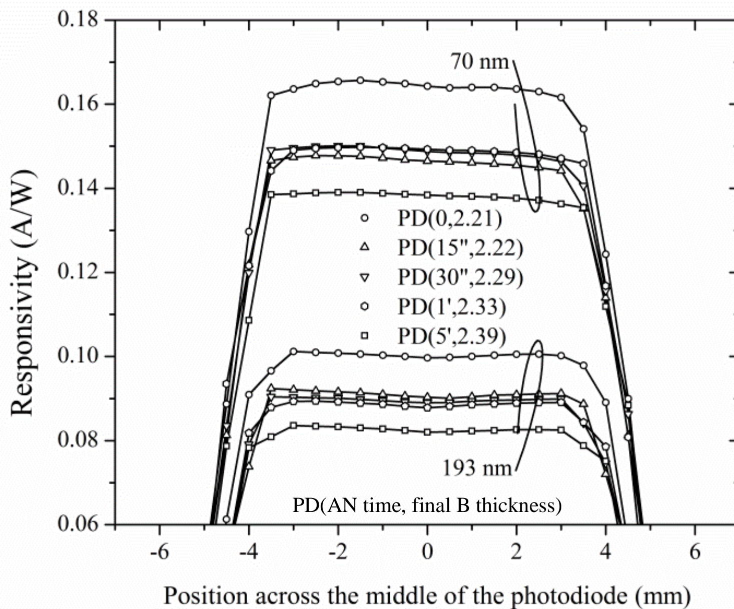

Fig. 6.6: Responsivity of the photodiodes with a final ~ 2.3-nm-thick boron layer measured across the middle of the diode and for exposure with 70 nm of light (see photodiodes types in Table 6.1).

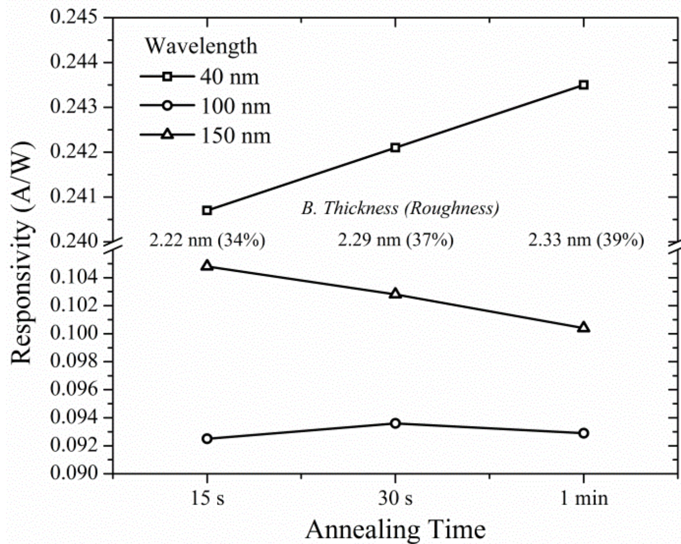

Fig. 6.7: Examples of responsivity for the photodiodes with the three shortest annealing times for exposure to 40 nm, 100 nm and 150 nm of light. For each annealing time the correspond boron layer thickness and percentage of the layer roughness (in the parenthesis) are also given. For the entire series of wavelengths measured and plotted in Fig. 6.4, there is a transition from decreasing to increasing responsivity as a function of annealing time as the wavelength goes from 150 nm down to 40 nm.

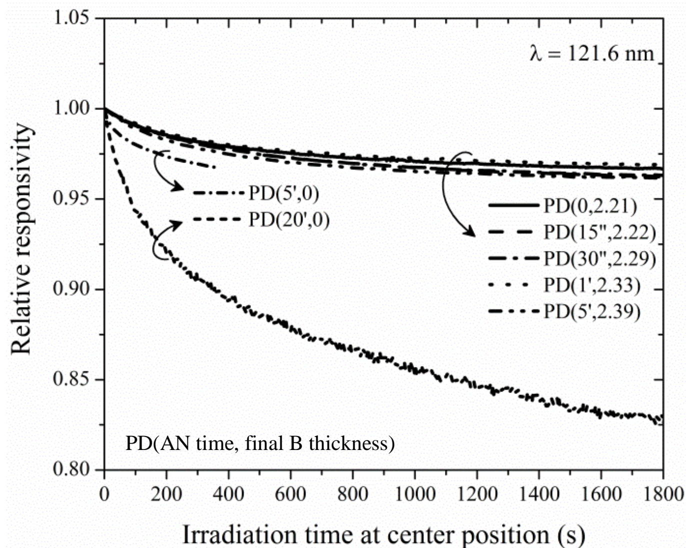

Fig. 6.8: Measured optical stability as a function of time for a total radiant exposure at a 121-nm wavelength of about 0.3 mJ in the central mm of the photodiodes (see photodiodes types in Table 6.1).

6.2 VUV/Low energy electron Si photodiodes with post-metal 400 °C boron deposition

Another VUV-sensitive process, which was reported in the work of B. C. Jacquot, *et al.* [9], has been integrated in back-illuminated CCD/CMOS imagers with good responsivity results by using boron delta doping of the Si near the surface. Here, the surface of the beam entrance window is SiO_2. However, no data on the effect of high level exposure was supplied. In general, it is well known that SiO_2/Si interfaces degrade due to the beam-induced creation of interface states which can cause degradation of both dark current and responsivity [48]. In the following, the experimental data will also be compared with this reference.

6.2.1 **Experimental procedure**

Fig. 6.9 shows the schematics of the basic process flows for the fabrication of photodiodes made with LT boron deposition, either before or after metallization. The LT boron deposition is performed at 400 °C as described in Chapter 5. In the pre-metal boron deposition case with either a HT or LT deposition, the metal directly contacts the entire boron surface. The central beam-sensitive area is opened by selectively removing the metal to the boron layer first by plasma etching and then HF wet etching [48]. The process flow is described in Appendix B. With the LT depositions it is also possible to deposit boron after the metal has been deposited (Fig. 6.9b). In this case the contact with the boron layer is made via a p^+-guard ring that is implanted and annealed before metallization. This flow has the advantage that the as-grown boron layer directly forms the beam entrance window and needs no post-processing such as metal removal, which can be a critical step [48].

A test was done to prove that the epi-reactor is free from any metal contamination during post-metal LT boron depositions (Fig. 6.9b). Three wafers were prepared as described in Table 6.3, and the amount of Al contamination was detected using surface secondary ion mass spectroscopy (SIMS). These measurements were done at the laboratory of Evans Analytical Group® (EAG) in the USA. The results as presented in Table 6.3 and Appendix C indicate that there was no detectable cross-Al contamination during processing such wafers at 400 °C.

Table 6.3: Results of surface SIMS for Al contamination test.

Sample nr.	Sample description	Al level (atom/cm^2)
#1	Bare Si wafer directly from box	9.80×10^9
#2	Bare Si wafer annealed for 60 min at 400°C for background contamination test	8.02×10^9
#3	Bare wafer annealed together with metal wafer for 60 min at 400°C for cross-contamination test	7.53×10^9

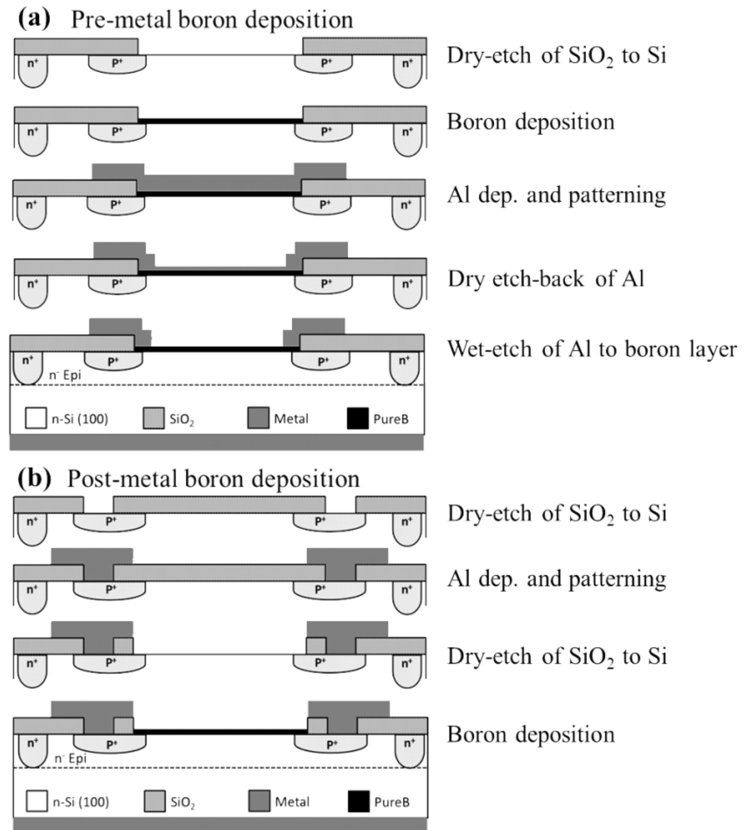

Fig. 6.9: Schematic of the fabricated photodiodes with boron-only beam entrance windows, for boron deposition either before (a) or after (b) the metallization.

6.2.2 Electrical characterization

In Fig. 6.10 the I-V characteristics of the LT and HT PureB photodiodes are compared based on (10×10) mm^2 devices with an active area of 9.6 mm × 9.6 mm. They were exposed to 1 keV electron irradiation. No degradation was observed and the current levels were similar in all cases: the saturation current density was below 100 pA/cm^2 at 1 V reverse voltage with a minimum value of 20 pA/cm^2 for the post-metallization PureB device. Both the HT and LT diodes with areas as small as 1 µm × 1 µm were found to be near-ideal, with or without the use of a *p*-guard ring at the window perimeter. This confirms that the boron coverage is complete and effective to the oxide edge. An example is included in Fig. 6.10.

In Fig. 6.11 the I-V characteristics across the wafer are plotted for the two types of LT PureB photodiodes showing a very tight distribution of low dark currents. A dark current value of 15 pA at -1 V was measured for post-metal devices with an active area of 9.6 mm × 9.6 mm, which is among the lowest ever measured for PureB devices and may be related to the fact that no post-PureB processing was performed.

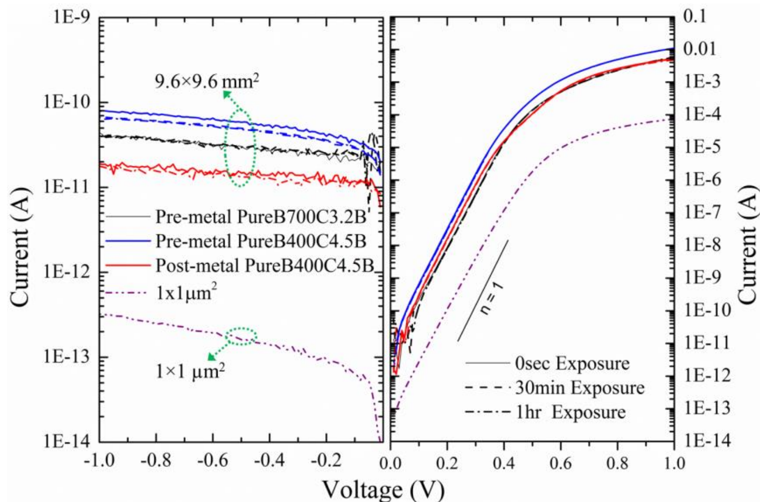

Fig. 6.10: Measured I-V characteristics of HT and LT photodiodes, with and without electron irradiation at 1 keV for either 30 min or 60 min with an active area of (9.6×9.6) mm^2. The boron layer thickness was measured by ellipsometry to be 3.2 nm for the HT diode and 4.5 nm for the two LT diodes for which the boron layer was deposited before (pre-metal) and after (post-metal) metallization. The (1×1) μm^2 LT diode was Al-covered and without a *p*-guard ring [131].

However, the good performance observed is still remarkable since the 400 °C devices were loaded into the CVD reactor and deposited at this temperature, and therefore they did not have the benefit of *in-situ* surface cleaning by H-baking at higher temperatures like the other devices. All in all, both types of LT devices performing so well strongly supports the idea that an effective hole layer with a strong concentration gradient creates an electric field that repels the injected minority carrier electrons away from the interface as can be seen in Fig. 6.5 and Fig. 6.6.

Statistics of across-the-wafer spread of the current (reverse and forward) is presented in Table 6.4. The spread of dark current at -1 V is small and its average values lie in the range of ~50 pA and ~150 pA for post- and pre-metal LT photodiodes, respectively. These show that the pre-metal devices have almost three times more leakage current than post-metal devices. The reason would be that there are two critical processing steps that can cause a deterioration of the boron/silicon interface and seriously increase the spread (see process flow described in Appendix B). The one is the anode window opening. Any contamination of the Si surface, either from the oxide isolation or wet etching/cleaning steps, will prevent deposition of boron, leaving thin spots or pin holes in the layer. The other critical step is the HF removal of the Al to the boron surface. Although boron has an extremely low etch-rate in both buffered and diluted HF, thin spots, for example due to contamination on the Si surface, may become pin holes if the etching is not stopped in time. Where a pin hole exposes the Si to air, oxide may form and become a source of generation-recombination centers. Since Al etching is not included in the post-metal PureB process (see Fig. 6.9), the post-metal devices have the lowest ever measured dark current value.

Table 6.4: Statistics of across-the-wafer spread of the reverse and forward current.

Type of LT photodiode	I_{Spread}			
	Bias	-1V	0.2 V	0.3 V
Post-metal PureB photodiode	min	19.15 pA	16.18 nA	0.64 µA
	av	55.75 pA	20.09 nA	0.85 µA
Pre-metal PureB photodiode	min	78.45 pA	32.01 nA	1.53 µA
	av	129.73 pA	53.56 nA	2.42 µA

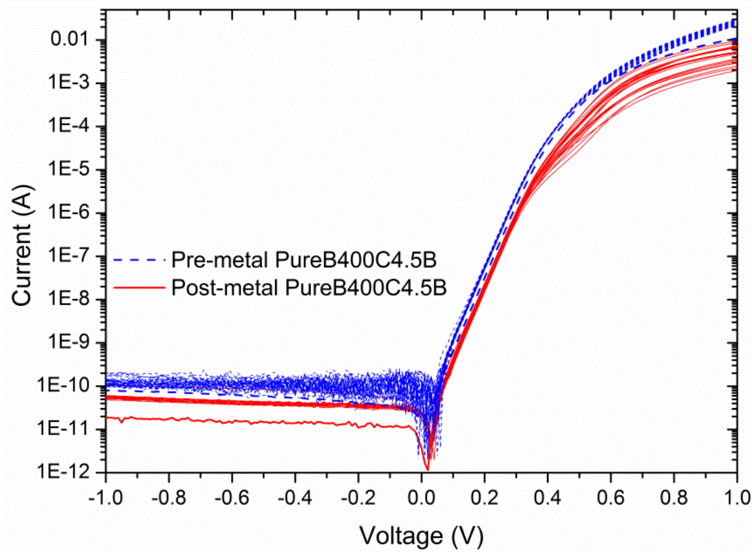

Fig. 6.11: The I-V characteristics of the pre- and post-metal LT photodiodes for 52 devices measured over the wafer. The active area is 9.6 mm × 9.6 mm.

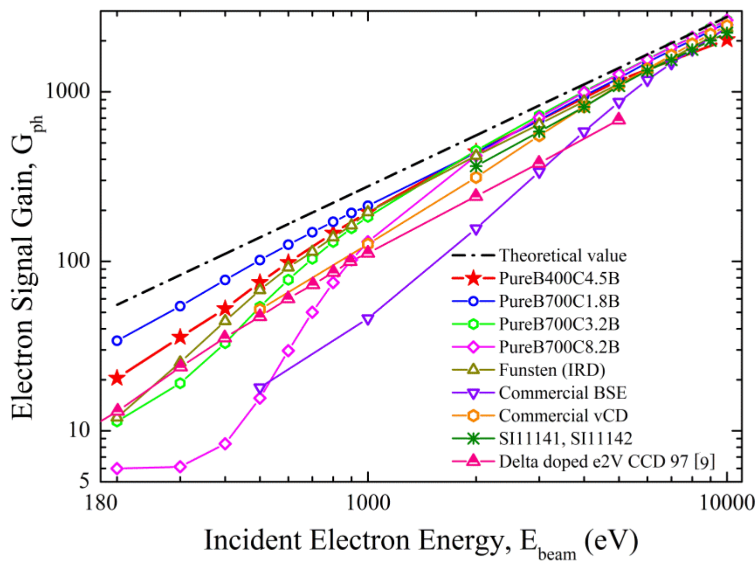

Fig. 6.12: Measured electron signal gain for LT and HT PureB photodiodes (area 9.6 $mm^2 \times 9.6\ mm^2$), compared to commercially available devices as well as the theoretical value and results reported in [9, 48]. The HT diodes have boron layer thicknesses of 1.8 nm, 3.2 nm, or 8.2 nm; the LT diodes have a 4.5-nm-thick layer.

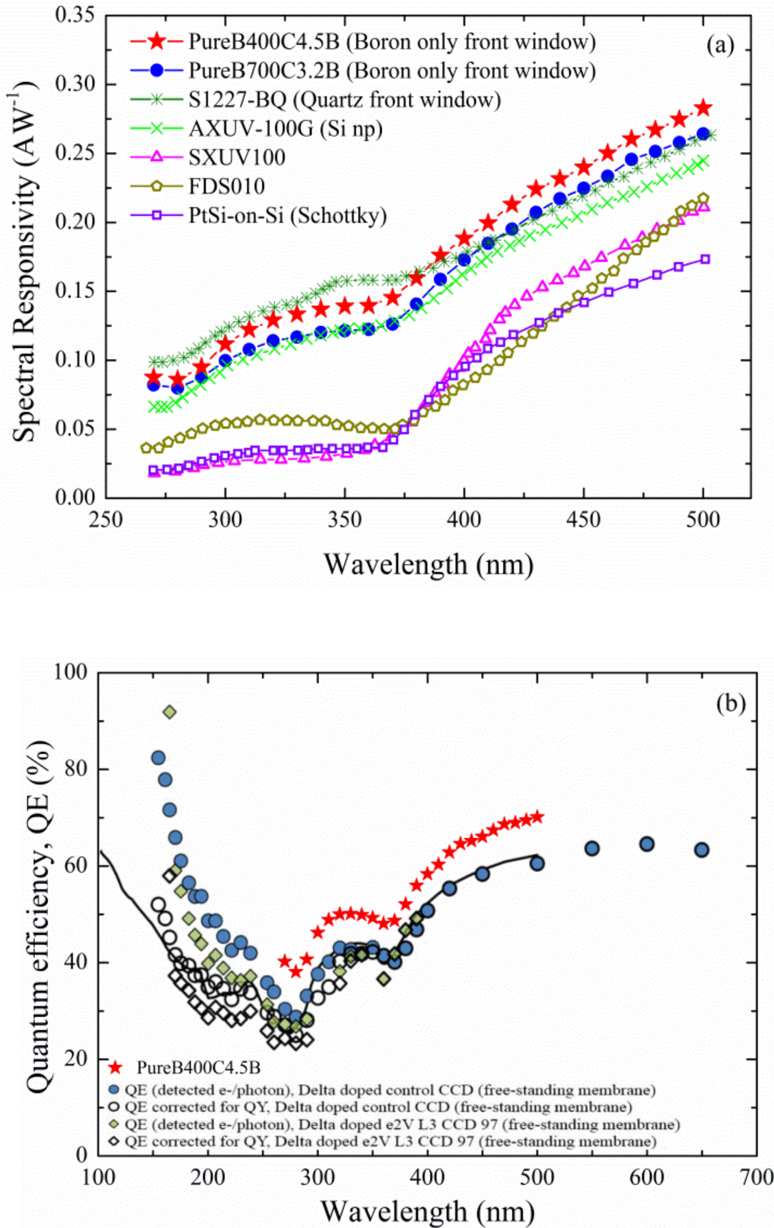

Fig. 6.13: Measured UV spectral responsivity (a) and quantum efficiency (b) of HT and LT PureB photodiodes (area 9.6 mm × 9.6 mm), compared to that of a number of commercial UV photodiodes (a) and results reported in [9] (b).

6.2.3 Optical characterization

In Fig. 6.12 the electron signal gain is plotted for PureB diodes in comparison to commercial electron detectors, a delta-doped CCD from [9], and the theoretical values found in [48].

Just like the HT PureB devices, the LT devices have near-theoretical sensitivity. The electron signal gains are measured 94% and 90% of the theoretical value at 1 KeV and 60% and 40% of the theoretical value at 200 eV for HT and LT PureB photodiodes (area 9.6 $mm^2 \times 9.6\ mm^2$) respectively. The absorption in the boron layer itself is visible from the slightly decreasing gain in the series of HT devices with layer thicknesses of 1.8 nm, 3.2 nm, and 8.2 nm, respectively. Nevertheless, the gain is nearly ideal also for the LT device with a 4.5-nm boron layer if the backscatter losses are considered to be 5%.

In Fig. 6.13 the measured UV responsivity down to a wavelength of 270 nm is displayed for both HT and LT photodiodes, showing slightly higher values for the LT device. This is possibly due to the higher surface roughness, which reduces reflectivity and/or absorption in the boron layer. The graph includes a comparison to commercial VUV devices some of which take advantage of the SiO_2 layers to reduce reflectivity and thus increase the responsivity. Also included is one of the back-illuminated CCD imagers reported in [9] with the highest responsivity. The PureB diodes have a very small absorption in the boron layer and display near-ideal responsivity if the reflectivity is assumed to be that of a bare Si surface.

Fig. 6.14 shows the measured responsivity in the VUV spectral range (120 nm - 400 nm) for both pre-metal and post-metal LT PureB photodiodes (PureB400C4.5B premetal/postmetal). As can be seen in this figure, the response for pre-metal photodiodes is slightly higher than post-metal ones. This could be explained by a small thinning of the boron layer due to the extra processing necessary to open the light entrance window (see Fig. 6.9). The HT PureB device is also shown in Fig. 6.14 as a reference. As will be commented on next, the rough LT boron surface proves to be much less chemically resilient than the smooth HT boron layers.

The optical stability of the post-metal LT PureB photodetector (PureB400C4.5B postmetal) is measured by exposing the center of the dies to high dose VUV irradiation. The high dose exposure is performed with a circular beam spot with a diameter of 1 mm, to a radiant exposure of 37 J/cm^2. The LT PureB photodiodes are found to be highly stable. As an example, the resulting

responsivity at the center of the post-metal LT PureB photodiode is included in Fig. 6.14. A slight reduction in the responsivity is visible with a decrease in the wavelength. This is seen more clearly in Fig. 6.15 where scans over the photodiode surface are shown for measurements with either 121 nm or 193 nm of light.

A slight dip in responsivity becomes clear for the 121 nm measurement. This is the result of build-up of carbon contamination during exposure. To remove this layer an ozone cleaning procedure is performed. For the HT devices, the cleaning procedure successfully removes the contamination, and the original high responsivity is regained [22]. In contrast, the LT device was not able to withstand this treatment, probably due to the rougher surface structure [131] that makes the boron more susceptible to oxidation. The higher responsivity after standard ozone cleaning suggests that the boron layer is thinned considerably, as can be seen in Fig. 6.14 and Fig. 6.15. The more visible dip seen for both measurement wavelengths is no doubt due to a reduced thinning where carbon contamination was present. Therefore, although the as-deposited LT boron layer is optically robust, it does not have the same degree of chemical resistance as the HT layers.

The LT and HT diodes are also tested for 1 keV electron irradiation with an exposed area of 1 mm^2 and a dose rate of 52.44 $\mu C/mm^2$, as shown in Fig. 6.16. The small decrease in gain of about 2% for both cases can be associated with the build-up of carbon on the exposed diode surface [136] as indicated by a clear discoloration in the SEM image of the exposed area, which is included as an inset in Fig. 6.16.

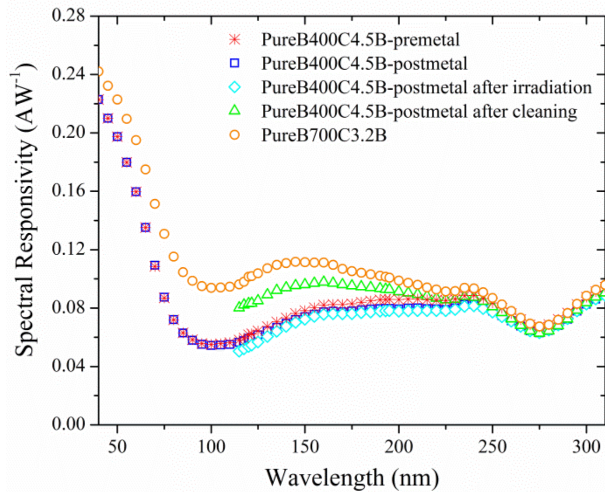

Fig. 6.14: Measured VUV spectral responsivity as a function of wavelength for HT and LT PureB photodiodes (area 9.6 mm^2 × 9.6 mm^2) before and after high level irradiation and after a final cleaning procedure.

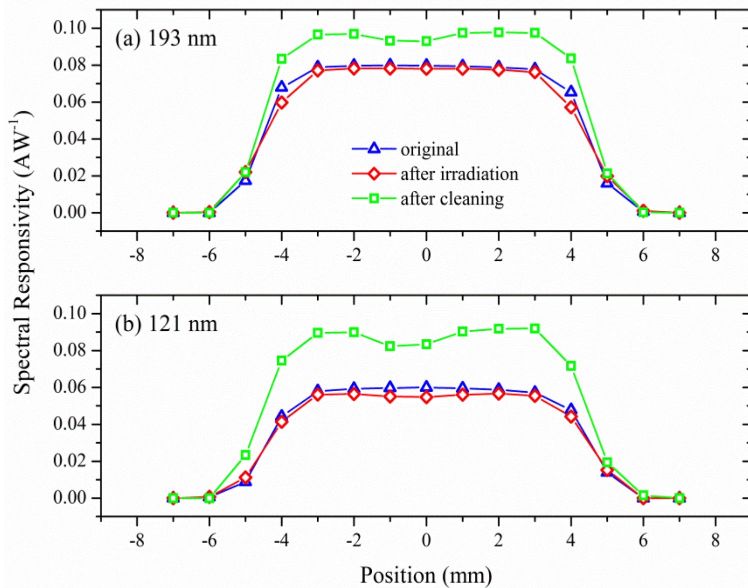

Fig. 6.15: Measured responsivity over the LT PureB photodiode at wavelengths of 193 nm and 121 nm, before and after high dose exposure, and after cleaning. The high dose exposure was performed with a circular beam spot with ø1 mm to a radiant exposure of 37 J/cm^2.

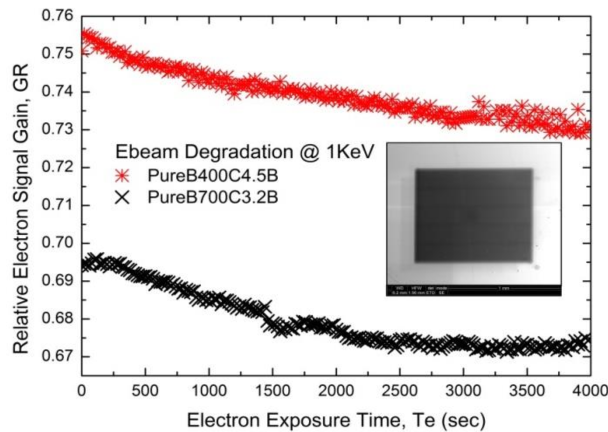

Fig. 6.16: Measured electron signal gain relative to the theoretical value as defined in [48], for LT and HT PureB photodiodes (area 9.6 mm^2 × 9.6 mm^2) as a function of exposure time for an exposed area of 1 mm^2 and a dose rate of 52.44 μC/mm^2 of 1 keV electrons. The inset shows a discoloration of the exposed area known to be due to a build-up of carbon on the exposed diode surface [136].

6.3 Summary

The overall results presented in the first part of this chapter show that high responsivity, highly stable PureB photodiodes with a 2-3 nm-thick boron-only front entrance window, can be fabricated with optimized HT technology as described in Chapter 4, even when the boron is driven-in by high temperature annealing. After the drive-in, an extra boron deposition is performed to maintain: (i) the desired layer thickness and the complete boron coverage necessary for maintaining high stability; and (ii) a monolayer of holes residing at the boron /Si interface. This monolayer of holes at the boron-silicon interface can give a very high electric field that repels photon-generated electrons from the interface thus substantially increasing the responsivity to high values measured even for 100-nm junction depths. This tolerance to thermal processing at temperatures above the boron deposition temperature contributes to the high CMOS compatibility of the PureB technology. Moreover, considering that most of these results were achieved by only using the advantages of the optimized HT PureB technology with the existing layouts but without the need to change the design, this technology is interesting and easy to use.

In the second part, it was shown that the LT boron depositions performed at 400°C can be used to create p^+n photodiodes with nm-thin boron-only beam

entrance windows and near-theoretical sensitivity for irradiation with either VUV/DUV/EUV lights down to a wavelength of 10 nm or low energy electrons down to 200 eV. Very low dark current of only 15 pA at -1 V bias voltage, was measured for post-metal LT PureB devices with anode area of 9.6 $mm^2 \times 9.6$ mm^2, which we relate to the fact that no post-PureB processing was performed.

Measurement results also show the reasonably good stability of the LT PureB devices. For high level exposure to either VUV irradiation or 1 keV electrons, there was negligible optical or electrical degradation. Even for devices without p^+-guard rings, the complete perimeter coverage of the LT boron layer ensures that near-ideal diodes are created. The LT boron deposition can be performed after metallization to create near-ideal diodes with low, deep junction-like, saturation currents which make the technology attractive for adding many types of diode-based functions to fully processed CMOS wafers. Hence, LT PureB photodiodes can be integrated together with electronic interface circuits and other sensors on a single chip. In this way, smart sensor systems or even CCD or CMOS UV imagers can be realized.

Chapter 7

Conclusions and recommendations

This thesis presents a study of the existing PureB technology for production of silicon detectors for UV radiation and low energy electron beams, with the main objective to recommend methods and practical solutions for: (i) improving the spatial uniformity of the deposited boron layer leading to significantly improved spatial uniformity of the responsivity of the PureB photodetectors, and (ii) making the PureB technology compatible with standard CMOS processes by reducing the boron deposition temperature below 450ºC.

The results of this research work have already been used in several other research and production activities related to a variety of applications such as those mentioned in Chapter 2 (L. Shi [6], A. Šakić [10]), and photodetectors fabricated by Iszgro Diodes BV.

In this chapter the major contributions of this research work are presented and recommendations for future work are shortly discussed.

7.1 Research achievements

The major achievements of this research work are:

- State-of-the-art PureB Si-based detectors are reviewed and their advantages and drawbacks are summarized, as detectors in the ultraviolet (UV) spectral range and also for low energy electron detection.

- The surface reaction mechanisms of boron CVD deposition are investigated to determine the activation energies of boron layer deposition at temperatures from 350 ºC to 850 ºC, with hydrogen and nitrogen as carrier gases.
- An analytical model is developed to describe the deposition kinetics and the deposition chamber characteristics that determine the deposition rate of boron layers over the wafer which is applicable for both ASMI Epsilon One and Epsilon 2000 reactors with completely different reactor conditions.
- The "end-of-line resistance measurement" is introduced as a non-destructive, accurate means of monitoring the boron layer uniformity with fine resolution.
- The pattern dependency and the loading effect of the HT boron deposition is investigated as a source of non-uniformity of the boron layer. The diffusion length of boron atoms along boron/silicon surfaces is obtained, both experimentally and analytically, to be about 2.2 mm for a boron deposition temperature of 700 °C and less than 1 mm, and for boron deposition temperatures below 500 °C.
- Methods are proposed on basis of the knowledge obtained in this thesis to control and minimize the pattern dependency and the loading effect during the deposition by slightly modifying the process flow, adjusting some recipe parameters and changing wafer layouts or die design (if necessary), to such a degree that the 2-nm-thick boron layer used in the present day applications can be deposited uniformly with variations in thickness of only a few angstroms.
- A novel low temperature (LT, 400 °C) boron deposition technology is developed. The temperature dependence of the kinetics of the boron deposition on patterned Si/SiO_2 surfaces in the temperature range of 400 °C to 700 °C is investigated. Selectivity issues that arise when the boron deposition temperature is reduced from 700 °C to 400 °C are discussed.
- An optimized high temperature (HT, 700 °C) PureB technology is employed to fabricate highly stable and sensitive PureB photodiodes with a 2-3 nm-thick boron-only front entrance window, even when the boron is driven-in by higher temperature annealing.

- It has be demonstrated experimentally that LT boron deposition can be performed after metallization to create near-ideal diodes with low, deep, junction-like saturation currents, which makes the technology attractive for adding many types of diode-based functions to fully processed CMOS wafers. Hence, LT PureB photodiodes can be integrated together with electronic interface circuits and other sensors on a single chip. In this way, smart sensor systems or even CCD or CMOS UV imagers can be realized.

To better conclude the major achievements of this research work, progress and development overview of this PhD thesis is presented in Table 7.1.

Table 7.1: Progress and development overview of this PhD thesis

	Dec 2010	**Dec 2014**[a]
B-layer thickness uniformity	Thickness variation: ~ 35% [60]	Thickness variation < 10%
Uniformity of the responsivity	Responsivity variation: ~ 20% [53]	Responsivity variation < 5%
Stability (EUV / VUV / DUV)	Responsivity drop up to 5% [b] [22, 26]	Responsivity drop < 1% [c]
Undesired surface oxide amounts	~ 30% [d]	< 10% [d]
Post deposition thermal tolerance	Responsivity drop up to 30% [53]	Responsivity drop < 15%
Critical processing steps	2 critical steps [137]	No critical steps [131]
Dark current level	~ 50 pA[e] [138]	~ 20 pA[f] [131]
B-dep. temp. range	500 °C – 700 °C [44]	400 °C – 700 °C [131]
CMOS compatibility	Not compatible [44]	Fully compatible [131]

a. This PhD thesis
b. Mostly due to degradation of the B/Si interface as well as build-up of carbon on the exposed diode surface.
c. Due to build-up of carbon on the exposed diode surface (see Fig. 6.16 in Section 6.2)
d. Atomic percentage of oxide (intensity ratio of oxide/elemental Si) based on XPS results (Section 5.3)
e. At -1 V, (10×10) mm^2 pre-metal HT PureB photodiode (see Fig. 6.9a)
f. At -1 V, (10×10) mm^2 post-metal LT PureB photodiode (see Fig. 6.9b)

7.2 Recommendations for future work

In this thesis, a novel technology for low temperature (LT, 400 °C) boron deposition is developed. Besides the very promising and interesting results, this technology still demands further development to provide a uniform, smooth, closed LT boron layer at lower layer thicknesses.

The other option for future work is to employ plasma/UV-light enhanced CVD systems to reduce the deposition temperature by keeping the properties of the layer the same as conventional CVD layers.

Further investigation is needed to study the optical performances of the LT PureB photodiodes presented in Chapter 6 especially for EUV light.

Up to now there has been no convincing explanation for the formation of the ultrashallow p^+n junction with PureB technology. In previous works presented by F. Sarrubi [19] and M. Popadic [18] it is claimed that a delta-doping of silicon during boron deposition at 700 °C creates a p^+n junction. However it has been demonstrated in this thesis that devices with very similar performances, both electrical and optical, can be created by low temperature boron deposition at 400 °C. However the solid-state electronics denies the possibility that boron atoms can diffuse into silicon at such a low temperature, which makes doping impossible. Therefore more investigation is needed to fully understand the real mechanism behind the photo-generated charge collection mechanism and p^+n junction creation. The simulation results presented in Chapter 6 support the idea that a monolayer of holes at the boron-silicon interface can generate a very high electric field that repels the electrons from the interface, thus successfully fulfilling the photo generated charge separation role of a normal depletion zone between *p*-type and *n*-type silicon. Furthermore, such a structure demonstrates electrical characteristics of an excellent *p-n* junction.

In this research work it has been found that the resistivity of the boron semi-metal material can be varied by a different doping of the layer. This needs to be studied in more detail and can be used for those applications where the high resistance of the nm-thick boron layer is an issue.

The excellent physical and chemical stability of silicon carbide (SiC), its wide bandgap (from 2.2 to 3.2eV for different polytypes), superior thermal conductivity (3.5-5 $W.cm^{-1}.C^{-1}$ for different polytypes vs. 1.3 $W.cm^{-1}.C^{-1}$ for Si), high critical breakdown field (2 MV/cm vs. 0.3 MV/cm for Si), high carrier saturation velocity (200 mm/ns vs.100 mm/ns for Si), very low leakage current,

and outstanding performance, justify the interest in applying this semiconductor for radiation detection and spectroscopy such as neutron, alpha, beta, gamma, neutron, ultraviolet (UV) and X-ray detection. However, the doping of this material and creation of *pn* junctions are still challenging issues. The first attempts to deposit boron over a bare 4H-SiC wafer using the PureB technology appear to be very promising (see the results presented in Appendix D). It makes it interesting and worthwhile to further study the boron layer-based device structures on SiC substrate.

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Summary

Low Temperature PureB Technology for CMOS Compatible Photodetectors

by Vahid Mohammadi

In this thesis, conventional high temperature (HT, 700 °C) PureB technology is optimized in order to fabricate detectors with improved key parameters such as the spatial uniformity of the responsivity. A novel technology for low temperature (LT, 400 °C) boron deposition is developed providing a uniform, smooth, closed LT boron layer. This technology is successfully employed to create near-ideal LT PureB (pure boron) diodes with low, deep-junction-like saturation currents which make it possible to fully integrate LT PureB photodiodes together with electronic interface circuits and other sensors on a single chip. In this way, smart sensor systems or even CCD or CMOS UV imagers can be realized.

Chapter 1 presents the motivation and the objectives of the research work.

In Chapter 2, an overview of the conventional PureB CVD technology performed at 700 °C is presented. The state-of-the-art PureB Si-based detectors, with applications in the ultraviolet (UV) spectral range and also for low energy electron detection, are overviewed together with a brief performance comparison with the other commercially available devices. The superior electrical and optical performance of these devices is reviewed together with some drawbacks, limitations and imperfections, which are the points of improvement in this thesis. From the discussion in this chapter it can also be concluded that an improvement of the PureB technology is required for two aspects:

- First, regarding the optical performance, particularly the spatial non-uniformity of the response to low energy beams, the current conventional HT PureB technology needs to be optimized. Such non-uniformity is unacceptable, especially for applications demanding a uniform response over the entire active region, such as the aforementioned UV and electron detectors.

- Second, the current PureB technology is limited to the deposition temperature range from 500 °C to 800 °C, which makes this technology incompatible with standard CMOS processes.

In Chapter 3, surface reaction mechanisms are investigated to determine the activation energies of boron layer deposition at temperatures from 350 ºC to 850 ºC. For better understanding of the chamber parameters, the gas flow and the heat transfer in the ASM Epsilon 2000 CVD reactor are numerically simulated by using commercial CFD software. The results are employed to develop an analytical model to describe the deposition kinetics and the deposition chamber characteristics, which determine the deposition rate of boron layers over the wafer. This model is based on a wide range of input parameters, such as: initial diborane partial pressure, total gas flow, axial position on the wafer, deposition temperature, activation energy of the diborane deposition, surface H-coverage, and reactor dimensions. By only adjusting these reactor process parameters, this model is also successfully transferred from the ASM Epsilon One to the Epsilon 2000 reactor, which has completely different reactor conditions.

In Chapter 4, conventional boron deposition is optimized to provide uniform and reliable deposition of 2-nm-thick boron layers, with thickness variations of only a few angstroms. To solve the boron layer non-uniformity problem, in this chapter the pattern dependency and the loading effect are investigated and identified as sources of layer non-uniformity. Since these investigations need a thickness monitoring technique, the end-of-line resistance measurement is introduced as a nondestructive and accurate means of monitoring boron layer uniformity with fine resolution. The local loading effect of the boron deposition is investigated at the macro- and micro-scales. At the macro-sale, the investigation is limited to the influence of the LOR on the final boron layer thickness at the middle of the millimeter-large Si opening window, while the micro-scale investigates the uniformity profile of the deposited boron layer inside the opening with micrometer resolution. With the results of this investigation, valuable information is extracted about the diffusion length of boron atoms along silicon and boron surfaces in the deposition temperature range of 700°C to 400°C, which presents the maximum distance that boron atoms can travel along the surface before being deposited (as a layer) or

desorbed back to the main gas stream. Finally in this chapter, methods are proposed on the basis of the knowledge obtained in this thesis to control and minimize the pattern dependency and the loading effect during deposition by slightly modifying the process flow, adjusting some recipe parameters and changing wafer layouts or die design (if necessary). This was accomplished to such a degree that the 2-nm-thick boron layers used in present-day applications can be deposited uniformly with variations in thickness of only a few angstroms.

In Chapter 5, a novel technology for low temperature (LT, 400 °C) boron deposition is presented providing a uniform, smooth, closed LT boron layer. With this low processing temperature (400 °C), the boron layer can be deposited at the last stage of the fabrication flowchart when the metal layers and implanted regions are already defined on the wafer. The latter can be affected at 700 °C, but not by a deposition temperature of 400 °C. Therefore with this LT technology, we believe that the boron deposition is fully compatible with standard IC/CMOS processes for integrating LT PureB photodiodes together with CMOS electronic interface circuits and other sensors on a single chip. In this chapter, the temperature dependency is also discussed of the kinetics of boron deposition on patterned Si/SiO_2 surfaces in the temperature range from 700 °C to 400 °C.

In Chapter 6 it is demonstrated how the new knowledge presented in Chapters 3, 4 and 5 is employed to fabricate high performance PureB detectors particularly for low penetration photon/electron beam detection. First, Section 6.1 presents the fabrication process of high responsivity, high stability PureB photodiodes with a 2-3 nm-thick boron top layer using an optimized conventional (700 °C) boron deposition. Then, in Section 6.2, it is shown that the low temperature (LT, 400 °C) boron deposition performed after metallization can be used to create p^+n photodiodes with nm-thin boron layer windows and near-theoretical sensitivity for irradiation with either UV light or low energy electrons down to 200 eV, with negligible optical or electrical degradation, making the technology attractive for realizing smart sensor systems or even CCD or CMOS UV imagers.

In Chapter 7 the conclusions and the major contributions of this presented research work are presented and suggestions are made for future work and potential extensions.

Samenvatting

Lage temperatuur PureB technologie voor CMOS-compatibele fotodetectors

door Vahid Mohammadi

In dit proefschrift wordt de conventionele hoge temperatuur (HT, 700 ^{o}C) PureB technologie geoptimaliseerd teneinde detectoren te vervaardigen met verbeterde sleutelparameters zoals de ruimtelijke uniformiteit van de responsiviteit. Een vernieuwde technologie voor lage-temperatuur (LT, 400 ^{o}C) boriumdepositie is ontwikkeld die een gelijkmatige, gladde, gesloten LT boriumlaag oplevert. Deze technologie wordt met succes gebruikt voor het realiseren van bijna-ideale LT PureB (zuiver borium) diodes met lage, diepe-junctie-achtige verzadigingsstromen waardoor het mogelijk is om de LT PureB fotodiodes te integreren met elektronische interface schakelingen en andere sensoren op een enkele chip. Op deze wijze kunnen smart-sensor systemen of zelfs CCD- of CMOS-UV-imagers worden gerealiseerd.

Hoofdstuk 1 bevat de motivering en de doelstellingen van het onderzoek.

In Hoofdstuk 2 wordt een overzicht gegeven van de conventionele PureB CVD-technologie die bij 700 ^{o}C wordt uitgevoerd. De PureB detectoren op Si basis, volgens de stand van de huidige techniek, met toepassingen in het ultraviolette (UV) spetrale gebied entevens voor de detectie van lage-energie elektronen, worden geevalueerd in combinatie met een kort vergelijk met de prestaties van andere devices die op de markt zijn. De superieure elektrische en optische prestaties van deze detectoren worden besproken samen met enkele zwakke punten, beperkingen en onvolkomenheden, die de verbeterpunten in dit proefschrift zijn. Uit de discussie in dit hoofdstuk kan ook de conclusie worden getrokken dat een verbetering van de PureB technologie nodig is in twee opzichten:

- Ten eerste, ten aanzien van de optische prestaties, is het vooral nodig om de ruimtelijke niet-uniformiteit van de respons op lage-energie-bundels van de conventionele HT PureB technologie te optimaliseren.

Deze niet-uniformiteit is onaanvaardbaar, in het bijzonder voor toepassingen die een gelijkmatige respons vereisen over het gehele actieve gebied, zolas bij de eerder genoemde UV- en elektrondetectoren.
- Ten tweede, de huidige pureB technologie is beperkt tot depositietemperaturen in een gebied tussen 500 en 800 ^oC, waardoor deze technologie niet compatibel is met standaard CMOS processen.

In hoofdstuk 3 worden oppervlakte-reactiemechanismen onderzocht om de activeringsenergieën te bepalen voor depositie van boriumlagen bij temperaturen van 350 ^oC tot 850 ^oC. Voor beter begrip van de parameters van de depositiekamer worden de gasstroom en de warmteoverdracht in de ASM Epsilon 2000 CVD reactor numeriek gesimuleerd met commerciële CVD software. De resultaten worden gebruikt om een analytisch model te ontwikkelen voor het beschrijven van de depositiekinetiek en de karakteristieken van van de depositiekamer, die de depositiesnelheid voor boriumlagen over de wafer bepalen. Dit model is gebaseerd op een breed scala van inputparameters, zoals: initiële partiële druk van diboraan, totale gassnelheid, axiale positie op de wafer, depositietemperatuur, activatieënergie van de diboraandepositie, oppervlaktebedekking met H, en reactorafmetingen. Slechts door deze reactor-procesparameters op de juiste wijze in te stellen is dit model met succes overgebracht van de ASM Epsilon One naar de Epsilon 2000 reactor, die volledig andere reactorcondities kent.

In hoofdstuk 4 wordt de conventionele boriumdepositie geoptimaliseerd voor het verkrijgen van uniforme en betrouwbare depositie van 2-nm-dikke boriumlagen, met een diktevariatie van slechts een paar angstroms. Om het probleem van de niet-uniformiteit van de boriumlaag op te lossen worden, in dit hoofdstuk, de afhankelijkheid van het patroon en het beladingseffect onderzocht; deze werden geïdentificeerd als bronnen van niet-uniformiteit van de lagen. Aangezien voor deze onderzoeken een techniek nodig is om laagdiktes te bepalen, wordt de end-of-line weerstandsmeting geintroduceerd als een niet destructieve en nauwkeurige methode om de uniformiteit van de boriumlaag met hoge resolutie te bepalen. Het lokale beladingseffect van de boriumdepositie wordt onderzocht op macro- en microschaal. Op de macroschaal is het onderzoek beperkt tot de invloed van de LOR op de uiteindelijke laagdikte van het borium in het midden van het millimeter-grote

venster voor Si terwijl op microschaal het uniformiteitsprofiel van de gedeponeerde boriumlaag binnen de opening wordt onderzocht met micrometer resolutie. Met de resultaten van dit onderzoek wordt waardevolle informatie verkregen over de diffusielengte van boriumatomen langs silicium- en boriumoppervlakken in het gebied van depositietemperaturen tussen 700 ^{o}C en 400 ^{o}C, welke de maximale afstand bepaalt waarover boriumatomen langs het oppervlak kunnen bewegen voor ze worden geabsorbeerd (als laagje) of gedesorbeerd terug naar de hoofdstroom van het gas. Tenslotte worden in dit hoofdstuk, op basis van de kennis die in dit proefschrift is verkregen, voorstellen gedaan voor methoden om de patroonafhankelijkheid en het beladingseffect gedurende de depositie te controleren en te minimaliseren door kleine veranderingen in het proces zoals het aanpassen van enkele parameters van het recept en het veranderen van de layout op de wafer of (zonodig) het ontwerp van de die. Dit werd in zodanige mate gerealiseerd dat de 2 nm dikke boriumlagen die gebruikt worden in huidige toepassingen kunnen worden gedeponeerd met diktevariaties van slechts een paar angstrom.

In hoofdstuk 5 wordt een nieuwe technologie gepresenteerd voor lage temperatuur (LT, 400 ^{o}C) borium depositie, welke een unforme, gladde, gesloten LT-boriumlaag oplevert. Bij deze lage procestemperatuur (400 ^{o}C) kan de depositie van de boriumlaag plaatsvinden als de laatste stap van het fabricageschema als de metaallagen en de geïmplanteerde gebieden al zijn gedefinieerd op de wafer. De laatste kunnen worden aangetast bij 700 ^{o}C, maar niet bij een depositietemperatuur van 400 ^{o}C. Daarom geloven wij dat, met deze LT technologie, de boriumdepositie volledig compatibel is met standaard IC/CMOS processen teneinde LT PureB fotodiodes te integreren met CMOS elektronische interface schakelingen en andere sensoren op een enkele chip. In dit hoofdstuk wordt ook de temperatuurafhankelijkheid besproken van de kinetiek van boriumdepositie op van patronen voorziene Si/SiO_2 oppervlakken in het temperatuurgebied van 700°C tot 400 ^{o}C.

In hoofdstuk 6 wordt getoond hoe de nieuwe kennis die in hoofdstukken 3, 4 en 5 is besproken wordt toegepast bij de fabricage van high performance PureB detectoren, in het bijzonder voor detectie van lage-penetratie fotonen/elektronenbundels. Eerst wordt in sectie 6.1 het fabricageproces gepresenteerd voor hoge-responsiviteit, hoge-stabiliteit PureB fotodiodes met een toplaag van 2-3 nm dik borium, met behulp van een geoptimaliseerde

conventionele (700 ^{o}C) borium depositie. Daarna, in sectie 6.2, wordt getoond dat de lage-temperatuur (LT, 400 ^{o}C) boriumdepositie die wordt uitgevoerd na de metallisatie, gebruikt kan worden om p+n fotodiodes te realiseren met vensters uit een nm-dikke boriumlaag en een gevoeligheid die het theoretische maximum benadert voor bestraling met UV licht danwel laag-energetische elektronen tot aan 200 eV, met verwaarloosbare optische of elektrische degradatie, waardoor de technologie aantrekkelijk is voor het realiseren van smart-sensorsystemen of zelfs CCD of CMOS UV imagers.

In hoofdstuk 7 worden de conclusies en de voornaamste bijdragen van dit onderzoek gepresenteerd en worden suggesties gedaan voor toekomstig werk en potentiële voortzettingen.

Appendix

A. Ex-situ preparation procedure of wafers for boron deposition

As experimentally proven, the boron deposition is disturbed by any oxide: even a few atomic layers of native oxide, or any other particle contamination or residues on the surface [45]. Therefore, it is crucial to provide an oxide-free Si surface for the deposition. This is achieved by first treating the substrates by a standard *ex-situ* cleaning procedure (i.e. 10 min: HNO_3 100% at 25 °C; 5 min: DI water; 10 min: HNO_3 70% at 110 °C; or 5 min: DI water) immediately followed by a 4 min HF (0.55%) dip to remove native oxide and H-passivate the surface against native oxide formation. This was followed by Marangoni drying, which is an effective substitute for spin rinse drying to avoid formation of drying spots. These otherwise readily form on mixed hydrophilic-hydrophobic surfaces, resulting in particle contamination from residues left behind after evaporation [139]. After drying, the wafers were then directly loaded into the oxygen-free N_2-purged load locks of the reactor.

B. Basic PureB (photo)diode process flow

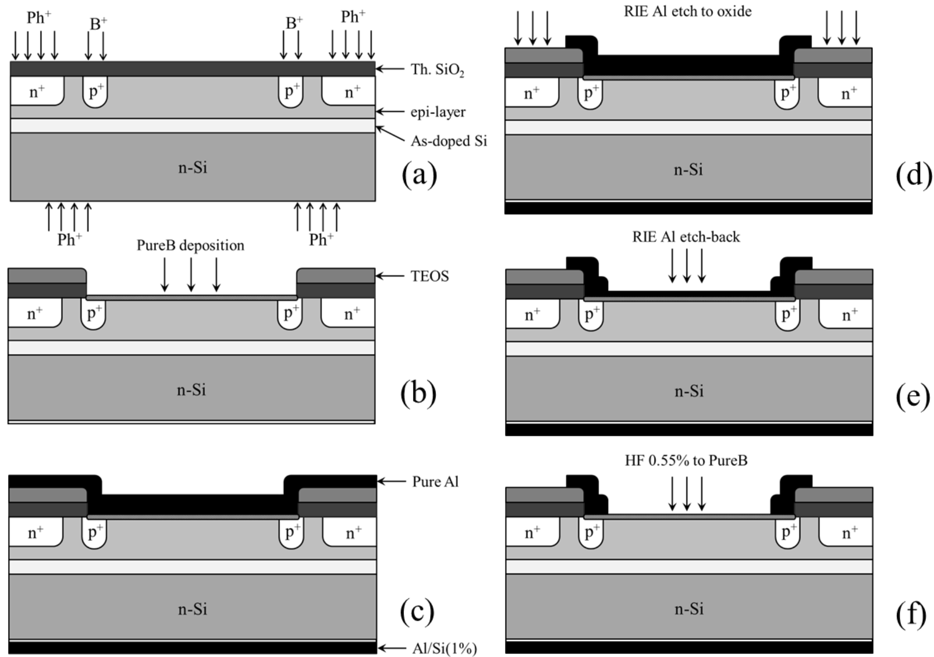
This appendix presents a basic process flow for fabrication of the PureB (photo)diodes in general as schematically described in Fig. APXB.1. It starts with n-type (100) wafers with a resistivity of 2-5 Ωcm. The substrates are prepared as follows: a 300-nm-thick As-doped Si layer, doped to 10^{16} cm^{-3}, is grown in the ASMI Epsilon One epitaxial reactor at 1050°C and 60 torr using arsine (AsH_3) as the dopant gas. This step is included depending on the design and the application. Immediately after this, the wafers are *in-situ* baked for 30 s at 1100°C in order to desorb the As atoms that have segregated on the layer surface. The epi-growth proceeds in cycles to achieve a total thickness of 10 μm to 40 μm depending on the application. Dihlorsilane (DCS) gas is used, and the doping of the layer in the range of 10^{12}-10^{13} cm^{-3} relies on the As segregation-incorporation dynamics from previously grown layers to supply doping. This As auto-doping process is described in more detail in [140]. The substrate preparation is completed with a dry thermal oxide passivation layer of about 240 nm thick. Through the thermal oxide, two guard rings are implanted. A p-type guard ring at the diode perimeter is formed by a B^+ implantation at 180 keV and an n-type guard ring separating neighboring diodes by a P^+ implantation at 300 keV. Ohmic contact to the back of the wafer is ensured by a blanket, high dose 150 keV P^+ implant (Fig. APXB.1a). These implantation energies can also vary with respect to the particular application and design.

After the sequence of implantations, an additional 400 nm of tetraethoxysilane (TEOS) is deposited by a low pressure chemical vapor deposition (LPCVD). The extra oxide is added in order to lower the contribution of the metal tracks to the device capacitance. The wafer is then annealed in inert gas for 35 min at 1000 °C.

Thereafter the boron layer anode formation is performed as shown in Fig. APXB.1b and described in detail in Section 2.2. It starts with a lithographical anode area definition, from which the oxide is etched away in a buffered HF (BHF) solution down to the Si. The wafers were *ex-situ* prepared for boron deposition as described in Appendix A. As an extra measure to assure an oxygen-free surface, *in-situ* cleaning is performed for the wafers destined for a HT boron deposition by baking in H_2 at 800 °C for 4 min [45] prior to the deposition of the boron layer for desired deposition conditions depending on the need.

A detailed description of the high temperature, HT 700 °C, boron deposition conditions is given in Section 2.2 and [45]. When the wafers are taken out of the epitaxial reactor, both the front and back sides of the wafer are coated with Al (Fig. APXB.1c). The metallization patterning directly on the boron surface is a crucial step for obtaining optimal efficiency and maximum performance as well as low series resistance (see Chapter 2). It is carried out in three steps: (i) first in Fig. APXB.1d the diode interconnect and diode contact are defined by dry etching the aluminum to the oxide; (ii) then in Fig. APXB.1e the anode region and/or Al-grid are designed on top of the boron surface (depending on the design and application) by reactive ion back-etching of aluminum down to a thickness of around 100 nm; and (iii) lastly in Fig. APXB.1f the wet etch to the boron layer removes the remaining Al. Both dry-etching steps are performed in HBr/Cl_2 etching chemistries and the etched Al thickness is time-controlled at the given RF power and temperature.

In the wet etching step, etched away reminded 100 nm of Al and landing on boron layer is finalized in a HF 0.55% solution that is highly selective to the nm-thin boron layer. This is the other crucial step mentioned in Chapter 2. For the last step the wafers are alloyed in forming gas for about 30 min at 400 °C.



- Epitaxy: as-doped Si – 300nm
- Epitaxy: low-doped epi – 40 µm
- Thermal oxidation – 240 nm
- Guard ring implantation – B^+
- p^+ implantation – Ph^+
- Backside contact p^+ implantation **(a)**
- LPCVD TEOS – 400 nm
- Annealing – 1000°C, 30 min
- Contact opening – BHF, HF + Marangoni
- Boron CVD deposition **(b)**
- Pure Al PVD deposition – front side: 1075 nm
- Al/Si(1%) PVD deposition – back side: 675 nm **(c)**
- Metal pattering by RIE – to oxide **(d)**
- Anode patterning etch-back by RIE – 900 nm **(e)**
- Anode wet landing to boron layer – HF 0.55% **(f)**
- Alloying - 400°C, 30min

Fig. APXB.1: Schematic process flow for the general fabrication of the PureB (photo)diodes.

C. Results of surface SIMS for Al contamination test

A test was done to prove that the epi-reactor will be safe for any metal contamination during post-metal LT boron depositions (Fig. 6.9b in Chapter 6). Three wafers were prepared as described in Table APXC.1, and the amount of Al contamination was detected using surface secondary ion mass spectroscopy (SIMS). These measurements were done at the laboratory of Evans Analytical Group® (EAG) in the USA. The results as presented in Table APXC.1 indicate that there was no detectable cross-Al contamination during processing of these wafers at 400°C.

Table APXC.1: Sample description.

Sample nr.	Sample description	Al level (atom/cm^2)
#1	Bare Si wafer directly from box (no treatment)	9.80×10^9
#2	Bare Si wafer annealed for 60 min at 400°C for background contamination test	8.02×10^9
#3	Bare wafer annealed together with metal wafer for 60 min at 400°C for cross-contamination test	7.53×10^9

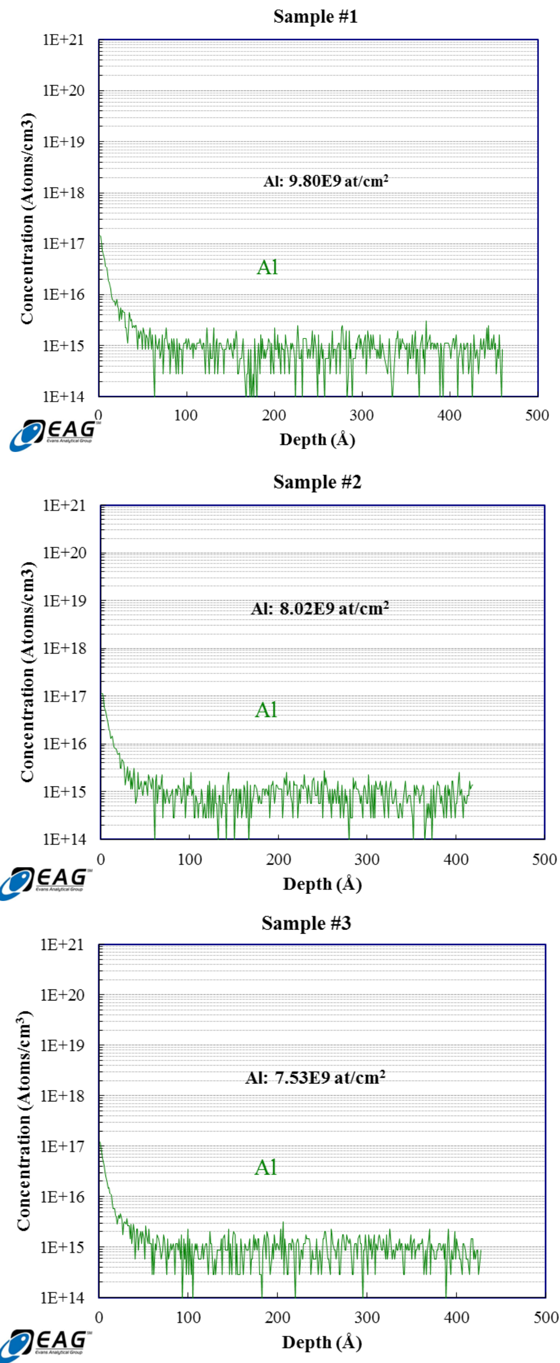


Fig. APXC.1: Results of surface SIMS for Al contamination test.

D. Boron deposition test on SiC substrate

To investigate the possibility of a boron layer deposition over a silicon carbide (SiC) substrate, the boron layer was deposited by PureB CVD technology at 700°C. Ellipsometry and PVMD transmittance measurements were employed to investigate whether the boron layer was deposited or not. Therefore three samples were examined; bare SiC-4H 4-inch wafer without any boron deposition, and wafers with boron depositions of 20 min and (20+30) min at 700 °C. PVMD transmittance and ellipsometry results are shown in Figs. APXD.1 and APXD.2, respectively. In these figures the results are compared with the results of a bare SiC wafer.

In Fig. APXD.1, a clear change in transmittance can be seen related to the different deposition times of 20 min and 50 min compared to the transmittance of the bare SiC wafer.

A clear change in the amplitude ratio, Ψ, and the phase difference, Δ, caused by interference between light reflecting from the surface and light traveling through the film, is detectable. This can be seen, for example, in Fig. APXD.2 for different deposition times and also different angles of accident of the light.

Therefore, so far, it is possible to conclude that the boron layer can be deposited over a SiC wafer with distinguishable differences regarding the deposition time.

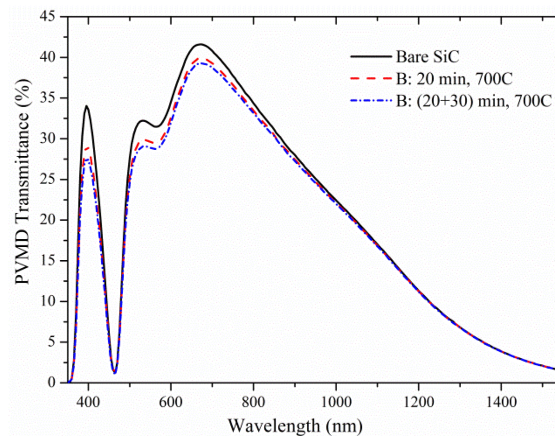


Fig. APXD.1: PVMD transmittance results.

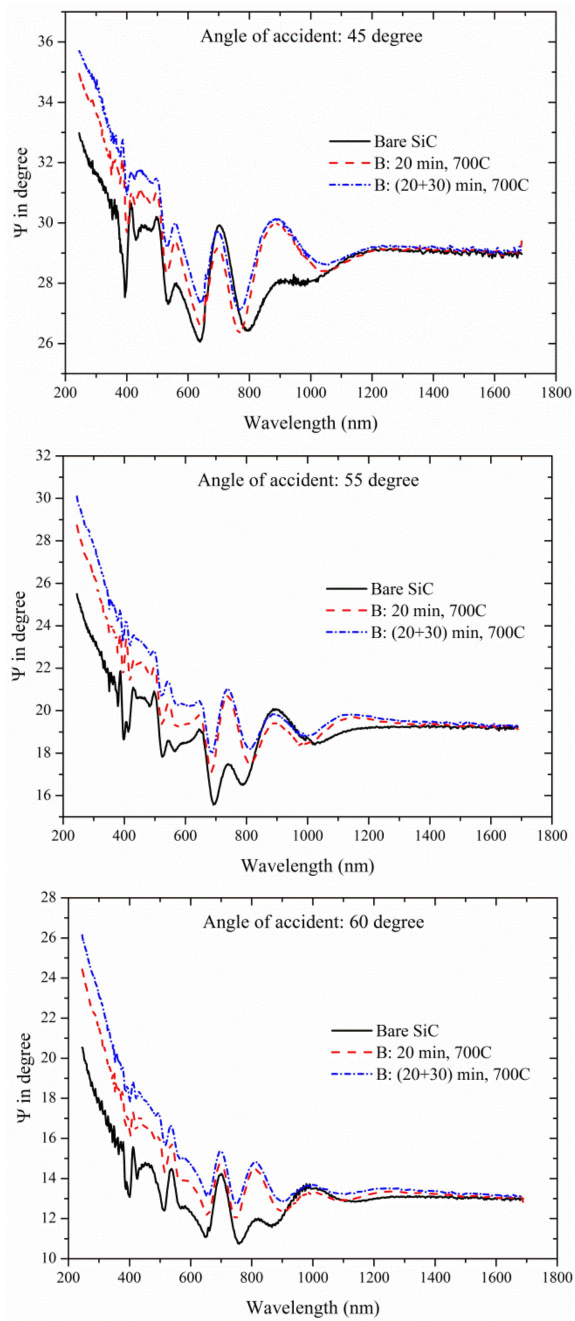


Fig. APXD.2: Ellipsometry results for different deposition times and also different angles of accident of the light.

E. Divisions of the UV spectral range

Table APXE.1: Divisions of the UV spectral range.

Sub-range[a]		**Wavelength range (nm)**
Near-UV	NUV	400 – 300
Middle-UV	MUV	300 – 200
Far-UV	FUV	200 – 100
Deep-UV	DUV	350 – 190
Vacuum-UV	VUV	200 – 10
Extreme-UV	EUV	100 – 10

a. These appear to be the most commonly used names and wavelength ranges, but other terminology can be found as well.

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List of symbols and abbreviations

List of symbols:

β	constant ~ 0.7
γ	constant ~ 0.7
θ	integration parameter
Γ	gamma function
γ	ratio of B sites to all surface sites
η	unitless constant
λ	wavelength
$\mu_0 T^{\gamma}$	temperature-dependent dynamic viscosity of the carrier gas
ρ_B	density of the deposited boron layer
ρ_{boron}	resistivity of the boron layer
ρ_g	density of the carrier gas
$\bar{C}_{L_{ox}}$	concentration of boron atoms accumulated over the oxide area at the edge of the Si opening
$\bar{C}_V$	concentration of boron atoms supplied by a vertical component
$\bar{C}(x)$	average concentration
C_L	lateral concentration of boron atoms
D_{BH_3}	diffusion coefficient of BH_3 in H_2
E_{BH_3-B}	unique activation energy for deposition of B on B
E_{BH_3-Si}	unique activation energy for deposition of B on Si
$P_S^{BH_3}$	BH_3 partial pressure at the surface
P_S^R	partial pressure of the reactant at the surface
f_{BH_3-on-B}	activated flux of BH_3 on a H-free B surface
$f_{BH_3-on-HB}$	activated flux of BH_3 on a H-terminated B surface
$f_{BH_3-on-HSi}$	activated flux of BH_3 on a H-terminated Si surface
$f_{BH_3-on-Si}$	activated flux of BH_3 on a H-free Si surface
m_{BH_3}	molecular mass of BH_3
$\vec{u}$	velocity vector
$\delta_{eff}(x)$	effective boundary layer thickness
$\theta_{H(B)}$	ratio of H-terminated B sites to all B sites
$\theta_{H(Si)}$	ratio of H-terminated Si sites to all Si sites
[B]	B concentration
b	width of the reactor
C	reactant concentration
C_0	initial reactant concentration
c_g	heat capacity of the carrier gas at a constant pressure
C_j	junction capacitance
D	diffusion coefficient of the active component in the carrier gas

E_A	deposition activation energy
f	activated flux of a precursor as the substrate
$F_m(x)$	mass flux
g	gravity force
G_{ph}	photon /electron signal gain
h	height of the reactor
I_{beam}	electron beam current
I_{dark}	photodiode dark current
I_{ph}	photo- /electron-induced current of the photodiode
k_b	Boltzmann constant
k_bT^{β}	temperature-dependent thermal conductivity of the carrier gas
L_B	diffusion length of boron atoms over Si/B surfaces
m	summation integer
M	mass of the boron atoms in the layer
m_R	mass of a reactant molecule
n	ideality factor of a diode
N_0	atomic density of the boron layer
N_R	number of reactant molecules in a unit volume of the gas phase
P	pressure
R_{boron}	resistance of the boron layer
Re	Reynolds number
R_s	series resistance
T	temperature
t	time
T_0	temperature of the inlet gases (room temperature)
T_s	temperature of the susceptor (deposition temperature)
T_w	temperature of the upper wall
u(y)	parabolic velocity profile of gases
u_0	initial gas velocity
W_{ox}	width of the oxide
W_{Si}	width of the opening windows
x	axial positions
y	vertical positions
μ	viscosity
ρ	density
$\delta(x)$	boundary layer thickness

List of chemical symbols:

Al	aluminum
Ai/Si(1%)	aluminum pre-saturated with silicon (percentage of silicon)
AlGaN	aluminum-gallium nitride
AlN	aluminum nitride
AsH_3	arsine
B	boron

B_2H_6	diborane
BHF	buffered HF
B_nH_m	boron hydride (borane)
B_xSi_y	boron silicide
Cl_2	chlorine
DCS	dihlorsilane
GaN	gallium nitride
Ge	germanium
H_B	H-free Si/B sites
H_Si	H-terminated Si/B sites
H_2	hydrogen
HBr	hydrogen bromide
HF	hydrofluoric acid
HNO_3	nitric acid
N_2	nitrogen
Si	silicon
SiC	silicon carbide
SiGe	silicon-germanium
SiH_4	silane
TEOS	tetraethylorthosilicate
TiSi	titanium silicide
TMAOH	tetramethylammonium hydroxide
Zr	zirconium
α-Si	amorphous silicon

List of abbreviations:

α–	amorphous
2D	two-dimensional
3D	three-dimensional
AFM	atomic force microscope
AN	annealing
AP	atmospheric pressure
ATM	atmospheric
BED	boron enhanced diffusion
BJT	bipolar junction transistor
BSE	backscattered electron
c-	crystalline
CBKR	cross-bridge Kelvin resistance
CBS	concentric backscattered
CCD	charge-coupled device
CDE	continuous dies to the edge wafer layout
CFD	computational fluid dynamics
CMOS	complementary metal oxide semiconductor
CO	contact openings, deposition windows

C-V	capacitance voltage
CVD	chemical vapor deposition
DIMES	Delft institute of microsystems and nanoelectronics
DR	depletion rate
DUV	deep ultraviolet
ECTM	electronic components, technology, and materials
EUV	extreme ultraviolet
eV	electron volt
FET	field effect transistor
FinFET	fin-shaped field effect transistor
FLP	Fermi level pinning
FUV	far-UV
FWHM	full width at half-maximum
GOR	global oxide ratio (area of SiO_2/wafer)
g-r	generation recombination
HBT	heterojunction bipolar transistors
HRTEM	high resolution TEM
HT	high temperature, 700 °C
IC	integrated circuit
I-V	current as a function of voltage
LA	laser annealing
LEEB	low energy electron beam
LOR	local oxide ratio (W_{ox}/W_{Si})
LPCVD	low pressure CVD
LT	low temperature, 400 °C
ML	monolayer
MOS	metal oxide semiconductor
MOSFET	metal oxide semiconductor field effect transistor
mtorr	millitorr
MUV	middle-UV
MΩ	megaohm
NUV	near-UV
OCR	oxide coverage ratio
pA	picoampere
PECVD	plasma-enhanced chemical vapor deposition
PTB	Physikalisch-Technische Bundesanstalt
PureB	pure boron
PVD	physical vapor deposition
PVMD	photovoltaic materials and devices
RF	radio frequency
RG	regular wafer layout
RIE	reactive ion etching
RM	remove margin wafer layout
rms	root-mean-square
RPCVD	reduced pressure CVD
rpm	rotation per minute

RTA	rapid thermal annealing
SB	Schottky barrier
sccm	standard cubic centimeters per minute
SEG	selective epitaxial growth
SEM	scanning electron microscopy
Sentaurus TCAD	advanced 1D and 2D semiconductor process simulator
SIMS	secondary ion mass spectroscopy
slm	standard liters per minute
SPE	solid-phase epitaxy
TED	transient-enhanced diffusion
TEM	transmission electron microscope
TEOS	tetraethyl orthosilicate
torr	1⁄760 of a standard atmosphere
TU Delft	Delft University of Technology
Taurus TSUPREM	advanced 1D and 2D semiconductor process simulator
UV	ultraviolet
vCD	low voltage high contrast detector
VUV	vacuum ultraviolet
XPS	X-ray photoelectron spectroscopy
μm	micrometer

List of publications

Journal papers

1. **V. Mohammadi**, N. Golshani, K. R. C. Mok, W. B. De Boer, J. Derakhshandeh, and L. K. Nanver, "Temperature dependency of the kinetics of PureB CVD deposition over patterned Si/SiO_2 surfaces," *Microelectronic Engineering*, vol. 125, pp. 45-50, 2014.
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2. **V. Mohammadi** and L. K. Nanver, "PureB photodetector technology research for application in detectors/imagers for the whole electromagnetic spectrum," presented at the *STW Annual Congress*, 3 Oct., Nieuwegein, The Netherlands, 2013.

3. **V. Mohammadi**, L. Shi, S. Nihtianov, and L. K. Nanver, "High performance PureB-photodiodes for DUV, VUV and EUV spectral ranges," presented at *The Sense of Contact 15*, 10 Apr., Kontakt der Kontinenten, Soesterberg, The Netherlands, 2013.

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About the Author

Vahid Mohammadi was born in 1981. He received his M.Sc. degrees in Electrical and Electronic Engineering from the University of Shiraz, Iran in 2009. During his M.Sc., he fabricated a piezoelectric MEMS pressure sensor based on an enhanced thin-film PZT diaphragm containing nanocrystalline powders. In December 2010, he joined the Faculty of Electrical Engineering, Mathematics and Computer Science (EEMCS), Laboratory of Electronic Components, Technology and Materials (ECTM) at Delft University of Technology, and Delft Institute of Microsystems and Nanoelectronics (DIMES), in the Silicon Device Integration group. His research focused on the characterization and control of the conventional 700°C pure-boron (PureB) CVD deposition and developing a novel 400°C pure-boron process integrated in CMOS compatible silicon detectors and imagers.

In December 2014 he joined the Department of Microelectronics at Delft University of Technology, Laboratory of the Electronic Instrumentation as a post-doc researcher.

Stellingen

Behorende bij het proefschrift

Low Temperature PureB Technology for CMOS Compatible Photodetectors

door

Vahid MOHAMMADI

Delft, 9 maart 2015

STELLINGEN

1- De lage-temperatuur (LT) depositie van borium bij 400 °C geeft de mogelijkheid om de PureB fotodiodes volledig te integreren met elektronische interface schakelingen en met andere sensoren op een enkele chip (*dit proefschrift*).

2- Zeer lage donkerstromen van de LT diodes doen vermoeden dat deze buitengewone eigenschappen verband houden met het specifieke interface dat door de B-atomen op het Si gevormd wordt tijdens de CVD depositie, eerder dan met dotering in de bulk (*dit proefschrift*).

3- Het "post-metal LT PureB" proces maakt het mogelijk om de twee kritische processtappen te vermijden die achteruitgang van het B-Si scheidingsvlak kunnen veroorzaken en kunnen leiden tot een ernstige toename van de spreiding in de donkerstroom, als gevolg waarvan de laagste donkerstroom voor PureB elementen bereikt kan worden die ooit is gemeten (*dit proefschrift*).

4- De mogelijkheid van het "post-metal PureB" proces om een specifiek B-Si scheidingsvlak te vormen maakt dit een goede kandidaat om het interface te passiveren en het maximum te bereiken voor de optische effectiviteit tot aan de theoretische grens, zelfs voor p^+n PureB fotodiodes (*dit proefschrift*).

5- De diffusielengte in de gasfase van borium atomen op Si/B oppervlakken is van de orde van enkele millimeters bij HT depositie maar wordt op dramatische wijze korter bij LT depositie (*dit proefschrift*).

6- Deadlines zijn medereizigers van een student tijdens zijn tocht naar de promotie, zonder hen is deze tocht niet mogelijk.

7- Naar het westen reizen brengt je niet noodzakelijkerwijs naar het westen.

8- Kennis is zich bewust zijn van wat uit onze monden komt.

9- Het leven is een lange enkele reis met een hop-on/hop-off bus.

10- Productiviteit wordt sterk beïnvloed door iemands vermogen zich te ontspannen.

Deze stellingen worden opponeerbaar en verdedigbaar geacht en zijn als zodanig goedgekeurd door de promotoren Prof. dr. ir. P. M. Sarro en Prof. dr. ir. A. J. P. Theuwissen.

PROPOSITIONS

1- Low-temperature (LT) boron deposition at 400 °C PureB photodiodes to be fully integrated with electronic interface circuits and other sensors on a single chip *(this thesis)*.

2- The very low dark currents of LT diodes suggest the idea that those extraordinary properties are related to the particular interface created by the B atoms on the Si during the CVD deposition rather than bulk doping *(this thesis)*.

3- The post-metal LT PureB process makes it possible to eliminate the two critical processing steps that can cause deterioration of the B-Si interface, while seriously decreasing the dark current spread and reaching the lowest ever measured dark current for PureB devices *(this thesis)*.

4- The ability of the post-metal PureB process to form a particular B-Si interface makes it a good candidate for passivating the interface and maximizing the optical performance up to the theoretical limits even for p^+n PureB-photodiodes *(this thesis)*.

5- The gas phase diffusion length of boron atoms over Si/B surfaces is in the order of few millimeters for HT depositions but drops dramatically for LT deposition *(this thesis)*.

6- Deadlines are fellow travelers of a student during the PhD journey; without them this journey is impossible.

7- Travelling to the west does not necessarily bring you to the west.

8- Knowledge is being aware of what comes out of our mouths.

9- Life is a long one-way journey with a Hop-on/Hop-off bus.

10- Productivity is highly affected by one's capability to relax.

These propositions are regarded as opposable and defendable, and have been approved as such by the supervisors Prof. dr. ir. P. M. Sarro and Prof. dr. ir. A. J. P. Theuwissen.