60GHz Quadrature Voltage-Controlled Oscillator for Radar Application

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Abstract

A voltage controlled oscillator (VCO) is an integral part of a phase lock loop (PLL) which by itself is the core of the frequency reference in a radar system. The generation of the in-phase and quadratue signals is crucial for many radar applications.

A 60GHz quadrature voltage controlled oscillator (QVCO) is presented in this thesis. The design is implemented in 130nm SiGe BiCMOS technology from STMicroelectronics with an f_T of 220GHz and f_{Max} of 320GHz. Two Colpitts oscillator cores are series coupled to each other to generate the required in-phase and quadrature signals.

The QVCO achieves a simulated tuning range from 53GHz to 59GHz with a tuning voltage from 0.5V to 2.3V. The phase noise is better than -76dBc/Hz at 1MHz offset from the carrier over the whole frequency tuning range. The total power consumption for the QVCO core is 28mW. The chip has been submitted for tape out in June 2010 and will be back for measurement in due time

Acknowledgement

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List of figures

List of tables

Table of contents

Chapter 1 Introduction

1.1 Background

With the quick development of IC technology, it is already possible to integrate the whole radar system on a single chip. A great variety of applications are envisioned for radar systems in the modern automobile industry. Automotive radar devices are now appearing on many luxury vehicles. By the use of a frequency modulated continuous wave (FMCW) radar system, one can measure the speed of the vehicle and the distance between the vehicle and the objects nearby for safety reasons.

1.2 FMCW basics

Frequency modulated continuous wave (FMCW) radar systems are well known and have been widely used in many applications. A block diagram of a FMCW radar system is shown in Fig. 1.1.

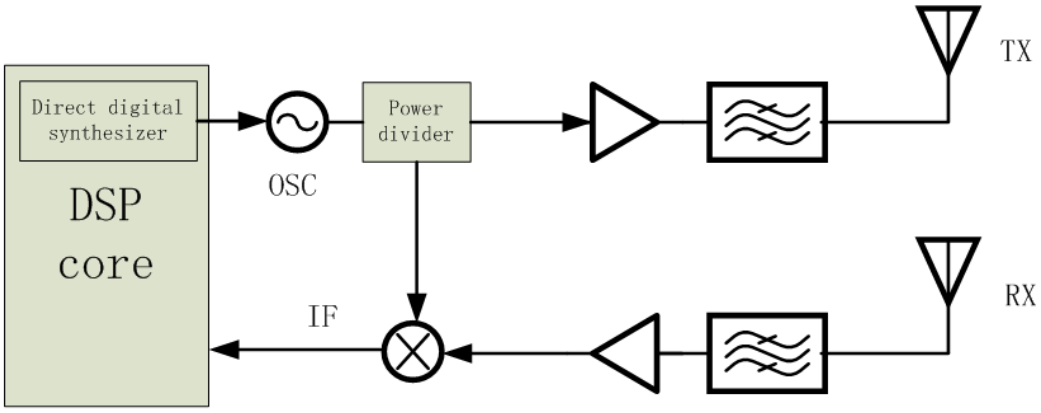

Fig. 1.1 FMCW radar block diagram

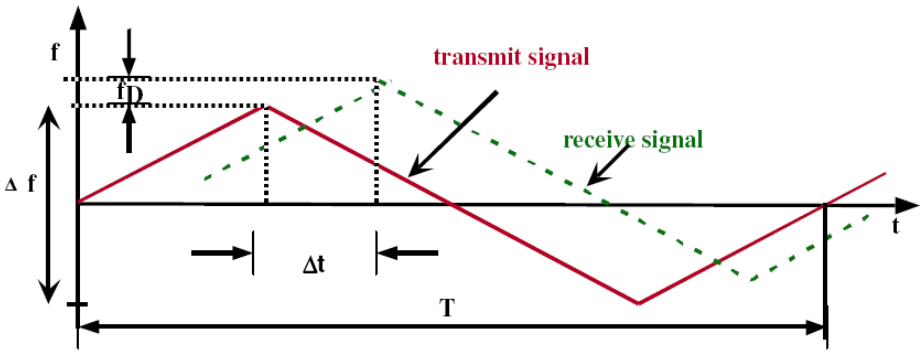

Fig. 1.2 Triangle wave FMCW modulation schemes

As the name itself suggests, the FMCW system adopts a continuous wave in the sense that the output signal is a continuous waveform and the frequency varies linearly with time, for example, a triangle wave as shown in Fig. 1.2.

As can be seen from Fig. 1.1, the frequency modulated wave from the oscillator is fed into a power divider and divided into two channels. One channel is sent to the mixer to be used as a reference signal at the receiver side. The other channel is amplified and sent to the transmitter. When the transmitted wave hits the target, it will bounce back and be detected by the receiver. The received signal will then be amplified and sent to the mixer to mix with the reference signal which is already available as a local oscillator source. By measuring the frequency difference between the transmitted signal and the reflected signal and considering the Doppler Effect, one can estimate the range and the speed of a certain target object[1].

In theory, the accuracy of the range measurement depends on the linearity of the frequency sweep. In a radar system, a voltage-controlled oscillator is needed to convert a time-varying voltage into a time-varying frequency. However, it is difficult to produce a high linearity stand-alone voltage-controlled oscillator. That's where the phase-locked loop (PLL) comes into play. A phase-locked loop together with a direct digital synthesizer can produce a highly linear ramp profile which alleviates the stringent requirement for the linearity of the VCO, thereby improving radar resolution. To handle modern modulation schemes, the separation of I and Q signals is needed to

fully recover the information. In the context of a direct-conversion system, accurate quadrature outputs are necessary. A complex demodulation receiver path is shown in Fig. 1.3.

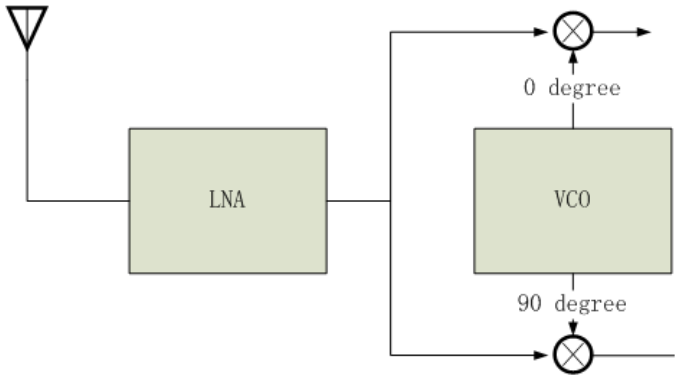

Fig. 1.3 Complex demodulation receiver path (I and Q signal)

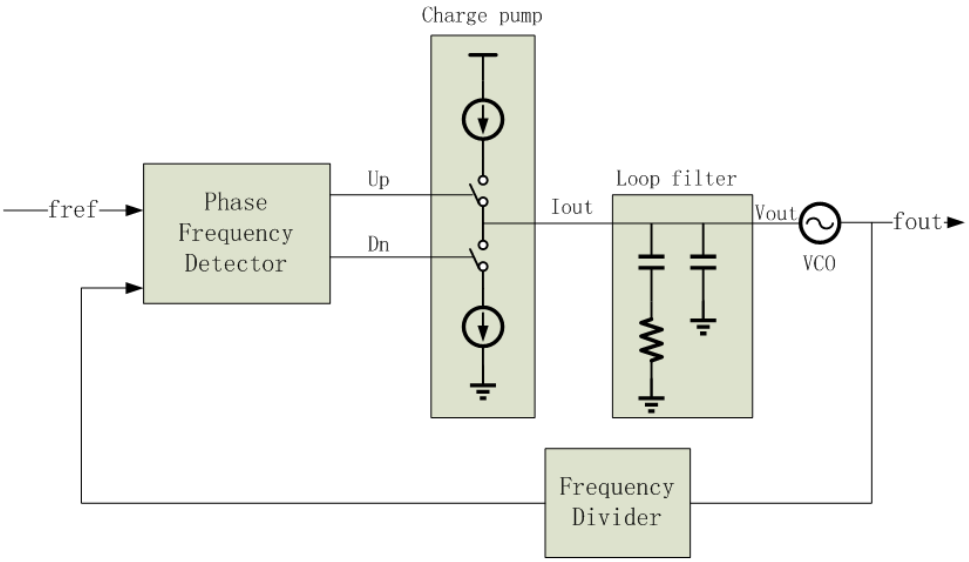

Fig. 1.4 Block diagram of a PLL system

Fig. 1.4 shows a block diagram of a PLL system. A phase frequency detector compares the two input signals. One is the input reference frequency which comes from a direct digital synthesizer and the other is a divided version of the VCO output. The phase frequency detector generates voltage pulses proportional to the phase difference between the two inputs. The Up and Dn pulses are then fed into a charge

pump which converts the pulses into current. The current I_{out} is then converted to a voltage V_{out} by a loop filter. This voltage acts as the tuning voltage for the VCO. The output frequency of the VCO is fed through a frequency divider back to the input of the system, completing a negative feedback loop. If there is any drift frequency in the output frequency, the error signal will vary accordingly, thereby driving the VCO frequency in the opposite direction in order to reduce the error. Thus the output is locked to the same frequency as the other input with a small constant phase offset.

This project aims at the realization of a 60GHz quadrature voltage-controlled oscillator (QVCO) in a 130nm SiGe BiCMOS technology by STMicroelectronics with a f_T of 220GHz and f_{Max} of 320GHz. The targeted tuning range is 10%, covering a whole band of 6GHz. The phase noise performance of the QVCO is not critical since noise of the PLL's frequency reference will determine the noise close to the carrier. However, we still would like to keep it at an acceptable level, say -80dBc/Hz at 1MHz offset from the carrier frequency.

1.3 Report organization

Chapter 2 reviews general VCO topologies. Several different approaches to generate quadrature signals are also investigated. Chapter 3 discusses the design approaches in more details, showing how the circuit evolves from its prototype to the proposed topology and the trade-offs that have been made during the design procedure. Chapter 4 gives an overview for the physical layout of the whole circuit and introduces the peripheral circuits needed for test and measurement purpose, including the intermediate frequency I/Q mixer, the differential filter and the differential to single-ended converter. Chapter 5 gives a summary and comparison with literature results. Future work is also explained.

Chapter 2 Voltage-Controlled Oscillator Review

2.1 General theory

In principal, an oscillator can be viewed as a positive feedback system. The block diagram is shown in Fig. 2.1.

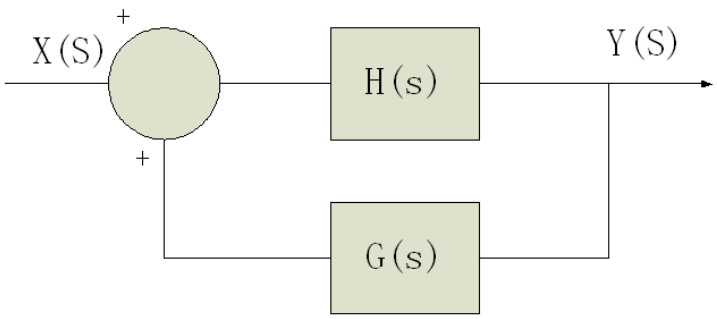

Fig. 2.1 Negative feedback system

The transfer function of the whole system is given by:

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1-H(s)*G(s)} \tag{2.1}$$

For steady oscillation to occur, the Barkhausen's criteria must be simultaneously met:

$$H(s) * G(s) = 1 \tag{2.2}$$

$$\angle H(s) + \angle G(s) = 2n\pi \tag{2.3}$$

The loop gain of the system is given by:

$$LG(s) = H(s) * G(s) \tag{2.4}$$

Oscillation occurs when the loop gain is equal to unity. The oscillator frequency is given by:

$$Im(LG(s))=0 \tag{2.5}$$

2.2 Categories of VCOs

By the nature of the resonator type, oscillators can be divided into two categories: resonator-less oscillator and resonator oscillator.

2.2.1 Resonator-less oscillator

The resonator-less oscillators can be further categorized into ring oscillator and relaxation oscillator.

2.2.1.1 Ring oscillator

A ring oscillator usually consists of an odd number of gain stages, each being an inverting amplifier for example. The oscillation frequency is inversely proportional to the sum of the total propagation delay of the whole inverting amplifier chain. By controlling the current and/or the power supply of each stage, the propagation delay can be tuned; therefore the output frequency can be controlled.

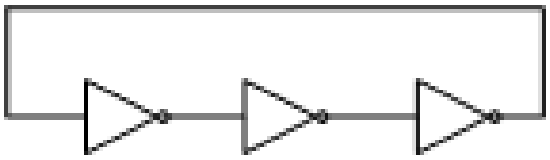

Fig. 2.2 A 3-stage ring oscillator

Basically, the oscillation frequency can be very high since it is related to the propagation delay of the inverting stage, which can be made rather small and decrease with improvements in technology. However, the major drawback of the ring oscillator is the poor phase noise performance and time jitter. A ring VCO does not store energy during each clock cycle. The node capacitances are charged and discharged within the same cycle. The noisy transistors therefore have to stay active for a relatively long time to replenish the energy lost and inject more noise into the circuits. In addition, this process takes place at the clock edges when the circuits are most sensitive to noise perturbation. Phase noise is a strong function of the number of stages.[2]

2.2.1.2 Relaxation oscillator

A relaxation oscillator is an oscillator based upon the behavior of a physical system's return to equilibrium after being perturbed. A dynamical system within the oscillator continuously dissipates its internal energy which needs to be sustained. The oscillation frequency is determined by the circuit RC time constants.

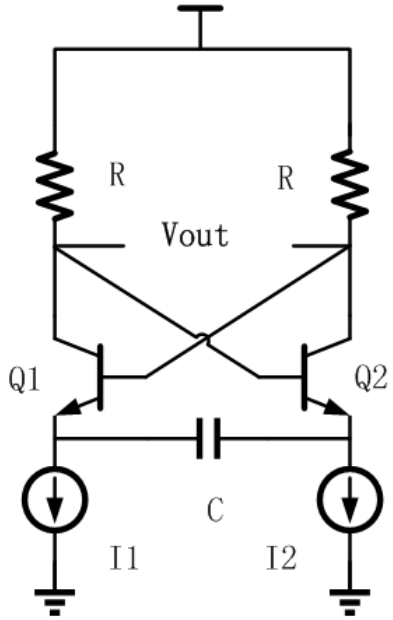

Fig. 2.3 Relaxation oscillator

As depicted in Fig. 2.3, the oscillator alternately charges or discharges the capacitor with a constant current. The oscillation frequency is inversely proportional to the product of the resistor R and the capacitor C. The oscillation is sustained by the positive feedback of the cross-coupled pair. By varying the current I_1 and I_2 through the transistors Q_1 and Q_2, we can have a control over the output frequency.

A relaxation VCO can have a high oscillation frequency and a wide tuning range. However, the poor frequency stability at high frequencies and mediocre phase noise performance limits its application.

2.2.2 Resonator Oscillator

The resonator oscillator, as its name suggests, has a resonating tank which uses passive components as inductors and capacitors to determine the oscillation frequency. An LC-VCO oscillates at the frequency given by the inductor L and the capacitor C:

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{2.6}$$

We can consider the oscillator model in the way of negative resistance compensation. The oscillator can be viewed as consisting of two parts: the active circuit and the resonator.

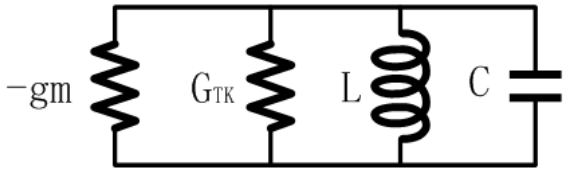

Fig. 2.4 Negative resistance model

Due to the relatively low quality factor of the passive components, the resonator part always has finite resistive losses which can be modeled by the tank conductance G_{TK}. The active part is therefore needed to behave as a negative conductance to compensate the loss from the tank in order to sustain the oscillation.

The oscillation condition is given by:

$$|g_m| > G_{TK} \tag{2.7}$$

In practical circuit realization, a cross-coupled pair is usually adopted to realize this negative conductance due to its ease of design and implementation as illustrated in Fig. 2.5. A more negative conductance is always desired to ensure a safer start-up condition.

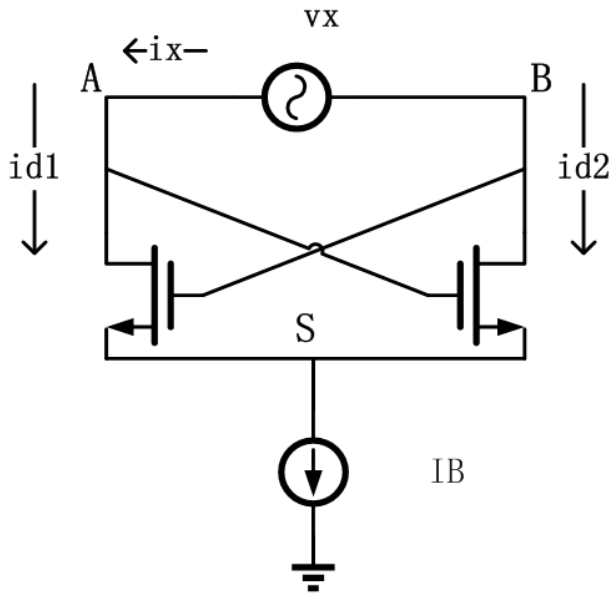

Fig. 2.5 Cross coupled pair to generate negative conductance

Consider the equivalent conductance of the cross coupled pair in Fig. 2.5. Let's assume we insert a voltage source V_x between node A and node B. By calculating the induced I_x, we can therefore calculate the equivalent conductance. As can be shown from the above circuit, the following equations are valid:

$$G_x = \frac{I_x}{V_x} = \frac{I_x}{V_A - V_B} \tag{2.8}$$

$$I_x = I_{d1} = -I_{d2} \tag{2.9}$$

$$I_{d1} = g_{m1} V_{GS1} = g_{m1}(V_B - V_S) \tag{2.10}$$

$$I_{d2} = g_{m2} V_{GS2} = g_{m2}(V_A - V_S) \tag{2.11}$$

For simplicity, the non-ideal terms are not present in the equation. However, at very high frequencies, the device capacitance and input resistance should also be included in the analysis. Rearranging the equations and assume the two transistors are identical which means $g_{m1} = g_{m2} = g_m$, we can get

$$G_x = -\frac{g_m}{2} \tag{2.12}$$

in which g_m represents the effective conductance of the transistor. For small amplitudes, the magnitude of the loop gain is greater than one and the oscillation grows. Let's take a look at the plot of effective transconductance versus input amplitude in Fig. 2.6. The effective transconductance is defined as the ratio between the fundamental harmonic of the output current and the peak amplitude A_0 of the harmonic voltage at the transconductor input (node A and node B). We can see that with the increase of the input amplitude, which is also the oscillation amplitude seen at the output of the transistors, the effective transconductance decreases. This mechanism will ensure the equilibrium of the output amplitude so that with the increase of the amplitude, the effective gain decreases and stabilizes at just the right amplitude to give an effective loop gain of unity. This can also be explained by means of closed loop root locus as g_m changes.

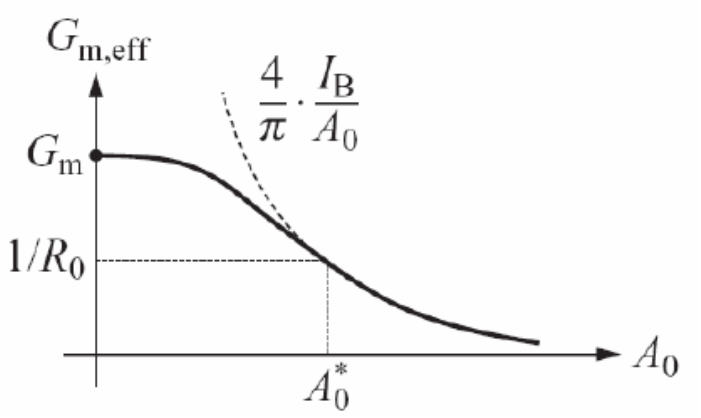

Fig. 2.6 Effective transconductance versus input amplitude

The passive components inevitably have some losses. Therefore the quality factor, which is defined as the ratio of the product of 2π and the energy stored in the tank to the energy dissipated per cycle, is always finite. In modern SiGe technology, the quality factor of a varactor is on the range of 5 or even less, which poses a great challenge on the design of the active part to compensate the dissipation due to the low quality factor. In principal, the higher the quality factor is, the easier the start-up condition is and the better the filtering and the phase noise performance is. This is due

to the fact that the low loss of the energy stored in the tank needs a short charging time by the active device during per clock cycle. According to Hajimiri's phase noise theory[3], the duration of the time when noised is injected directly has an impact on the phase noise. Therefore a high quality factor passive component also helps to improve the phase noise performance. The spiral inductors also have limited performance at 60 GHz due to substrate eddy currents. In addition the inductor values will also be influenced by the magnetic coupling to the substrate[4]. At frequency lower than 10GHz, the quality factor of the LC tank is limited by the inductor, but it's not the case at millimeter-wave frequencies since the Q of capacitors ($Q_C \sim {}^{1}/_{\omega R_s C}$) decreases with frequency while that of inductor ($Q_L \sim {}^{\omega L_s}/_{R_s}$) increase with frequency[5].

As the name itself suggests, the output frequency of the voltage-controlled oscillator should be voltage dependent. Tuning is achieved by the adoption of varactor. By tuning the voltage across the varactor, one can change the varactor's capacitance thus control the output frequency. In order to achieve a high oscillation frequency, a small value varactor would be desired. Meanwhile, the minimum varactor value and maximum varactor value also set the tuning range of the whole VCO.

$$\frac{f_{max}}{f_{min}} = \sqrt{\frac{\frac{C_{v,max}}{C_{v,min}} + 2\frac{C_{par}}{C_{v,min}}}{1 + 2\frac{C_{par}}{C_{v,min}}}} = \sqrt{\frac{C_{v,max} + 2C_{par}}{C_{v,min} + 2C_{par}}} \qquad (2.13)$$

f_{max}, f_{min} are the maximum and minimum oscillation frequency respectively, $C_{v,max}$, $C_{v,min}$ are the maximum and minimum capacitance of the varactor, C_{par} is the parasitic capacitance. In order to extend the tuning range of the VCO, a large ratio of $C_{v,max}$ over $C_{v,min}$ would be desired. However, there is always a limit to that due to technology limitations. To use an array of switched capacitors controlled digitally might seem to be a good approach. Different ranges of capacitors are switched to be connected to the tank or not according to the required tuning range so that a

coarse-tuning and fine-tuning mechanism is achieved. In addition, this method can get rid of the varactors which have extremely low quality factor at high frequency. However there are some disadvantages with this tuning mechanism. Details will be discussed in Chapter 3.

Table 2.1 Comparison of different types of oscillators

		Advantages	Disadvantages
Resonator Oscillator	LC Osc.	Good phase noise performance	Poor quadrature accuracy
Resonatorless Oscillator	Ring Osc.	Good quadrature accuracy	Poor phase noise performance
	Relaxation	Good quadrature accuracy	Poor phase noise performance

As can be seen from Table 2.1 and previous discussion, all the VCO categories can attain a relatively high frequency. LC-VCO has a good phase noise which is desired in the modern telecommunication applications, yet it has a limited tuning range. However, by careful design, a 10% tuning range can still be achieved which is sufficiently enough for this application. The details about the design of the LC-QVCO will be discussed in Chapter 3.

2.3 Quadrature signal generation

We have addressed the importance of generating in-phase and quadrature signal in the previous sections. There are mainly three ways to generate in-phase and quadrature signals (I and Q signals), by the use of frequency dividers, poly-phase filters, or by means of coupling two identical VCO cores together.

2.3.1 Frequency dividers

Probably the most straightforward way is to use the frequency dividers. The idea is to generate twice as high frequency as the desired signal and feed them into a

frequency divide-by-two circuit using a single master/slave flip-flop. A current mode logic divider can be used to achieve high speeds, but they consume a substantial amount of power which makes them less favorable. In addition, to generate double the targeted frequency is already difficult by itself due to limitations of the technology. Moreover, the random process mismatches and errors will result in significant degradation in phase noise performance.

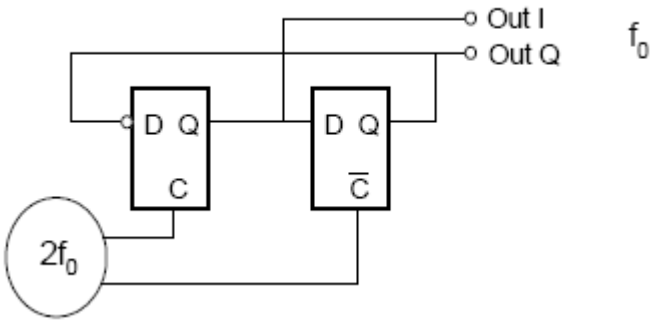

Fig. 2.7 Master-slave latch to generate I and Q output

2.3.2 Poly phase filters

A polyphase filter is another popular approach to generate in-phase and quadrature signals[6]. The VCO drives the polyphase filter which usually consists of several stages of individual filters. The polyphase filter is a symmetric RC network therefore it has bandwidth and gain limitations. The polyphase filter only operates at a frequency which is determined by the RC constant. If the input signal falls out of the bandwidth, the rejection is weaker. Therefore, a cascade of multi-stage filters is needed if high image rejection through a wide band is desired. However, the RC networks will always have some losses. The more cascaded stages, the more attenuation it will introduce. In addition, the RC network usually ends up with suffering from distributed capacitance to the substrate[6].

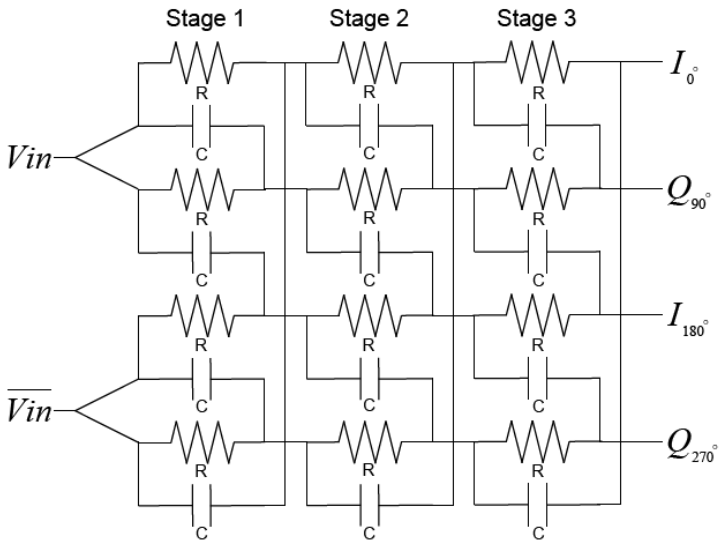

Fig. 2.8 A 3-stage polyphase filter

In order to minimize the loading effect of the polyphase filters on the VCO output, buffers are used between the VCO output and the polyphase filters input. The buffers themselves consume additional power. Moreover, some additional circuitry is needed to amplify the output signal from the polyphase filters since they are attenuated after several passive RC stages.

2.3.3 Coupled VCOs

Coupled VCO can also generate in-phase and quadrature signal output[7].

Two identical differential VCO cores are coupled in such a manner that the output of one VCO (let's denote it as I-VCO) is connected in common phase to the other VCO (let's denote it as Q-VCO) whereas the output of the Q-VCO is fed back to the I-VCO in anti-phase. This configuration works in the way that the two VCOs are synchronized in such a way that their differential output signals differ by 90 degrees.

It can be understood by means of loop analysis. As stated previously, the two VCO cores are coupled to each other to form a closed loop. By connecting one I-VCO output in phase with the Q-VCO and the Q-VCO output anti-phase with the I-VCO, a 180 degree phase shift is expected within the whole loop. If we can make sure that the two VCO cores are identical, a 90 degree phase shift is consequently acheived between the outputs of the two VCO cores.

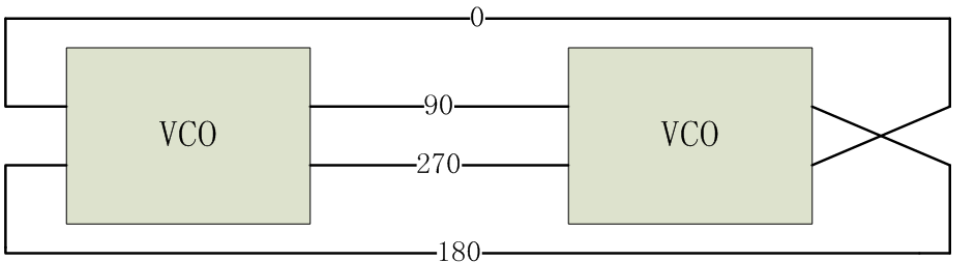

Fig. 2.9 Block diagram of the coupled VCO topology

Coupled QVCO needs 2 identical VCO cores so that the power consumption and the area needed are also doubled. However, with careful design, one can still achieve a coupled QVCO which consumes less power than the polyphase filter version. This is the topology that is adopted in this design.

There are several ways to couple the two VCO cores, namely parallel coupling, series coupling, back gate coupling and transformer coupling. The difference lies mainly in the way how the coupling is achieved.

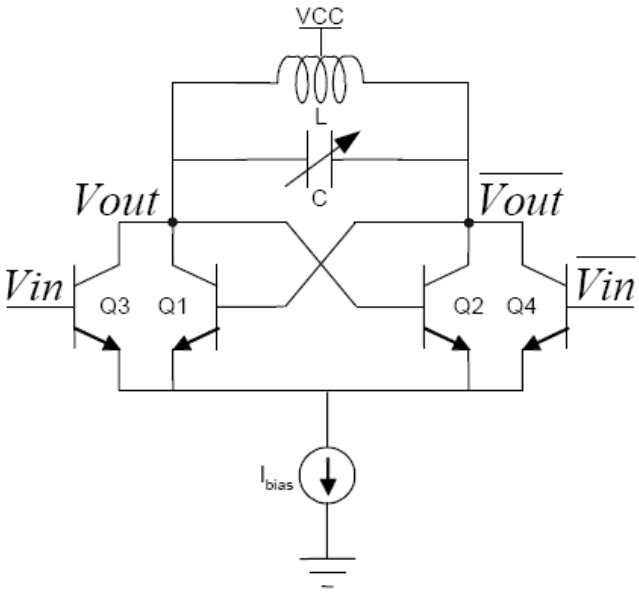

Fig. 2.10 Parallel coupled VCO

As can be seen from Fig. 2.10, the coupling transistors Q3, Q4 are in parallel with the switching transistors Q1, Q2[8]. The amount of coupling between the two VCO cores can be tuned by the size of the coupling transistors. There is a trade-off between the phase noise and the quadrature accuracy for this coupling mechanism. To circumvent this problem, another method using series coupling is suggested.

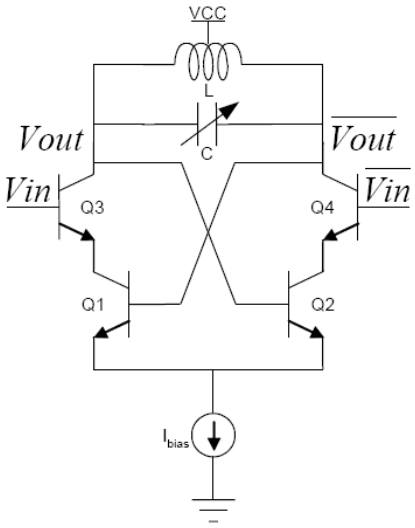

Fig. 2.11 Series coupled VCO

As can be seen from Fig. 2.11, the coupling transistors are connected in series with the switching transistors. The motivation behind is to reduce the noise caused by the coupling transistors, which contribute a great part for the overall phase noise. By connecting it in series with the switching transistors, in a cascode-like way, one can greatly reduce the noise from the cascoded device [9, 10]. In this design, there are some more modifications that are made for better performance; that's going to be discussed in more detail in the Chapter 3.

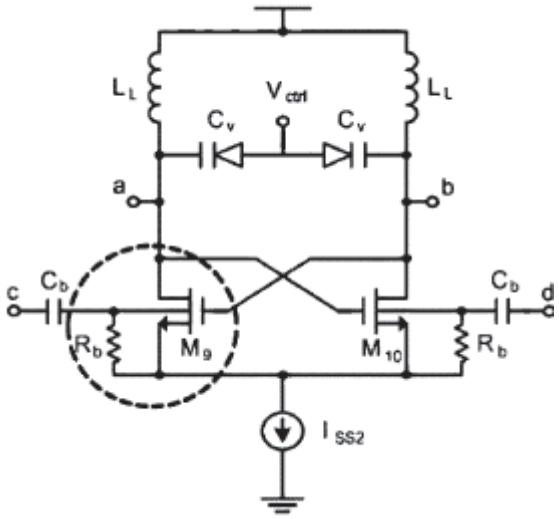

Fig. 2.12 Back-gate coupled VCO [6]

Another method is to use the back-gate coupling if the technology provides isolated NMOS transistors, e.g. triple well. As the name itself suggest, the coupling transistors are connected to the back gate of the switching transistors.[11]

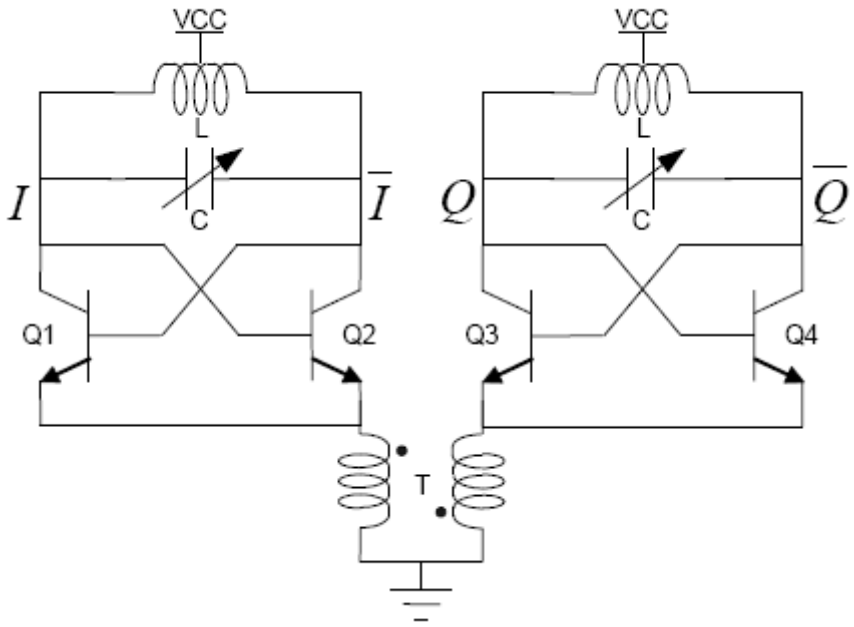

Fig. 2.13 Transformer-coupled VCOs

As stated before, what we need is a 180 degree shift within the loop. Therefore, a transformer coupling mechanism is naturally a candidate since it does not add additional power consumption and will not introduce noise sources. However, the silicon area needed for a high coupling coefficient transformer is usually significant and too many inductive components in a confined area may introduce significant magnetic coupling between them and will eventually worsen the phase noise.

Chapter 3 Design Approach

In this chapter, a detailed discussion about the topology of the VCO will be presented as well as the proposed modifications for better performance. A detailed evolution of the circuit topology from the conventional single-ended Colpitts VCO to the modified differential Colpitts Quadrature VCO is also demonstrated. Various design considerations and trade-offs are discussed.

3.1 Colpitts oscillator core

The Colpitts oscillator is a favored candidate for a LC-VCO due to its good phase noise performances. This is due to the fact that the noise current from the active devices is injected into the tank when the impulse sensitivity is low[12]. Fig. 3.1 depicts a simple single-ended version of a Colpitts VCO core. It is a resonator tank with an active device which compensates the loss due to the passive components and ensures the loop gain is sufficient to sustain the oscillation. The resistance R in Fig. 3.1 represents the loss due to the finite quality factor of the passive components (inductors and capacitors) in the resonating tank. Note that C_1 and C_2 also have parasitic resistance which should also be taken into account when calculating the equivalent tank losses.

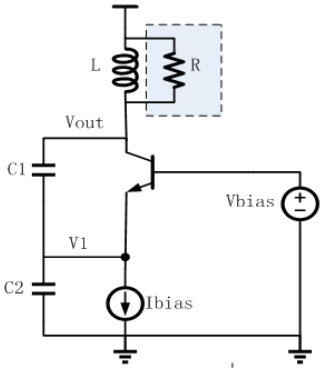

Fig. 3.1 Single-ended Colpitts VCO core

To understand the principle of the Colpitts oscillator, let's first calculate the small-signal admittance looking into the collector of the transistor. The small-signal model of the active part is shown in Fig 3.2.

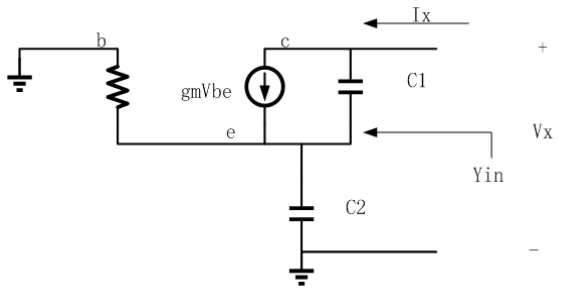

Fig. 3.2.1 Small signal model of the active part (without C_{be} and C_{bc})

From Fig. 3.2.1 we can write:

$$I_x = g_m V_{be} + j\omega C_1 (V_x - V_e) \tag{3.1}$$

$$V_e = \frac{1}{j\omega C_2}(I_x + i_b) \tag{3.2}$$

For simplicity, the dynamic elements of the transistor are ignored. By arranging the above equations, we can therefore calculate the admittance seen from the collector of the transistor to ground.

$$Y_{in} = \frac{I_x}{V_x} = -\frac{\omega^2 C_1 C_2}{g_m + j\omega(C_1 + C_2)} \tag{3.3.1}$$

The real part of the admittance is needed to compensate for the loss in the resonating tank and sustain the oscillation. The available admittance is directly related to the two capacitors C_1, C_2 and g_m of the transistor.

$$\mathrm{Re}(Y_{in}) = -\frac{g_m \omega^2 C_1 C_2}{g_m^2 + \omega^2 (C_1 + C_2)^2} \tag{3.4.1}$$

Now let's also consider the dynamic elements C_{be} and C_{bc} as shown in Fig. 3.2.2(a). Since the base of the transistor is biased at a fixed voltage, it's AC shorted to ground. Therefore, we can safely fold the C_{be} and R_{be} to the bottom to be in

parallel with C_2 as shown in Fig. 3.2.2(b) and C_{bc} to the right to be in parallel with the Y_{in} calculated in equation 3.3.1. The admittance seen from the collector of the transistor to ground in this case can be written as:

$$Y_{in}^{'} = \frac{I_x}{V_x} = -\frac{\omega^2 C_1 C_2}{g_m + j\omega(C_1+C_2+C_{be}) + {}^{1}/_{R_b}} + j\omega C_{bc} \tag{3.3.2}$$

$$Re(Y_{in}^{'}) = -\frac{\left(g_m + \frac{1}{R_b}\right)\omega^2 C_1 (C_2+C_{be})}{\left(g_m + \frac{1}{R_b}\right)^2 + \omega^2 (C_1+C_2+C_{be})^2} \tag{3.4.2}$$

As can be seen from the above analysis, C_{bc} won't influence the negative admittance and C_{be} has a minor influence since it is in parallel with C_2 but much smaller. A typical ratio of ${C_1}/{C_2}$ ranging from 2 to 4 gives the best phase noise performance[13].

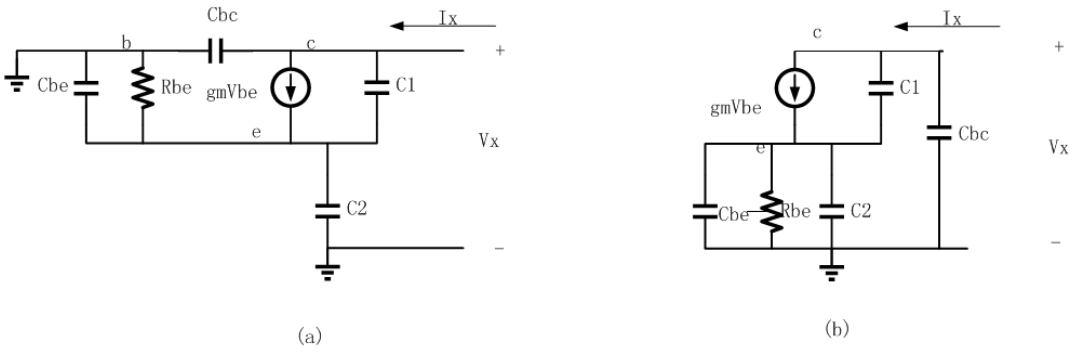

Fig. 3.2.2 Small signal model of the active part (with C_{be} and C_{bc})

3.2 Derivatives of the Colpitts oscillator

Now that we have the single-ended version of the Colpitts VCO, the next step is to make it differential for the sake of rejecting common-mode ground noise. The most straightforward way is to make a completely identical copy of the single-ended Colpitts VCO and combine the two inductors into a center-tapped inductor of which

the primary and secondary coils are connected to the two single-ended Colpitts VCO outputs respectively so that a differential output is ensured. In order to achieve a voltage tuning mechanism, varactors are also introduced in the tank to adjust the equivalent capacitances seen at the tank.

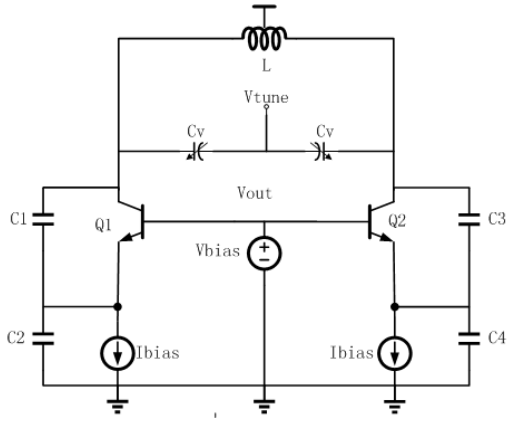

Fig. 3.3 Differential Colpitts VCO core

As shown in Fig. 3.3, the base of the transistor pair is biased by a fixed voltage V_{bias}. The next modification is to change the way of biasing. The two transistors are going to be connected in a “cross-coupled” manner as shown in Fig. 3.4, i.e., the base of Q1 is connected to the collector of Q2 and the base of Q2 is connected to the collector of Q1.

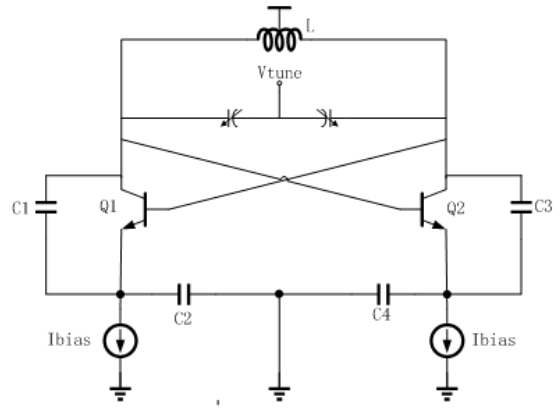

Fig. 3.4 Modification of the conventional differential Colpitts VCO

There are several advantages that go along with this configuration. First of all, the fixed voltage source for biasing is no longer needed. One can get rid of the blocking capacitors and biasing resistors which are otherwise needed in the conventional configuration. The cross-coupled pair can also be viewed as a “self-biased” pair in the sense that the biasing of the transistor is achieved by being connected to the output of its counterpart transistor. Second, the start-up condition is better than the conventional Colpitts VCO. This can be intuitively understood by the adoption of a cross-coupled-pair-like transistor pair. It can be verified [14] that the negative conductance generated by this configuration is boosted by a factor of $(2 + {C_2}/{C_1})$ compared to the conventional configuration. This ensures a safer start-up condition. The simulation result is shown in Fig. 3.5. The left plot in Fig. 3.5 shows the available negative conductance generated by the proposed cross-coupled Colpitts VCO and the conventional fixed base biasing Colpitts VCO respectively. The right plot shows the boosting factor. The simulation is performed with C_1 equal to 100fF and C_2 equal to 200fF. The operating frequency is 60GHz and the biasing current is swept from 1mA to 10mA as seen on the X axis. The boosting factor is approximately 4 within the whole sweeping range, which is in good accordance with the prediction above that a boosting factor of $(2 + {C_2}/{C_1})$ is expected for the proposed topology.

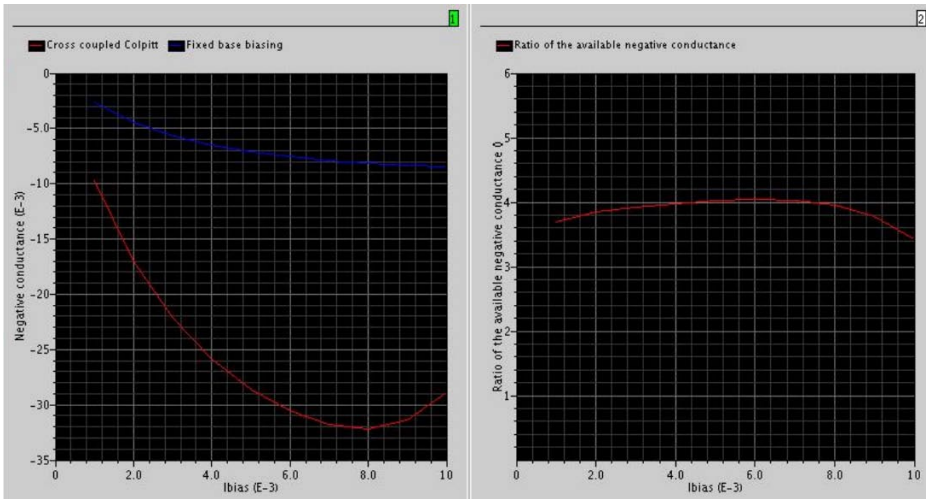

Fig. 3.5 Comparison between the proposed and conventional topology

A safer start-up condition is achieved by the use of the proposed cross-coupled Colpitts topology. Or, to put it in another way, the power consumption needed to ensure a reliable start-up is reduced since a smaller current is needed for the same start-up condition. Last but not least, a fast switching of Q1 and Q2 is realized in this configuration since the output of one Colpitts VCO core is directly connected to the base of the other VCO. Fast switching is desired for suppressing the noise contributions from the active devices during the zero-crossings of the tank. This will help to improve the phase noise performance.

Along with the benefits that the proposed configuration has introduced, there are also some things that need to be considered as a penalty. The most straightforward side effect is that the b-c junction is forward biased for half of each cycle and directly connected in parallel with the tank, which will de-Q the tank and reduce the tuning range as a result. In addition, the maximum swing on the tank will also reduce due to the clamping of the transistors.

Note that there are now 2 feedback loops within the oscillator, one via the tapped capacitors and the other via the cross coupling. They serve different purposes. The feedback via the tapped capacitors is essence for the Colpitts to provide negative transconductance, while the feedback via the cross coupling aims at enhancing the start-up condition.

The calculation of the passive component values will be given in detail in Appendix A.

3.3 General considerations

The process of designing a circuit is also a process of making trade-offs and compromises. The various things that we need to consider in designing the VCO are described in this section.

3.3.1 Optimum biasing current

Recall the negative conductance calculated in the previous section (eq. 3.4) and take the absolute value of it, we have:

$$|\mathrm{Re}(Y_{in})| = \frac{g_m \omega^2 C_1 C_2}{g_m^2 + \omega^2 (C_1 + C_2)^2} \tag{3.5}$$

Equation 3.5 is a function of g_m, C_1, C_2. Assume that we have fixed the values for the two capacitors C_1 and C_2. Then we can still control g_m by varying the biasing current.

We can sweep the I_C to see how the negative conductance will change accordingly. For very small I_C, g_m is also small. Therefore, the first term (i.e., g_m^2) in the denominator is small and can be safely ignored. The expression for the negative conductance can be reduced to the following expression, which is proportional to the biasing current.

$$|\mathrm{Re}(Y_{in})| = \frac{g_m \omega^2 C_1 C_2}{g_m^2 + \omega^2 (C_1 + C_2)^2} \approx \frac{g_m \omega^2 C_1 C_2}{\omega^2 (C_1 + C_2)^2} = \frac{g_m C_1 C_2}{(C_1 + C_2)^2} \tag{3.6}$$

With the increase of the biasing current, g_m also increases accordingly. The first item g_m^2 in the denominator can no longer be ignored. If we further increase the biasing current, the first item g_m^2 will be dominant. The expression therefore reduces to the following expression, which is inversely proportional to the biasing current.

$$|\mathrm{Re}(Y_{in})| = -\frac{g_m \omega^2 C_1 C_2}{g_m^2 + \omega^2 (C_1 + C_2)^2} \approx -\frac{g_m \omega^2 C_1 C_2}{g_m^2} = -\frac{\omega^2 C_1 C_2}{g_m} \tag{3.7}$$

As can be seen from the above analysis, with the increase of the biasing current, the absolute value of the negative conductance will first increase up till a certain point then decrease. Therefore, there exists an optimum value of the biasing current for the negative conductance to reach its maximum value. A large negative conductance is desired for the sake of easy start-up condition. Depending on the selection of operating frequency ω, C_1, C_2, and the g_m of the transistor, the available negative conductance is on the orders of several tens of milliSiemens (mS)

This can be also verified by the simulation result for the negative conductance generator at 60GHz. The result is shown in Fig. 3.6.

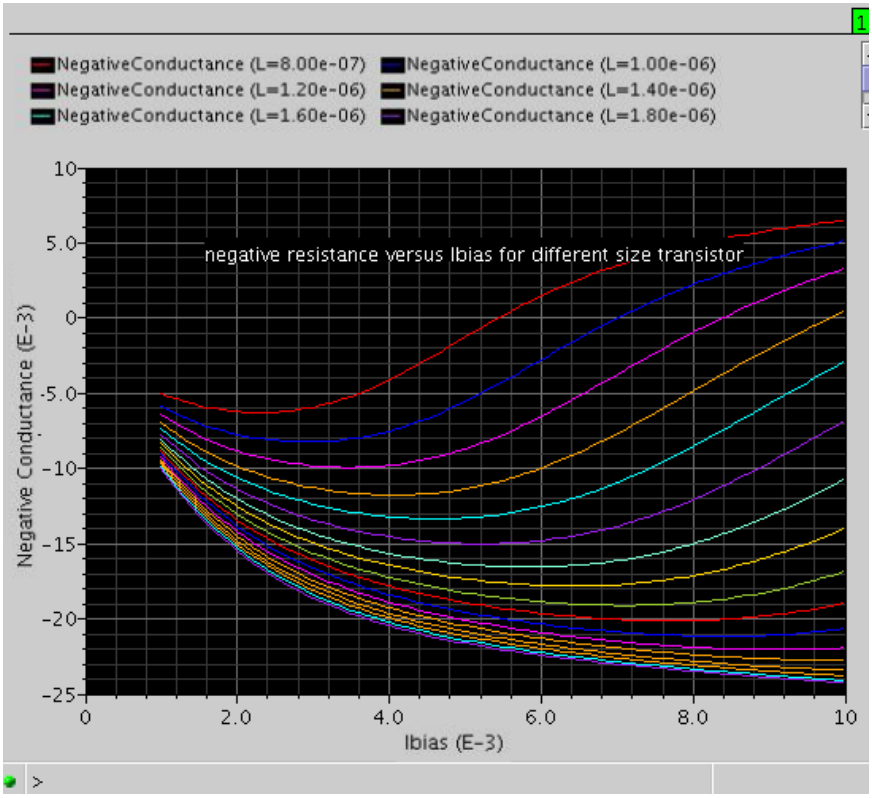

Fig. 3.6 Negative conductance produced by a single-ended Colpitts at 60GHz

The X axis is the biasing current ranging from 0 mA to 10 mA, the Y axis is the conductance seen from the collector of the transistor. The two Colpitts capacitors C_1 and C_2 are chosen to be 100fF and 200fF respectively. The base of the transistor is biased at a 0.8V voltage. A sweep of the emitter length ranging from 0.8 μm to 4μm with a step of 0.2μm is also performed to see the effect of the size of the transistor on the available negative conductance.

As can be seen from the plot, the absolute value of the negative conductance will first increase with the increase of the biasing current and then decrease for a fixed emitter length. Therefore, an optimum biasing current exists to achieve a maximum absolute value of the negative conductance which is predicted by the previous analysis and equations. The numerical result is in good accordance with the previous

predictions given by equation 3.6 and equation 3.7 which shows several tens of milliSiemens is available at 60GHz. In order to ensure a safe start-up, we would like to bias the transistor with this optimum current. However, the noise from the active device, which is related to the current flowing in the transistor, also needs to be taken into account.

3.3.2 Size of the transistor pair

Another useful conclusion from Fig. 3.6 is that the bigger the transistor, the more negative conductance it can provide. As can be seen from Fig. 3.6, the peak value of the absolute value of the available negative conductance also increases with the increase of the emitter length.

Various figure of merit about a single transistor have been investigated to judge the performance of the transistor in a high frequency application. f_{cross} is one of these metrics[15]. It represents the highest frequency at which a cross-coupled differential pair can provide a negative shunt resistance seen from the input.

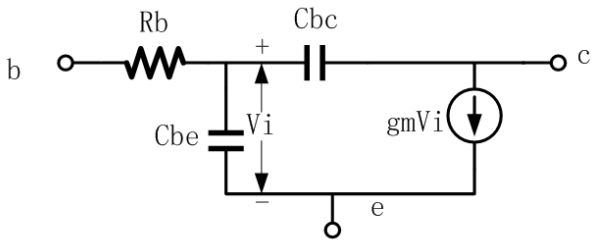

Fig. 3.7 Equivalent small-signal circuit diagram

Consider the small-signal equivalent circuit diagram shown in Fig. 3.7, where DC biasing is not shown. f_{cross} is given by the following formula:

$$f_{cross} \approx f_T \sqrt{\frac{1}{g_m R_b}} \tag{3.8}$$

f_T represents the unity-current gain bandwidth of the transistor if it is configured in a common-emitter manner, R_b is the base resistance of the transistor. A simulation of f_{cross} versus biasing current is shown in Fig. 3.8 with an emitter length of 5μm, which will give some hints on the selection of the biasing current.

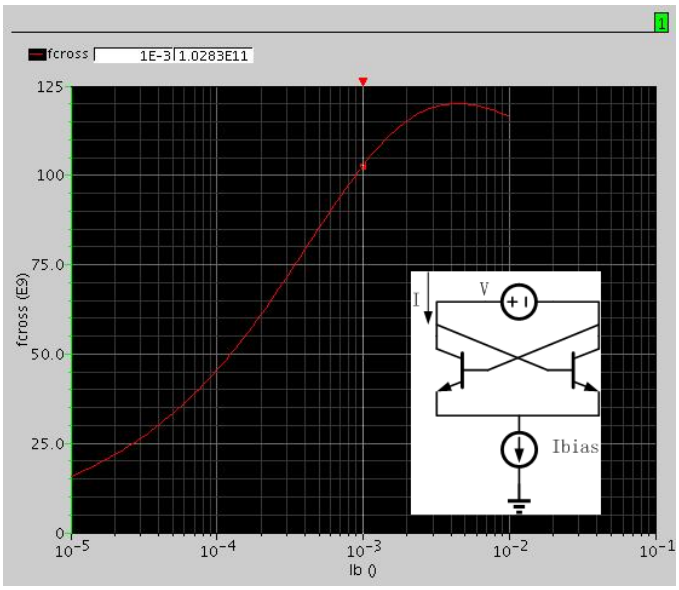

Fig. 3.8 f_{cross} versus bias current ($L_e = 5\mu m$)

It is straightforward to see that a lower R_b is desired if we want to achieve a high f_{cross}. Lower R_b means bigger size of the transistor. Along with the previous analysis and results shown in Fig. 3.6 that the bigger the size of the transistor, the more negative conductance it can provide, we tend to make the conclusion that bigger transistor size is favored. However, that's not the whole story.

As previously stated, one of the disadvantages of the cross-coupled Colpitts VCO in Fig. 3.5 is that the C_{be} of the transistor also manifests itself in the tank. The bigger the transistor is, the smaller the base resistance R_b is, but also the bigger the capacitance C_{be} is, which will cause a decrease in the tuning range. In addition, C_{be} itself is also bias dependent, so it is not only related to emitter area. Therefore, a trade-off has to be made between the safe start-up condition and the desired tuning range.

3.3.3 Frequency tuning

As the name voltage-controlled oscillator suggests, we need to have a mechanism to control the output frequency. The output frequency of VCO is mainly determined by the equivalent capacitance and equivalent inductance seen at the tank.

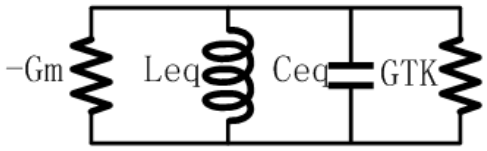

Fig. 3.9 Negative conductance model of a VCO

As can be seen from Fig. 3.9, L_{eq} is the equivalent inductance, C_{eq} is the equivalent capacitance, G_{TK} is the tank loss due to the finite quality factor of the passive components, $-G_m$ is the negative conductance generated by the active device to compensate for the losses. The oscillation frequency is given by:

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{eq}\,C_{eq}}} \tag{3.9}$$

In a practical circuit design, the inductor is not easy to tune. Therefore, we choose to introduce varactors into the tank to control the oscillation frequency. A varactor is a variable capacitor, whose capacitances can be controlled by an external voltage. Based on the way it is constructed, varactors can be categorized into two major types, namely, PN junction varactors and MOS varactors (inversion mode and/or accumulation mode).

There are several desirable characteristics of varators that need to be taken into account when choosing the correct varactor to use. A high C_{max}/C_{min} ratio and a high quality factor are the most important metrics among them. C_{max} and C_{min} are the maximum and minimum capacitance a varactor could achieve within the tuning

range. Quality factor ($Q \cong {}^{1}/_{\omega R_s C}$) indicates the losses for the capcitor. A high Q factor is always desired for lower losses.

The high ${}^{C_{max}}/_{C_{min}}$ ratio is desired since the tuning range is directly related to it. In this application a 10% tuning range or a 6GHz tuning range is considerably large, which poses a great challenge on the varactors.

$$\frac{f_{max}}{f_{min}} = \sqrt{\frac{C_{v,max} + 2C_{par}}{C_{v,min} + 2C_{par}}} \tag{3.10}$$

With the capability of the STMicroelectronics 130nm BiCMOS techonolgy, the available ${}^{C_{max}}/_{C_{min}}$ ratio for a MOS varactor is only approximately 2. In order to achieve a higher ${}^{C_{max}}/_{C_{min}}$ ratio, an array of different capacitor values, switched on and off digitally, could be a natural candidate. Fig. 3.10 shows the basic idea of this digitally-switched capacitor array. Based on the external control over the switch S1 to S4, different combinations of capacitance can be obtained.

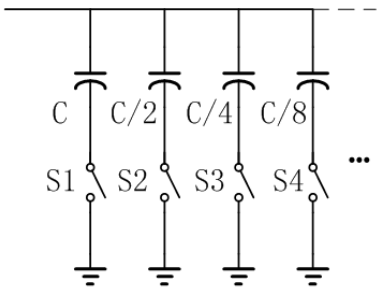

Fig. 3.10 Digitally-switched capacitor array

A very high ${}^{C_{max}}/_{C_{min}}$ ratio can indeed be achieved by this method. However, there are various concerns that go along with it. Firstly, the parasitic capacitances of the switch will manifest themselves in the tank, and add to the inaccuracy of the equivalent capacitance values. Secondly, the 'on' resistance of the switch will be in series with the capacitors, and therefore lowers the quality factor of the tank. The

switch itself will also contribute noise to the tank, which will worsen the phase noise performance. Last but not least, there will be some overlap between two adjacent tuning curves, as shown in Fig. 3.11. This implies that for a certain oscillation frequency there could be two control voltages related to it. This ambiguity in the voltage-controlled oscillator tuning characteristic is something that we would like to avoid.

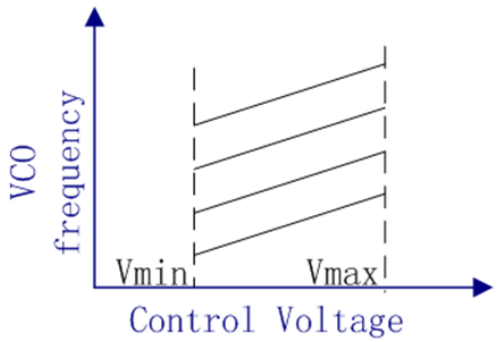

Fig. 3.11 Overlap of the tuning curves

Another issue related to the varactor, is the relatively low quality factor at high frequencies. There are inductors, varactors and capacitors in the resonating tank, which all have a limited quality factor. The lower the quality factor, the higher the losses. At 60GHz, the low quality factor (below 5) of the varactors will be a limiting factor. Some simulation results about the varactors at 60GHz are shown.

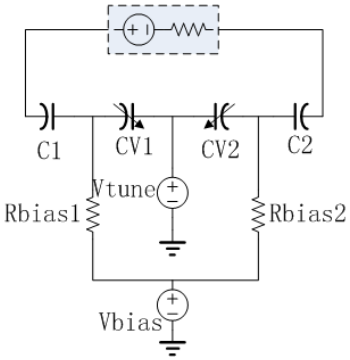

Fig. 3.12 Varactor tuning configuration (parasitic not shown)

As can be seen from the varactor tuning configuration of Fig. 3.12, C_{V1} and C_{V2} are the two MOS varactors, C_1 and C_2 are the two coupling capacitors which are chosen to be relatively big for AC coupling. $R_{bias\,1}$ and $R_{bias\,2}$ are two high-ohmic resistors which are used to isolate the RF current path through the capacitors from V_{bias} is chosen to be one-half of the supply voltage so that when V_{tune} varies from 0V to the supply voltage, the voltage across the varactor can experience both negative and positive values. Fig. 3.13 shows a typical varactor quality factor versus frequency plot. The simulation conditions are summarized in Table 3.1.

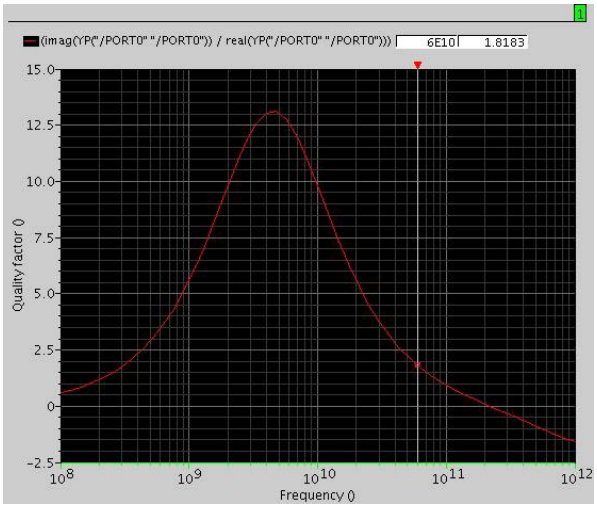

Fig. 3.13 Quality factor of the varactor versus frequency

Table 3.1 Simulation condition summary (STMicroelectronics 130nm BiCMOS)

V_{bias}	1.25
V_{tune}	1.25
Voltage across the MOS varactor	0
Finger of the MOS varactor	4
Width of the MOS varactor	2μm
Length of the MOS varactor	1μm
Frequency sweep range	100MHz – 1THz
Quality factor @60GHz	1.82

As can be seen from Table 3.1, the quality factor of the varactor at 60GHz is only 1.8. This low quality factor immediately poses a great challenge on the start-up condition or power consumption since a lower quality factor means more losses in the tank. Therefore, more negative conductance is needed to ensure a safe start-up and to sustain the oscillation. The phase noise performance will also suffer a lot due to this low quality factor.

Some more simulations have been done to gain some more insights into the parameters that have an impact on the quality factor at high frequency. There are several variables that we can adjust namely the finger numbers, width and lengths of the varactors. The simulations results are shown in Fig. 3.14.

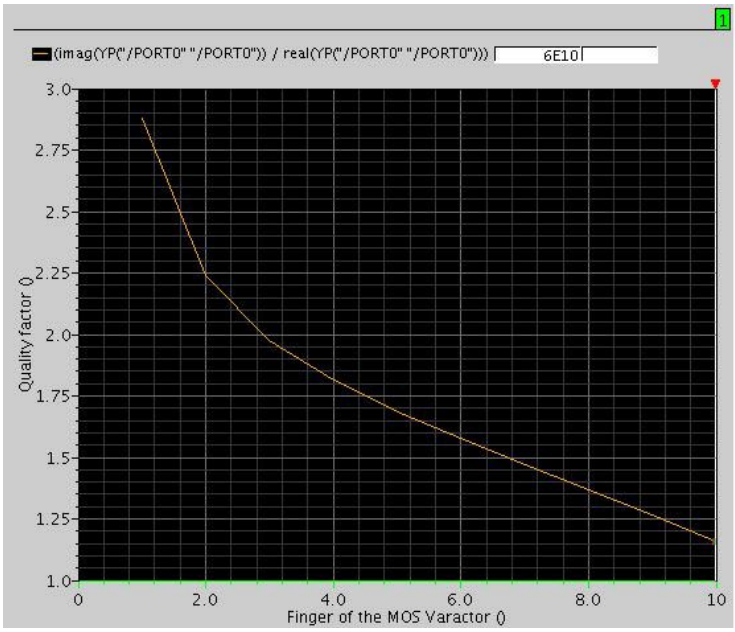

Fig. 3.14 Q factor versus finger numbers of the MOS varactor @ 60GHz

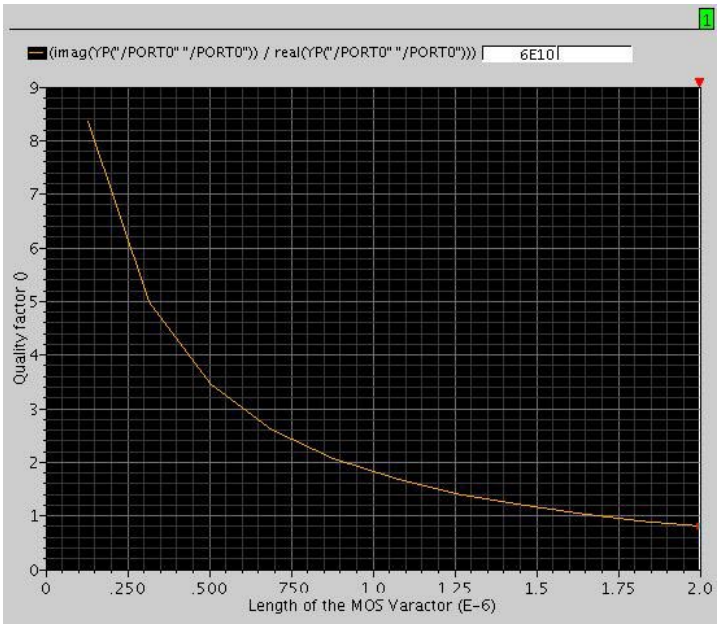

Fig. 3.15 Q factor versus length of the MOS varactor @ 60GHz

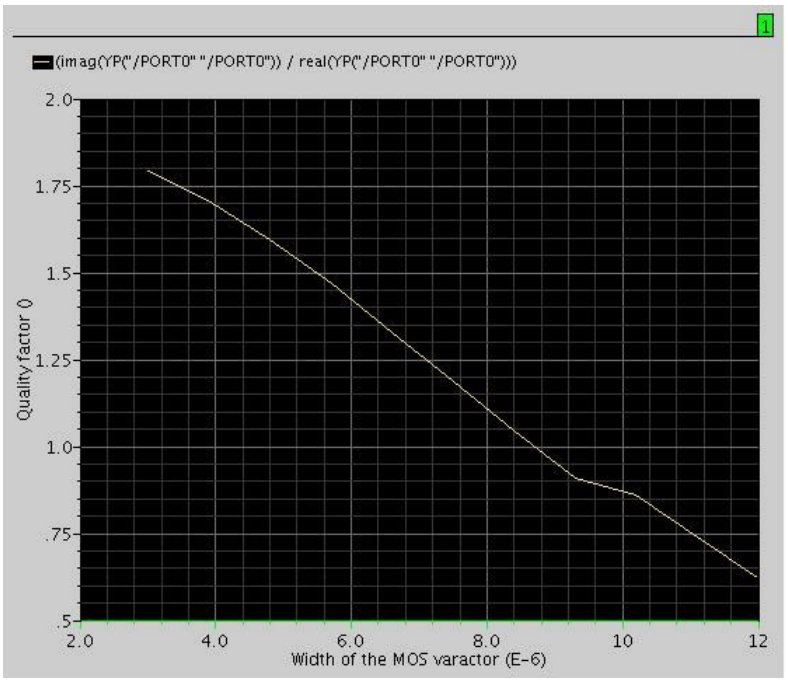

Fig. 3.16 Q factor versus width of the MOS varactor @ 60GHz

As can be seen from Fig. 3.14 to Fig. 3.16, any increase in the number of fingers, finger width or finger length will lead to a decrease in the quality factor. In other

words, the bigger the varactor capacitance is, the lower is the quality factor. This corresponds to the result given in [16]:

$$Q \cong \frac{1}{\omega R_s C} = \frac{12}{\omega C_{ox}(R_{nw} L^2 + R_{poly} W^2)} \tag{3.11}$$

where W and L are the width and length of each finger, R_{nw} and R_{poly} are the sheet resistances of the n-well and poly gate, C_{ox} is the gate-oxide capacitance per area.

All of these simulation results indicate that a smaller varactor size is desirable. However, recall equation 3.10, we can see that in order to maximize the tuning range, we would like to make the capacitance of the varactor much bigger than the parasitic capacitance. Therefore, there is a trade-off to make between the tuning range and the quality factor.

All the above simulation results are based on the use of MOS varactors in STMicroelectronics 130nm BiCMOS technology. There is also another type of varacotr in the library, the PN varactor. However, it is not useful since it has a very limited operating frequency. Above the frequency, the varactor behaves like an inductor rather than a capacitor. For a PN varactor with a finger of 4, width of 2μm, L_{fp} of 100μm, an operating frequency of only 30GHz is observed as shown in Fig. 3.17. Another problem for the PN varactor is the considerably larger area compared to MOS varactor implementation for the same capacitance.

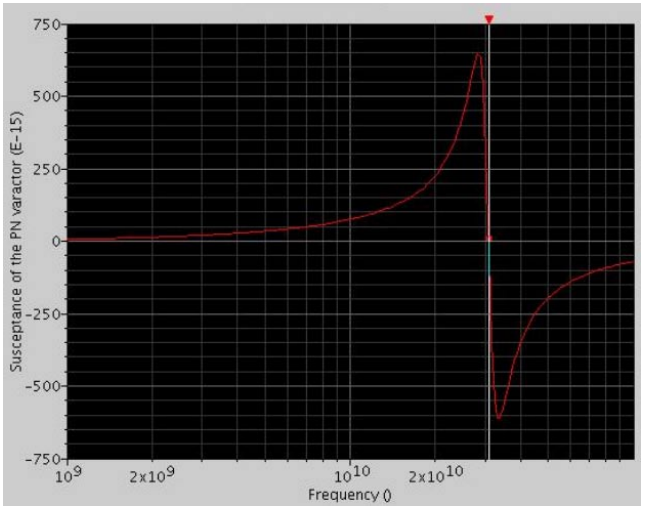

Fig. 3.17 PN varactor's susceptance versus frequency

3.3.4 Phase accuracy and phase noise

Consider the oscillator as a feedback system, then we can have another definition for the quality factor [17], which is known as the open-loop Q_{OL}.

$$Q_{OL} = \frac{\omega_0}{2}\sqrt{(\frac{dA}{d\omega})^2 + (\frac{d\theta}{d\omega})^2} \tag{3.12}$$

$$A = |H(j\omega)| \tag{3.13}$$

$$\theta = \angle H(j\omega) \tag{3.14}$$

Where A is the magnitude of the transfer function H(jω) and θ is the phase of the transfer function H(jω). The frequency response of a LC tank showing the magnitude and phase plot is given in Fig. 3.18. As evident from the plot, $\frac{dA}{d\omega}$=0 and $\frac{d\theta}{d\omega}$ reaches its peak value at the resonant frequency. Therefore, equation 3.12 can be reduced to

$$Q_{OL} = \frac{\omega_0}{2}\sqrt{(\frac{dA}{d\omega})^2 + (\frac{d\theta}{d\omega})^2} = \frac{\omega_0}{2}\sqrt{(\frac{d\theta}{d\omega})^2} = \frac{\omega_0}{2}\left|\frac{d\theta}{d\omega}\right| \ (\text{at } f_{osc}) \tag{3.15}$$

Quality factor indicates the slope of the phase versus frequency. A higher quality factor is related to a steeper slope which means a small deviation from the resonance

frequency already gives a significant phase variation. We would like to minimize the phase variation, which can be represented by $\frac{d\theta}{d\omega}$. This means a low Q is desired for minimizing the phase error. However, a low quality factor will immediately worsen the phase noise since the phase noise is inversely proportional to the quality factor of the tank.

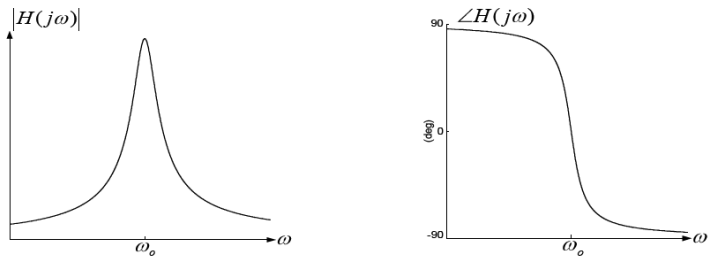

Fig. 3.18 Frequency response of a LC tank

3.4 Quadrature VCO

A quadrature VCO is essential to this design since quadrature error and amplitude mismatches between the I and Q signals will corrupt the down-converted signal constellation. Modern wireless applications contain different information in I and Q signals respectively, therefore a high quality Q-VCO with litte I/Q mismatch is desired. A series coupling method as shown in Fig. 3.19 is proposed to achieve the desired quadrature output

Recall the previous analysis of coupling the two identical VCO cores in Chapter 2.3. We need to force a 180 degree phase shift within the loop. First, we are going to build two identical VCO cores which take the prototype from Fig. 3.5. The current sources in Fig. 3.5 are now implemented with MOS transistors which function as current switches. The left VCO core is denoted as I-VCO (In-phase VCO) and the right VCO core is denoted as Q-VCO (Quadrature VCO). The output of the I-VCO is

connected in common phase to the switching pair of the Q-VCO, whereas the output of the Q-VCO is fed-back to the switching pair of the I-VCO in anti-phase. Therefore, a 180-degree phase shift is achieved within the whole loop. The switching pair switches the current into one branch or the other. Since it is in series with the Colpitts VCO pair, it is therefore referred to as series coupling. The switching pair also has a direct relationship with the phase noise performance. By optimizing the size of the switching transistor, one can control how strong the coupling is, and manipulate the time during which the branch is on or off. According to Hajimiri's phase noise theory[3], the time that the transistor is on or off also determines the time during which the noise is injected into the circuit. By coupling two VCOs together in a series manner, the injected current flows into the tank at the instance further away from the zero crossings than in the case of a single VCO, achieving a better phase noise than in parallel coupling configuration.

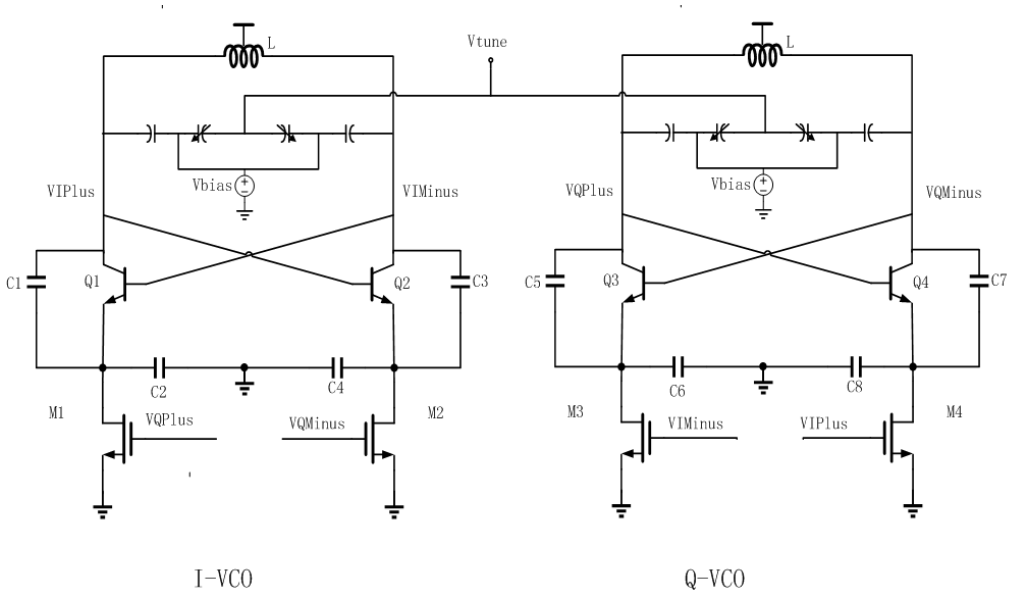

Fig. 3.19 Series coupled Q-VCO

The moment when the noise is injected into an LC tank has a direct relation to the phase change. The impulse sensitivity function (ISF) is a periodic function of time, capturing the time varying periodic nature of the system[3]. A noise disturbance

creates a phase disturbance as a convolution integral of the injected noise and the ISF, which in turn modulates the phase of the carrier. Consider the situation in Fig. 3.20. The impulse current is injected into the LC tank when the peak voltage is present across the tank. The current will flow into the capacitor, dumping a certain amount of charge Δq on the capacitor plates, therefore the amplitude of the signal will change accordingly whereas the phase remains unchanged. Another situation is when the current impulse is injected at the zero-crossing. As can be seen in Fig. 3.21, the dumped charge will influence not only the amplitude but also the phase of the signal. To improve phase noise performance, we would like the moment when the noise is injected to the tank far away from the zero-crossing and the duration of the noise injection is minimum.[13]

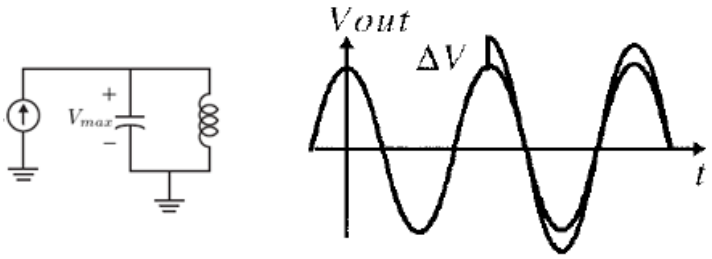

Fig. 3.20 Injection at peak amplitude

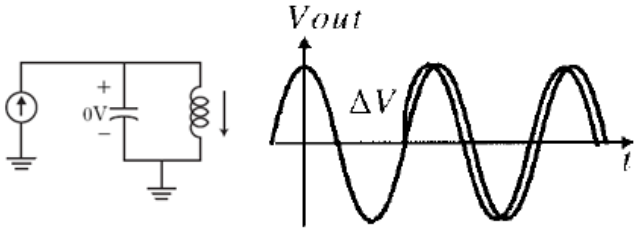

Fig. 3.21 Injection at zero-crossing

3.5 Trade-off summary

As can be seen from the previous analysis, there are various trade-offs that need to be considered when designing the oscillator. To summarize, there are 4 major aspects which are important, namely phase accuracy, phase noise, power consumption (startup condition) and tuning range. The target spec is to achieve a 10% tuning range with -80dBc/Hz at 1MHz offset from the carrier frequency. The power consumption is expected to be as low as possible. They trade-off with each other, therefore making it a multi-dimensional optimizing problem as illustrated in Fig. 3.22. The phase noise lies in the center position of this network, manifesting itself as the most challenging part to tackle. In addition to the limited quality factor of the tank and the noise from active devices, there are also other noise contributors due to power supply and external tuning voltage, which should be carefully handled. These noise sources can be minimized by careful design of the power supplies. Adequate RF ground is required and decoupling capacitors are needed between the power supply and ground. Interconnect to the tuning port must be as short as possible.

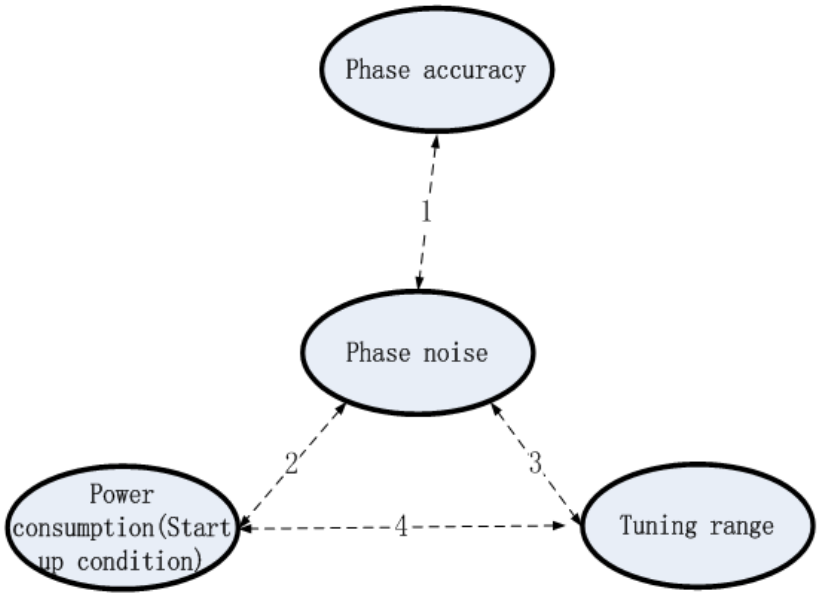

Fig. 3.22 Multi-dimensional optimizing problem

Trade-off 1:

Recall equation (3.15) $Q = \frac{\omega_0}{2}\sqrt{(\frac{dA}{d\omega})^2 + (\frac{d\theta}{d\omega})^2} = \frac{\omega_0}{2}\sqrt{(\frac{d\theta}{d\omega})^2} = \frac{\omega_0}{2}\left|\frac{d\theta}{d\omega}\right|$ (at f_{osc}), small phase error (phase variation) calls for a small $\frac{d\theta}{d\omega}$, which means a low quality factor while good phase noise requires a high quality factor. Thus, decreasing phase error implies increasing phase noise.

Trade-off 2:

According to Leeson's model for phase noise[18], the phase noise is inversely proportional to the signal power. We would like to reduce the phase noise by spending more power on the signal swing but this is at the cost of the total power consumption. Or, we can also keep the power consumption constant and raise the tank Q to achieve a better phase noise, which calls for more elaborate design for the layout of the varactors and inductor involved.

Trade-off 3:

As the previous simulation result shows, the smaller size of the varactor is, the higher quality factor it has. However, a bigger varactor is desired for maximizing the tuning range. A higher Q is always desired for lower phase noise. However, from a systematic point of view, a circuit with high Q implies a narrow bandwidth, which is the tuning range in the context of a VCO. Therefore a VCO designed for a big tuning range will have a poorer phase noise performance. A trade-off exists between phase noise and tuning range. An array of digitally-switched high-Q varactors is a possible solution at the cost of introducing an ambiguity in the oscillator tuning characteristic.

Trade-off 4

The smaller the varactor is, the higher quality factor it has and therefore fewer losses. Again, this contradicts the requirement for a bigger varactor in order to maximize the tuning range. In addition, for easy start-up, a big transistor size is desired to realize a large transconductance, which introduces more parasitic capacitance, therefore reducing the tuning range.

Chapter 4 Physical Layout and measurement setup

This chapter will cover the physical layout of the QVCO and peripheral circuits. We have to be careful with the layout in order to minimize deterioration of the performance.

4.1 General layout considerations

Due to various parasitic variations, process, voltage and temperature (PVT) variations, and packaging effects, the post-layout performance of the target circuit will inevitably deteriorate. What we are trying to do is to minimize these negative effects on the circuit performance by careful design and to meet the desired spec with some design margins.

In the context of a QVCO, the coupling of the two VCO cores is the most important thing for the layout. The I-VCO (In-phase VCO) and the Q-VCO (Quadrature-VCO) are expected to oscillate at the same frequency in the steady-state. The oscillation frequency is determined by the equivalent inductance L_{eq} and the equivalent capacitance C_{eq} seen at the tank as shown in equation 3.9

Any mismatch between the tank capacitances between the two VCO cores will cause a mismatch in the oscillating frequency. The discrepancy of the oscillation frequency is not desired since the two different oscillating frequencies will consequently introduce a “beat tone” whose frequency is the difference of the two oscillating frequency. This beat tone will manifest itself as an unwanted modulation effect on the output waveforms of the Q-VCO as shown in Fig. 4.1[19]. If there is a difference between the two output frequencies, the phase difference will also vary

with time. Therefore, the desired quadrature relation (90 degrees apart from each other) will no longer exist.

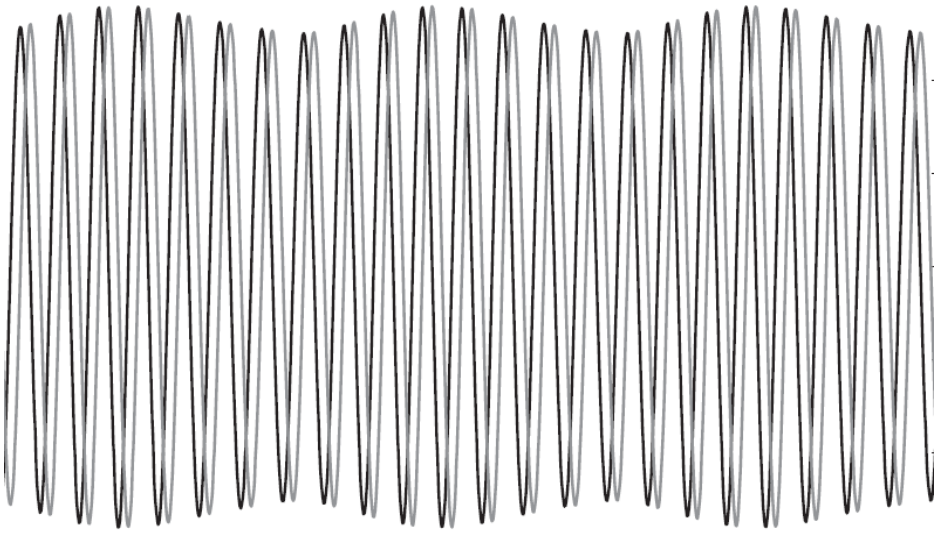

Fig. 4.1 Modulation effect at the QVCO output[19]

In order to minimize this effect, we would like to make the matching as good as possible. Symmetry is obviously on the top of the list. A high level of symmetry is desired for the interconnection between the two VCO cores. The coupling wires connect the output of one VCO core to the switches of the other VCO. The length difference is critical. Therefore, some additional adjustments for the lengths of the coupling wires are also needed to compensate for the length mismatch due to the crossing of the wires.

There is also a dilemma between phase accuracy and phase noise due to the position of the inductors. We would like to put the two inductors far away from each other to reduce parasitic mutual coupling between the two inductors. However, this is at the cost of longer length of the signal interconnects. The further away the two inductors are from each other, the lower the parasitic mutual inductances will be. However, a long signal line introduces more parasitic inductances as well as parasitic capacitance mismatch, which degrades the phase noise and phase accuracy. A trade-off has to be made in the placement of the two inductors.

A physical layout of the QVCO with high level of symmetry is shown in Fig. 4.2. Interconnect of the two VCO cores cross each other at the center of the layout. To avoid the modulation effect shown in Fig.4.1, the length mismatch should be carefully compensated. Interconnect between the two VCOs is modified in such a way that identical length is guaranteed. This is at the cost of a slightly bigger parasitic capacitance, which only has a minor effect on the operating frequency of the VCO. This can be later adjusted by changing the inductor value.

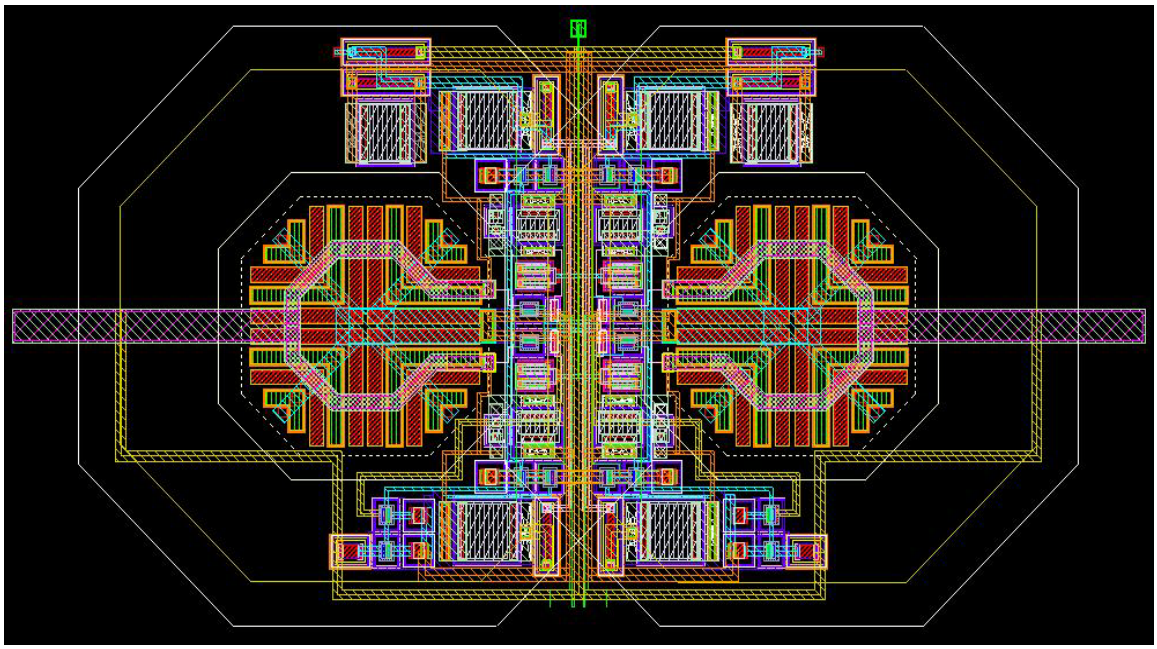

Fig. 4.2 Physical layout of the Quadrature VCO

4.2 Evaluation criteria

In addition to the common metrics for judging a VCO, e.g., tuning range, phase noise, etc., the most critical electrical parameters for this design are the correct phase and amplitude relationship between the two quadrature output signals. However, it is difficult to measure the amplitude and phase errors at high frequencies since the signal wavelength on silicon is only 2.5 mm at 60GHz. Any small difference in the

length of the test cables will already introduce several degrees of mismatch between the quadrature signals. In addition, amplitude mismatch will be introduced if the cables don't have the same losses.

Based on the above facts, it is desirable to down-convert the 60GHz signal to an intermediate frequency (IF) where errors in measurement and testing are lower than the quantities that we would like to measure. One reliable approach is to down-convert the signals using IF I/Q mixers and measure the power ratio of the desired signal to the image frequency[20]. At the IF (1GHz, for example), mature measuring equipment and quadrature hybrid devices are available therefore measurements errors can be minimized. This power ratio is known as the image rejection ratio (IRR) and can be defined as:

$$\mathrm{IRR} = -10\log\left(\frac{\frac{P_{im}}{P_{sig}}}{\frac{A_{im}^2}{A_{sig}^2}}\right)(dB) \tag{4.1}$$

where $\mathrm{P_{im}}$ and $\mathrm{P_{sig}}$ are the average power of the image and desired signal, $\frac{\mathrm{A_{im}^2}}{\mathrm{A_{sig}^2}}$ is the image-to-signal ratio. When the gain mismatch and phase imbalance are small, the expression can be reduced to:

$$\mathrm{IRR} = -10\log\left(\frac{\frac{P_{im}}{P_{sig}}}{\frac{A_{im}^2}{A_{sig}^2}}\right) = -10\log\left(\frac{(\frac{\Delta A}{A})^2+\theta^2}{4}\right) \tag{4.2}$$

where $\frac{\Delta A}{A}$ is the relative amplitude mismatch and θ is the phase error.

We have to bear in mind that from a systematic point of view, the measured IRR is not only due to the phase and amplitude mismatch of the QVCO itself. The mismatches from all other peripheral blocks like the mixers, filters, etc., will also contribute to the overall mismatch and therefore have an impact on the image rejection ratio. We will strive to keep the mismatches from elsewhere as small as

possible to have a more accurate evaluation of the phase error of the QVCO itself. Careful physical layout is needed to minimize mismatch between similar components and achieve the desired IRR. Fig. 4.3 shows the plot of IRR versus amplitude and phase errors in quadrature signals. As can be seen from the plot, for an image rejection of 40dB, for example, the amplitude and phase mismatch must be kept within 0.1dB and 1°, respectively. According to the observations in [19], in integrated circuits without using calibration techniques, the typical values for amplitude mismatch are 0.2–0.6 dB and 3−5◦ for the quadrature error, leading to an image suppression of 25 to 35 dB. In this design, only the phase error is of concern since the amplitude mismatch will not manifest itself as long as an amplitude limiting stage is followed, depending on the application. To achieve an image rejection ratio of 25-35dB, a phase error of less than 5 degree is tolerable.

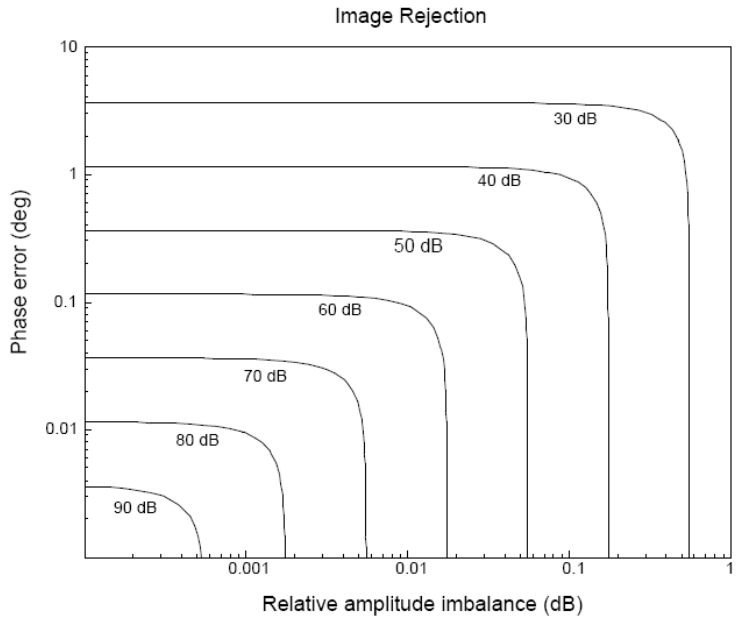

Fig. 4.3 IRR versus phase error and relative amplitude imbalance

4.3 Peripheral blocks for evaluation

As stated in the previous section, we would like to down-convert the high frequency signal to an intermediate frequency. Therefore, several peripheral building blocks are needed to perform this frequency translation. In this chapter, a floor plan of the measurement setup will be introduced along with the functionality of each block.

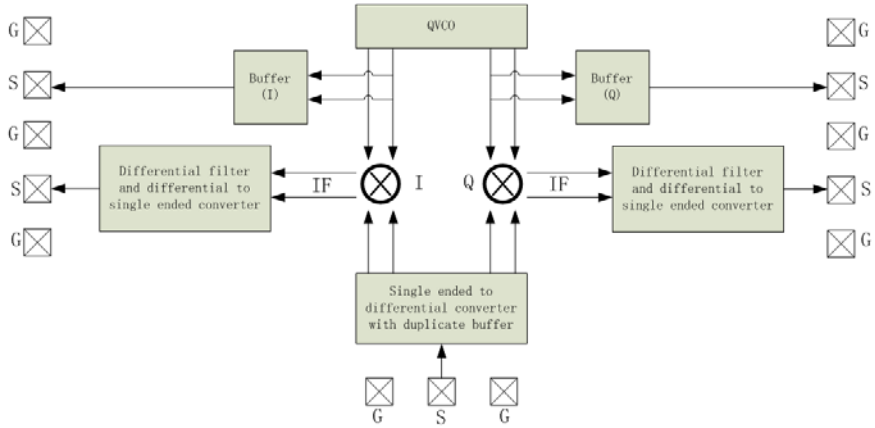

Fig. 4.4 Floor plan of the measurement setup

As can be seen from Fig. 4.4, there are several additional building blocks involved in the complete measurement setup, namely the single-ended to differential converter, the IF mixer, the differential filter and differential to single-ended converter, and the buffer.

The signal flow goes as follows. An external single-ended signal source operating at around 60GHz is fed into the system via the GSG plane, which stands for ground-signal-ground configuration. Due to the nature of the differential mixer, a differential signal is needed instead of a single-ended one. In addition, two paths of identical signals are needed for the I-channel and Q-channel, respectively. There are two possible ways to generate identical differential signals. One method is to first split the signal into two identical parts by a power splitter and then feed them into two singled ended to differential converters separately as in Fig. 4.5(a). The other is to

first convert the single-ended signal into differential signal and then use a power splitter to feed them into the I-channel and Q-channel, respectively, as in Fig. 4.5 (b). In this design, the second method is adopted, and the power splitter is replaced by a duplicate buffer stage for simplicity and to minimize mismatch.

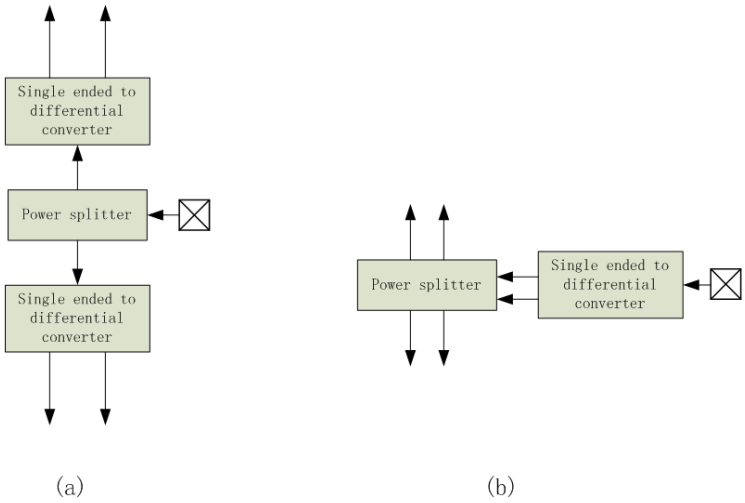

Fig. 4.5 Two ways of generating two differential signals

The differential signals for the I-channel and Q-channel are then fed into the IF I-mixer and Q-mixer, respectively, to do the frequency shift. The mixer is fully differential. The other input of the mixer comes from the QVCO output. Let's denote the frequency of the differential signal generated by the QVCO as f_{osc} and the frequency of the differential signal from the external source as f_{ext}. The mixer serves as a frequency manipulator. Given the two input frequencies as f_{osc} and f_{ext}, the output of the mixer will have two frequency components, namely $f_{ext} + f_{osc}$ and $f_{ext} - f_{osc}$. The output of the mixer is then fed into a differential low-pass filter to filter out the high frequency part $f_{ext} + f_{osc}$, and only the IF part $f_{IF} = f_{ext} - f_{osc}$ remains. The IF signal then goes through a differential to single-ended converter to make it easy for probing. In parallel to the signal fed into the mixer, the output of the QVCO is also connected to a buffer for probing to see whether the QVCO oscillates or not.

4.4 The selection of IF

In general, the selection of IF is not critical. The idea is to translate the high frequency to an intermediate frequency so that it is easier to measure the signal quality accurately. We can set the IF equal to 1GHz, or even lower. It is also related to the bandwidth of the following stage, which is a differential to single ended converter.

$$f_{IF} = |f_{ext} - f_{osc}| = 1\text{GHz} \tag{4.3}$$

f_{osc} is 60GHz and f_{ext} could be 59GHz or 61GHz. For the real application, it is critical to judge the sign of the difference since it indicates whether an object is moving towards, or away from the observer. However, in this test chip the sign is not that critical. For conformity and simplicity, we just make sure that the frequency of the external source is higher.

$$f_{IF} = f_{ext} - f_{osc} = 1\text{GHz} \tag{4.4}$$

4.5 IF Mixer

The intermediate frequency (IF) mixer adopts a Gilbert double-balanced topology as in Fig. 4.6. This is the preferred mixer implementation for most radio systems, due to its strong suppression of LO-RF feedthrough and cancellation of even-order harmonics. Some modifications have been made to enhance the LO-RF port-to-port isolation. An intermediate common-base stage (Q6 and Q7 in Fig. 4.6) is inserted between the 4 transistor quad at the top, and the differential pair at the bottom. The common-base stage serves the purpose of providing more isolation. This can be understood by the following observations. In Fig. 4.7(a), the point P experiences two full excursions in each period of the LO; $2f_{LO}$ is expected at this node. This signal will be coupled with V_{in} via the base-collector junction capacitance of Q1. This feedthrough will deteriorate the port-to-port isolation. This can be improved by the use of a common-base stage in Fig. 4.7(b). The feedthrough is greatly attenuated by the high reverse isolation of the common-base stage. A 30dB improvement in the

RF-LO isolation is obtained from addition of the common-base stage as can seen in Fig. 4.8.

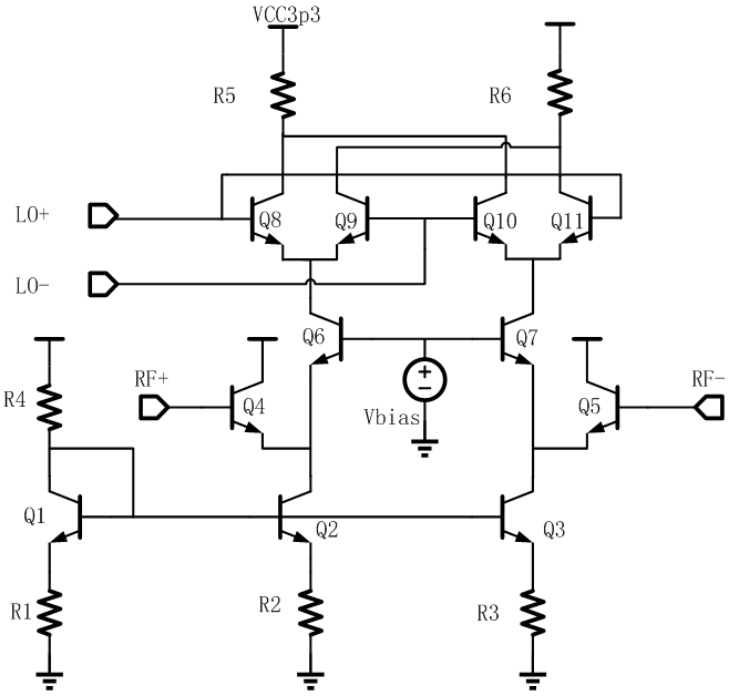

Fig. 4.6 Double balanced mixer with enhanced port to port isolation

Table 4.1 Mixer components values

R1,R2,R3	100Ω
Q1,Q2,Q3	3μm
Q4,Q5	5μm
Q6,Q7	3μm
Q8,Q9,Q10,Q11	4μm
R5,R6	400Ω

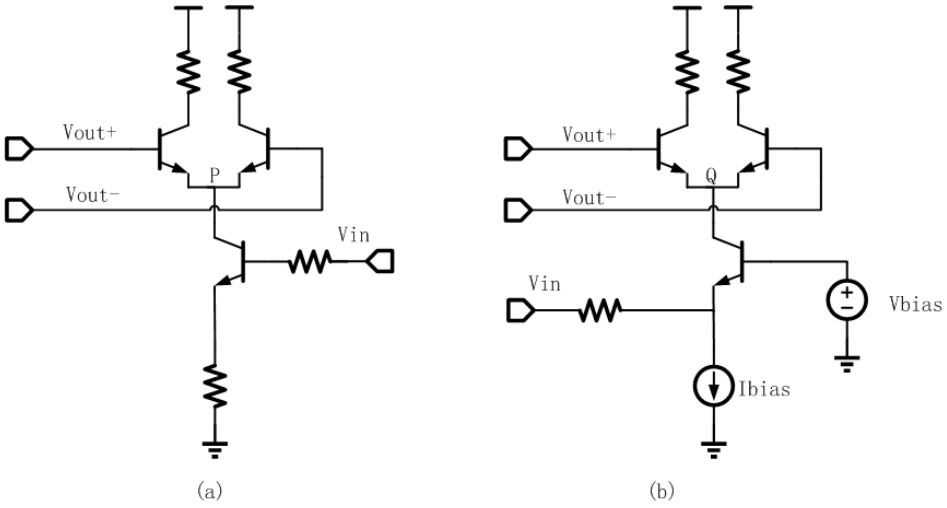

Fig. 4.7 Common-emitter input (a) versus common-base stage in (b) to enhance the LO-RF isolation

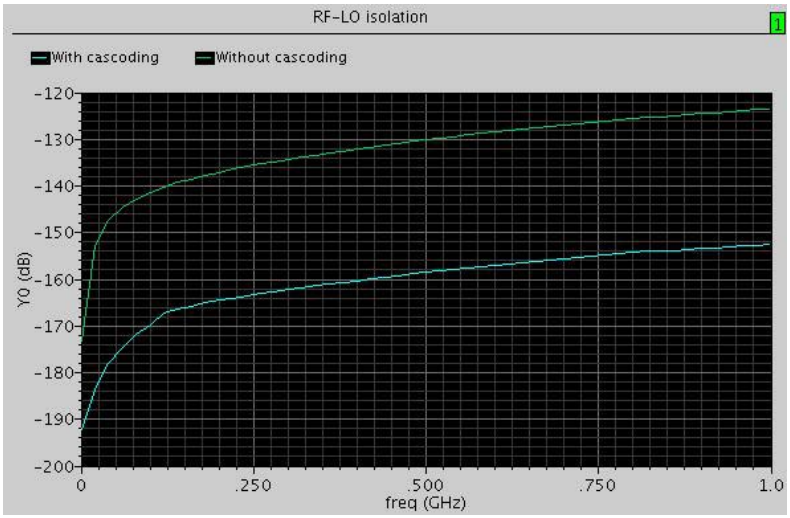

Fig. 4.8 RF-LO isolation with and without cascoding

4.6 Differential filter and differential to single ended converter

The signal from the mixer output contains both $f_{ext} + f_{osc}$ and $f_{ext} - f_{osc}$ signal components. We need to filter out the high frequency part as only the IF part is needed. Therefore, we feed the signal into a differential filter, which is shown in the top yellow box in Fig. 4.10. The RC network consisting of R1, R2, C1, C2 forms the low-pass differential filter. The cutoff frequency of the low-pass filter is given by:

$$f_{cutoff} = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi * 200\,\Omega * 400\,fF} = 2GHz \tag{4.5}$$

Since $f_{ext} + f_{osc}$ is almost 120GHz, and $f_{IF} = f_{ext} - f_{osc}$ is less than 1GHz, a f_{cutoff} of 2GHz is sufficient to do the filtering.

After the differential filter, the signal is then fed into a differential to single-ended converter so that it is easy to measure accurately with external equipment. The easiest and most straightforward way to do this transformation is to use an operational amplifier which is configured as in Fig. 4.9. The transfer function is given by:

$$V_{out} = \frac{(R_f+R_1)R_g}{(R_g+R_2)R1} V_{in2} - \frac{R_f}{R_1} V_{in1} \tag{4.6}$$

If we make $R_1 = R_2$ and $R_f = R_g$, the transfer function is reduced to

$$V_{out} = \frac{(R_f+R_1)R_g}{(R_g+R_2)R1} V_{in2} - \frac{R_f}{R_1} V_{in1} = \frac{R_f}{R_1}(V_{in2} - V_{in1}) \tag{4.7}$$

This configuration serves the purpose of differential to single-ended conversion perfectly. The closed-loop gain of the operational amplifier is shown in Fig. 4.11. The level shifter in the blue box in Fig. 4.10 is needed to set the DC level at the input of the operational amplifier to be compatible with the previous stage.

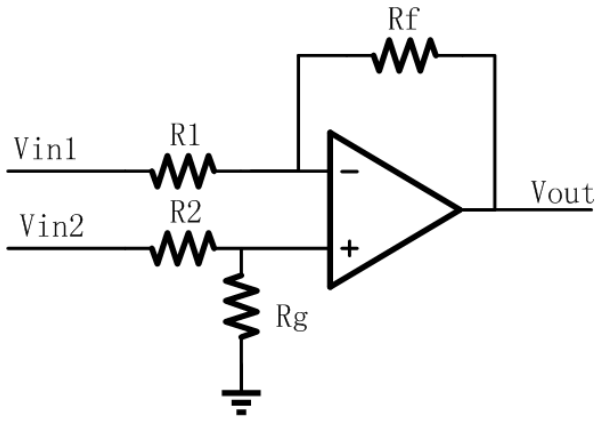

Fig. 4.9 Operational amplifier configuration

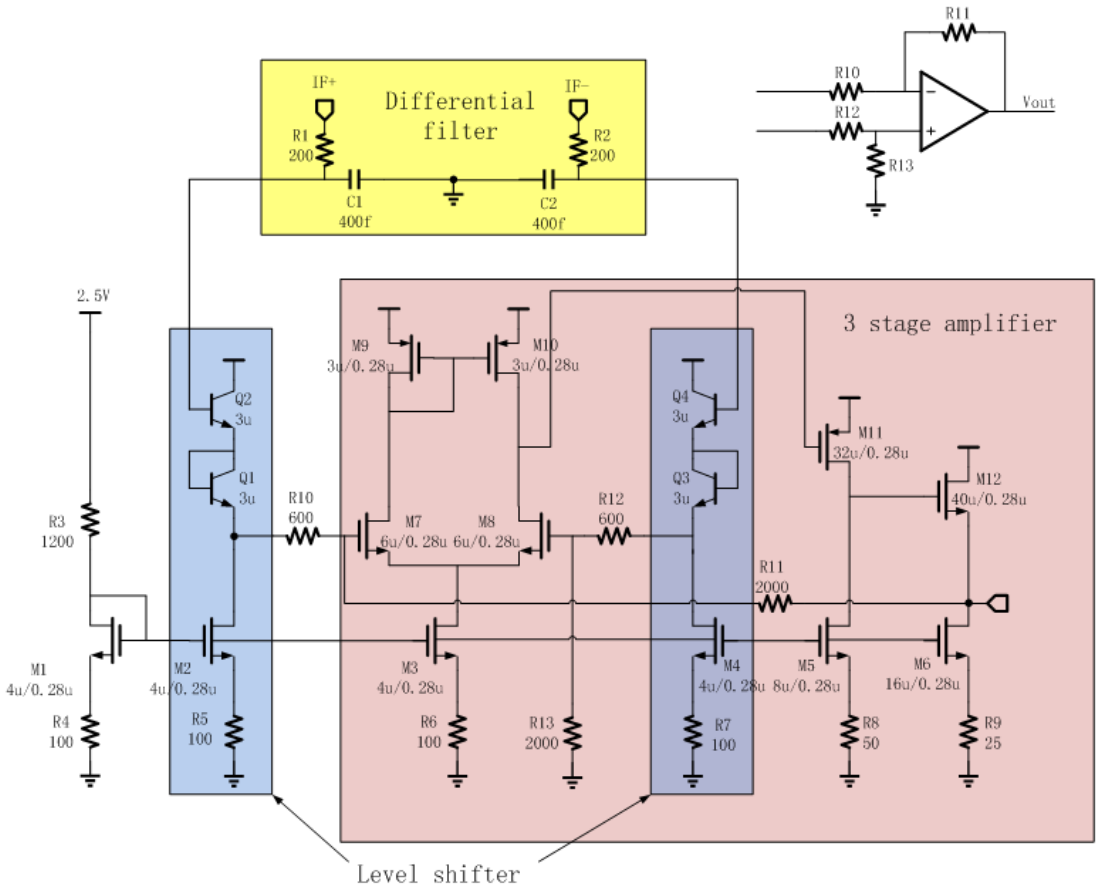

Fig. 4.10 Differential filter and differential to single-ended converter

The components values are shown in Fig. 4.10. The level shifter moves the DC level of the signal from 2.2V to 1.2V, which is desired for the correct operation of the

transistor pair M7 and M8. The first stage serves the purpose of converting a differential voltage to a single-ended voltage which is then fed into the common-source stage consisting of M11, M5 and R8 followed by a common-drain stage consisting of M12, M6 and R9. The resistors R10 to R13 form the passive feedback network and set the closed-loop gain of the entire system.

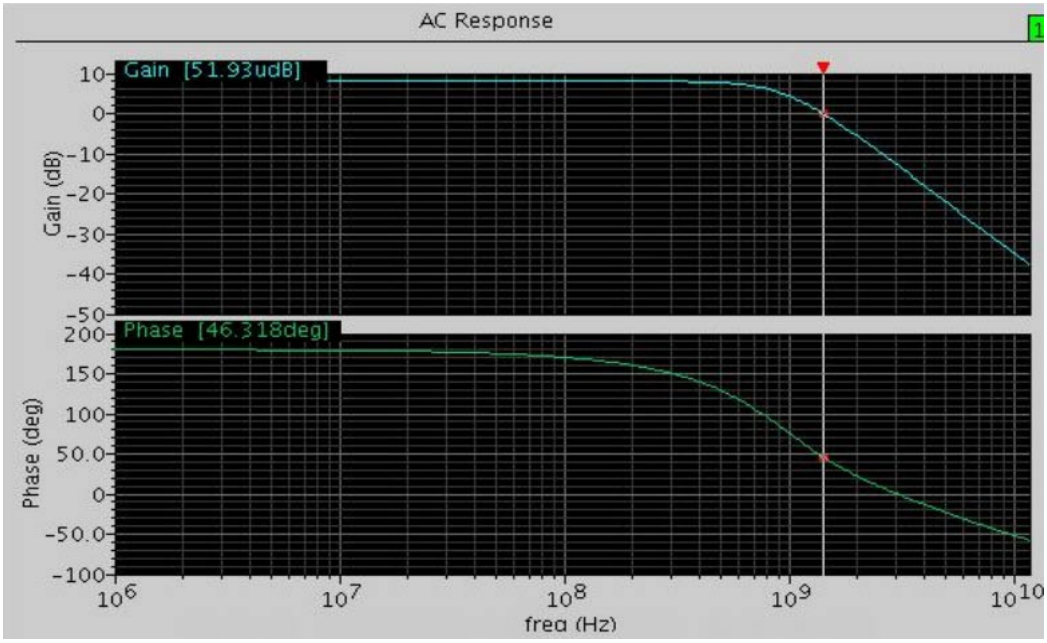

Fig. 4.11 Closed-loop transfer function

As seen in Fig. 4.11, the phase margin for the entire feedback system is 46 degree, which is adequate. Therefore, no frequency compensation is needed. Moreover, since the selection of IF is free, we can select the f_{ext} even closer to f_{osc} to get a lower IF, e.g., 200MHz. By doing this, the stability problem is no longer a big concern.

4.7 Overall layout

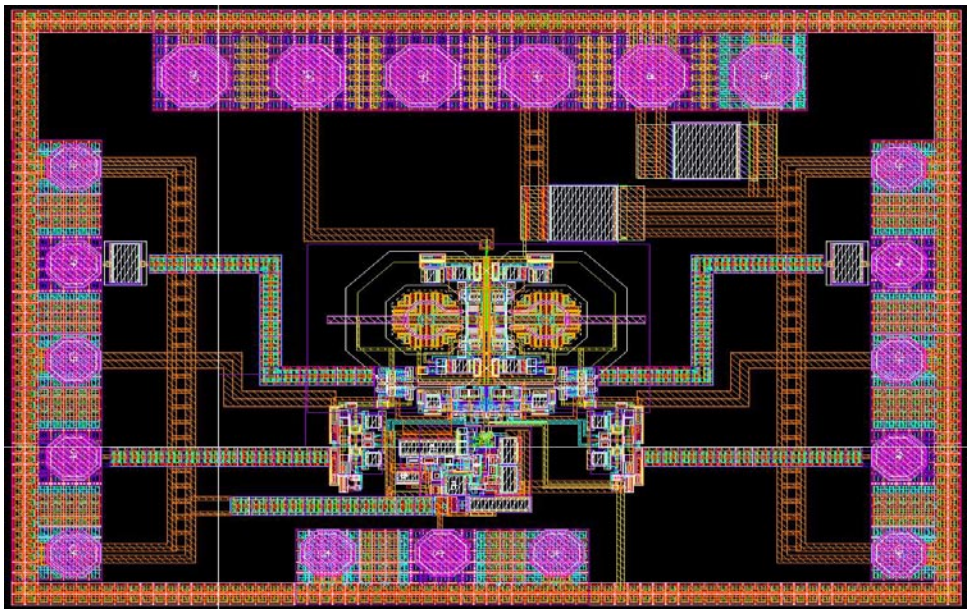

Fig. 4.12 Overall layout of the test chip

The overall layout of the test chip is shown in Fig. 4.12. The whole chip occupies an area of 1030μm x 730μm. It corresponds to the floor plan in Fig. 4.4. The QVCO lies in the center of the layout. The I and Q buffers are located at both sides of the QVCO. The I and Q mixers are in between the QVCO and the single ended to differential converter whose input comes from the GSG plane at the bottom. The outputs of the mixers are fed into the differential filters and the differential to single-ended converter, whose output is then connected to the ground-signal-ground-signal-ground (GSGSG) plane for probing. Decoupling capacitors are connected between the power supply and ground in order to reject the noise from the power supply.

4.8 Post-layout simulation result

The transient simulation result is shown in Fig. 4.13. The signals are taken at the positive node of the 50Ω load, which corresponds to the cable connection in the real

measurement setup. The in-phase and quadrature signals are depicted in the plot. The quadrature relationship is obtained. The intermediate frequency (IF) can be tuned by the control over the frequency of the external source.

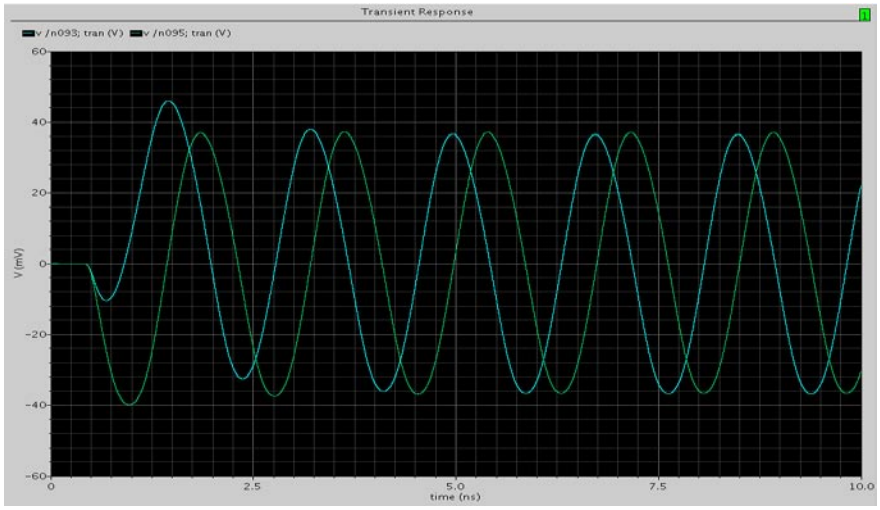

Fig. 4.13 Transient output waveform

From a supply of 2.5V, the QVCO core has a total power consumption of 28mW. The peripheral circuits consume another 131mW which adds up to a total power consumption of 159mW for the whole test chip. A list of the power consumption of each block is shown in Table 4.2. The tuning curve is shown in Fig. 4.14. With a tuning range from 0.5V to 2.3V, a tuning range from 53GHz to 59GHz is achieved.

Table 4.2 Power consumption of each block

Q-VCO	28mW
Buffers*2	7.5mW*2
IF Mixers*2	10mW*2
Diff. filter and diff. to single-ended converter	23mW*2
Single-ended to diff. converter	50mW
Total power consumption	159mW

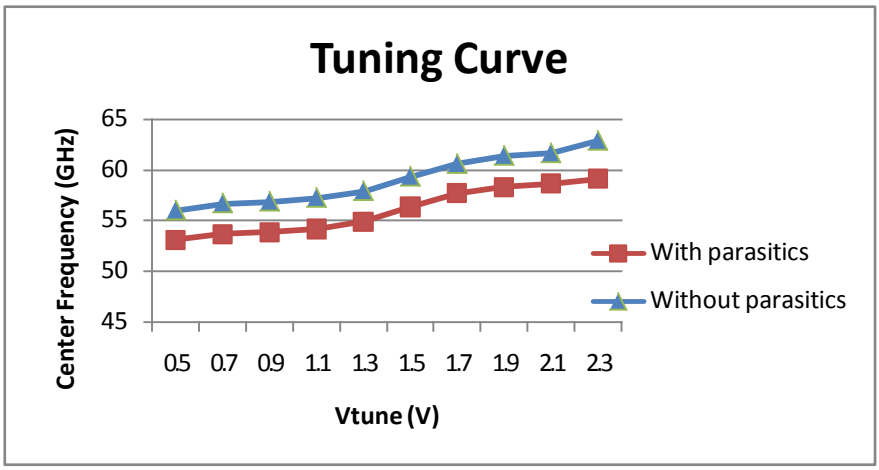

Fig. 4.14 Tuning curve

The phase noise and phase error plot are shown in Fig. 4.15 and Fig. 4.16 respectively. Within the range of carrier frequency from 53GHz to 59GHz, the phase noise is better than -75dBc/Hz at 1MHz offset from the center frequency. The phase error across the entire tuning range is within 4.27 degrees.

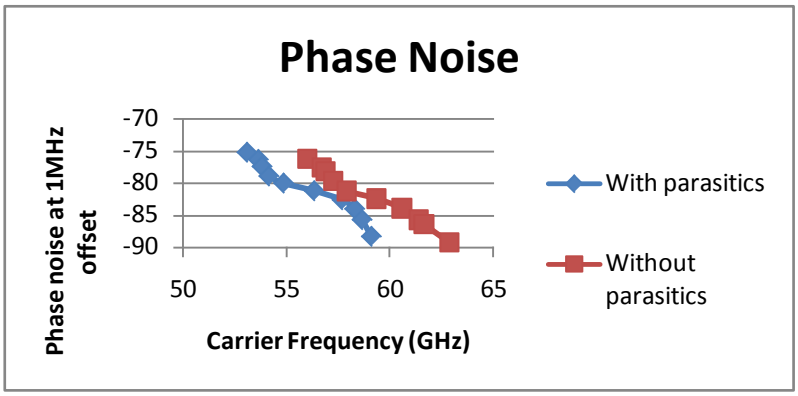

Fig. 4.15 Phase noise plot

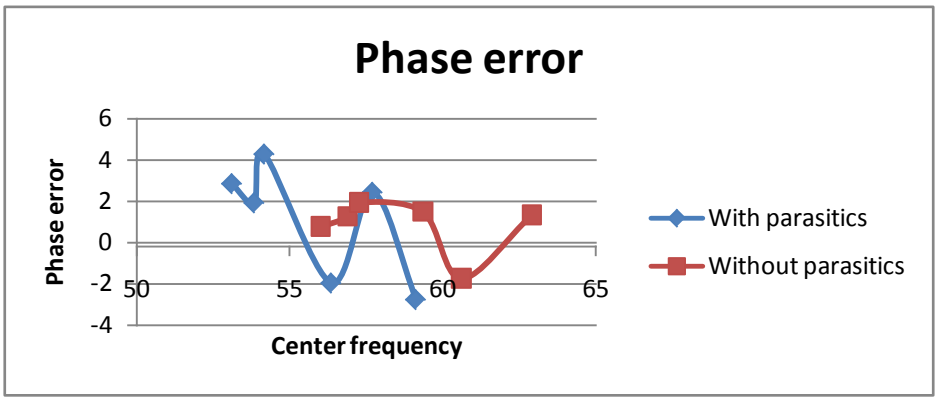

Fig. 4.16 Phase error plot

A summary of the performance is shown in Table 4.3. The layout parasitic mainly has an impact on the quadrature accuracy and phase noise performance. Iterations of the layout have been conducted in order to avoid the unwanted beat tone situation discussed in section 4.1. This is at the cost of a poorer phase noise since the lengths of interconnect are deliberately modified. Consequently, unwanted additional parasitic is introduced which deteriorates the phase noise.

Table 4.3 Performance summary

Specs	Targeted	Achieved(with parasitic)
Fosc(GHz)	57-63	53-59
Tuning range	10%	10.7%
Phase noise(dBc/Hz)	<-80 @1MHz offset	<-76 @1MHz offset
Quadrature error	<3°(IRR>35dB)	<4.27°
Pdiss(mW)	As low as possible	28 for the QVCO core, 145 for the whole chip

Chapter 5 Summary and future work

5.1 Summary

This thesis presents the design and implementation of a quadrature voltage-controlled oscillator in the 60GHz band. The 60GHz QVCO is designed in a 0.13μm BiCMOS process provided by STMicroelectronics.

The LC-VCO topology is clearly the choice due to its better phase noise performance than the relaxation oscillators. A Colpitts-based VCO is adopted for its easy start-up condition. Some unique modifications are made to enhance the performance of the QVCO. The "cross-coupled" differential Colpitts oscillator is proposed to further ease the start-up condition. The extremely low quality factor of the varactor at high frequencies ($Q \approx 2$ at $60GHz$) affects the phase noise performance of the QVCO. To generate quadrature outputs, coupled VCOs are used. In the proposed design, series coupling is used in the sense that the differential output of the I-VCO is connected in common phase with the switching pair of the Q-VCO, while the output of the Q-VCO is fed back to the switching pair of the I-VCO. The switching pair takes the place of the current source which is in series with the transistor in the Colpitss VCO core. By doing this, a 180 degree phase shift is ensured within the loop consisting of two VCO cores. Therefore, a 90 degree phase shift is expected if the two VCOs are identical. A nicely matched physical layout is therefore of importance in the design to ensure good phase noise and phase error.

With all the endeavors, a considerably high tuning range is achieved. With a tuning voltage from 0.5V to 2.3V, a 10% tuning range is achieved. The phase noise is inferior (<-76dBc/Hz @1MHz offset) due to the low quality factor at high frequency ($Q \approx 2$ at 60GHz). The power consumption is only 28mW for the QVCO core, making it easy to be integrated into a phase lock loop in the future. The whole design has been submitted for fabrication and will be measured in due time.

5.2 Comparison with literature

It is also interesting to compare the performance of the proposed design with the state-of-the-art design. To take all the important metrics of a VCO into account, the following figure of merit (FOM) is usually used[21].

$$\mathrm{FOM} = \left(\frac{f_{osc}}{\Delta f}\right)^2 \frac{1}{L(\Delta f) P_{diss}} \tag{5.1}$$

In which f_{osc} is the center oscillation frequency, Δf is the offset frequency away from the center frequency, $L(\Delta f)$ is the phase noise at Δf offset frequency, P_{diss} is the DC power dissipation of the VCO. Table 5.1 shows a summary of the proposed design and the comparison with similar designs reported in the recent literature. As evident from the table, the tuning range (10%) is among the highest of all the candidates, covering a whole band of 6GHz. However, the phase noise is inferior due to the low quality factor of the varactor at high frequency. The power consumption is average for a BiCMOS implementation. The overall performance is acceptable considering the fact that it is the only quadrature VCO while the other VCOs are single phased.

Note that the result is from simulation only. The performance of the real chip is expected to deviate from the simulated results. The operating frequency band might shift downwards due to the incomplete modeling of the parasitics from the inductor. This can be improved by selecting a smaller value for the inductor therefore pushing the frequency band back to the desired region. The tuning range will not see a dramatic change. Phase noise is vulnerable to mismatch and layout parasitic and is mostly prone to be affected. This can be improved by increasing the current to increase the carrier signal power. Since the thermal noise stays constant, increasing the signal power equivalently enhances the signal to noise ratio. A more symmetry layout also helps. Increasing the quality factor of the tank by applying shield to the substrate, which is indeed done in literature [22], is also a good approach to improve the phase noise.

Table 5.1 Comparison with literature

Ref	Process	f_{osc} [GHz]	Tuning [%]	Phase Noise [dBc/Hz]	P_{diss} [mW]	FoM [dB]
[22]	90 nm CMOS	60	0.17	-100@1MHz	1.9	192.8
[23]	SiGe HBT	98	3.3	-85@1MHz	60	167.0
[24]	SiGe HBT	85	2.7	-94@1MHz	25	178.6
[25]	InP HBT	108	2.6	-88@1MHz	204	165.6
[26]	130nm CMOS	90	2.4	-105@10MHz	15.5	172.2
[27]	130nm CMOS	114	2.1	-107.6@10MHz	8.4	179.5
[28]	0.12μ SOI CMOS	44	9.8	-101@1MHz	7.5	184.9
[29]	65nm SOI CMOS	70.2	9.55	-106@10MHz	5.4	175.4
[30]	SiGe BiCMOS	52.5	26.5	-108@1MHz	132	189.6
[31]	65nm CMOS	60	10.5	-81@1MHz	NA	162
[32]	130nm CMOS	59.1	10.2	-91@1MHz	3.9	181
This	130nm BiCMOS	60	10	-88@1MHz	28	171.1

It should be noted that [22] achieves the highest FOM by the use of an on-chip resonator with artificial dielectric in place of the LC tank which yields reduced metal/substrate losses therefore a higher resonator Q is obtained. A push-push VCO is described in [25], which alleviates the demand for high Q factor therefore achieving a high FOM. In [28] and [29], silicon-on-insulator (SOI) technology is used to reduce the substrate losses. Consequently, a high Q factor can be achieved. In [30], a very high FOM is achieved by the use of an array of capacitor which gets rid of the low-Q varactor. In addition, a frequency selector using loop-ground transmission line is used which further increases the complexity of the circuit. The Miller capacitances in [31], which serves as the frequency tuning component has a simulated quality factor of 6, three times as high as the Q factor in this technology. In[32], differential shielded transmission lines are used for a high-Q inductor solution, together with a simulated average varactor Q of 10.

5.3 Future work

The phase noise can be improved by increasing the quality factor of the tank. The tank quality factor is mainly limited by the varactor. Future work can be focused on finding a better tuning mechanism without the use of the low-Q varactor or a better implementation of the varactor. An advanced technology is also a possible approach.

Some improvements can be expected for the peripheral circuits such as the differential to single-ended converters and IF mixers so that a higher bandwidth (around 5GHz) and a lower power consumption can be achieved.

This thesis involves the design and implementation of a 60GHz QVCO. The next step is to integrate this QVCO into a QVCO-based phase lock loop (PLL) to complete itself as an integral component of the radar system. Based on that, the direct digital synthesis (DDS) technique might also be included for frequency modulated continuous wave (FMCW) radar application.

Appendix A Selection of the component values for the LC tank

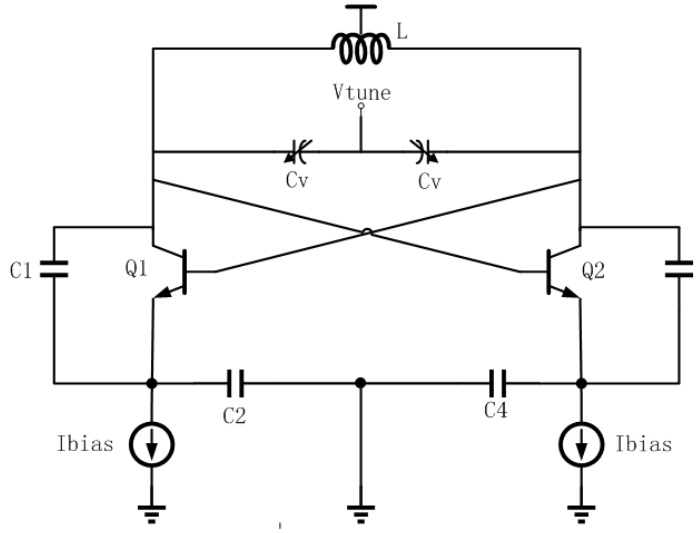

Fig. A.1 Proposed cross-coupled Colpitts oscillator

As discussed in Chapter 3, the proposed topology is an enhanced version of a conventional Colpitts oscillator. So let's first consider the conventional Colpitts oscillator core shown in Fig. A.1 to gain some insights on deciding the LC tank component values. The oscillation frequency is given by:

$$\omega = \frac{1}{\sqrt{L(\frac{C_1 * C_2}{C_1 + C_2} + C_v)}} \tag{A.1}$$

In order to obtain a relatively large tuning range, we would like to make C_v, which is the tuning knob, bigger than $\frac{C_1 * C_2}{C_1 + C_2}$. Therefore, we make the presumption in A.2. Also, this gives us a hint for the selection of the capacitors, C_1 is chosen to be the minimum value available in the technology, which is 30fF, C_2 is therefore chosen to be 150fF to give a considerably high boosting factor for the start-up condition while maintain a good phase noise performance[13].

$$C_v > C_1, C_v > C_2 \tag{A.2}$$

Every passive component has a finite quality factor which is reflected in the series resistance of it. The equivalent conductance of the varacor, two capacitors and inductor can be calculated. The targeted operating frequency is 60GHz.

$$R_{v,eq} = \frac{2}{\omega C_v Q_v},\ G_{v,eq} = R_{v,eq}(\omega C_{v,eq})^2 \tag{A.3}$$

$$R_{c1,eq} = \frac{2}{\omega C_{c1} Q_{c1}},\ G_{C1} = R_{C1,eq}(\omega C_{C1,eq})^2 \tag{A.4}$$

$$R_{c2,eq} = \frac{2}{\omega C_{c2} Q_{c2}},\ G_{C2} = R_{C2,eq}(\omega C_{C2,eq})^2 \tag{A.5}$$

$$R_{L,eq} = \frac{\omega L}{Q_L},\ G_L = \frac{R_{L,eq}}{(\omega L_{eq})^2} \tag{A.6}$$

$$G_{TK} = G_{v,eq} + G_{C1.eq} \parallel G_{C2,eq} + G_{L,eq} = \frac{\omega C_v}{2Q_v} + \frac{\omega C_1}{2Q_{C1}} \parallel \frac{\omega C_2}{2Q_{vC2}} + \frac{1}{\omega L Q_L} \tag{A.7}$$

As shown in Chapter 2, the quality factor of the varactor is the lowest among all the passive components and given the presumption A.2, we can safely neglect the second term in equation A.7. Therefore, it reduces to

$$G_{TK} = \frac{\omega C_v}{2Q_v} + \frac{\omega C_1}{2Q_{C1}} \parallel \frac{\omega C_2}{2Q_{vC2}} + \frac{1}{\omega L Q_L} \approx \frac{\omega C_v}{2Q_v} + \frac{1}{2\omega L Q_L} = \frac{1}{2\omega L}\left(\frac{\omega^2 L C_v}{Q_v} + \frac{2}{Q_L}\right) = \frac{1}{2\omega L}\left(\frac{C_v}{(C_v + C_1 \parallel C_2)Q_v} + \frac{1}{Q_L}\right) \approx \frac{1}{2\omega L}\left(\frac{1}{Q_v} + \frac{2}{Q_L}\right) \approx \frac{1}{2\omega L}\frac{1}{Q_v} \tag{A.8}$$

The quality factor of the tank is given by

$$\frac{1}{Q} = \frac{1}{Q_v} + \frac{1}{Q_c} + \frac{1}{Q_L} \approx \frac{1}{Q_v} \tag{A.9}$$

The noise voltage contribution of the LC tank is given by:

$$S_{LC} = 4kTG_{TK}|Z(\omega_0 + \Delta\omega)|^2 = 4kTG_{TK}\frac{1}{4{G_{TK}}^2 Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 = \frac{kT}{G_{TK}Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{A.10}$$

Denote the active part contributes A times as much as the LC tank, the typical value of A ranges from 3 to 7, let's assume A=5 in this case. The noise contribution from the active part is given by:

$$S_{AP} = AS_{LC} = A\frac{kT}{G_{TK}\,Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{A.11}$$

The phase noise is therefore given by:

$$L(\Delta\omega) = \frac{1}{2}\frac{S_{LC}+S_{AP}}{v_s^2/_2} = \frac{(1+A)kT}{G_{TK}\,Q^2 v_s^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{A.12}$$

where v_s is the peak amplitude of the differential oscillation voltage seen across the LC-tank and we assume v_s =0.4V. From A.12, we can already tell that any increase in G_{TK}, Q or signal amplitude will improve the phase noise performance.

From the phase noise and signal swing requirements, we can get

$$L(1\text{MHz}) = \frac{(1+A)kT}{G_{TK}\,Q^2 v_s^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \le 10^{-8} \tag{A.13}$$

From A.14, we can write:

$$G_{TK} \approx \frac{1}{2\omega L}\frac{1}{Q_v} \ge \frac{6kT}{Q^2 v_s^2}\left(\frac{60*10^9}{1*10^6}\right)^2 * 10^8 = 14\text{mS} \tag{A.14}$$

$$L = \frac{1}{2\omega Q_v G_{TK}} \le 94.7\text{pH} \tag{A.15}$$

$$C_v = \frac{1}{\omega^2 L} - \frac{C_1*C_2}{C_1+C_2} \ge 49\text{fF} \tag{A.16}$$

This gives us a rough estimation for the selection of the passive component values. Note that in the above calculation, a fixed quality factor for the varactor is assumed. However, the quality factor of the varactor is a function of many design variables such as the finger numbers, the length and width of the fingers. Iterations need to be performed to converge to a realistic result. Last but not least, modifications are needed for the component values based on the post-layout simulation results since the parasitic capacitance will reduce the operating frequency, phase noise and tuning range. The selection of biasing current and transistor size, on the other hand, is based on an overall considerations and trade-offs of f_{cross} versus biasing current, noise factor, signal swing at the LC tank, phase noise, etc..

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