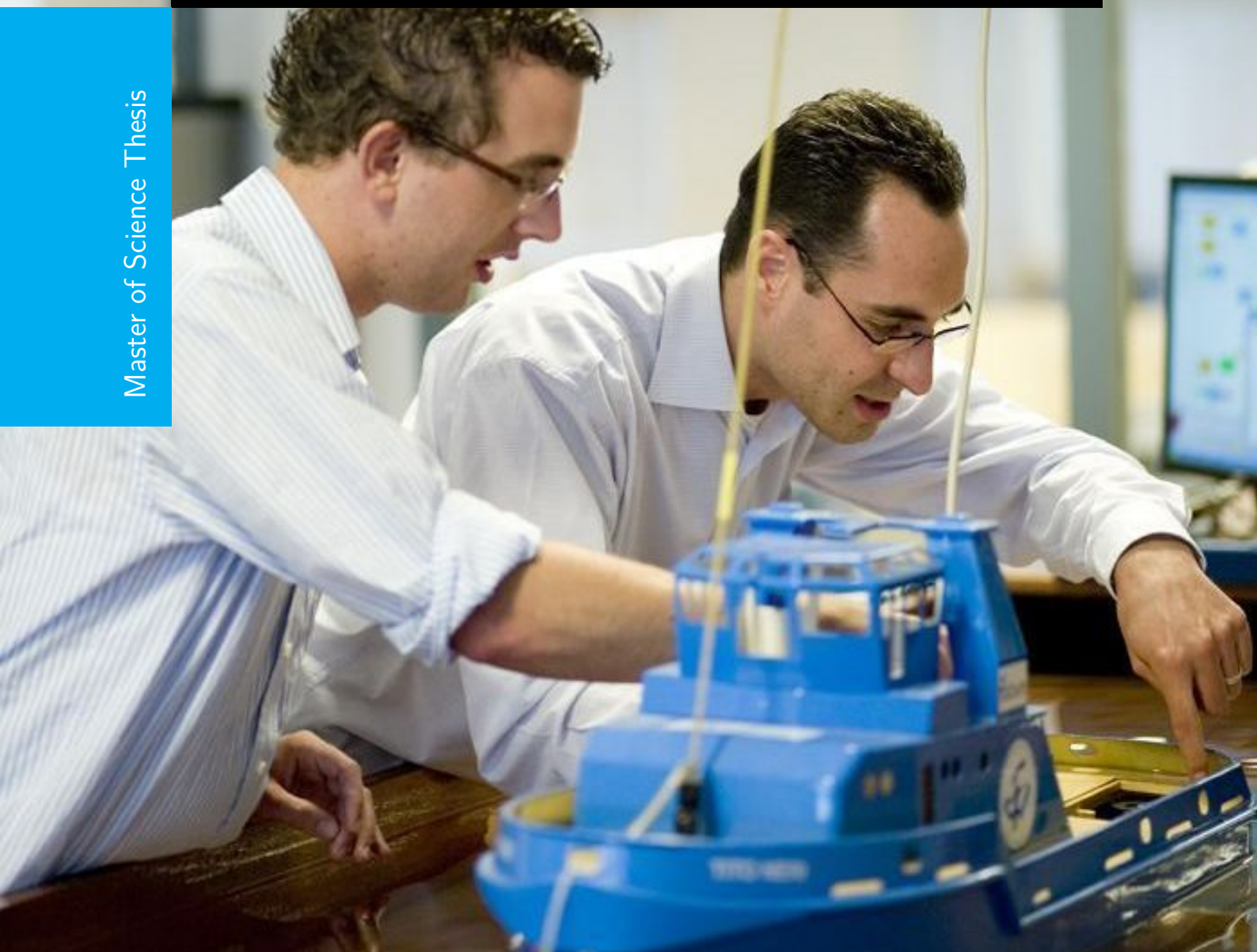


An Ultra-low power Direct Frequency Demodulator for Bluetooth Smart applications

Design and Implementation

Vijaya Kumar Purushothaman

Master of Science Thesis



An Ultra-low power Direct Frequency Demodulator for Bluetooth Smart applications

Design and Implementation

MASTER OF SCIENCE THESIS

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Faculty of Electrical Engineering, Mathematics and Computer Science (EEMCS)
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DELFT UNIVERSITY OF TECHNOLOGY
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MICROELECTRONICS

The undersigned hereby certify that they have read and recommend to the Faculty of Electrical Engineering, Mathematics and Computer Science (EEMCS) for acceptance a thesis entitled

AN ULTRA-LOW POWER DIRECT FREQUENCY DEMODULATOR FOR BLUETOOTH
SMART APPLICATIONS

by

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in partial fulfillment of the requirements for the degree of
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Abstract

This dissertation presents an ultra-low power (ULP) phase-domain RX architecture for the *Bluetooth Low Energy* (BLE) applications. By 2020, there will be up to 10 to 100 billion wireless sensor devices connected to internet-of-things (IoT)[1]. With the increasing demand on prolonging the battery lifetime, the power consumption of the RF transceivers for such applications has been dramatically reduced in the past few years [2][3]. However, the cost of replacing/recharging the batteries will become a bottleneck for massive deployment of the remote wireless sensors. Therefore, continuous innovation on power and supply reduction of the IoT RF transceivers is needed to extend the battery life time or one step further to achieve complete autonomous operation using energy harvesting.

A phase-domain single-channel RX, proposed in [4], transforms the analog-I/Q signal processing into digital-phase processing by combining a phase-rotator based phase tracking loop and the sliding-IF architecture. It demonstrates an approximately 40% power reduction compared to the conventional Cartesian RX architecture. However, it still requires multi-phase generation hardware and suffers from the image rejection issue. The proposed direct frequency demodulator (DIFDEM) RX has a zero-IF architecture and uses minimum possible analog circuitry, which allows it to avoid image issue and achieve low power consumption simultaneously.

Instead of phase rotator, the DIFDEM RX uses digitally controlled oscillator (DCO) as a feedback element in the phase tracking loop. Further, to meet tight adjacent channel rejection ratio (ACR) and frequency tolerance specifications of the BLE, DIFDEM employs a 3rd order elliptic filter and an automatic frequency noise cancellation (AFC) loop. Post layout simulation results indicate that DIFDEM RX can achieve -89 dBm sensitivity and -20/-30 dB ACR at 2/3 MHz, while consuming <1700 μ A current at 0.85 V supply. It also meets the BLE frequency tolerance specification of \pm 150 kHz.

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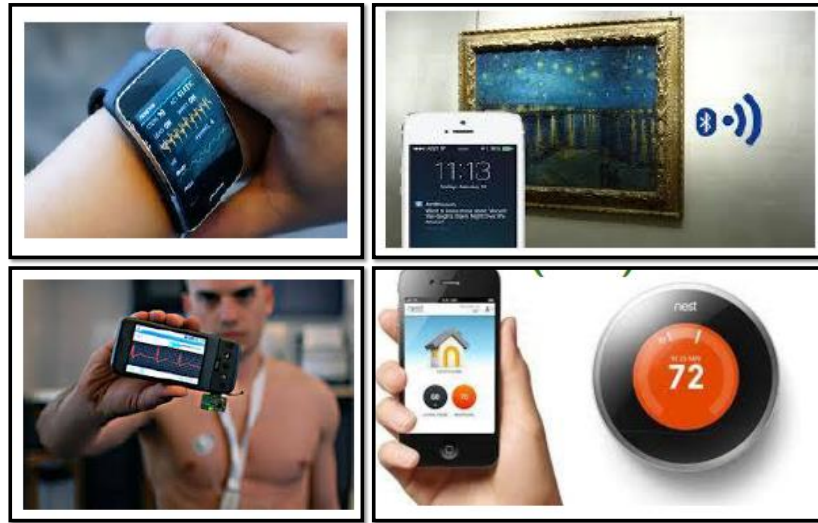
Chapter 1

Introduction

1-1 Motivation

Unimaginable advancement in information and communication technology in the last few decades has introduced numerous devices and applications that became integral part of our day-to-day life. Of these, wireless communication networks such as personal area network (PAN), body area network (BAN) and wireless sensor network (WSN) have redefined the term connectivity in the recent years. These communication networks together aim for ubiquitous wireless with large network of autonomous sensor nodes, enabling wide range of applications such as wearable smart devices for health and fitness, home and building automations and smart grids for monitoring, surveillance and disaster management (Figure 1-1). Apart from enhancing the performance of these devices, more emphasis is placed on improving their energy efficiency. As most of the devices are portable and battery-operated, improving their power efficiency increases the product lifetime and reduces the cost. On this front, several wireless standards such *Bluetooth Low Energy (BLE)/Bluetooth Smart* and *Zigbee* are proposed to achieve low power wireless connectivity. They use low data rates, low-complexity modulation schemes and short communication range to realize the low power implementations.

Power budget analysis of these wireless nodes would reveal that short-range radios (SRR), at the physical layer of these wireless standards, remain one of the bottleneck in achieving low power operation. Several commercially available BLE radios, like nRF24 series from Nordic Semiconductors and CC2541/CC2650 from Texas Instruments, consume >15 mW of power. Since most of the wireless nodes operate on batteries like 3.7 V Li-Ion, 1.5 V AA alkaline and 1.3 V Zn-air, which would provide at most a few hundreds of mAh, such high power consumption of transceiver would drastically reduce the lifetime of these nodes and consequently inhibit the growth of wireless markets [1]. Hence, improving energy efficiency of the short-range radios with high performance is one of the active area of research in analog and RF circuits.



Courtesy: <http://www2.imec.be>

Figure 1-1: Various applications of wireless-PAN/BAN.

1-2 Bluetooth Low Energy standard

Bluetooth Low Energy, as the name indicates, is a power-efficient variant of *Bluetooth*, developed to have ultra-low peak, average and idle power consumption. Operating in ISM band of 2.4 - 2.4835 GHz, BLE system uses frequency hopping technique to shift constantly between its 40 RF channels with centre frequencies at $2402+k*2$ MHz, where $k \in [0, 39]$. It transmits and receives the digital information, that are Gaussian frequency shift-keying (GFSK)-modulated at the rate of 1 Mbps with limited communication range of a few tens of metres. Further, relevant radio specifications of BLE standard, obtained from [14] are summarized in Table (1-1).

1-3 Thesis objective

On the direction of low power BLE receivers, several impressive works with high efficiency and performance can be seen in literature and some of them are compared here with commercial BLE radios in Table 1-2. These receivers, in general, use I/Q architecture to process the received signal in amplitude-domain and further, use the digitized amplitude to demodulate frequency information. This I/Q approach relies heavily on analog signal conditioning and matching between I/Q paths [19].

A non-conventional approach of digitizing the phase/frequency information directly from the radio frequency (RF) signal are getting attention in recent literature [4][18] for their high power-efficiency. Of these, [4] uses a novel phase-to-digital conversion (PDC) loop to track the phase/frequency-modulated signals by switching between multiple LO phases. Employing

Table 1-1: Summary of the relevant BLE receiver specifications.

Parameter	Specification
Operating frequency range	2.4 - 2.4835 GHz (ISM band)
Modulation	GFSK (BT = 0.5; modulation index = $0.45 < x < 0.55$)
Signal bandwidth	1 MHz
Data rate	1 Mbps
Sensitivity	<-70 dBm
ACR ($\pm 1/2/3$ MHz)	15/-17/-27 dB
Intermodulation	-50 dBm
Out-of-band blocking	-30 dBm
Frequency offset tolerance	
static offset	± 100 kHz
dynamic offset	± 50 kHz
maximum drift rate	400 Hz/ μ s

Table 1-2: Some examples for 2.4 GHz BLE receiver.

Parameter	Nordic nRF51822 [15]	TI CC2650 [16]	Dialog DA14580 [9]	ISSCC'15 [17]	TCAS'13 [18]
Sensitivity	-91 dBm	-96 dBm	-92.5 dBm	-94 dBm	-81.5 dBm
ACR ($\pm 2/3$ MHz)	25/51 dB	25/26 dB	20/30 dB	25/35 dB	17.6/30 dB
Maximum input	0 dBm	0 dBm	10 dBm	-5 dBm	-10 dBm
Supply voltage	3 V	3 V	3 V	1 V	1 V
Current consumption	13 mA	6.1 mA	4.3 mA	3.3 mA	1.1 mA
Frequency error tolerance	N.A.	350 kHz	N.A.	150 kHz	170 kHz
Technology	N.A.	N.A.	TSMC 55 nm	TSMC 40 nm	TSMC 130 nm

Table 1-3: Achieved and target specifications for PDC-based receiver.

Parameter	JSSC'14 [4]	Target
Standard	ETSI EN 300.400-1	BLE
Data rate	2 Mbps	1 Mbps
modulation	HS-OQPSK	GFSK
Supply voltage	1 V	0.85 V
Power consumption	2.4 mW	<1.8 mW
Sensitivity	-92 dBm	<-90 dBm
ACR ($2^{nd}/3^{rd}$)	-12/-17 dB	<-20/-30 dB
Technology	TSMC 40 nm	TSMC 40 nm

single-channel PDC loop, the receiver is shown to save up to nearly 40% of the total power consumption, compared to other conventional I/Q receivers [17][3].

The main objective of this thesis work is to adopt the PDC loop in the BLE receiver and reduce the overall power consumption. It is also known that, due to narrow channel spacing, BLE provides stringent adjacent channel rejection ratio (ACR) requirements compared to other 2.4 GHz ISM standards. Hence, to achieve high sensitivity and selectivity performance, the behaviour of PDC loop is analysed in detail and block-level specifications are derived in the first part of this work. Using the derived specifications, the receiver blocks are designed in the latter part of this work. The target specifications for this PDC-based receiver is given in Table (1-3).

1-4 Thesis outline

The thesis is divided into six chapters. Chapter 2 begins with an overview of commonly used frequency shift keying (FSK)/GFSK demodulators and receiver architectures. As the focus of the thesis is to design an ultra-low power receiver, more importance is given to the circuit techniques employed in the state-of-the-art radios to reduce power consumption. In the later sections of the chapter, a novel PDC based receiver [4], the basis of this thesis work, is studied with more focus on its power consumption. Lastly, a modified zero-IF PDC-based receiver is proposed to achieve higher energy efficiency and simultaneously meet the specifications of the BLE standard.

The dynamics of PDC loop are studied in the first half of the Chapter 3. The transient behaviour of the loop is explained using a phase-time representation of the signal at every node of the loop. Further, loop characteristics, such as response time, steady-state behaviour and stability, are discussed with simulation results. System-level performance analysis of zero-IF phase-to-digital conversion based receiver is carried out in second half of Chapter 3. Parameters, such sensitivity, selectivity and frequency-offset tolerance are analysed and block-level specifications, are derived using MATLAB simulations for the target performance.

Chapter 4 describes the circuit-level implementation of analog and digital blocks, used in the zero-IF PDC based receiver. Optimization of design parameters, such as noise, linearity and power for analog blocks – mixer, lowpass filter and opamp – are elucidated with relevant equations and trade-off considerations. The last section of the chapter discusses the

implementation details of an automatic frequency noise cancellation (AFC), a digital block to cancel frequency offsets and phase noise.

In Chapter 5, post-layout simulation results of the designed blocks – mixer, lowpass filter and AFC– are presented to describe their performance. Further, a short note on the reused blocks, such as low noise amplifier, comparator and digitally-controlled oscillator, are provided together with relevant post-layout simulation results. At the end of the chapter, results and bugs identified in the first tape-out and relevant fixes added to the second tape-out are reported in detail.

Finally, the overall summary, important conclusions drawn from this thesis work and potential areas of improvement for future work are mentioned in the Chapter 6.

Low power FSK/GFSK receivers

In this chapter, conventional frequency shift keying (FSK)/Gaussian frequency shift-keying (GFSK) demodulators employed in low power radios are reviewed first. Next, the low-power radio architectures adopted in ultra-low power (ULP)-*Bluetooth Low Energy* (BLE) radios are surveyed. Then, the low power circuit techniques exploited in these radios are summarized. At the end of this chapter, a novel direct frequency-to-digital converter adopted in this thesis work is introduced.

2-1 FSK/GFSK demodulators

As described in Chapter 1, BLE standard is designed to address several ULP wireless-personal area network (PAN)/body area network (BAN) applications [2]. In these applications, BLE radios are typically powered by a small, coin-cell batteries (for example 1.3 V Zinc-air) and could consume almost 90% of the total battery energy [3]. Recently, there have been several publications in the field of ULP-BLE transceivers addressing power/energy-efficiency while maintaining high sensitivity [9][11][4][3][2]. One such receiver, implemented in [4], employs a novel phase-to-digital conversion (PDC) to extract phase and frequency information from the input signal directly in the phase domain. Since, the scope of this thesis work includes analysis and implementation of this PDC, for better understanding, a few conventional FSK/GFSK demodulators available in the literature are discussed first in this section.

2-1-1 Zero-crossing detectors

Frequency discrimination using zero crossing detection is based on the principle that the instantaneous frequency of the input signal can be determined by estimating the number of zero crossings in it in a specified interval of time. Figure 2-1 shows a zero-crossing detector implemented in [5].

A hard limiter is often employed at the first stage of zero crossing detection to convert the input signal to a frequency modulated pulse train. It is followed by either a differentiator

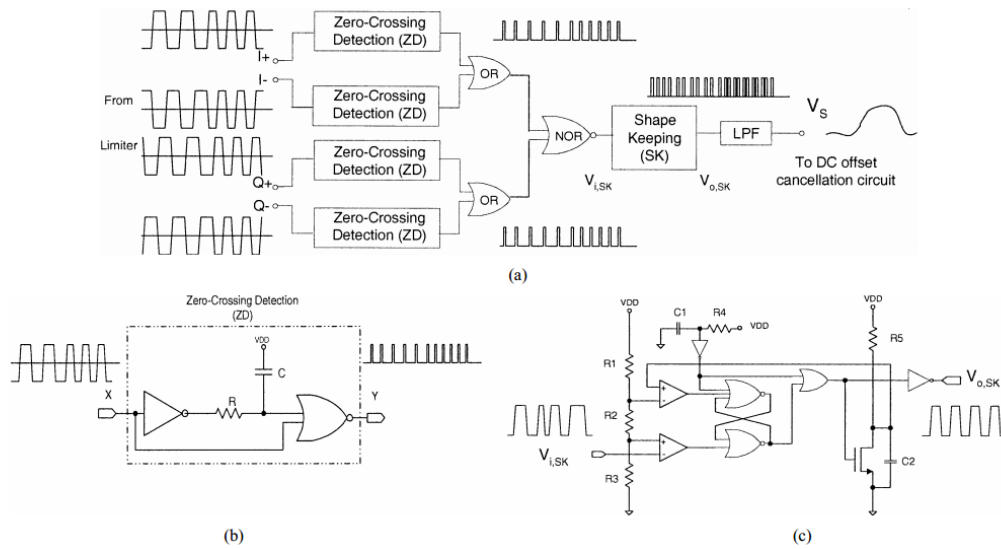


Figure 2-1: (a) Zero-crossing detector. (b) ZD one shot. (c) SK one shot [5].

[20] or one-shot circuit [5] that generates pulses when zero-crossing occurs at the signal. The pulse output is, later, shaped and averaged using low pass filter to determine the frequency information. Zero-crossing detector is employed after the down-conversion of RF signal and channel filtering. The power consumption and performance of limiter, differentiator and one shot circuits in the zero-crossing detector largely depends on the frequency of the down-converted IF [8].

2-1-2 Quadrature correlator

Quadrature correlator extracts phase/frequency information from in-phase and quadrature-phase (I/Q) signals using differentiator or delay elements [6][21][22]. FSK-modulated I/Q signals are limited and differentiated in continuous time domain [6]. The differentiated in-phase signal is multiplied with quadrature phase and vice-versa. These products are then linearly combined to produce an output signal whose magnitude is proportional to the instantaneous frequency of the I/Q signal. In certain implementations [6][21], low pass filters are employed after linear combination to remove any higher harmonics present in the output because of hard limiting or multiplication. Figure 2-2 shows the block diagram of continuous time domain quadrature correlator implemented in [6]. Discrete time implementations use delay elements in the place of differentiators [22].

2-1-3 Phase-domain ADC

The concept of phase domain ADC was first introduced in [23] as zero-IF zero-crossing demodulator (ZIFZCD). In GFSK modulation, the data are coded in frequency domain. This

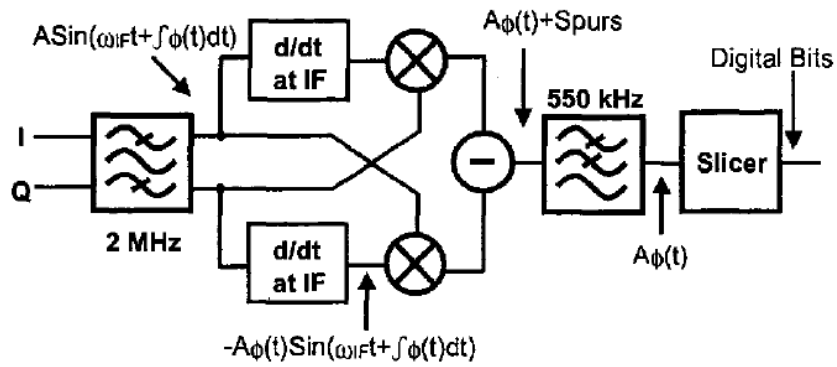


Figure 2-2: Quadrature correlator [6].

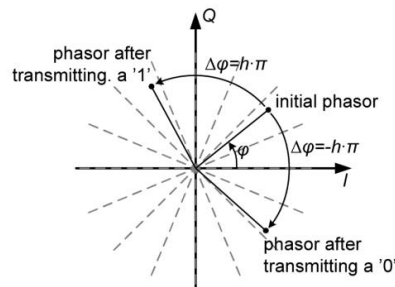


Figure 2-3: GFSK modulation with a modulation index 'h' in the complex plane [7].

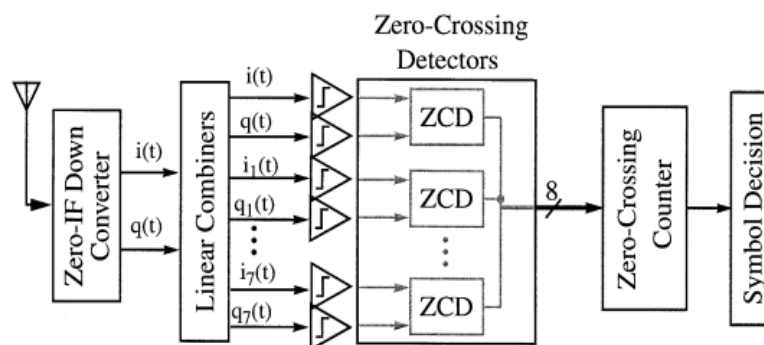


Figure 2-4: Phase domain ADC [8].

can be visualized in the complex plane, as the direction of rotation of constant magnitude phasor around the origin. The clockwise rotation of the phasor corresponds to bit '0' whereas anti-clockwise rotation correlates to bit '1' [Figure 2-3]. ZIFZCD generates multiple phase-rotated versions of I/Q signals and detects the time and direction of their zero-crossings. The cumulative number of clockwise and anti-clockwise zero crossings are used to determine the actual transmitted data.

Unlike ZIFZCD, [7] and [8] use the zero crossings of phase-rotated I/Q signals to obtain quantized phase of the received signal and post-process it to estimate transmitted data [Figure 2-4]. It is shown in [8] and [18] that GFSK demodulators, based on phase ADCs, are robust and power-efficient and consume as low as 190 μ W of power.

2-1-4 Digital demodulation

Several low power BLE receivers [9][3][2][24] employ digital baseband (DBB) to perform FSK/GFSK demodulation. Unlike analog demodulators, digital demodulators offer faster processing capabilities at low-power and low-cost. In addition to that, their design flexibility and portability across technology nodes make them preferable choice in any low-power implementation.

Digital demodulators use diverse techniques (like CORDIC and Matched correlators) to perform frequency demodulation. CORDIC (COordinate Rotation DIgital Computer) is one of the most widely adopted techniques [25] in digital demodulation because of their simple hardware. It uses an iterative algorithm based on simple shift-add operations to directly calculate phase of I/Q signals. In [3] and [26], a differential detector (also called as digital quadrature correlator) is employed to extract phase difference data from I/Q digital signals. The phase difference information is then processed by decision/maximum correlation blocks to decode the FSK input.

2-1-5 Phase locked loop demodulator

A phase locked loop (PLL), in its locked state, maintains constant phase difference between the output signal and the reference input signal. From the block diagram of PLL, shown in Figure 2-5,

$$\phi_{in}(t) = \phi_{div}(t) + \mathbf{C} \quad (2-1)$$

where \mathbf{C} is a constant. If $N = 1$ in Figure 2-5 then, $\phi_{div}(t) = \phi_{out}(t)$. Substituting it in Equation(4-27) and differentiating it further would result,

$$\frac{d\phi_{in}(t)}{dt} = \frac{d\phi_{out}(t)}{dt} \quad (2-2)$$

Equation (2-2) confirms that PLL output will track the frequency of input signal. In the case of frac-N/integer-N PLL, output frequency ($d\phi_{out}(t)/dt$) and the input frequency ($d\phi_{in}(t)/dt$) are different and related by the divider ratio, N . This property enables the PLL to act as a FSK demodulator.

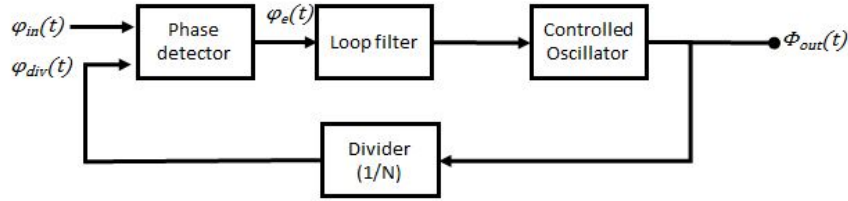


Figure 2-5: Block diagram of PLL.

Let us consider that a frequency-modulated signal is applied to the input of PLL. In order to maintain the locked state of PLL, the frequency of the oscillator should track the frequency of the input signal. Since it is known that frequency of the oscillator is proportional to the control signal applied to the oscillator input [voltage in case analog-PLL, tuning word in case of All-digital PLL], the control signal will provide the demodulated signal.

The phase domain linear model of PLL, shown in Figure 2-6, delineates the frequency modulation input, $M(s)$ and demodulated output signal, $V_c(s)$. The model represents analog-PLL, in its locked state and contains the transfer function of the blocks shown in Figure 2-5. In phase domain, phase detector (PD) is represented by a gain element K_{PD} (rad/V), loop filter by $F(s)$ (V/V) and voltage controlled oscillator (VCO) by K_{VCO}/s (rad/V).

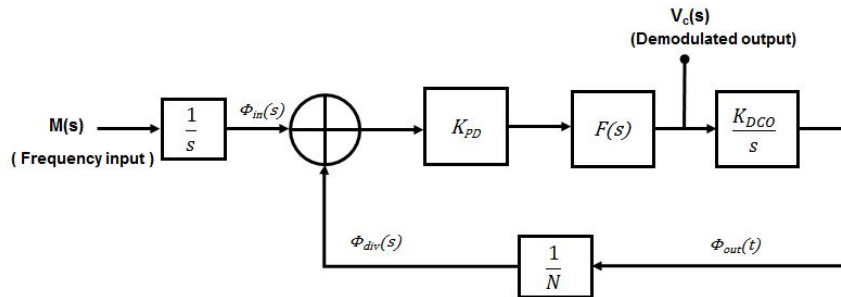


Figure 2-6: Phase-domain linear model of PLL.

Employing linear feedback analysis, the relationship between $V_c(s)$ and $M(s)$ can be derived as,

$$V_c(s) = M(s) \times \frac{K_{PD}F(s)}{s + K_{PD}F(s)K_{DCO}} \quad (2-3)$$

The closed loop transfer function of the PLL can be given as,

$$H(s) = \frac{K_{PD}F(s)K_{DCO}}{s + K_{PD}F(s)K_{DCO}} \quad (2-4)$$

Substituting this in Equation 2-3 gives,

$$V_c(s) = \frac{M(s)H(s)}{K_{DCO}} \quad (2-5)$$

Equation(2-5) states that frequency input signal is filtered by closed-loop transfer function of PLL and scaled by VCO gain to obtain demodulated output. This leads to an important condition that PLL bandwidth need to be larger than the input signal bandwidth for efficient demodulation. Wider loop-bandwidth in PLL also reduces the effect of PD distortion at the output [27]. Presence of K_{VCO} in the transfer function implies that low VCO gain is required for high demodulation sensitivity. However, low VCO gain limits the PLL tunability range and makes it susceptible to PVT variations.

Many examples of FSK demodulators using PLL are available in literature [28]. Specifically, a Bluetooth receiver that adopts PLL for GFSK demodulation is reported in [29]. In [30], a stand-alone FSK demodulator employs PLL with two mutually exclusive loops, a fine and a coarse tuning loop, to achieve high demodulation sensitivity and wide tunability simultaneously.

Besides conventional PLL, an alternative $\Sigma\Delta$ -DPLL architecture was introduced in [31] to perform FSK demodulation and digitization simultaneously. Usually a coarse A/D conversion is employed at the output of DPLL based demodulators for frequency digitization. The $\Sigma\Delta$ -DPLL demodulator in [31] employs oversampling and noise shaping to minimize the quantization errors that are introduced in demodulated DPLL output due to coarse A/D conversion. This increases the resolution of frequency digitization.

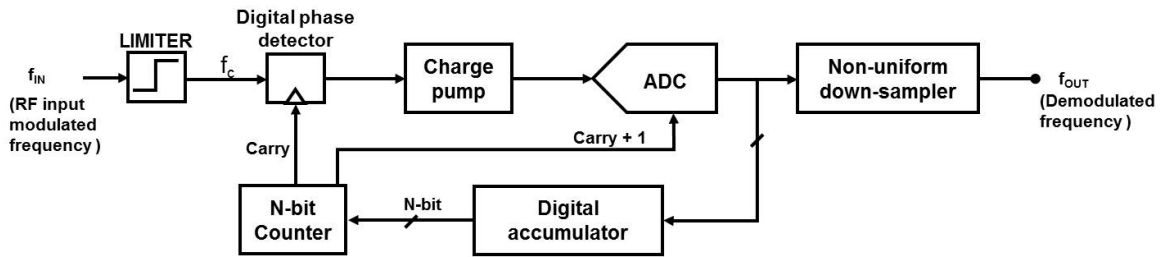


Figure 2-7: $\Sigma\Delta$ -DPLL based demodulator.

$\Sigma\Delta$ -DPLL based demodulator, as shown in Figure 2-7, uses a counter as a local oscillator (LO) phase controller and thereby eliminating the slow frequency drift of the oscillators. It is to be noted that $\Sigma\Delta$ -DPLL based demodulator uses 'carry + 1' signal from the counter to sample the charge pump output. This 'carry + 1' signal is input data dependent and causes non-uniform sampling. An additional non-uniform-to-uniform decimator is implemented in [31] to produce uniform samples for further signal processing. This unnecessary complication in digital hardware circuitry compromises the use of $\Sigma\Delta$ -DPLL for frequency demodulation.

2-2 Low power I/Q receivers

Conventional FSK/phase shift keying (PSK) receivers [5][6][9][2] use Cartesian I/Q structures (heterodyne/homodyne) for their RF and analog front ends. These I/Q structures enable complex-domain signal processing and conveniently adopts power-efficient demodulators. It also prevents self-corruption of asymmetric FSK/PSK signal during down-conversion in zero-IF receivers. Two parallel signal paths (in-phase and quadrature phase) require separate circuitry for down-conversion, filtering and analog-to-digital conversion. To achieve low power

operation, these I/Q structures are mostly realized as low-IF [9][11][24], sliding-IF [2] [3] and zero-IF [18] architecture. Along with these architectures, several low-power circuit techniques that are usually adopted in state-of-the-art transceivers are discussed next.

2-2-1 Architectures

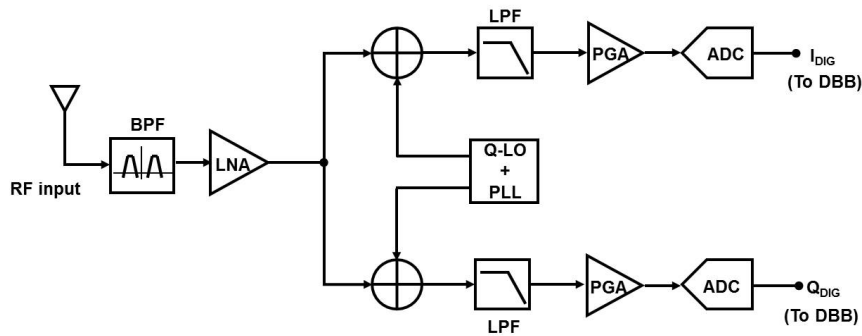


Figure 2-8: Zero-IF architecture.

Shown in Figure 2-8, is an example of zero-IF architecture that down converts the input RF signal directly to the baseband. Due to zero-IF, the architecture does not require additional image filters in the signal path. Simple LPFs are used to suppress interferers and higher harmonics. ADCs and DBB operate at baseband frequencies close to DC. All these attributes make zero-IF more power-efficient than both low-IF and sliding-IF. In addition to that, high level of integration and digitization are possible in zero-IF receivers.

Despite these benefits, use of zero-IF architectures is limited by its inherent DC-offsets and flicker noise problems. DC offsets, specific to zero-IF architecture, are due to the phenomenon of 'self-mixing' [19][32]. Here, strong LO signals will leak into the RF inputs of low noise amplifier (LNA) and mixer due to finite isolation between them and LO port. This leaked LO signal at the RF port of the mixer mixes with the LO signal and produces unwanted DC components at mixer output. High pass filtering (analog domain) [18] and DC offset cancellation (digital domain) are the most common techniques used to address the DC offsets. Along with DC offsets, flicker noise is becoming a prominent issue in deep submicron CMOS technologies, as it causes considerable SNR degradation in the zero-IF receivers. Though, it can be reduced by using large transistors in the baseband circuits, it is achieved at the cost of increased power consumption.

Low-IF architecture (Figure 2-9) avoids DC offset completely and flicker noise partially that are witnessed in zero-IF architectures, by selecting a non-zero IF. In this case, typical IF is twice the signal bandwidth. Low-IF architecture requires additional circuitry to filter the unwanted signal at image frequency. In I/Q receivers, IF image rejection is generally realized either in analog domain (RF polyphase and IF complex bandpass filters) or digital domain [33]. Especially, receivers, implemented in [9][11][24], employ complex filters that have asymmetrical frequency response as shown in Figure 2-10. This asymmetrical frequency response is synthesized by employing frequency translation technique on low-pass filters [34]. Besides finite filter stop-band rejection, image rejection in low-IF is further limited by mismatches

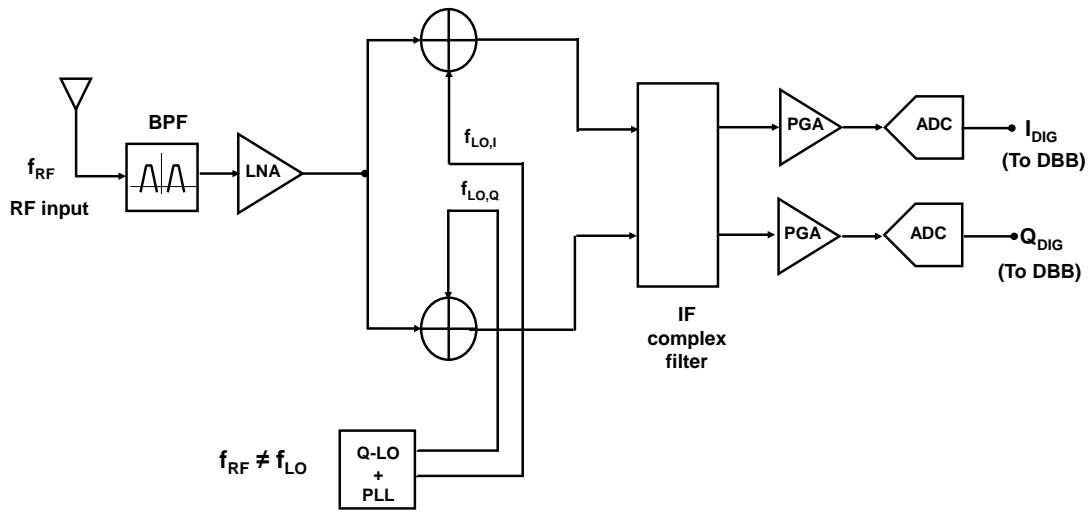


Figure 2-9: Low-IF architecture.

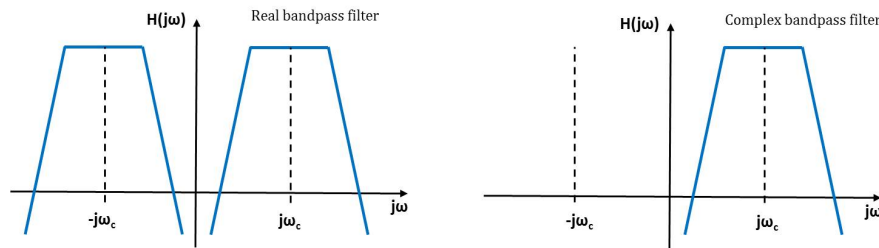


Figure 2-10: Real and complex filters.

between the I- and Q- paths [33]. It is to be noted that power consumption of complex filters is usually higher than that of low-pass filters and it increases with IF. Hence, compared to zero-IF, low-IF has slightly higher design complexity and may consume more power.

Sliding-IF architecture is another architecture that is gaining popularity among low-power RF designers [2] [3]. It performs two-stage down-conversion in which second LO is derived from the first LO by frequency division (Figure 2-11). In both zero-IF and low-IF receivers, quadrature phases (RF or LO) are generated at very high frequencies and hence receiver consumes large power. Moreover, even a minor layout/load difference in I/Q paths would result in a significant I/Q mismatch at these high frequencies affecting the receiver performance. However, in sliding-IF architecture, the problem of I/Q mismatch and quadrature generation are greatly reduced by generating quadrature signals at lower frequencies. It also makes them less susceptible to DC-offsets due to self-mixing. Besides its advantages, it should be noted that additional mixers, LO buffers and frequency dividers increase the design complexity and area.

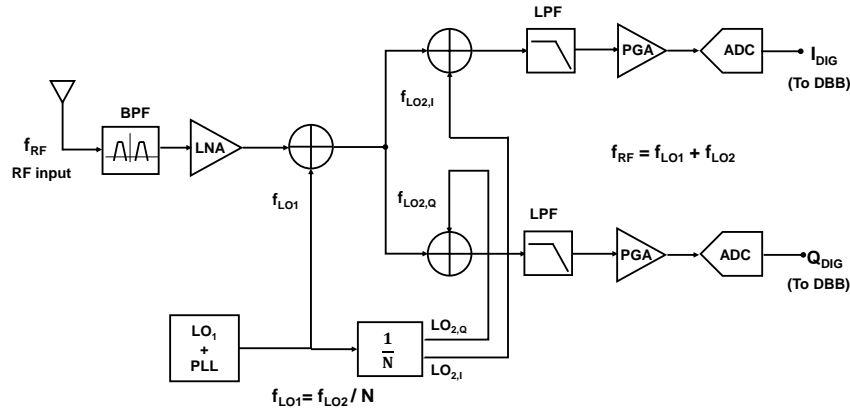


Figure 2-11: Sliding-IF architecture.

Considering only at the system level, it is difficult to select one architecture over the other for low power consumption, small chip area and high performance. The performance of these architectures largely depends on implementation of individual blocks (LNA/mixer/quadrature-VCO). For example, (a) sliding-IF RX in [3] has achieved high sensitivity (-98 dBm) at low power by running VCO at a frequency lower than the input RF and generating quadrature LO at a much lower frequency; (b) low-IF RX in [10] employs a single stage LNA, mixer and quadrature-VCO (LMV) cell to achieve sub-mW operation. Hence, in the next section, we briefly discuss the circuit techniques that are adopted in some of the state-of-the-art BLE receivers to achieve high performance and low power consumption.

2-2-2 Circuit techniques

High gain along with low noise is the desired LNA characteristic and is usually achieved using a single-ended [3][2] or differential [9] cascoded structure with a tunable integrated LC load (Figure 2-12). Considering their high power consumption ($\sim 25 - 30\%$ of RX power), in certain receiver implementations, LNAs are: (a) removed from the signal chain [18]; (b) operated at low supply voltage [11]; and (c) replaced with LMV cells [10] to minimize RX power at the cost of reduced sensitivity. In a LMV cell, LNA, mixer and quadrature-VCO are stacked one over the other and share same bias current without extra voltage headroom (Figure 2-12).

Current-driven passive mixers [18][24] and switched transconductor mixers [9] are used for their high gain and linearity at low power. To further reduce power consumption, switched transconductors (Figure 2-13) are operated at supply voltages as low as 0.6 V [11]. In the case of sliding-IF receivers [3][2], an active RF mixer is used along with quadrature passive IF mixers. To increase the gm/I efficiency and reduce the mixer noise, push-pull structure with a common-mode feedback (CMFB) is adopted in the RF mixer [3].

Active op-amp-RC [11][18][3] and gm-C [10] structures are used to implement complex band-pass filters and real low pass filters. They are usually combined with programmable gain

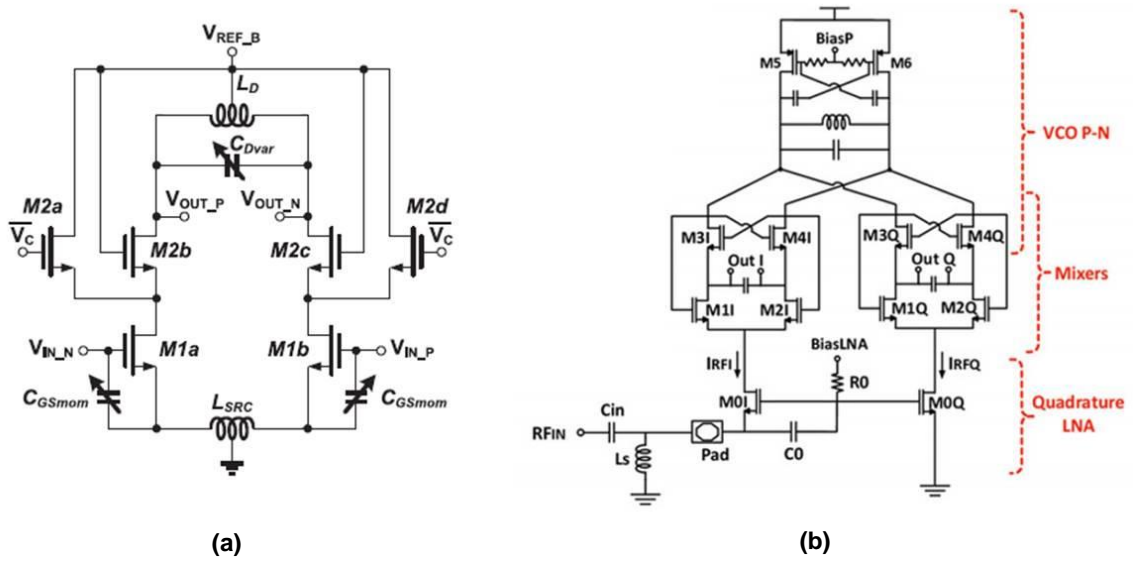


Figure 2-12: (a) Differential-ended LNA [9]. (b) LMV cell [10].

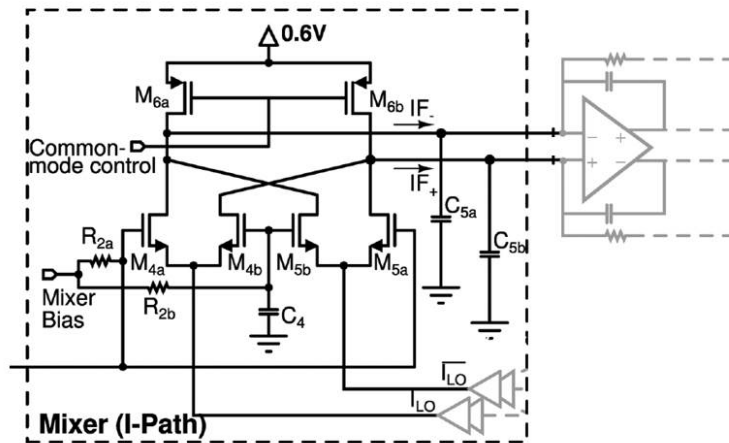


Figure 2-13: Switched transconductors [11]

stages to cover wide dynamic range [9][2]. SAR-analog-to-digital converter (ADC)s and digital demodulators are preferred for their high power efficiency [9][3]. However, BLE receivers designed in [18][24] employ phase-ADCs to directly quantize the phase from the I/Q signal. Stacked LO buffers [9] and polyphase filters in RF signal path [24] are other notable circuit techniques employed to reduce power consumption during quadrature LO generation.

2-3 Phase tracking receivers

Generally I/Q receivers process the input signal in amplitude domain. They employ ADCs in I/Q paths to digitize the amplitude information of the input signal and extract the relevant phase information using digital signal processing. Since FSK/PSK type modulations modulate data only on the frequency or phase of the carrier, demodulating phase or frequency directly could help simplifying the receiver implementation.

Though phase-ADCs [7] and quadrature correlators [22] determine the phase/frequency information without amplitude digitization, they employ I/Q architectures and provide no design simplification. In contrast, receivers that employ PLL or other similar demodulators [31] would require only single channel and could result in lower design complexity. Since PLL tracks the phase of the input signal, these receivers can be called as phase-tracking receivers.

Phase-tracking receivers are quite prevalent in the literature [28][35][30] and are often discussed as an important application of PLL in [27]. However, digital demodulators are often preferred over PLL-based phase-tracking receivers for their flexibility and adaptability [22]. Recently, a phase-tracking receiver employing a novel phase-to-digital conversion loop is published in [4]. Like PLL, PDC loop tracks the phase of the input signal by continuously switching to one of its pre-generated LO phases. It is reported that the receiver consumes only 2.4 mW with state-of-the-art sensitivity of -92 dBm. In the next section, the receiver is described in detail as it forms the basis for this thesis work.

2-3-1 Sliding-IF phase-to-digital converter

As described in Section (2-1-5), PLL tracks phase/frequency of the input signal and can be used as a frequency/phase demodulator. In [4], PLL behaviour is emulated using a mixer as phase detector, a low-pass filter as loop filter and a phase rotator as oscillator. Phase rotator is composed of a digital accumulator and a phase selector. Unlike usual PLL, low pass filter (LPF) output in this PLL is digitized using 1-bit ADC (comparator) before transferring to phase rotator. From the linear analysis of the PLL, the digitized LPF output is proportional to demodulated frequency information and the integrator in phase rotator provides digitized phase information. In concise, this loop performs direct phase-to-digital conversion. Figure 2-14 illustrates this account of PDC loop.

Employing mixer as analog phase detector enables the PDC loop to accommodate strong interferers. These strong interferers are later filtered by stop-band attenuation of LPF and capture-effect of comparator in the PDC loop so that demodulated phase/frequency data is least corrupted. Thus, analog phase detector, LPF and comparator together address the selectivity conundrum commonly seen in PLL-demodulators. Furthermore, 1-bit quantization after LPF cancels the effect of amplitude-dependent phase-to-voltage conversion at analog

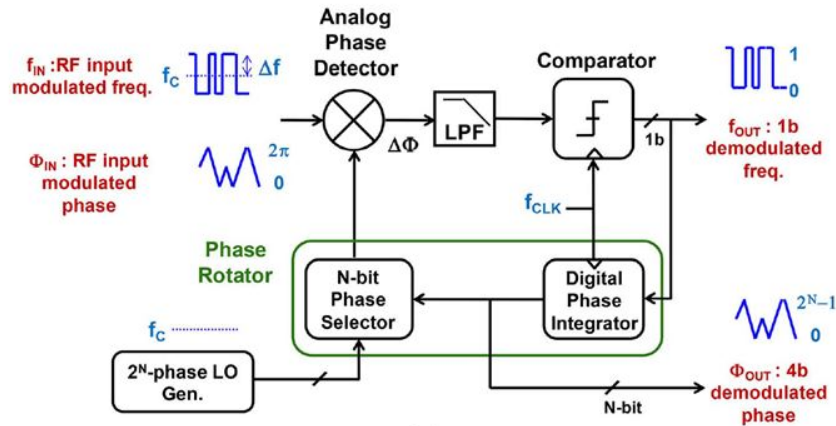


Figure 2-14: Phase-to-digital conversion loop [4].

phase detector and makes the loop more-tolerant to amplitude fluctuations. By employing this feature, PDC increases the dynamic range of receiver, it is embedded into.

Oscillator in the PLL generates output phase proportional to the integral of LPF output. The output phase is compared with incoming input phase at phase detector. Phase rotator produces similar oscillator behaviour using: (i) digital phase integrator – it integrates/accumulates the digital LPF output; (ii) phase selector – based on integrator output, it selects one of the 16 LO phases generated using another PLL output and frequency dividers. Phase selector and multi-LO phase generator are together termed as Digital-to-phase converter (DPC). LO phases are generated using a separate PLL. Consequently, PDC and PLL bandwidth can be optimized independently for fast signal demodulation and low VCO phase noise.

Generating multiple LO phases at RF poses a big threat to low power operation. Hence in [4], sliding-IF architecture (divide-by-8) is incorporated into the PDC. Thanks to sliding-IF plan, LNA and RF mixer simply down-convert the RF input signal and IF mixer acts as the analog phase detector in the PDC loop. Since phase detector operates with an IF input, multiple LO phases are generated at IF and thereby effectively consumes less power than the earlier PDC loop.

The complete block diagram of receiver with sliding-IF PDC proposed in [4] is shown in Figure 2-15. It is implemented in 90 nm CMOS technology and designed to operate in 2.4 GHz ISM band.

2-3-2 Proposed zero-IF phase-to-digital converter

Since one of the objective of this work is to improve the energy efficiency of the sliding-IF PDC based receiver, the scope for power reduction is identified and discussed in this section.

Table 2-1 lists out the power consumption of each block implemented in the sliding-IF PDC [4]. From the table, we identify that RF circuits (LNA + RF mixer) consume 42% of the total power and core PDC loop, comprising of IF mixer, LPF and DPC, consumes 38% of the

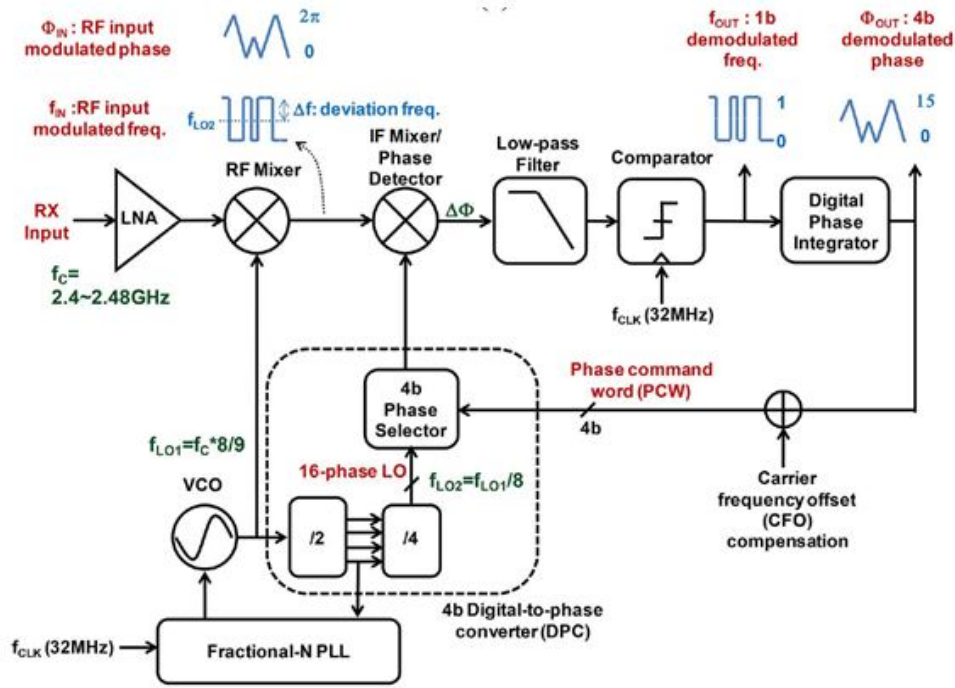


Figure 2-15: Sliding-IF PDC receiver [4].

Table 2-1: Power consumption of blocks in the sliding-IF PDC based receiver [4].

Circuit blocks	Power (μW)
LNA + RF mixer	1050
PD + LPF	400
DPC	500
VCO	300
Charge pump + Others	200
Total	2450

total power. Including the consumption of oscillator and PLL would increase the total power consumed by PDC loop and its auxiliary circuits to $1350 \mu\text{W}$ (55% of the total receiver power).

On sifting through the sliding-IF PDC receiver at system level, following components are identified as essential to the receiver:

- IF mixer along with LPF, comparator and phase rotator, forms the core of the PDC loop.
- Low noise amplifier is essential to achieve high sensitivity. By providing low noise and high gain, it improves the overall noise figure of the receiver and also suppresses the out-of-band blockers.
- Low pass filter is the only block in the sliding IF-PDC receiver that addresses in-band linearity. It filters the strong adjacent and alternate channel interferers after down-conversion.

RF mixer is employed only to facilitate sliding-IF conversion which in turn was adopted to reduce power consumption during multiple LO phase generation. PLL and VCO are used to produce the desired LO signal.

Since the phase rotator in the PDC loop behaves like an oscillator in the PLL, it can be easily replaced with digitally controlled oscillator (DCO), without inducing any drastic changes in the system behaviour. Linear models, employed in [4] to represent phase-rotator, further ratify the DCO replacement. As DCO is capable of providing phase output at RF at low power, it helps to realize the zero-IF PDC without resorting to power-hungry dividers. Moreover, RF mixer, PLL and VCO, employed in sliding IF-PDC, are not required in zero-IF PDC. Hence, the energy-efficiency of the zero-IF PDC receiver could be higher than that of sliding-IF PDC.

Though DCO improves the energy-efficiency of the receiver, the sensitivity and selectivity performance of the receiver would be affected by inherent oscillator non-ideal characteristics like phase-noise, slow frequency drift, limited resolution, limited tuning range and voltage swing. Problem of limited voltage swing can be easily avoided by: (a) employing DCO buffers - to achieve rail-to-rail voltage swing; (b) switching mixers - to minimize the effect of DCO amplitude on the mixer output. As the receiver is intended to operate in 2.4 GHz ISM band ranging between 2.401 GHz - 2.483 GHz, it is implicit that DCO covers this frequency range. Furthermore, this frequency range in DCO is quite achievable and it is shown in several state-of-the-art transceivers and ADPLLs [3][36].

In the PDC loop, the DCO tracks the phase of the RF input signal by altering its oscillating frequency. At any point of operation, efficient phase-tracking is achieved when the lowest DCO frequency step/resolution is at least equal to 0.5 times the instantaneous frequency deviation. Since the frequency deviation is 500 kHz in the BLE standard, it is necessary that the DCO achieves a resolution much higher than 250 kHz [14]. Later in Chapter 3, it will be shown that even higher resolution is required to address varying frequency offsets and also, a digital interface is needed between comparator and DCO, to dynamically adjust the DCO frequency step.

Setting any specifications for the DCO phase noise and slow frequency drift requires detailed analysis of its impact on receiver performance. Hence, it is discussed with the aid of MATLAB

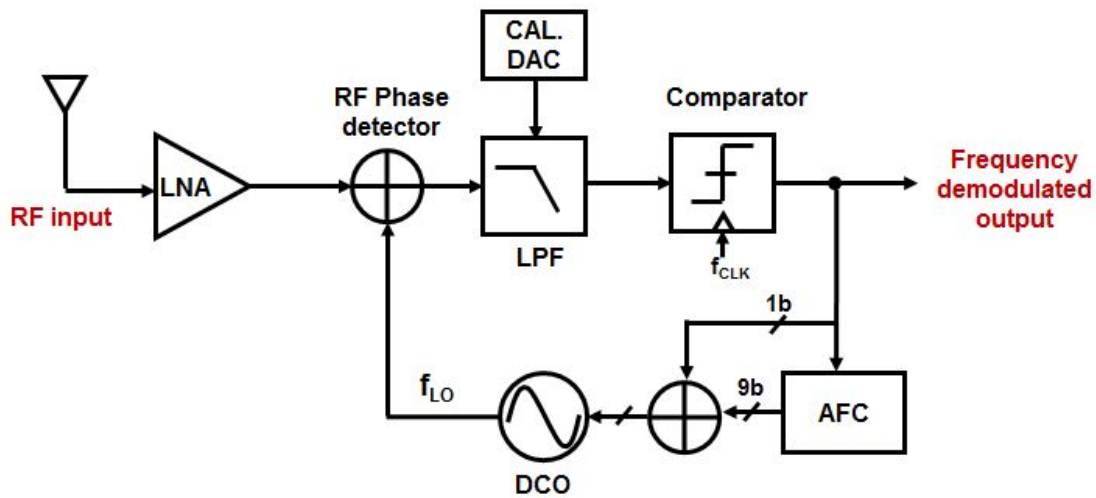


Figure 2-16: Proposed zero-IF phase-to-digital conversion based receiver.

simulations in the next chapter. However, for an architectural overview, an additional mixed-signal feedback loop is implemented along with the existing zero-IF PDC loop to minimize the effect of slow frequency drift along with varying frequency offsets. This loop facilitates LO carrier recovery directly from the received RF signal.

The top-level block diagram of the proposed zero-IF PDC based receiver is shown in Figure 2-16. Since this receiver performs direct frequency demodulation from the RF signal, it will be also referenced as direct frequency demodulator (DIFDEM) in this work. Compared to sliding IF-PDC and other I/Q receivers, it has lesser number of components. Besides the components described earlier, there are two new blocks in the DIFDEM: (a) automatic frequency noise cancellation (AFC) block and (b) DC offset calibration-DAC.

- AFC block along with PDC core forms the digital feedback loop. It is implemented in digital domain and employed to cancel the carrier frequency offsets due to dirty transmitter and the slow frequency drift of the DCO.
- As the name indicates, calibration-DAC is used to maintain the DC Offset within the limit identified during system analyses.

Zero-IF PDC is a system-level approach towards high energy-efficiency phase-tracking receivers. For maximum energy efficiency possible, circuit-level innovations are needed as well. Though, zero IF-PDC has fewer components, optimizing every one of them for low power is a task beyond this thesis time-frame. Hence, in this design, some of the blocks are re-used from previous designs. Further, according to the conclusions achieved through system analyses in Chapter 3, certain blocks are completely re-designed. These circuit blocks, along with the re-used ones, are discussed in Chapter 4 and Chapter 5. Finally, the entire receiver is designed to operate at a supply voltage of 0.85 V.

System analysis and design

The behaviour of phase-to-digital conversion loop will be studied in the first part of the chapter. Attributes such as response time, stability and steady-state conditions will be analysed in detail. The second part of the chapter is dedicated for system-level understanding of the receiver performance and obtaining block-level parameters to meet the target specifications.

3-1 Linear s-domain model of the PDC

Similar to a phase locked loop (PLL), the proposed zero-IF phase-to-digital conversion based receiver is inherently a non-linear system. Presence of comparator in the phase-to-digital conversion (PDC) loop only consolidates this assertion further. Despite being non-linear, most of the PLLs are described very well using linear models and transfer functions, when they are in the locked state and the phase error is very small [27]. A similar transfer-function based approach is used in [4] to model the frequency response of the PDC loop.

The approximated phase-domain linear model, used in [4], is shown in Figure 3-1 and the derived signal and noise transfer functions (STF and NTF) are given below:

$$STF = \frac{f_{out}(s)}{f_{in}(s)} = \frac{A \cdot K_{PD} \cdot K_{LPF}(s) \cdot K_{CMP}}{s + A \cdot K_{PD} \cdot K_{LPF}(s) \cdot K_{CMP} \cdot K_{DCO}} \quad (3-1)$$

$$NTF = \frac{f_{out}(s)}{f_{qn}(s)} = \frac{s}{s + A \cdot K_{PD} \cdot K_{LPF}(s) \cdot K_{CMP} \cdot K_{DCO}} \quad (3-2)$$

Here, f_{in} and f_{out} are the modulated input frequency and the digitized output frequency, $K_{LPF}(s)$ is the transfer function of low pass filter (LPF) and K_{DCO}/s is the gain of the digitally controlled oscillator (DCO) in phase domain. The non-linear behaviour of phase detector is modelled using an input amplitude dependent linear gain factor, $A \cdot K_{PD}$, assuming that instantaneous phase error is small. Since the comparator gain is inversely proportional to the instantaneous amplitude of its input signal, an approximated gain factor K_{CMP} , given in Equation(3-3), is used to characterize the comparator behaviour.

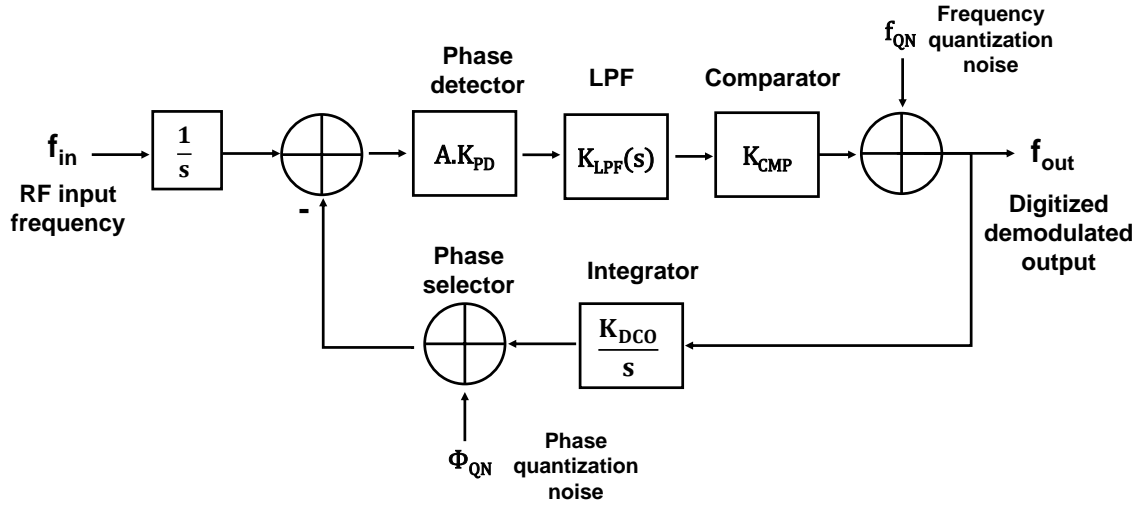


Figure 3-1: An approximated linear model of PDC loop.

$$K_{CMP} \approx \frac{1}{A \cdot K_{PD} \cdot K_{LPF}(s)} \quad (3-3)$$

Employing the transfer functions in Equations 3-1 and 3-2, authors in [4] concluded that:

- the open-loop gain of the PDC loop is independent of the input amplitude. It is due to the presence of comparator in the PDC loop as it negates the amplitude-dependent gain of the analog mixer.
- the loop bandwidth depends mainly on K_{DCO} and should be optimized to cover frequency deviation range (Δf) and meet the interference rejection requirement. LPF decouples the interference rejection from the K_{DCO} optimization at the cost of loop stability.

Despite its few acceptable predictions, the linear model of PDC loop is grossly inaccurate. Linear gain assumption of phase detector and comparator are error-prone, since the comparator gain largely depends on the statistical properties of its input signal and instantaneous phase error, θ_e can reach to a maximum of $\pm\pi/2$ at the phase detector output.

On the other hand, time-domain analysis, using extensive numerical simulations, is the most preferred approach to understand the non-linear systems that comprise comparators (e.g., $\Sigma\Delta$ analog-to-digital converters [37]). Hence, in the next section, a time-domain model is employed to describe the zero-IF PDC receiver. The model is extensively simulated in MATLAB to understand its non-linear dynamics and the effect of individual blocks on overall PDC performance.

3-2 A time-domain model of the zero-IF PDC

A time-domain MATLAB model of zero-IF PDC, similar to the block diagram shown in Figure 3-2, is developed for in-depth analysis in this work. Each block in the figure is modelled according to the mathematical exposition of the receiver given in the Figure 3-2.

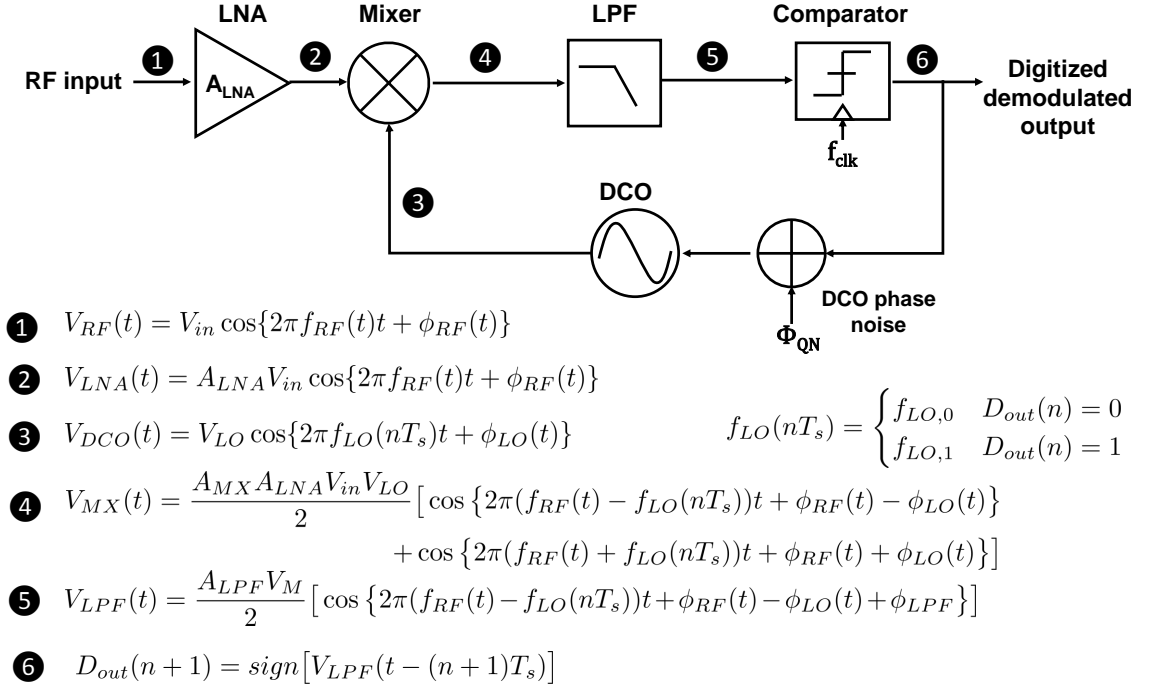


Figure 3-2: Time domain model of the PDC loop.

In the expressions given in Figure 3-2:

- $f_{RF}(t)$ and $f_{LO}(nT_s)$ are the instantaneous frequency of the RF input and LO signal at instant 't' and ' nT_s ' respectively; and V_{in} is the amplitude of the RF signal and $V_M = A_{MX} A_{LNA} V_{in} V_{LO}$, is the signal amplitude at LPF input.
- $\phi_{RF}(t)$ is the phase noise in the RF input signal. It can be attributed to several factors such as, carrier frequency drift due to dirty transmitter and doppler effect.
- $\phi_{LO}(t)$ is the inherent DCO phase noise. Initially, DCO is modelled without phase noise to study the loop behaviour and later on DCO phase noise is included to study its effect on the PDC loop.

As briefly mentioned in Chapter 2, zero-IF PDC also contains a DC offset cancellation block and an automatic frequency noise cancellation (AFC) block to address certain limitations of the PDC loop. These blocks will be included into the existing model, when those limitations are discussed in subsequent sections.

3-2-1 Simulation set-up

GFSK and BFSK signals, generated with either periodic or random binary inputs at a bit-rate of 1 Mbps, are used as inputs in all the time-step simulations of zero-IF PDC. GFSK is chosen as it is the modulation scheme employed by the *Bluetooth Low Energy* (BLE) wireless standard and BFSK, the simplest FSK, is used to study the fundamentals of loop dynamics without any Gaussian complexities. Figure 3-3 illustrates both GFSK and BFSK input signals, generated with binary inputs, "101011110000." The frequency deviation (Δf) of ± 250 kHz, a BLE specification, is used in both the modulation schemes. However, the carrier frequency, f_c is set at 200 MHz to shorten the simulation runtime. It is simple to conclude

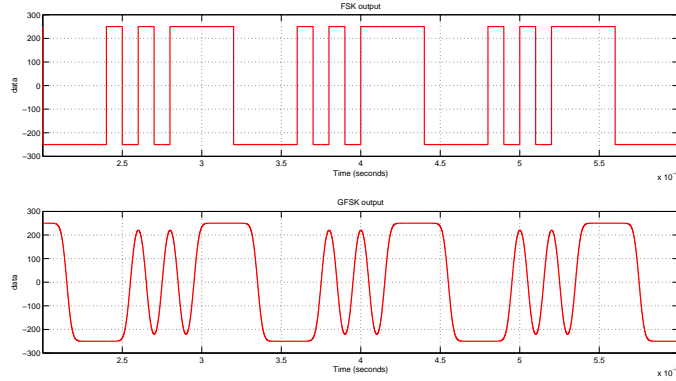


Figure 3-3: Comparison between FSK and GFSK.

that DCO should also oscillate at $f_c \pm \Delta f$ for PDC loop to track the input signal. In other words,

$$\begin{aligned} f_{LO,0} &= f_c - \Delta f \\ f_{LO,1} &= f_c + \Delta f \end{aligned} \quad (3-4)$$

Any mismatch between them would introduce undesired sinusoidal components into the PDC loop. An illustrative explanation together with maximum allowable mismatch and preventive measures are discussed in the Section (3-4).

For simulations in this section, a low-pass 3rd order Butterworth filter with a bandwidth of 600 kHz and a comparator, clocking at 32 MHz are used to complete the PDC loop. LPF and sampling frequency are adopted from the sliding-IF PDC [4]. Further, the gain of forward signal path is set to be unity for ease of analysis. It should be noted that all blocks are ideal in this section i.e. noiseless and linear with zero offsets.

3-2-2 Transient response - voltage-time representation

A simple time-step simulation is performed for a BFSK input signal, generated using periodic binary input "101011110000", and the transient signal at each node is plotted in Figure 3-4.

Following the simulation time-steps, one could identify that when the DCO and the low noise amplifier (LNA) output oscillate at same frequency, say $f_c + \Delta f$, they produce a DC signal

at the mixer output. After low-pass filtering, the DC signal at LPF output result in a stable comparator output. The comparator output together with the negative feedback behaviour keeps the DCO frequency unchanged which in turn maintains steady DC signal (SS_1) at the LPF output. For convenience, we define this steady state of PDC loop as 'static mode.'

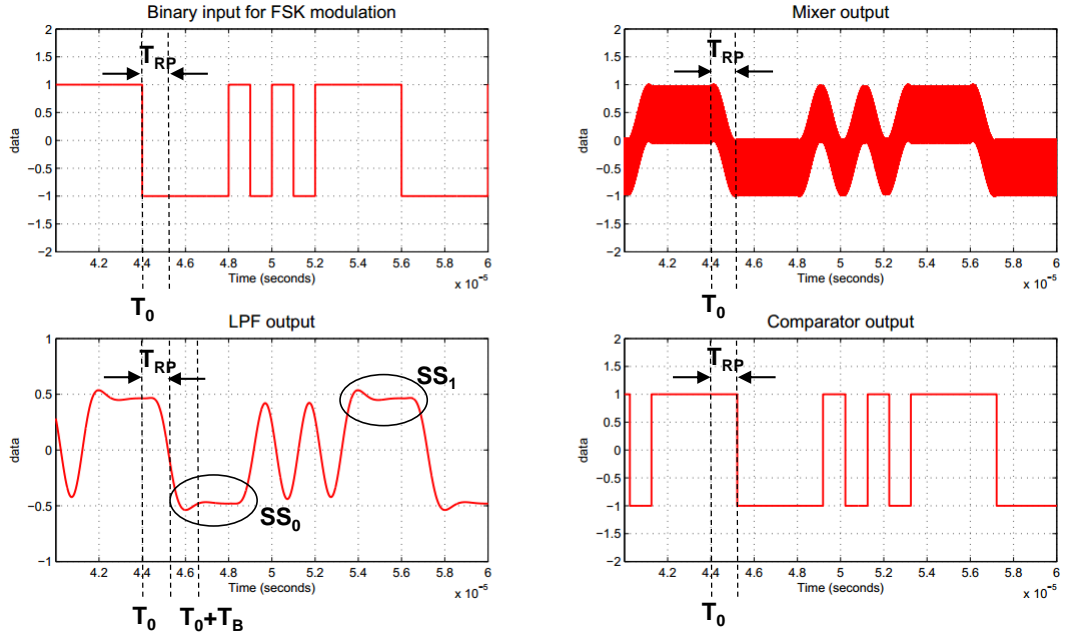


Figure 3-4: Time-step simulations - mixer, LPF and comparator output.

When BFSK input changes its frequency to $f_c - \Delta f$ at $t = T_0$, it introduces a difference-frequency component of 500 kHz ($2\Delta f$) at the mixer output. With bandwidth equal to 600 kHz, LPF transfers the 500 kHz signal to its output with marginal attenuation and considerable phase delay. Owing to its sinusoidal content, LPF output flips the comparator output after certain time, T_{RP} . In other words, PDC loop responds to the FSK modulation at $t = T_0 + T_{RP}$. The modified comparator output changes the DCO frequency to $f_c - \Delta f$ and thus makes the loop to track the current input frequency.

Though mixer outputs a DC signal instantaneously in response to the DCO frequency change, LPF takes time to settle. In this ideal simulation, this delay can be attributed completely to LPF phase response. At time $t = T_0 + T_B$, the LPF finally settles at DC value, SS_0 , thereby bringing the loop to static mode again. For future reference, we say that PDC loop is in 'dynamic mode' during the time period ($T_0 < t < T_0 + T_B$), as LPF output is transitioning from one steady-state to another.

To summarize, whenever input frequency changes, PDC loop steps into dynamic mode and returns back to static mode when LPF output settles at a steady-state. It should be noted that LPF output has two steady-states (SS_0 , SS_1), one for each frequency and they are of opposite polarity.

3-2-3 Transient response - phase-time representation

Voltage-time representation is widely used in PLL modelling [27], where the mixer is defined to provide the relevant phase-to-voltage conversion. However, for PDC loop, author believes that considering only phase transfer at each node of the loop would provide a better insight into the loop dynamics. Author also concedes that the phase-time domain model has certain limitations which need to be reworked to explain phase of composite signal with multiple frequencies.

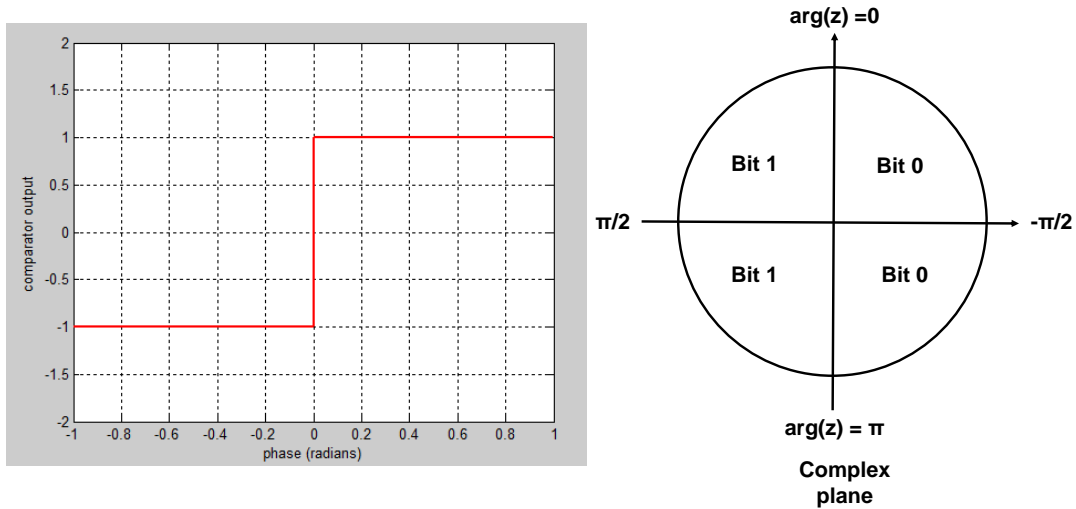


Figure 3-5: Phase-to-digital transfer curve and its representation in complex plane.

Phase-to-digital transfer curve of comparator

For phase-time domain representation, the voltage-digital transfer characteristics of the comparator is translated to phase-digital transfer characteristics by mapping the threshold voltage to a phase threshold. For an ideal comparator, since $\sin(n\pi) = 0$ where $n \in \mathbb{Z}$, the zero threshold in voltage domain can be translated to one of the several $n\pi$ thresholds¹ in phase domain (see Figure 3-5). Negative feedback prevents the phase at comparator input from crossing more than one phase threshold. The factors that cause the comparator input to cross more than 1 would distort the PDC behaviour and introduce instability.

The transient behaviour of PDC, shown in Figure 3-4, will be discussed again in phase-time domain by following the simulation time-steps. At $t < T_0$, the BFSK input and DCO output are oscillating at same frequency, $f_c + \Delta f$. Mixer and LPF outputs are settled at a constant phase, ϕ_{s1} . Though, mixer also contains sum-frequency component at its output, it is neglected in the analysis, as it will be filtered and has negligible effect at the comparator input. Comparator digitizes the constant phase ϕ_{s1} , seen at its input. Due to negative feedback, DCO oscillates at same frequency and ensure that loop is locked. As defined earlier, we term this steady-state as 'static mode', since phase at mixer and LPF output is constant.

¹ *sin* or *cos* is just a matter of preference. For *cos*, zero threshold translate to $(2n + 1)\pi/2$ thresholds

At time-step, $t = T_0$, the BFSK input changes its frequency from $f_c + \Delta f$ to $f_c - \Delta f$ and moves the loop into dynamic mode. In response, the phase at mixer output starts drifting at the rate of $-2\pi(2\Delta f) \text{ rad s}^{-1}$ instantaneously. However, the phase at LPF output remains unchanged at ϕ_{s1} , which in turn causes DCO frequency to remain at $f_c + \Delta f$. Here negative frequency, $-2\Delta f$ accounts for the situation where, $f_{in} < f_{DCO}$. For positive frequency difference $f_{in} > f_{DCO}$, the phase drifts at opposite direction, thereby confining the steady-state phases around one threshold.

After certain delay, δt , the $-2\Delta f$ signal at mixer output reaches the LPF output at $t = T_0 + \delta t$. This causes the phase at LPF output to drift at the rate of $-2\pi(2\Delta f) \text{ rad s}^{-1}$ towards one of the comparator threshold. When the drifting phase at LPF output crosses the phase threshold at $t = T_0 + T_{RP}$, the comparator flips its output. Subsequently, DCO changes its signal frequency to $f_c - \Delta f$ and mixer output settles at constant phase, ϕ_{s0} . In ideal case, all these changes occur instantaneously and mixer output settles at constant phase at ϕ_{s0} at $t = T_0 + T_{RP}$. However, the LPF output phase continues to drift at the rate of $-2\pi(2\Delta f) \text{ rad s}^{-1}$ away from the comparator threshold.

Finally, LPF output also settles at phase, ϕ_{s0} at $t = T_0 + T_B$. Logically, the settling delay can be attributed to phase response of LPF and mixer/comparator/DCO delay (For ideal simulation, mixer/comparator and DCO has zero delay). This will be verified in the next section. So, at $t = T_0 + T_B$, BFSK input and DCO output are, once again, at same frequency ($f_c - \Delta f$) and the signals at mixer and LPF output are at constant phase, ϕ_{s0} . It indicates that PDC loop is moved back to static mode. Further, it can be inferred that new steady-state phase, ϕ_{s0} is just negative of the previous steady-state phase, ϕ_{s0} , as both are due to delay caused LPF phase response. In summary, PDC loop shifts from static mode to dynamic mode at $t = T_0$ and returns back to static mode at $t = T_0 + T_B$ with different steady-state phase at mixer and LPF output.

Figure 3-6 graphically illustrates the phase-time representation using the phasor diagram of LPF output. Phasor diagram differentiates the negative and positive phase drift by rotating in clockwise and counter-clockwise direction respectively. It also shows the comparator output and signal frequencies at input, DCO and LPF at time instants described above.

Since the graphs in Figure 3-4 confirm that PDC loop can track the frequency of the input signal, we study the following features of the loop to fathom the loop behaviour.

- Stability of the PDC loop.
- Steady-state response.
- Response time and bandwidth.
- Effect of Gain and DC offset.

All these characteristics are interrelated and analysing one requires understanding of one or more other characteristics. Of these, stability analysis uses the essence of all the other attributes. Hence, it will be discussed last, despite its paramount importance. Both voltage-time and phase-time representations are used to discuss these attributes.

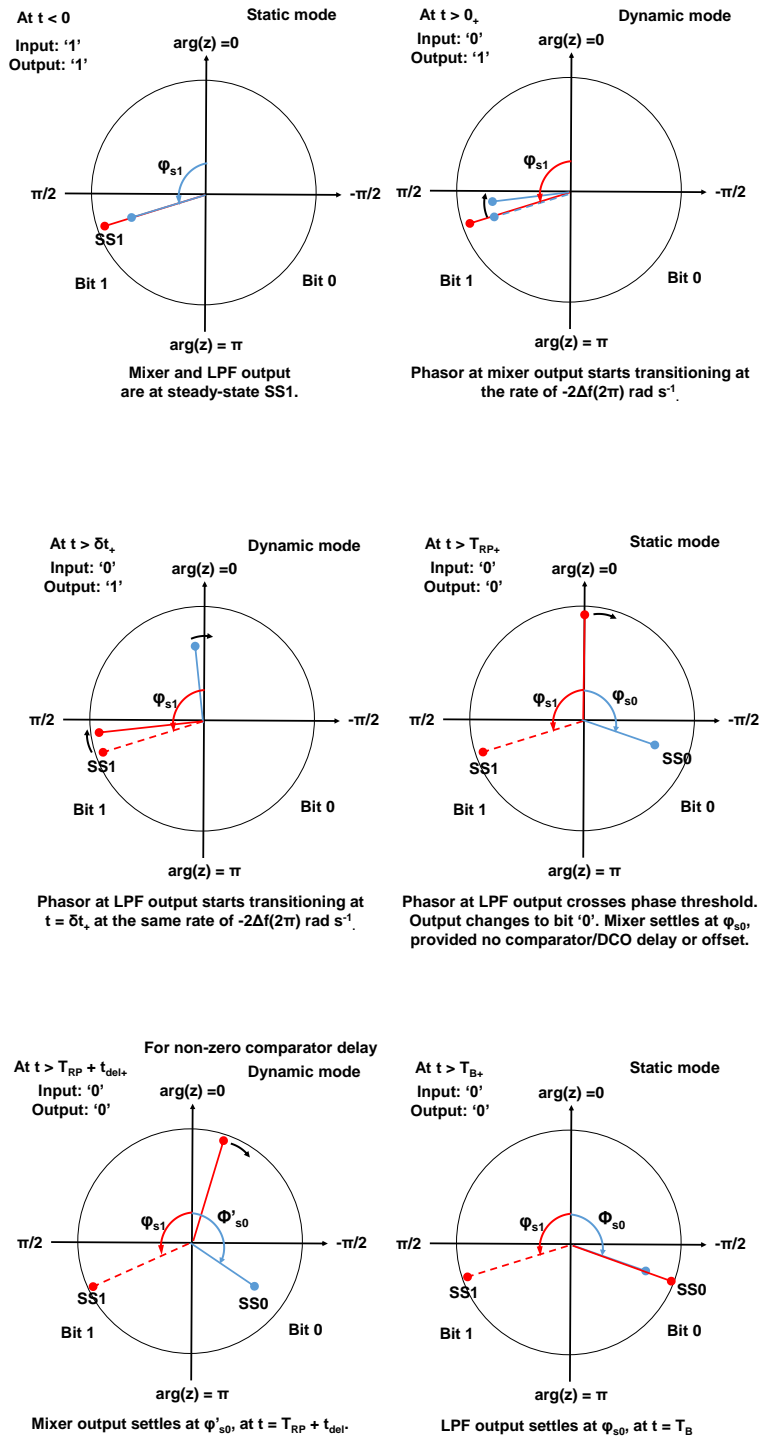


Figure 3-6: Phase-time domain representation of transient behaviour of the PDC loop.

3-3 Loop characteristics

For reasons mentioned in previous section, PDC loop uses BFSK input signal generated with periodic binary pattern "101011110000" for all the analyses in this section.

3-3-1 Steady-state response

As shown in both representations, the mixer and LPF output in the PDC loop settles at either SS_0 or SS_1 in voltage domain or at ϕ_{s0} or ϕ_{s1} in phase-domain after responding to an input frequency change. With its ability to provide extreme gain, the comparator could push the steady-state phase and DC close to zero, in the ideal scenario without LPF. However, in the presence of LPF, the 500 kHz ($2\Delta f$) signal will be delayed by LPF phase response, which in turn determines the steady-state phase response at mixer and LPF output. To prove this supposition, multiple simulations are performed with LPFs providing different phase responses to the 500 kHz signal.

Transient simulations are performed with a family of Butterworth filters with order (2,3 and 4) and bandwidth (400 kHz – 2 MHz). Simulation results, in Figure 3-7, point out a strong correlation between the LPF phase response and steady-state phase at LPF output in the PDC loop. Folding of steady-state phase around LPF phase of $-90^\circ (-\pi/2)$, is due to mismatch in output range of *asin*, inverse sine function $[-\pi/2, \pi/2]$ and *freqz*, frequency response function $[-\pi, \pi]$ in MATLAB. Accounting that, the results confirm that LPF phase response indeed determines the steady-state phase and DC at LPF output. Hence, through optimum selection of LPF, steady-state phase can reach up to a maximum of $\pm\pi/2$. It will be shown later that large steady-state DC at mixer and LPF output improves the noise and offset tolerance of the PDC loop. Simulations are also performed with a different family of filters, elliptic in this case, to catch any filter-specific limitations and results, also plotted in Figure 3-7, wards off this concern.

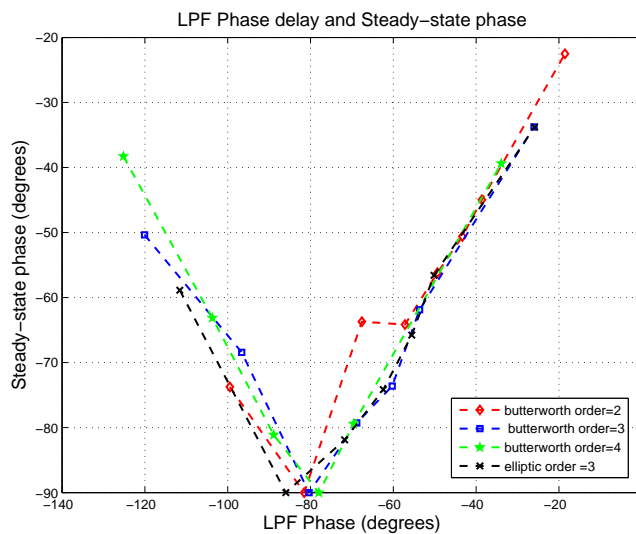


Figure 3-7: LPF phase response and steady-state phase.

Considering non-ideal situations, besides LPF phase response, transient delays of comparator and DCO also affect the steady-state response. They introduce an additional phase offset of $(2\pi f_{DCO} t_{del}) \bmod 2\pi$ at the mixer and LPF output. Here, f_{DCO} is the previous DCO frequency and t_{del} is the cumulative delay of comparator and DCO. Using the phase-time representation, shown in Figure 3-6, the loop can become unstable, if the incremental phase offset pushes the phasor at LPF output beyond $\pm\pi$. Figure 3-8 shows this additional phase offset and instability occurrence for different cumulative delays. In this simulation, the cumulative delay of DCO and comparator are modelled using delay elements with unit delay of 31.25 ns. For the case of delay = $10 \times$ unit delay, the PDC loop fails to reproduce FSK input '101011110000.' Hence, the delay of comparator and DCO should be optimized together with LPF to keep the steady-state phase around $\pm\pi/2$ for better noise and offset performance.

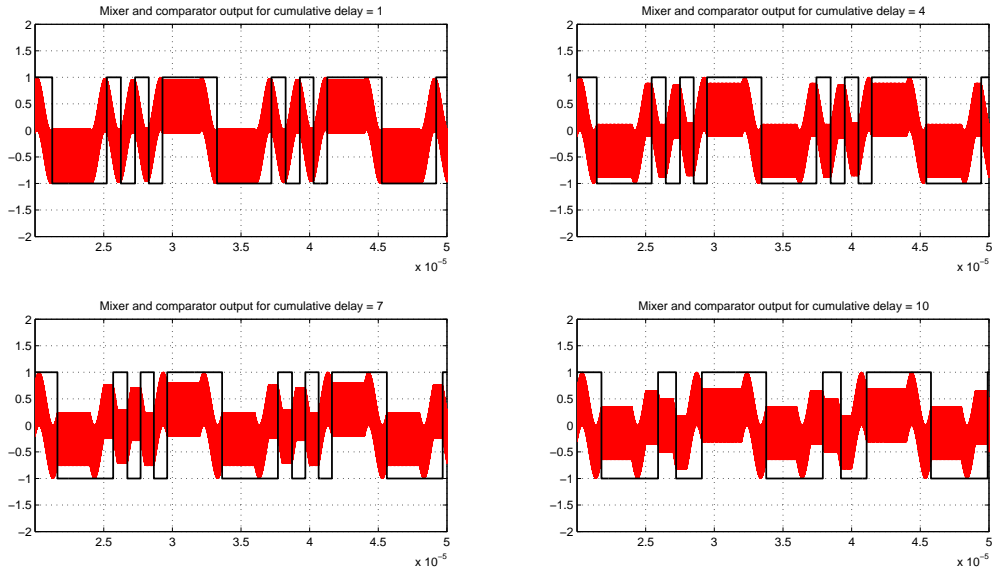


Figure 3-8: Mixer and comparator output for different comparator and DCO delays.

3-3-2 Response time and bandwidth

Analysing bandwidth, a linear frequency domain property, using a non-linear comparator is cumbersome and difficult². Hence response time, its time-domain equivalent, is discussed in this section to have a fair understanding of the tracking ability of the PDC loop.

As briefly mentioned in the earlier sections, PDC loop takes finite time, T_{RP} to respond to the input stimulus. It can be mathematically expressed as,

$$T_{RP} = T_{LNA} + T_{MX} + T_{LPF} + T_{cross} + T_{CMP} \quad (3-5)$$

where, T_{LNA} , T_{MX} , T_{LPF} and T_{CMP} are the delays due to LNA, mixer, LPF and comparator respectively and T_{cross} is the time taken by the $2\Delta f$ signal to cross the comparator threshold, ϕ_{th} , from its steady-state phase, $\phi_{s0,1}$.

²Author concedes his defeat in this Herculean task.

In ideal conditions, the delays of LNA, mixer and comparator can be considered zero. LPF delay is simply its phase response to the 500 kHz ($2\Delta f$) signal. T_{cross} can be calculated using the equation given below:

$$\int_0^{T_{\text{cross}0,1}} f dt = \frac{1}{2\pi} (\phi_{th} - \phi_{s0,1}) \quad (3-6)$$

where, f is the frequency of the signal at the LPF output. For BFSK input signal³, f is constant and equal to $2\Delta f$ during the transition. With comparator threshold, $\phi_{th} = 0$, above equation can be simplified as,

$$T_{\text{cross}0,1} = \frac{-\phi_{s0,1}}{2\pi(2\Delta f)} \quad (3-7)$$

Using Equations (3-5) and (3-7), the response time can be given as,

$$T_{RP} = \frac{\phi_{LPF,500\text{ kHz}}}{2\pi(2\Delta f)} + \frac{-\phi_{s0,1}}{2\pi(2\Delta f)} \quad (3-8)$$

From the conclusions derived in the previous section, LPF phase response and steady-state phase are approximately equal to each other ($\phi_{LPF,500\text{ kHz}} \approx \phi_{s0,1}$). Then,

$$T_{RP} = 2 \left| \frac{\phi_{LPF,500\text{ kHz}}}{2\pi(2\Delta f)} \right| \quad (3-9)$$

Equation (3-9) states that response time can be minimized by using LPFs with shorter phase delay at 500 kHz. The results, obtained by simulating the PDC loop with different LPFs, confirm this behaviour Figure 3-9. For completeness, under ideal conditions, the time (T_B)

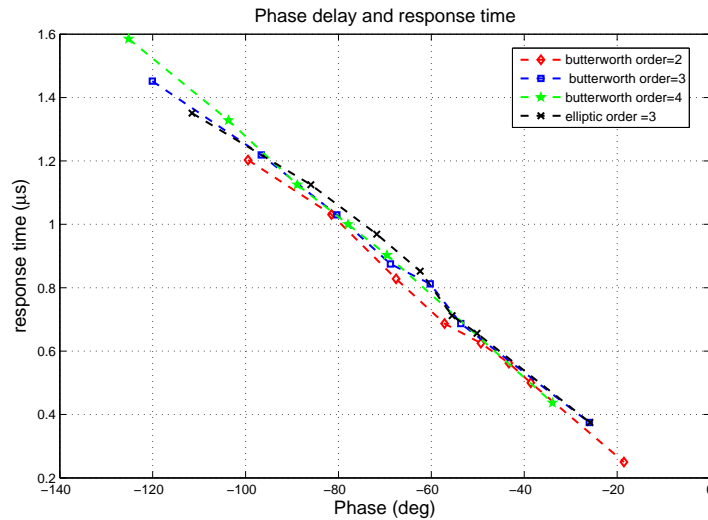


Figure 3-9: LPF phase response and response time.

³For BFSK, input frequency shift considered to occur instantaneously, whereas for GFSK, frequency shift occurs gradually.

taken by the PDC loop to settle at steady-state phase $\phi_{s0,1}$, after input frequency change can be expressed as,

$$T_B = T_{RP} + \left| \frac{\phi_{s0,1}}{2\pi(2\Delta f)} \right| \quad (3-10)$$

$$T_B = 3 \left| \frac{\phi_{LPF,2\Delta f}}{2\pi(2\Delta f)} \right| \quad (3-11)$$

When mixer, comparator and DCO have non-zero delays, they tend to contribute to the steady-state phase, $\phi_{s0,1}$. In this scenario, the steady-state phase would be,

$$\phi_{s0,1} \approx \phi_{LPF,2\Delta f} + 2\pi(2\Delta f)t_{del} + \phi_{mx,2\Delta f} \quad (3-12)$$

where t_{del} is the cumulative delay of comparator and DCO and $\phi_{mx,2\Delta f}$ is the phase delay due to mixer for frequency component, $2\Delta f$. Employing this relation in Equations (3-5) and (3-10), one could estimate response and settling time respectively.

Equation (3-9) also indicate that increasing the frequency difference, $(2\Delta f)$ would improve the response time. It can be achieved by increasing the frequency range of DCO during PDC operation, i.e. $f_{LO,1} > f_c + \Delta f$ and $f_{LO,0} < f_c - \Delta f$. Though, large DCO frequency range reduces the T_{cross} , it also increases the LPF delay, $\phi_{LPF,2\Delta f + \delta f}$, for a given LPF bandwidth and order. Further, due to frequency mismatch of δf between input and DCO frequencies in the static mode, the phase at mixer and LPF outputs fails to settle and continues to drift at the rate of $\pm 2\pi\delta f$. It would introduce undesired pulse-modulation at the comparator output. A phase-time representation, given in Figure 3-10 illustrates the phase-drift in the static mode. In conclusion, increasing the frequency difference, $2\Delta f$, has conflicting effects on the response time and should be carefully considered before employing it.

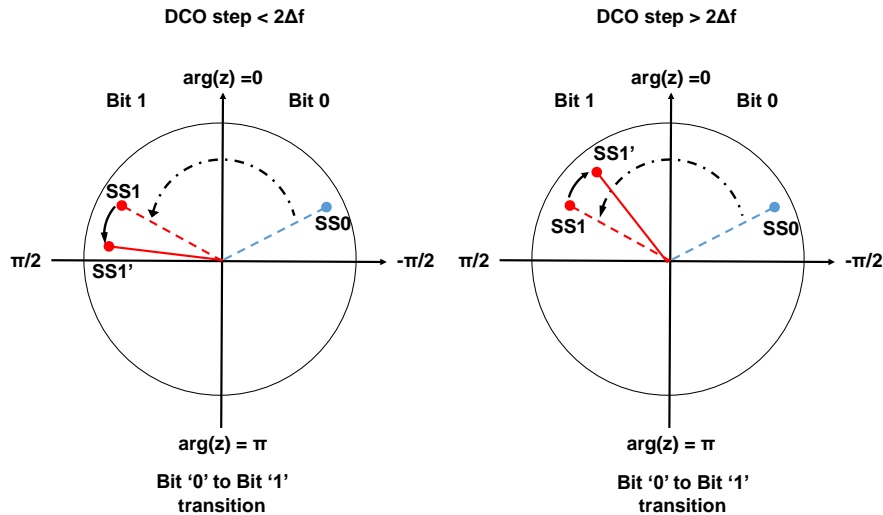


Figure 3-10: LPF output phasor drift for DCO step $\neq 2\Delta f$.

Finally, it is obvious that, frequencies corresponding to alternate 1s and 0s in the input signal will be missed if the PDC closed loop delay (T_{cl}) is greater than $2 \times T_b$, where T_b is bit period.

Mathematically, it can be given as,

$$T_{cl} = T_{MX} + T_{LPF} + T_{cross} + T_{CMP} + T_{DCO} \quad (3-13)$$

$$T_{cl} < 2 \times T_b \quad (3-14)$$

Equivalent phase delay constraint, in terms of frequency difference component $2\Delta f$, can be given as,

$$2\pi(2\Delta f)T_{cl} < 2\pi \quad (3-15)$$

To evaluate the above conditions, multiple time-step simulations are performed by varying comparator delay for fixed LPF. Obtained results, shown in Figure 3-11 and Figure 3-12, indicate that effective phase delay in the closed loop, $(2\pi 2\Delta f T_{cl}) < (5/3)\pi$ for the PDC loop to track every single FSK input.

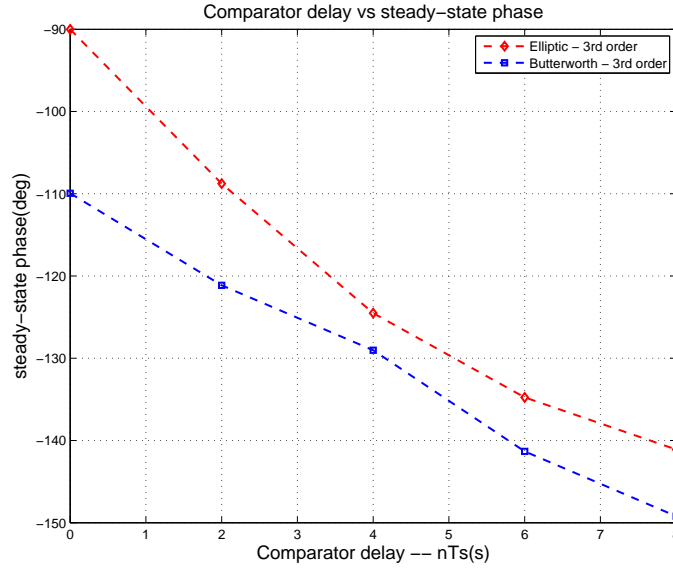


Figure 3-11: Comparator delay and steady-state phase.

In conclusion, non-zero delays of the mixer, LPF, comparator and DCO determine the steady-state phase and response time. The closed loop delay should be smaller than twice the bit-period for efficient tracking. DCO frequency steps, different from input frequency deviation, would introduce phase drift in static mode.

3-3-3 Gain and DC offset

Since the PDC loop operates in phase domain, intuitively one could suppose that the gains of LNA, mixer and LPF have hardly any effect on the PDC performance. Qualitatively, this can be explained by considering the phase drift of signal phasor at LPF output for different gain scenario. Despite magnitude difference, all these phasors have same steady-state phase and drift at the same speed ($2\Delta f$) towards the phase threshold when input frequency changes. Hence, they cross the threshold at the same instant Figure 3-13. To verify this understanding, multiple time-step simulations with different LNA, mixer and LPF gains are performed and

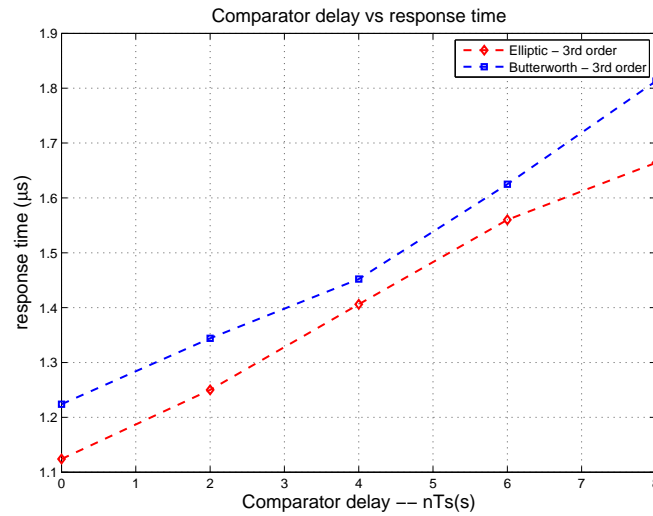


Figure 3-12: Comparator delay and response time.

the resultant steady-state phase and response time are plotted. The response time and steady-state phase results, shown in Figure 3-14 confirm that gain has negligible effect on the PDC performance.

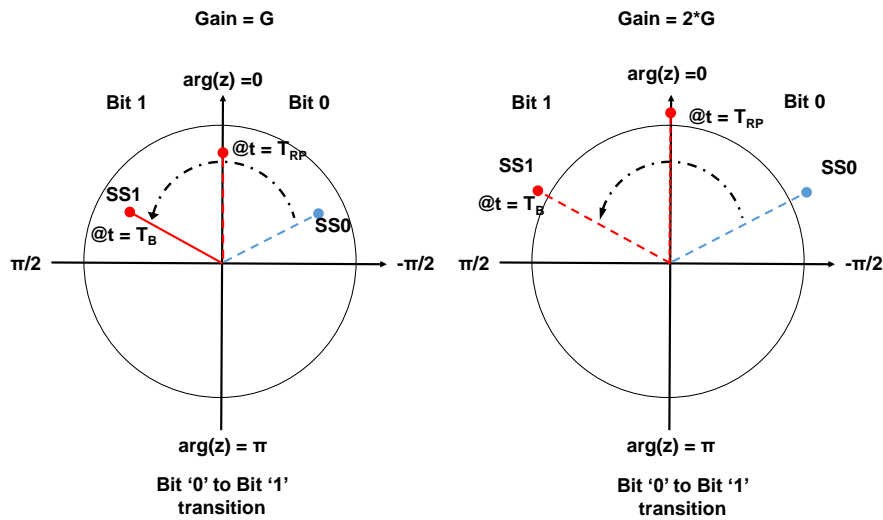


Figure 3-13: The behaviour of LPF output phasor for different forward path gains.

Direct conversion behaviour of zero-IF PDC makes the study of DC offset and its impact on PDC performance pertinent. DC offsets in the PDC loop are due to factors such as self-mixing, non-ideal mixer, opamp DC offsets and non-zero threshold of the comparator. Cumulatively, these factors modify the threshold point of the comparator for input signal and cause early or late decisions.

In phase-time representation, DC offset at the comparator can be modelled as an angular

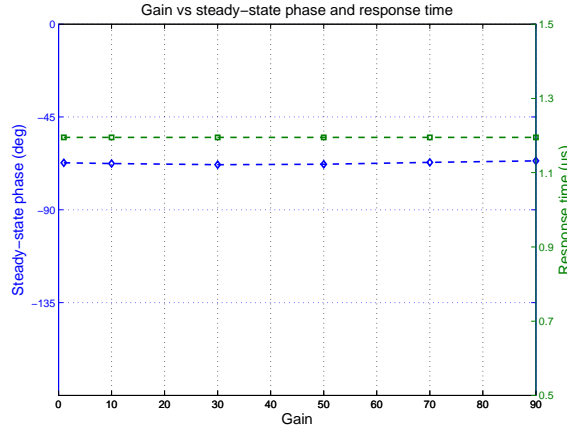


Figure 3-14: Steady-state phase (blue) and response time (green) for different forward path gains.

shift of comparator phase threshold from its ideal zero phase. As shown in the Figure 3-15, the angle of rotation can be given as

$$\theta = \sin^{-1} \left(\frac{Offset}{A} \right) \quad (3-16)$$

where *Offset* and *A* are the effective DC offset and input signal amplitude at the comparator input. Evidently, this angular shift displaces the steady-state phases ($\phi_{s0,1}$) of the signal at mixer and LPF output by same magnitude. Results of multiple time-step simulations with different DC offsets are shown in Figure 3-16. In this figure, the incremental shift of steady-state phase, $\phi_{s0,1}$, at mixer output for increasing DC offset clearly depicts the angular displacement of threshold and steady-state phases. It also indicates that angular shifts induce no behavioural change in the PDC loop, until it forces a cumulative steady-state phase of more than π at mixer and LPF output. This supposition is verified by predicting the maximum allowable offset for different steady-state phase. The results, shown in Figure 3-17, highlight that PDC loop with smaller steady-state phase can withstand large DC offsets.

In conclusion, voltage gain in the signal path has no effect on the performance of PDC loop, whereas, to sustain large DC offsets, PDC loop should have small steady-state phase.

3-3-4 Stability

Conventional linear s-domain/z-domain models of phase-locked loops describes the stability of the loop when it is locked. Analyses until now indicate that PDC operation involves loop going out of locked condition whenever the input bit changes. Hence, stability predictions using linear models will be grossly inaccurate. In this work, extensive MATLAB simulations are carried out for each scenario to ensure that loop is stable with no limit-cycles in the desired bandwidth.

Meanwhile, continuing phase-time based analysis of the PDC loop, the phase at every node of the PDC loop can be expressed using the equations given below. Since, DCO frequency gets

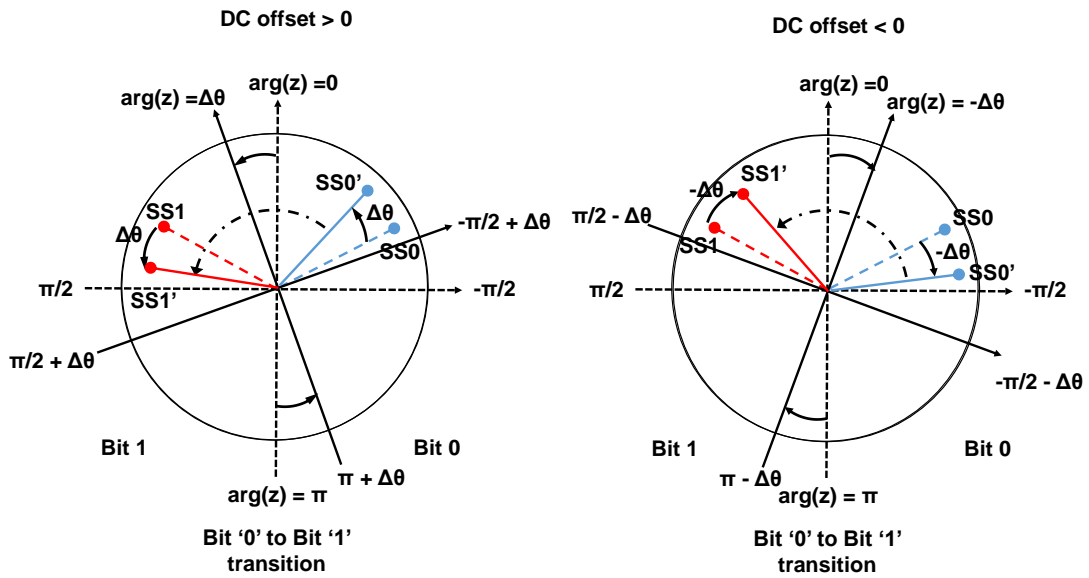


Figure 3-15: Phase threshold change for different DC offsets.

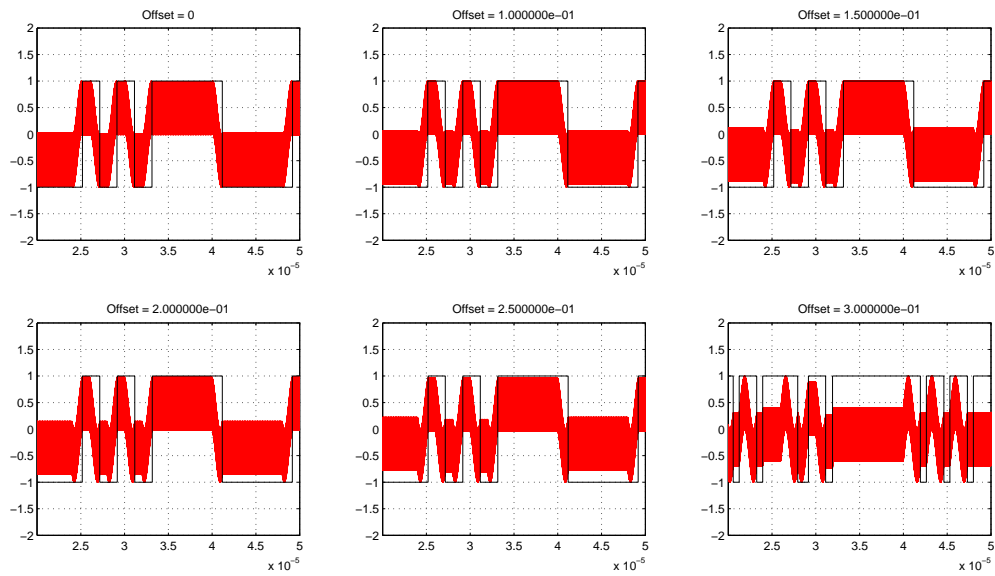


Figure 3-16: Mixer output for different DC offsets.

updated every T_s seconds, the sampling period of comparator, the phase is also evaluated at every T_s seconds in these equations.

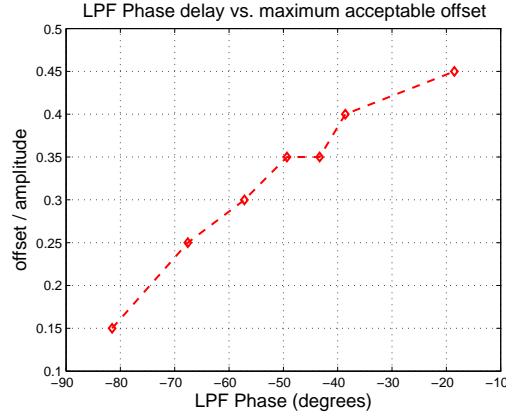


Figure 3-17: Maximum allowable DC offsets for different LPF phase response.

$$\phi_{\Delta}(t + T_s) = \phi_{\Delta}(t) + 2\pi f_{\Delta}(t)T_s \quad (3-17)$$

$$\phi_L(t + T_s) = \phi_{\Delta}\left(t + T_s - \frac{\phi_{LPF,2\Delta f}}{2\pi(2\Delta f)}\right) \quad (3-18)$$

$$D_{OUT}(t + T_s) = \text{sign}[\phi_L(t + T_s)] \quad (3-19)$$

where, $f_{\Delta}(t) = f_{in}(t) - K_{DCO}D_{OUT}(t)$ is the difference frequency at the instant, t ; ϕ_{Δ} and ϕ_L are the phases⁴ at mixer output and LPF output respectively; $\phi_{LPF,2\Delta f}$ is used to account for the phase introduced by LPF; and D_{OUT} is the comparator output. As discussed earlier, the high frequency components ($f_{in}(t) + K_{DCO}D_{OUT}(t)$) in the mixer output are filtered by LPF and hence they are safely neglected here.

Considering only phase information, the above equations indicate that the mixer acts as a phase subtractor and subtracts the DCO output phase from the RF input phase. LPF transfers the phase at the mixer output to comparator input. For LPFs with large bandwidth ($BW \gg 2\Delta f$), there would be no delay in the phase transfer. However, in the case of LPF bandwidth comparable to $2\Delta f$, the phase transfer is delayed by an amount equal to the LPF phase response at $2\Delta f$. In other words, LPF could be interpreted as a block with unity phase gain and negligible delay in case of large bandwidth and finite delay in other cases. As described earlier, the behaviour of comparator in phase domain is same as in voltage domain with thresholds at $\pm n\pi$.

Phase domain representation of the PDC loop is depicted clearly in Figure 3-18(a). Using this illustration, the integrators in the DCO and the RF input can be translated to the mixer output without causing any behaviour change. Now, mixer can be considered as a combination of: (i) subtractor that subtracts DCO output frequency from the RF input frequency; and (ii) integrator due to the translation. Based on this premise, the PDC loop can be modelled as a $\Sigma\Delta$ -modulator in the frequency domain, where mixer performs subtraction and integration, LPF acts as simple delay element and DCO behaves as a frequency DAC. This is shown in the Figure 3-18(b).

⁴Unless otherwise specified, phase is referenced with respect to the maximum difference frequency, $2\Delta f$.

Further, the $\Sigma\Delta$ -modulator is of first order which means that the PDC loop is always stable in frequency domain. In other words, PDC loop digitizes the frequency of the input signal with limit-cycles outside the desired bandwidth.

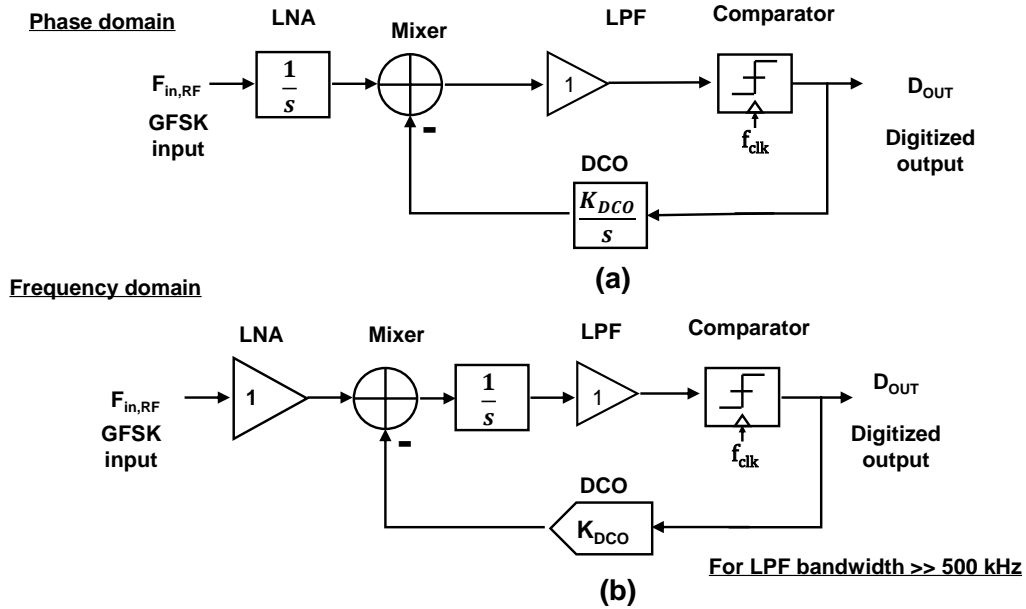


Figure 3-18: Frequency domain $\Sigma\Delta$ -modulator model of the PDC loop.

Using $\Sigma\Delta$ -modulator model, one can easily understand the behaviour of PDC loop in the presence of frequency offsets and DCO phase noise. On the other hand, it is restricted by its own assumptions and fails to explain the behaviour of the PDC loop in the scenarios where those assumptions don't hold true. Some situations, where $\Sigma\Delta$ -modulator model could be grossly inaccurate, are given below.

- When there are multiple frequencies at LPF input and LPF has limited stopband suppression, the equivalent phase at the output is a non-linear function of input frequencies. A simple unity gain delay model of LPF cannot describe this non-linear behaviour. Hence the model fails in the presence of strong interferers.
- Due to random input frequency drift and DCO phase noise, LPF delay cannot be predicted accurately in the model. Moreover, the LPF delay has non-linear dependency on the difference frequency. Together, they compromise the accuracy of the model in these scenarios.
- The $\Sigma\Delta$ -modulator model fails to describe the noise and linearity performance of the PDC loop. Since non-linearity produce DC and intermodulation tones in the desired signal band, this would complicate the estimation of equivalent phase.
- Since phase wraps around 2π radians, *modulo* integration should be used in the place of linear integration for better accuracy.

In conclusion, PDC loop can be considered as 1st order frequency-domain $\Sigma\Delta$ -modulator and hence always stable.

3-4 Frequency tolerance

Free-running oscillator, in the absence of PLL, suffers from unconstrained phase noise and frequency drift. In PDC loop, one could realise that the phase noise and the frequency drift at the DCO will manifest directly at the comparator input and in large magnitude, could force the PDC loop to make wrong decisions. Same can be explained for the carrier frequency offset/drift in the received signal. Since BLE expects the receiver to tolerate a maximum frequency offset of ± 150 kHz (static/dynamic: $\pm 100/\pm 50$ kHz), it is necessary to understand the frequency tolerance of the PDC loop.

3-4-1 Frequency noise in the PDC loop

Let $f_{in}(t)$ and $f_{DCO}(t)$ be the RF input and DCO frequencies at the time instant, 't' and $\delta f(t)$ be the frequency of the signal at the LPF output. For ideal BFSK input, $\delta f(t)$ would be either 0 or $2\Delta f$ depending on whether the PDC loop is in the static mode or the dynamic mode. However, for the reasons mentioned earlier, $\delta f(t)$ would also contain other noise components. For the ease of analysis, let us categorize these noise components into two groups - $\delta f_{n,DC}$, constant frequency offset and $\delta f_{n,AC}$, varying frequency noise.

$$\delta f(t) = \delta f_0(t) + \delta f_{n,DC}(t) + \delta f_{n,AC}(t) \quad (3-20)$$

where, $\delta f_0(t)$ is the ideal $\delta f(t)$. As briefly discussed in the Section (3-3-2), if DCO step differs from $2\Delta f$, it would introduce state-dependent frequency offset to $\delta f(t)$. Since the introduced offset would be constant throughout the static/dynamic mode, it is grouped with constant frequency offsets. Hence, constant frequency offset, $\delta f_{n,DC}(t)$ becomes quasi-state/time dependent.

Constant frequency offset, $\delta f_{n,DC}(t)$

Possible causes for constant frequency offsets in $\delta f(t)$ are:

- Static offset between the RF input carrier frequency and the DCO centre frequency. BLE allows a maximum static frequency offset of ± 100 kHz from the defined RF input channel frequency.
- Mismatch between the input frequency deviation, $2\Delta f$ and the DCO step, K_{DCO} . DCO step mismatch usually arises due to design limitations.⁵

Using $\Sigma\Delta$ -modulator analogy, discussed in Section(3-3-4), $\delta f_{n,DC}(t)$ in the PDC loop can be considered analogous to DC offset in the voltage-domain $\Sigma\Delta$ modulator. Since, DC offset either shrinks or expands the pulse at the comparator output, similar behaviour can be observed in the PDC loop with $\delta f_{n,DC}(t)$. Transient results, presented in Figure 3-19, shows the output of LPF and comparator in the PDC loop for the input pattern '101011110000...' Different pulse widths at the comparator output are observed for different $\delta f_{n,DC}$. This is further confirmed by plotting the running integral of the comparator output in the Figure 3-20. Observing the Figure 3-20, one could postulate that average pulse width is a rough measure of frequency offset.

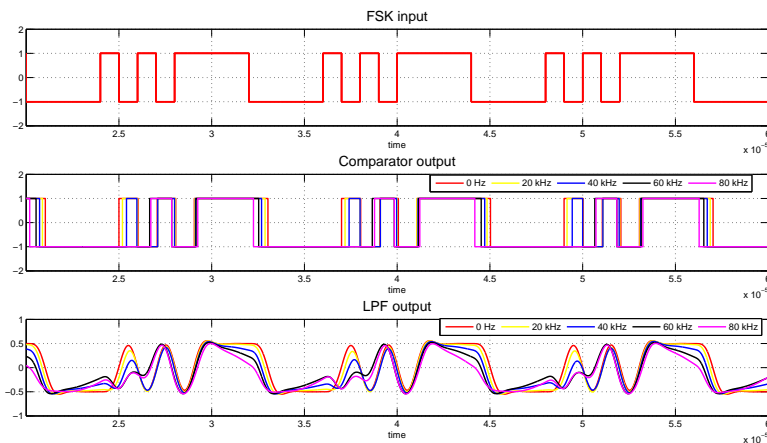


Figure 3-19: Transient simulation results for different frequency offsets.

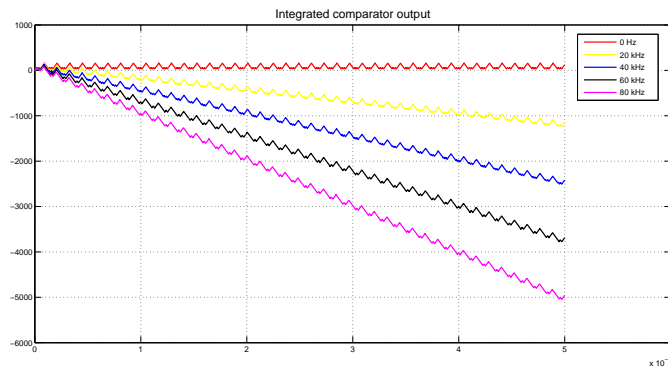


Figure 3-20: Integrated comparator output for different frequency offsets.

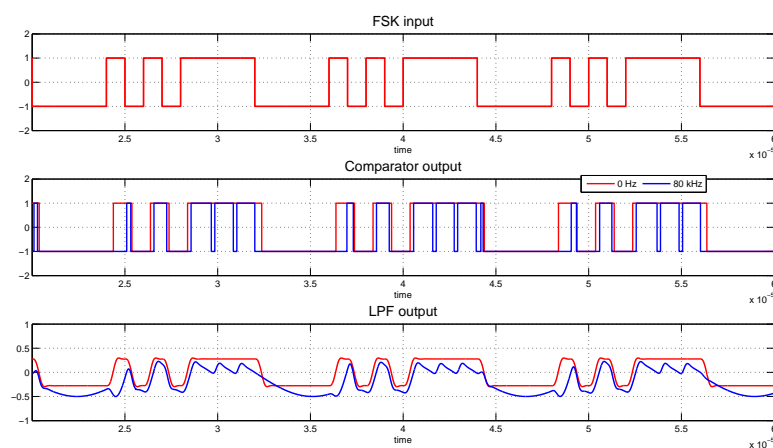


Figure 3-21: An example of bit slip when short 1s/0s immediately follow long 0s/1s.

Unchecked phase drift, due to $\delta f_{n,DC}$, could cause spikes at the comparator output (Figure 3-19), if the input contains a long sequence of 1s or 0s. Furthermore, it could also cause bit slip (Figure 3-21), if the accumulated phase, due to phase drift, at the end of long 1s and 0s is not compensated by short 0s or 1s that immediately follows them. Continuous phase drift, with drift-rate of $2\pi\delta f_{n,DC}$ in the static mode, is the cause for this behaviour. LPF output, shown in Figure 3-19 and Figure 3-21, exemplifies the static mode phase drift. Hence one could realise that longer the consecutive 1s and 0s at the input, more the loop will be troubled by the phase drift. If the frequency offset and LPF phase response is known, an approximate safe limit for consecutive 1s and 0s can be given as below.

$$N_{critical} = \begin{cases} \frac{\phi_{s0,1}}{2\pi\delta f_{n,DC} T_b} & 0 < |\phi_{s0,1}| < \pi/2 \\ \frac{\pi - \phi_{s0,1}}{2\pi\delta f_{n,DC} T_b} & \pi/2 < |\phi_{s0,1}| < \pi \end{cases} \quad (3-21)$$

Though, BLE randomises the bit stream, there is no explicit limit for maximum consecutive 1s/0s at the input. Hence, a calibration mechanism is needed to minimize the effect of frequency offset on the PDC loop. A simple background calibration, that uses average pulse width of comparator output to estimate $\delta f_{n,DC}(t)$ and later use the estimation to adjust the DCO step, is employed in this work. More about the features of background calibration and its limitations are discussed in the next section.

Finally, realising optimum steady-state phase at the mixer and LPF output would further minimize the risks of spikes and bit slip due to phase-drift. It is understandable that any phase drift would take maximum time to cross the threshold if its initial steady-state phase is $\pm\pi/2$. Hence, to make PDC loop robust to frequency offset, the steady-state phase should be close to $\pm\pi/2$.

Case 2: AC frequency noise, $\delta f_{n,AC}(t)$

Time-varying frequency noise components in $\delta f(t)$ are mostly due to a dirty transmitter, $\delta f_{n,TX}(t)$ and DCO phase noise, $\delta f_{n,DCO}(t)$.

$$\delta f_{n,AC}(t) = \delta f_{n,TX}(t) + \delta f_{n,DCO}(t) \quad (3-22)$$

Once again using $\Sigma\Delta$ -modulator analogy, discussed in Section(3-3-4), the frequency noise, $\delta f_{n,AC}(t)$ can be considered analogous to noise in the voltage-domain $\Sigma\Delta$ modulator. More specifically, $\delta f_{n,TX}(t)$ behaves like random input noise and experiences transfer behaviour similar to that of BLE input signal. In other words, $\delta f_{n,TX}(t)$ will induce pulse width variation at comparator output.

Time-step simulations are performed to confirm the direct transfer behaviour of $\delta f_{n,TX}(t)$. For that, dirty transmitter is modelled by varying RF channel frequency sinusoidally⁶ and the running integral of comparator output is plotted for different variation amplitude and frequency. Figure 3-22 and Figure 3-22 prove that the frequency variations due to dirty transmitter are reflected at the PDC output.

⁵In the case of GFSK modulation, to accurately track the input frequency, high DCO resolution and gaussian shaped DCO input are required. As a design trade-off, an acceptable DCO step mismatch is invariably allowed in the design.

⁶For 376 bit-long packet, the BLE-RF PHY testing procedure defines the worst-case frequency variation, expected in the received packets, to be a sinusoidal with frequency, 625 Hz and maximum variation, 50 kHz.

Like $\delta f_{n,TX}(t)$, $\delta f_{n,DCO}(t)$, due to DCO phase noise, can be considered analogous to random input noise in the voltage-domain $\Sigma\Delta$ modulator. Its spectral density can be derived from that of DCO phase noise, using the equation below.

$$S_{f,DCO}(f) = f^2 S_{\phi,DCO}(f) \quad (3-23)$$

Resultant spectral density, $S_{f,DCO}(f)$ indicates that $\delta f_{n,DCO}(t)$ has $1/f$ behaviour in the bandwidth of PDC loop. And its $1/f$ corner frequency is same as $1/f^3$ corner frequency of the $S_{f,DCO}(f)$. It is discussed later in Section(3-4-2) with an illustration. In general, one could conclude that DCO phase noise in the PDC loop provides equivalent flicker noise component in the voltage-domain $\Sigma\Delta$ modulator. From earlier analysis, one could realise that the DCO phase noise would also experience transfer behaviour similar to that of BLE input signal.

Finally, similar to constant frequency offset, unchecked frequency noise will induce spikes, bit slips and pulse width variation at the comparator output. It should be noted that impact of frequency noise on the PDC loop is significantly small, due to mixer in the loop. Mixer, being an integrator in the frequency domain, averages the random frequency noise and thus reduces the disturbance at its output. However, the random $1/f$ component due to DCO phase noise, would still cause trouble and requires a background calibration mechanism to cancel them.

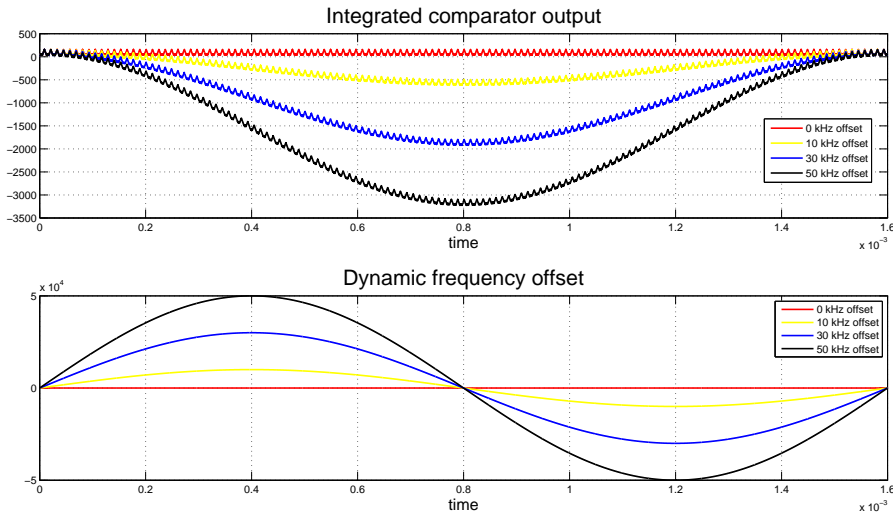


Figure 3-22: Integrated comparator output for dynamic frequency offsets with different variation amplitudes.

3-4-2 AFC loop

As described earlier, the frequency offset and noise affect the zero-crossings at the comparator input and induce pulse width variations. The $\Sigma\Delta$ -modulator model indicates that frequency offset and noise in the signal bandwidth will be transferred to the PDC output without any shaping. Degradation in the loop performance can be minimized by using a background calibration mechanism that continuously extracts the frequency offset and noise from the

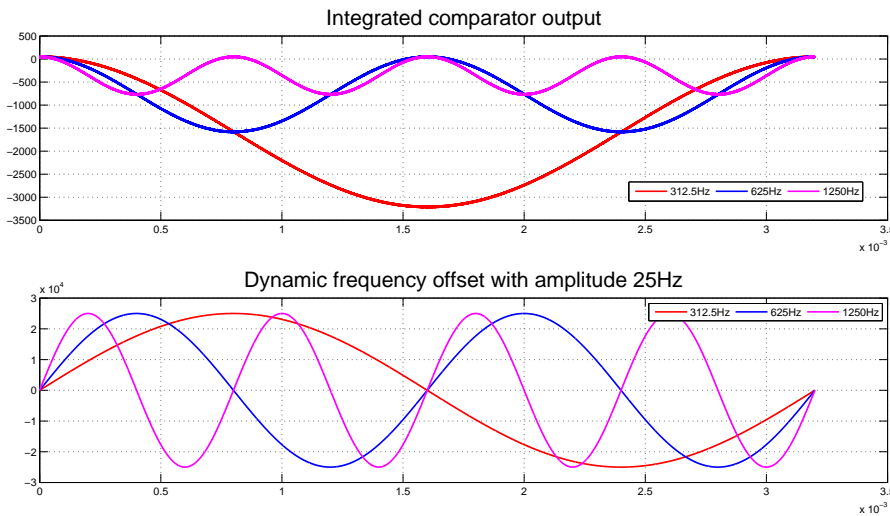


Figure 3-23: Integrated comparator output for dynamic frequency offsets with different variation frequencies.

comparator output and feed it back to the DCO for cancellation. Since the background calibration mechanism behaves as a negative feedback loop and is used to cancel the frequency offset and noise, it is termed as automatic frequency noise cancellation (AFC) loop in this work. Figure 3-24 illustrates direct frequency demodulator (DIFDEM) with both PDC and AFC loop.

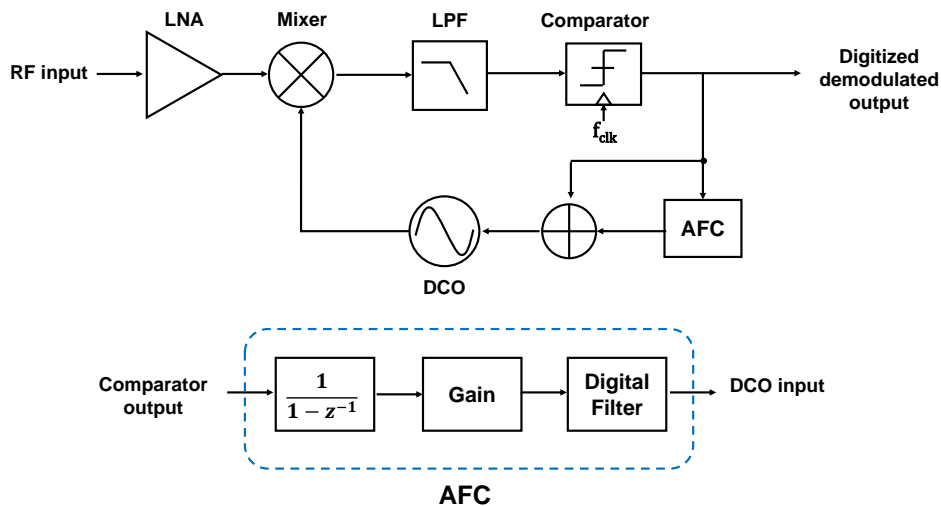


Figure 3-24: DIFDEM with PDC and AFC loop.

One of the identifiable manifestation of the frequency offset and noise in the PDC loop is the pulse width variation at the comparator output. As shown in figure(3-20) - (3-23), the running integration of the comparator output can be used as a rough measure of the frequency

offset and noise. Hence, an AFC block, which integrates the comparator output and uses the integrated output to generate a frequency control word (FCW) for the DCO, is used in this work for frequency offset/noise cancellation.

As shown in Figure 3-24, AFC encompasses an integrator, a variable gain amplifier and a digital LPF. The variable-gain amplifier and digital LPF are added to control the settling behaviour of the loop. Gain of the amplifier and bandwidth of the filter are tuned such that PDC loop meets the frequency tolerance specifications of the BLE standard. For example, the performance of the AFC block for a static offset of 100 kHz is shown in the Figure 3-25. However, the performance of the AFC loop degrades when it is evaluated for longer packets ($>400 \mu\text{s}$), as per new *Bluetooth Low Energy 4.2* standard [38]. Analysing the output of the AFC loop, revealed that the loop responds to the desired input signal and modifies the DCO frequency accordingly.

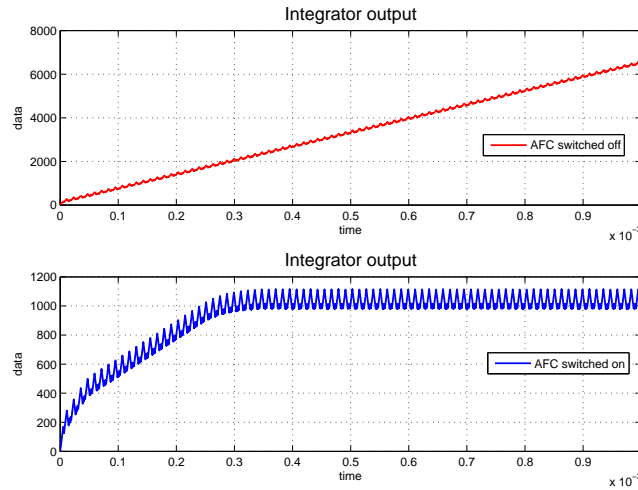


Figure 3-25: Performance of AFC loop in the presence of constant frequency offset of 100 kHz.

On retrospective, this behaviour can be explained by considering PDC loop, as frequency domain $\Sigma\Delta$ modulator and using the spectrum of frequency offset and noise, shown in the Figure 3-26. Troublesome components such as, constant frequency offsets, and $1/f$ frequency noise, occupy lower end of the frequency spectrum. As per BLE test procedure, the maximum frequency of dynamic frequency offset is 625 Hz. Further, nominal $1/f^3$ corner frequency of DCO phase noise would be $<10 \text{ kHz}$. Hence, to filter this low-frequency frequency noise, AFC loop should possess a low-pass behaviour with bandwidth $\sim 10 \text{ kHz}$. This would effectively change the low-pass behaviour of the PDC loop to bandpass, with corner frequencies determined by AFC loop and LPF.

It is obvious that larger the bandwidth of AFC, poorer the tracking ability of the PDC loop. Further, for given AFC bandwidth, longer the packet duration, more the chances of tracking failure of the PDC loop. This explains the high BER in the previous simulation in which packets are longer than $400 \mu\text{s}$. Furthermore, it should be understood that the response time of the AFC loop is inversely proportional to bandwidth. It means AFC with smaller bandwidth would fail to cancel the offset if the packet duration is shorter, say $\sim 400 \mu\text{s}$ for example. This verifies the selection of large bandwidth for AFC loop in first place.

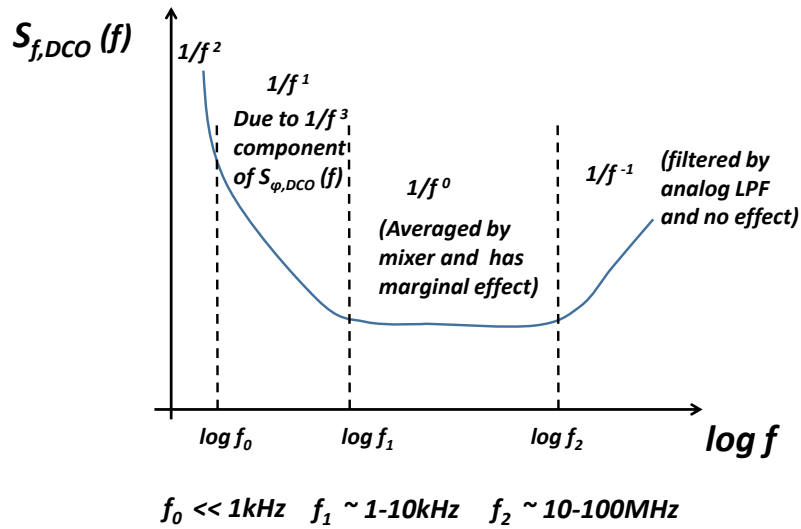
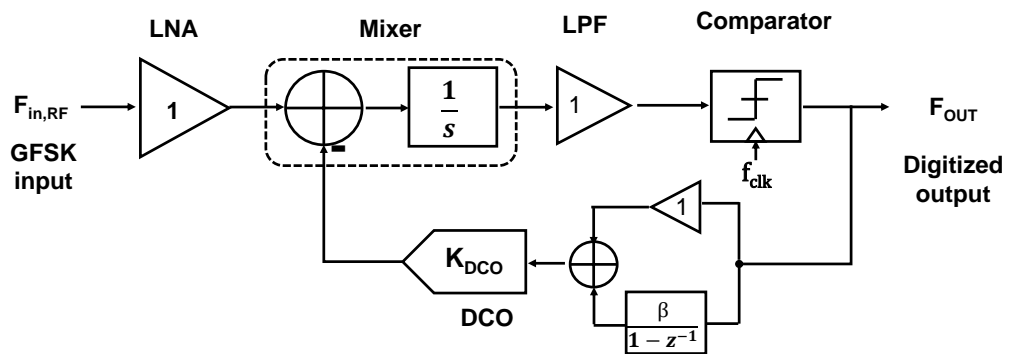


Figure 3-26: Single sided spectrum of frequency noise $S_{\delta f,DCO}(f)$.

For LPF bandwidth \gg 500 kHz



If $\beta \ll 1$, then the integral path can be neglected and the loop behaves as 1st order $\Sigma\Delta$ modulator.

Figure 3-27: $\Sigma\Delta$ modulator model of the DIFDEM with AFC loop.

From this, one could conclude that the correlation between the low-pass behaviour of the AFC loop and the bandpass characteristics of the PDC loop limits the frequency tolerance of the DIFDEM. In this work, the tuning range of variable gain amplifier is increased to address

this bandwidth limitation. However, it is a simple quick fix and more improvement is needed in this regard in future for an optimum solution.

Regarding stability, one could realise that the integrator in the AFC block would change the modelling of $\Sigma\Delta$ -modulator. In this case, it increases the order of the $\Sigma\Delta$ -modulator to 2. The block diagram, shown in Figure 3-27, explains the modelling of the DIFDEM in the presence of the AFC loop. As described in [39], if the AFC loop is slow enough and the frequency change caused by the AFC loop at each update is smaller than that of the comparator output, then the stability of the second-order $\Sigma\Delta$ -modulator would be similar to that of first order $\Sigma\Delta$ -modulator.

3-5 Receiver design

3-5-1 Sensitivity

Sensitivity of the receiver represents the minimum signal level that can be received and demodulated with the desired Bit error rate (BER) by the receiver. Generally, it is calculated using the following expression.

$$\text{Sensitivity} = -174 \text{ dBm/Hz} + 10 \log(BW) + NF + SNR_{min} \quad (3-24)$$

where -174 dBm/Hz is the thermal noise floor; BW refers to the signal bandwidth; NF is the overall noise figure of the receiver; and SNR_{min} is the minimum signal-to-noise ratio required by the demodulator used in the receiver chain to achieve desired BER.

DIFDEM performs both analog signal conditioning and frequency demodulation using a single PDC loop⁷. This intertwines the calculation of noise figure and SNR_{min} for this receiver. Understanding the correlation and calculating these parameters are largely constrained by the non-linear behaviour of the PDC loop. Hence in this section, a simple qualitative description of the noise performance of the DIFDEM, using phase-time representation, is provided. Based on that, extensive time-step simulations are carried out to estimate gain and noise of the individual blocks for desired receiver sensitivity.

Let us consider that input to the comparator, $V_c(t)$, consists of desired signal, $V_{LPF}(t)$ and additive noise, $n(t)$. Represent the instantaneous phase of $V_c(t)$ by $\phi_c(t)$ and that of noise-free $V_{LPF}(t)$ by $\phi_L(t)$. Phase distortion induced by $n(t)$ on $\phi_L(t)$ is termed as $\phi_n(t)$. In other words, $\phi_c(t)$ fluctuates around $\phi_L(t)$ and the amount of fluctuation is determined by $\phi_n(t)$. The situation is clearly illustrated in the Figure 3-28.

Similar to $n(t)$, $\phi_n(t)$ is also stochastic in nature and causes undesired jitter at the comparator output whenever $\phi_L(t)$ crosses or is in the vicinity of phase threshold. The amount of jitter is directly related to the density function of $\phi_n(t)$ and its variance. As long as $\phi_n(t)$ is lesser than $\phi_{s0,1}$ or $\pi - \phi_{s0,1}$ (whichever is stricter), the jitter will be localised around transition edges and can be partially filtered using digital low pass filters. However, not every transition ends up with ϕ_L at $\phi_{s0,1}$ due to interferers and frequency noise. This leads to a much

⁷Additional loop with AFC is used only for low-frequency frequency noise cancellation and hence serves as an accessory feature.

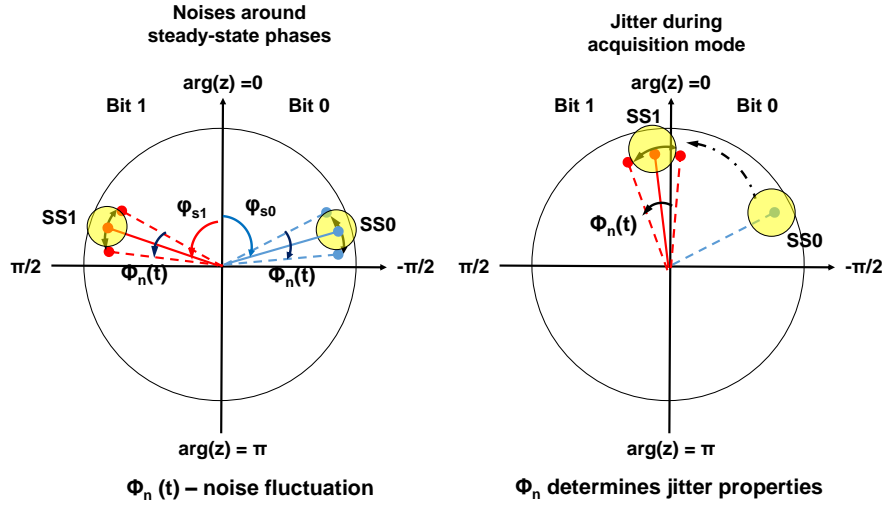


Figure 3-28: Representation of noise and jitter using phasors.

tighter constraint for $\phi_n(t)$. Hence time-step simulations are employed to estimate the $\phi_n(t)$ constraint for acceptable jitter.

Before discussing the simulation set-up, one could realise from the Figure 3-28 that $V_c(t)$ is the resultant vector of $n(t)$ and $V_{LFP}(t)$ and,

$$\phi_n(t) = \sin^{-1} \left(\frac{n(t)}{V_{LFP}(t)} \right) \quad (3-25)$$

With $n(t)$ and $\phi_n(t)$ being stochastic in nature, this relationship can be extended to obtain $\overline{\phi_n(t)^2}$ from noise and signal power spectral densities. For small variations, the $\overline{\phi_n(t)^2}$ can be approximated to $1/(2 \cdot \text{SNR}_i)$, where SNR_i is the signal to noise ratio at the comparator input. This is similar to equivalent phase jitter in the PLL [27]. Further it confirms the familiar understanding that large signal-to-noise ratio (SNR) is needed to achieve low jitter.

Having discussed that, the maximum allowable $\phi_n(t)$ at comparator input should be estimated for PDC loop to achieve BER of 10^{-3} . With relationship between SNR at the comparator input and $\phi_n(t)$ already established, estimating minimum SNR at the comparator input for BER of 10^{-3} would be a much simpler procedure. Proceeding on that direction, time-step simulations have been performed for different SNR and the obtained results, shown in Figure 3-29, revealed that minimum SNR of 12 dB is required at comparator input to achieve desired performance. Additional 3 dB margin is added in the subsequent calculations for worst-case scenario.

Using Friis' formula, SNR at comparator input is referred back to the receiver input and used to determine the receiver sensitivity. In other words, estimated SS SNR is used in the place of SNR_{min} in Equation(3-25) to calculate receiver sensitivity. It indicates that noise figure of the receiver (from receiver input to comparator input) should be <8 dB to achieve the desired sensitivity of <-90 dBm.

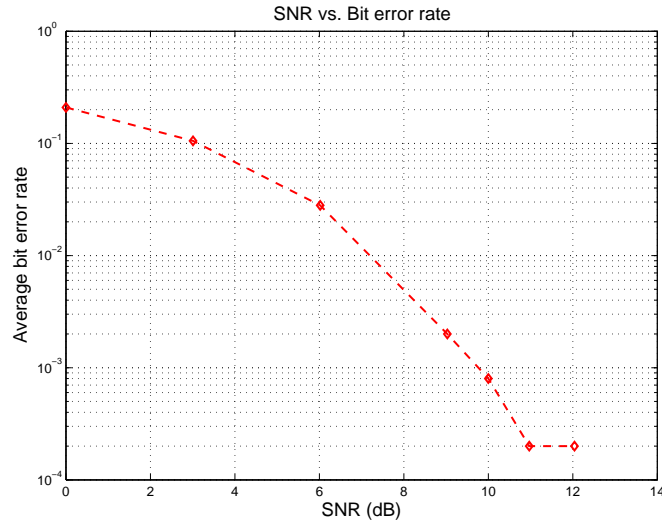


Figure 3-29: Simulation results of SNR vs. bit error rate.

Table 3-1: Gain and noise requirements for blocks in the DIFDEM receiver.

Blocks	Gain	Noise figure / Noise
LNA	25 dB	5 dB NF
Mixer	25 dB	-89 dBm ($10 \text{ nV}/\sqrt{\text{Hz}}$)
LPF	36 dB	-76 dBm

The operating point of the comparator, together with receiver sensitivity, is used to calculate the gain requirements of the individual blocks in the receiver chain. On considering the operating point of comparator to be -10 dBm⁸ and target sensitivity of <-90 dBm, the overall receiver gain is calculated to be >80 dB. Trade-off with linearity constraints are evaluated while selecting individual gain and noise requirements. After few iterations. specifications, summarized in Table (3-1) are adopted for the receiver.

3-5-2 Selectivity

Selectivity describes the rejection performance of the receiver to both in-band and out-of-band interferers. As summarized in Table (1-1), adjacent channel rejection ratio (ACR) stipulates acceptable levels of in-band (2400 - 2483.5 MHz) interferers whereas blocking performance specifies acceptable levels of out-of-band interferers.

For the attenuation of out-of-band interferers, LNA is optimized to provide desired bandpass response around 2.45 GHz. Further, LPF after frequency down-conversion ensures that any residual out-of-band interferes will be effectively suppressed out.

As mentioned in Chapter 2, LPF is the only block in the PDC loop that filters the in-band interferers and thus solely determines the overall ACR performance of the receiver. On

⁸-10 dBm is equivalent to 100 mV in 50 Ω system

the other hand, the phase response of the LPF determines several functional characteristics of the PDC loop, as elaborated in Section (3-3). Hence, filter selection should involve both magnitude constraints, for desired ACR and phase constraints, for optimum loop functionality.

Phase constraints

Following are the constraints related to LPF phase response, obtained from the analyses carried out in the earlier sections.

- Phase response of LPF at frequency, $2\Delta f$ determines the steady-state phase ($\phi_{s0,1}$) of the PDC loop in the static mode. So, the phase response should be between 0° and -180° for stability. Additional margin should be allowed to account for frequency offsets and transient delays of comparator and DCO.
- For fast response time and large DC offset tolerance, LPF phase response at $2\Delta f$ should be as close to 0° as possible.
- To be more robust against frequency noise (both drift and phase noise) and amplitude noise, the steady-state phase should be closer to $\pm 90^\circ$.

Since being robust to frequency and amplitude noise is of prime importance, the LPF phase response target at $2\Delta f$ is set to be around -90° . Though, it safely meets the stability condition, the response time is traded-off in this selection. Additional measures, such as Offset cancellation loop, are needed to improve the DC offset tolerance of the receiver. Crippled by 1-bit comparator, a simple current-steering DAC without feedback loop will be used in this work to trim the DC offsets manually. A multi-bit analog-to-digital converter (ADC) would facilitate Offset cancellation loop and should be considered for future work.

Magnitude constraints

Similar to additive noise, interferers at the input of the comparator induce phase fluctuations, which invariably result in jitter at the comparator output. Therefore, the conditions for minimal jitter should also be considered together with ACR specifications in determining LPF magnitude response.

For a brief understanding of the induced phase fluctuations at the comparator input, consider an input signal, $V_{LPF} \cos(2\pi f_o t)$ with an interference, $V_{if} \cos(2\pi(f_o + f_\Delta)t)$ at the input of the comparator. Let $\Delta\phi$ be the additional phase delay experienced by the interferer with respect to the input signal. Then,

$$V_c(t) = V_{LPF} \cos(2\pi f_o t) + V_{if} \cos(2\pi(f_o + f_\Delta)t + \Delta\phi) \quad (3-26)$$

Rewriting it, would result,

$$V_c(t) = \left[V_{LPF} + V_{if} \cos(2\pi f_\Delta t + \Delta\phi) \right] \cos(2\pi f_o t) - V_{if} \sin(2\pi f_\Delta t + \Delta\phi) \sin(2\pi f_o t) \quad (3-27)$$

Equation(3-27) indicates that interferer causes both amplitude and phase modulation. Comparator suppresses the amplitude modulation and leaves only phase fluctuations at its output. The amount of phase fluctuation can be given as,

$$\phi_f(t) = \tan^{-1} \left[\frac{V_{if} \sin(2\pi f_\Delta t + \Delta\phi)}{V_{LPF} + V_{if} \cos(2\pi f_\Delta t + \Delta\phi)} \right] \quad (3-28)$$

$$= \frac{V_{if}}{V_{LPF}} \sin(2\pi f_\Delta t + \Delta\phi) \quad \text{for } V_{if} \ll V_{LPF} \quad (3-29)$$

The ratio of amplitudes of interferer and signal, as shown in Equation(3-29), determines the acceptable jitter at the comparator output. Like sensitivity analysis, time-step simulations are performed for different amplitude ratios with interferers at 2 MHz and 3 MHz. Obtained results suggest that the ratio should be at least 12 dB for 10^{-3} BER.

Adding the minimal jitter constraint of 12 dB to the desired ACR target concludes that LPF should provide at least 32 dB and 42 dB attenuation at 2 MHz and 3 MHz respectively. Further, LPF bandwidth should be >500 kHz, as it should accommodate $2\Delta f$ signal in the dynamic mode. Frequency drift and phase noise are duly considered in finalising the bandwidth to be 600 kHz.

To achieve minimum bandwidth of 600 kHz, attenuation of 32/42 dB at 2/3 MHz and close to -90° phase response at 500 kHz, a 3rd order elliptic filter with a complex pair of zeros at 2 MHz is adopted in this work. The benefit of zeros at 2 MHz is two-folded: (i) it provides very high attenuation at 2 MHz; and (ii) it compensates for phase-lag introduced by the poles in the filter. Hence, by carefully optimizing the pole location, the bandwidth of 600 kHz and phase response of -90° at 500 kHz can be realised. Desired 42 dB attenuation at 3 MHz also plays a role in selecting poles. Considering these, a complex pair of poles at 640 kHz and a real pole at 390 kHz are chosen for this filter. The BER performance of the PDC loop with elliptic filter for difference interference strengths at 2/3 MHz are plotted in Figure 3-30. The results indicate that target ACR specifications are achieved.

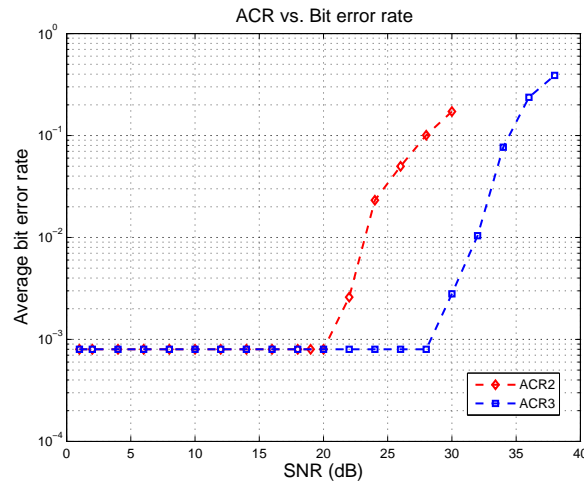


Figure 3-30: Simulation results of adjacent channel rejection ratio vs. bit error rate.

3-5-3 Linearity

On a different note, ACR performance determines the maximum signal strength allowed in the signal path and thereby defines certain linearity constraints of the receiver. To be specific, 1 dB input compression point of the receiver can be estimated from ACR specification using the below expression.

$$P_{1\text{dB}} = \text{Sensitivity} + \text{ACR} \quad (3-30)$$

where, *Sensitivity* is the target sensitivity of the receiver (-90 dBm), *ACR* is the worst-case ACR specification (-30 dB @ 3 MHz). Applying these values in the above equation and including additional 10 dB margin would define the target $P_{1\text{dB}}$ to be -50 dBm. Employing cascade analysis $P_{1\text{dB}}$ requirement of the individual blocks in the receiver chain are determined.

For third-order intermodulation, BLE standard specifies that the system should receive and demodulate the signal of strength -64 dBm with BER of 10^{-3} in the presence of two blocker tones with power of -50 dBm. Since, intermodulation components, generated by 3rd order non-linearity falls in the wanted signal channel, they can be evaluated, similar to noise. Applying the conditions derived for noise analysis, the IM3 level at the receiver input can be calculated as follows.

$$IM3 = P_{in,tone} - [-64\text{ dBm} - SNDR - NF] \quad (3-31)$$

where *NF* is the noise figure of the receiver (7-8 dB, from sensitivity analysis); $P_{in,tone}$ is the power of two tones that causes intermodulation, in this case it is -50 dBm; and *SNDR* is the minimum signal to noise-distortion ratio expected at the comparator input. Using results obtained from time-step simulations in noise analysis, SNDR should be at least 12 dB at the comparator input. Applying all these values in the above equation, one could get the maximum allowable IM3 level at the receiver input to be 34 dBc.

With IM3 level and input power for two-tone analysis are known, the target IIP3 at receiver input is calculated to be -30 dBm using the equation below.

$$IIP3 = P_{in,tone} + \frac{IM3}{2} + 3\text{ dB} \quad (3-32)$$

Once again, employing cascade analysis, the IIP3 requirements of individual blocks in the receiver are determined.

It should be mentioned that, though explicit targets for IIP2 are not calculated for the individual blocks, the overall DC offset at the comparator input is kept as minimum as possible. Further, an offset-trimming DAC, that works on current-steering principle, has been included in the receiver chain to manually reduce the DC offset.

Chapter 4

Circuit design

This chapter describes the design and implementation of analog and digital blocks: current-driven passive mixer, programmable low-pass elliptic filter and an automatic frequency noise cancellation (AFC). These blocks are implemented in TSMC LP 40 nm CMOS process.

4-1 Mixer

Mixer produces a baseband output signal that is proportional to the instantaneous phase difference of its RF inputs: LNA and digitally controlled oscillator (DCO). Being the first block in the phase-to-digital conversion loop, its behaviour largely affects the overall performance of the phase-to-digital conversion (PDC) loop and the receiver. Based on the analyses and discussions carried out in Chapter 3, the required specifications for mixer implementation are listed out in Table 4-1. Since the receiver is targeted for ultra-low power *Bluetooth Low Energy* (BLE) applications, it is essential that mixer has to be low power while meeting the specifications. Hence current driven passive mixer structure is chosen for implementation in this design. The mixer receives single-ended low noise amplifier (LNA) output and feeds low pass filter (LPF) with a differential output. The general design considerations for the current-driven passive mixer are discussed next. It is followed by design of its building blocks: transconductor, passive mixer and transimpedance amplifier. The post-layout simulations are covered in Chapter 5.

Table 4-1: Target specifications for RF mixer.

Parameter	Target
Current consumption	$< 350 \mu\text{A}$
Conversion gain	25 dB
Input-referred noise	$\sim 10 \text{ nV}/\sqrt{\text{Hz}}$ ($\approx -89 \text{ dBm}$)
Output compression point, OP1dB	$\sim 0 \text{ dBm}$

4-1-1 Architecture selection

Analog multipliers or mixers are selected as phase detectors in the PDC loop for their immunity to strong interferers [4]. Like the desired radio frequency (RF) signal, they also down-convert the interferers to baseband which can be filtered later using LPF. For this design, Gilbert mixer and its switching variants [19][40] can be considered for their high conversion gain as it would relax the design specifications of LPF and improve the receiver sensitivity. A single-balanced¹ Gilbert switching mixer is shown in Figure 4-1.

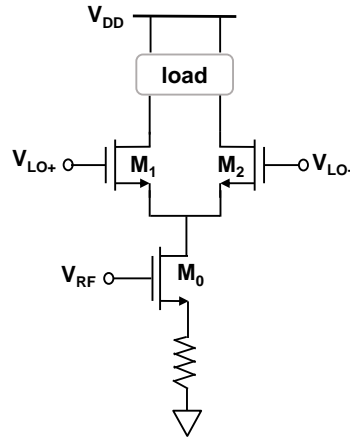


Figure 4-1: Single balanced active CMOS mixer.

All DC tail current flows through the transconductor, switching transistors and load impedances. The $1/f$ noise of tail transconductor is frequency translated at the output due to mixing action. On the other hand, $1/f$ noise of switching transistors appears at the output without frequency translation. In zero-IF architecture, this flicker noise could overwhelm the desired signal in the band of interest and degrade the overall noise performance of the receiver. Any measures to improve the noise figure either affect the mixer linearity or increase the circuit complexity and power consumption [41]. Further, stacked transistors undermine the performance of the mixer at low supply voltage.

Unlike Gilbert switching mixers, current-driven passive mixer, proposed in [42], simply commutates the RF current supplied by a RF transconductor (Figure 4-2). Since the mixer switches carry no DC current, its flicker noise contribution at the output is negligible. The down-converted mixer current is fed to a transimpedance amplifier (TIA) to produce baseband voltage. Typically, the feedback loop of the TIA provides the dc bias to the input and output terminals of the mixer. For efficient switching, the transistors in the mixer are usually biased in the deep-triode region with switching resistance, R_{SW} .

$$R_{SW} = \frac{L}{\mu_n C_{ox} W (V_{GS} - V_{TH} - V_{DS})} \quad (4-1)$$

where, V_{GS} and V_{DS} are the gate-source and drain-source voltages respectively, μ_n is the channel mobility, C_{ox} is the gate oxide capacitance and W and L are the width and length of the switch.

¹Single ended LNA is re-used in this work, hence single balanced mixer

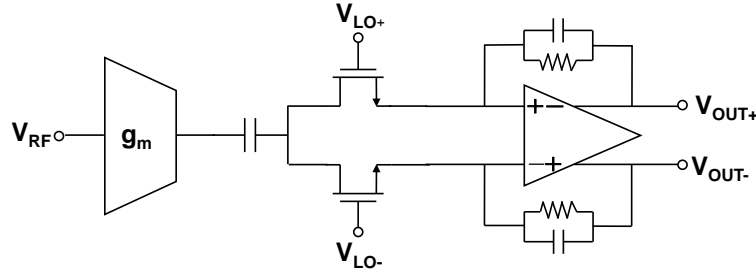


Figure 4-2: Single balanced passive CMOS mixer.

Due to its low input impedance, TIA keeps the voltage swing across the switches very small (ideally 0 V) and makes it highly linear [43]. Further, the desired high conversion gain can be achieved by carefully choosing the transconductance and load impedance. Additionally passive mixers pose modest voltage head-room requirements. This attribute makes them suitable for low-voltage operation.

For completeness, voltage-driven passive mixer is not selected as it provides low gain and has poor linearity due to voltage swing across the switches [44].

4-1-2 Design considerations

The conversion gain, noise and linearity performance of current-driven passive mixer are analysed in this section. A qualitative approach is followed to understand noise and distortion mechanisms and a few design considerations are inferred to achieve the desired performance.

The simplified model of the single-balanced current-driven passive mixer, shown in Figure 4-3, is used for discussion in this section. The transconductor is modelled with a voltage-dependent current source with an output impedance, $Z_L(s)$. It is coupled to the switching transistors, M1 and M2 through a coupling capacitance, C_c . TIA is modeled with an operational amplifier (opamp) and load impedance, $Z_{load}(s)$. The switching transistors are driven by an ideal local oscillator (LO) signal, a 50% duty-cycle rail-to-rail square wave with frequency ω_{LO} .

Gain

The overall voltage gain for RF to baseband conversion due to fundamental tone mixing can be approximated as

$$\frac{V_{out}(f_{out})}{V_{in}(f_{rf})} = \frac{2}{\pi} g_m Z_{load}(f_{out}) \quad (4-2)$$

where,

$$Z_{load}(f_{out}) = \frac{R_F}{1 + j2\pi f_{out} R_F C_F} \quad (4-3)$$

Here, g_m is the trans-conductance of the input stage, the factor $2/\pi$ is related to the first harmonic amplitude of periodically time-varying mixer transfer function [40], R_F and C_F are the components of load impedance, shown in Figure 4-3.

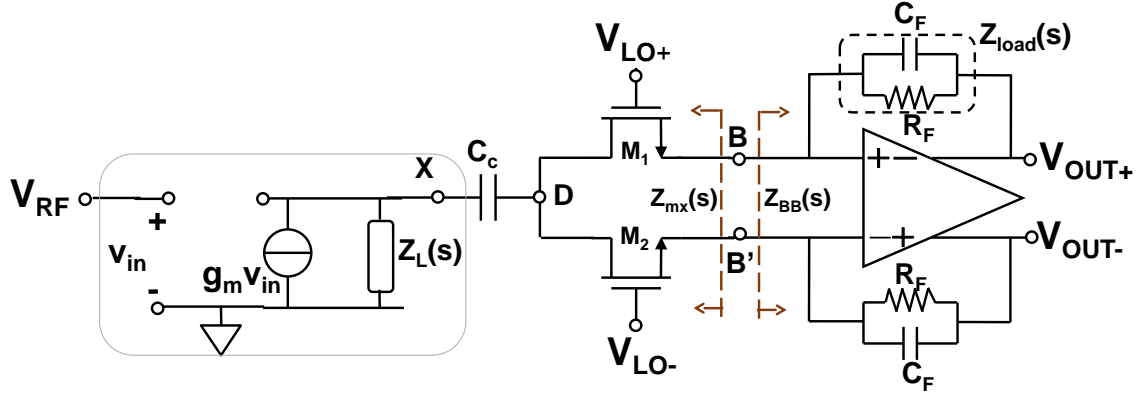


Figure 4-3: A simplified model of single balanced passive CMOS mixer.

In contrast to active mixers, current-driven passive mixers provide no reverse isolation between the RF and baseband nodes [45]. As a result of this lack of reverse isolation, the baseband impedance of TIA is frequency-translated to ω_{LO} and its odd harmonics. Hence, the low pass filter at TIA load becomes a bandpass filter around ω_{LO} , when seen from the mixer input (Figure 4-4). This property can be used to suppress out-of-band blockers in the received input [46] and to improve the receiver blocker tolerance level and 1 dB linearity of the subsequent elliptic filter. Care should be taken in choosing optimum corner frequency so that the desired signal experiences negligible phase delay.

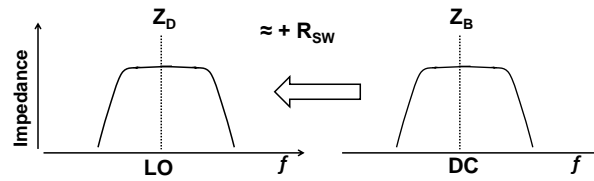


Figure 4-4: Impedance transfer - an illustration.

Due to no reverse isolation, the impedance seen at node X can be given as,

$$Z_X(f_{LO}) \approx Z_L(f_{LO}) \parallel \left[R_{SW} + \frac{2}{\pi^2} Z_{BB}(f - f_{LO}) \right] \quad (4-4)$$

where $Z_L(f_{LO})$ is the output impedance of transconductance at frequency, f_{LO} , R_{SW} is the on-

resistance of the switch and $Z_{BB}(f)$ is the TIA input impedance. Let $R_{SW} + \frac{2}{\pi^2}Z_{BB}(f - f_{LO})$ is the load impedance seen by the transconductor.

Depending on the ratio of load impedance to output impedance of transconductance, only a fraction of RF current (I_{RF}) will be transferred to the switching stage for conversion and available at TIA input (I_{BB}). Hence, to achieve high current conversion (I_{BB}/I_{RF}), $Z_L(f_{LO})$ should be as high as possible whereas R_{SW} and $Z_{BB}(f)$ should be as low as possible [45]. Though, sizing up switching transistors could minimize R_{SW} , it should be done carefully as it also increases parasitic capacitance at switching nodes. Large LO swing with sharp transition enables transistors to turn on in triode mode and hence low R_{SW} . Equation (4-5) provides an approximate relation between TIA input impedance, $Z_{load}(f)$ and opamp DC gain, A_{DC} . It indicates that the TIA opamp should have high DC gain to achieve low $Z_{BB}(f)$. Also, unity gain bandwidth of opamp should be larger than the signal bandwidth.

$$Z_{BB}(f) \approx \frac{2Z_{load}(f)}{A_{DC} + 1} \quad (4-5)$$

Noise

For a linear periodically time-varying (LPTV) system like mixer, an input signal at a given frequency produces a discrete set of output frequencies. Such non-linear behaviour of the system complicates its noise analysis. Since a thorough and systematic analysis of a LPTV system is beyond the scope of this work, a widely-adopted, simple qualitative model for the mixer noise analysis is employed here.

In this model, the total noise at the mixer output is contributed by three major sources: transconductor, switching stage and TIA. Due to coupling capacitor C_c , flicker noise of the transconductor will not be transferred to the switching stage and mixer output. For an ideal LO signal, the white noise of transconductor around the frequencies, $(2k+1)\omega_{LO}$ for $k \in N$, will be down-converted to baseband at the output. The single sided power spectral density (PSD) of the noise current at the mixer output can be given as [47],

$$S_{n,gm}(f_{out}, f_{RF}) = 4kT\Gamma g_m \zeta^2 |Z_{load}(f_{out})|^2 \quad (4-6)$$

where, k is the Boltzmann's constant, T is the temperature in kelvin, Γ is a noise factor that accounts for all the noise contribution of transconductor and ζ^2 accounts for the periodic switching behaviour, including noise-folding due to mixing with higher harmonics.

Since switching transistors commute only RF current and the receiver exhibits narrowband behaviour, it is safe to assume that contribution of flicker noise of switching transistors at mixer output is negligible [48]. The white noise due to switching resistance, R_{SW} is transferred to the mixer output with a conversion gain as shown in

$$S_{n,sw}(f_{out}, f_{RF}) = \frac{4kT}{R_{SW}} \left| \frac{R_{SW}}{R_{SW} + Z_{mx}(f_{RF})} \right|^2 \zeta^2 |Z_{load}(f_{out})|^2 \quad (4-7)$$

where, Z_{mx} is the effective impedance¹ looking into the switches seen from TIA. If the output impedance of the transconductor is high, then Z_{mx} is composed of R_{SW} and parasitic capacitance, C_{PAR} at the mixer input.

¹for direct conversion receiver f_{RF} and f_{LO} can be used interchangeably.

The input referred noise of the opamp, $S_{n,opamp,in}$ contains components of both flicker noise and white noise. Its contribution at the mixer output is given as

$$S_{n,opamp}(f_{out}, f_{RF}) = S_{n,opamp,in} \left| 1 + \frac{2Z_{load}(f_{out})}{Z_{mx}(f_{RF})} \right|^2 \quad (4-8)$$

Finally, the noise contribution of load impedance $Z_{load}(f)$ at mixer output is

$$S_{n,load}(f_{out}, f_{RF}) = \frac{4kT}{R_F} |Z_{load}(f_{out})|^2 \quad (4-9)$$

The total output noise at the mixer output can be obtained by summing up the individual noise contributions given in (4-6)-(4-9). On dividing it by voltage gain of the mixer would give the PSD of total input-referred noise of the mixer.

$$S_{n,in}(f_{out}, f_{RF}) = \frac{4kT\Gamma}{g_m} \left| \frac{\pi}{2}\zeta \right|^2 + \frac{4kT}{R_{SW}} \left| \frac{\pi\zeta R_{SW}}{2g_m(R_{SW} + Z_{mx}(f_{RF}))} \right|^2 + \frac{S_{n,opamp,in} \left| 1 + \frac{2Z_{load}(f_{out})}{Z_{mx}(f_{RF})} \right|^2}{\left| \frac{2}{\pi}g_m Z_{load} \right|^2} + \frac{4kT}{R_F} \left| \frac{\pi\zeta}{2g_m} \right|^2 \quad (4-10)$$

This expression can be used as the basis for noise optimization of the mixer. Some of the important conclusions derived from the expression are given below:

- In general, the total input-referred noise can be minimized by choosing large g_m , at the expense of power and linearity.
- Usually, the noise due to switching transistors are much smaller than the other sources. If measures are taken to minimize R_{SW} , it can be safely neglected for any further optimization.
- Focussing on the input-referred noise of opamp, the expression (4-10) indicates that it is inversely related to Z_{mx} i.e., it increases when Z_{mx} decreases. If R_{SW} is small, Z_{mx} will be dominated by parasitic capacitance, C_{PAR} . Due to its switching behaviour, the resistance of C_{PAR} can be given as

$$R_{par} = \frac{1}{2f_{LO}C_{PAR}} \quad (4-11)$$

Combining (4-10) and (4-11) implies that parasitic capacitance should be reduced to minimize the contribution of opamp noise. Opamp being the main source of flicker noise in mixer, magnifies the importance of parasitic capacitance.

- Opamp should be designed with low flicker ($1/f$) noise.

Linearity

Similar to noise analysis, a qualitative approach is used here to understand the large signal behaviour of mixer and to obtain a few design considerations for high linearity performance.

The input-output relationship of transconductor can be modelled as

$$i_{RF}(t) = g_m v_{in} + \alpha_2 v_{in}^2 + \alpha_3 v_{in}^3 + \dots \quad (4-12)$$

Employing above relation for an input RF signal $V_{in} \cos(\omega_{RF}t)$, the second-order distortion terms will occur at DC and $2\omega_{RF}$. The coupling capacitor, on-resistance of switch and low-pass RC load of TIA together provides a bandpass filtering around ω_{RF} for the transconductor outputs. The IM_2 distortion terms at DC and $2\omega_{RF}$ lie in the stop-band of this band-pass filter and get filtered out. Only in the presence of widely spaced blockers (around $2\omega_{RF}$), the second-order non-linearity of the transconductor affects the mixer. On other cases, like this narrow band receiver, it has no effect on the mixer.

For an input signal of $V_{in} \cos(\omega_{RF}t) + V_x \cos((\omega_{RF} + n\Delta\omega)t)$, with $\Delta\omega \ll \omega_{RF}$, the IM_3 distortion terms lie in the pass-band of the above-said band-pass filter and directly appear at TIA output. Since channel filtering occurs only after the mixer, it is essential for the transconductor to have high IP_3 to allow strong interferers from adjacent/alternate channels to pass through. As discussed in Chapter 3, the desired adjacent/alternate channel rejection ratio can be used to determine the IP_3 of the mixer and transconductor.

The linearity of the on-resistance determines the linearity of the switching transistors. The on-resistance can be expressed using Equation (4-1). Employing a LO signal close to an ideal square wave with 50% duty cycle minimizes the non-linearity due to mismatch in threshold voltage (V_{TH}) of the switching transistors. Non 50% duty cycle will cause IM_2 distortions and produce DC offset at the TIA output.

Variation in $\mu_n C_{ox} W/L$ also causes second-order non-linearity [49]. Sizing up the transistors would diminish this non-linearity at the cost of increased parasitic capacitance and noise. Besides minimizing $\mu_n C_{ox} W/L$ variation, sizing up also reduces the average R_{SW} . Indirectly, it also reduces the bias point variation across the switching terminals ($V_{DS} \approx 0V$) and improves the linearity. On the other hand, to minimize small signal v_{DS} variations due to RF input (signal + interferers) and to achieve high IP_3 for mixer, the input impedance of TIA should be as small as possible and the output impedance of transconductor should be as high as possible [50].

The DC input impedance of TIA, given in Equation (4-5), points out that high opamp gain is required to achieve low input impedance for TIA. Also, high opamp gain increases the loop-gain of the TIA and thereby enhances the linearity performance of TIA. However, since opamp gain is a function of frequency, a detailed expression for TIA input impedance and loop gain should be used for more insight.

Taking opamp as a single pole amplifier¹ for simplicity, its voltage gain and unity gain-bandwidth (GBW) can be given as:

$$A(s) = \frac{A_{DC}}{1 + j(s/\omega_c)} \quad \text{and} \quad GBW = \omega_c A_{DC} \quad (4-13)$$

¹Here s is used as Laplace variable instead of f for simpler analysis. Also, note $s = j2\pi f$

Using that, the input impedance and loop gain of TIA can be calculated as:

$$Z_{BB}(s) = \frac{\omega_{tia} R_F (s + \omega_c)}{s^2 + s [\omega_c (1 + A_{DC}) + \omega_{tia}] + \omega_{tia} \omega_c [1 + A_{DC}]} \quad (4-14)$$

$$\text{Loopgain, } T(s) = A_{opamp}(s) \frac{Z_{mx}(s)}{Z_{mx}(s) + Z_{load}(s)} \quad (4-15)$$

where, $\omega_{tia} = 1/R_F C_F$ is the corner frequency of TIA filter. These equations advocate for a large unity gain-bandwidth for the opamp, together with high DC gain for high TIA linearity and low input impedance.

Besides switching transistors and TIA, another mechanism responsible for DC offsets is self-mixing. It is due to parasitic coupling of strong LO signals to the input of the mixer and/or the transconductor. LO-RF coupling at the mixer input creates DC offset and degrades the performance of PDC loop. If LO couples to the input of the transconductor, it creates IM_2 distortion due to cross-modulation. RF-LO leakage also adds up to the dc offset at the mixer output. Hence, careful measures should be taken during layout and routing to reduce the parasitic coupling between LO and RF ports.

Looking back on this section, one could conclude that conversion gain, noise and linearity performance trade-off with each other. All these trade-offs in the mixer design should be considered while designing the mixer for desired specification. Since low power consumption is the ultimate goal of this work, it should also be involved in the design optimization.

4-1-3 Building blocks - transconductor

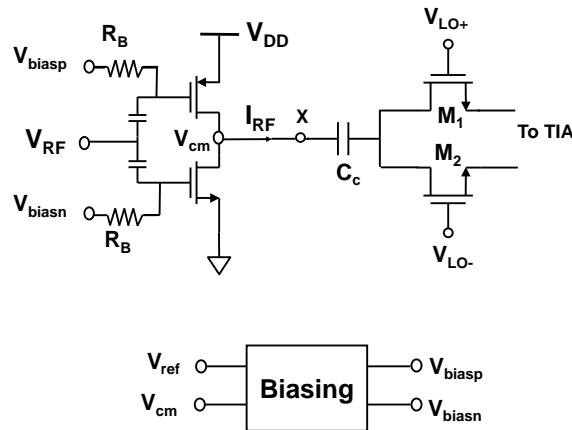


Figure 4-5: Transconductor, feedback biasing and passive mixer.

Figure 4-5 shows the transconductance stage of the mixer. It comprises of a CMOS inverter-based transconductor and a feedback biasing circuit. The output of transconductor is AC coupled to the passive mixer.

The transconductance, g_m , of the CMOS inverter is

$$g_m = g_{mn} + g_{mp} \quad (4-16)$$

where g_{mn} and g_{mp} are the transconductances of the NMOS and PMOS transistors respectively. Since both the transistors use same biasing current, I_D , it can achieve high gain and high power efficiency (g_m/I_d) as well as low noise figure.

Their inherent complementary structure enables CMOS inverter based transconductors to be highly linear. As explained in [51], if the β factors of NMOS and PMOS transistors are perfectly matched, the distortion terms due to PMOS transistor will be cancelled by that of NMOS transistors. This cancellation relies on proper biasing and sizing and sensitive to process, voltage and temperature (PVT) variations. Further, the low output impedance of inverter, due to virtual ground at the mixer output, reduces the voltage swing at output node and enhances transconductor linearity.

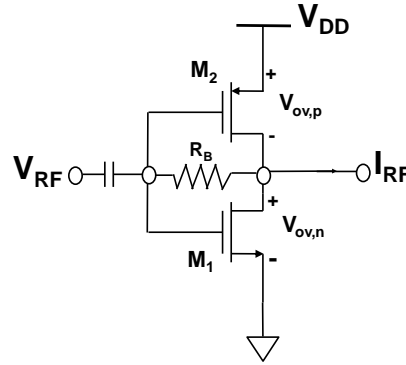


Figure 4-6: Transconductor with self-biasing.

For low voltage operation, it is necessary to determine the minimum desired supply voltage, V_{DD} for the transconductor [33]. Consider a CMOS inverter in the Figure 4-6, the overdrive voltages of M1 and M2 can be given as

$$\begin{aligned} V_{ov,n} &= V_{bias} - V_{t,n} \\ V_{ov,p} &= V_{DD} - V_{bias} - V_{t,p} \end{aligned} \quad (4-17)$$

where, V_{bias} is the biasing voltage applied to the transistors M1 and M2. Usually M1 and M2 are self-biased at $V_{DD}/2$ using large feedback resistance. The minimum supply voltage desired for transconductor can be expressed as

$$V_{DD,min} = V_{ov,n} + V_{ov,p} + V_{t,n} + V_{t,p} \quad (4-18)$$

Since typical threshold voltage for TSMC 40 nm CMOS process is in the range of 400–550 mV, Equation(4-18) implies that $V_{DD,min}$ should be higher than 1.1 V. Further, using a supply voltage less than $V_{DD,min}$ would degrade the performance of transconductor drastically. The transconductor is simulated at lower supply voltages to quantify the magnitude of degradation. Since I_{DC} of transconductor is proportional to its g_m , it is used as an approximate

Table 4-2: Transconductor vs supply voltage.

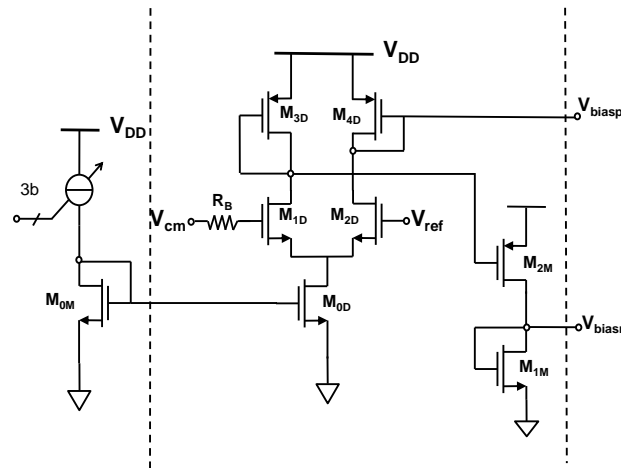
VDD (V)	I _{DC} (μA)
0.9	12.4
1	27.4
1.1	51.7

indicator for the performance of the transconductor. The simulation results are tabulated in Table 4-2. It delineates that a 10% reduction in the supply voltage would diminishes the bias current by 50%. Hence additional circuit techniques are needed to realize low voltage transconductor. Fortunately, a simple technique of employing separate biasing for NMOS and PMOS transistors would repress this supply voltage limitation. If V_{biasn} and V_{biasp} are biasing voltages of M1 and M2, then Equation(4-18) becomes

$$V_{DD,min} = V_{ov,n} + V_{ov,p} + V_{t,n} + V_{t,p} + V_{biasp} - V_{biasn} \quad (4-19)$$

and choosing V_{biasn} larger than V_{biasp} would minimize the supply voltage requirement of the transconductor.

While considering the methods to bias the transconductor, it should also be noted that its conversion gain and linearity are sensitive to bias current. Hence to limit the variations in the bias current and to bias N/PMOS transistors in the transconductor, a feedback bias circuitry is implemented. As shown in Figure 4-7, it consists of a differential amplifier and current-mirrors to regulate the biasing voltage. The current-mirrors are sized appropriately so that the biasing condition of $V_{biasn} > V_{biasp}$ is satisfied and supply voltage (VDD) of 0.85 V is enough to achieve targeted gain. To ensure stability, a phase margin $>60^\circ$ is maintained while sizing the current mirrors and biasing resistors.

**Figure 4-7:** Feedback biasing.

The length of transistors in the transconductor is selected to be 100 nm. The total width of PMOS is chosen to be twice that of NMOS. The ratio is chosen so that both the transistors have same $\mu_n C_{ox} W/L$ factor, enabling high transconductor linearity [51]. Further, the width

and biasing of the transistors are optimized together with TIA and its load impedance to achieve a maximum gain ~ 27 dB. It resulted in a transconductance of ~ 2 mS.

Since opamp noise and mixer SNR degradation is directly proportional to parasitic capacitance between transconductor and mixer, additional care is taken during layout and routing to minimize it. As a result of low parasitic capacitance, the specification for total input referred noise of the opamp in 1 MHz bandwidth is relaxed to -76 dB, providing a scope for power reduction. Dummy transistors are added to the N/PMOS transistors to improve the matching performance and decoupling capacitors are added to minimize supply voltage fluctuations. The physical layout of the transconductor is presented in Figure 4-8.

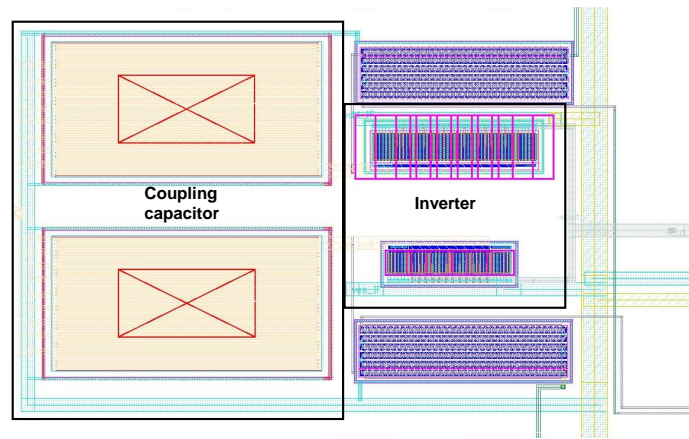


Figure 4-8: Transconductor - layout.

4-1-4 Building blocks - passive mixer

The RF current from the transconductor is AC coupled to the passive mixer. A coupling capacitance of 500 fF is chosen as a trade-off between gain, noise and linearity performance. Owing to its single ended input, a single-balanced structure with two NMOS switches is implemented as a passive mixer (Figure 4-5). NMOS transistors are preferred over PMOS transistors for their low on-resistance, R_{SW} . The DC bias point of the source and drain terminal is set at $0.4 \cdot V_{DD}$ using TIA feedback load. The gate terminals of switches are driven by LO output of DCO buffer.

The rail-to-rail LO swing improves the gain, linearity and noise performance of the mixer. Further reduction in on-resistance can be achieved by sizing up the transistors. However, increased opamp noise and LO power consumption due to the increase in parasitic capacitance determine the upper limit on the size of the transistors (8 $\mu\text{m}/40$ nm). Similar to transconductors, dummy transistors are added to improve the matching performance. Layout and routing is done as symmetrical as possible to minimize the DC offset. The physical layout of the passive mixer is given in Figure 4-9.

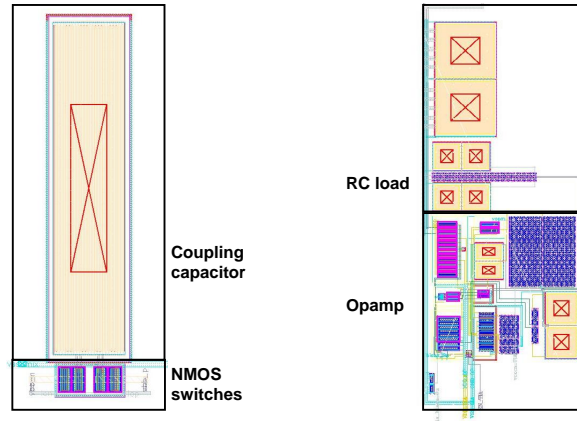


Figure 4-9: Layout of the passive mixer and TIA.

4-1-5 Building blocks - TIA

Applying Equation (4-10) and other design considerations, discussed in the Section 4-1-2 and after a few simulation iterations, the load impedance (R_f) of TIA is selected to be $18\text{ k}\Omega$ for an opamp with total input referred noise of -80 dBm in the bandwidth of 1 MHz . Selection of that resistance value is a trade-off between gain and noise. A capacitive load (C_f) of 225 fF is added in parallel to the resistive load. It results in a low pass filter with a bandwidth of 40 MHz which easily suppresses the leaked LO signals ($>2\text{ GHz}$), due to single balanced mixer and the out-of-band blockers ($>80\text{ MHz}$) from the received input signal. Though, out-of-channel blockers can be filtered by increasing the capacitance, C_f , it is not used here to completely avoid undesired phase delay to the wanted signal. However, this technique could be considered for future work after determining the maximum allowable phase delay for efficient PDC behaviour using system simulations.

Since the feedback impedance partially defines the input impedance of TIA (Equation (4-14)), it sets the specifications for opamp DC gain to ensure high linearity of switching transistors. Also, being the only source for flicker noise, TIA should be designed with low $1/f$ corner frequency. In this work, to speed up the design process, single opamp architecture is used for both TIA and low-pass filter. Hence, further discussion on opamp design and implementation will be covered in the Section 4-3.

In conclusion, a current driven passive mixer is designed based on the above discussions. Transconductor and TIA are optimized together to achieve the desired conversion gain and noise figure. Switching transistors are sized to minimize on-resistance and parasitic capacitance. Post-layout simulations are carried out to verify the performance and the results are covered in Chapter 5.

Table 4-3: Target specifications for Elliptic LPF.

Parameter	Target
Current consumption	< 350 μ A
Maximum gain	36 dB
Bandwidth	600 kHz
Stopband suppression	30/42 dB @ 2/3 MHz
Input-referred noise (BW < 1 MHz)	-76 dBm
Output compression point, (V_{pk-pk})	700 mV

4-2 Programmable LPF

According to the conclusions derived in Chapter 3, LPF should suppress adjacent and alternate channel interferers effectively to facilitate accurate phase-to-digital conversion. It also should provide gain to achieve the desired receiver sensitivity. To accommodate, 20 dB 2nd channel and 30 dB 3rd-channel interference in the PDC loop, a low pass 3rd order elliptical filter with cut-off frequency of 600 kHz and a notch at 2 MHz is chosen based on MATLAB simulations.

Further, cascade analysis revealed that a maximum gain of 36 dB and input referred noise of -76 dBm in 600 kHz bandwidth is required to achieve the desired receiver sensitivity of -90 dBm. The complete list of target specifications for the elliptic low pass filter (ELPF) is enumerated in Table 4-3.

4-2-1 Filter topology

The transfer function of the low pass 3rd order elliptical filter is given below. It has a pair of complex conjugate zeros and 3 poles: a pair of complex-conjugate poles and a negative pole at the real axis.

$$F(s) = k \frac{(s + z_1)(s + z_2)}{(s - p_1)(s - p_2)(s - p_3)} \quad (4-20)$$

where k is the gain factor, $z_{1,2} = \pm j1.26 \times 10^7$ rad, $p_{1,2} = (-1.11 \pm j3.88) \times 10^6$ rad and $p_3 = -2.47 \times 10^6$ rad.

Several circuit techniques (passive and active) are available in the literature to synthesize this network function [52][13][53]. Despite their power consumption, active filters are chosen for their ease of integration, as realization of complex poles and zeros in passive implementation require bulky inductors. Moreover, active filters provide tunable gain for varying input signal. It should be noted that transfer function in Equation(4-20) can be re-written as a product of two filter functions (Equation (4-21)): a complex biquad and a real 1st order low pass filter.

$$F(s) = \left[\frac{k_0 (s + \omega_z^2)}{s^2 + s \frac{\omega_o}{Q} + \omega_o^2} \right] \left[\frac{k_1}{s - \omega_p} \right] \quad (4-21)$$

where, $Q = 1.82$, is the quality factor and $\omega_o = 4.04 \times 10^6$ rad, is the natural frequency of the second-order function.

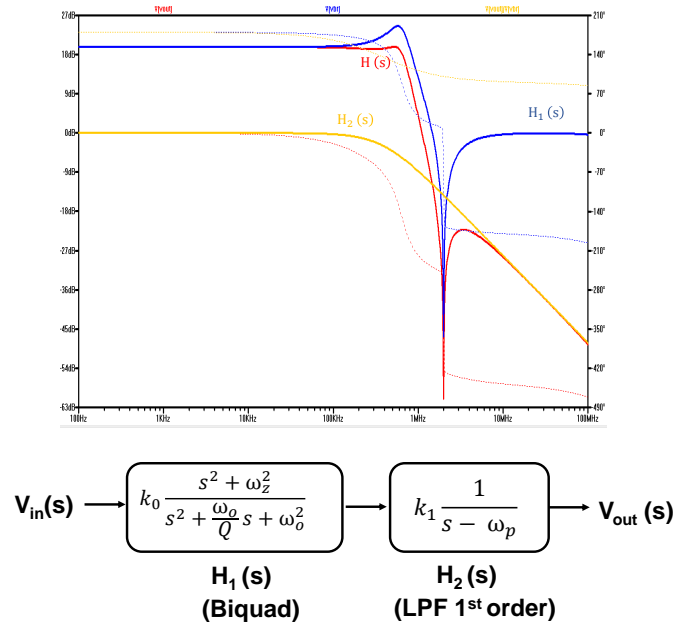


Figure 4-10: Elliptic LPF - cascade topology.

This implies that a simple cascade topology (Figure 4-10), comprising of a biquad and an active RC filter, can be used to implement elliptic filter. Owing to simple modular form, easy-to-design and troubleshoot, the cascade topology is adopted in this work. It will be shown here that how target power consumption and other specifications are achieved using this topology.

Of the choices available for biquad structure, Fleischer-Tow (FT) biquad [12] (Figure 4-11), a variant of Tow-Thomas biquad, is adopted for following reasons.

- It provides independent control over DC gain, cut-off frequency and Q-factor. This orthogonality is essential for independent gain and bandwidth tuning requirement in the receiver baseband.
- It has better sensitivity than Sallen-Key and multi-feedback structures [13]. In other words, less susceptible to component mismatches.

It should be mentioned here that a more robust leapfrog topology is available as an alternate for cascade topology. However, its advantages are limited by its high stop-band sensitivity and low Q of the required elliptic filter.

4-2-2 LPF implementation

FT biquad is one of the several integrator based biquad topologies realized using state-variable method.

The general integrator based realization of biquads is shown in Figure 4-12. The transfer function of this system can be given as,

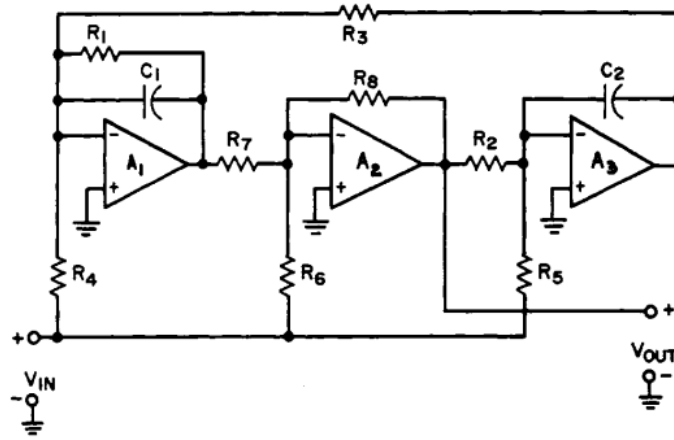


Figure 4-11: Fleischer-Tow biquad [12].

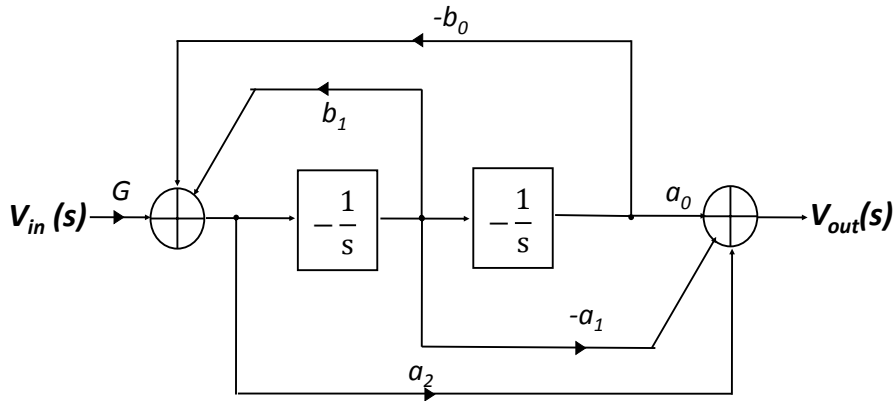


Figure 4-12: General integrator based biquad realization [13].

$$\frac{V_2}{V_1} = G \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0} \tag{4-22}$$

Considering a simple opamp-RC implementation, this realization requires a minimum of 4 opamps (2 each for integration and summation). Using state space analysis, several variations of above signal flow diagram have been proposed to minimize the number of opamps [52]. FT biquad is one such power-efficient realization as it requires only 3 opamps. Analysis of its single ended opamp RC implementation in Figure 4-11, would result in following transfer function.

$$\frac{V_{out}(s)}{V_{in}(s)} = - \frac{\frac{R_8}{R_5} s^2 + \frac{1}{R_1 C_1} \left[\frac{R_8}{R_5} - \frac{R_1 R_8}{R_4 R_7} \right] s + \frac{R_8}{R_3 R_6 R_7 C_1 C_2}}{s^2 + s \frac{1}{R_1 C_1} + \frac{R_8}{R_2 R_3 R_7 C_1 C_2}} \tag{4-23}$$

Besides opamps, Gm-cells can also be used to realize biquad. However, in this thesis work, opamp-RC biquad is preferred over gm-C biquad for their high linearity at low supply voltage and insensitivity to parasitic capacitances [54]. Compared to gm-cells, opamps are power-hungry and hence should be optimized to reduce the overall power consumption. At the top level, power reduction is obtained by further decreasing the opamp count in FT biquad.

The signal flow diagram of FT biquad is shown in Figure 4-13 to get better insight of its two integrator based structures. For implementation, FT biquad requires 3 opamps to perform integration and summation. As highlighted in the figure, opamp1 and opamp3 serve as summing integrator whereas opamp2 acts as summing amplifier in the inverting configuration. Since, differential opamps provide sign inversion by flipping the input signals, it is used to replicate the inversion operation of opamp2 in the desired differential implementation.

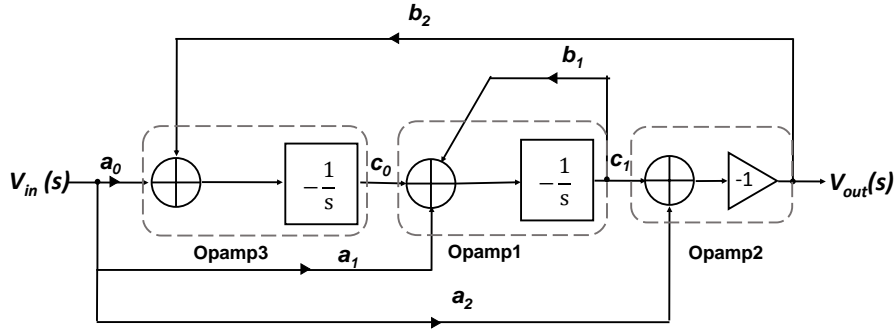


Figure 4-13: Fleischer-Tow biquad - signal flow diagram.

Summing operation of opamp2 can be replaced in two steps:

1. Modify the branch a_0 such that it compensates for the partial signal transfer gain $(-a_2b_2)$ achieved through branch a_2 , inverter and b_2 . This will push the summing node out of the feedback loop without affecting the overall transfer function.
2. Combine the pushed-out summing node with the second-stage LPF. This results in a feed-forward path from the input of elliptic LPF to the input of second-stage LPF.

The two alterations and the resulting elliptic LPF structure are illustrated in Figure 4-14. The circuit diagram of elliptic LPF (differential structure) encompassing modified biquad and LPF is depicted in Figure 4-15 and their transfer function is given in Equation(4-24). It can be mentioned that, with feed-forward path to the second stage, the elliptic LPF is no longer a pure cascade structure.

$$\frac{V_{out}(s)}{V_{in}(s)} = - \left[\frac{R_F}{R_X(1+sC_F R_F)} \right] \left[\frac{s^2 + \frac{1}{C_1} \left[\frac{1}{R_1} - \frac{1}{R_4} \right] s + \frac{1}{R_3 C_1 C_2} \left[\frac{1}{R_2} - \frac{1}{R_6} \right]}{s^2 + s \frac{1}{R_1 C_1} + \frac{1}{R_2 R_3 C_1 C_2}} \right] \quad (4-24)$$

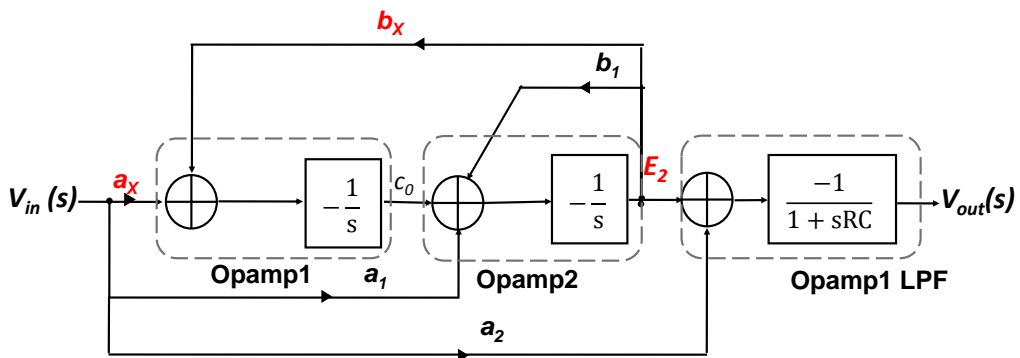


Figure 4-14: Elliptic LPF with Fleischer-Tow biquad - modified signal flow diagram.

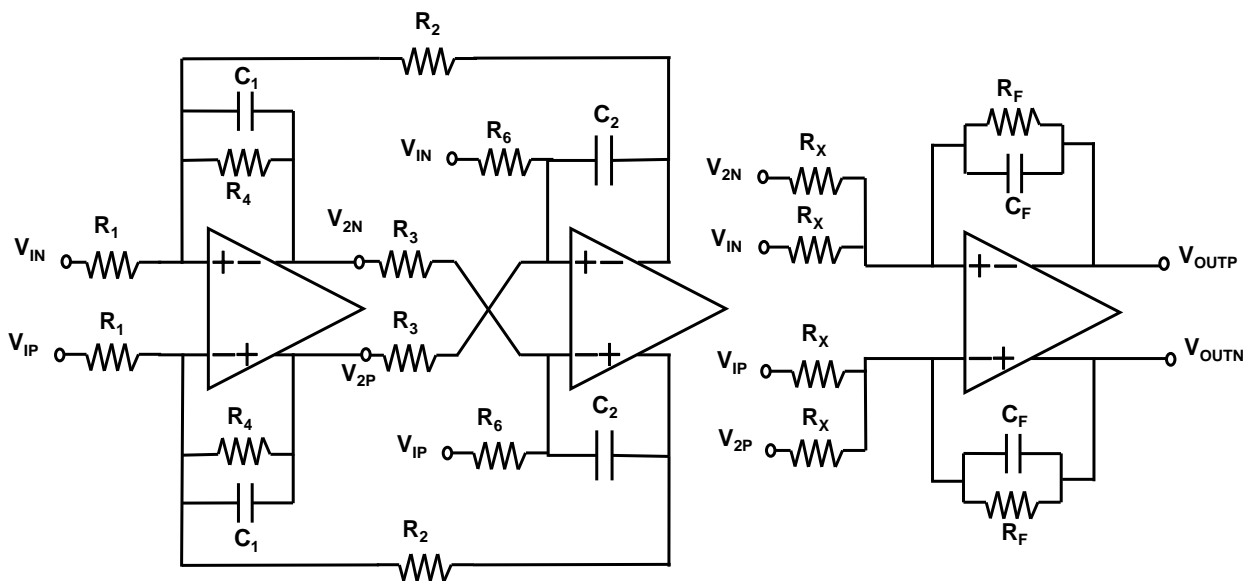


Figure 4-15: Elliptic LPF - implementation.

Comparing system and circuit transfer functions given in Equation(4-21) and Equation(4-24)

would result in following conclusions:

$$\begin{aligned}
 \text{natural frequency, } \omega_o &= \sqrt{\frac{1}{R_2 R_3 C_1 C_2}} \\
 \text{Q-factor, } Q &= \sqrt{\frac{R_1^2 C_1}{R_2 R_3 C_2}} \\
 \text{zero frequency term, } \omega_z &= \sqrt{\frac{1}{R_3 C_1 C_2} \left[\frac{1}{R_2} - \frac{1}{R_6} \right]} \\
 \text{LPF DC gain, } k &= -\frac{R_F}{R_X} \\
 \text{LPF corner frequency, } p_3 &= \frac{1}{R_F C_F}
 \end{aligned} \tag{4-25}$$

and more importantly, R_4 should be equal to R_1 to generate desired complex zeros in the biquad transfer function.

From above expressions, it is quite evident that bandwidth of biquad can be tuned by scaling C_1 and C_2 together while R_1 , R_2 , R_3 and Q-factor remain unchanged. Similarly, Q-factor and notch location (zero frequency) can be adjusted using R_1 and R_6 respectively. However, tuning zero frequency using R_6 varies the gain in biquad whereas scaling bandwidth using C_1 and C_2 moves the notch considerably. Marginal gain variation is not a major concern in this architecture. In contrast, these two features can be combined together to perform both coarse and fine zero-tuning.

With following considerations, actual resistor and capacitor values are obtained by equating similar terms in Equations (4-21) and (4-25)

- Since C_1 and C_2 have to scale together for bandwidth tuning, they are set to have same capacitance C . To simplify the design, the LPF capacitance C_F is also set to be C and Resistors R_2 and R_3 are set to be R .
- Presence of zeroes and poles in the biquad provides an inherent gain of 20 dB (ω_z^2/ω_o^2). Since the required elliptic LPF gain is 36 dB, the remaining 16 dB gain is obtained through the second LPF stage.
- It is understandable that input impedance of ELPF is a major contributor to the LPF noise along with opamps. From Chapter 3, the noise budget of LPF is -76 dBm. Assuming noise contribution of R_{in} and opamps are equal, R_{in} should contribute less than -79 dBm noise. The following relation can be used to calculate maximum input impedance:

$$10 \log \frac{4kT(2R_{in})BW}{50 \times 10^{-3}} < -79 \text{ dBm} \tag{4-26}$$

where, $BW = 600 \text{ kHz}$ is the LPF bandwidth, $T = 300 \text{ K}$ is the temperature, factor 2 is due to differential structure, conversion factor 50×10^{-3} is used to convert into 50Ω and dBm system. The maximum input impedance thus calculated is $38 \text{ k}\Omega$. Since R_{in} is a combination R_4 , R_6 and R_X , they need to be chosen accordingly.

For 600 kHz bandwidth of ELPF, C_1 and C_2 are chosen to be 2 pF. The derived values of other components are shown in Table 4-4.

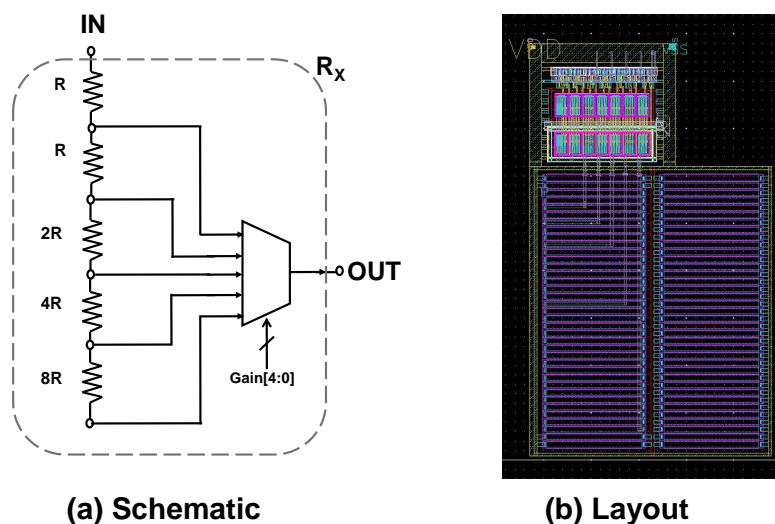
Table 4-4: RC component values of Elliptic LPF.

Components	Magnitude
C_1, C_2, C_F	2 pF
R_1, R_4	225 k Ω
R_2, R_3	124 k Ω
R_6	12.7 k Ω
R_X	25 - 400 k Ω
R_F	200 k Ω

4-2-3 Gain, bandwidth and zero tuning

As discussed in the previous section, biquad is designed to have a fixed gain of 20 dB. This inherent gain is due to the squared ratio of zero frequency to natural frequency (ω_z^2/ω_o^2). The second stage LPF is designed to generate an additional 18 dB gain through ratio of its feedback and input resistance (R_F/R_X). For simple and effective gain tuning of ELPF, the gain of second stage LPF can be adjusted using R_X as programmable resistor. R_F is not chosen here as varying it would change the LPF bandwidth.

For ease of implementation, the gain range and step are chosen to be 14–38 dB and 6 dB. The programmable resistor chain is built using binary-weighted resistors as shown in the Figure 4-16. These binary-weighted resistors are in-turn realized with a unit resistance of 25 k Ω . The desired gain is set by a control word stored in the serial-to-parallel interface (SPI) register slave on chip. Two of the programmable resistive chains are paired to form a differential resistor at the LPF input.

**Figure 4-16:** Gain tuning - schematic and layout.

Bandwidth of ELPF is the resultant of the biquad and LPF bandwidths. As mentioned earlier, bandwidth tuning is simplified by implementing C_1, C_2 and C_F as programmable

capacitors. They are built using Metal-Insulator-Metal capacitors and its schematic and layout of the programmable capacitor are shown in Figure 4-17. The capacitance can be tuned from 1.2 – 2.6 pF with a tuning step of 100 fF/steps. It provides $\pm 30\%$ margin to compensate process variations. This translates to a frequency range of 400 kHz to 900 kHz. The tuning is controlled by a 3-bit frequency tuning code.

Similar to bandwidth and gain tuning, zero-tuning is implemented in this circuit to compensate process variations. As proposed in previous section, zero-tuning is achieved in two steps: (i) coarse tuning using C_1 and C_2 – The programmable capacitors, implemented for bandwidth tuning, is re-used here; (ii) fine tuning using Resistor R_6 – To achieve this, R_6 is implemented as a programmable resistor with range $10.9\text{ k}\Omega$ – $14.5\text{ k}\Omega$, a margin of $\pm 15\%$ with respect to nominal resistance. The programmable resistor is built using unary elements with unit resistance of $600\ \Omega$. The range of coarse and fining tuning are 1.5 – 3.0 MHz and 0 – 250 kHz respectively.

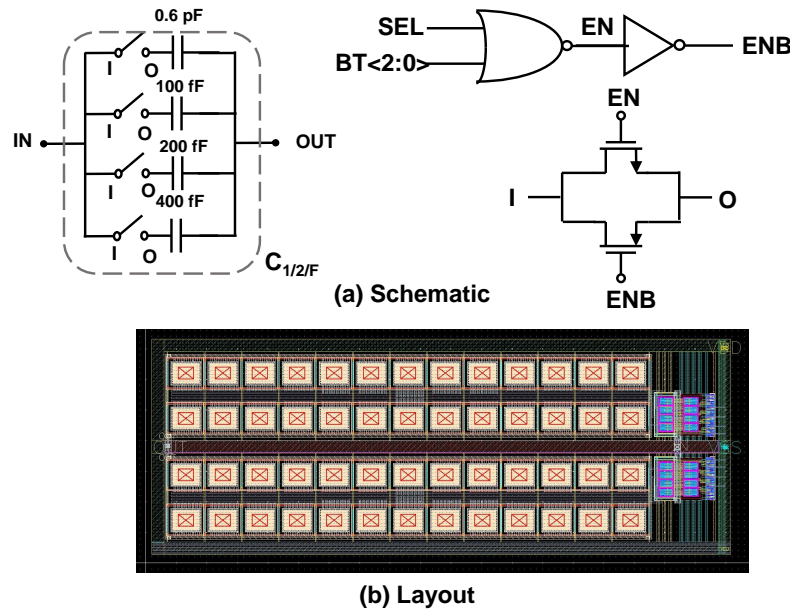


Figure 4-17: Bandwidth tuning - schematic and layout.

The post-layout simulation results for ELPF gain, bandwidth-tuning and zero-tuning are covered in Chapter 5. Figure 4-18 shows the top-level layout of the LPF with 3 opamps, gain, bandwidth and zero-tuning blocks.

4-3 Operational amplifier

In this receiver chain, operational amplifiers (opamps) are employed at two different blocks: Mixer-TIA and ELPF. The requirements of mixer-TIA and ELPF are evaluated together in deriving the specifications for the single robust opamp, usable in both TIA and ELPF. Designing exclusive opamps for TIA and ELPF costs design time for marginal improvement in the performance.

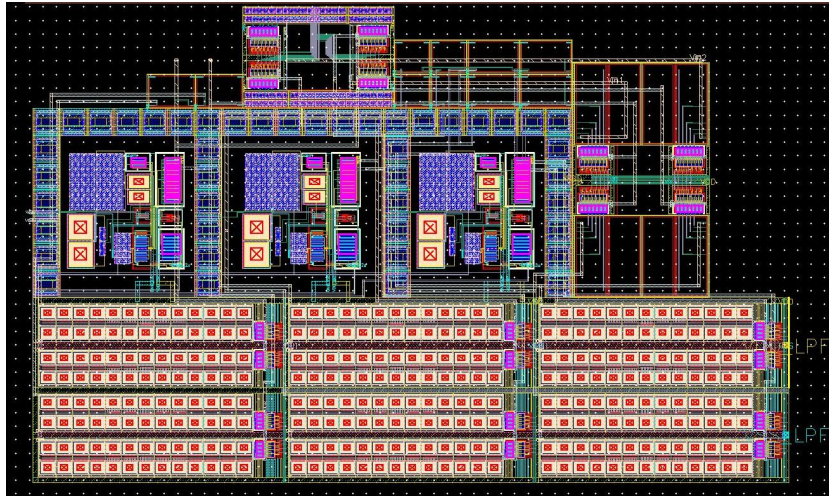


Figure 4-18: Elliptic filter - layout.

TIA opamp

For TIA opamp, the maximum output current to be delivered can be calculated using the target mixer OIP3 and load impedance at its output. Target mixer OIP3 of 0 dBm (equivalent to 310 mV_{pk}) and minimum load impedance of $10 \text{ k}\Omega$ (TIA output impedance parallel to LPF input impedance) define the maximum output current to be $16 \mu\text{A}$. From Section (4-1-5), the input referred noise of opamp noise should be $< -80 \text{ dBm}$ so that input referred noise of mixer is $< -89 \text{ dBm}$.

Further, TIA requires opamp with high DC gain and wide bandwidth for minimum input impedance. Low input impedance is necessary to maintain linearity of the passive mixer. The input impedance of TIA, given in Equation (4-14) confirms the above exposition.

Elliptic LPF opamp

Similarly, for ELPF opamps, maximum output current is determined by the desired output swing and load impedance. Considering rail-to-rail output swing with minimum load impedance of $\sim 20 \text{ k}\Omega$, opamp has to supply a maximum load current of $\sim 22 \mu\text{A}$. Since, the target input referred noise of the ELPF (-76 dBm) is equally split between resistors and opamp, the input referred noise of opamp should be less than -79 dBm .

Moreover, maximum DC gain for single section of ELPF is 20 dB. This can be translated to a DC gain constraint of more than 40 dB for the opamp. It should be noted that biquad architectures are less sensitive to loop-gain. Hence only 20 dB margin is considered for opamp DC gain with the intent to minimize power. ELPF operates in two bandwidth modes: 600 kHz (*Bluetooth Low Energy* (BLE)) and 1.2 MHz (IEEE 802.15.4). So the maximum GBW in the ELPF should be greater than the required 12 MHz. Usually, 10x the required GBW (120 MHz) is preferred for open loop opamp. However, limited by power consumption, the target here is set to be $> 50 \text{ MHz}$.

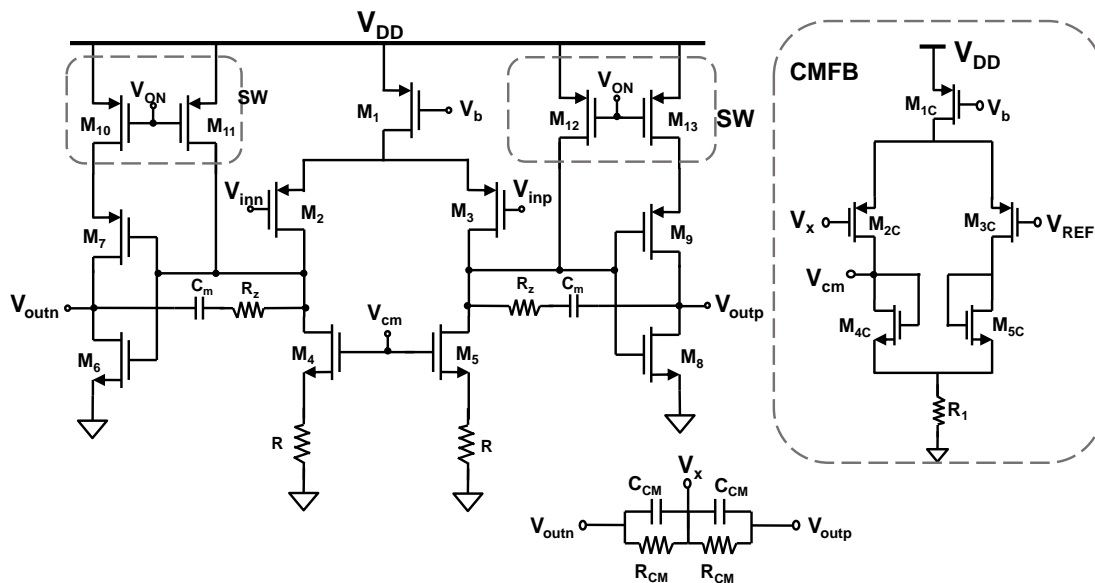
From Chapter 3, the targeted current consumption for mixer and ELPF is $300\text{--}350 \mu\text{A}$ for 0.85 V operation. Since mixer g_m stage consumes $\sim 100 \mu\text{A}$, the remaining $200 \mu\text{A}$ is split

Table 4-5: Target specifications of opamp ($V_{DD}=850$ mV)

Parameter	Target
Current consumption	$<50 \mu\text{A}$
Noise (1 kHz – 1 MHz)	<-76 dBm
Unity gain Bandwidth	>50 MHz
Open loop gain	>40 dB
Phase margin	$>60^\circ$

between 4 opamps (1 TIA + 3 ELPF). The target opamp specifications, evaluated until now, are summarized in Table 4-5.

To design high gain opamp with low power in deep sub-micron process, a two-stage architecture, shown in Figure 4-19, is adopted from earlier works [4][3]. The architecture is optimized to operate at 0.85 V and simultaneously meet targeted specifications. A simple differential PMOS amplifier with NMOS current-source load is used as input first stage in this architecture. Push-pull output stage is employed to achieve large output dynamic range with low quiescent current. A Miller capacitance, C_m with nulling resistor, R_z is added between the input and output node of the second stage to improve the stability of the opamp.

**Figure 4-19:** Operational amplifier with common-mode feedback biasing.

Mismatch in p-type and n-type current sources along with high output impedance affects the output common-mode level. Hence, an active continuous-time common-mode feedback (CMFB) circuit is added to the opamp. It measures output common mode voltage using resistor divider and the error amplifier output is applied to the first-stage load. CMFB resistor with parasitic load at the input of the error amplifier adds phase-lag to the common-mode signal and detracts the stability of CMFB loop. So, a capacitive divider is added

across the resistive divider to introduce phase lead and ensure stability. A phase margin $>50^\circ$ is achieved for CMFB loop after post-layout.

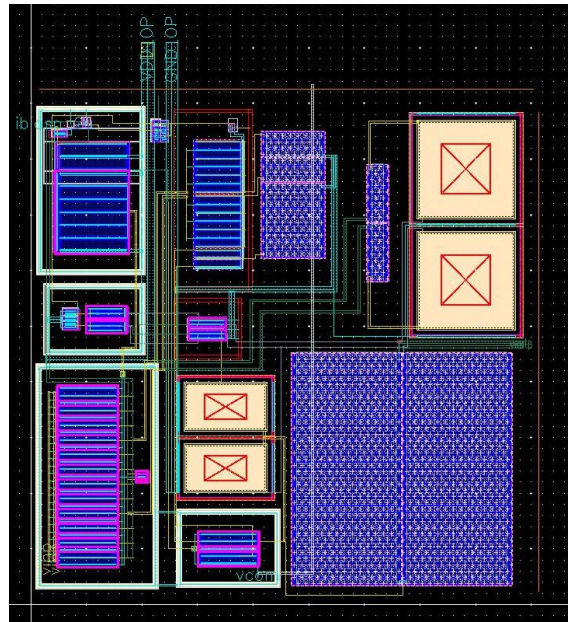


Figure 4-20: Operational amplifier - layout.

Transistors in the opamp are optimized for high gain and wide bandwidth while maintaining stability. As indicated, output stage is optimized for output swing and input stage for gain and noise. Since opamps are the main source of flicker noise, additional measures like resistive degeneration at source terminals of M4 and M5 are employed. Switches (M10 – M15) are added to turn on/off the opamp. This reduces leakage current during sleeping mode and also improves the start-up behaviour of the opamp.

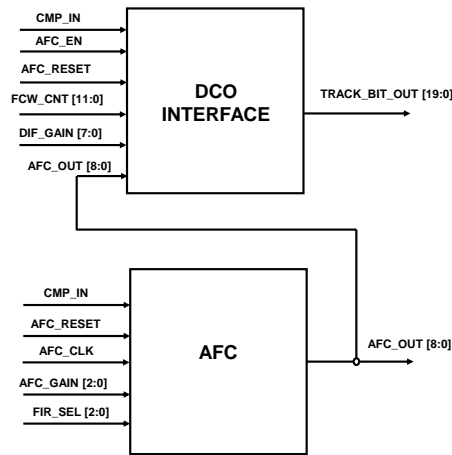
The circuit is designed and optimized for 0.85 V supply voltage. The common mode voltage is set at 0.38 V ($0.4 \cdot V_{DD}$). After sizing and post-layout optimization, the opamp is simulated stand-alone with 20 k Ω resistance in parallel with 2 pF capacitance load. The open loop gain at 500 kHz is 39.92 dB and the phase margin is 59° . The input referred noise, integrated from 1 kHz to 1 MHz, is less than -79 dBm (design target). The results of the small-signal and large-signal simulations are summarized in Table 4-6. The relevant graphs from simulation are provided in appendix A.

4-4 AFC and digital interface

The digital logic required for processing the comparator output to generate appropriate frequency control word (FCW) is described here. Verilog HDL is chosen to synthesize and implement the digital logic and it is designed to operate at a clock frequency of 32 MHz. Separate clock generation block is implemented at the top-level to generate desired clock signals from an external master clock for digital logic, comparator and offset DAC. A top level block diagram of the digital logic is shown in Figure 4-21.

Table 4-6: Opamp post-layout simulation results ($V_{DD}=850$ mV) - summary.

Specification	Result
Current consumption	25 - 35 μ A
Noise (1 kHz – 1 MHz)	-85 dBm
Unity gain Bandwidth	42 MHz
Open loop gain	49/38 dB @ DC/600 kHz
Phase margin	59 $^{\circ}$
Output swing (V_{pk})	700 mV
Input 1 dB compression point	3.5 mV

**Figure 4-21:** Digital logic - top level block diagram.

The digital logic consists of an interface to DCO and an AFC block. DCO interface block receives inputs from: (i) the comparator output, (ii) the AFC output and (iii) a frequency tuning word from SPI control register. It processes these inputs to generate an instantaneous FCW for tracking bank of DCO. The tracking bank of DCO covers >15 MHz frequency range and it is more than the desired range (2MHz) for receiver operation. Hence, the interface is designed to adjust only tracking bank FCW. The FCW of PVT and acquisition banks of DCO are set by SPI control register.

The AFC block estimates the frequency error due to carrier frequency offset and DCO phase noise from comparator output. The estimated error output is fed into DCO through DCO interface block for automatic cancellation in phase/frequency domain. Programmable filter and $\Sigma\Delta$ modulator are employed in the AFC block for more accurate estimation of frequency error. The implementation details of both these blocks are described in the following section.

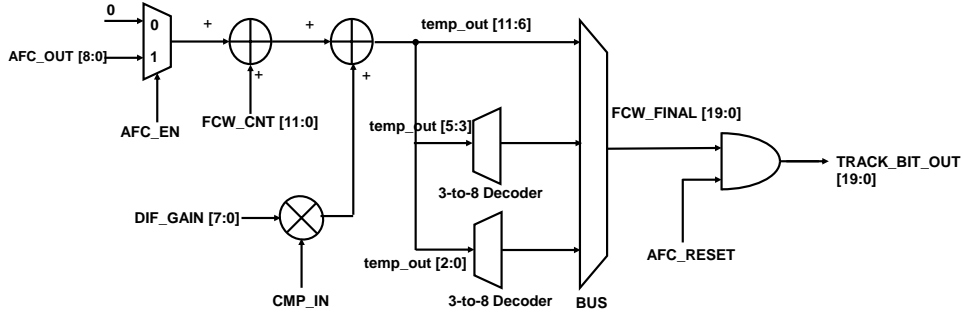


Figure 4-22: Digital logic - DCO interface.

4-4-1 DCO interface

Figure 4-22 shows the implementation of the DCO interface block. As mentioned above, the inputs to this block are 1-bit comparator output that represents the instantaneous demodulated frequency, a 9-bit AFC output that carries the frequency error estimation and a 12-bit base FCW that sets the initial DCO center frequency.

The desired 12-bit FCW for tracking bank is generated based on the equation given below.

$$FCW_{\text{track}} = [DIF_GAIN \times CMP_IN] + AFC_OUT + FCW_CNT \quad (4-27)$$

It should be noted that tracking bank of DCO, employed in this design, has a resolution of 4 kHz. Hence, for typical BLE operation, the comparator gain (DIF_GAIN) is programmed to 64. It enables DCO to switch its frequency between $f_c + 256$ kHz and $f_c - 256$ kHz, based on the comparator output. With 8 bits, DIF_GAIN [7:0] can cover up to ± 512 kHz (128×4). The center frequency, f_c is set by base word FCW_{CNT} and it is dynamically adjusted based on the AFC output. The 9-bit AFC output provides a frequency tuning range of ± 1024 kHz. In other words, a frequency error within ± 1024 kHz can be corrected using this digital circuitry.

Finally, two 3-to-7 bit decoders is employed to convert 6 LSBs of FCW_{track} into 14 unary LSBs of TRACK_BIT_OUT[13:0]. 14 unary LSBs along with 6 unchanged binary MSBs of FCW_{track} forms the 20-bit TRACK_BIT_OUT [19:0] that is connected to the tracking bank of the DCO.

4-4-2 AFC

As described in Chapter 3, the DCO phase noise and carrier frequency offset are present in the low-frequency spectrum of comparator output. An accumulator is used at the comparator

output to extract these low-frequency components. The accumulator provides 20 dB attenuation to components at 500 kHz, compared to those at 50 kHz. Numerical simulations in Chapter 3 confirmed that it is enough to achieve desired operation.

However, as frequency decreases, gain of accumulator increases exponentially. To compensate very high gain of accumulator at low frequencies, a gain factor is applied to the accumulator output. The gain factor, α , is chosen to be a negative power of 2 to minimize the hardware complexity. In this way, a multiplication can be replaced by a simple right shift operation. The number of right shifts can be programmed from 0 to 7 using the value of 'afc_gain' in SPI registry.

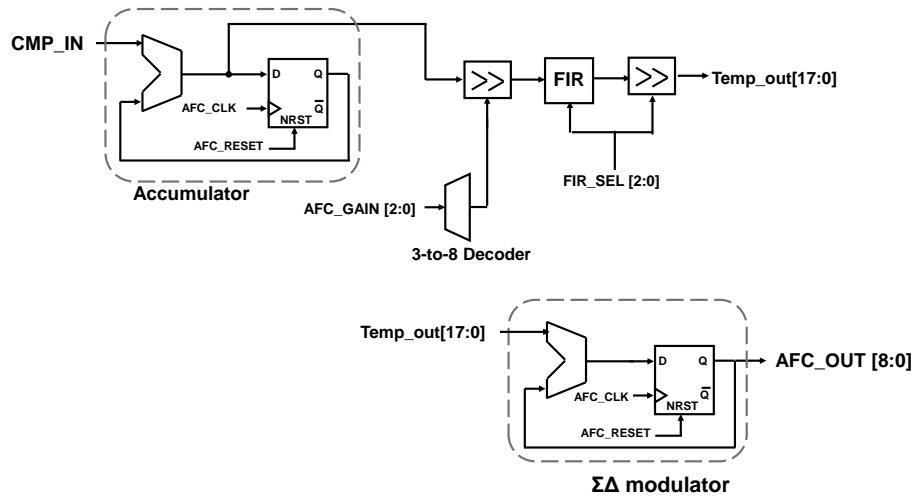


Figure 4-23: Digital logic - Automatic frequency noise cancellation block.

An additional finite impulse response (FIR) filter is used to further suppress the out-of-band frequency noise. The sinc filters with 3 different taps ($N = 32, 64$ and 128) are employed as FIR filter. Using Equation(4-28), the bandwidth of sinc filters can be calculated. For $N = 32, 64$ and 128 , it is 150 kHz, 301 kHz and 600 kHz respectively. Since the highest FIR tap is 128 (2^7), the size of FIR output is set to be 18 bits ($11+7$). In case of $N = 32$ and 64 , MSBs in the FIR output are not used in full operation. Hence, additional gain normalization is applied to the FIR output to avoid ambiguous results.

$$\text{N-tap sinc filter, } H_N(\omega) = \frac{1}{N} \left[\frac{1 - \exp(j\omega N)}{1 - \exp(j\omega)} \right] \quad (4-28)$$

Number of taps in sinc filter can be chosen using the value of 'FIR_SEL' in the SPI. Finally, in this AFC implementation, the power consumption of FIR filter is traded for its stability. In future work, FIR filters will be replaced by efficient Infinite impulse response filters while maintaining stability.

Finally, the 18-bit FIR output is fed into a first order $\Sigma\Delta$ modulator to produce 9-bit quantized AFC output. The $\Sigma\Delta$ modulator reduces the quantization noise and thereby improves the

AFC resolution. The output is connected to the input of the block 'DCO interface'. Figure 4-23 shows the block diagram of the AFC.

Cadence SOC Encounter is used to synthesize and implement this RTL level digital logic and the performance is shown in Chapter 5.

Layout and simulation results

In this chapter, post-layout simulation results of the circuit blocks, analysed in Chapter 4, are presented first to demonstrate their performance. Then, reused blocks – low noise amplifier (LNA), digitally controlled oscillator (DCO) and comparator – are discussed. Later, layout and simulation results of the full chip are presented. Finally, the debugging results of the first test chip are discussed together with the design modifications added to the second test chip.

5-1 Post-layout simulations

5-1-1 Mixer

The parasitics from the layout (described in Chapter 4) are extracted using Cadence-QRC extractor and the post-layout simulations are performed to estimate the conversion gain, noise, 1 dB compression point and current consumption. The input and loading conditions are properly set using LNA and low pass filter (LPF). The effect of bond wire connections from the supply to the chip are modelled using IMEC in-house bondwire model.

Using the schematic given in Figure 4-2 and Equation(4-2), the conversion gain of the mixer is estimated. Figure 5-1 shows that the mixer provides a conversion gain of ~ 25 dB. Figure 5-2 highlights that a noise factor of $5.5 \text{ nV}/\sqrt{\text{Hz}}$ is achieved at a frequency close to ~ 500 kHz. Using the equation given below, the total input referred noise, integrated over 1 MHz bandwidth, is calculated to be -92 dBm.

$$dBm = 10 \log \left(\frac{V_{n,rms,BW}^2}{50 \times 10^{-3}} \right) \quad (5-1)$$

where, $V_{n,rms,BW}^2$ is the total input referred noise in the bandwidth, BW and 50×10^{-3} is the conversion factor for 50Ω and 1 mW system. Further, in terms of large signal performance, the mixer achieves a 1 dB compression point of ~ -24 dBm at the mixer input (Figure 5-3). Using the conversion gain obtained earlier, 1 dB compression point at the mixer output can

be calculated. A conversion gain of 25 dB fairly indicates that it meets the design target, 0 dBm. All these results are obtained using periodic steady-state analysis.

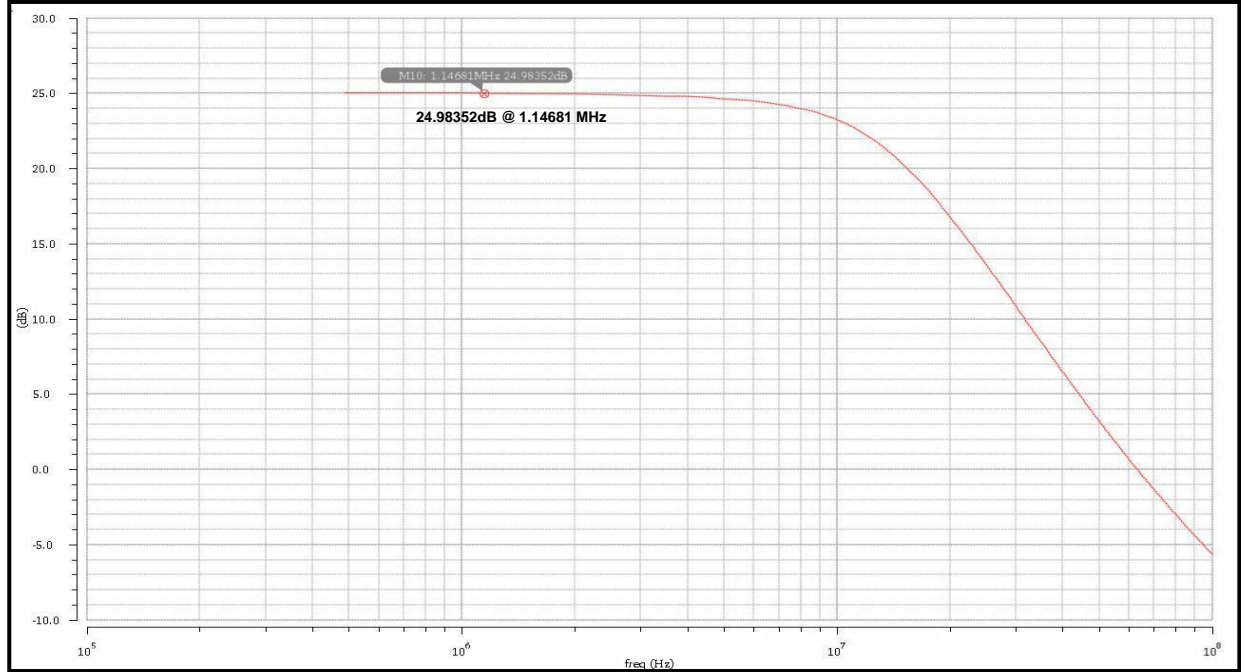


Figure 5-1: Simulation results of the mixer - conversion gain.

A transient simulation, in which the mixer is turned on and off, is performed to analyse the settling behaviour and the overall stability of the mixer. The waveforms of input at V_{RF} and resultant transimpedance amplifier (TIA) output, ($V_{out+} - V_{out-}$) are shown in Figure 5-4 and it indicates that mixer settles in $\sim 1 \mu\text{s}$, after it is turned on without causing any stability issues. Due to single-balanced architecture, mixer experiences local oscillator (LO) leakage and is usually filtered by the load impedance of the TIA. To substantiate this filtering performance, a transient simulation is performed with RF input tied to the ground. The FFT of the resulting TIA output is shown in Figure 5-5. It reports a LO leakage power of -56 dBm / -69 dB at fundamental LO frequency.

The transconductor and TIA in the mixer consume $101 \mu\text{A}$ and $32 \mu\text{A}$ of current respectively. In total, mixer consumes $133 \mu\text{A}$ of current at a supply voltage of 0.85 V, translating to a power consumption of $113 \mu\text{W}$.

5-1-2 Elliptic lowpass filter

In Chapter 4, elliptic lowpass filter is designed to provide a maximum voltage gain of 38 dB in the bandwidth of 600 kHz together with a notch at 2 MHz. Post-layout filter gain, the ratio of ($V_{OUTP} - V_{OUTN}$) to ($V_{INP} - V_{INN}$) in the schematic given in Figure 4-15, confirms that the desired gain and notch behaviour is achieved (Figure 5-6). Next, the programmable resistor, R_X is swept to evaluate the gain-tuning characteristics of the filter¹. Figure 5-7 shows that

¹In this section, the term '*filter*' will also be used to refer elliptic LPF.

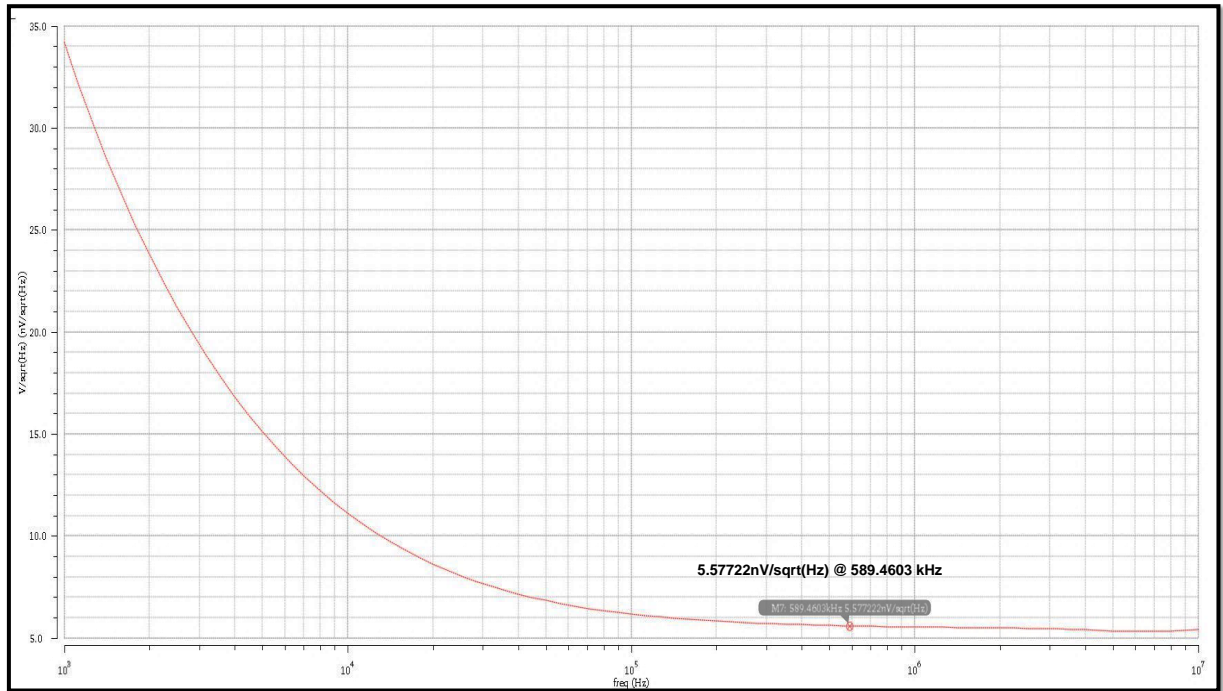


Figure 5-2: Simulation results of the mixer - noise factor.



Figure 5-3: Simulation results of the mixer - input referred 1 dB compression point.

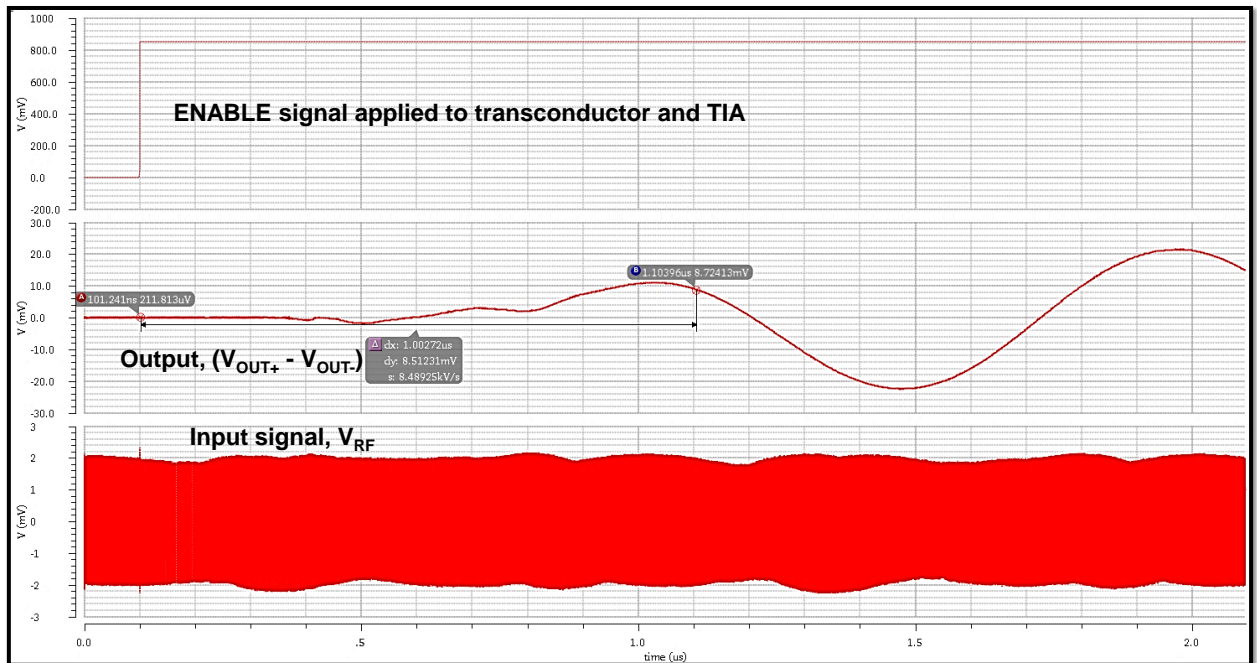


Figure 5-4: Simulation results of the mixer - start-up behaviour.

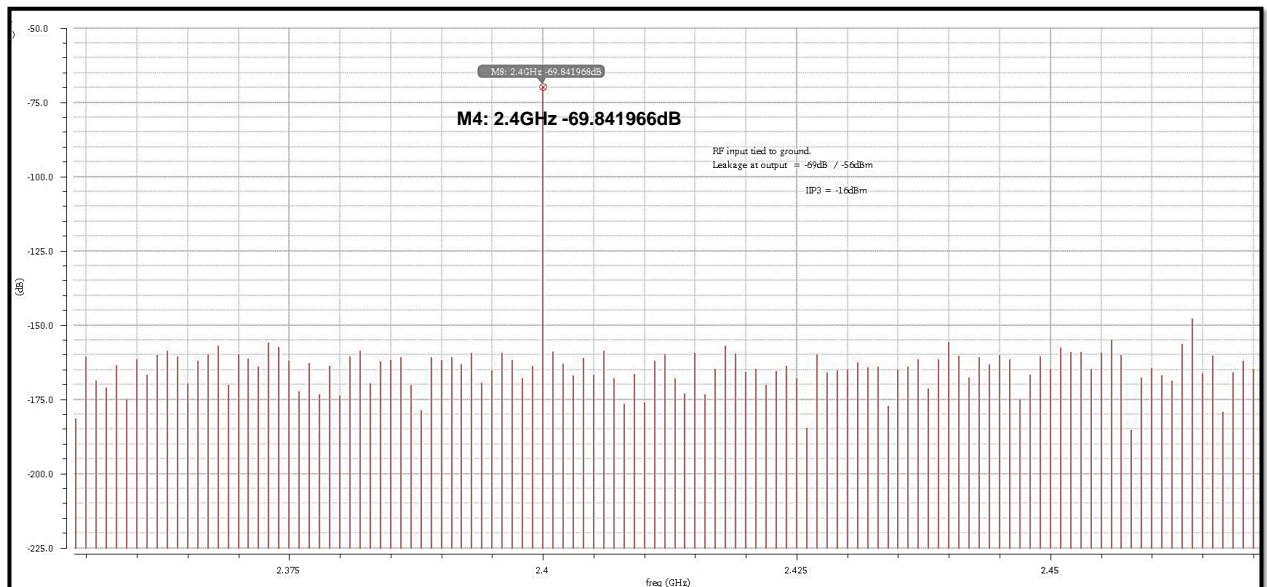


Figure 5-5: Simulation results of the mixer - LO leakage at mixer output.

the gain of the filter can be programmed from 13 dB to ~ 37 dB in steps of 6 dB. It should be noted that the filter is loaded with comparator and D2S buffer to account for actual loading conditions.

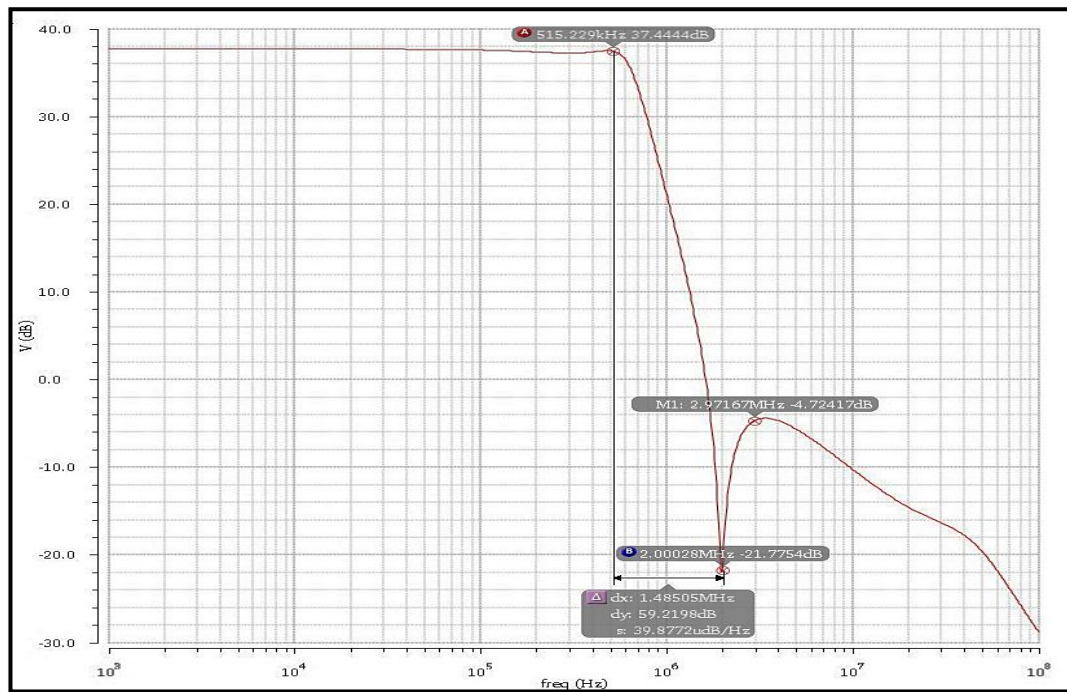


Figure 5-6: Simulation results of the elliptic filter - AC gain.

Similar to gain tuning, bandwidth tuning behaviour is also verified. As shown in Figure 5-8, the programmable capacitors provide a frequency tuning range of 420 kHz - 910 kHz. Besides, bandwidth tuning, these capacitors also facilitate coarse zero-tuning (4-2-3). Zooming into the region of 2 MHz shows that coarse tuning can cover a range of 1.5 MHz - 3.1 MHz (Figure 5-9). For fine zero tuning, R_6 is varied and the resulting behaviour is plotted in the Figure 5-10.

Further, the noise performance of elliptic LPF is evaluated by calculating the total input referred noise in the bandwidth of 1 MHz for maximum gain. The equivalent noise in dBm is calculated using Equation (5-1). The result, shown in Figure 5-11, reports it to be -77.5 dBm for maximum gain. Large-signal characteristics of the filter are analysed using transient analysis. To predict the 1 dB compression point, filter gain is calculated from the FFT plots of its input and output signal for different input amplitudes. The results are plotted and curve-fitted as shown in Figure 5-12. It indicates that, at 0.85 V supply voltage, filter can handle up to 11 mV of input swing (V_{pk}).

Similar to mixer, the stability of the filter is also analysed by instantly turning it off and turning it on during transient simulation. Figure 5-13 shows that it takes $\sim 1.1 \mu s$ for the elliptic LPF to start up and settle. Absence of sustained ringing in the waveform indicates the stability of the filter. Finally, an input signal, composed of tones at 500 kHz and 2 MHz, each with a magnitude 1 mV is applied to the filter in the transient analysis. The FFT of the

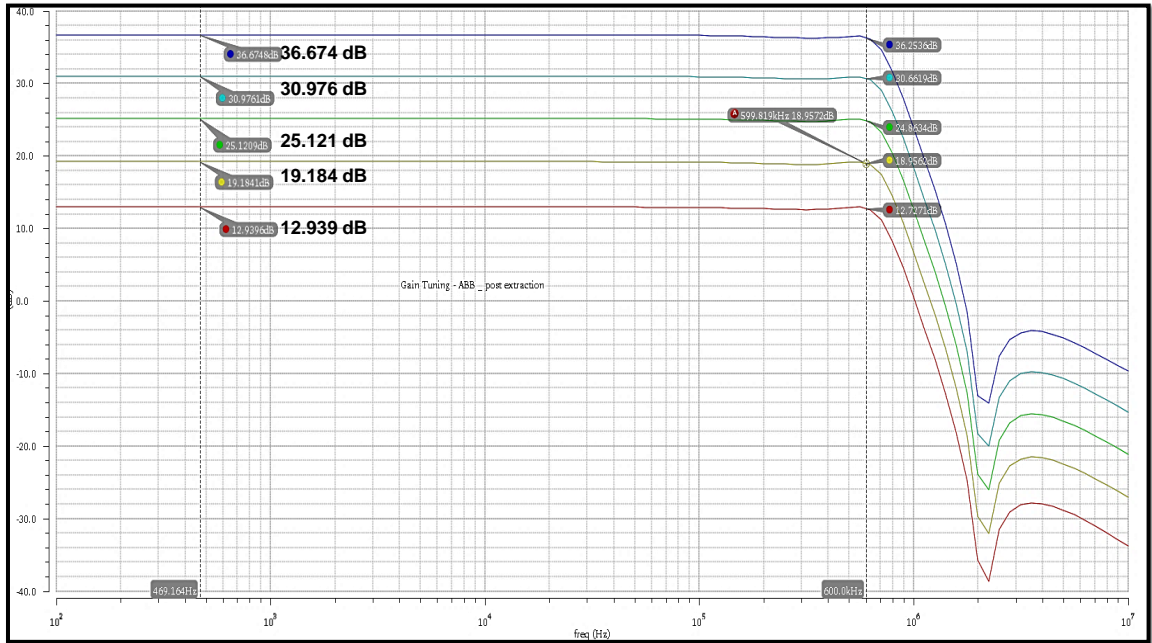


Figure 5-7: Simulation results of the elliptic filter - gain tuning.

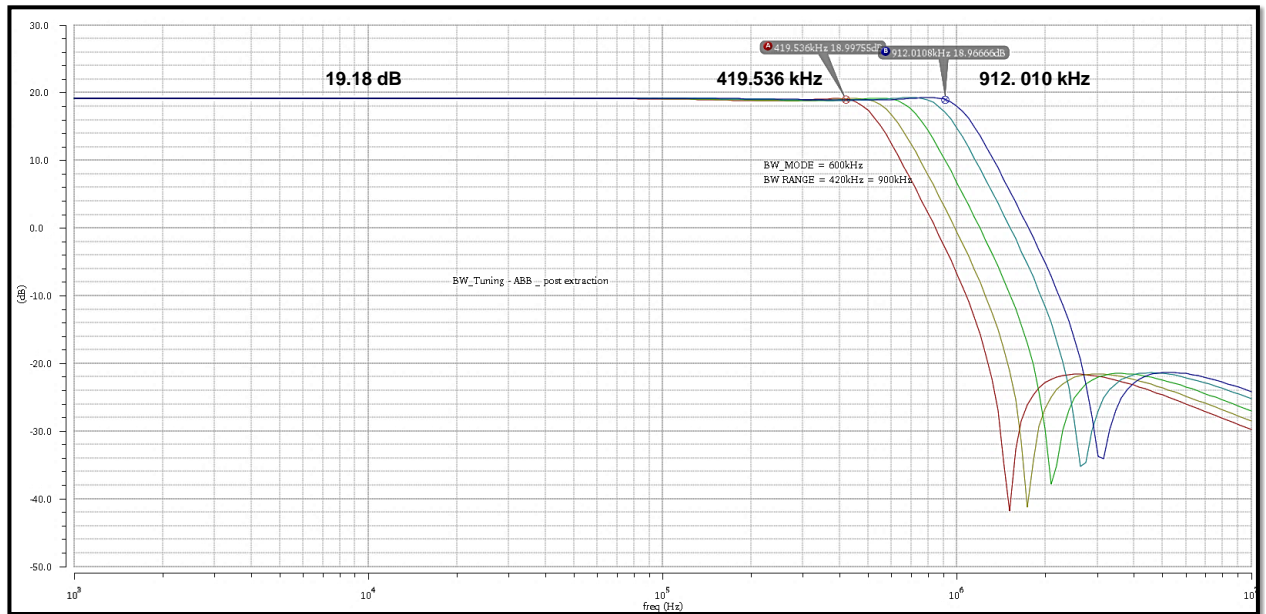


Figure 5-8: Simulation results of the elliptic filter - bandwidth tuning.

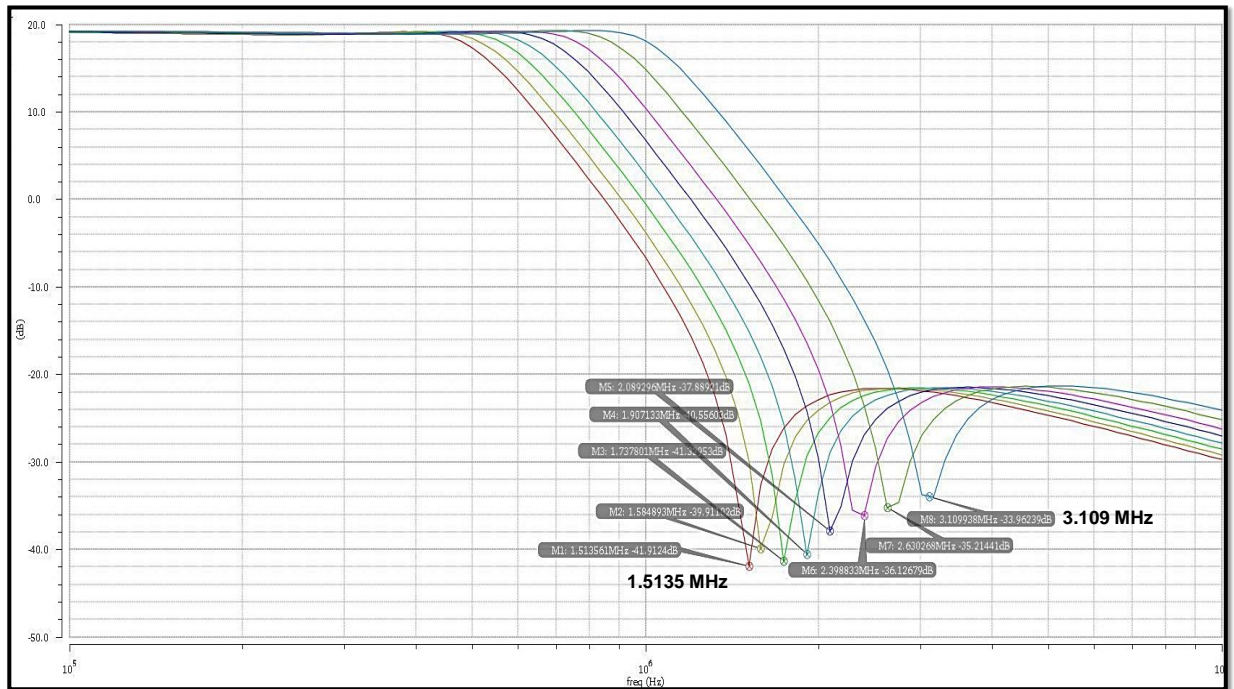


Figure 5-9: Simulation results of the elliptic filter - coarse zero tuning.

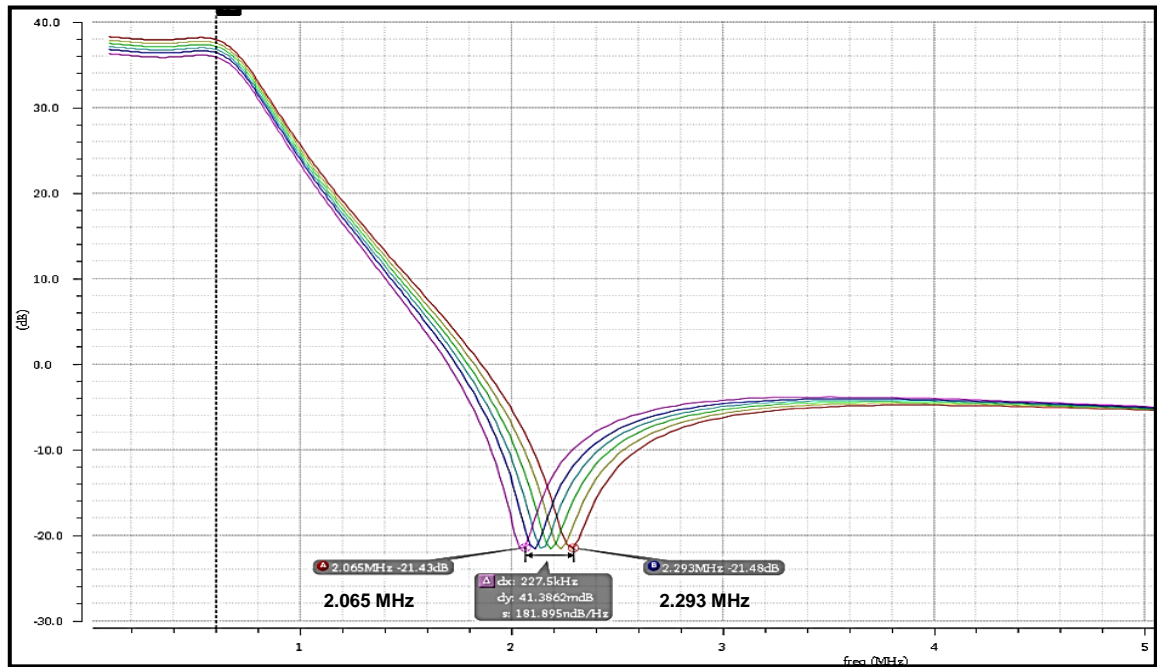


Figure 5-10: Simulation results of the elliptic filter - fine zero tuning.

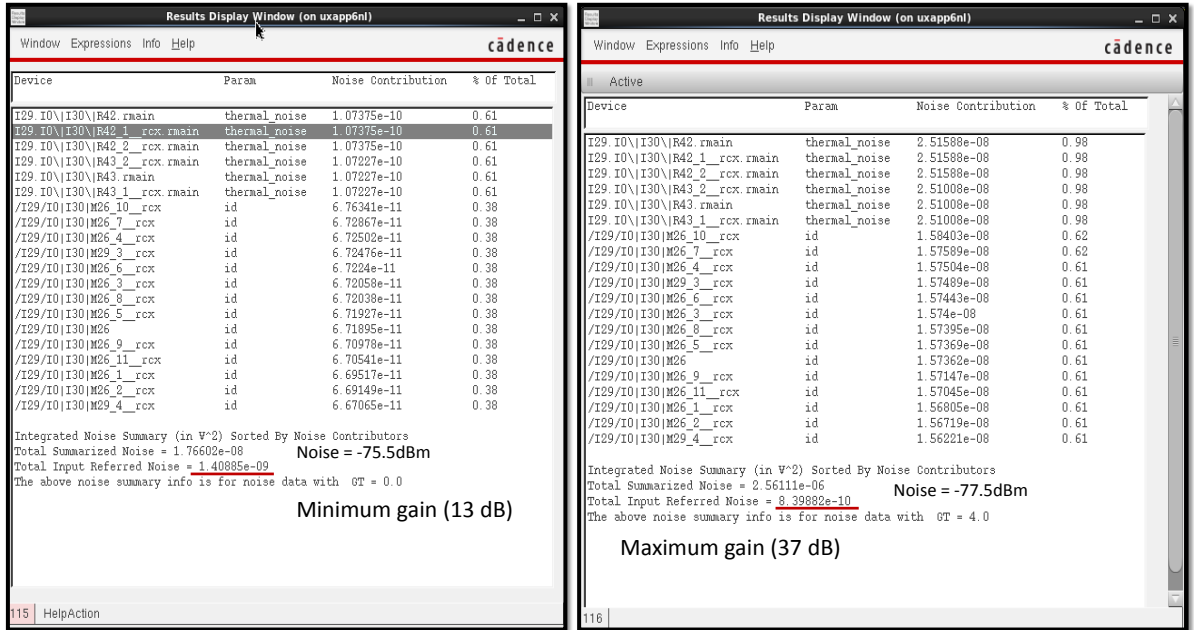


Figure 5-11: Simulation results of the elliptic filter - input referred noise.

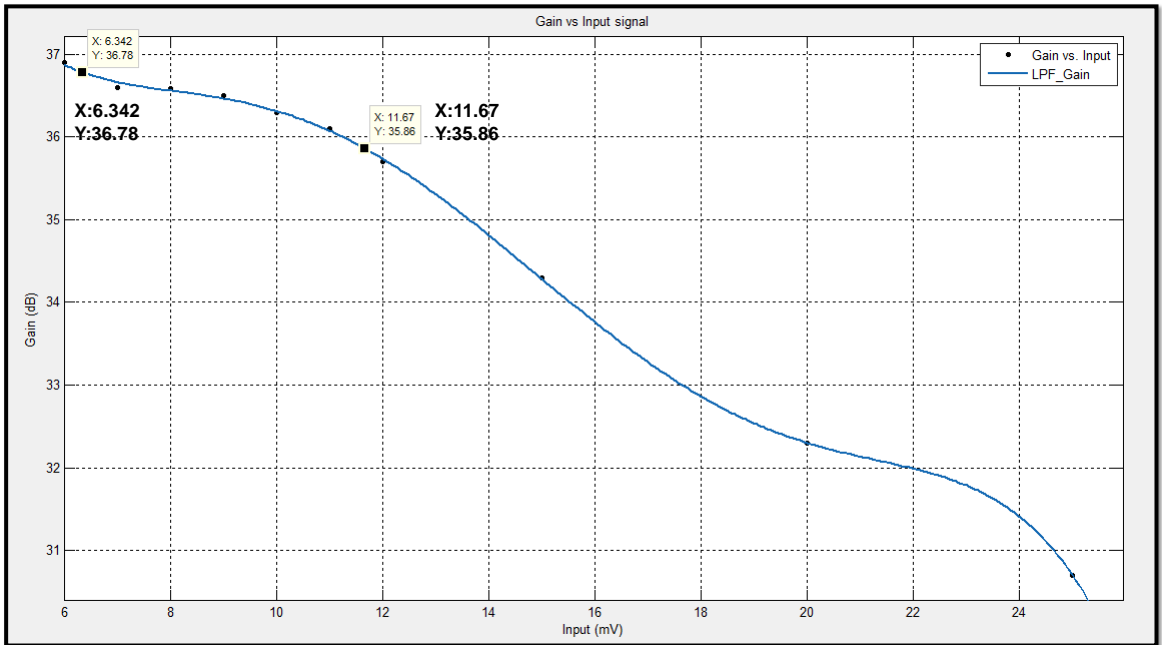


Figure 5-12: Simulation results of the elliptic filter - input referred 1 dB compression.

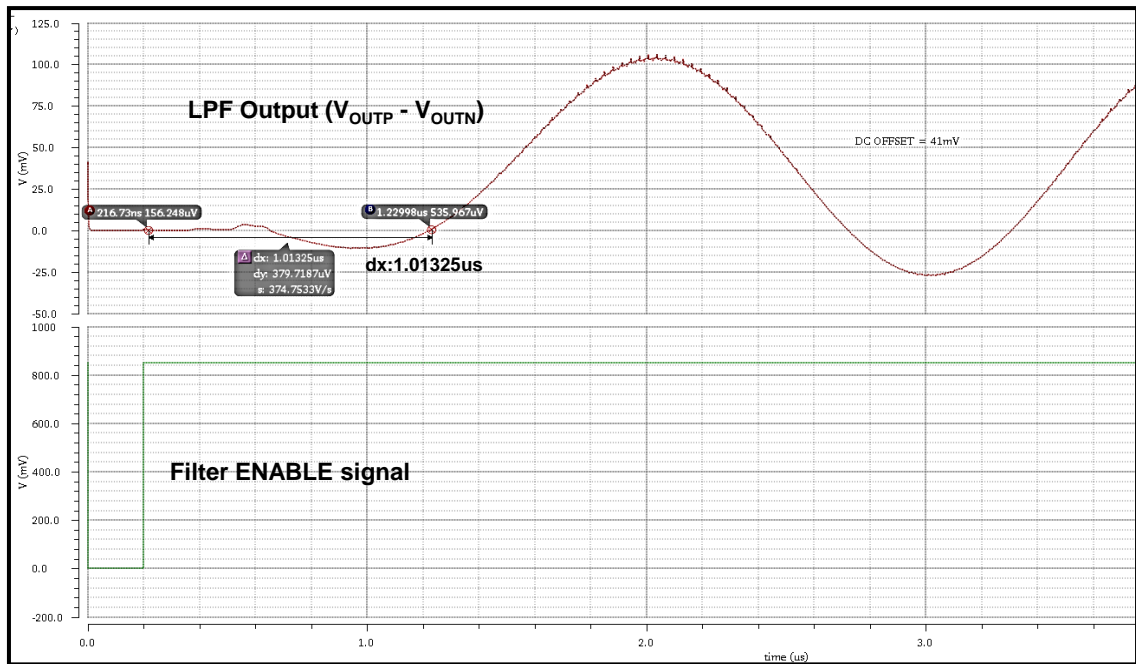


Figure 5-13: Simulation results of the elliptic filter - start-up behaviour (transient analysis).

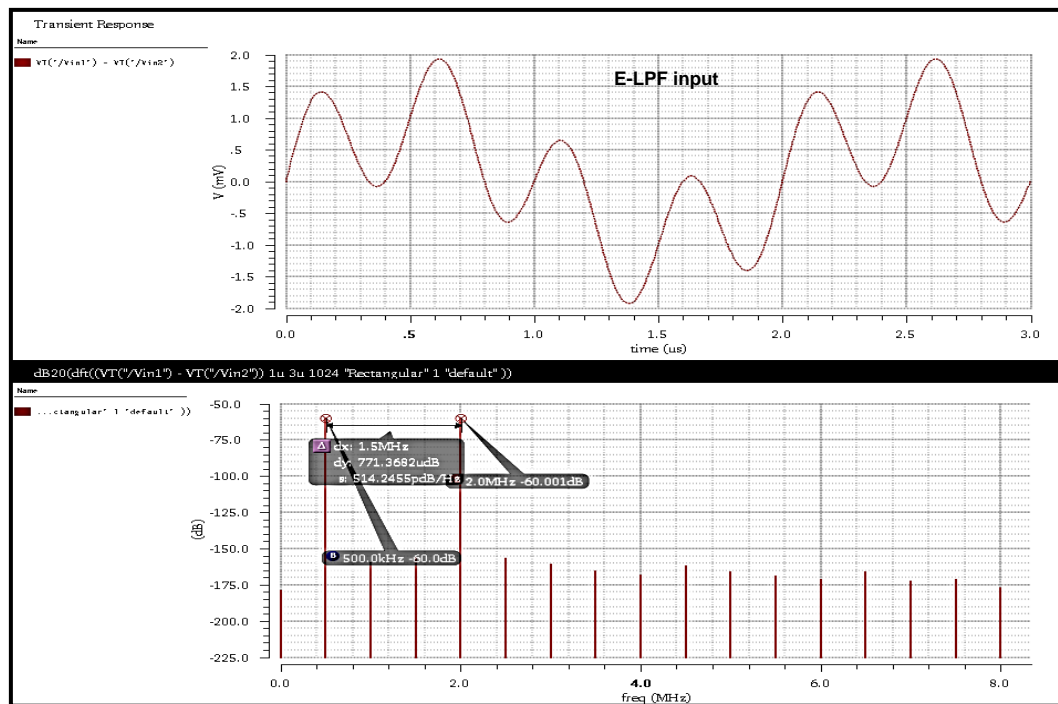


Figure 5-14: Simulation results of the elliptic filter - filter input (transient analysis).

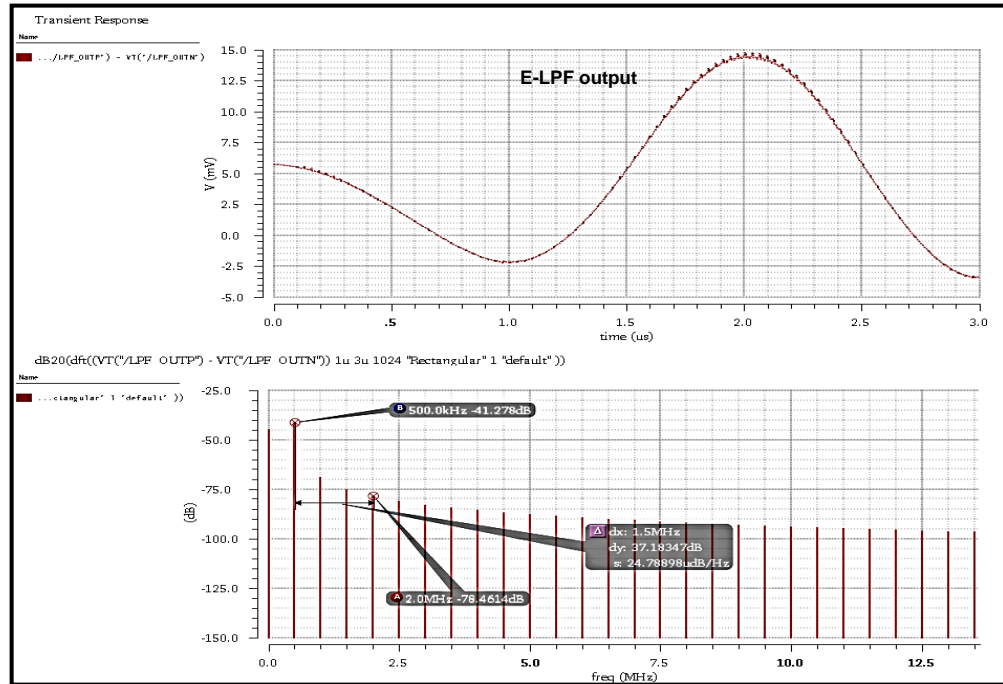


Figure 5-15: Simulation results of the elliptic filter - filter output (transient analysis).

output signal is plotted to estimate the attenuation at notch. Figure 5-14 and Figure 5-15 show that tone at 500 kHz is amplified by 19 dB, whereas tone at 2 MHz is attenuated by 19 dB. It translates to an effective suppression of ~ 38 dB at the notch frequency, 2 MHz.

5-1-3 Digital circuits

System-level behavioural simulations are executed to verify the performance of the DCO interface and the automatic frequency noise cancellation (AFC) block. RF and analog blocks of the receiver – LNA, mixer, low pass filter and comparator – are described using Verilog-A models, available in the CADENCE library. Those are used together with RTL-level Verilog description of digital interface and AFC to perform mixed signal simulations using Spectre-Verilog simulator.

FSK-modulated signals, generated using random binary inputs, are applied to the receiver input. The demodulated comparator output and the AFC output are plotted for the scenarios in which:

- the frequency offset between input carrier frequency, f_c and DCO center frequency, f_{DCO} is either constant or drifting, as per *Bluetooth Low Energy* (BLE) standard¹.
- AFC is either disabled or enabled. As shown in Chapter 4, AFC can be independently controlled using AFC_EN.

¹As per BLE standard, maximum tolerable frequency offset is ± 100 kHz and frequency drift is ± 50 kHz at 400 Hz/ μ s

Static offset

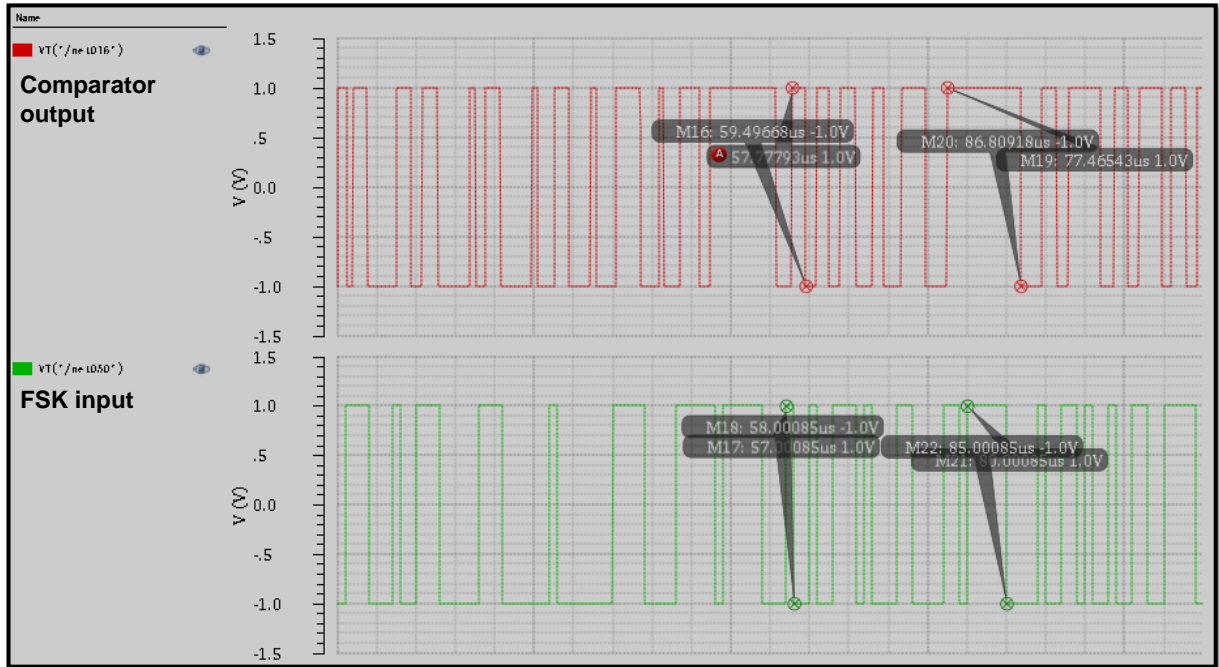


Figure 5-16: Simulation results of the AFC - static offset of 100 kHz and AFC disabled.

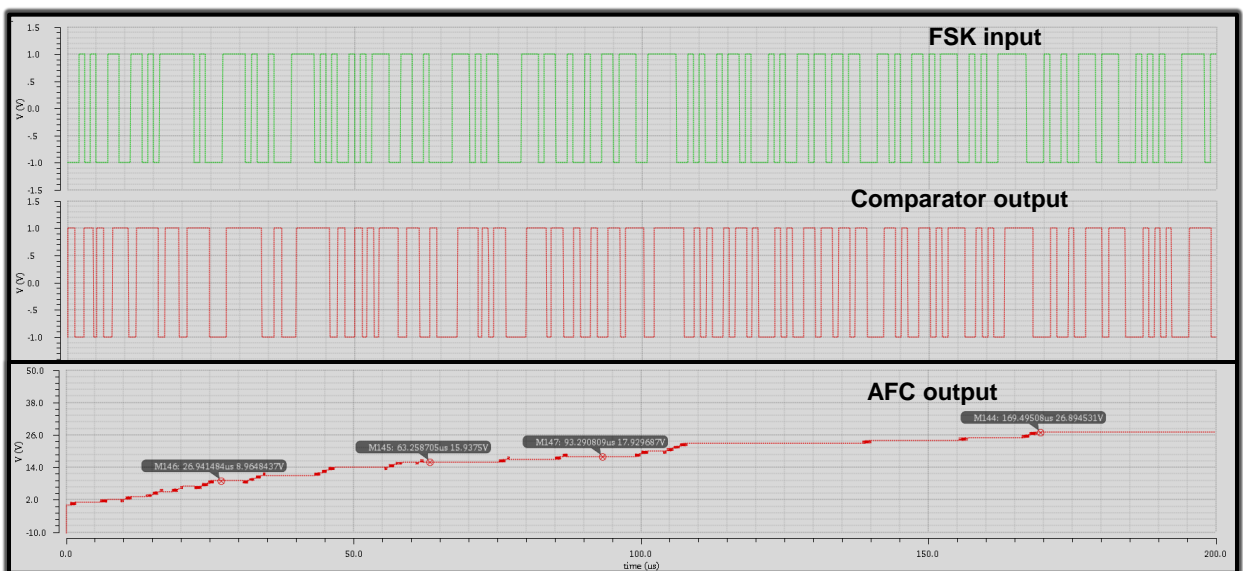


Figure 5-17: Simulation results of the AFC - static offset of 100 kHz and AFC enabled.

Figure 5-16 shows the random binary input (green) and comparator output (red) in the presence of 100 kHz frequency offset when AFC is disabled. It can be identified in the figure that the comparator output often fails to reproduce the random input and the mismatches are the result of undesired phase accumulation due to frequency offset, as described in Chapter 3.

When the simulations are repeated with AFC turned on, AFC modifies the frequency tuning word based on its estimation of frequency offset. This negates the undesired phase accumulation and forces the loop to track the input signal. The plot, shown in Figure 5-17, reveals that comparator output concurs with the random binary input and the AFC estimation of frequency offset is 26.89 (≈ 108 kHz). Insufficient filtering by the integrator is the prime reason for estimation error.

As discussed in Chapter 3, AFC response can be sped up and slowed down using `AFC_GAIN`. Based on the results of the MATLAB simulations, `AFC_GAIN` is set to be '011', for AFC to settle within $150 \mu\text{s}$. Figure 5-17 confirms the settling behaviour. A sinc filter with tap 32 is used in this simulation by setting `FIR_SEL` to be '00.'

Dynamic offset

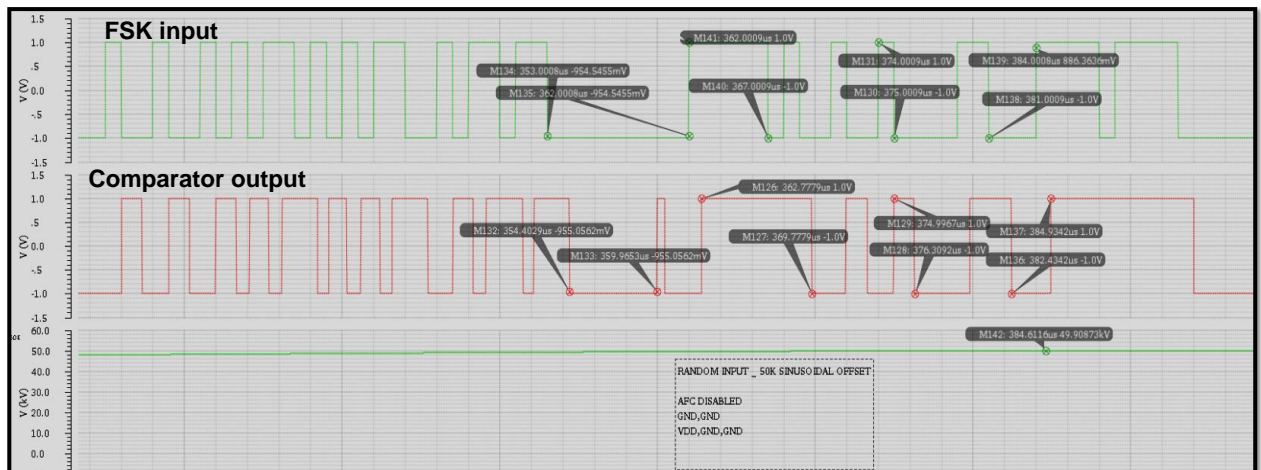


Figure 5-18: Simulation results of the AFC - sinusoidal offset of 50 kHz and AFC disabled.

For dynamic offset simulations, a sinusoidal frequency offset with amplitude 50 kHz and frequency 625 Hz is added to the frequency shift keying (FSK) modulated signal [14]. Further, the comparator output is used to generate eye-patterns for the duration of $400 \mu\text{s}$. The eye-patterns are plotted in 4 windows each with a time-span of $100 \mu\text{s}$ to provide a qualitative measure of the tracking behaviour of the AFC.

The comparator output is compared with the random input in Figure 5-18, when AFC is turned off. Similar to static offset scenario, the phase-to-digital conversion (PDC) loop fails

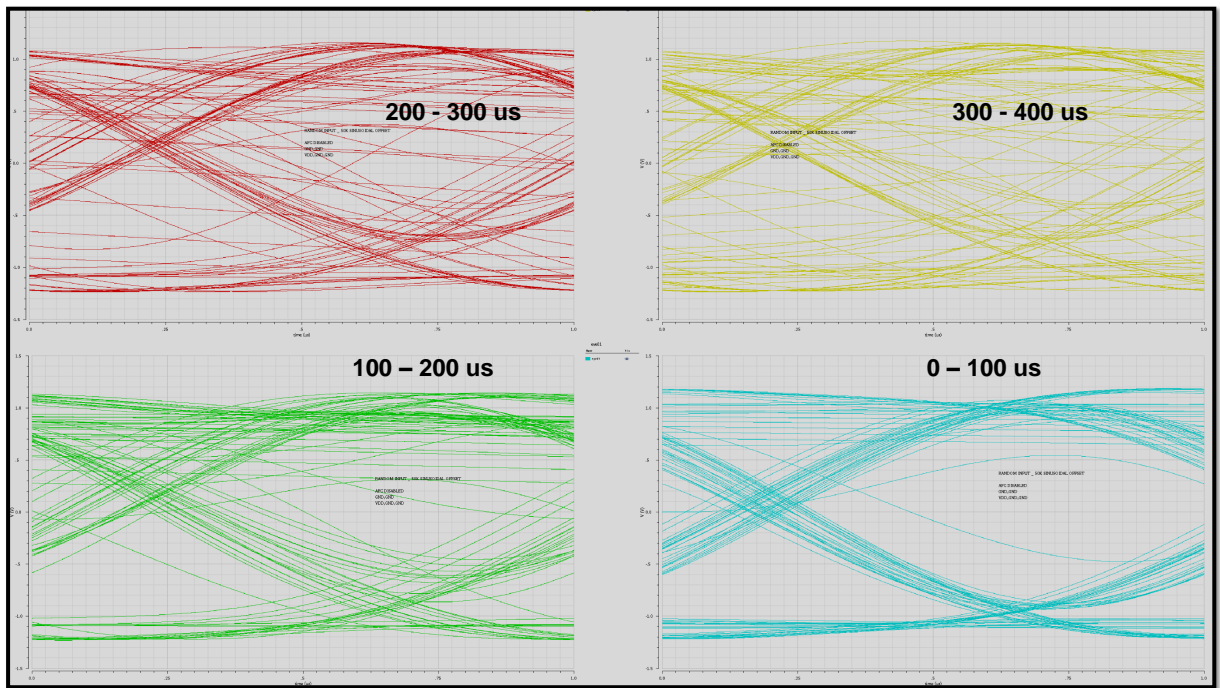


Figure 5-19: Eye diagram - sinusoidal offset of 50 kHz and AFC disabled.

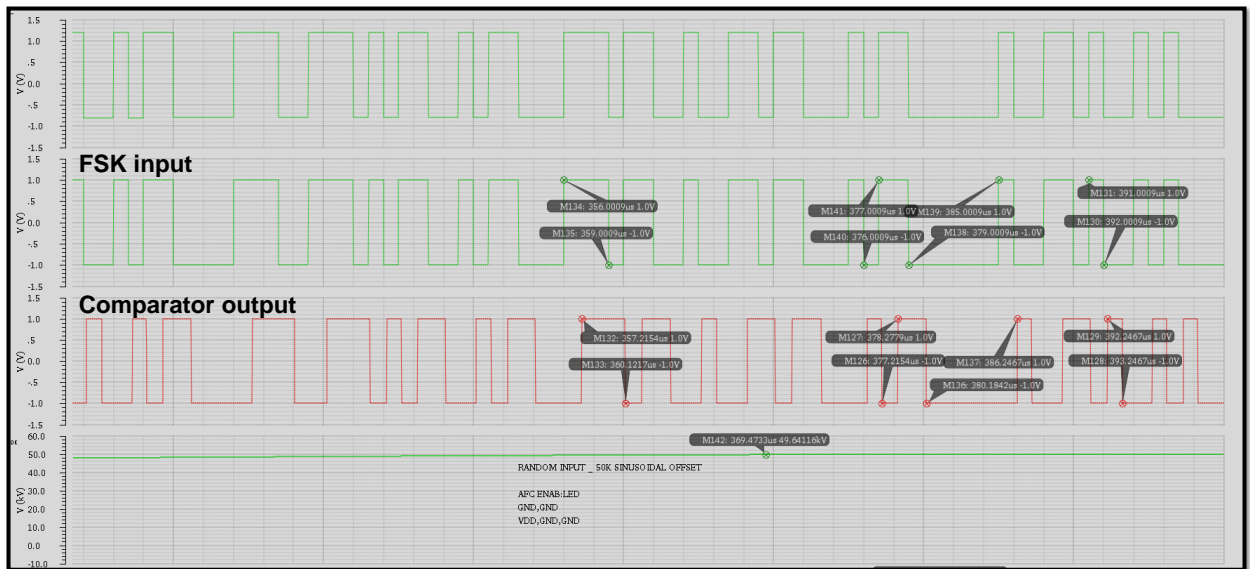


Figure 5-20: Simulation results of the AFC - sinusoidal offset of 50 kHz and AFC enabled.

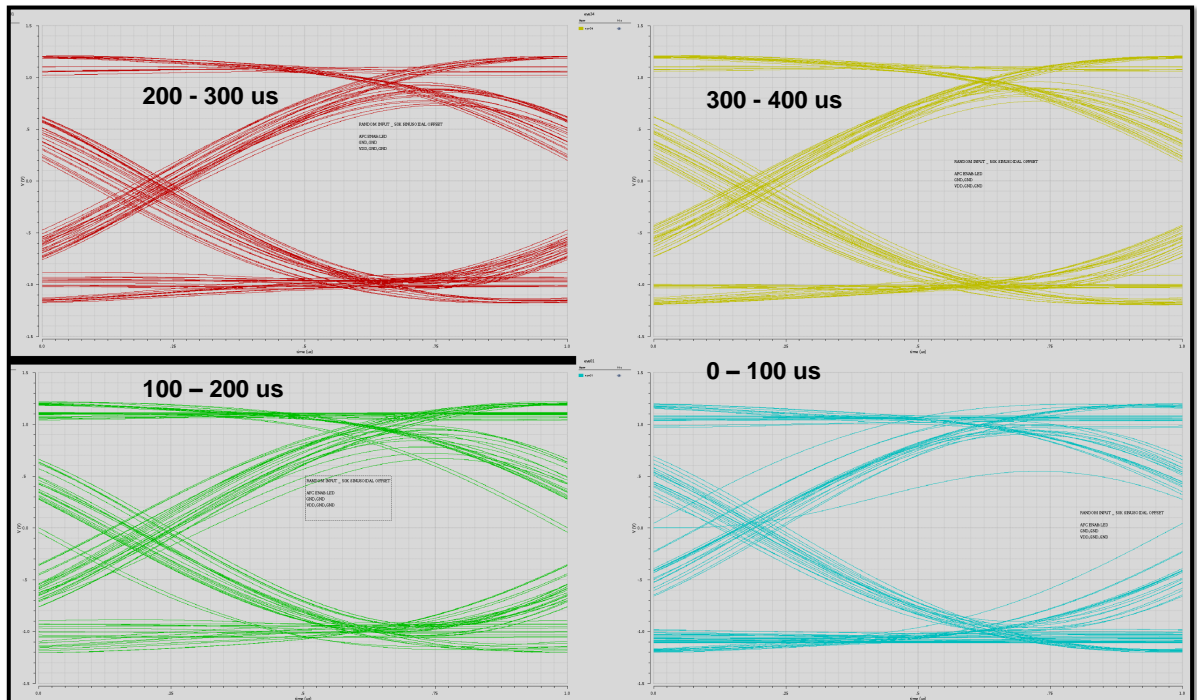


Figure 5-21: Eye diagram - sinusoidal offset of 50 kHz and AFC enabled.

to track the input resulting in mismatches between comparator output and random input. Besides confirming the behaviour, the eye-diagram, shown in Figure 5-19, indicates that mismatches are scant in the span of 0–100 μs and increases with time.

The simulations are repeated with AFC enabled and the results are plotted in Figure 5-20 and Figure 5-21. With bereft of mismatches, Figure 5-20 implies an efficient tracking of PDC loop in the presence of offset. Sharp and wide-opened eyes in Figure 5-21 provide more explicit account on AFC's performance. Settings of AFC_GAIN and FIR_SEL are kept unchanged from static offset scenario.

Performance of the AFC block is observed for large frequency offsets and found out that it can track a maximum dynamic frequency offset of 75 kHz. However, in the case of static frequency offset, its performance is limited by its smaller bandwidth. As explained in Chapter 3, a trade-off exists between speed and accurate tracking of frequency offsets due to its overlap with input band. Orthogonal optimization of tracking speed and accuracy and power-efficient implementation are marked for future work.

5-2 Other blocks

In this section, the blocks, that are reused – low noise amplifier, digitally controlled oscillator and comparator – are described briefly.

5-2-1 Low noise amplifier

A single-ended cascoded LNA is employed for its low power consumption and better noise performance in comparison to differential LNA [40]. Post-layout simulations of the circuit, shown in Figure 5-22, reports that LNA could achieve 5.9 dB noise figure and voltage gain of 25 dB from antenna input to LNA output while consuming 650 μA of current at 0.85 V supply voltage. Impedance matching is achieved using a LC network, which also provides a passive voltage gain of 14 dB. It should be noted that gain of the matching network is determined by the impedance conversion ratio and it is shown below:

$$Gain = 20 \log \left(\sqrt{\frac{R2}{R1}} - 1 \right) \quad (5-2)$$

where, $R1$ is the 50Ω source impedance and $R2$ is the impedance seen at the gate of the LNA input. Further, Resonant LC tank employs switch-able capacitors for accurate passband tuning, thus allowing high-Q load. Wide metal layers and additional bondpads for supply and ground are used to minimize parasitics in the layout.

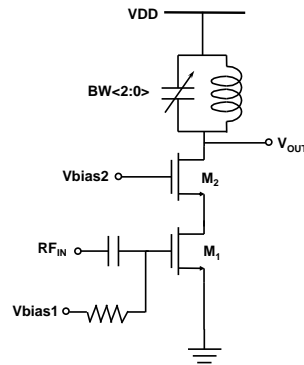


Figure 5-22: Schematic of the reused LNA.

5-2-2 Digitally controlled oscillator

A LC resonant tank based oscillator with digitally tunable capacitor banks is used in this receiver. LC resonant tank is preferred for their better phase noise performance compared to relaxation oscillators. The capacitors are designed such that oscillating frequency of DCO covers entire BLE operating range 2.4 – 2.5 GHz with a resolution of 4 kHz. A complementary cross-coupled topology is adopted to provide negative resistance in the oscillator. The schematic of the oscillator is shown in Figure 5-23. The tail bias current is controlled using a programmable resistor bank connected to the supply using PMOS switches.

The performance of DCO based on post-layout simulations are summarized in Table 5-1. It should be noted that tunable DC coupled buffer is used at the output of DCO to drive passive mixer and power amplifier [36].

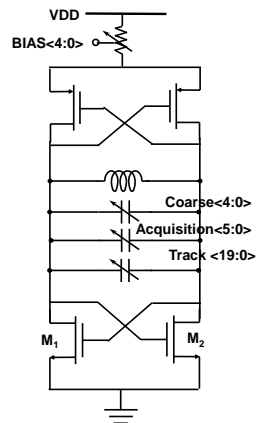


Figure 5-23: Digitally controlled oscillator.

Table 5-1: DCO simulation results - summary.

Parameter	Result
Frequency range	2.06 GHz - 2.85 GHz
Frequency resolution	≈4.5 kHz
Phase noise @ 1 MHz	-115 dBc/Hz
Current consumption (DCO + DCO buffer)	<580 μA

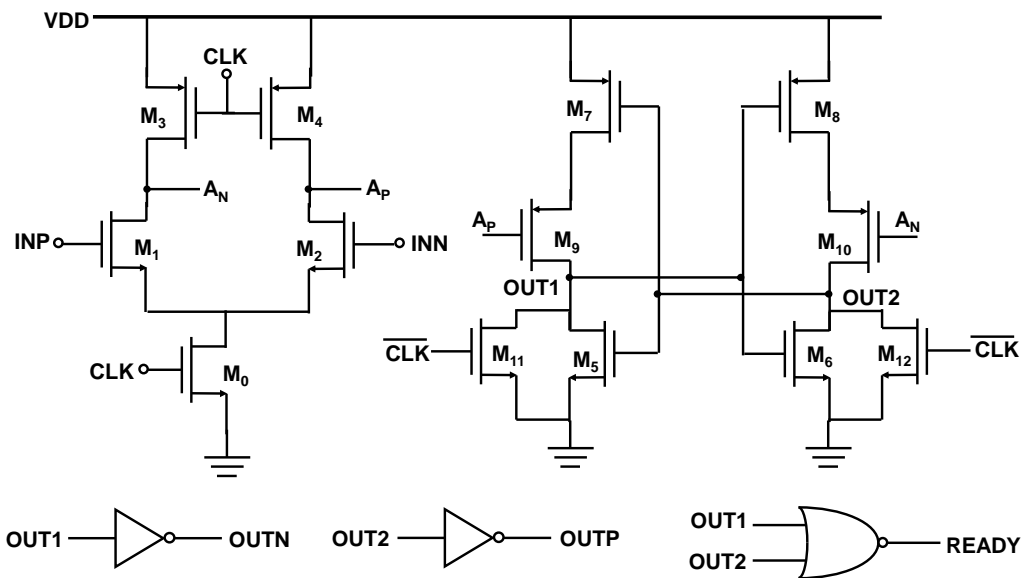


Figure 5-24: Two-stage dynamic comparator.

Table 5-2: Comparator - delay profile.

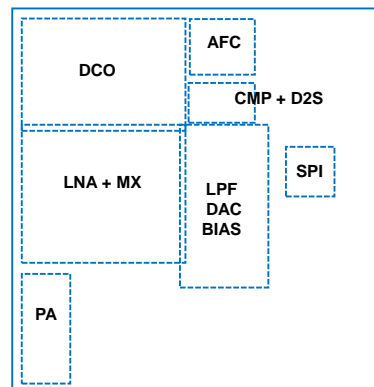
Input amplitude (mV)	delay (ns)
0.1	9.3
1	8.7
10	7.7
100	4.3

5-2-3 Comparator

A two-stage dynamic comparator, shown in Figure 5-24, is used in this work [55]. During comparison operation, the two outputs OUTP and OUTN are pre-charged low. As soon as the comparator makes a decision, one of the outputs will go high. A logical NOR is used to generate an active-low *ready* signal to sample the comparator output. No static biasing, selective use of high and low V_T transistors and careful layout minimize the total power consumption. Dummy transistors and dummy metal-wiring are used to reduce dynamic offset matching. Comparator delay is estimated for different input amplitudes, sampling at 32 MHz and are tabulated in Table 5-2. Based on the conclusions given in Chapter 3, the results indicate that comparator delay, lower than 31.25 ns, hardly affects the receiver performance.

Besides these blocks, offset trimming DAC (OT-DAC) and differential-to-single ended (D2S) buffer are reused in this design. Employing current-steering principle, OT-DAC introduces offset current at the input nodes of the opamp in the last section of the elliptic LPF to maintain zero offset at filter output. The offset current can be programmed using a control word from a serial-to-parallel interface (SPI) slave. D2S buffer, as the name indicates, converts filter differential output into single-ended signal that can be read-out from the IC.

5-3 Top-level layout

**Figure 5-25:** Top-level floorplan of DIFDEM.

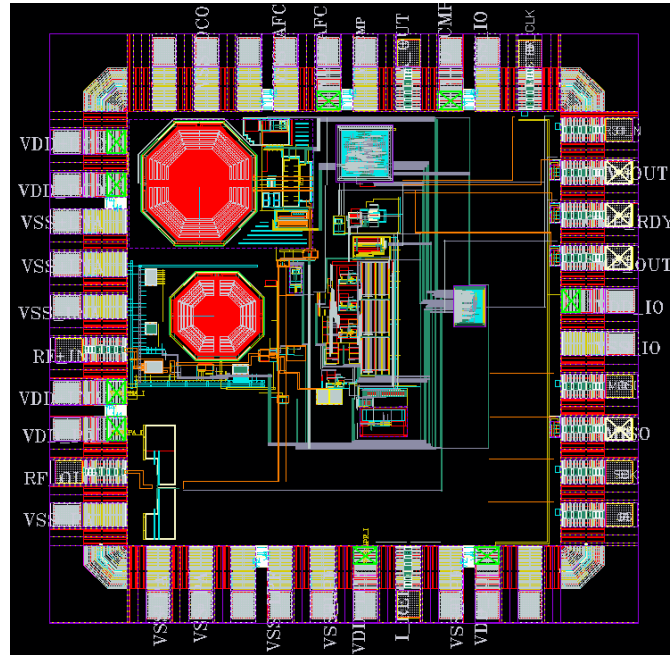


Figure 5-26: Top-level layout of DIFDEM.

Figure 5-25 and Figure 5-26 show the floorplan and layout of the entire receiver including the designed and reused blocks. It also includes clock generation circuitry, LO buffers, power-amplifier, SPI slave and bond-pads.

LNA is placed as close as possible to the bond-pads so that any undesired impedance due to metal-connects at LNA input is reduced, as it would degrade signal-to-noise ratio (SNR) of the receiver. For similar reasons, LNA, transconductor and passive mixer are also placed as close to each other as possible. Especially, parasitic capacitances to ground at LNA and transconductor output introduce unwanted loading and thus deteriorate maximum achievable gain and minimum noise figure.

As described in Section (4-1-2), mismatches in LO trace driving passive mixer would cause DC offsets. Hence, care is taken to maintain symmetric routing between LO buffer and passive mixer. Also, for hard switching of passive mixer, LO signal traces are kept short. Inadvertently, short LO signal traces reduce the loading capacitance of LO/DCO buffers and thus improve the energy efficiency of the receiver. Top metal layers (M6-M8) are always preferred for longer routing in RF blocks.

Short LO signal traces constrain the location of LO/DCO buffers and DCO. However, two inductors (each one from resonant tanks of LNA and DCO) placed close to each other would suffer from injection pulling due to their magnetic coupling. Accounting for this trade-off, an optimum location, based on other earlier tape-outs, is chosen. Further, digital interface is placed adjacent to the DCO, as it drives the tracking bank of DCO.

Placement of low-frequency blocks – TIA, elliptic LPF and comparator – are less constrained by parasitic capacitance. In these blocks, routing is optimized to minimize gain degradation

and DC offsets and to ensure desired pole/zero frequency. Location of biasing circuitry and SPI slave are decided, considering optimum routing to all the blocks.

Multiple power domains are employed to reduce parasitic coupling between the high frequency blocks and to minimize ground fluctuations for sensitive blocks. Metal layers M1 and M2 are adopted for power routing. Large width is used wherever possible to minimize IR drop. Decoupling capacitors are used to reduce supply voltage fluctuations. Diodes are used to avoid potential latch-ups. Bondpads, from IMEC in-house library, are used for off-chip interface in this design.

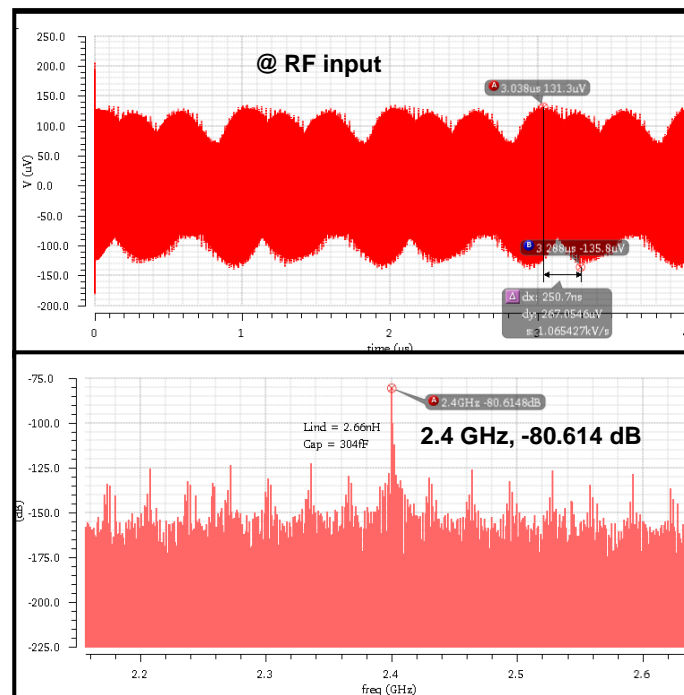


Figure 5-27: Top-level simulations - RF signal at the input.

Post-layout transient simulations are performed to verify the overall receiver gain from antenna input to comparator output. To verify the performance, a RF signal of -80 dBm magnitude at 2.4 GHz is fed to the input of the impedance matching circuit. LO oscillator is tuned to oscillate at 2.401 GHz, resulting in a baseband signal of 1 MHz at the mixer output. The comparator is clocked at 32 MHz and the input signal at the output node of every block is plotted in the Figure 5-27 – Figure 5-31. Since LNA and current-driven passive mixer provide ~ 50 dB gain, their combined noise figure, shown in Figure 5-32 would provide a rough estimate for the overall noise figure of the receiver. On the other hand, large-signal characteristics of the elliptic LPF would mostly determine the linearity of the receiver.

5-4 Tape-outs

In this section, a testbench developed for measurements is discussed first and then the bugs encountered in the first test chip are analysed and debugged. Later, based on the discussion,

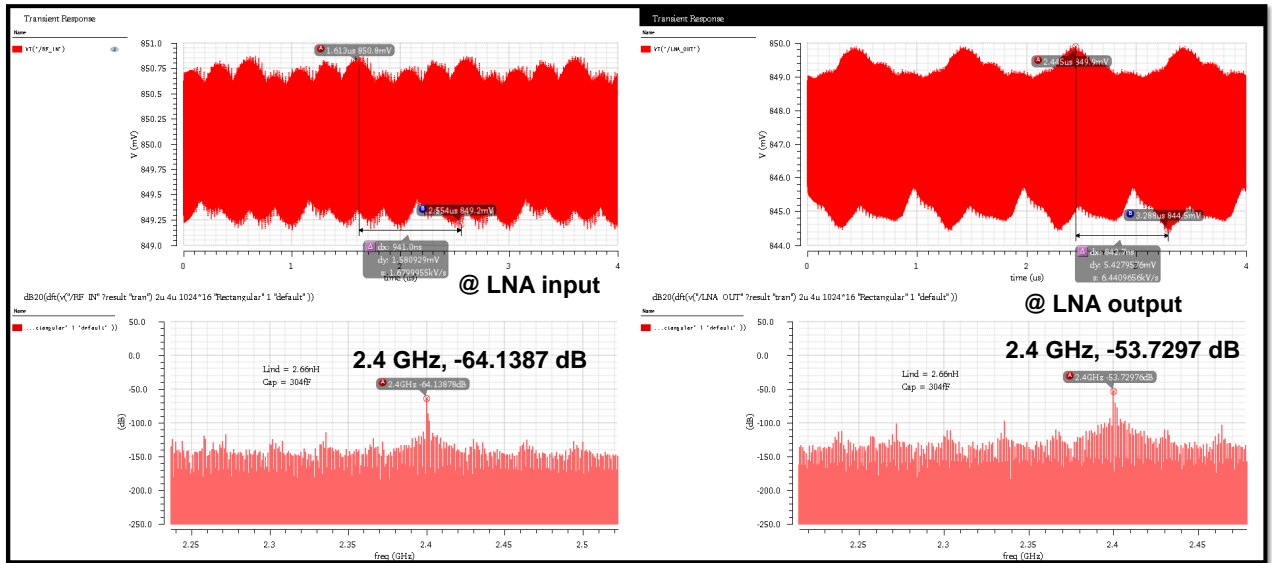


Figure 5-28: Top-level simulations - RF signal at the LNA input and output.

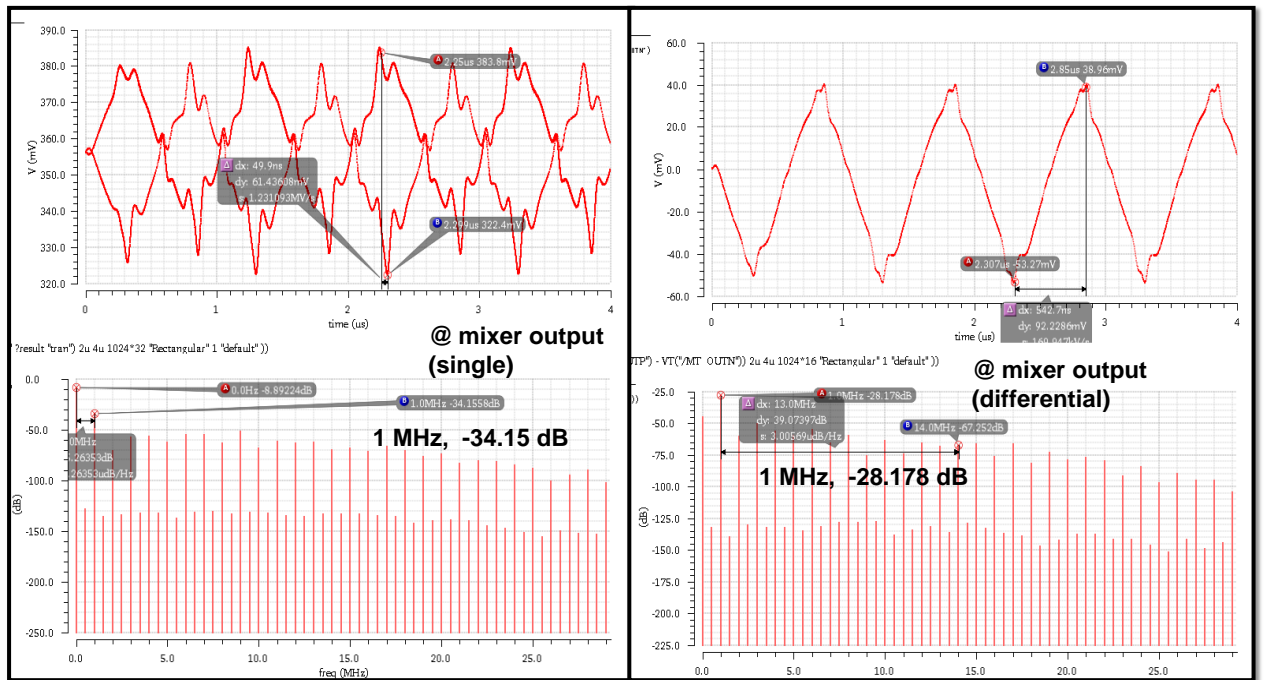


Figure 5-29: Top-level simulations - baseband signal at the mixer output.

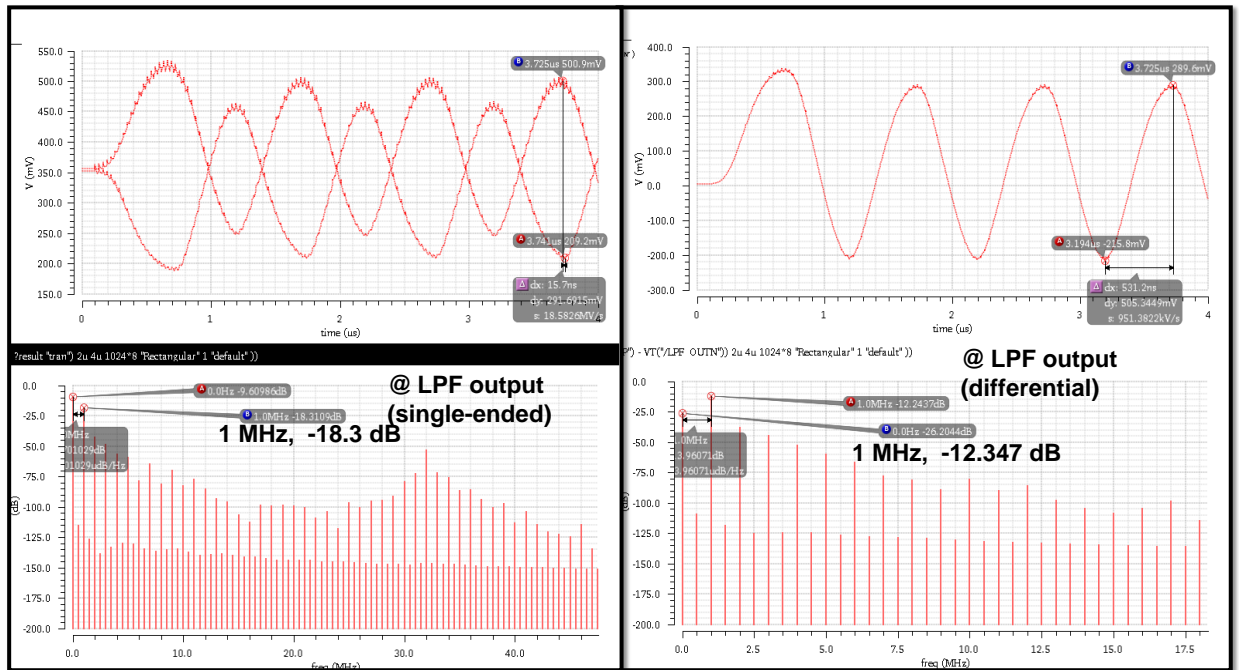


Figure 5-30: Top-level simulations - baseband signal at the elliptic LPF output.

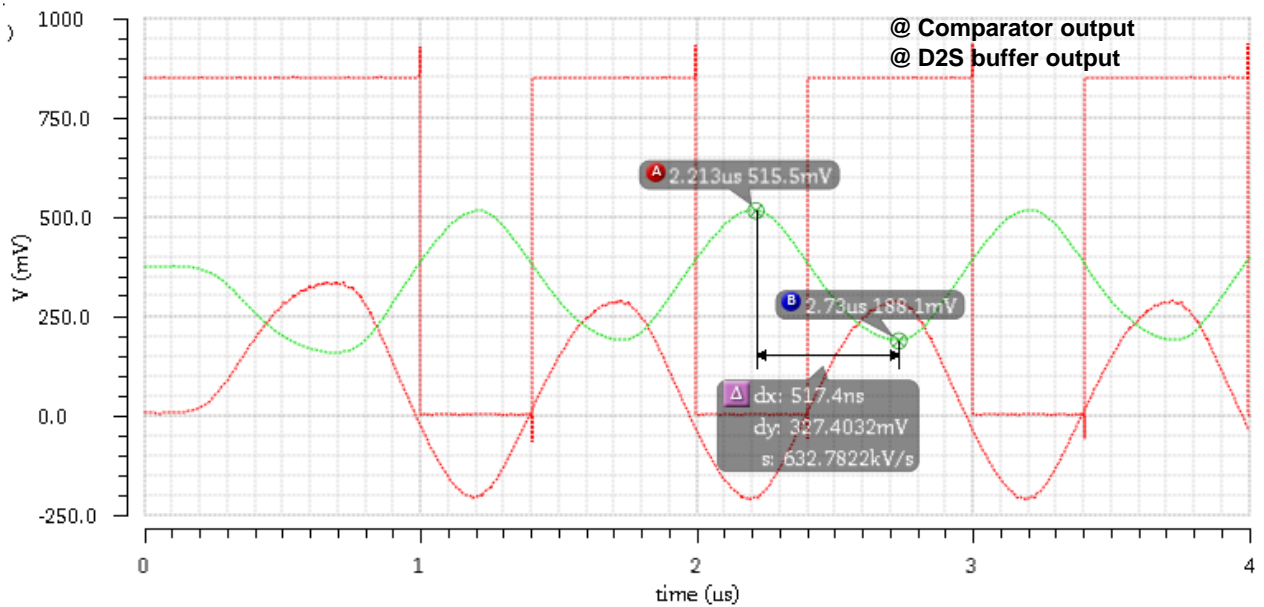


Figure 5-31: Top-level simulations - baseband signal at the comparator output and buffer output.

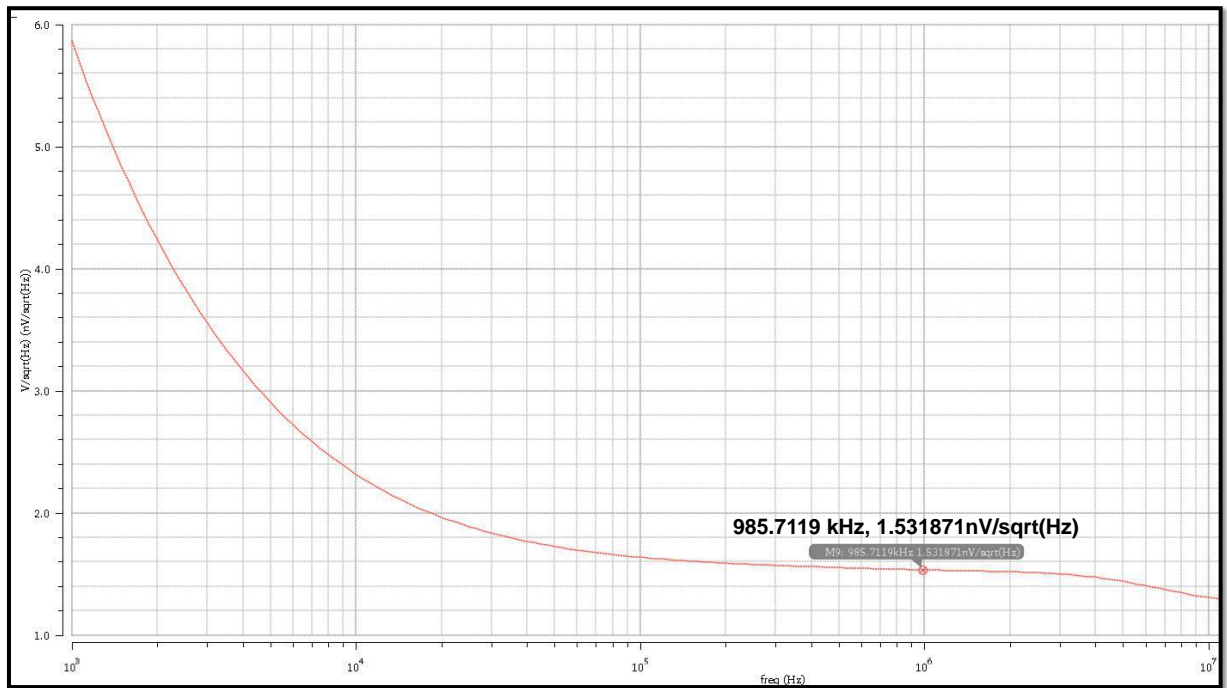


Figure 5-32: Top-level simulations - noise performance of LNA and mixer.

the modifications introduced into the second test chip are described.

5-4-1 Measurement setup

The chip micrograph of the first test chip is shown in Figure 5-33. The entire chip consumes an area of $1.30\text{ mm} \times 1.30\text{ mm}$. As seen in the figure, the chip is pad-limited and the core area is much smaller. It has six separate power supplies for analog and digital circuitries to avoid noise coupling via supply and ground. Down-bonds are used to connect the grounds of all power domains except digital circuitry to IC metal-casing. It minimizes the inductance due to bond-pads. The chip is placed in a QFN40 package.

Printed circuit board (PCB) contains packaged chip, low drop-out (LDO) regulators, level-shifters, impedance-matching circuit, FPGA interface and Teensy micro-controller. An external clock of frequency 32 MHz, generated by signal generator, is used as reference clock for the chip. SMA connectors are used to read out PA output, D2S output, comparator and its ready signal. They are also used to feed in RF signal to LNA input port via impedance matching circuits. The photograph of test PCB is shown in Appendix B.

Figure 5-34 shows the block diagram of the measurement setup. Teensy micro-controller and FPGA are used to interact with SPI interface from PC. Python-based GUI is developed to read into/out of the SPI registers.

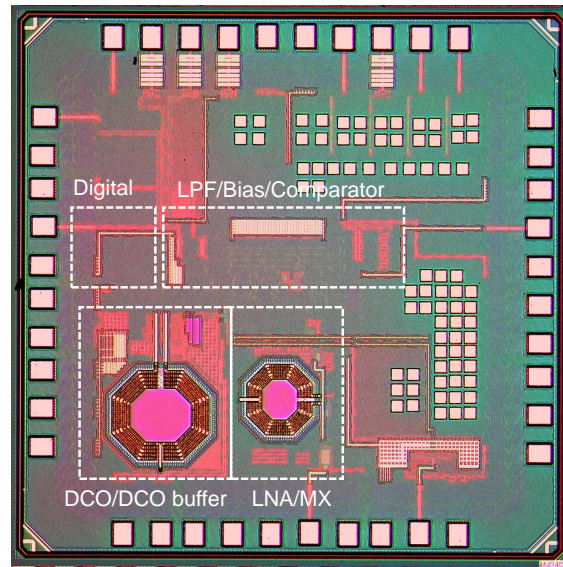


Figure 5-33: Chip micrograph of the first test chip.

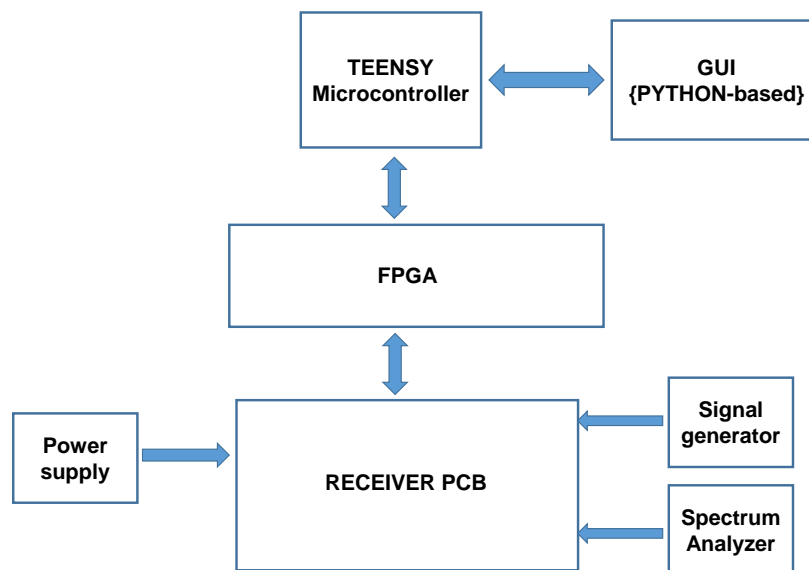


Figure 5-34: Block diagram of the measurement set-up.

5-4-2 First test chip – bugs and fixes

The performance of the receiver is measured with the test-bench described above. Sadly, functionality test of the receiver failed during measurements, leading to a post tape-out analysis. On debugging, following issues are identified in the chip and necessary modifications are

added to the second test chip.

Comparator output is always 'high'

When a FSK signal with input pattern '101011110000' is introduced at the RF input, it is found that comparator output is always 'high' irrespective of input signal. This behaviour is identified due to a positive edge-triggered flip-flop at the comparator output. As described in earlier section, an active-low ready signal is used to sample the comparator output. Hence, comparator output should be followed by a negative edge-triggered flip-flop clocked by *ready* signal. An eleventh-hour change for high drive strength would have caused this mistake, as it was not observed during simulations.

Common mode voltage fluctuations at elliptic LPF output

Elliptic LPF output via D2S buffer is measured to characterize the filtering behaviour. Measurement results showed fluctuations in common mode voltage at filter output, leading to poor gain performance. Extensive debugging, together with post-layout simulations, revealed three issues that actuate this behaviour in tandem.

- D2S buffer, adopted in this work from the earlier design, has two channels for I/Q paths. For single channel phase-domain processing, only I-channel is used and output of the Q-channel is tied to ground. Due to feedback action, this pulls down the common mode voltage of filter output and degrade the performance.
- Common mode voltage (V_{CM}) of RF transconductor in the mixer and that of opamps in the baseband share the V_{CM} node in the biasing circuit. It results in undesired parasitic coupling between these nodes. Post-layout simulations confirmed that using different separate V_{CM} s for RF transconductor and opamp in the biasing circuitry would minimize these fluctuations.
- Self-mixing and LO mismatches are also identified from the measurements. They were induced by a long LO trace running parallel to the GND of RF transconductor, shown in Figure ???. Layouts are redone to shorten this long LO trace and minimize self-mixing and asymmetry.

Though functionality and performance of the taped out chip are affected by above issues, it can be used to obtain a reasonable estimate on the power consumption of individual blocks. The measured current consumption of these blocks is given in Table 5-3. The numbers correlate well with simulation results (except DCO), suggesting the possibility of more energy-efficient receiver compared to SIF-PDC [4], provided these bugs are resolved.

5-4-3 Second test chip

The bugs, identified in the first test chip, are fixed in the design intended for second test chip.

- Incorrect positive edge-triggered flip-flop is replaced with negative edge-triggered flip-flop at the comparator output.

²It should be noted that post-layout simulations failed to predict this large variation. Designer has been notified about this behaviour.

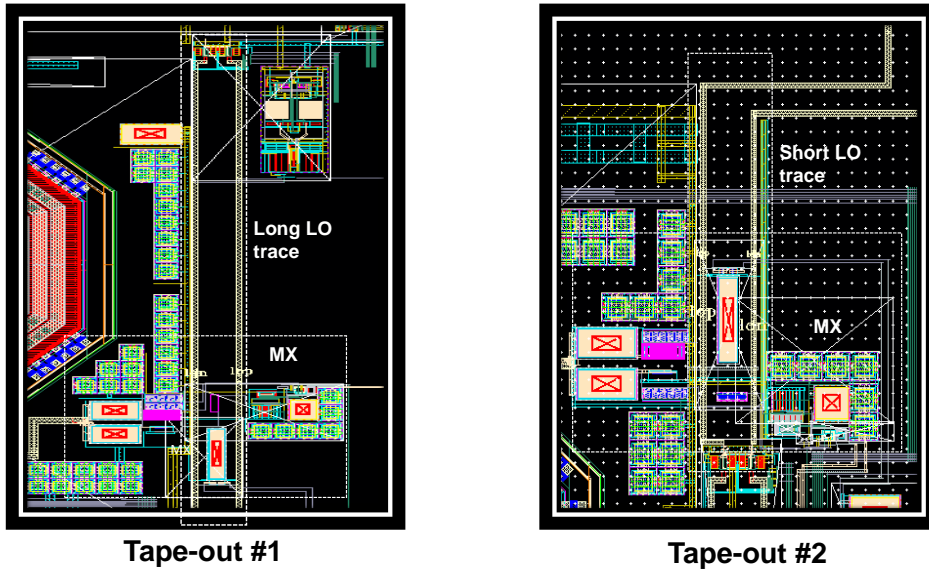


Figure 5-35: Long and short LO traces.

Table 5-3: Measured current consumption of the blocks in the receiver.

Blocks	Current consumption (μA)
LNA + RF transconductor	620 – 800
TIA + LPF + biasing	180 – 210
DCO + DCO buffer	740 – 1200 ²
Digital circuitry + clock generation	95 – 110
Total	1635 – 2320

- Q-channel outputs of D2S buffer are left unconnected to prevent V_{CM} fluctuations.
- Separate V_{CM} nodes are used to independently set V_{CM} of RF transconductor and elliptic LPF.
- Symmetrical LO trace layout is realized to reduce DC offset at TIA output. To shorten the length of LO trace, LNA is flipped vertically and RF transconductor, mixer and TIA are relocated and rerouted accordingly. Meanwhile, the edge-to-edge distance between two inductors (DCO and LNA) is maintained to be $>150\ \mu\text{m}$ to minimize magnetic coupling.

In addition to the bug-fixes, some blocks are updated in this tape-out version. The measurement results of other in-house designs of IMEC raised questions on the operation of existing DC-coupled DCO buffer at lower supply voltages ($<1\ \text{V}$). Hence, it is replaced by a conventional AC-coupled inverter based DCO buffer for low-voltage operation, despite its poor noise performance [36]. Post-layout simulations showed only marginal degradation in phase noise performance.

AFC block in the digital circuitry is revised in this design. Existing version the AFC block is found to have bandwidth dependent frequency-noise cancellation range. In other words, AFC saturates at different frequency offset for different bandwidths, as shown in Figure 5-36. This limitation is fixed in the new design and simulations are carried out to confirm the behaviour. The modification reduces the gate count marginally.

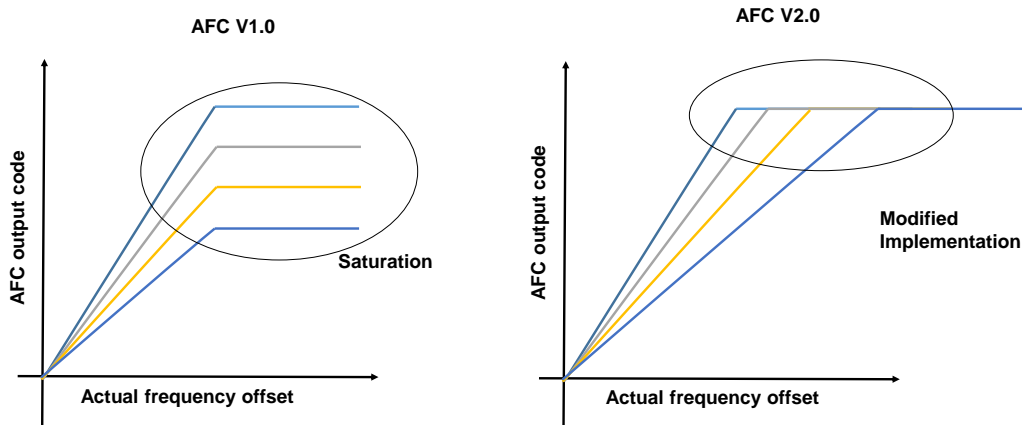


Figure 5-36: First and second version of AFC.

At top-level, no changes are effected on the bond-pads for PCB reuse and minimum complications during the measurement. It results in same chip area 1.7 mm^2 . It should be mentioned that extensive post-layout simulations are carried out on this updated version at different levels of hierarchy to ensure the functionality and performance.

Conclusions

6-1 Summary

An ultra-low power single-channel phase-tracking receiver for *Bluetooth Smart* applications has been proposed in this dissertation. The receiver, also called a direct frequency demodulator (DIFDEM), adopts a phase-to-digital conversion (PDC) loop to directly demodulate the phase/frequency-modulated information at 2.4 GHz frequency.

The first PDC-based receiver, implemented in [4], employs sliding-IF frequency plan to reduce the power consumption of multi-phase LO generation. Thanks to it, receiver consumes only 2450 μA current at 1 V, while achieving -92 dB sensitivity, a state-of-the-art performance. In this work, to further improve the energy efficiency of the receiver, the PDC loop is modified to accommodate a digitally controlled oscillator (DCO), in the place of digital-to-phase converter, without compromising loop functionality. By changing its frequency according to the digital input, DCO provides high-frequency LO phase at low power, thereby it makes energy-efficient zero-IF PDC feasible. It is estimated in Chapter 2 that zero IF PDC could reduce the overall receiver power consumption by at least 20%.

In the process of phase-tracking, the PDC loop behaves similarly to a phase locked loop (PLL) with the received input signal as its reference. This opens up several questions regarding its behaviour and performance, especially in the presence of DCO phase noise. In Chapter 3, not all but some relevant characteristics, such as response time, steady-state behaviour and stability of the PDC loop, are qualitatively analysed using phase-time representation. Further, it is identified that low-frequency DCO phase noise and slow frequency drift, either at the input or DCO, cause pulse width variation at the comparator output. These variations are the resultant of non-zero average frequency difference between DCO and input. Hence to negate their effect, an automatic frequency noise cancellation (AFC) block has been added to the PDC loop. It roughly estimates the frequency difference from the pulse width variation and feeds back to the digital input of DCO for cancellation. Furthermore, the sensitivity and selectivity performance of the DIFDEM are investigated and target specifications are derived for individual blocks for the desired performance.

Based on the derived specifications, blocks such as RF mixer, low-pass elliptic filter and AFC are designed (both circuit and layout) with focus on low-power and low-voltage operation while achieving target specifications. Choice of architecture, low-power circuit techniques, tuning behaviour and layout considerations, applied in their design process, are elucidated in Chapter 4. Blocks such as low noise amplifier (LNA), DCO, comparator and offset-trimming DAC are reused to speed up the design-to-tape out time. Top-level layout of the complete receiver, including SPI registers and bond-pads are done in TSMC 40 nm process.

Post-layout simulation results of the designed blocks and the complete receiver are presented in Chapter 5. They confirm that individual blocks perform as targeted and the receiver could achieve a sensitivity of -89 dBm with ACR of -20/-30 dB while consuming $< 1700\mu\text{A}$ current at 0.85 V. Finally, the failure of first test chip is thoroughly investigated and the identified reasons are listed out. The description of necessary bug-fixes and additional design updates added to the second test chip wrap up Chapter 5.

6-2 Thesis contribution

Objectives of this thesis work are employ PDC loop, achieve ultra-low power consumption and simultaneously meet tight ACR and frequency tolerance specifications of BLE. On this front, PDC loop has been analysed and relevant architecture-level and circuit-level solutions are proposed (Chapters 3 and 4). Proposed solutions are tested through MATLAB modelling and circuit simulations (Chapters 3 and 5).

More specifically, the key contributions of this thesis work are as follows:

- **Adopting DCO as a digital-to-RF phase converter in the PDC loop to improve the energy efficiency of the receiver.** As discussed in Chapter 2, multiple LO phase generation circuits, RF mixer and PLL circuitry can be made redundant by using DCO in the PDC loop. Thus, it reduces the overall power consumption of the receiver.
- **Additional low-speed AFC loop neutralises the effect of slow-frequency drift and close-in DCO phase noise on the PDC loop.** Analysis in Chapter 3 reveals that slow-frequency drift and DCO phase noise cause pulse width variations at the comparator output. A simple background calibration solution, that continuously estimates the average frequency noise in the comparator output and changes frequency control word (FCW) of the DCO accordingly, has been proposed and implemented. Top-level behavioural simulations indicate that desired frequency tolerance specifications are met, thanks to the AFC loop.
- **Using phase-time representation for the internal signals to understand the nuances of the PDC loop and derive conclusions for high performance.** In Chapter 3, essential loop characteristics such as steady-state response, settling time and loop stability are qualitatively analysed using signal phasors at internal nodes. Further, relevance of low pass filter (LPF) phase response and impact of frequency noise and DC offsets, conditions for high sensitivity and selectivity are figured out using this approach.

- **High ACR and resilience to frequency drift and phase noise are achieved simultaneously using a LPF with a pair of complex zeros at 2 MHz.** Besides suppressing interferers at 2 MHz, zeros help to achieve $\sim -90^\circ$ phase delay at 500 kHz by compensating the phase-lag caused by poles. Furthermore, Fleischer-Tow (FT) biquad is restructured to reduce the number of opamps used in the LPF implementation and thus contributing to energy efficiency.

6-3 Future work

The design presented in this dissertation gives satisfactory results in simulations. Due to unfortunate mistakes, the first test chip failed to produce convincing results and the second test chip is due for two more weeks at the time of writing this dissertation. Meanwhile, in this section, few potential improvements for DIFDEM at both system and circuit level are summarized below.

- First, power consumption of AFC can be reduced by using energy-efficient infinite impulse response (IIR) structures for digital LPF, instead of finite impulse response (FIR). Second, with large corner frequency (100-150 kHz), AFC also filters the desired input signal. This causes significant increase in the number of bit errors for long packets ($>400 \mu\text{s}$). Analysing this limitation and addressing it could be the next step in improving AFC performance.
- Offset estimation and cancellation are severely hampered by the use of 1-bit comparator in the PDC loop. Multi-bit ADCs, in the place of comparator, would provide more amplitude information that can be used for background offset cancellation. The benefits of 1-bit comparator can still be achieved by using only MSB of the ADC output to determine the instantaneous DCO frequency. Moreover, the available amplitude information can be effectively used to enhance the accuracy of frequency-noise estimation in the AFC block.
- During the measurement of first test chip, DCO showed abnormal power consumption for supply voltage $< 0.9 \text{ V}$. This behaviour should be investigated and if needed DCO should be redesigned for next fabrication. Further, the possibility of using low-noise transconductance amplifier (LNTA), in the place of LNA and RF transconductor can be explored for minimizing power consumption.

Appendix A

Simulation results

A-1 Opamp

Post-layout simulation results of the opamp, discussed in the Chapter 4, is presented in this section. As summarized in Table (4-6), the opamp provides a open-loop gain of ~ 49 dB close to DC. Figure A-1 shows that opamp also achieves a unity gain bandwidth of 42 MHz and phase margin 59°.

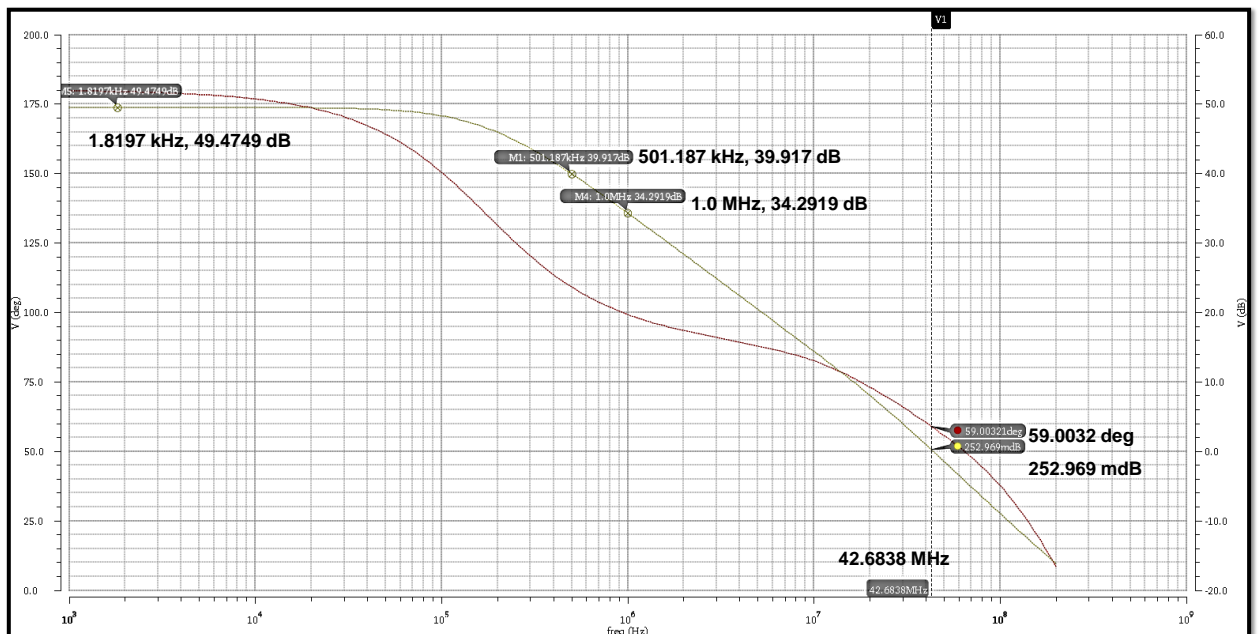


Figure A-1: Simulation results of the operational amplifier - open loop gain.

Noise of the opamp is summarized in Figure A-2. It indicates that total integrated noise of the opamp in 1 kHz - 1 MHz band is -85 dBm. Figure A-3 shows the input referred equivalent noise voltage of the opamp.

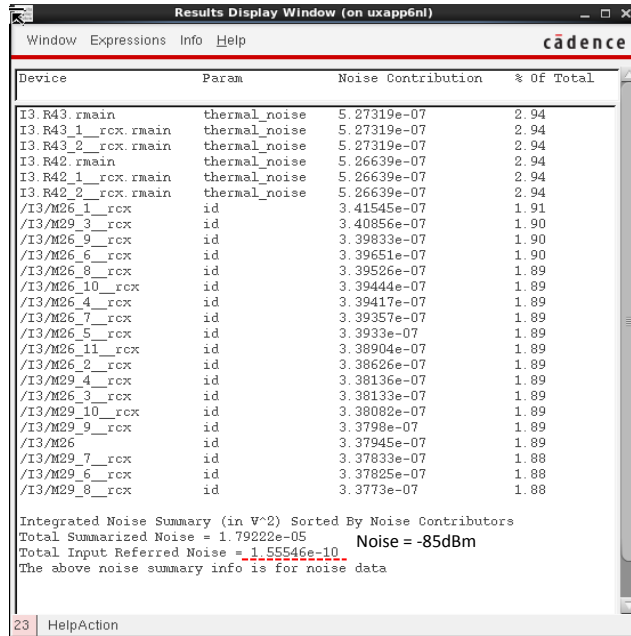


Figure A-2: Simulation results of the operational amplifier - noise summary.

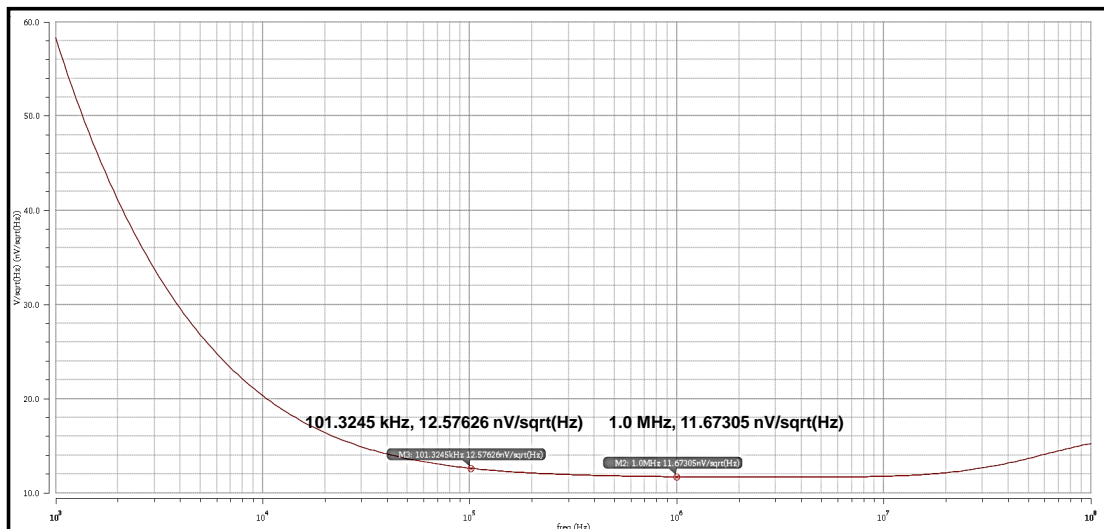


Figure A-3: Simulation results of the operational amplifier - noise.

Figure A-4 shows the input referred 1 dB compression point of the opamp, whereas Figure A-5 verifies the settling behaviour of the opamp by instantly turning it on.

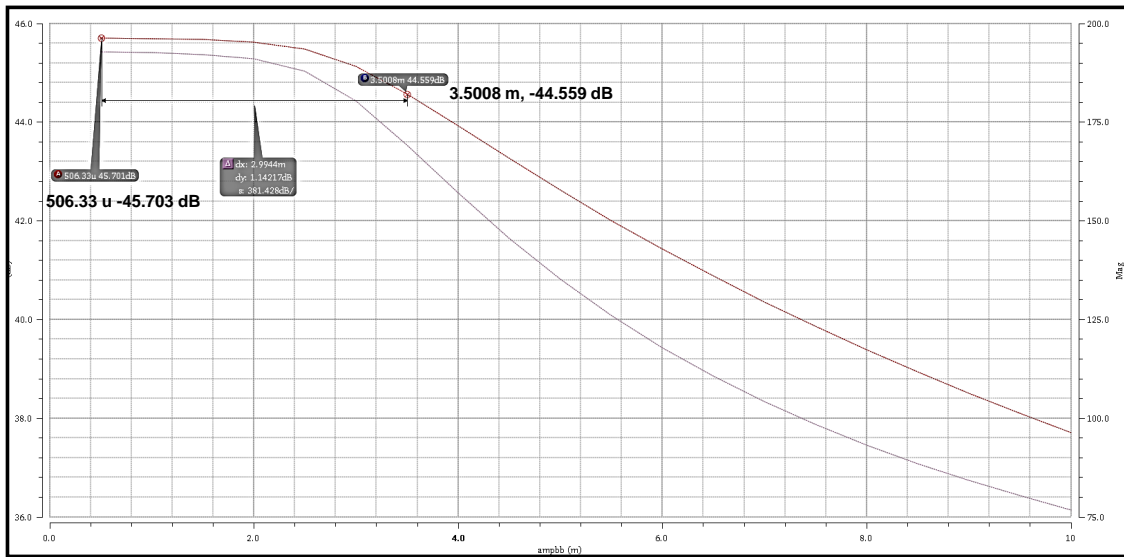


Figure A-4: Simulation results of the operational amplifier - Input 1 dB compression point.

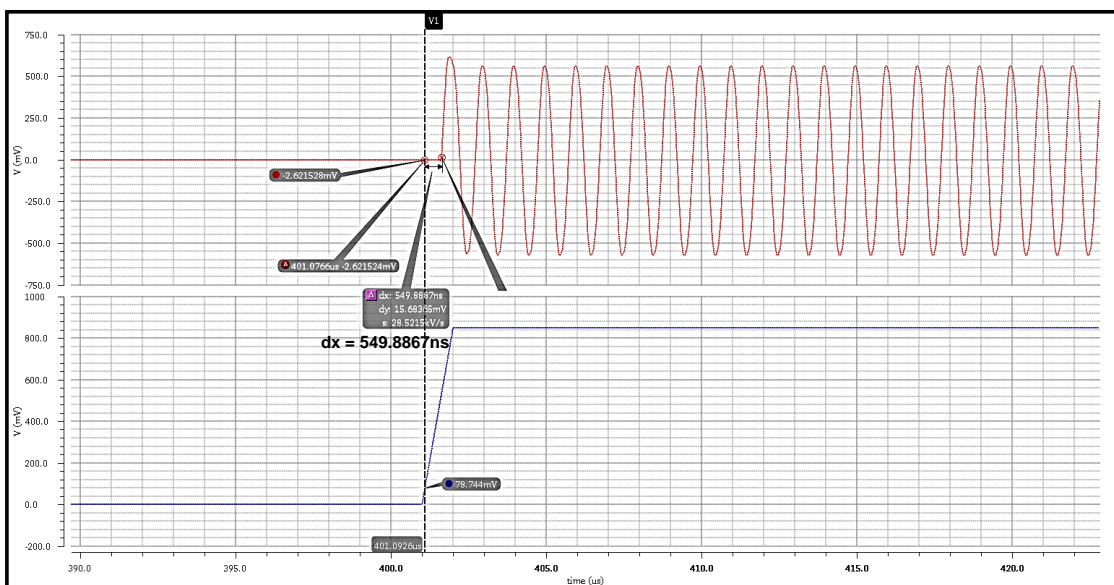


Figure A-5: Simulation results of the operational amplifier - Step input.

A-2 Mixer

This section presents the IIP3 simulation results of the mixer designed in Chapter 4. RF input to the mixer comprises of tones at 2.404 GHz and 2.406 GHz with magnitude of -35 dBV each (Figure A-6). Passive switches are turned on and off by a LO signal, oscillating at 2.4 GHz. The FFT of the mixer output signal, obtained from transient simulation, is plotted in Figure A-7. It shows two desired tones at 4 MHz and 6 MHz with magnitude ~ 10 dBV and IM3 tones at 2 MHz and 8 MHz with magnitude -42.8 dB and -41.4 dB respectively. Using the equation given below, the IIP3 is estimated to be -19 dB.

$$IIP_3 = P_{in} + \frac{1}{2}IM_3 \quad (A-1)$$

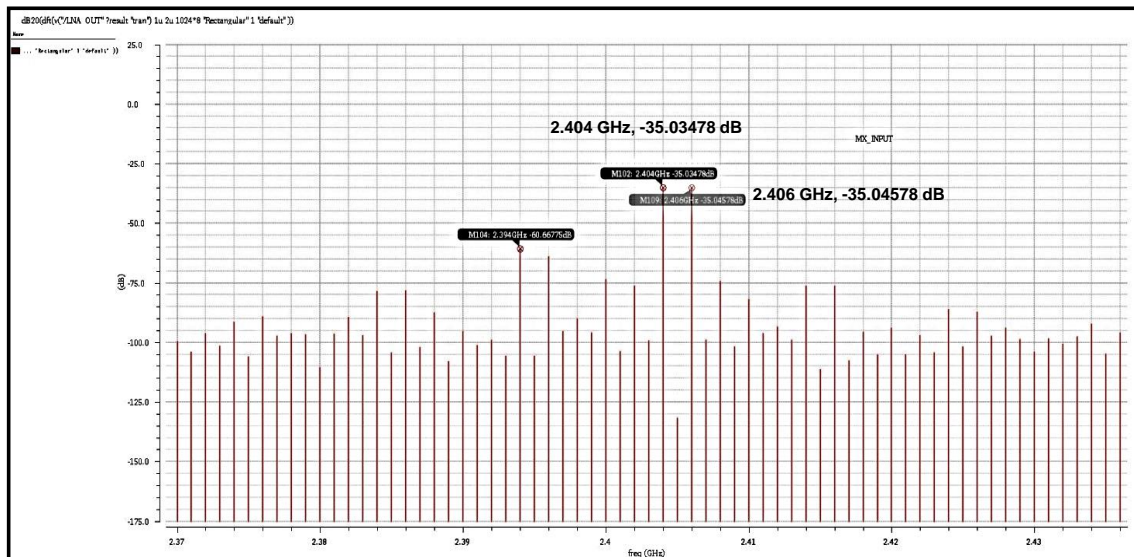


Figure A-6: Simulation results of the mixer - tones at 2.404 GHz and 2.406 GHz at mixer input.

A-3 Combination of LNA and mixer

In this section, the performance of low noise amplifier (LNA) and mixer combination is presented. It achieves a maximum gain of ~ 50 dBm, a noise figure of 7.726 dB and input referred 1 dB compression point of -44.7513 dBm.

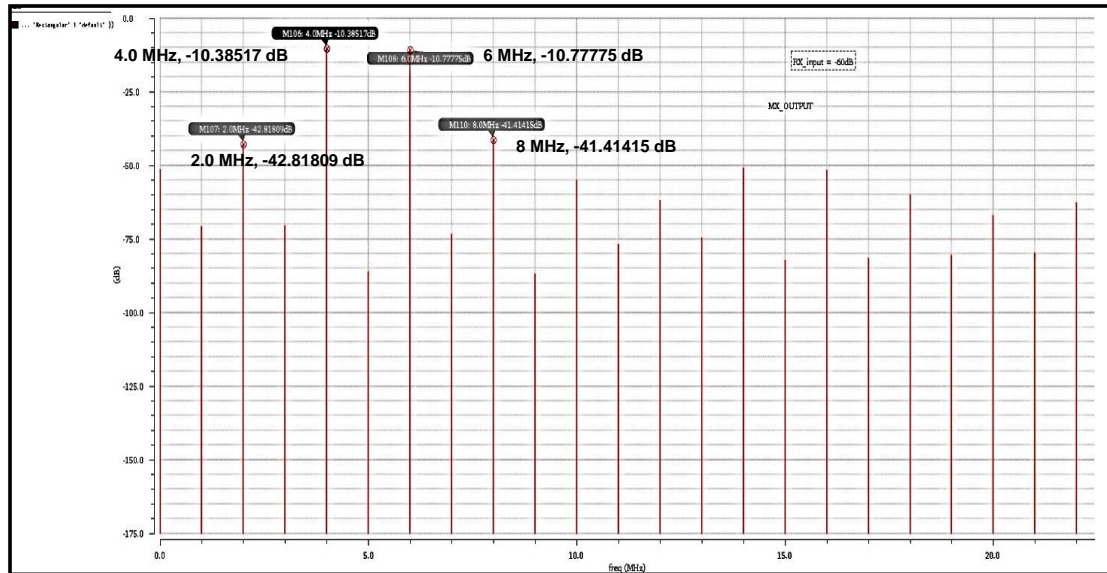


Figure A-7: Simulation results of the mixer - IM3 tones at 2 MHz and 8 MHz together with desired tones at 4 MHz and 6 MHz at mixer output.

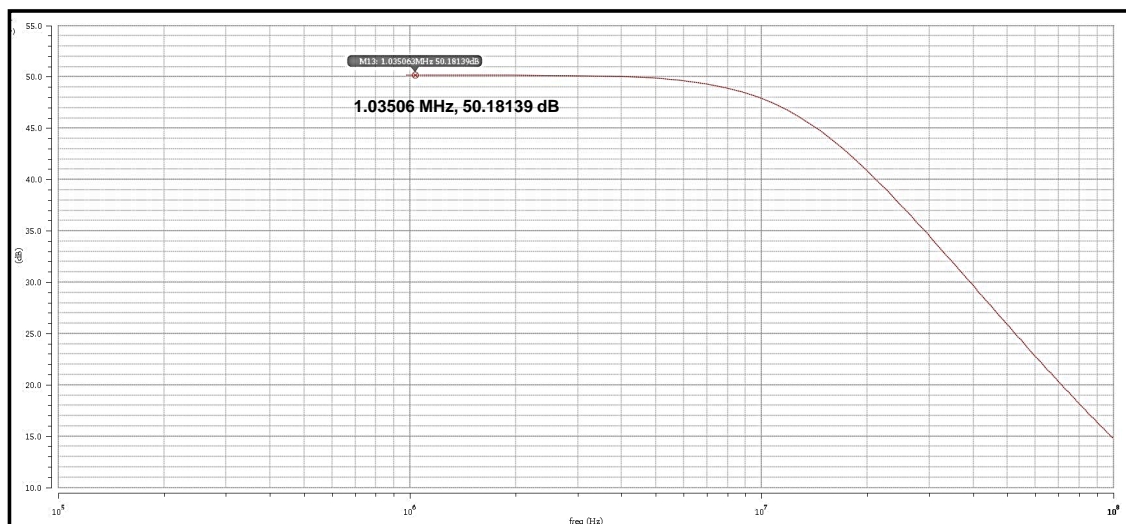


Figure A-8: Simulation results of the LNA + mixer - gain.

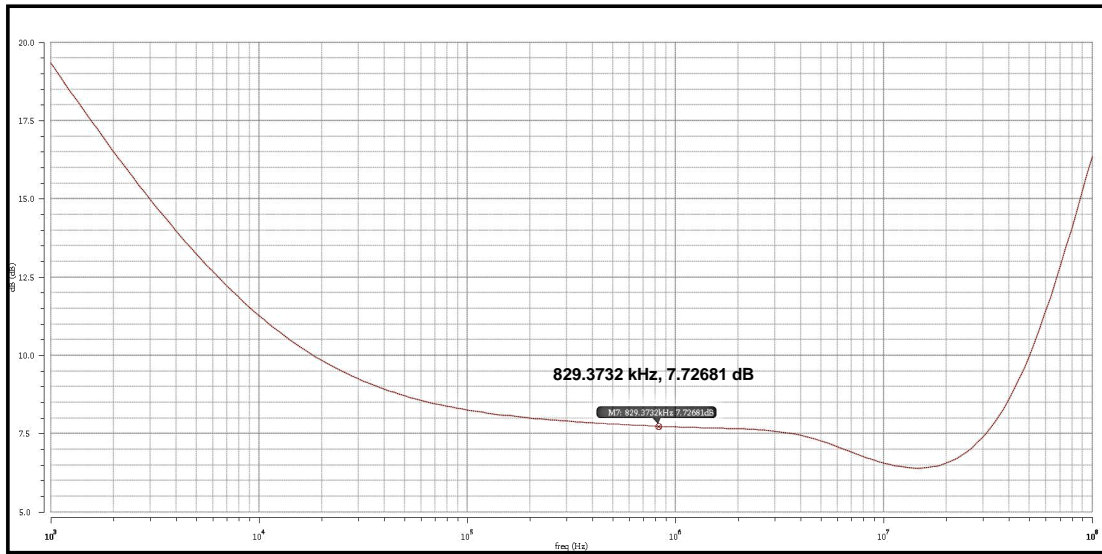


Figure A-9: Simulation results of the LNA + mixer - noise.

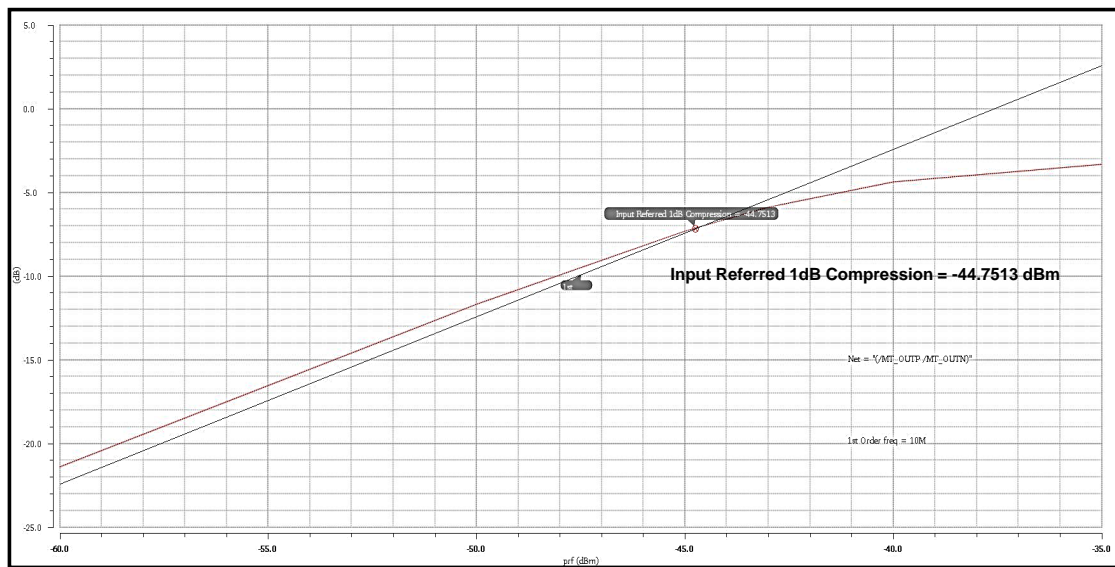


Figure A-10: Simulation results of the LNA + mixer - 1 dB compression point.

Bonding diagram, chip pinout and measurement setup

B-1 Bonding diagram

Figure B-1 shows the bonding diagram of the chip with QFN40 package. Ground connections of analog circuitry are connected to the metal layer underneath the package through down-bonds. It minimizes the impedance seen at the internal ground node and improves the connectivity. B-1 lists the pin-out configuration of the DIFDEM chip.

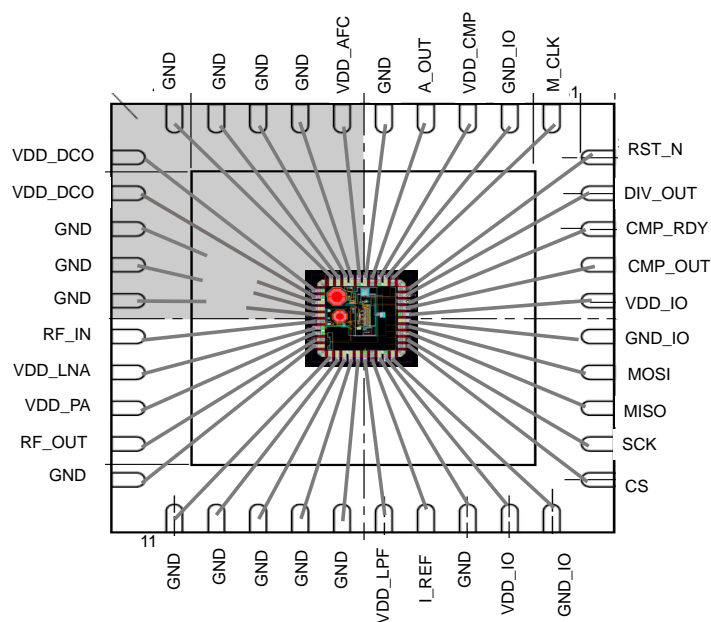


Figure B-1: Bonding diagram of the DIFDEM IC.

Table B-1: Chip pinout of the DIFDEM IC.

Pin number	Name	Description
1	VDD_DCO	0.85V DCO supply
2	VDD_DCO	0.85V DCO supply
3	GND_RF	LNA and mixer ground
4	GND_RF	LNA and mixer ground
5	GND_RF	LNA and mixer ground
6	RF_IN	RF input to the LNA
7	VDD_LNA	0.85V LNA supply
8	VDD_PA	0.85V PA supply
9	RF_OUT	DCO output
10	GND	Ground
11	GND	Ground
12	GND	Ground
13	GND	Ground
14	GND	Ground
15	GND	Ground
16	VDD_LPF	0.85V LPF supply
17	I_REF	Reference input current to the biasing circuit
18	GND	Ground
19	VDD_IO	0.85V Digital supply
20	GND_IO	Digital ground
21	CS	SPI chip select
22	SCK	SPI clock
23	MISO	SPI master-in slave-out control
24	MOSI	SPI master-out slave-in control
25	GND_IO	Digital ground
26	VDD_IO	0.85V Digital supply
27	CMP_OUT	Comparator output
28	CMP_RDY	Comparator ready signal to select rise/fall edge for comparator clock
29	DIV_OUT	1/2 MHz clock output derived from master clock
30	RST_IN	Asynchronous reset active low
31	M_CLK	Master clock 32 MHz reference
32	GND_IO	Digital ground
33	VDD_CMP	0.85V comparator supply
34	A_OUT	Analog output port to read out LPF output
35	GND	Ground
36	VDD_AFC	0.85V AFC supply
37	GND	Ground
38	GND	Ground
39	GND	Ground
40	GND	Ground

B-2 Measurement setup

The photograph of the printed circuit board used for the measurement is shown in Figure B-2. External signal generator is used to supply the RF input and the master clock to the DIFDEM chip through SMA connectors. An impedance matching network is inserted between RF input in the PCB and RF port in the DIFDEM chip to provide desired matching and voltage gain. The buffered LPF output is read out using a separate SMA connector. Further, the level-shifted digital output of the chip can be stored in internal RAM of FPGA/logical analyser for further processing.

Teensy micro-controller and FPGA (not in the picture) are used to read/write the SPI interface registers of the DIFDEM chip. A graphic user interface (GUI), shown in Figure B-3 is developed using PythonQt to control the micro-controller and eventually chip.

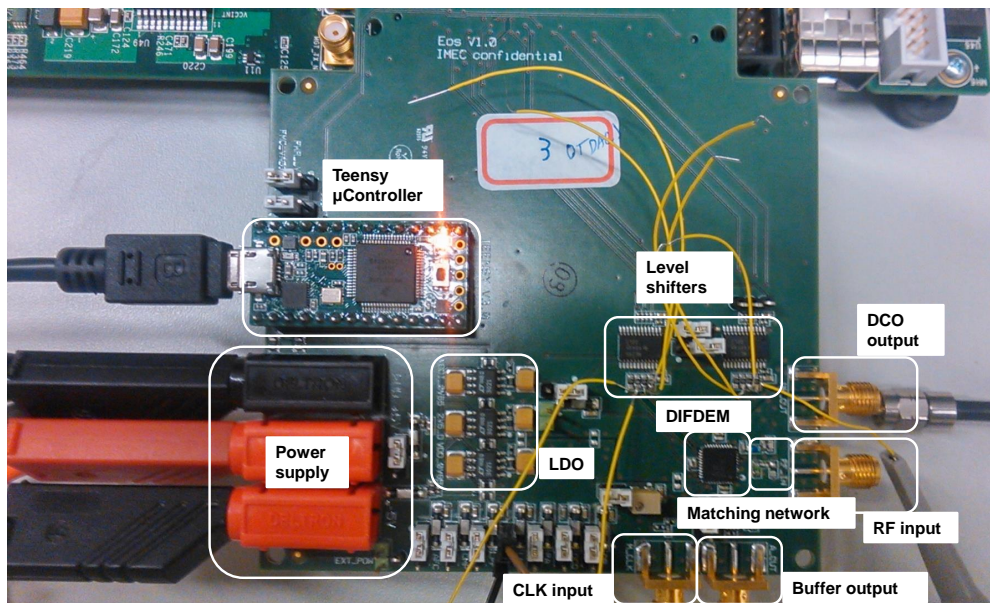


Figure B-2: Photograph of the test PCB.

The screenshot shows the DIFDEM GUI V1.0 - 0907.cfg window. The main content is a table of registers with columns for address, register name, parameter, and bit fields (B7 to B0). The table lists various registers such as DFE_REG0 through DFE_REG6, each with its corresponding bit settings and a comment describing its function.

ADDR	REG	PARAM	B7	B6	B5	B4	B3	B2	B1	B0	WR	RD	COMMENT
000000	DFE_REG0	ACQ_2_0						1	0	0	00000004	00000004	Acquisition bank - 1
		PVT				1	1	0	1	1	0000001B	0000001B	PVT bank
000001	DFE_REG1	TRACK_4_0				0	0	0	0	1	00000001	00000001	Tracking bank -1
		ACQ_5_3						0	0	0	00000000	00000000	Acquisition bank - 2
000002	DFE_REG2	TRACK_11_5	1	1	1	0	1	0	0	0	00000074	00000074	Tracking bank -2
		TRB									00000001	00000001	trb control
		DCOA_EN									00000000	00000000	dco amplitude cal enable
		DUCYCAL_EN									00000000	00000000	duty cycle cal enable
		DCO_BUF_EN									00000001	00000001	dco buffer enable
000003	DFE_REG3	LOBUF2_EN									00000001	00000001	lobuffer2-enable
		LOBUF_EN									00000001	00000001	lobuffer_enable
		DCO_EN									00000001	00000001	DCO_enable
		PA_EN									00000001	00000001	PA_enable
000004	DFE_REG4	DCO_R	1	0	1	0	1	1	0	0	00000056	00000056	DCO bias control
000005	DFE_REG5	DCO_BUF_SEL	1	0	0	1	1	1	1	1	00000027	00000027	DCO buffer selection
000006	DFE_REG6	PA_CTRL					1	1	1	1	0000000F	0000000F	PA control
		DCOA_CTL_H					1	0	0	1	00000009	00000009	DCO amplitude control

At the bottom of the GUI, there are buttons for 'Write All', 'Write', 'Read', 'Diff', and 'Copy'. A 'Filter' input field and a checked 'Advanced Mode' checkbox are also visible. The footer includes logos for Holst Centre and imec.

Figure B-3: Snapshot of the GUI developed for measurement.

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Glossary

List of Acronyms

ACR	adjacent channel rejection ratio
ADC	analog-to-digital converter
AFC	automatic frequency noise cancellation
BAN	body area network
BER	Bit error rate
BLE	<i>Bluetooth Low Energy</i>
DBB	digital baseband
CMFB	common-mode feedback
DAC	digital-to-analog converter
DIFDEM	direct frequency demodulator
DCO	digitally controlled oscillator
ELPF	elliptic low pass filter
FIR	finite impulse response
FT	Fleischer-Tow
FCW	frequency control word
FSK	frequency shift keying
GBW	unity gain-bandwidth
GFSK	Gaussian frequency shift-keying
HS-OQPSK	half-sinusoid offset quadrature phase shift-keying

IIR	infinite impulse response
IoT	internet-of-things
ISM	industrial, scientific and medical
LMV	LNA, mixer and quadrature-VCO
LNA	low noise amplifier
LPF	low pass filter
LO	local oscillator
PAN	personal area network
PDC	phase-to-digital conversion
PLL	phase locked loop
PSK	phase shift keying
PVT	process,voltage and temperature
RF	radio frequency
SRR	short-range radios
SNR	signal-to-noise ratio
SPI	serial-to-parallel interface
TIA	transimpedance amplifier
ULP	ultra-low power
VCO	voltage controlled oscillator
WSN	wireless sensor network
ZIFZCD	zero-IF zero-crossing demodulator