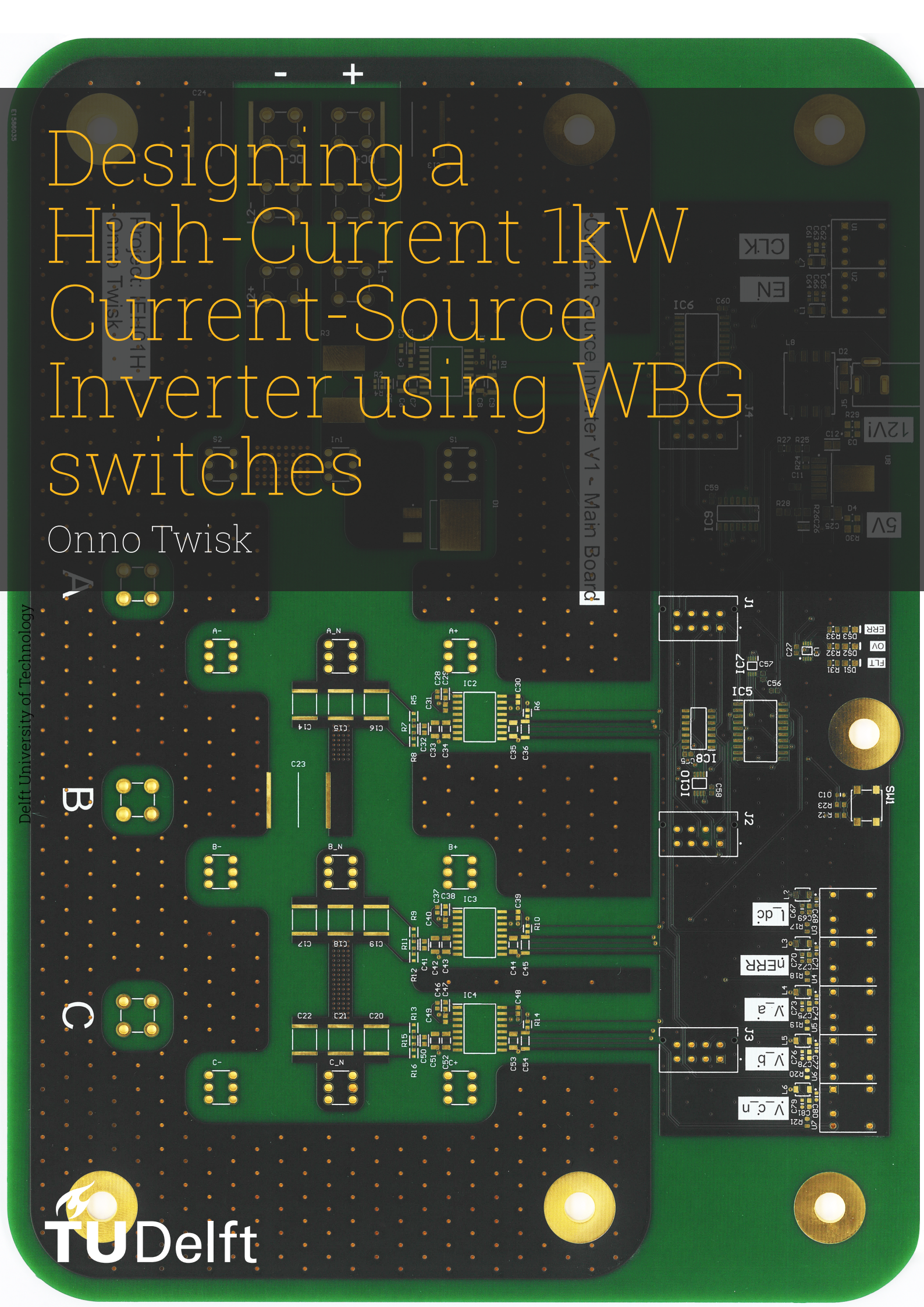

Designing a High-Current 1kW Current-Source Inverter using WBG switches
Onno Twisk
Delft University of Technology
TU Delft

Designing a High-Current 1kW Current-Source Inverter using WBG switches

by

Onno Twisk

to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on Monday November 4, 2024 at 12:30 PM.

Student number:	4718968	
Project duration:	September 4, 2023 – November 4, 2024	
Thesis committee:	Dr. J. Dong,	TU Delft, supervisor
	Dr. Z. Qin,	TU Delft
	Dr. M. G. Niasar,	TU Delft

An electronic version of this thesis is available at `http://repository.tudelft.nl/`.

TU Delft

Abstract

Due to recent developments in current-soruce inverter technology the topology becomes more attractive for use in electric aircraft. However recent studies have shown that electric aircraft are unlikely to be able to operate at high voltages due to the insulation derating, meaning that higher current solutions should be evaluated. In this paper a design is presented that is intended to operate at high currents and lower voltage in order to investigate what influence this shift in operating point has on the functionalit of the inverter. Different design elements are discussed and motivated, including the topology, component selection, and current control methods. After validating the functionality through experimentation the discovered issues are explained and discussed. The design will be shown to be functional, although some of these issues do limit its performance.

Preface

This thesis marks the end of my master program at the Delft University of Technology. In my period here I learned and developed more than I could have imagined when I started my bachelor. The university taught me to think critically and acadmically. My student association Sint-Jansbrug helped me develop social skills and many friendships. My time developing a race car at Formula Student Team Delft is where I developed a passion for power electronics, and what it really means to work in a team.

I do not believe any student will argue that getting a masters degree in Electrical Engineering here is easy, so I would love to thank the people that made it easier.

- Dr. Jianning Dong
  As a neurodivergent person, I had a lot of anxiety surrounding the master thesis project. For a project of this scale, planning and motivation are non-trivial tasks for anyone, especially when it does not align with my interests and curiosity. Jianning helped me by effectively tailoring this project to suit my interests, and accomodated my every need throughout. For that I cannot thank you enough.
- MSc Jundong Wang
  My thesis falls under Jundong's PhD thesis, and I would not have it any other way. Not only was he always prepared to help out with whatever problems I was facing that day, he also looked out for me and my mental health whenever I was pushing too hard. I could always count on him.
- Dr. Bart Roodenburg
  Especially during the manufacturing and assembly phases of my design, Bart and his practical design insights were an invaluable resource. I must have sent him dosens of messages, discussing manufacturing processes and ordering components.

I would like to thank Manon, who has cared for and supported me even when I did not know I needed it.
I would like to thank my parents, Henk and Laura, that always provided love, assistance and advice.
I would like to thank my brothers, Lucas and Maarten, whom I have always looked up to and always pushed me forward

Onno Twisk
Delft, October 2024

Contents

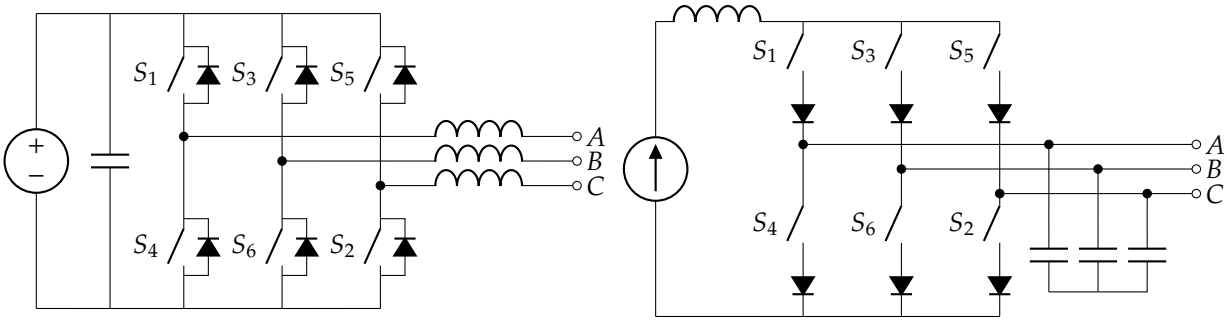
Nomenclature

Abbreviations

Abbreviation	Definition
BD	BiDirectional
CSI	Current Source Inverter
DPT	Double Puse Test
EMI	ElectroMagnetic Inteference
FET	Field Effect Transistor
FOC	Field Oriented Control
GaN	Gallium-Nitride
HEMT	High-Electron-Mobility-Transistor
IMMD	Integrated Modular Motor Drive
RB	Reveres Blocking
SiC	Silicon-Carbide
SVPWM	Space Vector Pulse Width Modulation
VSI	Voltage Source Inverter
WBG	Wide-BandGap

1 Introduction

When looking at inverters throughout history, the preferred or dominant topologies have been changing constantly. This change comes both from the development in semiconductors that make up these topologies and from wider application of power inverters in different industries. In recent times the most common type of inverter would be some form of a Voltage Source Inverter (VSI), which would consist of an array of switches closing and opening the input DC voltage to the output. This input DC voltage would be held stable by DC link capacitors.



(a) Voltage Source Inverter (VSI)

(b) Current Source Inverter (CSI)

Figure 1.1: Different core inverter concepts CSI and VSI.

There exists a different version that works similar yet opposite, the Current Source Inverter (CSI). This inverter works in the same manner except has a constant DC voltage at its input, held stable by a DC link inductor. This poses some extra requirements on the switches, as they would need to be Reverse Blocking (RB). This would restrict the possible switch choice to ones that only work at low switching frequencies, making it only really suitable for grid applications. It is possible to use no single switch, but have faster switches like IGBT or FET's in series with a diode to provide the RB. This helps increase the switching frequency to the level of VSI, but at an efficiency penalty from the diodes forward voltage.

This efficiency penalty can be reduced massively by replacing that diode with another switch in anti-series. This increases the switch count and thus also the complexity of the inverter. There also exist an unconventional type of switch in the form of a monolithic bidirectional GaN transistor that has BD capabilities without performance penalties[1], which could be used in future designs once the technology has matured. But CSI's have also been shown to have many other advantages.

ElectroMagnetic Interference (EMI) Especially when using Wide BandGap (WBG) switches (which have rise and fall times in the nanoseconds) EMI is an import consideration, as high quantities of EMI can cause various problems, like signal integrity issues, ground leakage current and even bearing failures[2]. Compared to VSI, the CSI produces less EMI [3, 4, 5].

dv/dt issues Those WBG rise and fall times when applied in a VSI cause a high change in voltage on the output. These abrupt voltage changes have been shown to cause unneccesary stresses on components, most famously the motors themselves [6].

Fault tolerance While both CSI and VSI have ways in which it can fail quite spectacularly, the way they fail and the consequences of the failure could not differ more. A CSI is plagued by over-voltage failures when the DC link current loop is broken, which can cause the switches to break if no protection is implemented. When a VSI fails it is due to over-current failures, which occur after the DC link capacitor is shorted. This can cause both the switches in the loop to break, but in some cases the current can also short through the motor. In this case the current can actually demagnetise the motor[7].

DC-link reliability As discussed above, a VSI requires DC link capacitors to function. The problem is that capacitors have been shown to be a major reliability concern[8]. As inductors seem to be much more predictable in their reliability, for safety critical designs the CSI is preferable [9].

1.1. Application Context

One field where CSI could be particularly beneficial would be electric aircraft. The loss in efficiency is easily offset by the decreased EMI, Increased fault tolerance and lower size and mass, as well as the higher temperature capabilities making it easier to cool in compact designs. The only real hiccup is that the maximum input voltage of the inverter is limited by the voltage rating of individual switches. This is particularly bothersome as at high altitudes this voltage rating derates significantly[10]. This might be fixed by making an Integrated Modular Motor Drive (IMMD) and wiring the converters in series. Further research required.

As electric aircraft motors tend to be, you know, expensive, this design will focus on the nearest scaled version of this in the form of a drone motor. The motor used is the MN501-KV240, as its parameters have been extracted previously [11]. The motor is pictured in Figure 1.2, and its parameters are listed in Table 1.1.

Table 1.1: Motor Parameters for the Tmotor MN501-KV240[11]

MN501-KV240			
Parameter	Symbol	Value	Unit
Phase Resistance	R_s	42.5	mΩ
Phase Inductance	L_s	11.29	µH
Pole Pairs	p	14	
Back-Emf Constant	k_e	0.0398	$\mathrm{V\,rad^{-1}\,s}$
Speed	n_{rpm}	20.000	rpm

Figure 1.2: The MN501-KV240 motor

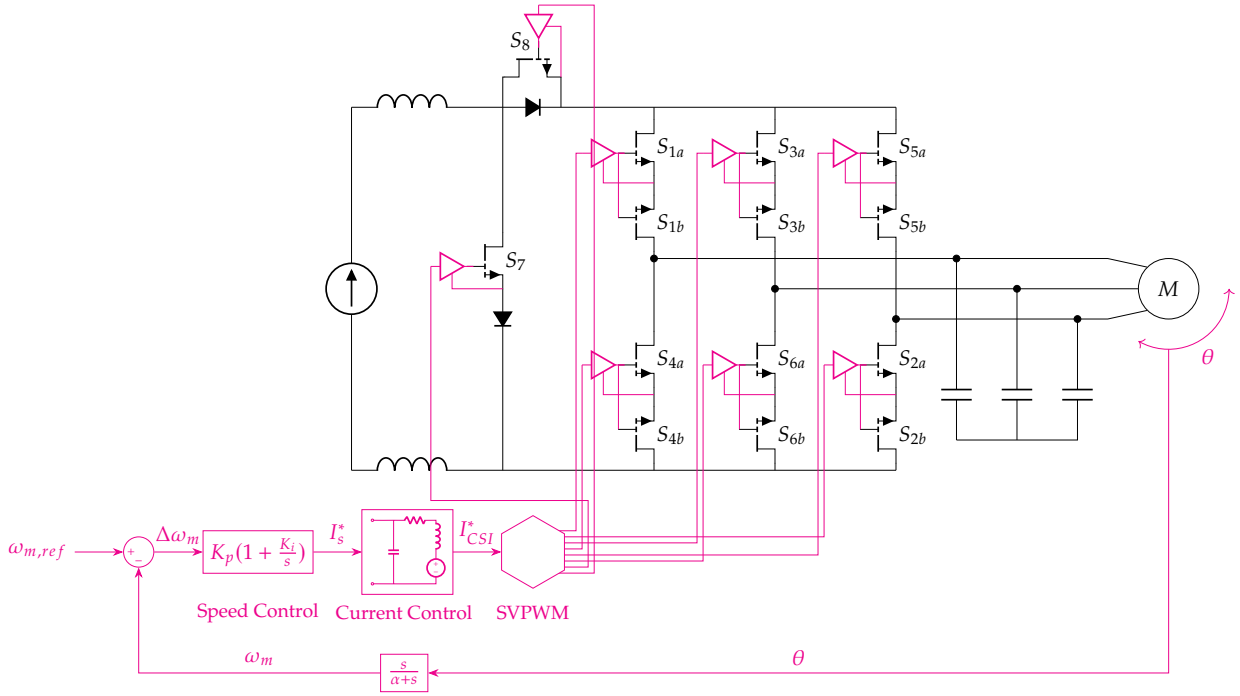


Figure 1.3: CSI system overview

1.2. Design Goals & Methodology

Due to the voltage limitations the system will be running at higher currents to match the desired output power. Usually higher voltage is preferred as higher currents will require larger (and thus heavier cables) in the vehicle. As this is the road less travelled, the goal of this thesis is to design a 1kW CSI that can be used in a laboratory setting to see what issues come up when voltage is limited.

1.2.1. Analysis

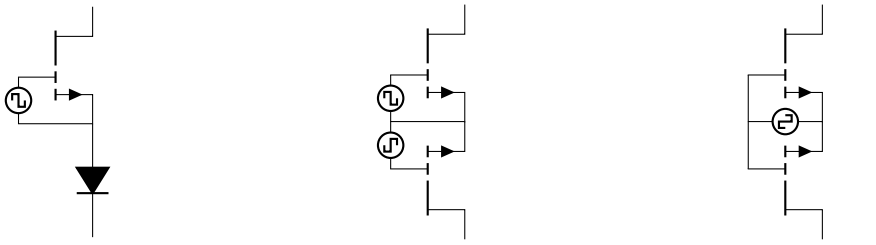
Many of the requirements for the inverter are derived from the motor it drives, their parameters shown in Table 1.1. From these requirements the system shown in Figure 1.3 is built in MATLAB and Simulink. The important design choices in this stage mainly concern the topology, the value for the output capacitor and the evaluation of speed and current control methods, discussed in Chapters 2 to 4 respectively.

1.2.2. Design and Implementation

For component selection a different simulation tool is used, LTspice, as it is better suited for transient responses and individual component analyses and modelling. This is discussed in Chapter 3. The model was also useful to evaluate what kinds of protection circuits are necessary and which ones perform the best, also shown in Chapter 3.
From this point the schematic and PCB design is done using Altium designer.

2

CSI motor drive topology and modulation



(a) Switch + Diode
RB Switch

(b) Switch + Switch
Single Gate BD switch

(c) Switch + Switch
Dual Gate BD switch

Figure 2.1: Three possible switch types in CSI topologies

2.1. Switches

As mentioned in the introduction, current-source converters have some exotic switch requirements. It needs to facilitate Reverse Blocking (RB), as it would otherwise allow for the output capacitors (shown in Figure 1.1b) to be shorted through the switches. This requirement can be solved in a few different ways. The original way to deal with this was to use a Gate Turn-Off Thyristor, or GTO [12]. These switches traditionally had a maximum switching frequency of about 1kHz due to the relatively high turn-off time, making it unsuitable for usage in high power density applications.
With IBGT and MOSFET technology maturing the GTO was replaced. However, neither of the new switches were capable of blocking reverse voltages effectively. To remedy this they were placed in series with a diode to form a hybrid RB switch, pictured in Figure 2.1a. As discussed previously, this introduces a significant conduction loss compared to the VSI equivalent. The next improvement on this issues is the bidirectional (BD) switch. Placing 2 transistors in anti-series allows for conduction and blocking in both direction, reducing the conduction losses significantly (but still being twice that of a VSI). This switch also brings added complexity. Figure 2.1c features the form that works with the basic H6 topology, shown in Figure 2.2. As this switch does not provide RB when both switches are open, the commutation procedure requires first the top switch to close before the bottom switch, using the bottom switch as a diode. This means both switches need to be driven separately. For topologies where this is not required (which will be discussed in Section 2.2), a third variant is available with only one gate signal. This switch pictured in Figure 2.1b is likely to be the most beneficial, as it has the lower conduction loss that comes with the BD design while minimising on the required driving signals.

As a clarification, for all symbols in this paper that represent a transistor the symbol for galliumn nitride high-electron-mobility transistors (GaN-HEMT) are used. This does not insinuate that each of these switches must be GaN-HEMT, but in the final design this type of switch is used and to simplify

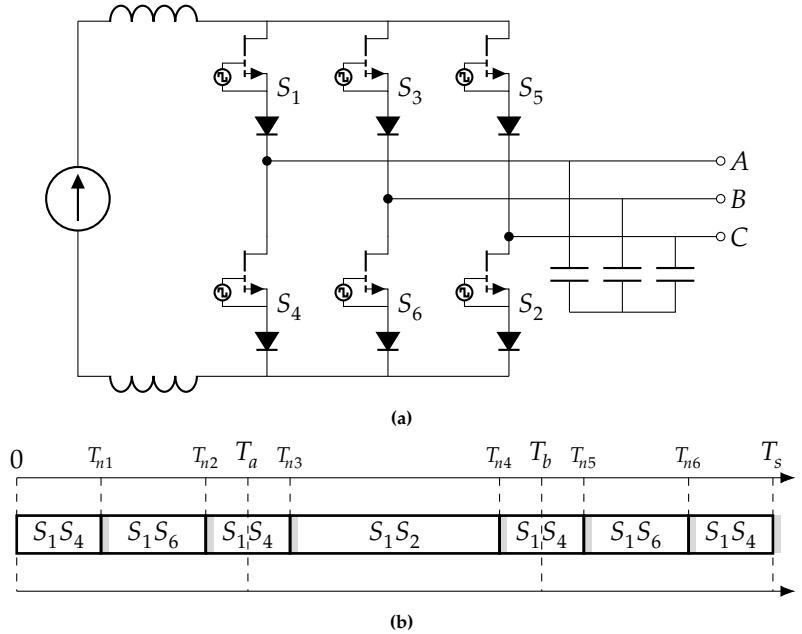


Figure 2.2: CSI H6 topology using hybrid RB switches

the rest of the figures this symbol was used everywhere.

2.2. Topology

In this section the topologies H6, H7 and H8 will be discussed. These are chosen as moving from one to the other creates an intuitive sense of how each new topology reinforces a shortcoming of the one before. There do exist topologies that could prove to be even more advantageous than the ones listed here, but as this thesis is an initial voyage into the current-source converter world the performance of the listed topologies is deemed to be adequate. Especially as the higher performing CSI topologies tend to be significantly more complex, whereas the H8 topology is only a little more complicated. The main metric for complexity used in this comparison will be number of gate signals required. This is because higher number of (independent) gate signals will always be more complicated to drive, and in cases where all are required to function without fault a higher number also indicate a lower reliability. Below each

2.2.1. H6

The H6 topology is what would typically be referred to as a "classic" CSI. Especially the variant shown in Figure 2.2. As mentioned in Section 2.1, the use of hybrid RB switches in this topology causes a major efficiency penalty due to the increased conduction losses due to the diodes forward voltage. The variant using the BD switches from Figure 2.1c is shown in Figure 2.3. Compared to the RB variant this one has much lower conduction losses (while still more than VSI).
However this one now poses a new challenge: Due to the fact that both switches need to be controlled independently to provide reverse blocking during commutation, this topology requires a grand total of 12 separate driving signals. Due to the increased complexity of this variant often the RB variant is preferred as it only requires six different signals.

Section 2.2 shows the modulation scheme for the RB variant, and the BD variants is shown in Figure 2.3b. In these figures the gray area after each transition indicates overlap

2.2.2. H7

Pictured in Figure 2.4, the H7 topology incorporates a seventh switch S_7 that short the DC link inductor, as well as a diode D_8 that prevents current from flowing from the switching legs through S_7. This allows for the switches to commutate with deadtime instead of overlap as the DC link current is shorted through S_7 during commutation. Using dead-time then means that the switches no longer require

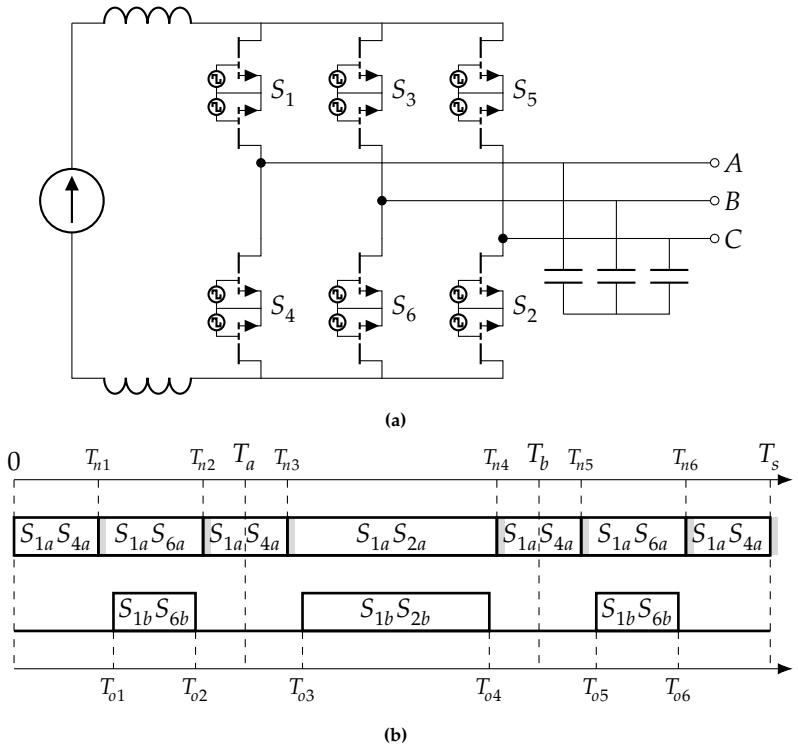


Figure 2.3: CSI H6 topology using dual gate BD switches

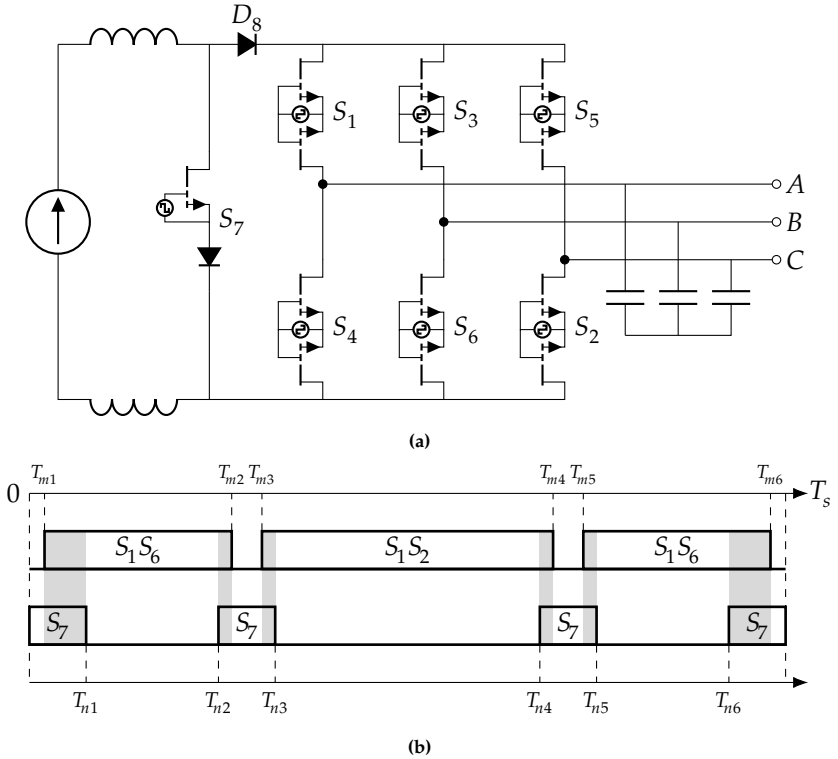


Figure 2.4: CSI H7 topology using single gate BD switches

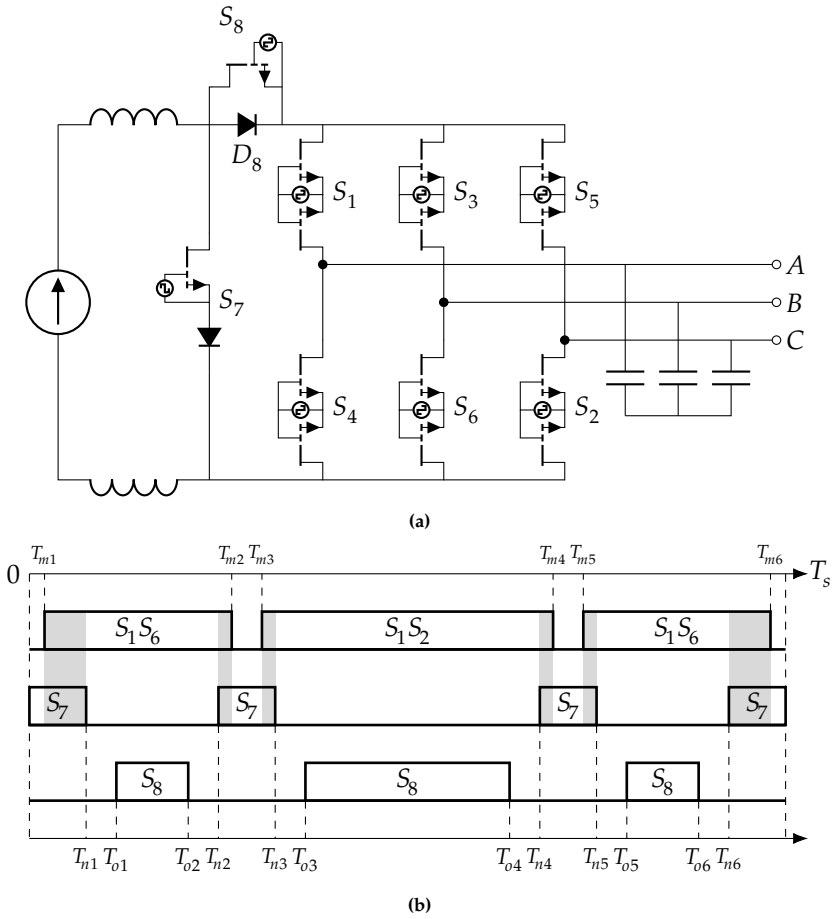
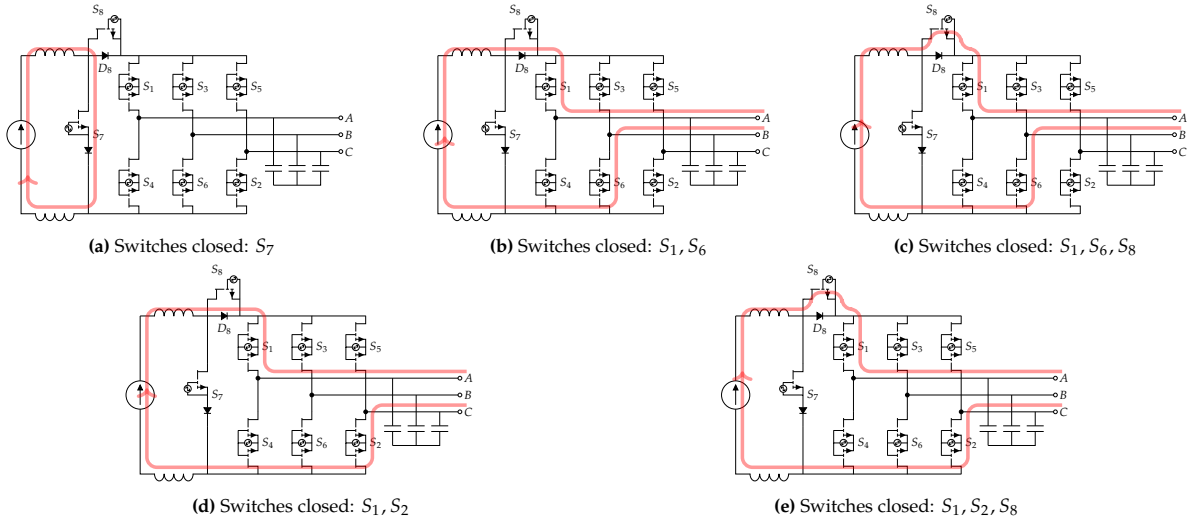


Figure 2.5: CSI H8 topology using single gate BD switches



(a) Switches closed: S_7 **(b)** Switches closed: S_1, S_6 **(c)** Switches closed: S_1, S_6, S_8

(d) Switches closed: S_1, S_2 **(e)** Switches closed: S_1, S_2, S_8

Figure 2.6: All states during one switching period

explicit RB during commutation which then allows for the use of single gate BD switches. Compared to the BD variant of H6, the use of BD switches decrease conduction losses. Furthermore the single gate BD switch means that the complexity is only increased slightly as the number of required signals goes from six to seven.
A consequence of this reduction of complexity is that the inclusion of D_8 is necessary, as otherwise the output capacitors would be shorted through S_7 when it closes. D_8, being a diode, again increases conduction losses significantly. Granted it would not be as much as the RB variant of H6, but it would be preferred to have the efficiency of BD H6 with the simplicity of H7.

For the H7 the modulation strategy is shown in Figure 2.4b. Here it is shown that S_7 is engaged during commutation. The gray areas in this figure represent the overlap of the other switches with S_7. Note that as the other switches only switch once S_7 is closed, S_7 is the only switch experiencing any kind of switching losses.

2.2.3. H8

This section will be kept a little brief as the H8 topology is the one picked for this project, and will be discussed in depth. Compared to the H7, the change is subtle. The circuit is completely identical, except for the inclusion of switch S_8, which is positioned in anti-parallel to D_8. This has the function that while S_8 is not driven (open) the circuit has the same function as H7, but after commutation S_8 closes to allow a low resistance path for the current that would otherwise travel through D_8. Right before commutation S_8 opens once again to make sure the output capacitors are not shorted once S_7 closes. Effectively S_8 is complementary to S_7 with dead-time.

The H8 modulation strategy is similar to H7, and can be seen in Figure 2.4b. The addition of S_8 is shown to be on between commutations, with a deadtime between it and S_7. The states during one switching period are illustrated in Figure 2.6.

2.3. Space Vector Modulation

Conceptually, SVPWM for CSI is similar to VSI. The voltages or currents are switches such that the average on or through each phase is approximately the reference voltage/current. Methodically though they differ significantly. The most fundamental difference comes from the fact that in a VSI every leg is independently generating a voltage to match the reference. The function of reaching a reference voltage is achieved by having either the top switch or the bottom switch on for a specific period at any given time (except during commutation). This averages then out to this reference voltage. Modulating current is different as there always need to be one leg that supplies current and one that sinks current. This difference results in a SVPWM scheme that is simpler in its implementation as only three switches are

actually switched in any sector.
Figure 2.7 pictures the space vector diagram for the CSI. In Sector 1 the current will flow from Phase A into Phase B and Phase C. To achieve this S_1 is kept on permanently, and S_6 and S_2 are used to reach $\vec{I_1}$ and $\vec{I_2}$ respectively, alternating between the two to reach the right angle for the reference current. To reach the right amplitude a zero vector is required. For this there are 2 options depending on the topology. H6 can use S_4 to short the current back into Phase A. H7 and H8 can both use S_7 as the zero vector as it shorts the DC link current. Using S_7 has the added benefit that it is already used during commutation. To calculate the right timings the following equations are used[13]:

$$m_a = \frac{I_{ref}}{I_d} \tag{2.1}$$

$$T_1 = m_a \cdot \sin\left(\frac{\pi}{6} - \left(\theta - \frac{(k-1)\pi}{3}\right)\right) \cdot T_s \tag{2.2}$$

$$T_2 = m_a \cdot \sin\left(\frac{\pi}{6} + \left(\theta - \frac{(k-1)\pi}{3}\right)\right) \cdot T_s \tag{2.3}$$

$$T_0 = T_s - T_1 - T_2 \tag{2.4}$$

$$T_a = \frac{T_1}{2} + \frac{3}{8}T_0 \tag{2.5}$$

$$T_b = T_a + T_2 + \frac{1}{4}T_0T_{n1} \qquad = \frac{1}{4}T_0 \tag{2.6}$$

$$T_{n2} = T_a - \frac{1}{8}T_0 \tag{2.7}$$

$$T_{n3} = T_a + \frac{1}{8}T_0 \tag{2.8}$$

$$T_{n4} = T_b - \frac{1}{8}T_0 \tag{2.9}$$

$$T_{n5} = T_b + \frac{1}{8}T_0 \tag{2.10}$$

$$T_{n6} = T_s - \frac{1}{4}T_0. \tag{2.11}$$

Here T_1 and T_2 represent the time S_6 and S_2 spent on during one switching period. T_0 is the zero vector time, k represents the sector number and θ is the angle. The values correspond with the the diagram in Figure 2.5b. The values for T_o and T_n are computed simply by adding dead time and overlap to T_n.

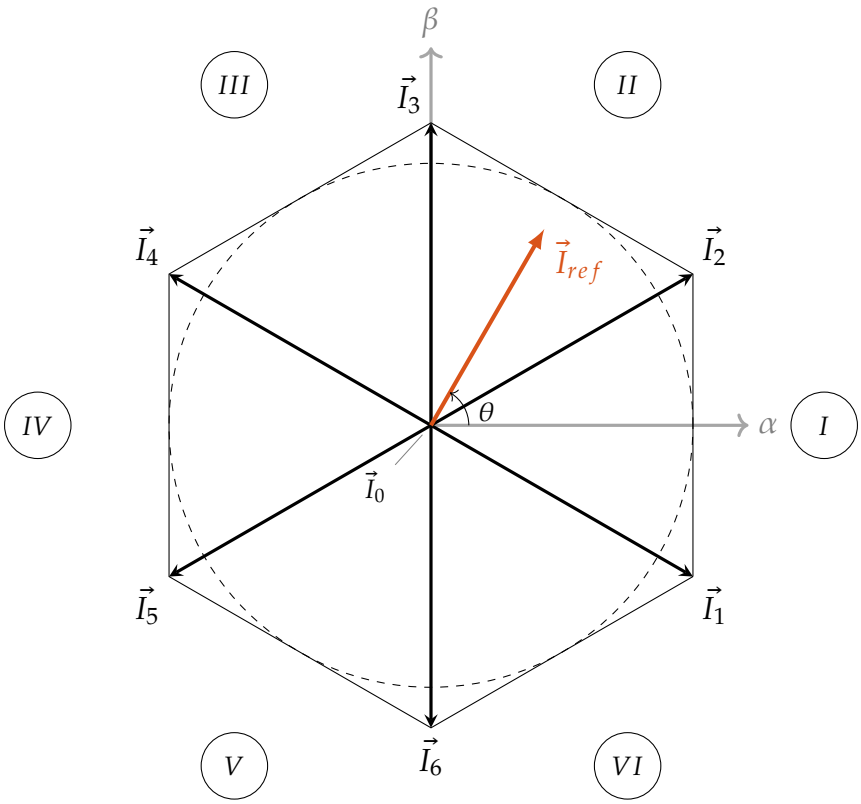


Figure 2.7: CSI Space Vector Modulation

3

Design of H8 CSI based motor drive

As this design is a first foray into CSI driven motor control, the most important aspact in this design is keep the design simple and measureable, while still allowing for testing and measuring of advanced techniques. In this chapter first the critical components are introduced. Later the critical subcircuits are laid out and explained. Then the microcontroller platform is introduced, while explaining how the control system functions. In Table 3.1 the requirements for the CSI are introduced. It's values are derived from either the motor specifications (Table 1.1,[11]) or based on what is required for state of the art motor control.

Table 3.1: CSI requirements

CSI operating parameters			
Parameter	Symbol	Value	Unit
DC Voltage	V_{DC}	50	V
DC Current	I_{DC}	30	A
Switching Frequency	f_{sw}	100	kHz
Fundamental Frequency	f_1	4.6	kHz

3.1. Component Selection

3.1.1. Switch

For the switch first the technology is selected. For our switch it would be great if the on-state drain-source resistance ($R_{DS(on)}$) is as low as possible. This is even more important for this design than a conventional inverter as the switches are in anti-series thus doubling conduction losses, and due to the derating issue[10] the inverter will be run at a higher current. The second important feature is the switching loss. Power density is crucial when designing anything for aerospace applications, and increasing switching frequency (and thus switching losses) decreases passive component size and weight.
These requirements combined with the relaxation that for the initial prototype input voltage will be limited, point towards using Gallium-Nitride (GaN) switches. GaN technology features low on resistance and high switching capabilities. Their downsides are few, but the biggest is that switches generally do not feature a high voltage rating. If this would be required Silicon Carbide (SiC) would be preferred. These switches come with a higher voltage rating at the cost of lower switching frequencies, higher switching energy and higher $R_{DS(on)}$[14].

Having selected the technology the next step is to find a switch with a suitable voltage and current rating in convenient packaging. The selected switch is the GS61008T, pictured in Figure 3.1. Apart from the adequate voltage and current ratings, this switch is particularily convenient due to the top mounted cooling that allows for simpler PCBs for cheaper prototyping and the symmetrical package is

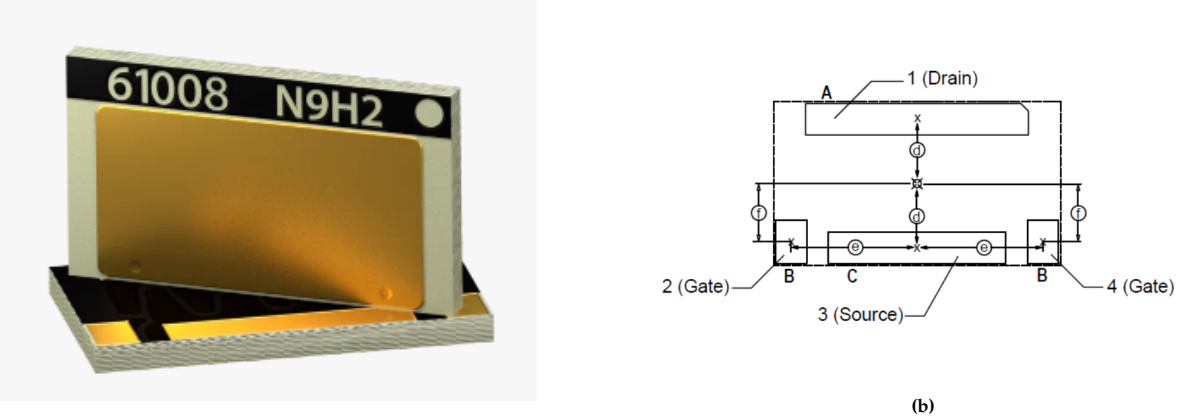


Figure 3.1: GS61008T GaN HEMT and footprint [15]

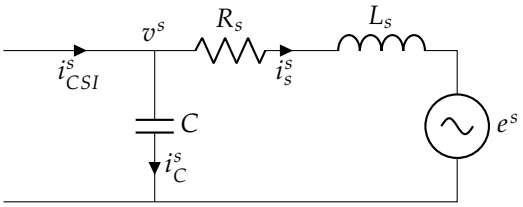


Figure 3.2: CSI equivalent circuit in stationary reference frame

ideal when wiring 2 switches in anti-series. The package is shown in Section 3.1.1. The gate is accessible on a pin from both sides.

3.1.2. Filter Capacitor

When driving current through an inductor (or a RL circuit), generally voltage is used as the input as current already is what needs to be controlled. If current is forced directly through an inductor there will be a huge voltage overshoot (depending on the $\frac{di}{dt}$). It is analogous to applying voltage directly on a capacitor, the inrush current will be massive. A way to mitigate this for the capacitor is that an inductor is put in series with the capacitor to resist the rate of change of the current. In the driving inductor scenario the equal circuit is to put a capacitor in parallel with the RL circuit. This dampens the voltage increase, and also gives a high frequency path for the current so the actual motor windings receive only the fundamental frequency.

Analysing the equivalent circuit with added filter capacitors, the transfer function becomes

$$Z_C(s) = \frac{1}{sC} \tag{3.1}$$

$$Z_{R_s,L_s}(s) = R_s + sL_s \tag{3.2}$$

$$I^s_s(s) = I^s_{CSI}(s)\frac{Z_C(s)}{Z_C(s) + Z_{R_s,L_s}(s)} \tag{3.3}$$

$$G_P(s) = \frac{I^s_s(s)}{I^s_{CSI}(s)} = \frac{\frac{1}{L_sC}}{s^2 + s\frac{R_s}{L_s} + \frac{1}{L_sC}} \tag{3.4}$$

To evaluate how this circuit responds to a change in capacitance, the system is analysed using the motor parameters and the resulting bode plot is shown in Figure 3.3. As can be analytically expected, with a higher capacitance the resonance peak moves to lower frequencies and the peak decreases in magnitude. The sharp peak from the lowest capacitance corresponds a very long settling time. This is

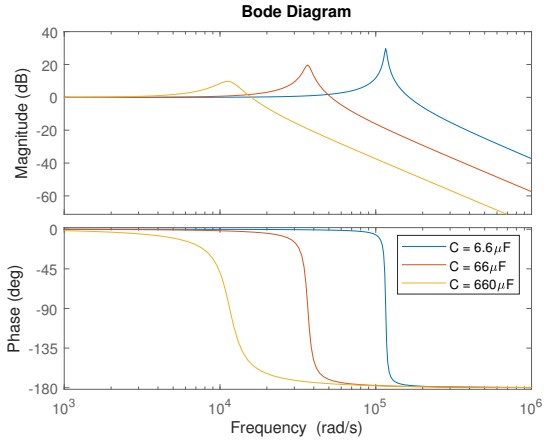


Figure 3.3: Bodeplot for G_P

clearly visible in Figure 3.4. The larger capacitance, while decreasing the ringing, does not help the settling time. The settling time i long as there is little to no damping in the system as that is provided by the phase resistance, which is measured to be only 45mΩ[11]. To get an idea of what is necessary for the system to become critically damped, which would be the fastest response without ringing, first Equation (3.4) is rewritten into the pole-zero format Equation (3.5)

$$G_P(s) = \frac{1}{L_s C} \frac{1}{\left(s + \frac{R_s}{2L_s} + \frac{1}{2}\sqrt{\frac{R_s^2}{L_s^2} - \frac{4}{L_s C}}\right)\left(s + \frac{R_s}{2L_s} - \frac{1}{2}\sqrt{\frac{R_s^2}{L_s^2} - \frac{4}{L_s C}}\right)} \tag{3.5}$$

From this the pole locations can be determined to be

$$P = -\frac{R_s}{2L_s} \pm \frac{1}{2}\sqrt{\frac{R_s^2}{Ls^2} - \frac{4}{L_s C}} \tag{3.6}$$

From this the requirement for a critically damped system can be given by

$$R_s = 2\sqrt{\frac{L_s}{C}} \tag{3.7}$$

From this formula it is determined that for a critically damped circuit the resistance should be increased. This is usually not an enticing prospect as this will directly cause significantly higher conduction losses. Picking a higher capacitance reduces the required resistance, but due to space and cost constraints this is not always viable. For this thesis a middle route is picked. By going for 66μF, the required resistance is only about 0.8Ω, and using a virtual resistance it is possible to achieve critical damping without any extra losses[16]. This ended up being outside of the scope for this project, but parasitic resistance did turn out to be enough for some low power running. This approach and others are discussed in Section 4.2

3.1.3. Gate Driver

Added benefit to the GS1008T switch is the simple gate driving requirements, and the possibility to use the AHV85110. This gate driver is remarkable as it allows for full isolation with incorporated isolated power supply. This results in a simple and compact design that allows for cheap manufacturing, while maintaining performance and isolation requirements in high voltage and high power applications. An example of the entire driver circuit is shown in Figure 3.6. Apart from the IC these components can be imperial size code 0402 so they take barely any space.

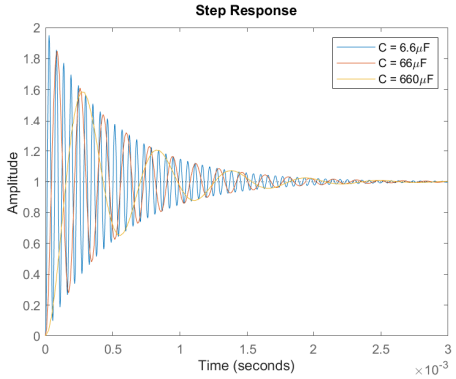


Figure 3.4: Step response for G_P

Figure 3.5: The AHV85110 gate driver[17]

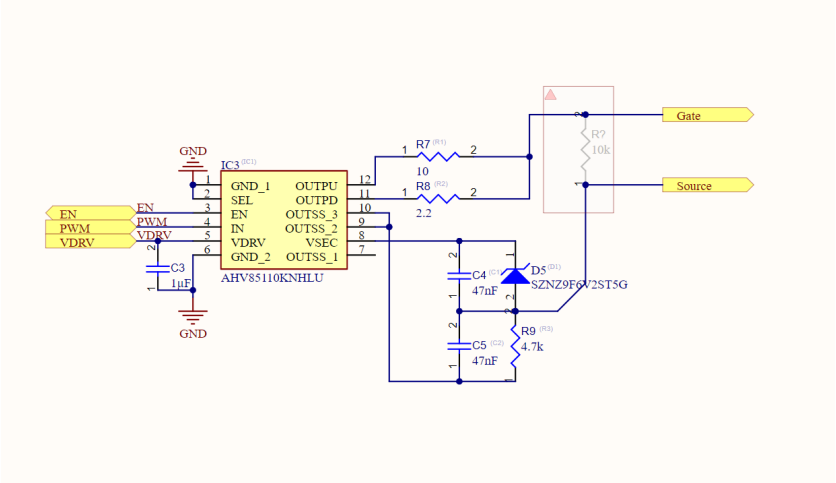


Figure 3.6: AHV85110 driving circuit schematic

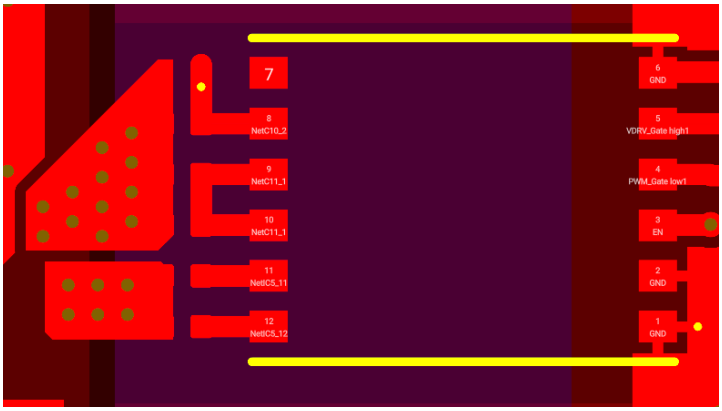


Figure 3.7: AHV85110 Circuit PCB footpring

3.2. Gate Driver

After the choice for the driver is made the circuit is designed, as shown in Figure 3.6. The circuit is adapted form the APEK85110KNH-01-T-MH board by GaN systems, a schematic is shown in [17]. Adaptations to the GS61008T were done by changing the value of C_{SEC}, labeled C4 and C5 in Figure 3.6, to suit the output capacitance of the switch. This circuit allows for the output voltage to be bipolar. In this particular circuit the zener diode limits the positive gate-source voltage to 6.2 volts, and sets the low state voltage to be about -3V. The final PCB layout is shown in Figure 3.7.

The main disadvantage of this circuit (and using this gate driver) is that if the gate driver encounters a fault state the designed safe state is to keep the switch open [17]. This is the logical choice for a VSI but in the case of a CSI it can damage the switches. Due to this effect the overvoltage circuit introduced in Section 3.4.1 is crucial.

3.3. Position Sensing

For any kind of speed control some version of position (or speed) sensing is required. Measuring angle also allows for Field Oriented Control (FOC). In terms of requirements the chosen position sensing method would require a high enough bandwidth to represent the correct position at higher speeds, and the accuracy of the angle estimation should be high enough. The last part is especially important for motor with high pole pair count. The method chosen for this project is to estimate the angle based on using a 2-axis hall effect sensor. This is chosen for 2 primary reasons: Firstly the picked chip (MLX90380) is designed for this specific application and thus values high bandwidth and high accuracy in its design. The second reason is that this concept allows for relatively simple implementation. Compared to an angle encoder based on a encoded disk, axially mounting a magnet to an existing motor that was designed to be used with sensorless control. The solution for axially mounting a magnet involved a simple 3D printed mount, and is shown in Figure 3.8. Later on this solution was shown to have some problems as the response proved to be slightly non-linear. This did not limit the performance of the CSI.

3.4. Protection

As with most power converters, CSI topologies require adequate fault protection. The CSI requires no output shortcircuit protection like a VSI would[7]. In fact the CSI requires a lot of opencircuit protection, as the current from the DC link always needs a path to take. This and other protections will be discussed in this chapter.

3.4.1. Overvoltage

Overvoltage in this design is tackled in 2 ways: prevention and intervention. The prevention part is done by hardware logic circuitry to check whether or not the input signals will cause an open circuit state to occur, and will S_7 closed in such a scenario. Intervention happens when a overvoltage occurs. Every switch has a circuit that both clamps the voltage to keep it from reaching dangerous levels and

Figure 3.8: 3D printed magnet mount

signals the controller that an overvoltage event.

3.4.2. Prevention

To prevent overvoltage, Equation 3.8 must hold always true. In this formula each switch is a logical 1 when it is closed, and a logical 0 when it is open.

$$(S_1 + S_3 + S_5) \cdot (S_4 + S_6 + S_2) + S_7 = 1 \tag{3.8}$$

Open circuit occurs when no high side or no low side switches are closed. If this condition is not met, S7, which in a safe state short the DC input, should not open. This is done by first using 2 OR gates with three inputs, to generate signal SH and SL. These signals are for the high and low side respectively, and are high when a switch is closed and low when all switches are open. Then signals SH and SL are fed into an AND gate to generate signal Signal Closed (SC). Finally this signal is connected to an AND gate with nERR (inverted error) to create signal nDIS, which when high allows S7 to open, and when low keeps it closed, overriding the S7 PWM signal.

3.4.3. Mitigation and detection

In Figure 3.9 the overvoltage circuit is depicted. During normal operation the majority of the voltage is over R_1, until that voltage reaches the breakdown voltage of D_1, in this case 54 V. At that point it starts conducting more and when the voltage rises further the voltage over D_2 rises, causing current to flow through the optocoupler. The optocoupler is a 2 channel one that is wired such that the signal is transmitted when the voltage hits a certain amplitude, regardless of polarity. This in combination with the bidirectional TVS diodes ensures that both switches are protected from overvoltage, and that the bidirectional capabilities of the circuit are preserved.

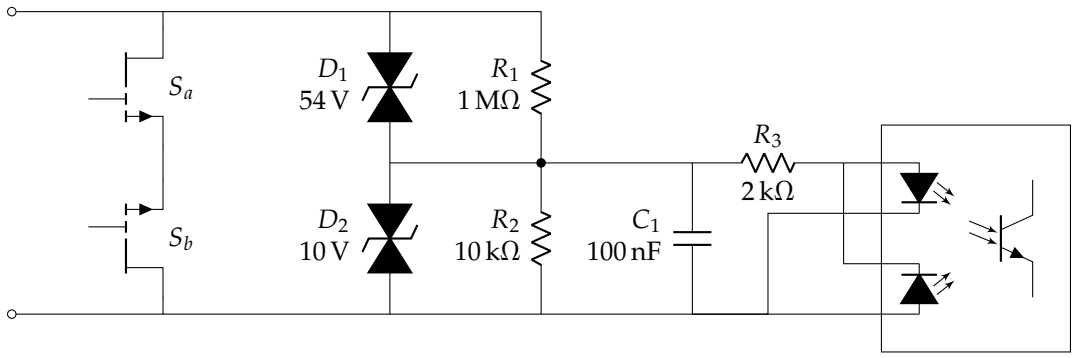


Figure 3.9: An TVS based overvoltage mitigation and detection circuit

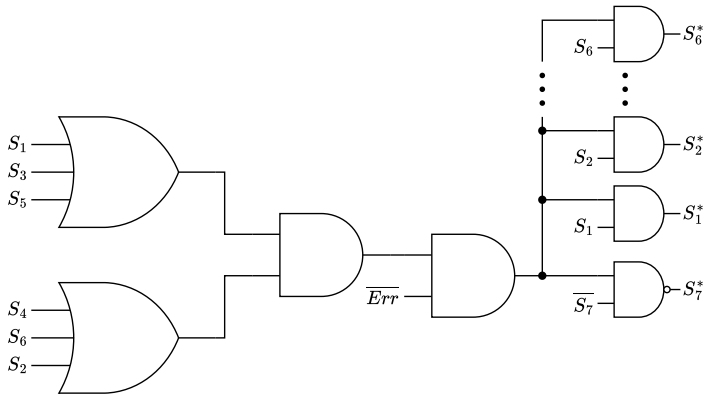


Figure 3.10: Safety logic circuit

3.5. Fault detection

For added safety the most critical devices were selected to include a fault signal. These devices include the gate drivers, output voltage ADC devices and input current sensor. This fault signal was controlled to be of the inverted type, meaning that a fault would be a low state and the all good a high state. This was combined with the enable signal in a wired-AND network. This means that the network has a weak pull up, and all devices on the network that want to drive the signal do so with a open-drain output. So if everything is good the signal is high due to the pull up, but the entire line gets pulled down when one device encounters an error. This method of fault handling was chosen to be able to string many devices together without ending up with a massively complex PCB. The downside of this method is that there is not way to actually find out which device caused the fault. This was mitigated by running 5 seperate fault lines. 1 for each phase leg and its gate drivers, 1 for S_7 and S_8 and their gate drivers, and 1 for the sensors.This meant that each fault line only handled at max 4 devices at the time, and actually also meant that each line handled 1 PCB in my design. This design is presented in Figure 3.11.

3.6. Controller

The DSP used in this design is the TMS320F28379D, on the launchpad evaluation board LAUNCHXL-F28379D. The main reasons for this choice are that it is a popular controller for similar applications, which means that there exist many tools and resources that help with controller design and it can be programmed straight from MATLAB. It features modules for PWM generation that are convenient for inverters. Regrettably this was also what made implementation difficult as the modulation is made specifically with VSI in mind. The PWM is synthesized using a carier wave and a threshold value. The controller allows 2 of these values. This means that the output waveform can switch states 4 times when using a triangle carrier wave. Looking back at Figure 2.5b, S_7 switches output states 6 times. This means that an extra complex solution is required, where the first value is changed mid cycle. An example from the official C2000 documentation [18] is presented in Figure 3.12.

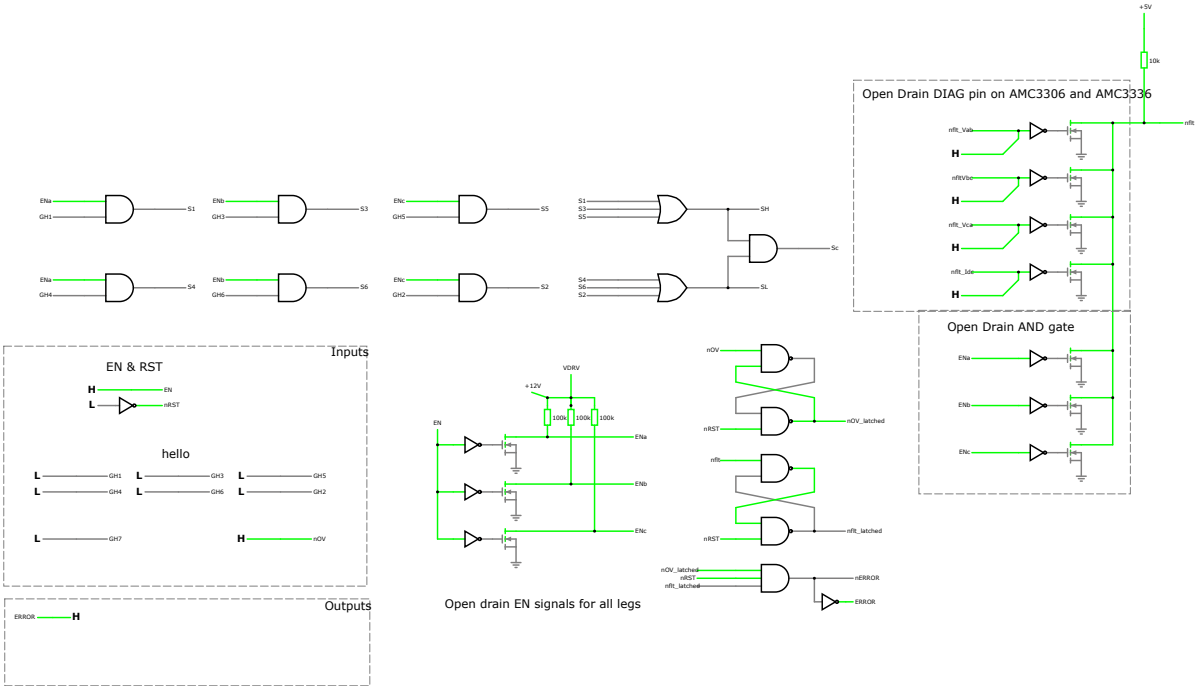


Figure 3.11: Enable and Fault latching circuit

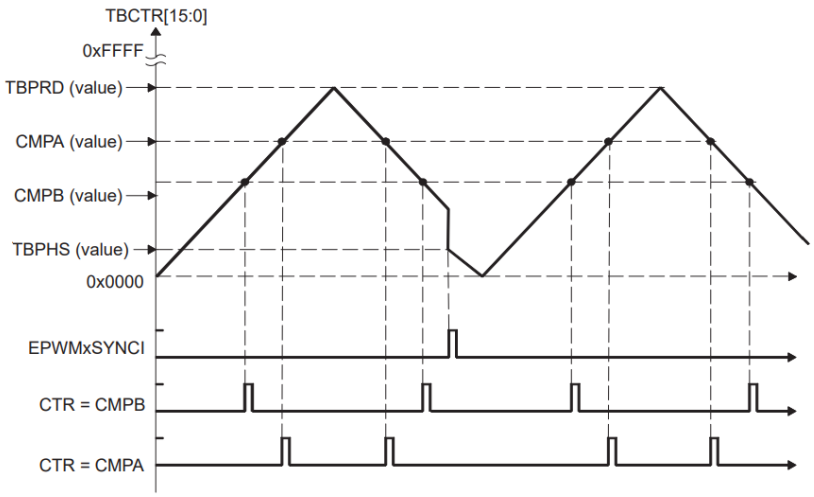


Figure 3.12: enhanced PWM module waveforms from [18]

4

System transfer function and controller

In this chapter a deeper analysis is performed on the system as a whole. Following the system analysis some control methods will be introduced and considered for both controlling the current and for speed control. As the goal of this design is to get a working system, and not necessarily one that needs to reach some particular performance metric, the decision for these control methods will mostly be guided by ease of implementation, and not performance.

4.1. System Analysis

This section aims to analyse the dynamics of the plant (passive electronics, motor dynamics) and use these findings to identify key parameters to use when designing the control loop.

In Section 3.1.2 the passive circuit of the system is analysed, and a block diagram version of the passive circuit is presented in Figure 4.1. The input signal of the model is the current output from the CSI, in a stationary reference frame. Ideally for control and simplicity it would be useful if the system has a unit gain. This is true for the DC-gain, and as the frequency is expected to be below the peak in Figure 3.3 the system will be at unit gain during a quasi-static state. However at higher than this frequency or increasing rapidly the resonance in the system can cause instability. This is further discussed in Section 4.2.

4.2. Current Control

Current control in a CSI ensure that the requested current from the speed controller is put through the motor. In bode plot terms this means that the response should be unity for the entire bandwidth. The major challenge is that the system requires a filter capacitor. The inductor in the motor and the filter capacitor have a resonance frequency that causes instability at the higher end of the bandwidth. The effect that this has is that increasing the size of the capacitor dampens this peak but also decreases the resonance frequency. There are many ways of tackling this issue, but here three common methods will be discussed:

Direct Control By far the simplest control scheme, essentially assumes that the open loop response

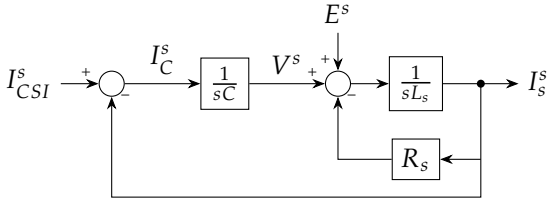
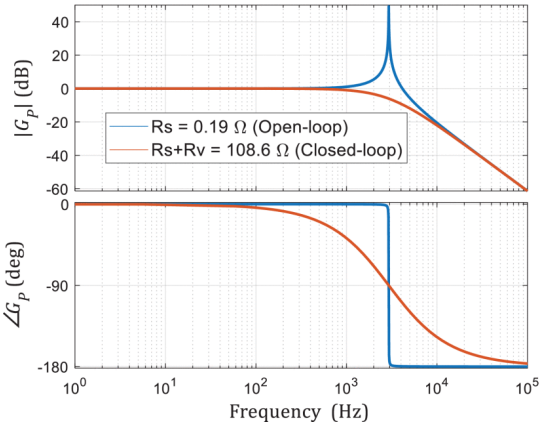
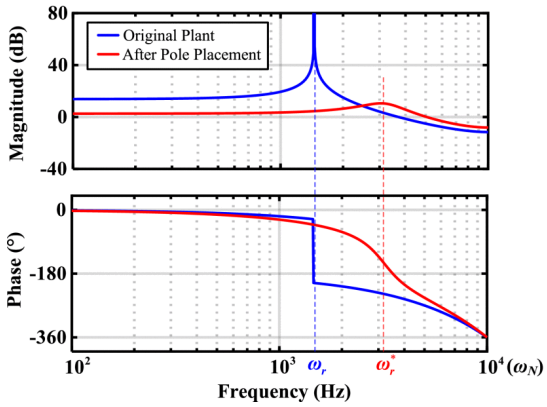


Figure 4.1: Electrical model



(a) Virtual Resistor Bode Plot[16]



(b) Pole Placement Bode Plot[19]

Figure 4.2: Alternative current control bode plots

of the system is sufficient. This control requires no sensors as there is no feedback, and is the simplest to implement because there is nothing to implement. Compared to the other schemes it lacks any form of dampening capabilities.

Virtual Resistor This method addresses the amplitude of the resonance peak. By carefully selecting a capacitor value and modulating the output current in such a way that the voltage on the motor terminals acts as if a dampening resistor is introduced, it is possible to a simple yet robust controller. Compared to the Direct Control it requires feedback in form of current sensors and may require larger than expected filter capacitors[16]. In Figure 4.2a the bode plot from [16] is shown for both the open-loop and closed-loop response.

Pole placement In the situation that increasing capacitance on the output is not possible and/or the system needs to function at a high bandwidth it is possible to do pole placement in such a way that not only increases the bandwidth of the system but also dampens that resonance peak. In [19] a version of this method is shown that does not require any additional voltage sensing. In Figure 4.2b the bode plot from [19] is shown for both the open-loop and closed-loop response.

As mentioned previously the purpose for this design is to make a basis for further research. With that in mind the direct control is chosen but the system is designed in such a way that future modification to test the other methods is possible. The expected effect of choosing this basic form of control is that the speed will be limited until the electric frequency is about 3 tenths of the resonance frequency [16].

4.3. Speed Control

For the speed control the current loop is assumed to be a unit gain. Again as direct current control is used this will only be true at lower speeds and quasi-static states, so the performance of speed control is not expected to be excellent, just easy to implement and stable. Furthermore the motor is only modelled as an inertia and no resistance. The simplified system model is presented in Figure 4.3. The speed control is handled by a PI controller, and the PI constants are calculated using a simple bode plot method. From the block diagram the transfer function is calculated and written in Equation (4.1). ω_B depicts the bandwidth of the system, and it is equal to the proportional gain divided by the inertia, Equation (4.2). After choosing a bandwidth and a dampening factor ζ, the proportional and integral gains K_p and K_i are calculated using equations (4.2) and (4.4).

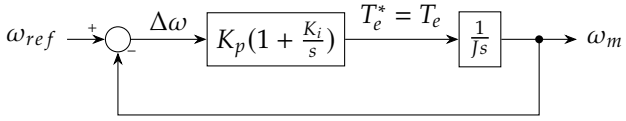


Figure 4.3: Mechanical Model

$$\begin{aligned}\frac{\omega_m}{\omega_{ref}} &= \frac{K_p(s + \frac{1}{K_i})}{\frac{J}{K_i}S^2 + \frac{K_p}{K_i}s + K_p} \\ &= \omega_B \frac{s + K_i}{s^2 + \omega_B s + \omega_B K_i}\end{aligned} \tag{4.1}$$

$$\omega_B = \frac{K_p}{J} \tag{4.2}$$

$$\zeta = \frac{1}{2}\sqrt{\omega_B / K_i} \tag{4.3}$$

$$K_i = \frac{\omega_B}{4\zeta^2} \tag{4.4}$$

For this application a bandwidth of 250 rad/s is chosen and a dampening of 1.

5

Experiments and Validation

Due to the complexity in designing a motor controller, after production of the CSI all its different functions should be evaluated in a manner where each separate feature can be tested in its entirety before moving on. The first test will be a Double-Pulse Test (DPT) which tests the gate driving circuitry, the switching performance, and in case those do not work properly, it will test the safety circuitry.
After this the modulation scheme of the CSI is tested by attaching the encoder of the motor and scoping the gate signals. If the test is successful the gate signals should be as expected for the entirety of the rotation.
Next the previous 2 functions are combined to see if the CSI can synthesize current into a static load. If this goes well a motor is connected to see if open loop spinning is possible.
For the last test the encoder is used to test if the closed loop speed control is possible.

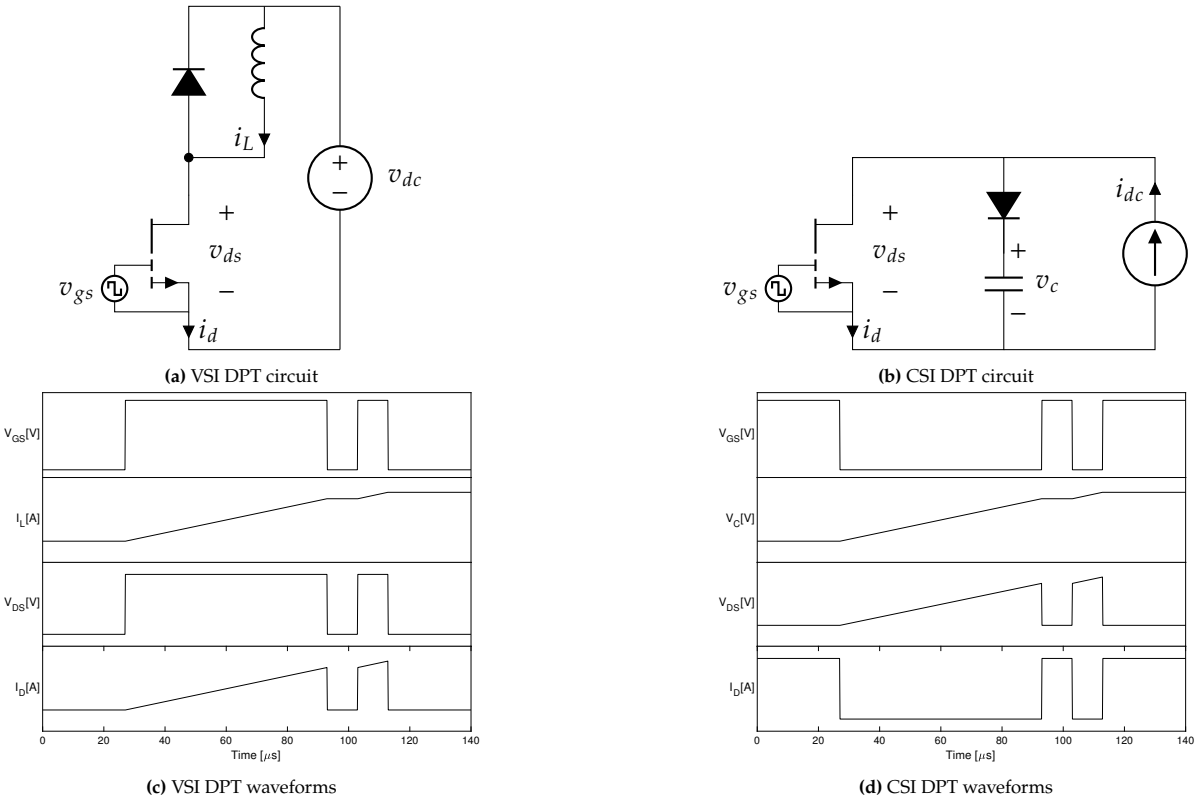
5.1. DPT

5.1.1. Methodology

In the industry the DPT is a common test to measure a converters switching performance. The circuit usually looks like Figure 5.1a in a VSI, where the top diode represents the body diode for the top switch. The working principle is that during a initial pulse the switch is turned on and current through the inductor will build up. Then the switch turns off and the current flows through the diode, remaining constant. then the switch is turned on and off again. During the last switches the current i_d and voltage v_{ds} are measured. These when multiplied give the switching power loss. The ideal waveforms in this circuit are presented in Figure 5.1c.
For the CSI the previous circuit should not be used, as the fundamental mechanics of a CSI dictate that the input current remains constant and the voltage can fluctuate. The circuit in Figure 5.1b is the equivalent version for a CSI. In this case the gate signal is inverted compared to the VSI test. In the CSI test the switch first turns off, blocking current through the switch and sending it through the capacitor and diode. When the switch turns on the current flows through the switch, but the capacitor remains charged as the diode blocks reverse current. Then the switch is turned off and on again, once more measuring v_{ds} and i_d. The ideal waveforms are presented in Figure 5.1d.
For the H8 configuration that is chosen the only switch experiencing switching losses is S_7, so the DPT will be performed only with that switch. The diode can be D_8 and the output capacitor will be the filter capacitors, connected through S_2 and S_3 (see Figure 5.2). These switches are chosen as they are physically the furthest from S_7, resulting in a worst case measurement. The CSI DPT method is discussed in [20], although it has been adjusted to fit this topology.

5.1.2. Simulation

This test is first simulated using LTspice, in combination with the gate driver circuitry. The results are depicted in Figure 5.3. One notable feature in this plots are the big overshoots, which can cause unnecessary strain on the switches or require those switches to be rated to be higher than necessary. The cause of this overshoot is explained in Chapter 6.



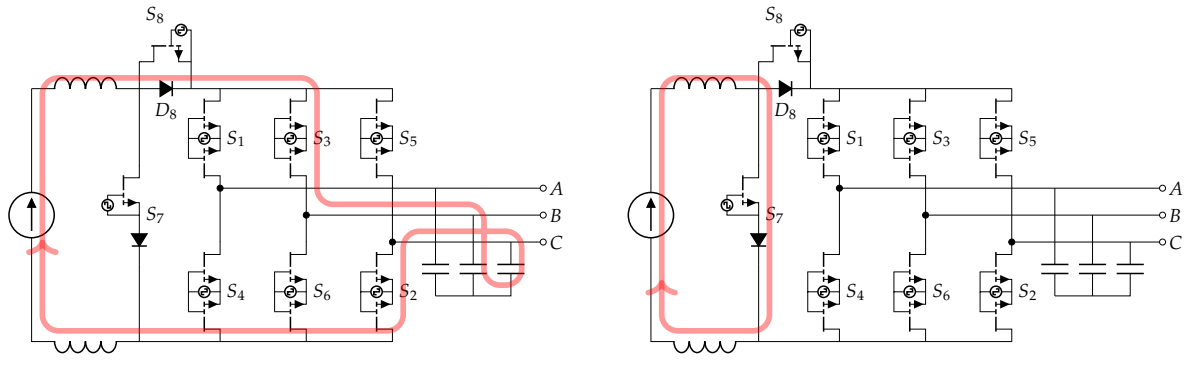
(a) VSI DPT circuit

(b) CSI DPT circuit

(c) VSI DPT waveforms

(d) CSI DPT waveforms

Figure 5.1: VSI and CSI circuits and waveforms



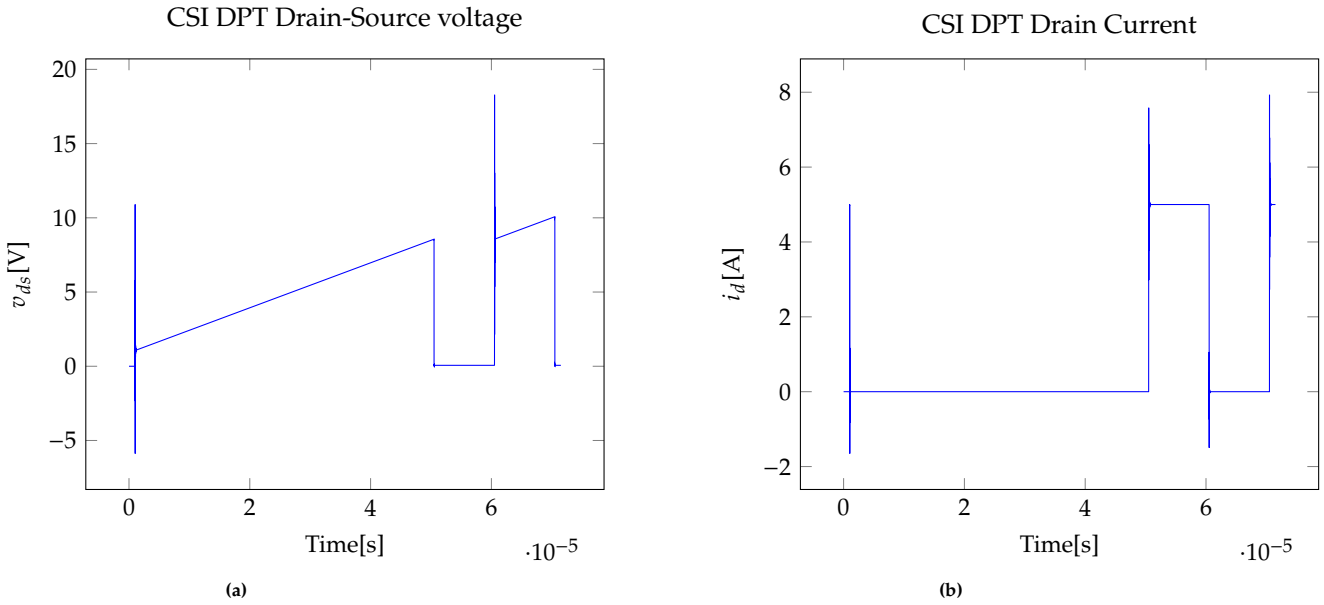
(a) DPT current path when S_7 is open.

(b) DPT current path when S_7 is closed.

Figure 5.2: The path the current takes during a CSI DPT

Table 5.1: CSI requirements

DPT parameters			
Parameter	Symbol	Value	Unit
Capacitor Voltage	V_D	10	V
DC Current	I_{DC}	5	A
Capacitance	C_f	33	µF
Pulse on-time	T_1	66	µs



(a) (b)

Figure 5.3: DPT CSI simulation waveforms

5.1.3. Result

The results of the DPT test are shown in Figure 5.4. The peaks in Figure 5.3 are still present and have exacerbated, and the current waveform also depicts major ripples. It should be noted that this is after adding a RC snubber to the switch to aid dampening the voltage ripple. In Figures 5.4c and 5.4d the transients are zoomed in on and the calculated on and off losses are presented.

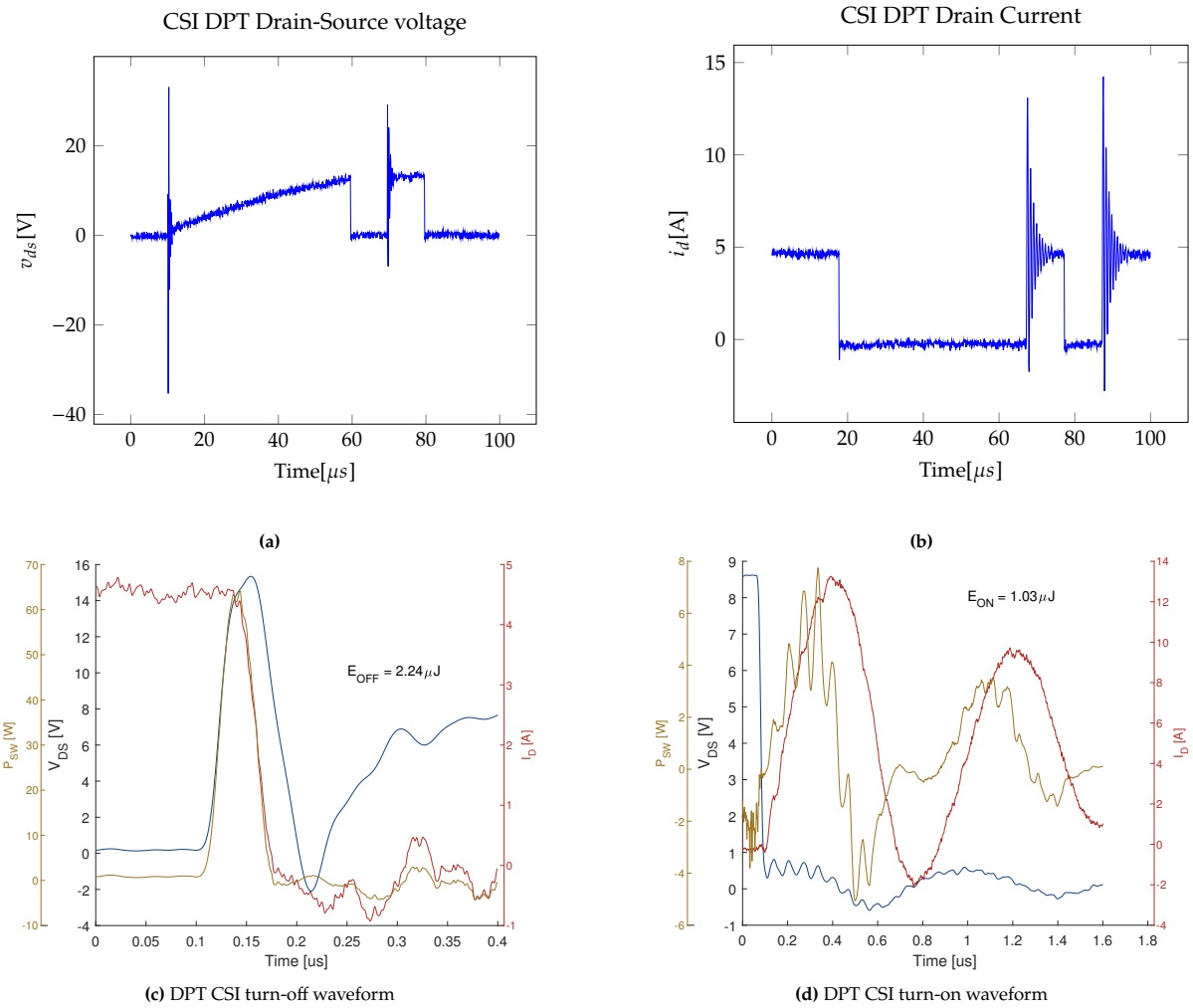
5.2. Modulation

The modulation is quickly evaluated by measuring the gate signals at a known angle. For repeatability the signals are measured during commutation, and are shown in Figure 7.2. There are 2 major difference between this and the diagram in Figure 2.5b: S_7 is inverted so that the failure state of this signal shorts the DC link and prevents an overvoltage, and S_b features a spik in the same spot as S_a. This is a consequence of a limitation from the used C2000 processor.

5.3. Current Control

As a test to see if the currents are synthesized as intended, the system is first evaluated at standstill. The electric angle is set to 0, I_{DC} is set to 1A and m_a is set to 0.8. The result for all three phases is presented in Figure 5.6. As expected phase A reaches 0.8 A, and both B and C are at −0.4 A.

After the current amplitude modulation is verified to work properly at no speed, an artificial angle signal was generated at 28 Hz. This test was done for 2 reasons: to evaluate if the converter is able to produce a proper sinusoid, and to see what the actual pole-pair count is of the motor as this was not specified in its documentation. The motor speed was measured to be 2Hz, so the pole-pair count was determined to be 14. The current of phase A was measured and displayed in Figure 5.7



(c) DPT CSI turn-off waveform

(d) DPT CSI turn-on waveform

Figure 5.4: DPT CSI measurement waveforms

5.4. Speed Control

To evaluate the speed control of the motor drive the controller is fed a stair case reference signal. This allows for multiple setpoints to be evaluated and shows the difference in performance as speed increases. The chosen input waveform is shown in Figure 5.8, and consists of 9 different setpoints ranging from 500 to 2500 rpm, with a step size of 250 rpm. In the same figure the measured speed response is plotted. What is notable in this response is that the response is consistent until about 1500 rpm, after which the overshoot flattens out and after 2000 rpm the controller is not able to reach the speed setpoint. This has to do with 2 issues that are explained in Chapter 6, one that limits the possible input current and anothe one that limits the modulation index. These meant that this test had to be performed with severely limited modulation index at a low input current, resulting in a low torque on the rotor.

Another part of the speed control worth analysing is how it compares to the simulated version. This comparison is shown in Figure 5.9. Quite obviously, the simulation predicts a many times quicker response than reality. Again this is probably an effect of the simple nature of the speed control, as it assumes unity response from the speed control and there has been no analysis for disturbance rejection or any effect of the back-emf. That being said the control features acceptable overshoot and keeps the speed stable. The high frequency ripple visible is more than likely an effect from a non-linearity in the angle from the rotor position sensor.

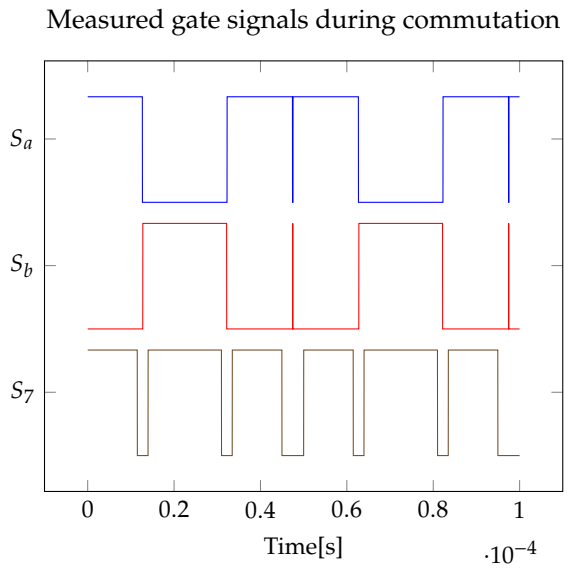


Figure 5.5: The measured gate signals during commutation. Measured with a logic probe

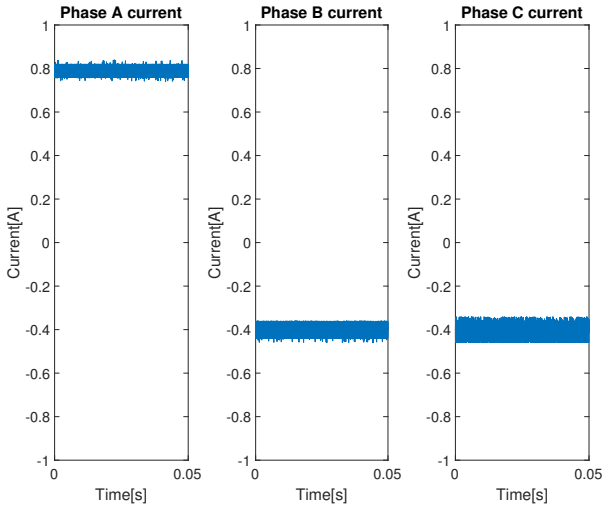


Figure 5.6: Phase currents through the motor for $I_{DC} = 1A$, $m_a = 0.8$, $\theta_e = 0$ and $\omega_e = 0$, measured with a current probe.

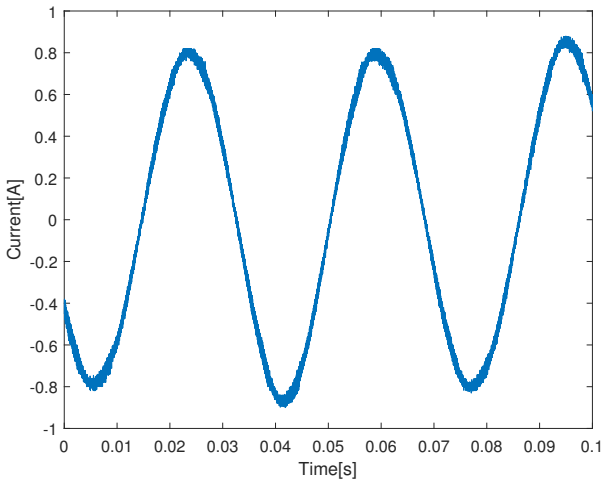


Figure 5.7: Phase A current, $I_{DC} = 1A$, $m_a = 0.8$ and $f_e = 28$, measured with a current probe.

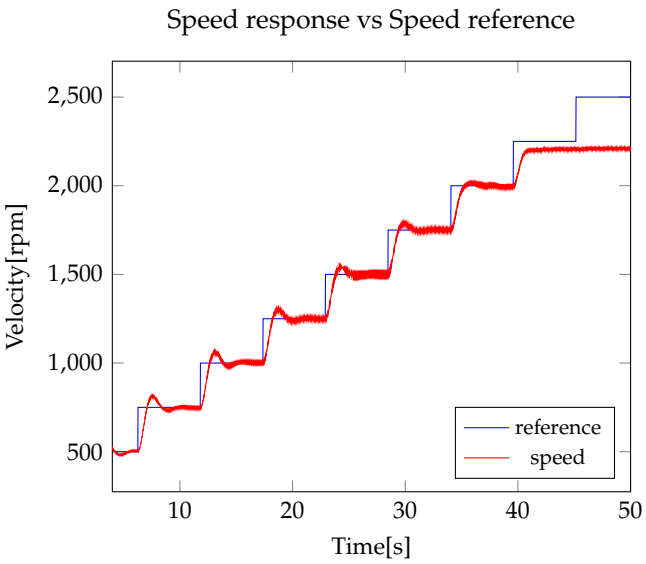


Figure 5.8: Measured Speed response to a stairway reference signal, starting at 500 rpm to 2500 rpm.

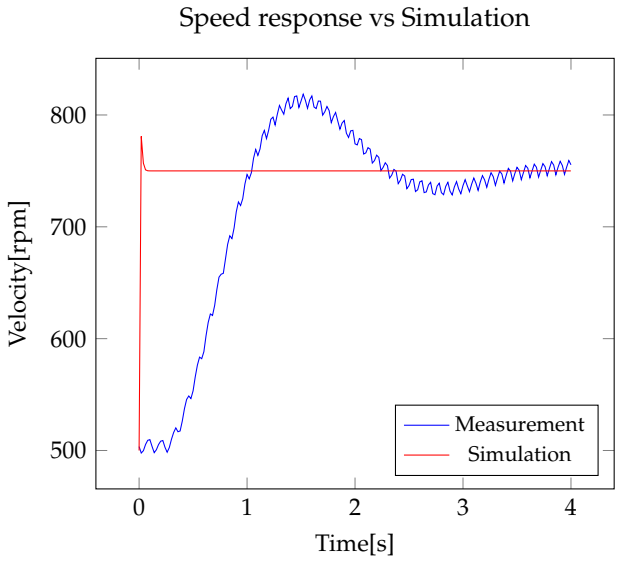


Figure 5.9: Comparison between the measured and simulated speed step response.

6 Issues

The purpose of this project has been to build a prototype of a CSI with high current capacity, in order to see if there are any problems that would make the chosen concept unsuitable. In this chapter various of these problems will be discussed and explained, starting off with the most important one, nicknamed "The Diode Problem".

6.1. The Diode Problem

As hinted at before in Chapter 5, when performing the DPT, an overshoot was seen. This overshoot is many times worse than predicted, and it caused the overvoltage protection circuit to kick in when trying to do a DPT at higher currents.

Now conventionally, overshoot is cause by 2 things working in tandem. Something has a steep increase in either current or voltage, which injects high frequencies into a circuit. Secondly poor circuit design can cause the circuit to be more vulnerable to these high frequencies due to high parasitics in the system.

In this case this conventional explanation did not hold water. The circuit was adapted to increase the gate resistances on S_7 to be around one hundred times larger, without noticeable impact on the ripple and overshoot. Secondly an RC snubber was introduced. This reduced the ringing significantly but again did nothing for the overshoot. The overshoot appears to be caused by something else.

"When you have eliminated the impossible, whatever remains, however improbable, must be the truth." [21, p. 26]. After the effects from the switching of S_7 were ruled out, the only plausible device that could cause these issues is the diode D_8. Diodes do have a mechanism that could cause an overshoot, the forward or reverse recovery. However this diode is of the Schottky variety, which are widely used in power electronics mainly due to the absence of this effect.

It appears that this effect is still present in diodes, only when driving it with voltage the effect is not visible. In Figure 6.2 the ideal characteristic from a diode is shown. At low voltage the current is nearly 0, so the resistance is also high. The mechanism that changes this resistance is driven by voltage, so when S_7 suddenly closes, the current ramps up at the same speed through D_8. The voltage has no time to build up over the diode, causing it to conduct while still moving from the high resistance to the low resistance region. So when the current ramps up and is forced through the diode the high resistance means that a voltage spike is introduced over the diode until it is in full forward conduction. This is a fundamental flaw with the H7 or H8 topology as described in this thesis. While changing components can definitely mitigate this overshoot, doing so without compromising on efficiency or size will be challenging to say the least. Here are a few suggestions on how to cope with this phenomenon:

Passive solution There may be space in the design to find a solution in the form of a parallel circuit could absorb this overshoot. It is recommended to attempt this with either just passive components, or using the fast reaction capabilities of a TVS diode. While attempting a solution the use of normal diodes was unsuccessful as other diode just had the same issue.

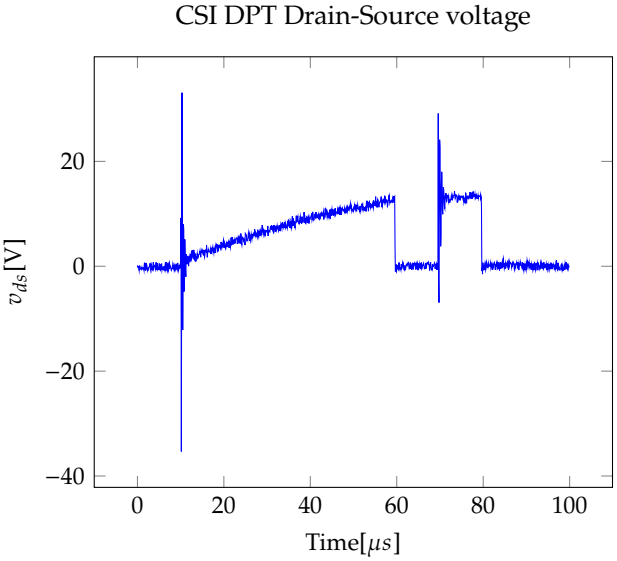


Figure 6.1: Overshoot and ripple during initial DPT measurement

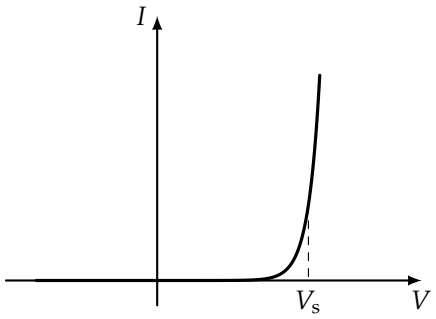


Figure 6.2: Ideal Diode Characteristic [22]

Active solution In this design the input current was assumed and regulated to be constant. More advanced topologies can be considered where the input current is modulated to ZCS when commutating, which fully eliminates the overshoot.

Design around it During testing it appeared that the overshoot was not a function of voltage or rise time, but mainly one of rise amplitude. Therefore if the output voltage increases substantially the overshoot becomes lower in relation. Likely though this means that a higher DC bus voltage would be necessary.

For this design this flaw meant that the input current was ultimately limited to a few amps, as any higher would cause an immediate overvoltage event.

6.2. The Front End

This CSI was designed without what is commonly referred to as "The Front End". In the context of a CSI the front end acts as a voltage to current converter. If a CSI is to be used in any kind of electric vehicle a proper front end will be required as most if not all energy storage solutions (like batteries or power cells) have a constant voltage on the output, not a constant current. For this prototype the choice was made to replace the front end with a lab bench power supply. However, from experimentation it has become clear that the current control on these devices was not designed to maintain a proper output current but rather to limit current to a maximum setpoint. In practise it means that at high current modulation the input current would become an offset sinusoid at 50Hz, with its amplitude increasing rapidly and quickly causing the overvoltage due to "The Diode Problem". The current waveform is shown in Figure 6.3.

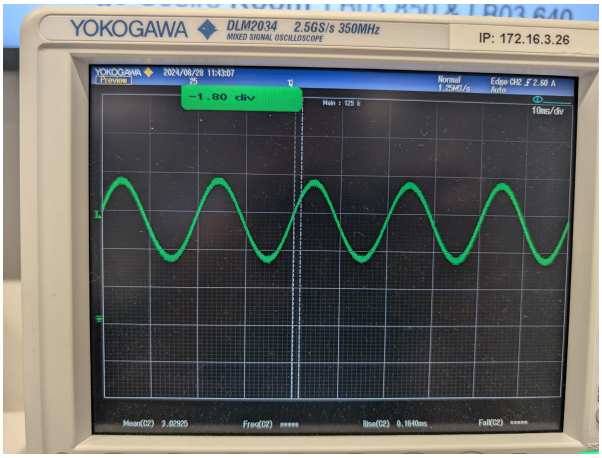


Figure 6.3: Measured DC link current with a sinusoid, picture taken shortly before the system crashed.

6.3. Layout

The last main issue of the design concerns its layout. Now compared to the previous issues this one did not actually limit any performance. However it is something that was not done properly in this design and may have caused issues at higher speed. In the first months of this design some decisions were made that eventually made proper layout for a CSI very difficult. For instance the decision to give every switching leg a seperate PCB is something that makes more sense for a VSI than for a CSI. The better solution may be having all the top switches and bottom switches together, on 2 separate PCBs. In [23] the motivation behind this concept is explained pretty clearly, but basically it allows for the filter capacitors to sit closer to the switches, reducing the path inductance compared to the chosen solution.

7

Conclusion

7.1. Reflection

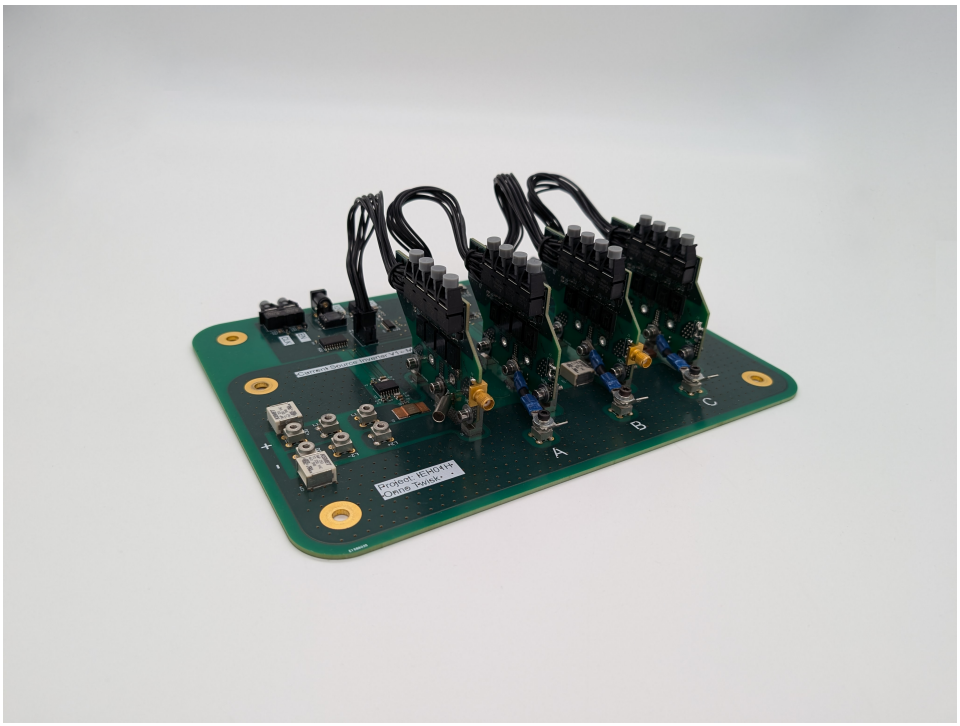


Figure 7.1: The final design of the inverter

Before reflecting on the design let us first state the design goals once again:

"The goal of this thesis is to design a 1kW CSI that can be used in a laboratory setting to see what issues come up when voltage is limited"

Due to the proven functionality shown in Chapter 5 and the discovery of the major issues discussed in Chapter 6, it is fair to say that this goal has been accomplished. It is easy to get lost in the fact that the speed and torque are both limited to about 10% of the design spec, but for a first attempt at such an unconventional type of converter these flaws are only to be expected. Combining the gained knowledge and the benefit of this new CSI development platform, its only reasonable to say that the project was a success.

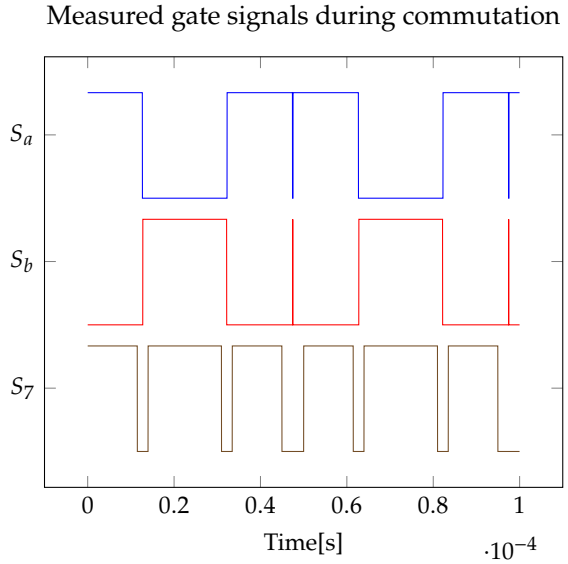


Figure 7.2: The measured gate signals during commutation. Measured with a logic probe

7.2. Future work

As discussed in Chapter 6, 3 main issues have come up with this design. Besides this for scaling up a few other consideration or alterations can be made in the second version.

Modular Drive Much of the initial appeal from the CSI is that it can be used in a modular fashion constructed around a motor without adding a significant amount of bulk to the package. This modularity is the main piece of the puzzle that cannot be evaluated by improving the existing design, and should be definitely included in the next version.

Advanced Control Electronics The actual control of the motor (while analysed to an advanced extent) was very simple as no real power transfer was used in this system. The main problem in including the designed control scheme was the limitations of the microcontroller, so moving to a more advanced system (like FPGA based processing) should definitely yield positive results.

Resonance Front-end It has become apparent that a proper front-end is critical in any future design, however a special mention should be made for the resonance type of front-end. A topology that could incorporate such a front-end could have the potential to achieve full ZCS/ZVS operation and also could require smaller DC link components.

IMS packaging The current temperature management strategy can be summed up as "just put a big heatsink on it". In fact as input current was limited no heatsink was needed during testing. Higher power density can be achieved by using an IMS PCB, which features a thick layer of alumnium that can sink much of the generated heat and dissipated the heat much more effectively.

References

[1] Salvatore Musumeci et al. "Monolithic Bidirectional Switch Based on GaN Gate Injection Transistors". In: *2020 IEEE 29th International Symposium on Industrial Electronics (ISIE)*. 2020, pp. 1045–1050. DOI: 10.1109/ISIE45063.2020.9152230.

[2] T. Halkosaari and H. Tuusa. "Reduction of conducted emissions and motor bearing currents in current source PWM inverter drives". In: *30th Annual IEEE Power Electronics Specialists Conference. Record. (Cat. No.99CH36321)*. Vol. 2. 1999, 959–964 vol.2. DOI: 10.1109/PESC.1999.785627.

[3] Thomas Friedli et al. "Design and Performance of a 200-kHz All-SiC JFET Current DC-Link Back-to-Back Converter". In: *IEEE Transactions on Industry Applications* 45.5 (2009), pp. 1868–1878. DOI: 10.1109/TIA.2009.2027538.

[4] Hang Dai et al. "Common-Mode EMI Examination of Three-phase Voltage-Source and Current-Source Converters Systems using WBG Devices". In: *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2020, pp. 3558–3565. DOI: 10.1109/ECCE44975.2020.9235369.

[5] Hang Dai et al. "Comparative Study of Conducted Common-Mode EMI in WBG-Enabled DC-Fed Three-Phase Current-Source Inverter". In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 10.6 (2022), pp. 7188–7204. DOI: 10.1109/JESTPE.2022.3161422.

[6] A.F. Moreira et al. "High-frequency modeling for cable and induction motor overvoltage studies in long cable drives". In: *IEEE Transactions on Industry Applications* 38.5 (2002), pp. 1297–1306. DOI: 10.1109/TIA.2002.802920.

[7] Y. Zhang. *Investigation of Approaches for Improving the Performance and Fault Tolerance of Permanent Magnet Synchronous Machine Drives Using Current-source Inverters*. University of Wisconsin–Madison, 2016. URL: https://books.google.nl/books?id=0b6pnQAACAAJ.

[8] Huai Wang and Frede Blaabjerg. "Reliability of Capacitors for DC-Link Applications in Power Electronic Converters—An Overview". In: *IEEE Transactions on Industry Applications* 50.5 (2014), pp. 3569–3578. DOI: 10.1109/TIA.2014.2308357.

[9] Xiaoqiang Guo. "Three-Phase CH7 Inverter With a New Space Vector Modulation to Reduce Leakage Current for Transformerless Photovoltaic Systems". In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* 5.2 (2017), pp. 708–712. DOI: 10.1109/JESTPE.2017.2662015.

[10] Doris Ragna Meyer et al. "Influence of impulse voltage repetition frequency on RPDIV in partial vacuum". In: *IEEE Transactions on Dielectrics and Electrical Insulation* 25.3 (2018), pp. 873–882. DOI: 10.1109/TDEI.2018.006722.

[11] Maarten van Schagen and Yana Brodskaya. "Control Algorithm Design for a High Power Electronic Speed Controller". English. BA thesis. Delft University of Technology, June 26, 2023. URL: https://resolver.tudelft.nl/uuid:8c784c3a-7882-4a9a-bdfe-1367254539ad.

[12] N.G. Hingorani and L. Gyugyi. *Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems*. Wiley, 2000. ISBN: 9780780334557. URL: https://books.google.nl/books?id=2-ceAQAAIAAJ.

[13] Hang Dai et al. "An H8 Current-Source Inverter Using Single-Gate WBG Bidirectional Switches". In: *IEEE Transactions on Transportation Electrification* 9.1 (2023), pp. 1311–1329. DOI: 10.1109/TTE.2022.3202303.

[14] *Wide-bandgap semiconductors: Performance and benefits of GaN versus SiC*. SLYT801. Texas Instruments. 2020.

[15] *Top-side cooled 100 V E-mode GaN transistor*. GS61008T. Rev. 200402. GaN Systems. Jan. 2020.

[16] Renato A. Torres et al. "A Simple and Robust Controller Design for High-Frequency WBG-Based Current-Source-Inverter-Fed AC Motor Drive". In: *2020 IEEE Transportation Electrification Conference & Expo (ITEC)*. 2020, pp. 111–117. DOI: 10.1109/ITEC48692.2020.9161527.

[17] *Self-Powered Single-Channel Isolated GaN FET Driver with Power-Thru Integrated Isolated Bias Supply*. AHV85110. Initial release. ALLEGRO microsystems. June 2023.

[18] *TMS320x280x, 2801x, 2804x Enhanced Pulse Width Modulator (ePWM) Module Reference Guide*. SPRU791F. Texas Instruments. Nov. 2004.

[19] Jindong Zhang et al. "Pole Placement-Based Current Control Method for CSI-Fed PMSM Drive With Eliminating Capacitor Voltage Sampling". In: *IEEE Transactions on Power Electronics* 38.8 (2023), pp. 9409–9420. DOI: 10.1109/TPEL.2023.3267075.

[20] Feida Chen et al. "Performance Evaluation and Loss Modeling of WBG Devices based on a Novel Double-Pulse Test Method for Current Source Inverter". In: *2021 IEEE Transportation Electrification Conference & Expo (ITEC)*. 2021, pp. 219–224. DOI: 10.1109/ITEC51675.2021.9490060.

[21] A.C. Doyle. *The Case-book of Sherlock Holmes*. Collection of British and American authors. George H. Doran Company, 1927. ISBN: 9781427035417. URL: https://books.google.nl/books?id=lL9EAAAAYAAJ.

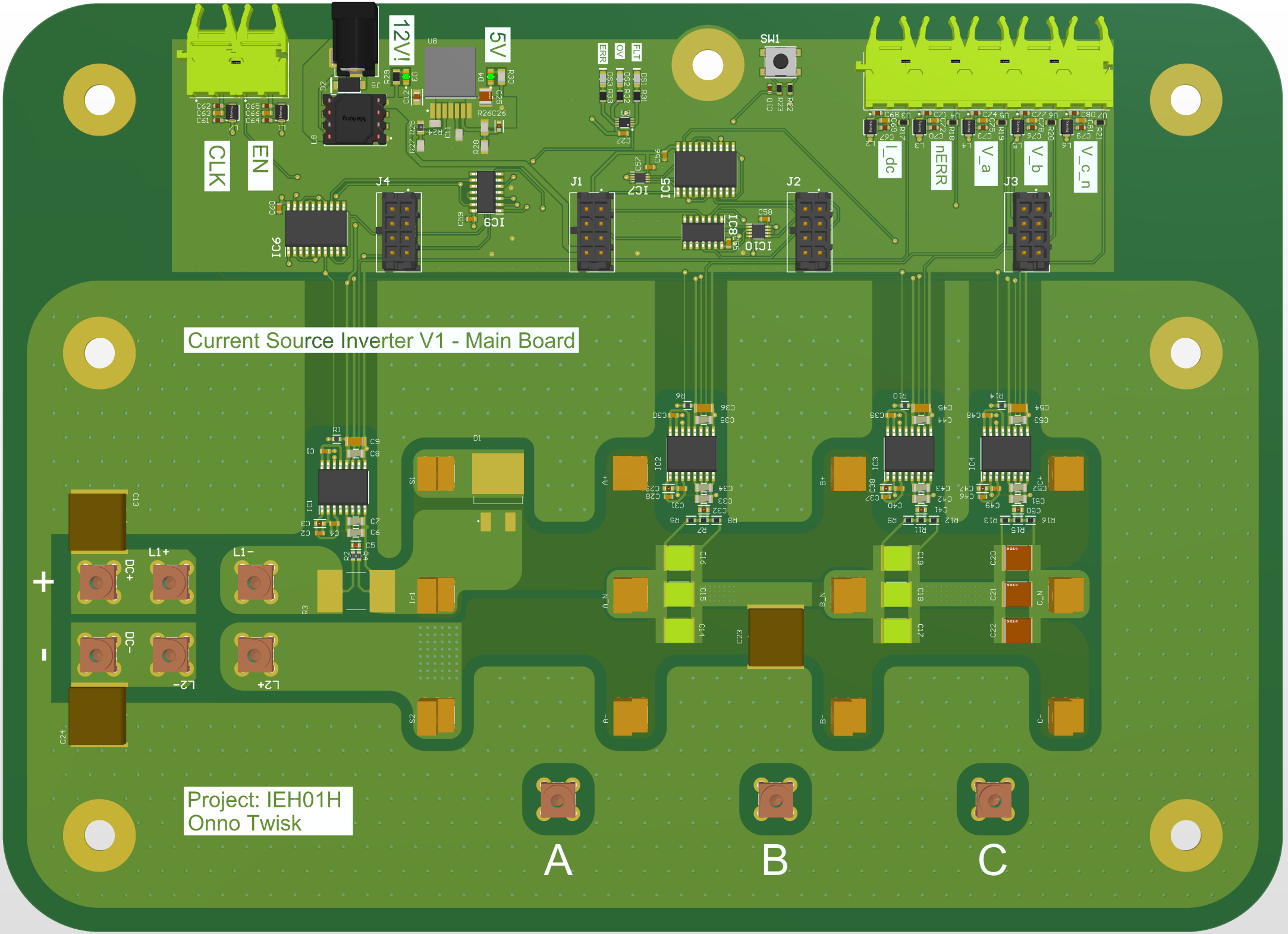
[22] Alexandros Tsagkaropoulos. *Ideal Diode Characteristic*. URL: https://tikz.net/ideal-diode-characteristic/.

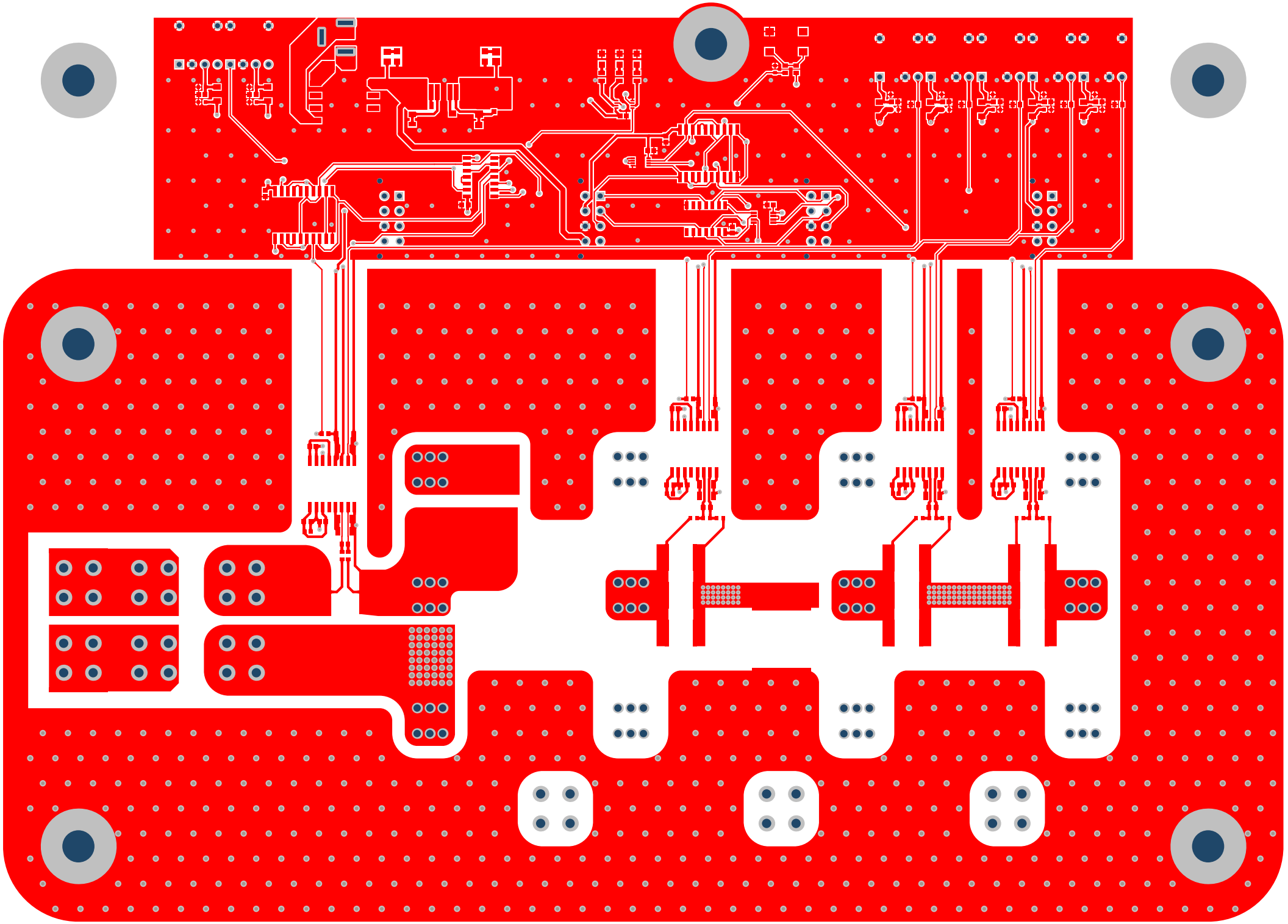
[23] Mustafeez-ul-Hassan and Fang Luo. "Influence of Layout Parasitics and its Optimization in Two-Level Gallium-Nitride Based Current Source Inverter". In: *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2022, pp. 1–6. DOI: 10.1109/ECCE50734.2022.9947592.

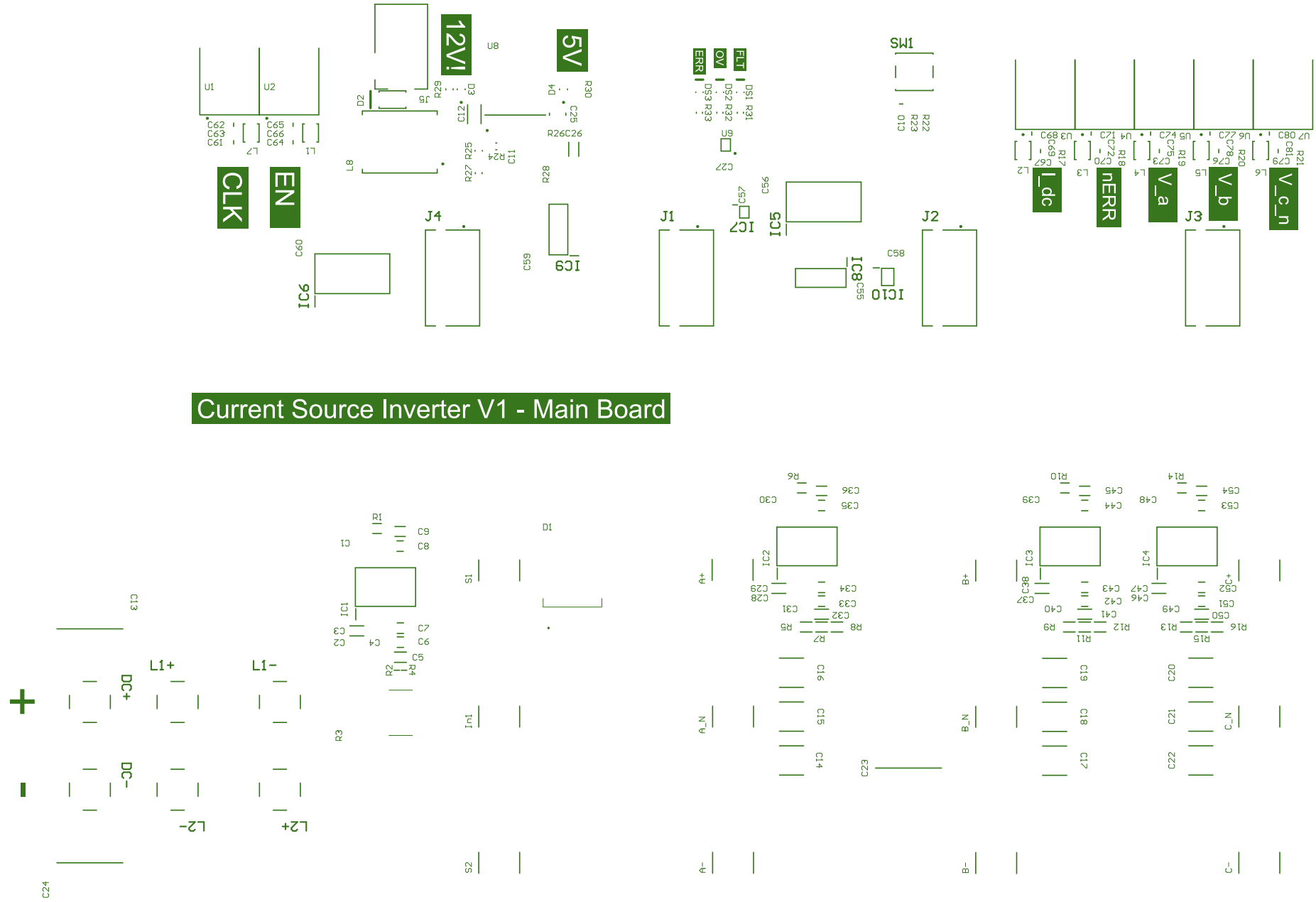
A

PCB design documentation

This Appendix contains the design files generated using Altium Designer. First the mainboard is presented, and then the seperate switching leg PCB.


12V!
5V
CLK
EN
I_dc
nERR
V_a
V_b
V_c_n
J1
J2
J3
J4
SW1
Current Source Inverter V1 - Main Board
L1+
L1-
L2+
L2-
DC+
DC-
A
B
C
Project: IEH01H
Onno Twisk

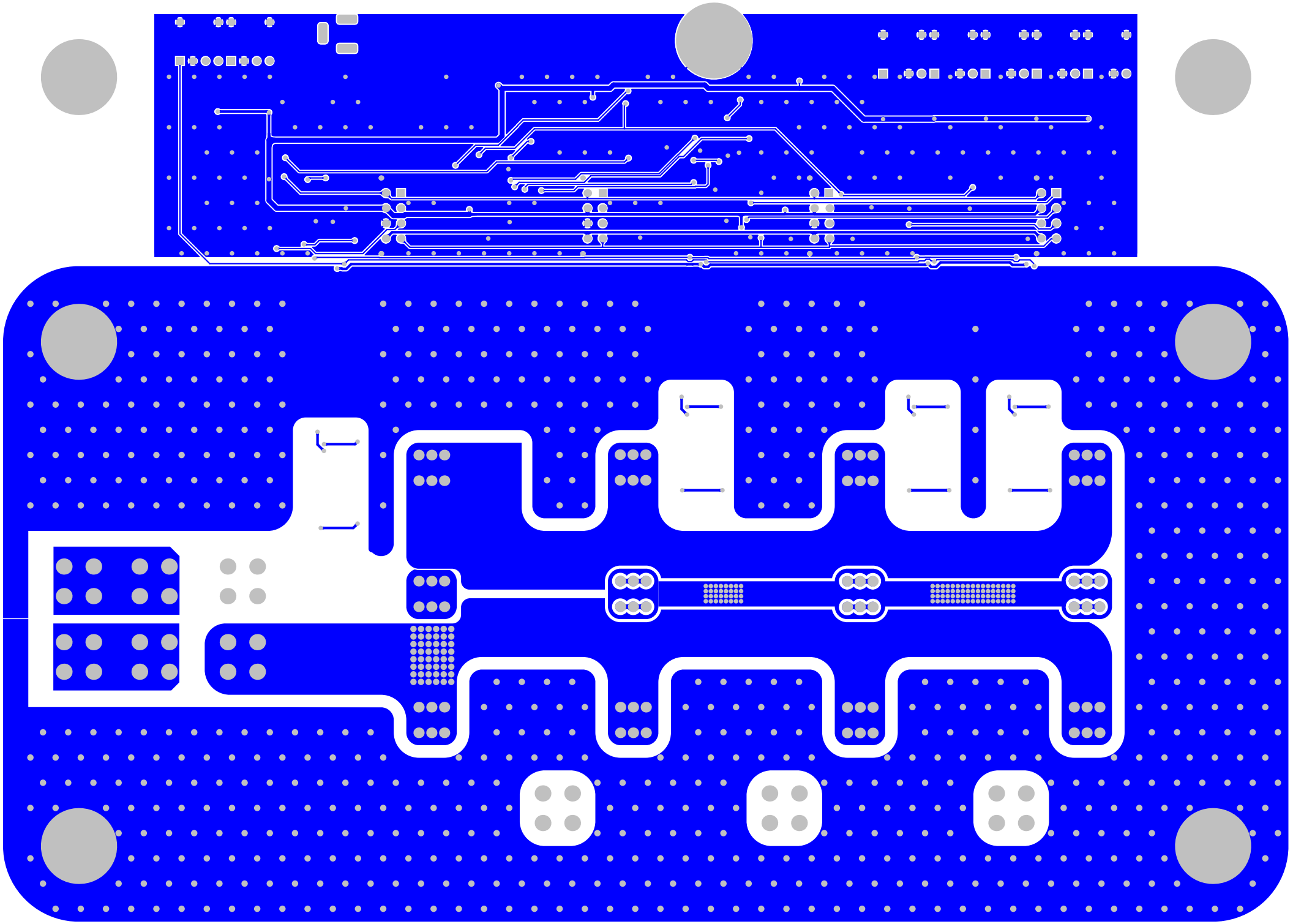




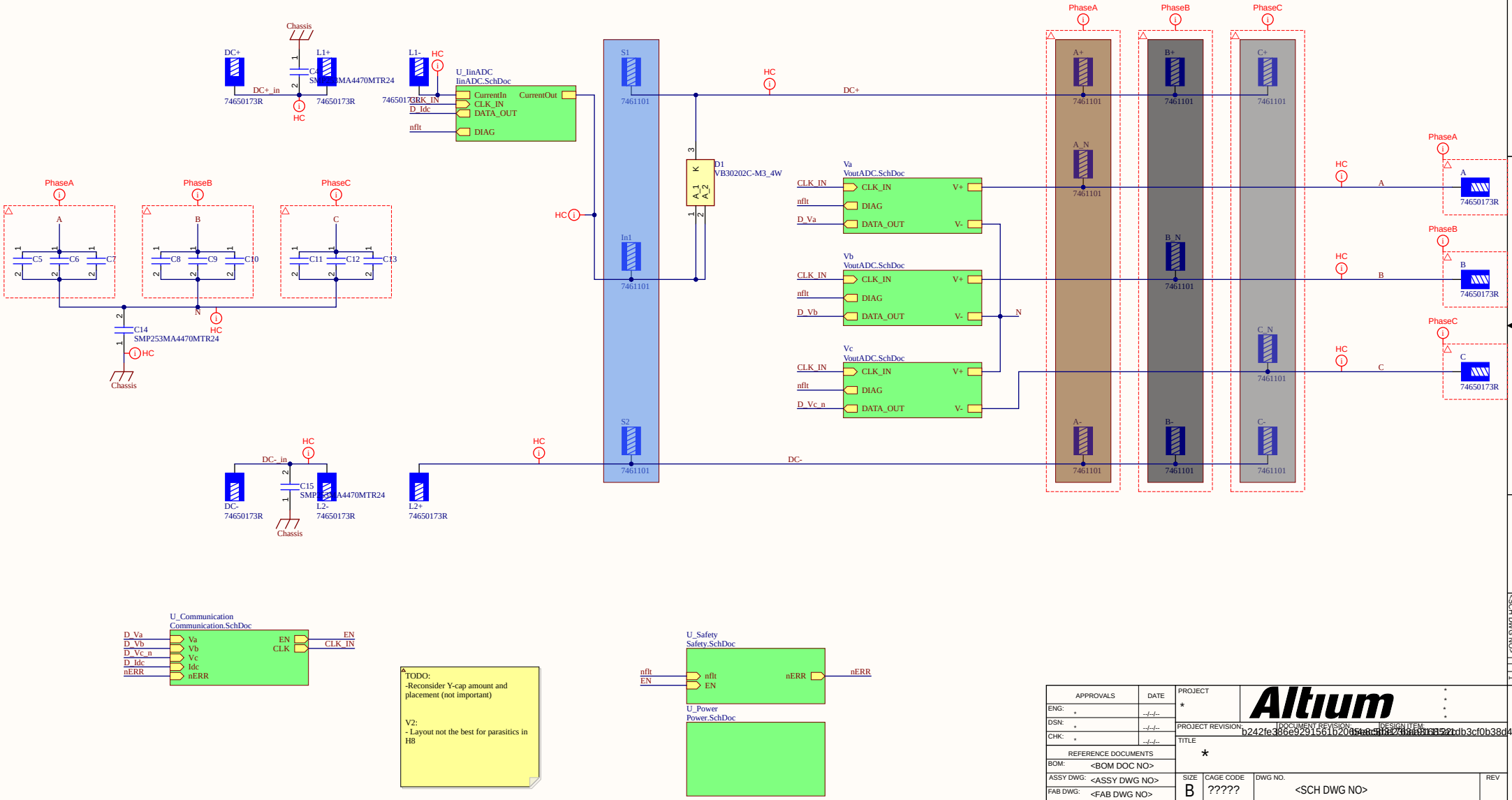
Current Source Inverter V1 - Main Board

Project: IEH01H
Onno Twisk

A B C



REVISION	DESCRIPTION	DATE	APPROVED



TODO:
-Reconsider Y-cap amount and placement (not important)

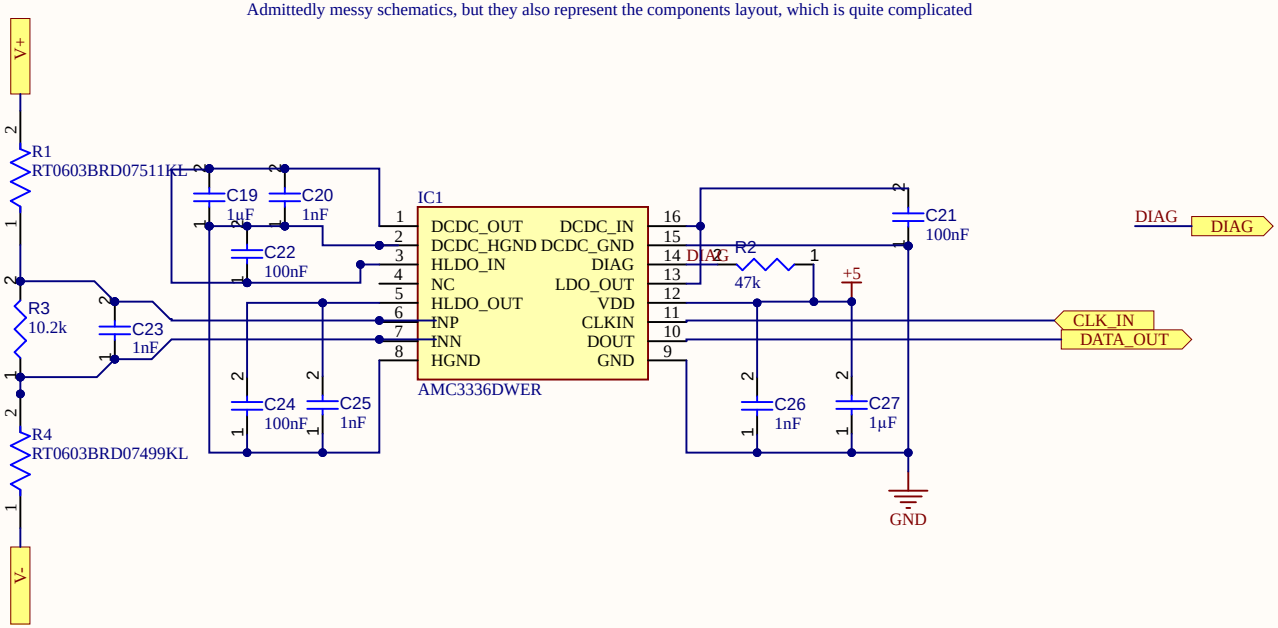
V2:
- Layout not the best for parasitics in H8

APPROVALS	DATE
ENG: *	--/--/--
DSN: *	--/--/--
CHK: *	--/--/--
REFERENCE DOCUMENTS	
BOM: <BOM DOC NO>	
ASSY DWG: <ASSY DWG NO>	
FAB DWG: <FAB DWG NO>	
PCB DWG: <PCB DWG NO>	

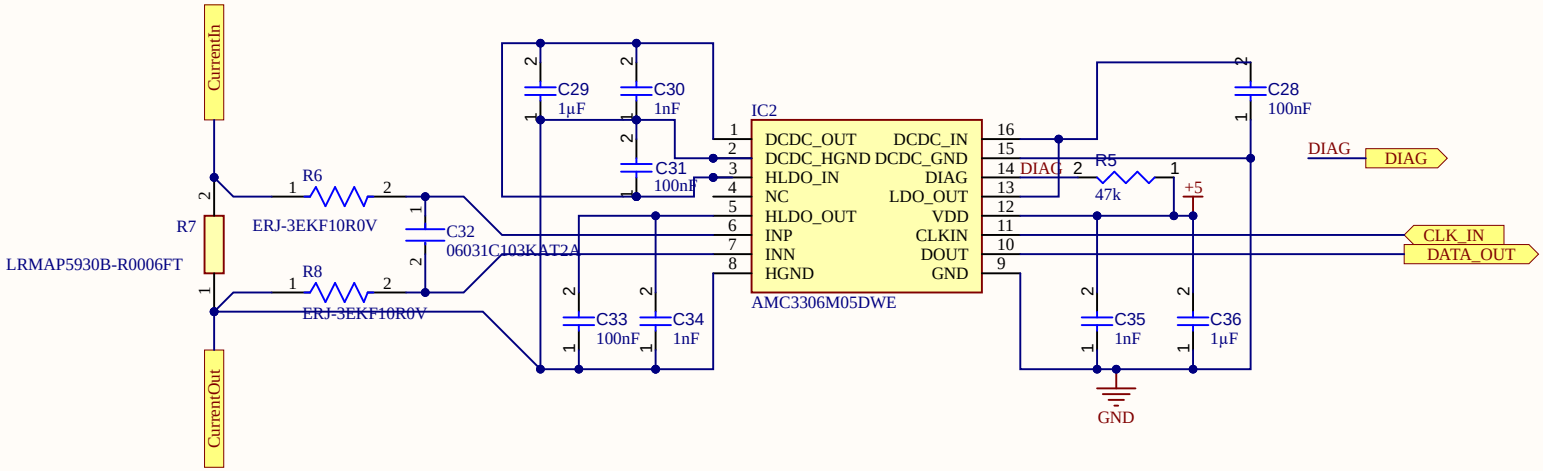
PROJECT *	Altium		
PROJECT REVISION:	DOCUMENT REVISION:	DESIGN ITEM:	
TITLE *			
SIZE B	CAGE CODE ?????	DWG NO. <SCH DWG NO>	REV
SCALE:	FILE NAME Sheet1.SchDoc	SHEET 1 OF 10	

b242fe386e9291561b20[illegible]db3cf0b38d48d4

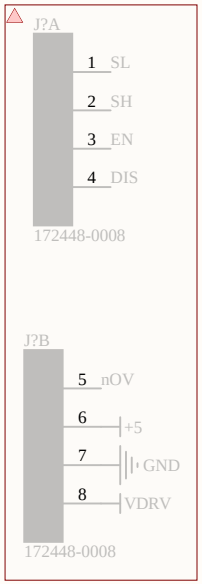
Admittedly messy schematics, but they also represent the components layout, which is quite complicated

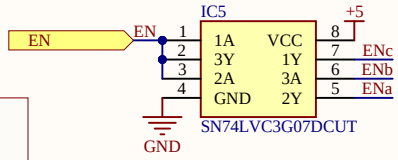


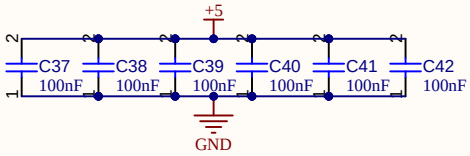
Title		
Size: A4	Number	Revision
Date: 10/28/2024		Sheet of
File: C:\Users\..\VoutADC.SchDoc		Drawn By:

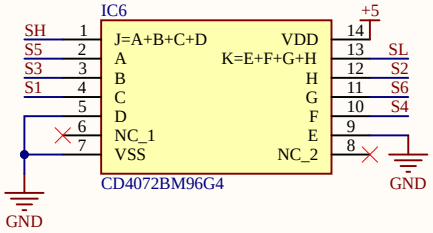


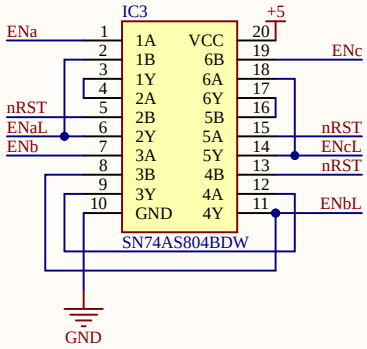
Title		
Size: A4	Number	Revision
Date: 10/28/2024		Sheet of
File: C:\Users\..\IinADC.SchDoc		Drawn By:

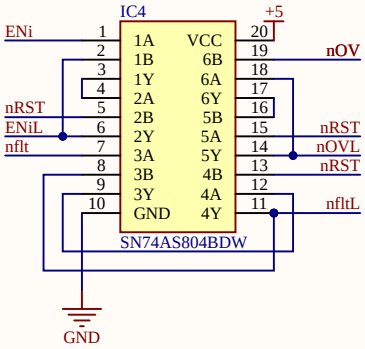




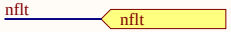


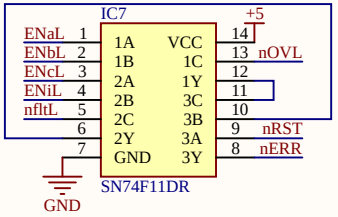






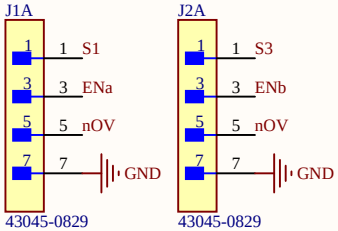
NAND Latching

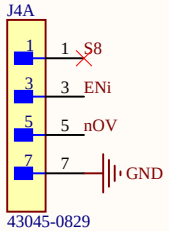


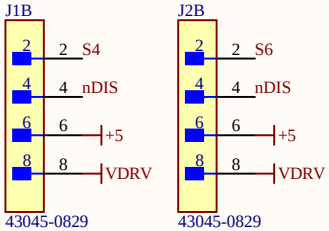


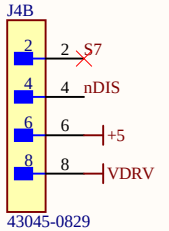
AND Gate to sum errors

TODO:
- Add falstad link
- improve legibility
- Add status LED

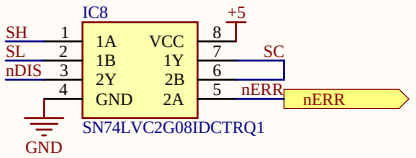




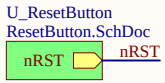


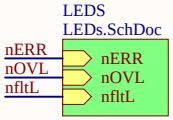


The input dim should be fitted with a NAND gate, meaning that nDIS function is inverter (still disables but disabled (or safe state) means closed

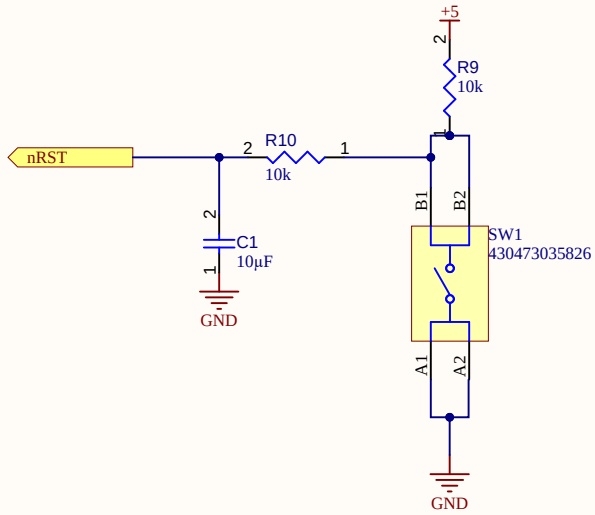


Final disable logic

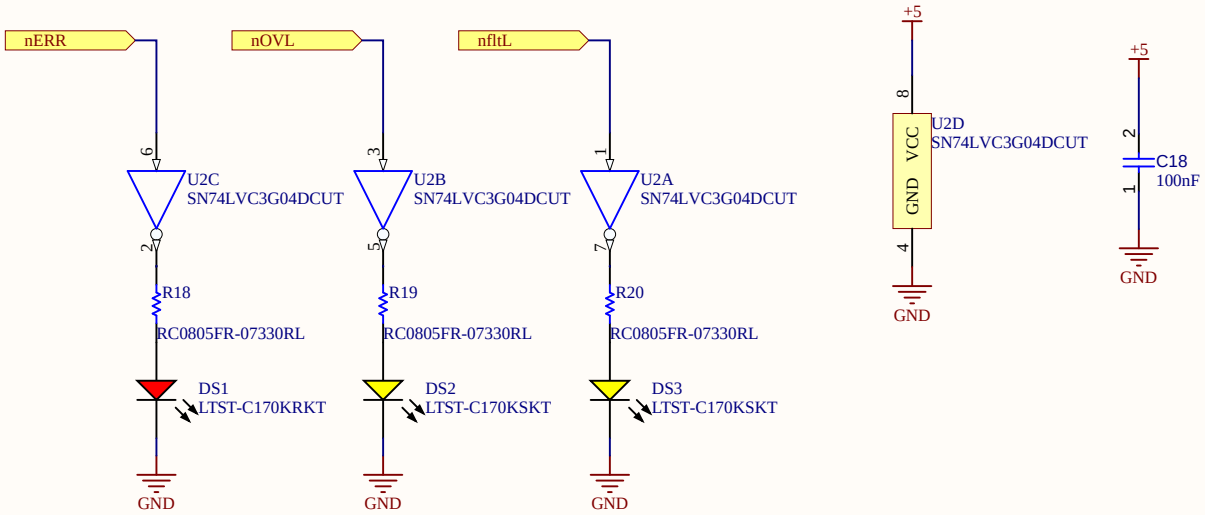




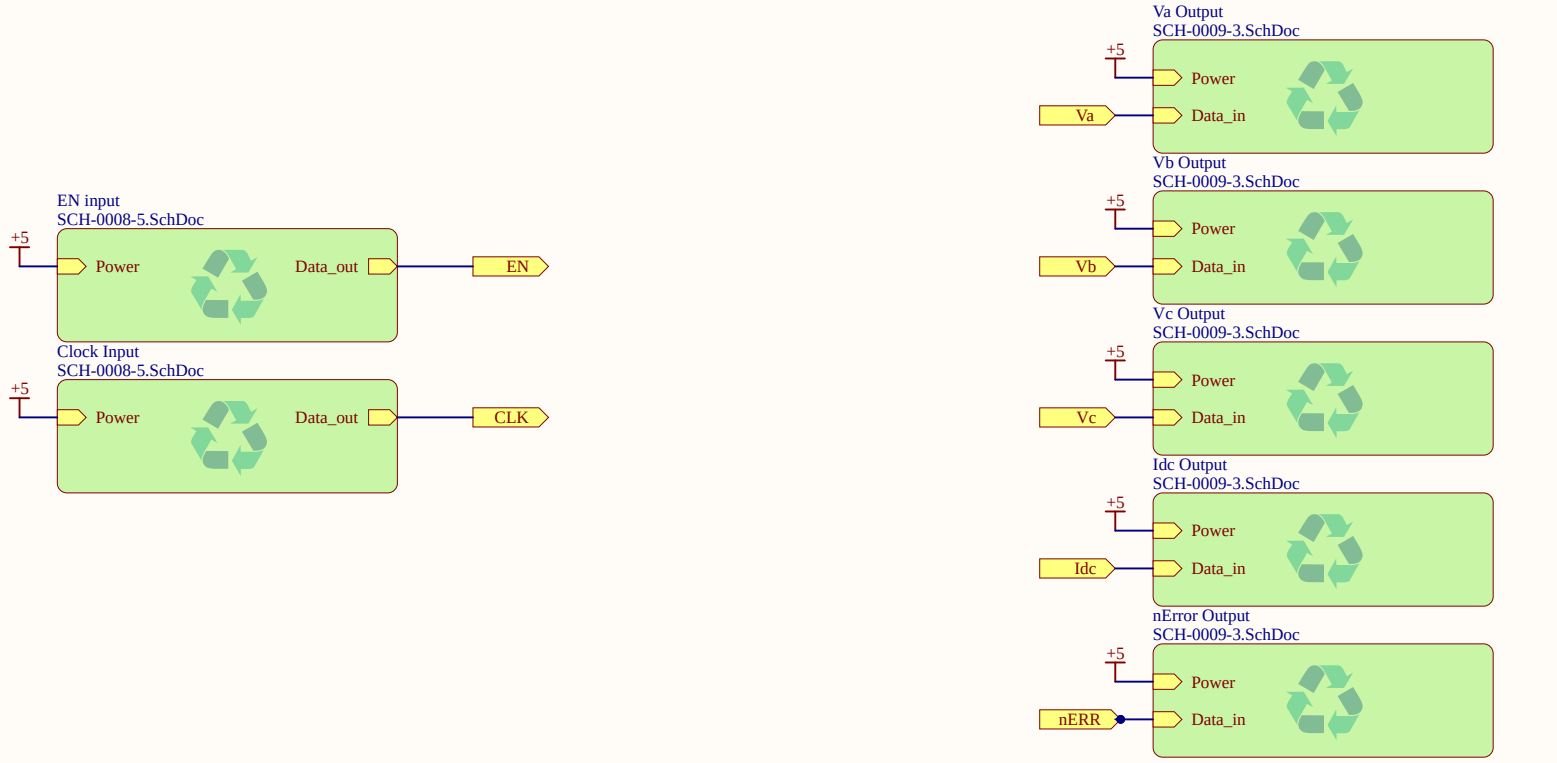
Title		
Size A4	Number	Revision
Date: 10/28/2024		Sheet of
File: C:\Users\..\Safety.SchDoc		Drawn By:



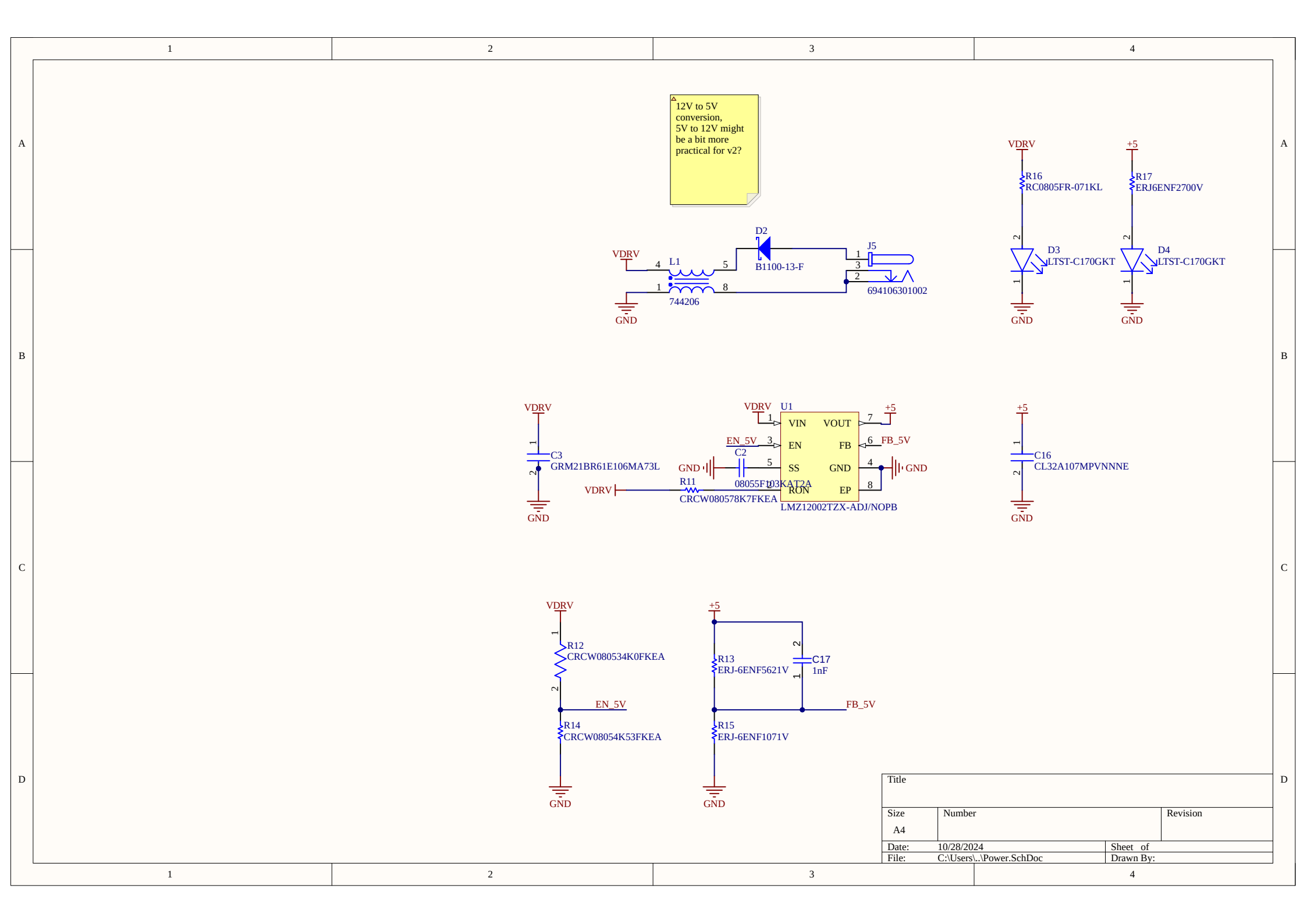
Title		
Size: A4	Number	Revision
Date: 10/28/2024		Sheet of
File: C:\Users\..\ResetButton.SchDoc		Drawn By:



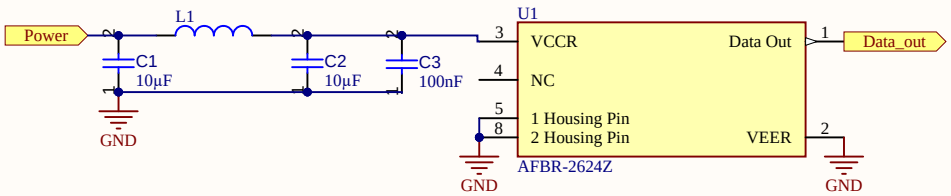
Title		
Size: A4	Number	Revision
Date: 10/28/2024		Sheet of
File: C:\Users\..\LEDs.SchDoc		Drawn By:



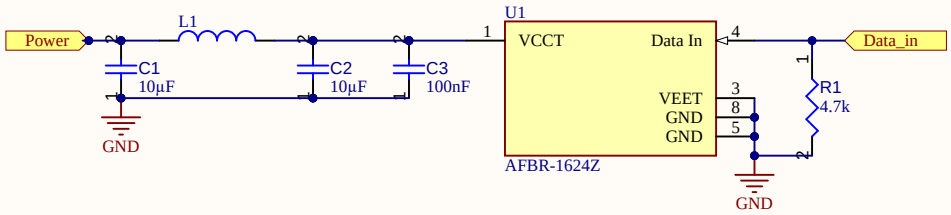
Title		
Size: A4	Number	Revision
Date: 10/28/2024		Sheet of
File: C:\Users\..\Communication.SchDoc		Drawn By:



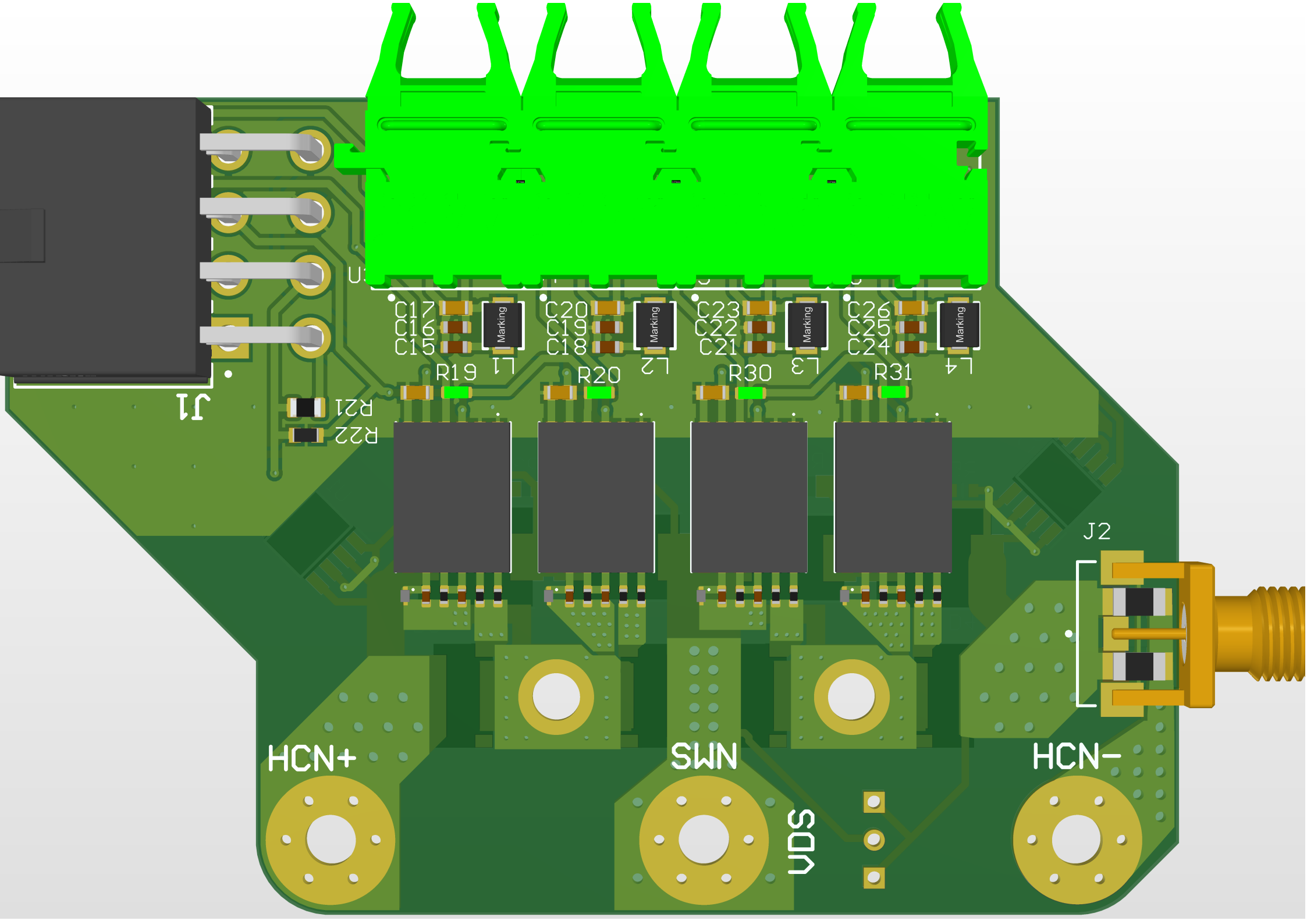
Title		
Size: A4	Number	Revision
Date: 10/28/2024		Sheet of
File: C:\Users\..\Power.SchDoc		Drawn By:

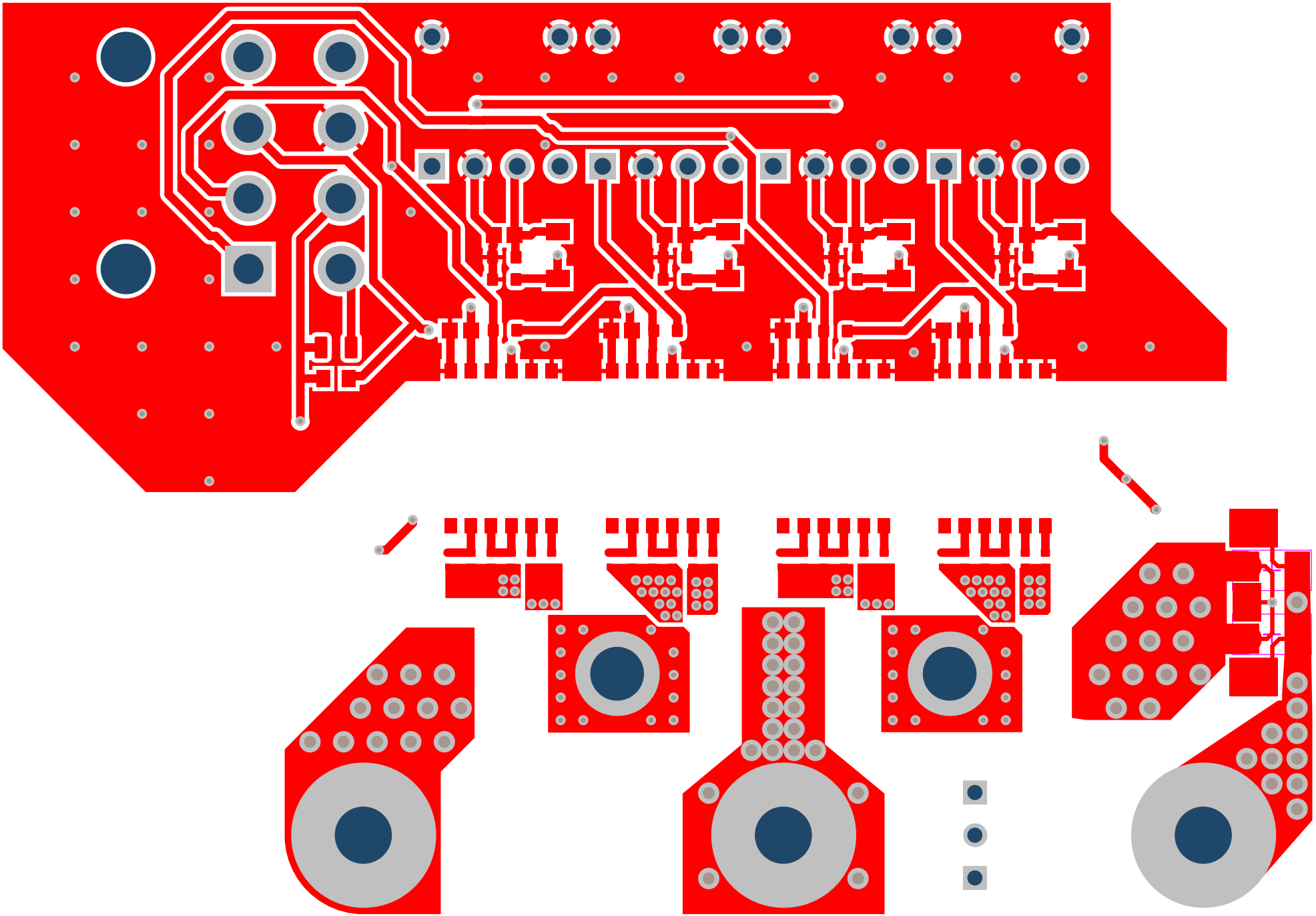


Title			
Size A4	Number		Revision
Date: 10/28/2024		Sheet of	
File: C:\Users\..\SCH-0008-5.SchDoc		Drawn By:	

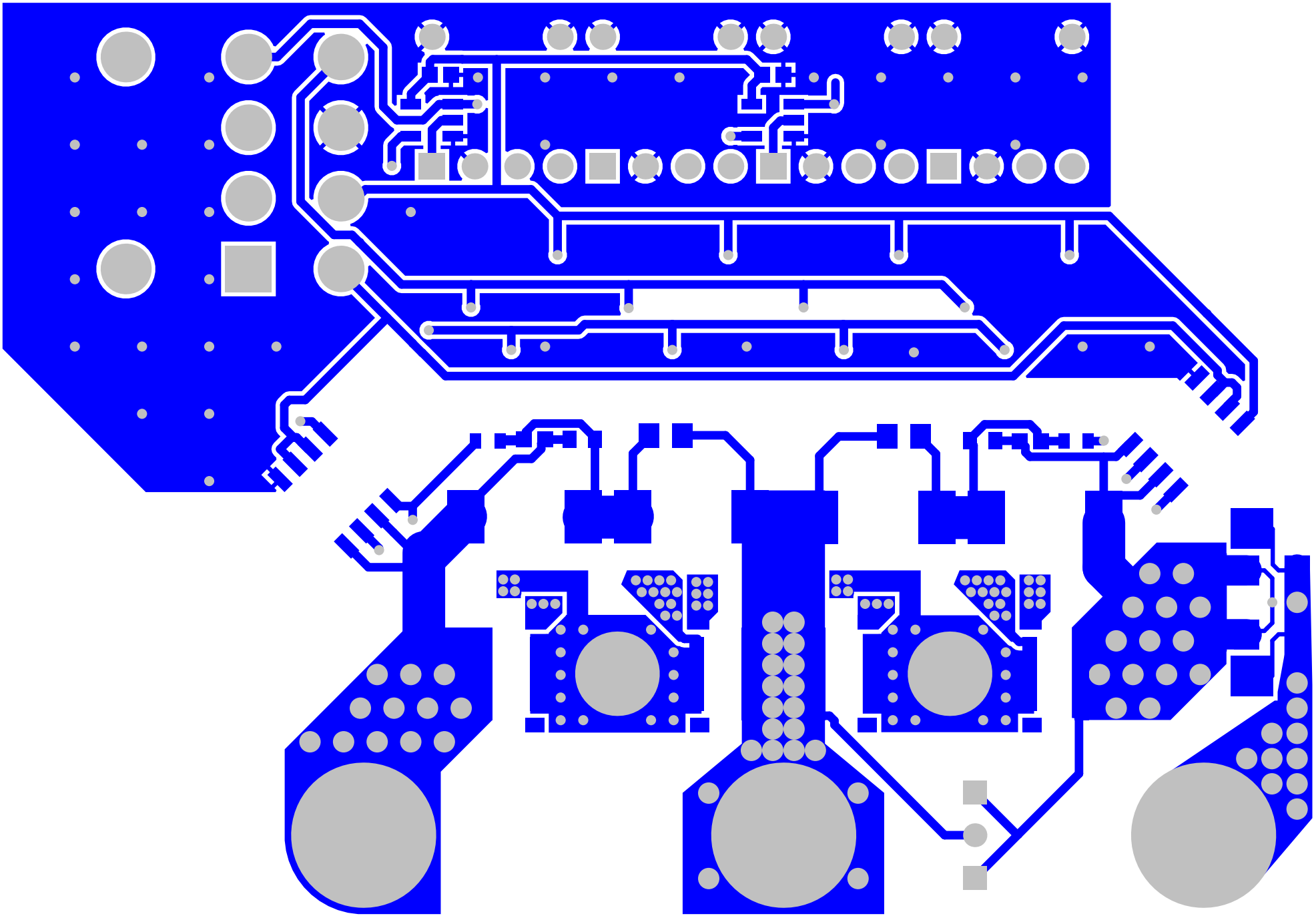


Title			
Size A4	Number		Revision
Date: 10/28/2024		Sheet of	
File: C:\Users\..\SCH-0009-3.SchDoc		Drawn By:	


J1
R21
R22
C17
C16
C15
Marking
L1
R19
C20
C19
C18
Marking
L2
R20
C23
C22
C21
Marking
L3
R30
C26
C25
C24
Marking
L4
R31
J2
HCN+
SWN
HCN−
VDS



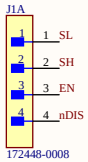
U3
U4
U5
U6
C17
C16
C15
C20
C19
C18
C23
C22
C21
C26
C25
C24
R19
L1
R20
L2
R30
L3
R31
L4
J1
R21
R22
J2
HCN+
SWN
HCN-
VDS

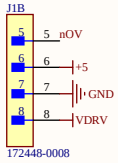


REVISION	DESCRIPTION	DATE	APPROVED

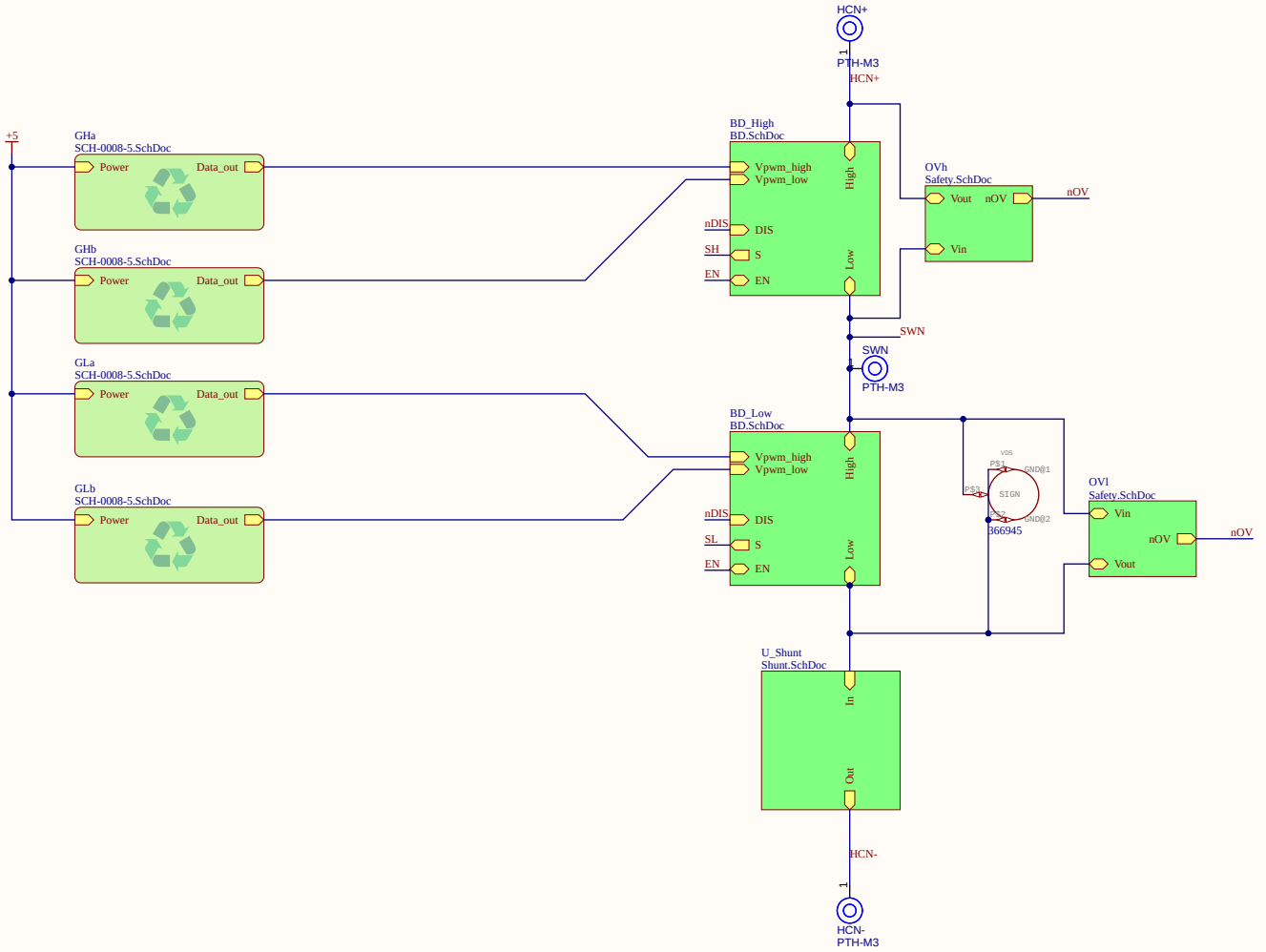
EN Is the ENable signal for the gate drivers. In this case its mainly used as a fault pin

nDIS Is a "not Disabled" signal. It is used with an and gate on the switching legs, and with a nand gate on the input stage. This is because the ideal safe state





V2 Note:
- GaN can be placed closer to the gate driver circuitry



APPROVALS	DATE
ENG: *	--/--/--
DSN: *	--/--/--
CHK: *	--/--/--
REFERENCE DOCUMENTS	
BOM: <BOM DOC NO>	
ASSY DWG: <ASSY DWG NO>	
FAB DWG: <FAB DWG NO>	
PCB DWG: <PCB DWG NO>	

PROJECT: *

Altium

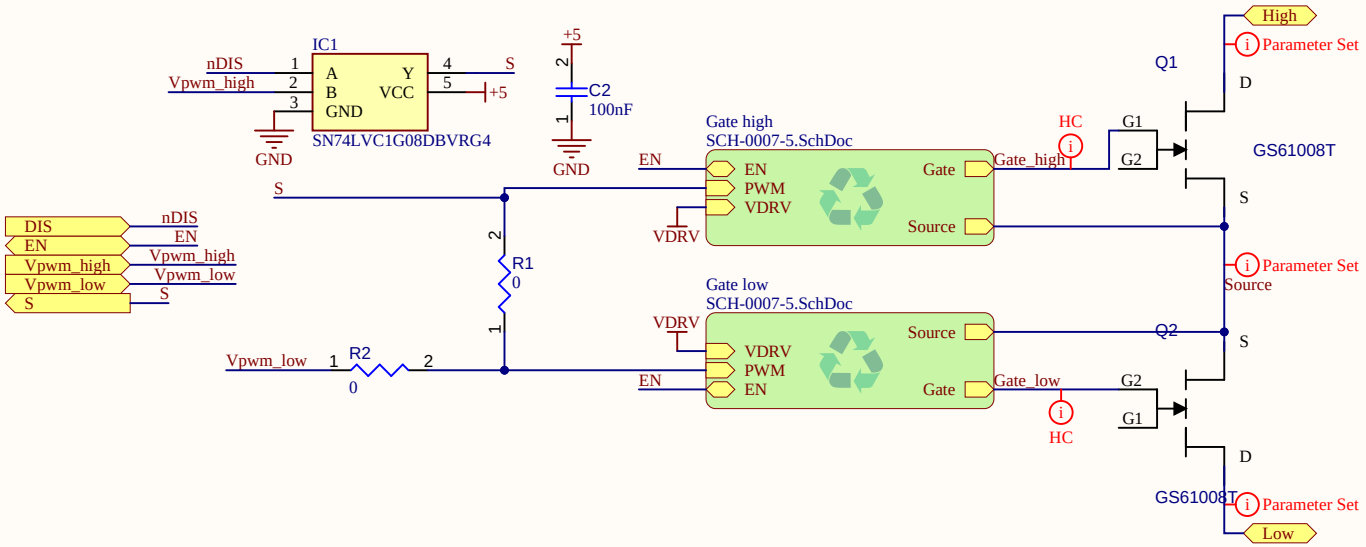
PROJECT REVISION: 5b6a38441da7b75ca923 DOCUMENT REVISION: 5b6a38441da7b75ca923 DESIGN ITEM: 5b6a38441da7b75ca923 1fb0b5e7379e3

TITLE: *

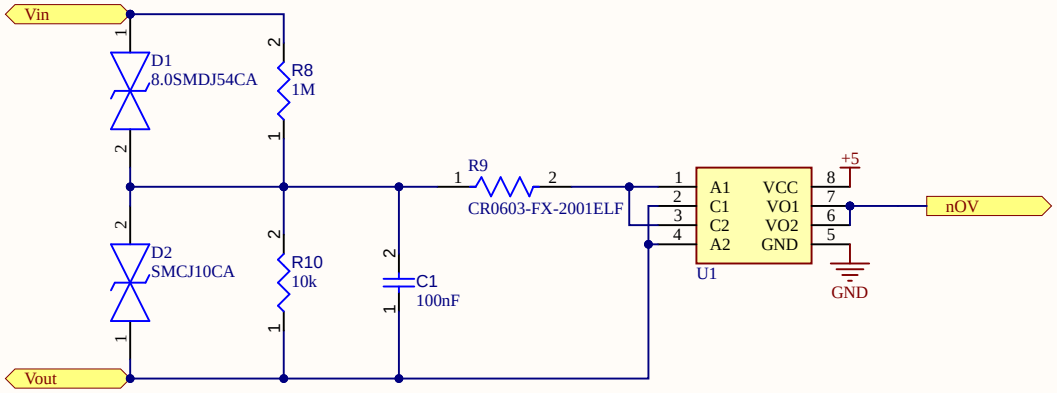
SIZE	CAGE CODE	DWG NO.	REV
B	?????	<SCH DWG NO>	

SCALE: FILE NAME TopLevel.SchDoc SHEET 1 OF 6

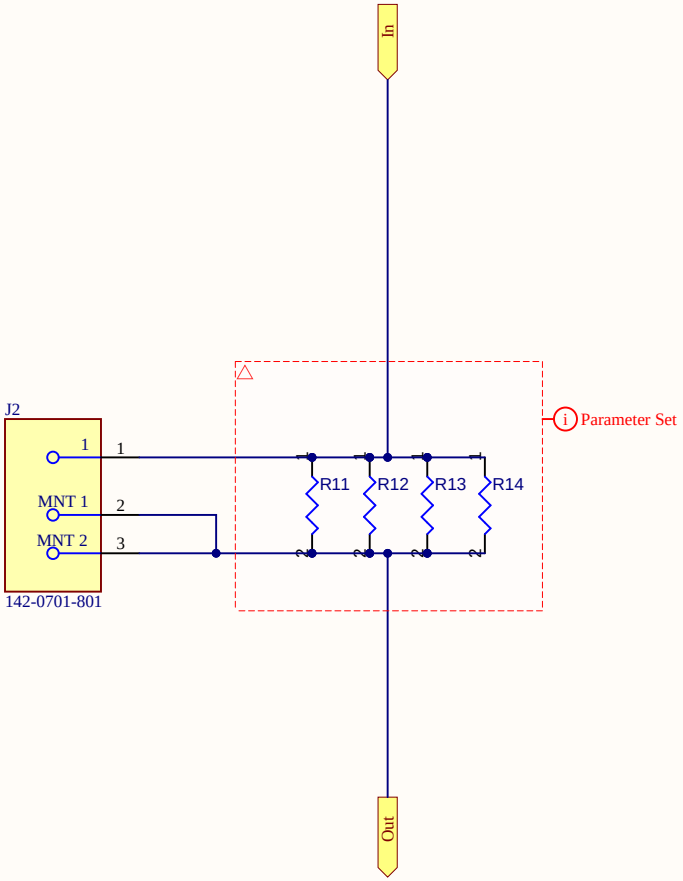
<SCH DWG NO> REV 1 SHT.



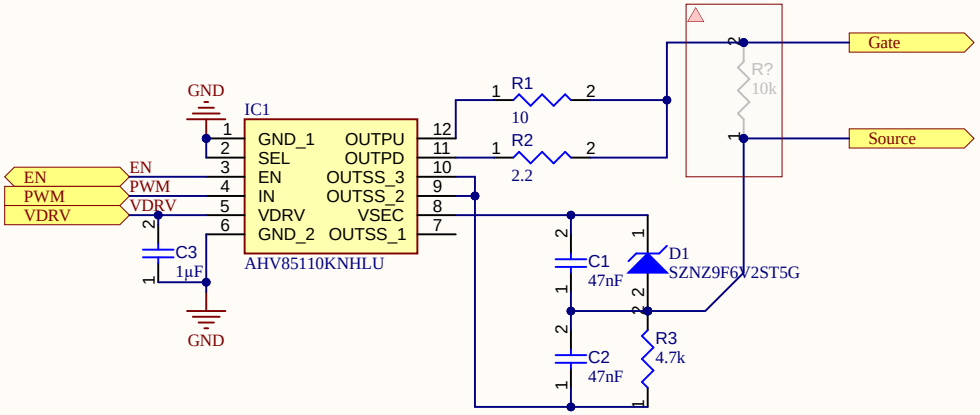
Title		
Size A4	Number	Revision
Date: 10/28/2024		Sheet of
File: C:\Users\..\BD.SchDoc		Drawn By:



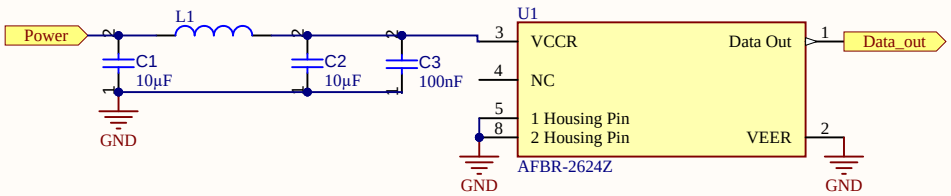
Title		
Size: A4	Number	Revision
Date: 10/28/2024		Sheet of
File: C:\Users\..\Safety.SchDoc		Drawn By:



Title		
Size: A4	Number	Revision
Date: 10/28/2024		Sheet of
File: C:\Users\..\Shunt.SchDoc		Drawn By:



Title		
Size A4	Number	Revision
Date: 10/28/2024		Sheet of
File: C:\Users\..\SCH-0007-5.SchDoc		Drawn By:



Title			
Size A4	Number		Revision
Date: 10/28/2024		Sheet of	
File: C:\Users\..\SCH-0008-5.SchDoc		Drawn By:	