Rapid thermal processed high-mobility IO:H films and their application to c-Si solar cells featuring TOPCon passivating contacts

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by

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Preface

I would like to thank my supervisors Dr. Zhirong Yao and Prof. Dr. Olindo Isabella for giving me the opportunity to take on in this project. Their detailed support has helped me achieve the goals that were set before the start of the project and to make adjustments to the project plan based on discoveries made during experiments. During this project, I have had the opportunity to learn from experts in the field of c-Si solar cell development and to operate equipment allowing for the development and characterization of materials involved. Taking on this project and working as a Master Thesis student in the high-thermal budget c-Si team of the Photovoltaic Materials and Devices research group has taught me about the theory behind the development of Hydrogenated Indium Oxide thin films. In addition, the challenge of application to c-Si solar cells featuring TOPCon passivating contacts required studying the theory of passivation and band alignment.

Secondly, I would like to thank the professors, post-docs and technicians of the PVMD group and the staff of the Else Kooi Laboratory and Kavli NanoLab who have helped me conduct my research. I would like to thank Prashand Kalpoe and Federica Saitta for helping me determine the starting point for IO:H development by sharing their results.

Lastly, I would like to thank my friends and family that have supported me during my time as a student of the Master of Science program of Sustainable Energy Technology at Delft University of Technology.

Hugo Korthals Altes
Delft, December 2025

Summary

High-mobility Hydrogenated Indium Oxide (IO:H) thin films were developed and the influence of the post-deposition treatment process on the opto-electronic properties of these thin films was investigated. The electron mobility of the IO:H film reached the value of 146 cm^2/Vs after annealing. These IO:H layers were deposited using magnetron sputtering and annealed utilizing Rapid Thermal Processing, involving short exposure to temperatures between 400 and 700 °C, instead of the commonly used annealing methods that involve longer exposure to a lower and stable temperature.

Since application of Transparent Conductive Oxides (TCOs) can help decrease the electrical and optical losses in c-Si solar cells featuring Tunnelling Oxide Passivating Contacts (TOPCon), the influence that the deposition and post-deposition treatment of IO:H have on the passivating qualities of the contacts is investigated. Depositing the thin films on symmetrically passivated c-Si wafers damages the passivating quality of the contacts significantly, which can partially be recovered by post-deposition annealing. The degradation of the passivation quality can be explained by the breaking of Si-Si bonds and the creation of defect states as a result of particle bombardment. Lowering the power density during deposition has proven to be crucial for mitigation of the passivation damage. A maximum power density of 0.62 W/cm^2 ensures minimal passivation losses in the contact during deposition and allowed for recovery of most of the damage after post-deposition annealing. Due to in-diffusion of dopants in the contact, the temperature during annealing must be limited to 550 °C.

Cox-Strack measurements of symmetrically passivated c-Si wafers with TOPCon/IO:H contact stacks reveal high contact resistivity, mainly induced by oxygen adsorption when IO:H is deposited at a low power density. The formation of an electron barrier causes a low field-effect driven mobility for electrons travelling from the contact to the TCO. Therefore, reducing the thickness and the carrier concentration in the buffer layer of an IO:H bi-layer is crucial for limiting the contact resistivity. Further literature study revealed that inserting a small fraction of ITO between IO:H and silver is necessary to reduce the contact resistivity and therefore improve the cell's performance.

Contents

1
Introduction

1.1. Renewable energy sources

Through the years, the evolution of energy generation technology using the photovoltaic effect has become increasingly valuable to help meet the global energy demand. The capacity of solar power is expected to surpass the installed power capacity of coal in 2027, after which solar power will become the largest source of electricity in the world[1], see figure 1.1. In the pursuit of lower levelized cost of electricity, researchers and developers look for methods to decrease the cost of materials used to produce solar cells and increase energy conversion efficiency.

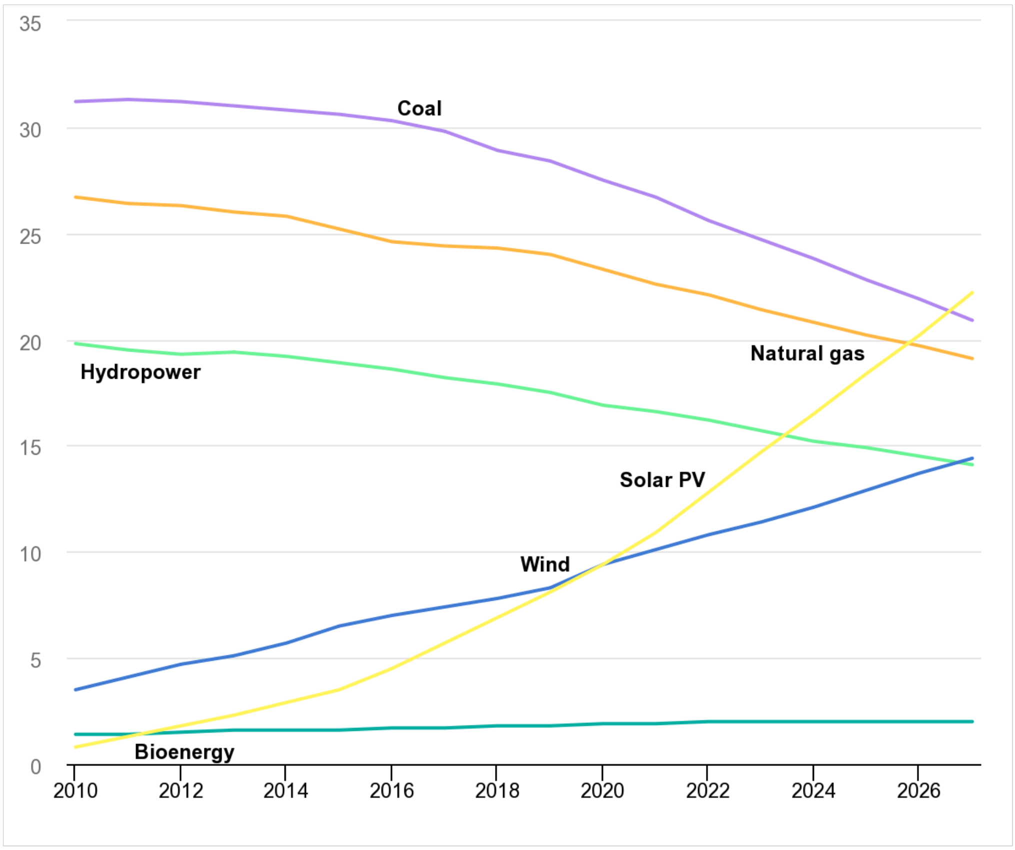


Figure 1.1: Trend and forecast of the global share (%) of cumulative power capacity by technology, 2010-2027, predicted by the International Energy Agency in 2022[1].

1.2. Future of solar cells

In the past, most of the c-Si solar cells have been produced in the Passivated Emitter Rear Cell (PERC) line. But these cells reached their efficiency limit. To keep increasing the efficiency of solar cells, widespread interest goes to research and development of silicon heterojunction and Tunnelling Oxide Passivating Contact (TOPCon) solar cells. The production of TOPCon solar cells has grown exponentially due to the passivating qualities of the rear contact and the compatibility of these cells with the equipment already involved in the production of PERC solar cells[2] and the latter is phased-out, see figure 1.2. Only a few extra steps are required in the production process of i-TOPCon solar cells, which involves application of the Tunnelling Oxide Passivating Contact to the rear side.

As the next generation of solar cells, along with the development of Interdigitated Back-Contact (IBC) solar cells, which consists of both the n-type and p-type carrier-specific passivating contact (CSPC) on the rear side, widespread interest goes to research and development of multi-junction solar cells. By separating light absorption based on the wavelength of photons, the two subcells of these solar cells can cumulatively convert a larger fraction of the Sun's energy to electricity than silicon-only solar cells[3]. The perovskite in the upper cell is used to reduce thermalization losses during the absorption of photons in the high-energy region of the spectrum. The crystalline silicon in the bottom cell absorbs the lower-energy photons that are transmitted by the perovskite of the upper cell.

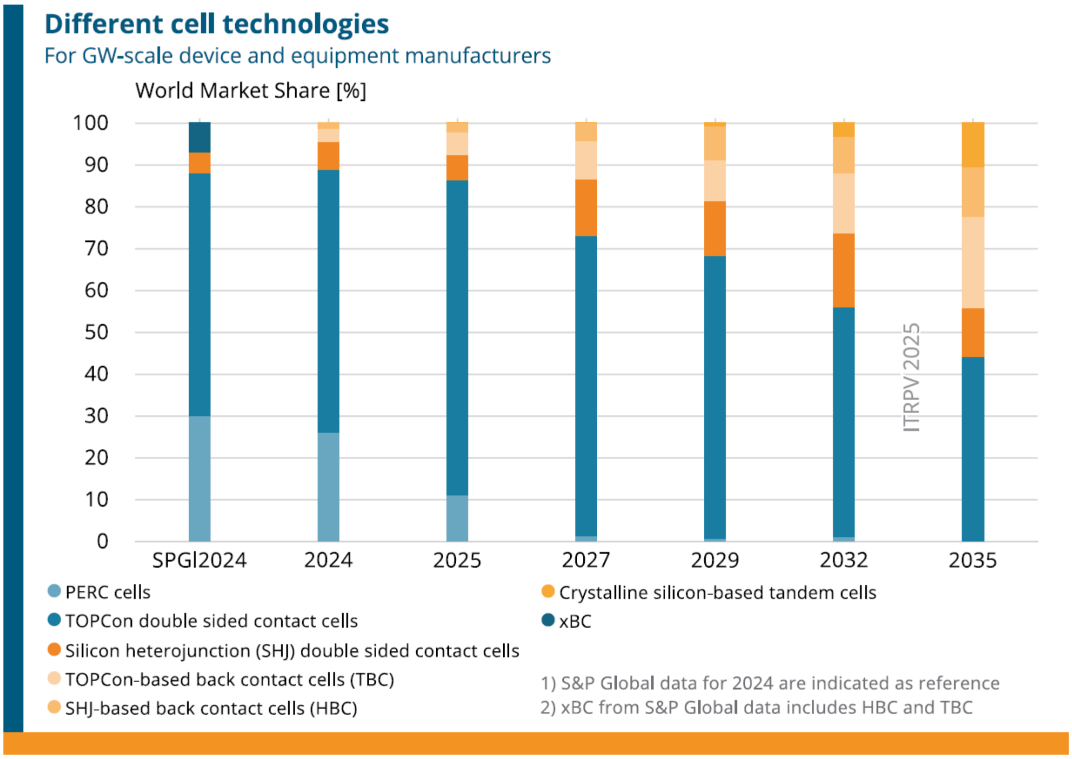


Figure 1.2: Market share for different cell technologies from GW-scale manufacturers[4].

Multi-junction, or tandem solar cells, can be connected using a 2, 3 or 4-terminal configuration. By using a 4-terminal configuration, the subcells can be operated separately and the problem of current mismatching, which restricts the optimization of perovskite, specifically the bandgap, can be avoided. A visual representation of the light absorption in the subcells of a 4-terminal tandem solar cell is given by the left side of figure 1.3. The low-energy photons are represented by the yellow-red part of the incoming radiation in the figure. In a 2-terminal configuration, holes collected at the rear side of the upper cell and electrons collected at the front side of the bottom cell meet in the recombination junction. The figure shows why low sheet resistance and large-wavelength transparency are required in the front contact of the bottom cell (4T) and in the recombination layer (2T). In IBC solar cells, due to the fact that both CSPCs are located separately on the rear side, metal fingers are several centimeters long and benefit from a low sheet resistance in the contact.

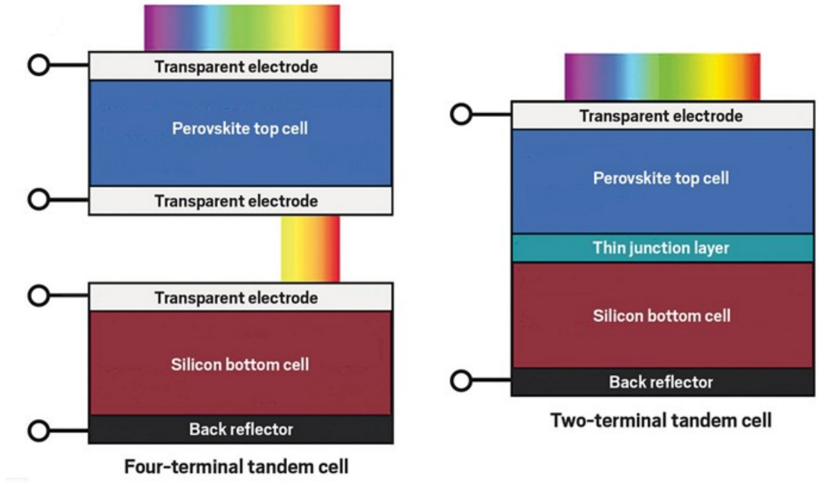


Figure 1.3: Schematic representation of a 4-terminal and a 2-terminal perovskite-silicon tandem solar cell.

1.3. High-thermal budget CSPCs and Transparent Conductive Oxides

Both high- and low-thermal budget CSPCs, or a hybrid version[5], are optional for the passivation of IBC solar cells and the bottom cell of multi-junction solar cells. For application of the TOPCon passivating contact, challenges need to be overcome. The polycrystalline silicon (poly-Si), which is used in i-TOPCon solar cells, shows high parasitic absorption in the near-infrared (NIR) part of the solar spectrum. Therefore R&D groups have developed more transparent options to replace poly-Si in high-thermal budget CSPCs.

Efforts have been made to significantly decrease the parasitic absorption in the NIR-region by alloying poly-Si with oxygen to form polycrystalline silicon oxide (poly-Si(O_x))[6]. Due to their metal-like conductivity and high transmittance for visible light and photons in the near-infrared spectrum, Transparent Conductive Oxides (TCOs) are used to decrease the sheet resistance of the contact. In addition, depending on the solar cell architecture and the location of the TCO, the thin films can function as an anti-reflective coating (ARC) and allow the use of low-temperature metallization techniques with minimal loss of passivating quality.

1.4. Project objectives and research questions

Problems arise when depositing TCOs with the use of magnetron sputtering, a technique that is often used but in the case of application to passivating contacts damages the passivating quality. In this project, Hydrogenated Indium Oxide (IO:H) and its suitability for application to c-Si solar cells featuring TOPCon passivating contacts was studied. IO:H was chosen as the TCO for its excellent opto-electronic properties. Since IO:H is deposited directly on poly-Si(O_x)), investigation of the effect of the deposition and post-deposition treatment on the passivating quality is required. The goal is to protect the passivating contact during the synthesis of IO:H while ensuring low parasitic absorption and sheet resistance. Studying the band alignment of the contact is also necessary, which requires investigating the influence of IO:H thin films on the contact resistivity. Special attention has been paid to the post-deposition annealing method called Rapid Thermal Processing (RTP), which significantly shortens the process step and exposes the thin film to high temperatures.

Below, the research questions that will be answered with the help of the experiments of chapter 3 are presented.

1. What is the influence of the peak temperature during the post-deposition treatment on the opto-electronic properties of IO:H when using Rapid Thermal Processing?

2. What is the influence of the power density during deposition of IO:H and the peak temperature during post-deposition annealing on the passivating quality of TOPCon passivating contacts?

3. What is the influence of the thickness of a protective IO:H sublayer on the passivating quality of TOPCon passivating contacts?

4. What is the influence of the thickness of a protective IO:H sublayer on the contact resistivity of the TOPCon/IO:H contact stack?

Because the three aforementioned solar cells are different, the requirements, regarding both internal (microstructure) and external (thickness) parameters, for the high-thermal budget n-type passivating contact and the TCO in each of these are different as well. Nevertheless, improvement or optimization of the passivation, opto-electronic properties and band alignment in the investigated contact stack is beneficial to the conversion efficiency in each of the discussed solar cell types.

2

Theoretical background

2.1. Fundamental theory of c-Si solar cells

In this section, the fundamental principles of power generation with the use of c-Si solar cells are explained. Energy conversion with the help of the photovoltaic effect is explained in paragraph 2.1.1. In paragraph 2.1.2, the mechanisms that facilitate separation of generated electron-hole pairs are explained. Paragraph 2.1.3 explains what roles the short-circuit current density, open-circuit voltage and fill-factor of the cell play in photovoltaic devices. Lastly, paragraph 2.1.4 can be read to understand the different mechanisms that cause recombination of electron-hole pairs and how recombination can be avoided.

2.1.1. Photovoltaic energy conversion

Every second, on average 1360 J/m^2 arrives at the top of the Earth's atmosphere in the form of solar radiation. This energy is distributed over a spectrum of photon wavelengths λ and, as a result of attenuation by the atmosphere, the fraction of incident photons that reach the Earth's surface depends on their wavelength. So does the photon energy E_{photon}, see equation 2.1, in which h and c represent Planck's constant and the speed of light, respectively. Figure 2.1 shows the energy density distribution of the solar spectrum and how the photon wavelength determines the attenuation in the atmosphere.

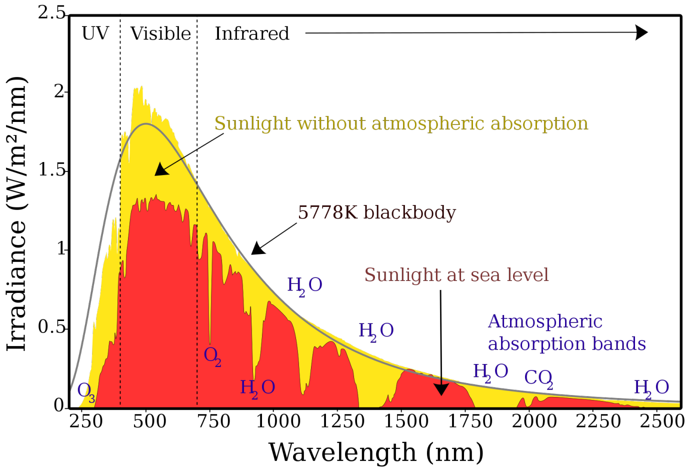
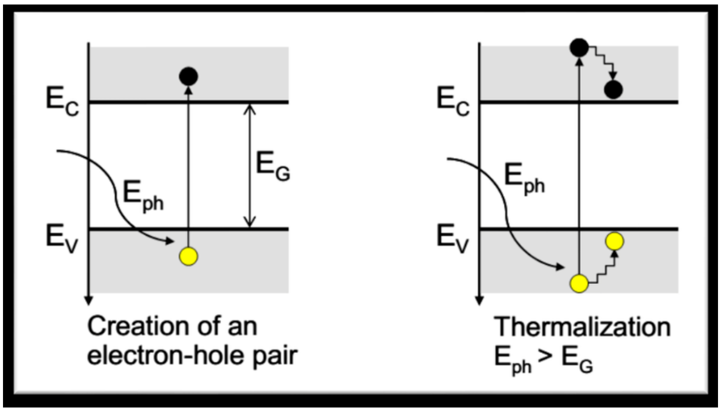


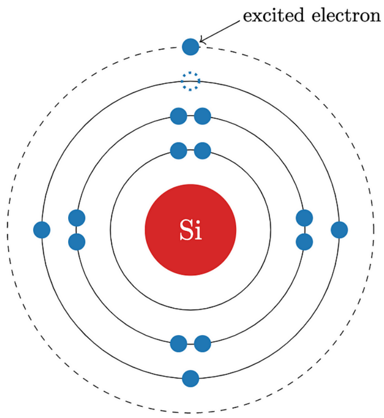
Figure 2.1: The spectrum of solar radiation at the top of Earth's atmosphere (yellow) and at sea level (red).

$$E_{photon} = \frac{hc}{\lambda} \tag{2.1}$$

On a clear day, a maximum of 1 kW/m^2 direct normal irradiation reaches the Earth's sea level. In the visible and near-infrared part of the spectrum, the irradiance is highest and therefore the most energy can be generated by absorbing these photons. When a photon reaches the active layer of a solar module, depending on the amount of energy it carries, it can be either absorbed, transmitted, or reflected. When a photon with sufficient energy is absorbed by the material, the electron leaves its energy state in the valence band and excites to the conduction band. The energy required is equal to or larger than the difference between the conduction band minimum and the valence band maximum. A hole is left behind in the valence band. If the energy of the photon is larger than required for absorption, excess energy of the photon will be released into the lattice. This is called thermalization, see the right half of figure 2.2a. A schematic representation of the resulting band occupation after this excitation is shown in figure 2.2b. In the case of crystalline silicon, a photon energy of at least 1.12 electronvolt (eV) is required for this electron-hole pair generation, which corresponds to a photon wavelength of 1100 nm and is low enough for absorption of photons in the visible and near-infrared (VIS-NIR) spectrum.



(a) The excitation of an electron to the conduction band by photon absorption and the release of excess energy.



(b) A schematic representation of the silicon atom and its rings

Figure 2.2: Schematic representation of the excitation of an electron and the resulting electron-state occupation in silicon

2.1.2. Electron-hole pair separation

As stated in the previous paragraph, upon photon absorption the electron leaves the valence band to occupy a state in the conduction band. As a result, an excess concentration of both holes and electrons is present in the semiconductor lattice. By separating the holes and electrons, the energy can be extracted from the illuminated crystalline silicon. The hole and the electron must travel in different directions. The movement of a hole is also interpreted as the movement of an electron in the opposite direction. With the use of certain techniques, layers that facilitate carrier-specific conductivity can be applied so that a current is created. In order to minimize electrical resistance of the contact layers, their energy bands are aligned. A layer with a relatively large concentration of one type of carrier, either electrons or holes, will limit the photo-generated current. By electrically connecting both ends, a current will flow as long as the active layer is subject to illumination. A schematic representation of the electron and hole pathways in a solar cell can be found in figure 2.3.

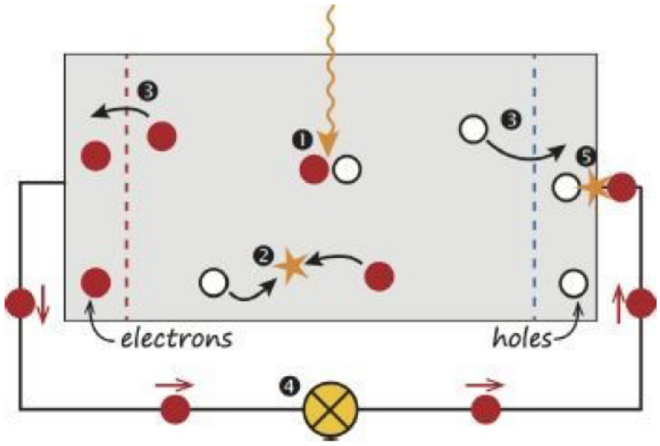


Figure 2.3: A schematic representation of the (1) generation, (3) separation and (5) recombination of an electron-hole pair after being generated through the photovoltaic effect. At (4), the electron passes a load where it releases its energy, after which it can easily recombine with a hole. Section (2) of the figure represents recombination before the electron-hole pair can transfer energy to the load.

2.1.3. Open-circuit voltage, short-circuit current density and fill-factor

To predict the efficiency of the solar cell the open-circuit voltage, short-circuit current density and fill-factor are used.

Open-circuit voltage is defined as the voltage between both sides of the active region when no electric current is possible, i.e. the electrical resistance is infinitely high. By applying contacts to the active material that facilitate carrier-specific conductivity, a high open-circuit voltage can be created. The open-circuit voltage, which is often presented in units of mV, determines the maximum energy electrons can carry.

The short-circuit current density is defined as the current per unit of solar cell surface area that is generated when no electrical resistance is present between both sides of the active region. The short-circuit current density is determined by the amount of photons reaching the active material that have enough energy to excite an electron from the valence band to the conduction band. By applying contact layers with a low absorption coefficient for photon wavelengths in the visible and near-infrared spectrum (VIS-NIR), the short-circuit current density can be optimized.

As the load resistance gradually changes - from zero (short-circuit state) to infinity (open-circuit) - so do the current through the load and the measured voltage. The exact shape of the so-called IV-curve, see figure 2.4, depends on the internal resistance of the solar cell. Where the product of the current and voltage reaches its maximum, the measured power is called the maximum power point. The fill-factor is defined as the ratio between the maximum power density that can be delivered by the solar cell and the product of the short circuit current density and the open circuit voltage. A high fill-factor is therefore crucial for the conversion efficiency of a solar cell. By decreasing the internal electrical resistance of the solar cell, the fill-factor can be increased. Two important contributors to the internal resistance of a c-Si solar cell are the sheet resistance of the contacts, determined by the lateral conductivity and thickness of the contact layers, and the contact resistivity, which is determined by the band alignment in the contact stack.

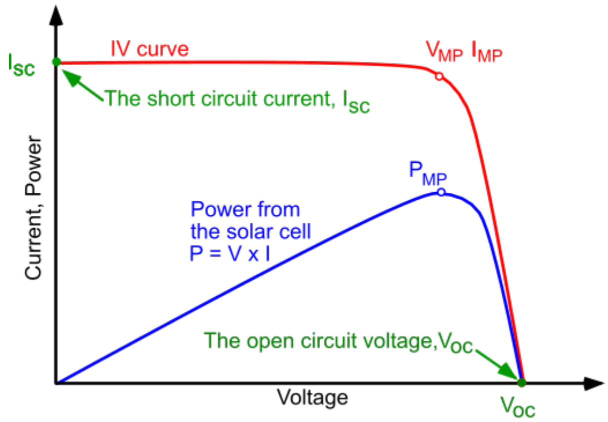


Figure 2.4: An example of the current-voltage and power-voltage curves of a solar cell. The maximum power is reached at the maximum power point P_{MP}, at which point the voltage and current are V_{MP} and I_{MP}, respectively.

2.1.4. Recombination mechanisms

Not all generated electron-hole pairs can be separated and contribute to the current flow. There are three recombination mechanisms that limit the current density and are therefore detrimental to the performance of the cell. These mechanisms are called: Radiative, Auger and Shockley-Read-Hall recombination. For each of these three mechanisms, energy generated is lost. Figure 2.5 displays the interactions involved in the recombination mechanisms.

- Radiative recombination occurs when an electron moves back into a state in the valence band and releases the energy in the form of a photon. The photon has an energy equal to the difference between the conduction band minimum and the valence band maximum. This recombination type mainly occurs in materials with a *direct* bandgap and therefore is negligible in crystalline silicon solar cells.

- For Auger recombination, three charge carriers are involved: either two electrons and one hole or one electron and two holes. Just like with radiative recombination, an electron and a hole recombine. In the case of two electrons and one hole, the excess energy is transferred to the second electron in the conduction band, which is excited further into the conduction band. Through thermalization, energy transfer to the crystal lattice, the second electron releases the energy and moves back down to the conduction band minimum. For Auger recombination, a high concentration of carriers is required, caused by heavy doping of the material or high injection through concentrated sunlight.

- Shockley-Read-Hall (SRH) recombination is caused by defects in the crystal structure. In a crystal lattice without any defects, there are no energy states inside the bandgap available to electrons. However, defects or impurities in the lattice create a 'trap state', an energy level inside the bandgap that can be occupied by electrons. Once a carrier is trapped in this energy state, it can more easily recombine with a carrier of the opposite charge. It is therefore crucial to limit the amount of defects in the crystalline silicon or contact layers.

The degree to which a defect state contributes to the SRH recombination depends on the location of the defect state in the band gap. When the defect state is close to one of the band gap edges, the contribution to SRH recombination is smaller than when it is found close to the middle of the band gap. For example, an electron found in a defect state close to the conduction band minimum is more likely to be re-emitted into the conduction band than an electron found in a defect state close to the middle of the bandgap.

Sections 2.2 and 2.3 will present the relevant theory behind TOPCon passivating contacts and the development of Hydrogenated Indium Oxide thin films for application to these contacts.

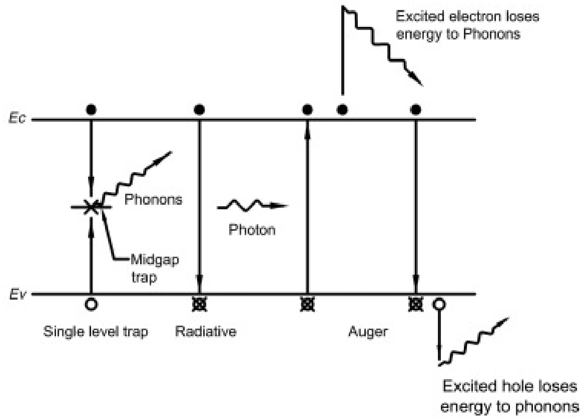


Figure 2.5: The three possible recombination mechanisms in the bulk material.

2.2. C-Si solar cells featuring Tunnelling Oxide Passivating Contacts (TOPCon)

TOPCon passivating contacts are known for their excellent passivating quality when applied to c-Si wafers. By facilitating one-way electron transport to the contact and blocking holes, see the band diagram of figure 2.6, a high open circuit voltage can be enabled. The carrier-specific conductivity is created by separating the either n- or p-doped poly-Si(O_X) layer from the crystalline silicon with a silicon oxide layer. This silicon oxide layer does not facilitate any energy states electrons and holes can occupy and therefore requires the carriers to tunnel and find an available energy state on the other side of the silicon oxide, i.e. in the contact. Because the energy bands in the n-type contact are slightly lowered, electrons can easily tunnel through the silicon oxide, and hole mobility is low. With the help of the carrier-specific conductivity, electrons are gathered in the contact while the hole concentration, and therefore the carrier recombination, is low. In the case of p-type TOPCon, the carriers are swapped in terms of mobility.

The implied open circuit voltage of c-Si wafers featuring n-TOPCon passivating contacts is reported to reach 728 mV[7]. Properties of the phosphorous-doped polycrystalline silicon contact, such as doping level and the crystallinity determine the level of passivation.

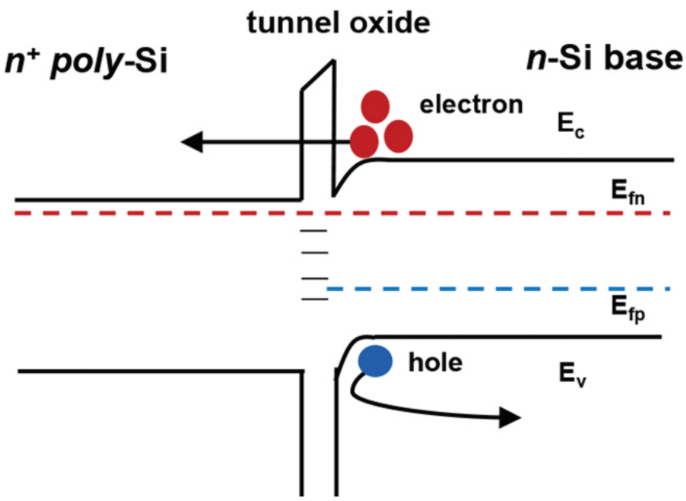


Figure 2.6: A band diagram of a c-Si wafer with an n-TOPCon passivating contact structure[7]. Note: the material represented by the bandgap on the left side of this figure typically belongs to P-doped polycrystalline silicon. The bandgap of the oxygen-alloyed variant used for experiments in this project is significantly larger, further decreasing hole mobility.

2.3. Transparent Conductive Oxides

Transparent Conductive Oxides are direct-bandgap semiconductors that can be utilized for their high optical transmittance for visible light and photons in the near-infrared (NIR) region and their metal-like conductivity. These qualities allow for minimal parasitic absorption while improving electric performance of the cell. The optical absorptance and the electrical conductivity of the TCO thin films are interdependent as both variables are linearly proportional to the concentration of carriers N_e, see the equations for conductivity σ and free carrier absorption α_{fca}, respectively 2.2 and 2.3[8][9]. For photons with an energy smaller than the bandgap of the TCO, a high carrier concentration results in a high free-carrier absorption. A low carrier concentration results in low electrical conductivity.

2.3.1. Hydrogenated Indium Oxide

Here, the electron mobility μ of the TCO comes into play. Since only the electrical conductivity increases with the electron mobility and the free-carrier absorption does not, a high electron mobility can provide a good trade-off position for the electrical conductivity and optical transmittance. Hydrogenated Indium Oxide (IO:H) is a TCO with a high electron mobility. When IO:H was first reported about by Koida et al. in 2007, it reached electron mobility values over 100 cm^2/Vs[10], making it one of the most promising TCOs. Indium-Tin-Oxide (ITO) is among the most common TCOs applied to solar cells. However, it was reported to only reach values of electron mobility up to 40 cm^2/Vs, which in theory gives ITO a disadvantage compared to IO:H. More recently, the electron mobility of IO:H was reported to reach 160 cm^2/Vs[11], which currently remains the highest reported value.

$$\sigma = q\mu N_e \tag{2.2}$$

$$\alpha_{fca} = \frac{\lambda^2 q^3 N_e}{4\pi^2 \epsilon_0 c^3 n (m_e^*)^2 \mu_{opt}} \tag{2.3}$$

In addition to the ones previously mentioned, the variables involved in equations 2.2 and 2.3 are the elementary charge q, the wavelength of photons λ, the vacuum permittivity ϵ_0, the speed of light c, the refractive index n, the effective electron mass m_e^* and the optical mobility μ_{opt}.

The high transmittance of indium oxide-based TCOs is a result of the large band gap, which is larger than 3 eV. Due to the presence of hydrogen, which acts as an electron donor, the Fermi level in IO:H is raised above the conduction band minimum. Because the energy states below the Fermi level are occupied, the phenomenon also known as the Moss-Burstein Shift requires electrons excited from the valence band to find an energy state above this level and therefore absorb photons that carry the increased amount of energy. As a result, a larger part of the solar spectrum is transmitted by the TCO.

2.3.2. Synthesis of IO:H

Application of IO:H is commonly done by means of Radio-frequency (RF) magnetron sputtering and post-deposition annealing. Magnetron sputtering utilizes assisted ionization of gaseous argon, after which the highly energetic, positively charged ions are directed towards the cathode, where the target is located. Upon impact, the target material is ejected and directed towards a substrate. At the surface of the substrate, a thin film will grow, the composition of which is determined by the target material and gasses in the process chamber. However, these sputtered particles also damage the substrate, depending on sputtering conditions and the surface of the substrate. In figure 2.7, an overview of the processes involved in IO:H deposition can be found.

The conditions in which the thin films are deposited determine the composition and microstructure of the TCO. A high oxygen partial pressure can suppress crystal growth of Indium-Tin-Oxide (ITO)[13] and a high water vapor partial pressure can suppress crystal growth during IO:H deposition. The hydrogen concentration in IO:H is dependent on the water vapor partial pressure in the chamber[11].

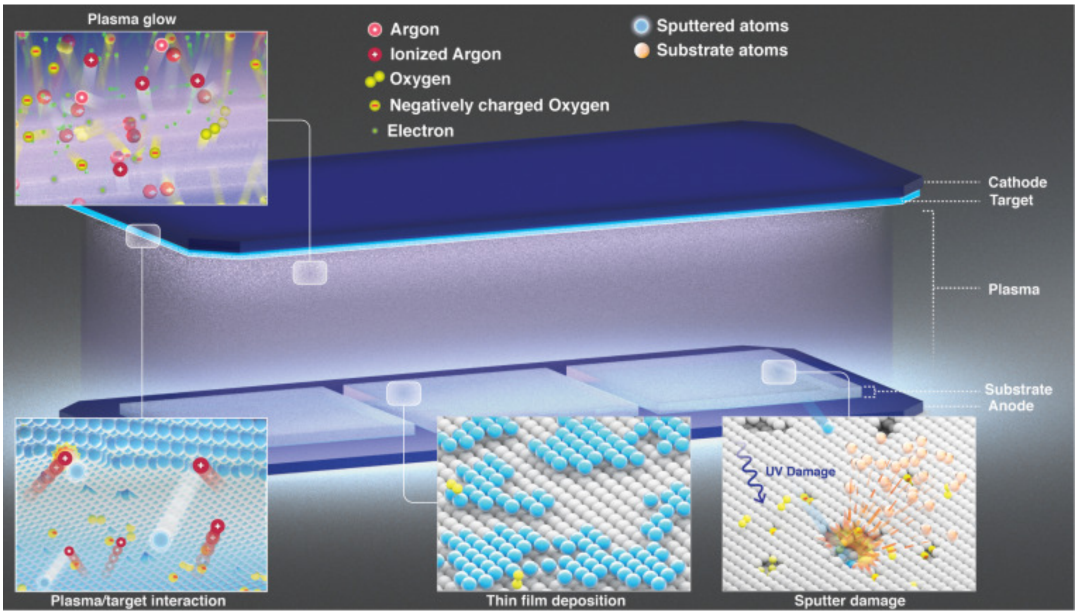


Figure 2.7: An overview of the processes involved in magnetron sputtering. The image highlights the processes of ionization, plasma/target interaction, thin-film deposition and sputter damage due to ion bombardment[12].

Opto-electronic properties of as-deposited IO:H layers are not useful in solar cells. The layer is amorphous, a state in which electron mobility is limited by grain boundary scattering. Due to the limited size of crystal grains, the electrons have a high number of grain boundaries to traverse. To crystallize the thin film, post-deposition annealing is performed, an application step during which the thin film temperature is temporarily increased. Upon crystallization, the grain boundary scattering has decreased and impurity- and phonon scattering are the electron mobility-limiting mechanisms[14]. Oxygen vacancies disappear and as a result the free-carrier absorption has decreased[15][11]. The annealed thin film absorbs fewer photons, while maintaining electrical conductivity.

2.3.3. Influence on passivating quality poly-Si(O_x)

As mentioned in section 2.2, the passivating quality of TOPCon passivating contacts is heavily dependent on the amount of defect states in the contact. A low level of defect states is crucial for high passivation. The dissociation energy of the Si-Si and Si-H bonds present in the contact is approximately 3.5 eV, whereas the kinetic energy of bombarded particles can exceed 10 eV depending on the applied power during deposition[8]. Deposition of IO:H damages the surface of the contact and creates dangling bonds, facilitating Shockley-Read-Hall recombination and decreasing lifetime of generated carriers. Lowering the power density applied during IO:H deposition can therefore preserve part of the Si-Si and Si-H bonds in the contact [12].

The post-deposition annealing of TCOs is reported to recover the dangling bonds of the passivating contact it was deposited on, decreasing the number of defect states and therefore restoring passivating quality[15][16]. Both the carrier lifetime and the implied open circuit voltage iV_{OC} showed significant recovery. The contact can withstand annealing temperatures up to 550°C, allowing these temperatures to be used to anneal the TCO. At higher temperatures the dopants in the contact are reported to show in-diffusion, permanently damaging the passivating quality. Limiting the temperature during post-deposition annealing is therefore crucial.

2.3.4. Thickness of the thin film

IO:H layers designed for the front side application of a c-Si solar cell act as anti-reflective coating. Optical interference is important when considering the reflection of light reaching the IO:H, in particular the photons that are reflected at the front of the IO:H and photons that are reflected at the back of the IO:H. The optical waves representing these photons meet when leaving the IO:H at the front. When the waves are in-phase, the intensity of the reflected light is maximized. When they are out-of-phase, i.e. a phase difference $\Delta\Phi$ of 0.5 between the wave reflected off the back of the TCO and the wave reflected at the front of the TCO, destructive interference occurs and reflection is minimal. The refractive index of the TCO determines the speed of light within any medium. To achieve destructive interference and, with it, high optical performance, the product of the thickness of the thin film and the refractive index must be approximately $1/4$ of the wavelength of the photons with the highest irradiance. If this thickness limitation is applied, the TCO will act as an anti-reflective coating at the front side of a solar (sub)cell and improve the optical performance. Figure 2.8 shows a visualization of destructive interference. Assuming a refractive index n=2 for photons with a wavelength of approximately 950 nm, the region of the solar spectrum with the highest contribution to the performance of c-Si bottom cells in double-junction solar cells, the required thin film thickness is approximately 120 nm.

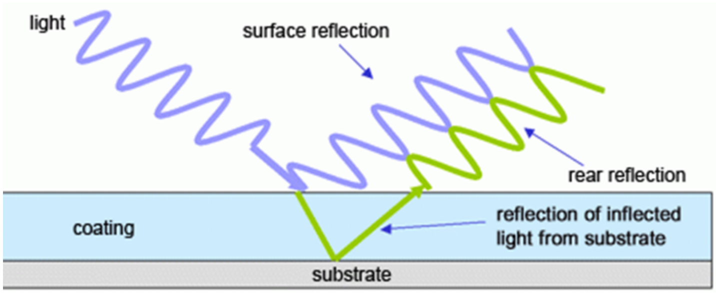


Figure 2.8: A schematic overview of two optical waves reaching an anti-reflective coating that are being reflected. After being reflected at different interfaces, the phases of the waves are exactly half of a wavelength apart.

In the recombination junction of 2-terminal double-junction solar cells, ultra-thin films with a thickness between 5 and 20 nm are required to balance parasitic absorption and lateral conductivity. IO:H applied at the rear, for example in the case of IBC solar cells, is required to have a thickness between 130 and 150 nm. This is to prevent light waves from exciting the surface plasmons at the rear metal reflector. If the penetration of the light waves into the metal is not prevented, a parasitic absorption is caused that is higher than the absorption inside the TCO itself[17].

2.4. Impact on c-Si solar cells featuring high-thermal CSPCs

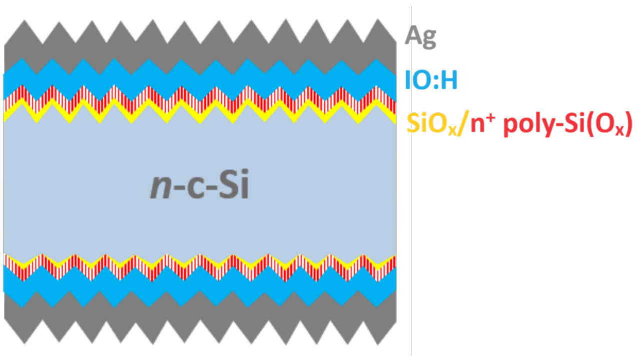
As stated in chapter 1, the investigation of the opto-electronic properties of IO:H thin films and the optimization of their application to c-Si solar cells featuring TOPCon passivating contacts is carried out to decrease optical and electrical losses in the front contact of the bottom cell of 4T perovskite-silicon tandem solar cells, the recombination junction of 2T double-junction solar cells and the n-type CSPC of IBC solar cells. By substituting ITO for IO:H as the TCO of choice, the lateral resistance of the front contact can be reduced, which, when applied correctly, increases the fill-factor of the bottom cell and therefore the overall efficiency.

Developing thin films with a high electron mobility while limiting carrier concentration is crucial for the performance of the solar cell. During application of these thin films to poly-Si(O_x), ensuring minimal losses of the passivation and alignment of the bandgaps are requirements for preservation of cell performance as well.

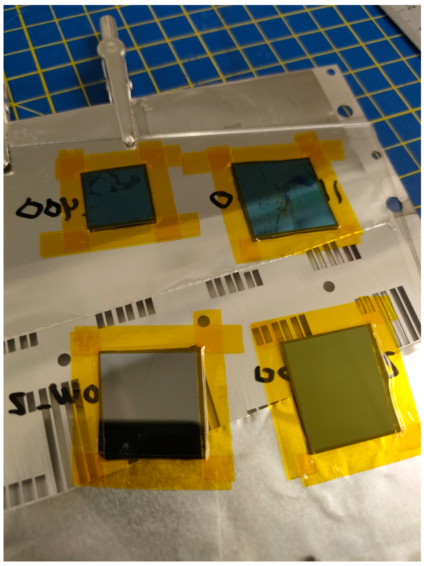
3

Experimental method

During this project, the goal is to design a IO:H thin film that is suitable for front side application to c-Si solar cells featuring TOPCon passivating contacts. First, the opto-electronic properties of IO:H on glass are optimized, see section 3.1. The second objective is to investigate the damage to the TOPCon passivating contact caused by deposition of IO:H and the recovery after post-deposition annealing, with varying temperatures. After that, the effect of lowering the deposition power density on the passivating quality is investigated, before and after annealing. The method is explained in section 3.2. Lastly, obtained results are used to design a suitable thin film for contact resistivity analysis, see section 3.3. This thin film is divided into two sublayers: one used for protection of the passivating contact and one deposited at high power density. Samples prepared for contact resistivity measurements are shown in figures 3.1a and 3.1b.



(a) Schematic representation of the cross-section of samples used for contact resistivity measurement. Ordered starting from the inside, the samples consist of the c-Si wafer, an n-TOPCon passivating contact, IO:H and a 500 nm silver coating.



(b) Wafers ready for silver deposition.

Figure 3.1: Images of samples used for contact resistivity measurements. Figure 3.1a is a schematic representation of the cross-section. Figure 3.1b displays the IO:H thin films deposited on symmetrically passivated c-Si wafers.

3.1. IO:H development

First, the opto-electronic properties of IO:H and the effect of the peak temperature during post-deposition annealing on these properties were investigated. The IO:H depositions were done with the use of the Radio-Frequency magnetron sputtering equipment shown in figure 3.2. In the deposition chamber, conditions such as substrate temperature, the mixture of gasses and power density applied to the IO target could be tuned. Results from previous studies in the PVMD department were used to determine a suitable deposition recipe. The thin films are deposited at a substrate temperature of 75°C, a water vapor partial pressure of $5 \cdot 10^{-5}$ mbar and a power density of 1.85 W/cm^2. The thickness of the thin film was set to 80 nm. By measuring the thickness of the thin film after a test deposition, the deposition rate could be determined and used to realize the desired thickness.

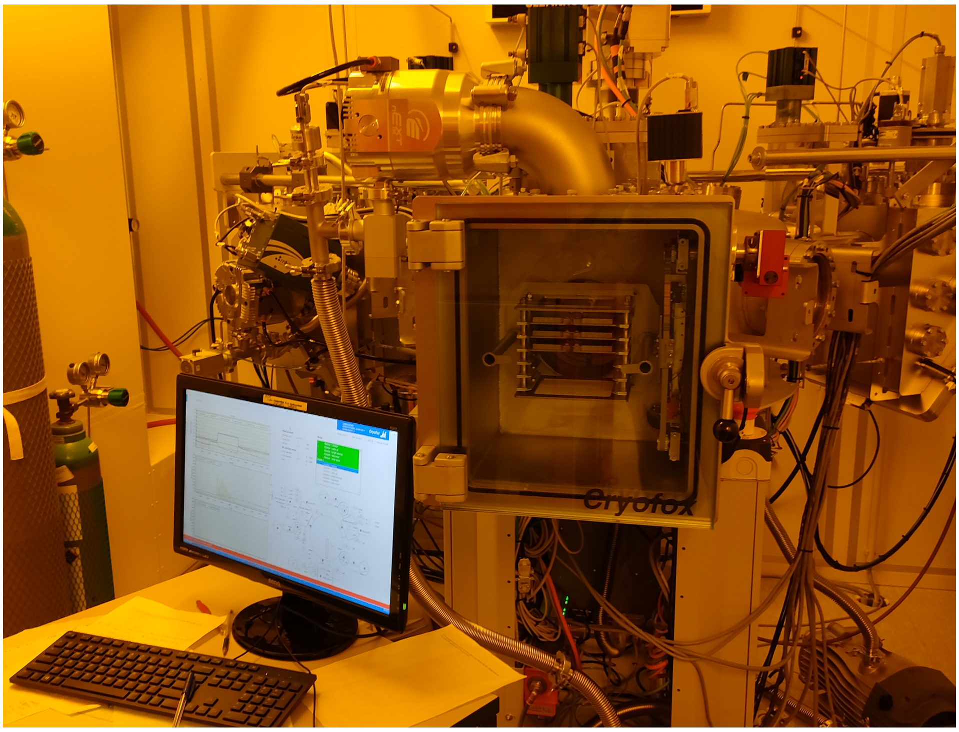


Figure 3.2: The equipment used for deposition of IO:H.

During post-deposition annealing, the sample is heated up quickly in a nitrogen gas-filled chamber. The peak temperature was varied to see the effect on the thin film properties. The shape of the temperature profile was adjusted to accommodate these variations. Because of this, the period during which the sample temperature exceeded 400°C was dependant on the peak temperature. The longest time a sample was exposed to a temperature higher than 400°C is 27 seconds. Figure 3.3 shows the temperature profile of the annealing recipe. In this example, the sample reaches a peak temperature of 700°C. To limit exposure to the oxygen-rich environment of the cleanroom and prevent thermal shock, the sample was cooled down to a maximum of 40°C before opening the processing chamber. The opto-electronic properties of the IO:H layers before and after annealing are measured.

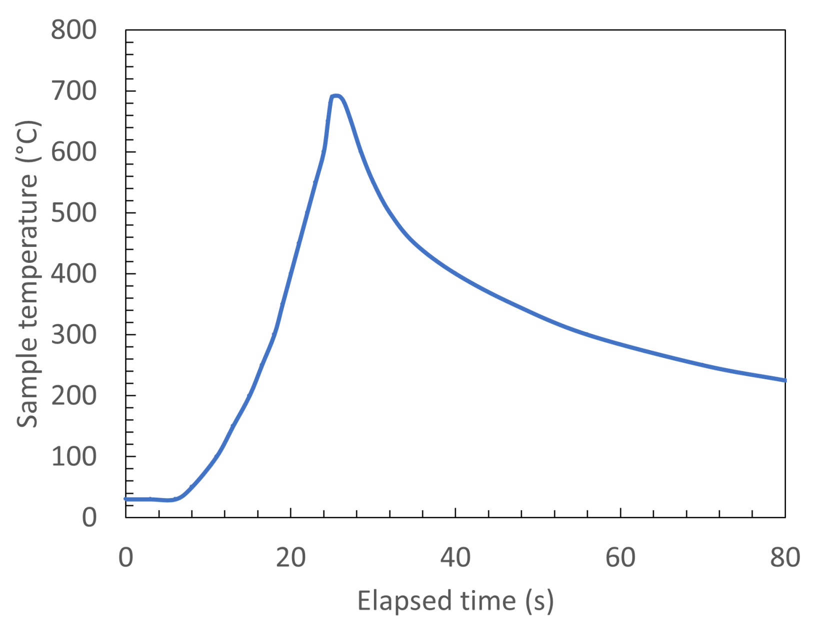


Figure 3.3: Graph displaying the time-temperature profile of the sample during annealing. After reaching the peak temperature, the chamber slowly cools down to room temperature.

3.2. Passivation degradation mitigation

The recipe described in section 3.1 is used to deposit the IO:H layers with symmetrically passivated c-Si wafers as a substrate. In section 3.4, the preparation of these wafers is explained. Before and after the deposition of IO:H, the passivating quality of the TOPCon passivating contact was measured.

A range of temperatures is used to investigate the effect the post-deposition treatment has on the passivating quality of the contact. These temperatures are determined using the results of the previous section. After annealing, the passivating quality is measured again. In addition, to get a grip on the influence of the deposition power density on the passivating quality, the experiment was repeated using deposition recipes for which the power density was decreased, and the deposition duration increased.

3.3. Contact resistivity

Cox-Strack measurements of the c-Si wafers and the TOPCon/IO:H contact stacks are performed. The IO:H consists of two sublayers, deposited on both sides of the symmetrically passivated wafer: one deposited at low power density and one deposited at higher power density. Annealing is done after deposition of the upper layer. The vertical resistance through the samples is measured for contact resistivity analysis. To create a homogeneous electric field when measuring, both sides are coated with a 500 nm layer of silver. During the silver depositions the edges of the samples are protected to prevent shunting.

3.4. Substrate preparation

10 by 10 cm^2 glass plates were rinsed with acetone and isopropyl alcohol in ultrasonic baths for 10 minutes and dried with nitrogen for preparation of the thin film investigation. For passivation measurements, 280 micron thick Float Zone-grown n-type c-Si wafers with a <100> oriented crystal structure have been symmetrically passivated by applying n-TOPCon passivating contacts on both sides of the wafers. The steps required to prepare the wafers are described in this section.

3.4.1. Cleaning and thermal oxidation

The c-Si wafers are cleaned to get rid of organics and inorganic contaminants from the surface. This is done in a 99% HNO_3 bath at room temperature and a 69.5% HNO_3 bath warmed up to 110°C respectively, both for ten minutes. The surfaces are subsequently dipped into a 0.055% HF bath followed by Marangoni drying, which involves treating the surfaces with IPA to prevent them from reacting with the oxygen in the cleanroom.

After Marangoni drying, the surfaces are loaded in a TEMPRESS furnace for thermal oxidation. They are treated for 3 minutes at 675 °C in a tube filled with nitrogen and oxygen gas. The gasses are introduced to the tube at a flow rate of 6.00 and 0.60 slm respectively. A 1.3 nm silicon oxide layer is grown. Nitric acid oxidation of silicon (NAOS) can be used as well but was not used in this project. In figure 3.4 a boat with c-Si wafers that are loaded into the tube is shown.

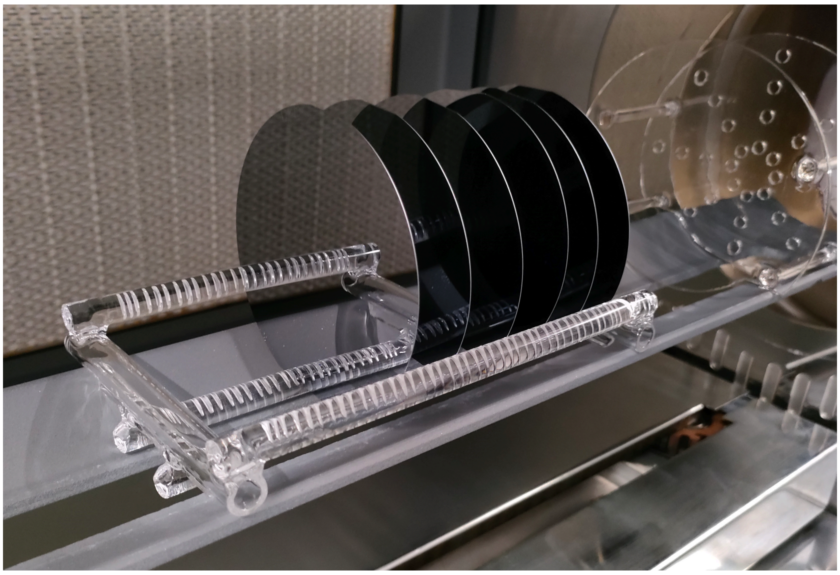


Figure 3.4: Picture of six wafers held by the boat going in and out of one of the tubes used for intrinsic poly-Si layer deposition.

3.4.2. Low-Pressure Chemical Vapor Deposition

5 nm intrinsic polycrystalline silicon is deposited on the thermally grown Si(O_x) surface using Low-Pressure Chemical Vapor Deposition. The deposition with silane (SiH_4) as the introduced gas is performed at low pressure and 580°C.

Since the polycrystalline silicon oxidizes when exposed to the ambient air of the cleanroom after coming out of the hot LPCVD tube, the wafers need to be treated afterwards with 0.55% hydrofluoric acid (HF) to remove the native oxides. This was expected to take approximately four minutes per wafer and could be checked by taking the wafers out of the HF bath and dipping them into water to see if the surfaces were hydrophobic.

3.4.3. Plasma-Enhanced Chemical Vapor Deposition

Plasma-Enhanced Chemical Vapor Deposition (PECVD) was performed to deposit a layer of amorphous phosphorous-doped silicon oxide. The 30 nm silicon oxide layer is deposited in two phases. During the first phase, a 25 nm layer alloyed with oxide is deposited. During the second phase, carbon dioxide influx is terminated and the layer grown will not contain oxygen.

After transferring the holder from a load lock, where the gasses are evacuated, to the deposition chamber, the substrate is heated up to 300°C. When the temperature is stable, a mixture of gasses is introduced to the chamber, which consists of silane, carbon dioxide, phosphate and hydrogen that are introduced at a flow rate of 4.0, 6.4, 4.8 and 35.0 cubic centimeter per minute, respectively. When the pressure of the gasses is stabilized, the RF generator, set at 5 Watt, is switched on. This will ignite a plasma that initiates the deposition of P-doped amorphous silicon oxide. After 5 minutes and 55 seconds the inlet of CO_2 is terminated and P-doped amorphous silicon will be deposited for 1 minute and 11 seconds. The amorphous layers will afterwards be crystallized, activating the dopant, at 900°C for 30 minutes to form poly-Si(O_x).

The second-to-last step of the substrate preparation is to once more remove the native oxide that has grown after exposure of the hot wafer to oxygen. Before the IO:H deposition, the wafers are cut into four quarters and loaded into the substrate holders as shown in the image of figure 3.5.

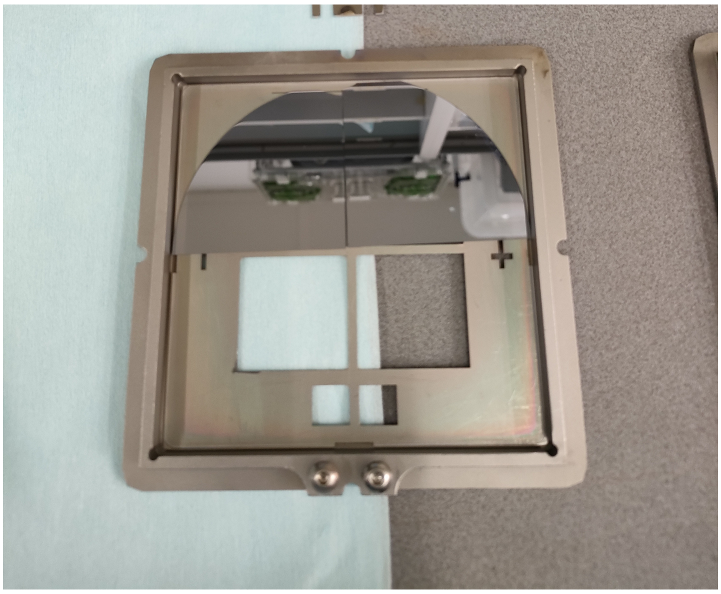
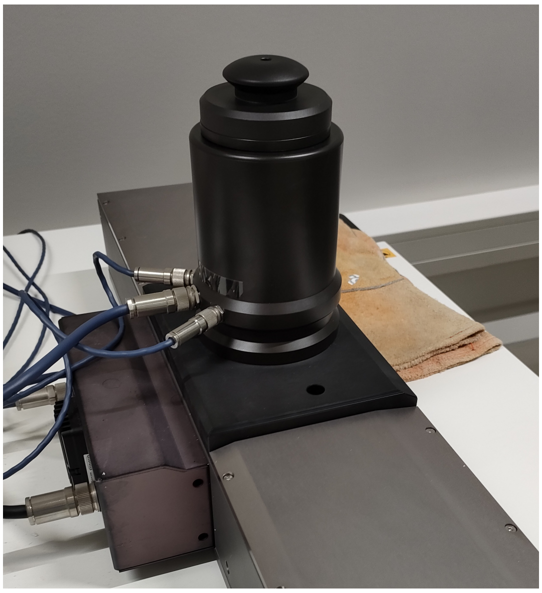


Figure 3.5: Picture of the substrate holder prepared for IO:H deposition on the rear side of two pieces of a symmetrically passivated wafer.

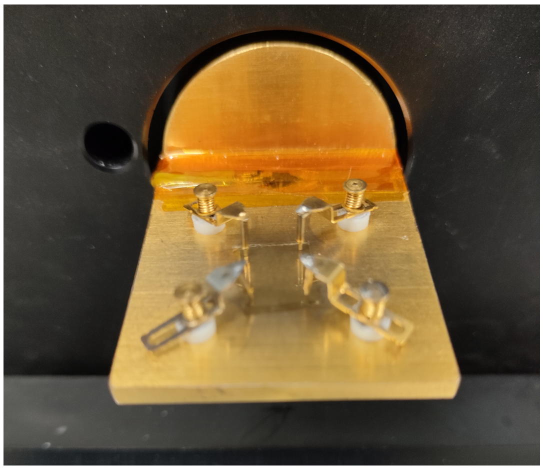
3.5. Measurement equipment

With the use of a Hall-Effect measurement system, measurements were carried out to determine the opto-electronic properties of the IO:H thin films. This system makes use of contacts on four corners of a film and a magnetic field perpendicular to the surface. By applying a potential between the contacts and measuring the carrier displacement due to the Lorentz force when the magnetic field is applied, the carrier concentration and electron mobility can be calculated. The pictures in figures 3.6a and 3.6b show the Hall-effect measurement equipment.

Sheet resistance measurements were carried out using a four-point probe. The equipment forces current through the two outer probes and reading the voltage across the two inner probes, see figure 3.7a. These measurements were then repeated at different locations of the surface of the thin film for uniformity measurements. Spectral ellipsometry measurements were used to determine the thickness of IO:H and therefore the deposition rate of the applied conditions.



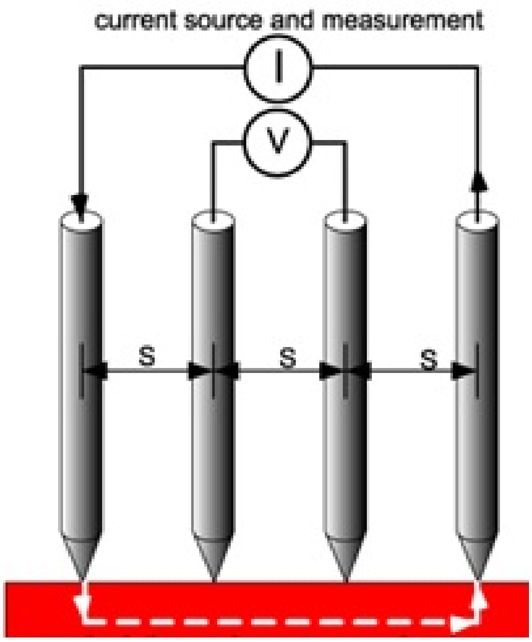
(a) Picture of the exterior of the Hall-effect measurement setup



(b) Picture of the holder of the Hall-effect measurement setup and a pinned IO:H sample deposited on glass

Figure 3.6: Images of the Hall-effect measurement system

To measure the passivating qualities of the wafer, the WCT-120 made by Sinton Instruments, see figure 3.7b, was used. This system makes use of the Quasi-Steady-State Photoconductance (QSSPC) measurement method developed in 1994. The system measurements are used to determine the lifetime of carriers τ_{eff}. The vertical resistance has been measured with the AAA Wacom WXS-90S-L2 solar simulator.



(a) A schematic representation of the equipment used to calculate the sheet resistance of a sample

(b) The WCT-120 by Sinton Instruments, used to measure passivating quality of contacts

Figure 3.7: Measurement systems used during this project

4

Results

In this chapter, the results of experiments described in chapter 3 are shown. IO:H thin films were investigated. The Hall-effect measurement results can be found in section 4.1. In section 4.2, the changes of the passivating quality of TOPCon passivating contacts after IO:H deposition and annealing are shown. In section 4.3 the results are shown of Cox-Strack measurements of symmetrically passivated c-Si wafers that are covered with n-TOPCon/IO:H/Ag stacks. The latter are performed with bi-layers of IO:H.

4.1. Annealing effect on opto-electronic properties IO:H

In this section, the results from Hall-effect measurements of the IO:H thin films can be found. Before and after post-deposition annealing, electron mobility and carrier concentration were measured. Figure 4.1 shows the effect of post-deposition annealing at a peak temperature of 600°C on the carrier concentration and the electron mobility in the film. With decreasing amount of oxygen vacancies, the carrier concentration drops significantly, from $2.8 \cdot 10^{20}$ to $8.2 \cdot 10^{19}$ cm^{-3}. The electron mobility increases from 59.3 to 146 cm^2/Vs.

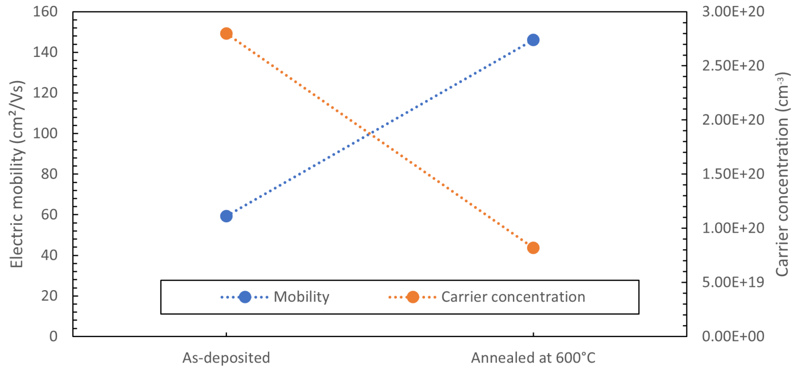
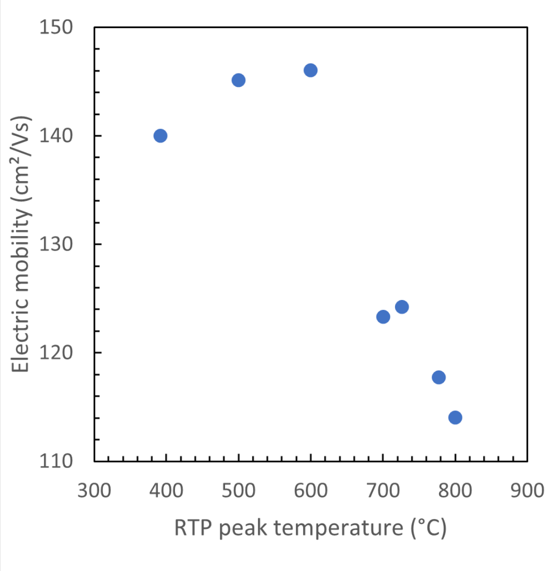
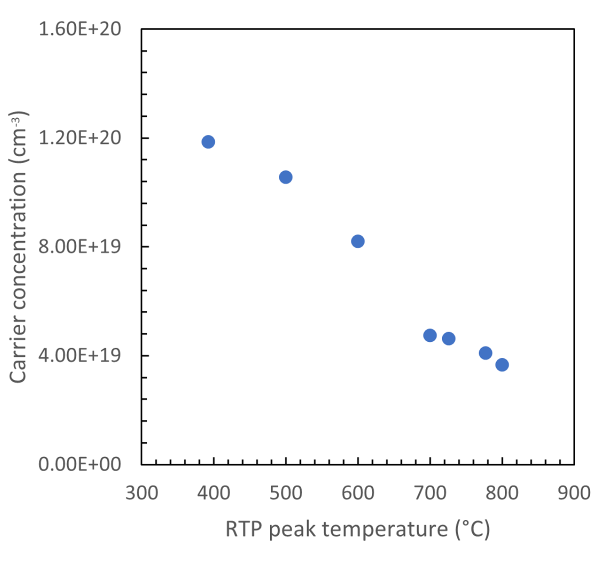


Figure 4.1: Carrier concentration and electron mobility of the IO:H thin film before and after fast-annealing at a peak temperature of 600°C

In figures 4.2a and 4.2b, the electron mobility and carrier concentration of samples that are annealed at different peak temperatures are shown. As stated in previous section, after deposition these films have an electron mobility of 59.3 cm^2/Vs and a carrier concentration of $2.8 \cdot 10^{20}$ cm^{-3}. From results of the Hall-effect measurements with samples annealed at temperatures below 600°C, it can be seen that the electron mobility gradually increases and the carrier concentration decreases. For samples annealed at higher temperatures, the carrier concentration continues this trend. However, for these samples the electron mobility drops rapidly.



(a) Electron mobility of IO:H thin films after annealing at different peak temperatures



(b) Carrier concentration of the IO:H film after annealing at different peak temperatures

Figure 4.2: Results from Hall-effect measurements.

4.2. Damage to passivating quality poly-Si(O_X)

From the passivation measurements, the minority carrier lifetime results were extracted and are shown in figure 4.3. It can be seen that the deposition of IO:H negatively impacts the passivating quality of the contact.

In this figure, the change after annealing at different peak temperatures can be seen as well. Whereas the deposition damaged the passivating quality of the contact, a very small portion of the passivation loss could be recovered during annealing. This is only the case for temperatures below 600 °C, whereas the passivation damage is increased after annealing at higher temperatures. The majority of the damage caused by IO:H deposition appears to be non-recoverable and investigation of the influence of the annealing temperature seems unnecessary. For these samples, the passivation damage due to breaking of the Si-Si bonds during deposition is too large.

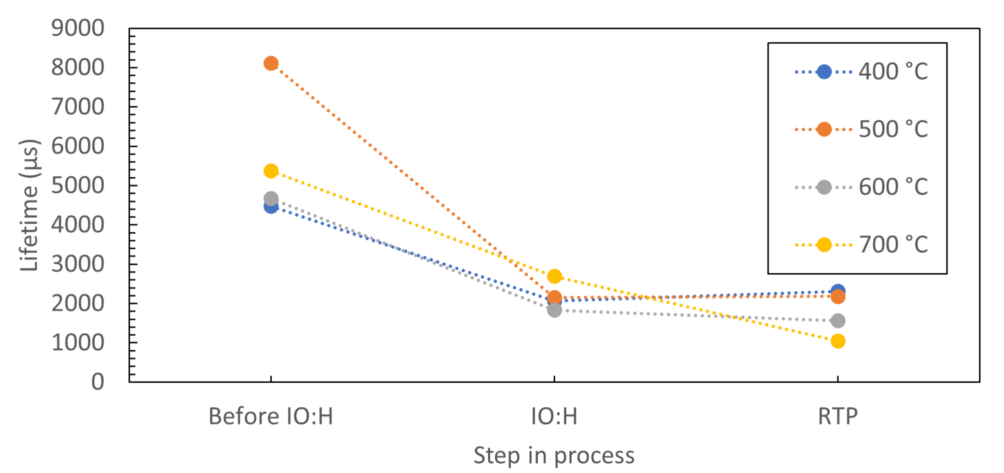
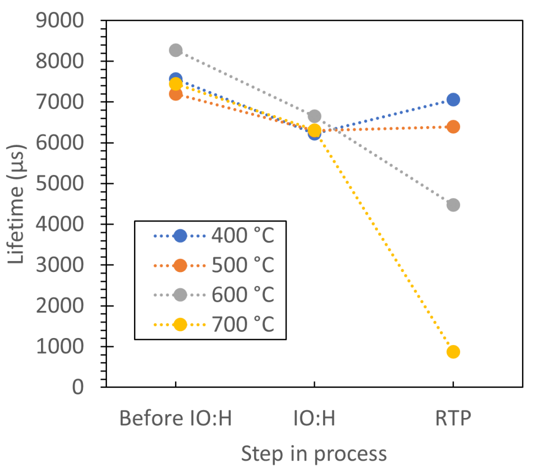


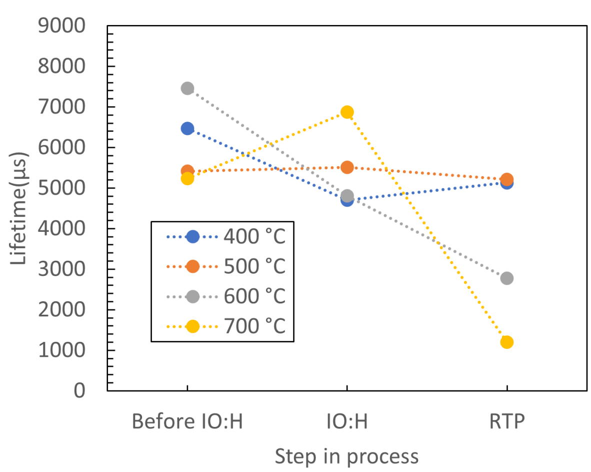
Figure 4.3: Minority carrier lifetime results extracted from passivation quality measurements of symmetrically passivated wafers throughout the IO:H application process. The power density applied on the indium oxide target during deposition was 1.85 W/cm^2. The figure shows the results before IO:H deposition, after IO:H deposition and after rapid thermal annealing at four different peak temperatures.

4.2.1. Influence of sputtering power density

The power applied during IO:H deposition is lowered to investigate the effect this has on the damage done to the passivating quality. The results can be found in figures 4.4a and 4.4b. It is clear that lowering the power density during deposition has a positive effect on the passivating quality. Figure 4.5 shows the effect of changing the power density on the relative change more clearly. Comparing these figures to figure 4.3, it can be seen that lowering the power density during IO:H deposition helps protect the contact in such a way that the passivating quality can be recovered during annealing. The effect of lowering the power density from 1.85 W/cm^2 to 1.23 W/cm^2 is the most significant. In addition, these figures indicate the need to limit the peak temperature during annealing to 550°C. Because of indiffusion at higher annealing temperatures, the results show that it does not matter if the deposition was performed at low power density. A bi-layer consisting of a sublayer deposited at low power density and a high-mobility sublayer seems most viable for further IO:H investigation.



(a) 0.62 W/cm^2



(b) 1.23 W/cm^2

Figure 4.4: Carrier lifetime (in microseconds) results extracted from passivation measurements throughout the process. Figures 4.4a and 4.4b show four values before and after deposition of IO:H with an applied power density of 0.62 and 1.23 W/cm^2 respectively. The relative change after annealing at 400, 500, 600 and 700 °C are also shown in figure 4.5.

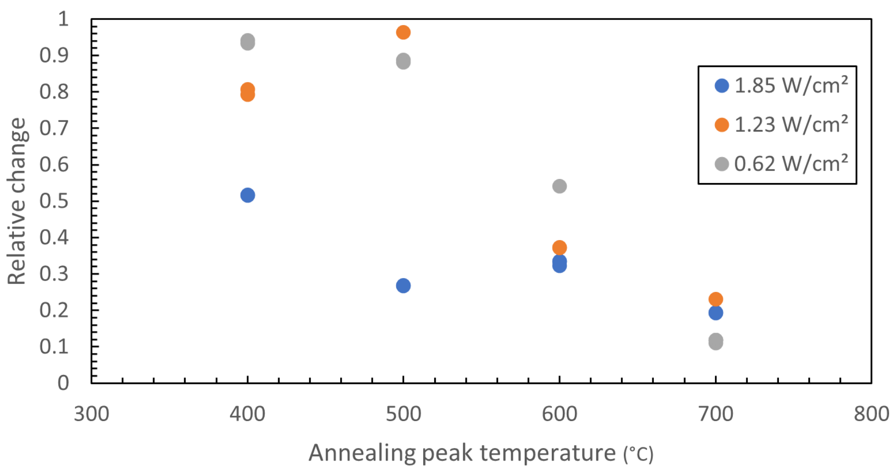
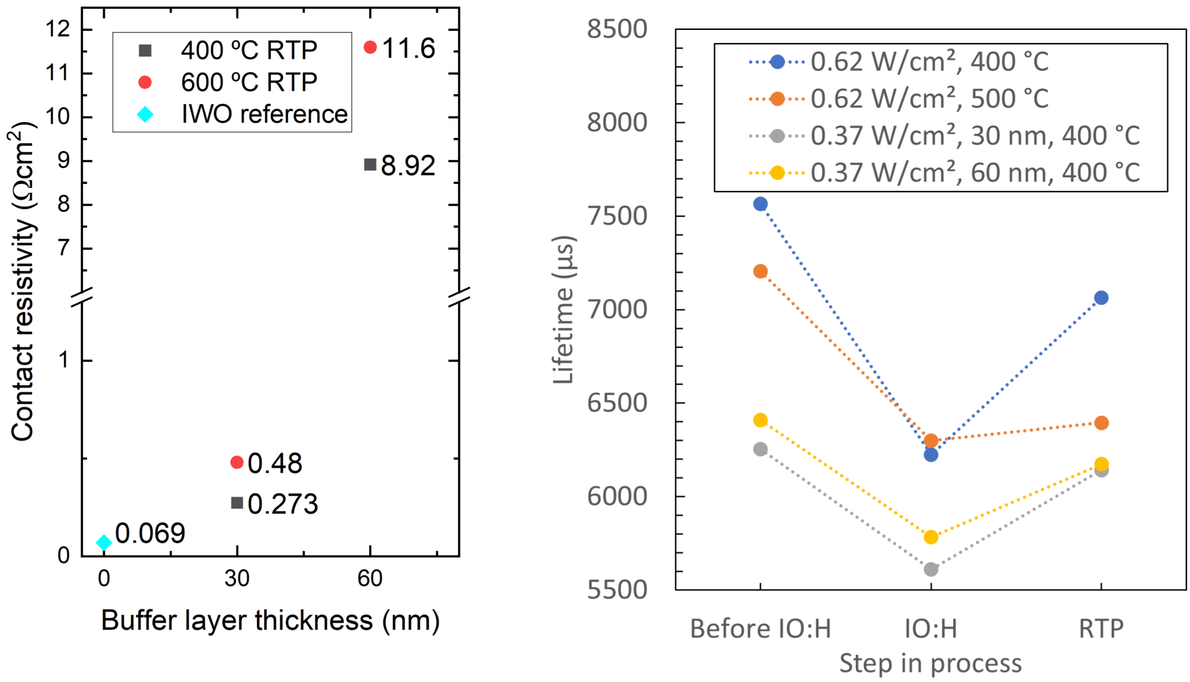


Figure 4.5: Relative change of the passivating qualities of the TOPCon passivating contact after IO:H deposition and annealing, visualized using carrier lifetime. The peak temperature during annealing and the power density during deposition are varied.

4.3. Contact resistivity

Based on the results of the experiments shown in the previous sections, it was decided to use the deposition and annealing conditions used for high-mobility IO:H thin films for the upper layer of the bi-layer and 0.37 W/cm^2 was chosen as the power density during deposition of the buffer layer. The resistance measured between the two silver electrodes is multiplied by the surface area of every sample, which varied between 2.6 and 4.4 cm^2, to determine the value independent of the surface area.

The surface area-independent values are used to determine the contact resistivity of the n-TOPCon/IO:H stack. This can be done by subtracting the contribution of the c-Si bulk and taking into account the fact that the stack is applied to both sides of the wafer. Figure 4.6a shows the values representing contact resistivity. It is clear that increasing the thickness of the buffer layer negatively impacts the contact resistivity. The y-axis is broken in order for the measurements to fit in one graph. An additional measurement obtained from a similar study on Indium-Tungsten-Oxide as the TCO has been added as a reference, showing that the measured contact resistivity of each of the n-TOPCon/IO:H stacks is high[15].



(a) Resistivity of the TOPCon/IO:H/Ag contact stack of symmetrically passivated samples, plotted against buffer layer thickness.

(b) Lifetime results throughout the process of samples deposited at low power density, mono-layer (0.62 W/cm^2) and bi-layer with varying buffer layer thickness (0.37 W/cm^2).

Figure 4.6: Contact resistivity results and passivation changes after IO:H application to symmetrically passivated wafers.

4.3.1. Buffer layer protection

The results of the passivation measurements from before and after IO:H application are again investigated. In section 4.2, it could be seen that the damage caused by magnetron sputtering could be significantly reduced by lowering the power density. In this section, the results of bi-layer sample measurements are compared to those of previous processes. In figure 4.6b the carrier lifetime evolution of these samples is shown. The thickness of the buffer layer, deposited at 0.37 W/cm^2, was varied and the upper layer is deposited at 1.85 W/cm^2. It can be seen that a large part of the passivation loss during bi-layer deposition can be recovered by post-deposition annealing: the relative loss after the full application process is only 2 and 4 percent for the samples with a buffer layer thickness of, respectively, 30 and 60 nm. The results show that increasing the buffer layer thickness from 30 to 60 nm does not yield a significant improvement.

5 Discussion

In chapter 4, results of measurements of the opto-electronic properties of IO:H thin films, passivating quality of TOPCon passivating contacts and contact resistivity of TOPCon/IO:H stacks are presented. Not all results can be explained by the theory presented in chapter 2. In this chapter the explanation of findings in this project will be given.

5.1. Thin film optimization

During post-deposition annealing, the previously amorphous IO:H thin films crystallize, resulting in a decrease of the amount of oxygen vacancies. The grain boundary scattering, which in amorphous films is the limiting factor for electron mobility, significantly decreases as well due to the crystallization. The resulting thin film absorbs fewer photons, while maintaining its electrical conductivity. Whereas the carrier concentration kept decreasing after increasing the annealing temperature, the electron mobility suddenly did as well. The decreasing electron mobility of IO:H thin films annealed at temperatures above 600°C is a result of the carrier concentration falling below a critical value. According to Magari et al., due to the decrease of carrier concentration, the electrons can no longer tunnel through the grain boundaries, which are not more than 1 nanometer thick, and the electron mobility is limited[18]. This is typically the case for TCOs with carrier concentration below 10^{20} cm^{-3} and therefore explains the sudden decrease of the electron mobility when the thin film is exposed to temperatures higher than 600°C.

5.2. Passivating quality preservation

As expected, the passivating quality of TOPCon passivating contacts decreases during the deposition of IO:H, except for two samples (see paragraph 5.2.1). Since this is caused by the kinetic energy of the approaching particles exceeding the breaking energy of Si-Si and Si-H bonds, lowering the power density during deposition improved results. When lowering the power density during deposition, a large amount of Si-Si and Si-H bonds in the poly-Si(O_X) are maintained and the number of defect states causing recombination is significantly reduced. The recovery of a portion of the passivating quality of the contact during annealing at low temperatures is in agreement with the results of Tao et al., that show a peak of the carrier lifetime and open circuit voltage when the post-deposition annealing temperatures is between 350 and 500°C. During annealing, some of the Si-Si and Si-H bonds are recovered and the number of defect states decreases. If the annealing temperature is raised to 600°C, the passivating quality is lost due to indiffusion of the dopant.

5.2.1. TCO booster

Two samples show a different change in the passivating quality after the deposition of IO:H than the other ten samples. The samples that were used as substrates for deposition of IO:H at a power density of 1.23 W/cm^2 and post-deposition annealing at peak temperatures of 500 and 700°C received a boost in passivation from the IO:H deposition. This could be caused by inconsistencies in the substrate preparation process. Even though the aim has been to keep the process conditions for all prepared substrates equal, the thickness of the poly-Si(O$_X$) layer of the samples in question could have been smaller than that of the other samples. As a result, the influence of the IO:H layer on the hole conductivity in the contact, and therefore the carrier lifetime, could have increased. The valence band maximum of IO:H is significantly lower than that of n-type polycrystalline silicon oxide and increases the barrier for holes generated in the crystalline silicon bulk. This effect is also known as a TCO booster. Post-deposition annealing of the IO:H does not necessarily nullify the TCO booster, unless the temperature limit is exceeded and the dopants diffuse into the c-Si bulk.

5.3. Contact resistivity analysis

An explanation for the high contact resistivity in the samples can be found in the low deposition rate of the buffer layer. The deposition rate of the buffer layer was 30 nm per hour which is very low compared to the deposition rate of the high-mobility IO:H layer, which was deposited at a rate of 274 nm per hour. Since the film is grown in a partially oxygen-filled chamber, a high oxygen concentration should be found in the buffer layer. Oxygen acts as an electron donor via a complex reaction and increases the electron concentration in the buffer layer, see equation 5.1[19]. The carrier concentration of the IO:H thin film deposited at 0.37 W/cm^2 was $4.3 \cdot 10^{20}$ cm^{-3}. Since this is much higher than the carrier density in poly-Si(O$_X$), the field-effect driven mobility μ_{FE} of electrons into the buffer layer is limited. This can severely decrease the performance of a solar cell as the separation of electrons and holes is limited. If the thickness of the negatively charged barrier is increased from 30 to 60 nm, the contact resistivity is affected even more.

$$2O^{2-} <=> O_2 + 4e^- \tag{5.1}$$

6

Conclusion and recommendations

6.1. Conclusion

During this project, the research questions presented in chapter 1 have been answered with the help of experiments presented in chapter 3. The conclusions, that help improve process conditions for IO:H application to c-Si solar cells featuring TOPCon passivating contacts, are presented in this section.

6.1.1. Influence of annealing temperature on opto-electronic properties IO:H

For the specific set of deposition conditions presented in section 3.1, a clear distinction can be made between the effect increasing the annealing temperature has on opto-electronic properties of the samples annealed below or above 600°C. For both regions, the carrier concentration continuously decreased. Whereas the electron mobility in the first region is predominantly determined by the crystallization of the thin film and therefore increases with the annealing temperature, the carrier concentration falling below the critical value of 10^{20} cm^{-3} resulted in the rapid decrease of the electron mobility in the second. The exact temperature that separates these regions has not been accurately determined and varies for different sets of deposition conditions, as each set results in an as-deposited thin film with a different microstructure and composition.

6.1.2. Influence annealing temperature and power density on passivating quality

For preservation of passivating qualities of TOPCon passivating contacts two methods were found. These include lowering the applied power density during IO:H deposition to 0.37 W/cm^2 and the partial recovery during annealing with a peak temperature between 350 and 550°C. At higher temperatures the passivation is further damaged. It is clear that by limiting the power density to 0.37 W/cm^2, preservation of the passivating contact can be ensured. The maximum annealing temperature allowed for recovery of the TOPCon passivating contact aligns with the annealing peak temperature that resulted in high-mobility IO:H thin films.

6.1.3. Influence of buffer thickness on passivating quality

Reducing the buffer layer thickness from 60 to 30 nm had no significant effect on the passivating quality of the TOPCon passivating contact; both values resulted in high passivation preservation. Comparing these results with the results from experiments with mono-layer thin films deposited at 1.85 W/cm^2, it is clear that the thickness region where the contact is no longer protected is between 0 and 30 nm.

6.1.4. Influence of buffer thickness on contact resistivity

The deposition conditions for the buffer layers, specifically the low deposition rate and the resulting high oxygen concentration of these layers, caused a high thickness-dependency of the contact resistivity; the contact resistivity increased rapidly when increasing the thickness from 30 to 60 nm. For these process conditions, the thickness for these buffer layers should be decreased below 30 nm.

6.2. Recommendations

Even though progress has been made in the development of high-mobility IO:H thin films for front-side application to c-Si solar cells featuring TOPCon passivating contacts, in this section possible approaches to improve the balance between contact resistivity, passivation and thin film optimization are discussed.

6.2.1. Buffer layer integration

From the results of this project, it is clear that optimization could be achieved by further improvement of the integration of the buffer layer. Looking at the results, one method that stands out is decreasing the thickness of the protective layer. The thickness of the buffer layer clearly affected the contact resistivity and decreasing this could improve the contact resistivity. However, the passivating quality of the contact could be affected since without a protective layer, deposition at high power density severely damages the contact. The passivating quality of the contact should be monitored while decreasing buffer layer thickness. Eventually, an optimal thickness of the buffer layer can be found.

Decreasing the carrier concentration in the buffer layer, which requires the decrease of oxygen adsorption during deposition, is necessary as well. This could be achieved by changing the mixture of gasses or lowering the substrate temperature. According to Tao et al., TCO deposition at room temperature was beneficial with regard to the passivating quality of TOPCon passivating contacts after annealing[16]. Even though progress has been made in the preservation of the passivating quality of the contact, depositing the buffer layer at room temperature could offer a degree of freedom and improve the trade-off between contact resistivity and passivating quality.

6.2.2. ITO topping

In another study, it was found that the interaction between IO:H and silver could produce an insulating interface[20]. According to the results of this study, topping off the IO:H-based TCO with a small ITO sublayer significantly improved the results. The cumulative thickness of the IO:H and ITO layer can not exceed that of an ARC. Substituting at most 20% of the IO:H layer by ITO ensures low contact resistivity, while maintaining low sheet resistance and free-carrier absorption. This combination outperforms IO:H-only and ITO-only thin films in certain solar cells.

6.3. Outlook of the project

6.3.1. Thin film optimization

As stated in chapter 2, it is found that IO:H thin films can reach values for the electron mobility of 160 cm^2/Vs. The development of high-mobility Hydrogenated Indium Oxide thin films with the help of Rapid Thermal Annealing had not yet been explored prior to this project and proves to be a useful outcome in cases that require the post-deposition annealing step of the development process to be done at high temperatures. The results spark interest in further investigating potential changes in the development process that would result in values of the electron mobility that are closer to the known theoretical limit. A logical first step would be to vary the process conditions used in this project, such as the partial pressure of water vapor, the substrate temperature or the power density during deposition. This could potentially combine the benefits of sufficient crystallization, so that grain boundary scattering has become negligible, and a high ($>10^{20}$ cm^{-3}) carrier concentration for electron tunnelling at the grain boundaries when the thin film is annealed.

6.3.2. Perovskite/c-Si bottom cell and IBC integration

As stated in the introduction of this report, the value of IO:H/TOPCon contact stacks is for specific solar cell architectures, namely as a front contact of the c-Si bottom cell in 4T perovskite-silicon tandem solar cells or for application to the n-side of IBC solar cells. Due to the high electron mobility in the IO:H, the investigated high-thermal contact stacks are promising for both applications. Because of the limited thickness that is required to balance parasitic absorption and lateral conductivity in the recombination layer of 2T double-junction solar cells and the requirement of a buffer layer to protect the passivating contact, the results of this project are not useful for this specific type of solar cell.

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