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A 28 nm 2 GS/s 5-b Single-channel SAR ADC with g_m-boosted StrongARM Comparator

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***Abstract*— This paper presents a 2 GS/s 5-b single-channel SAR ADC in 28 nm CMOS. The ADC uses a g_m-boosted StrongARM comparator to achieve the highest reported sampling frequency for a non-time-interleaved SAR ADC. Its high sampling frequency, large input signal capability and one clock cycle latency make the ADC suitable for time-interleaved, multi-stage and feedback ADC architectures. The ADC occupies 900 µm^2 and consumes 1.25 mW from a 0.9 V supply. Without calibration, and when operated at 1.5 GS/s it achieves 30.3 dB SNDR (FOM$_W$=31.2 fJ/conv.-step). This drops slightly, to 27.4dB, at the maximum sampling rate of 2 GS/s.**

***Keywords*—SAR converter, Single-channel, rail-to-rail input signal, asynchronous logic, bottom plate sampling, 28 nm CMOS, g_m-boosted StrongARM comparator.**

I. INTRODUCTION

To push the limits of advance data converters (resolution and bandwidth) ADC architectures such as time-interleaved, feedback (oversampled) and multi-stage are employed [1-5, 8, 9]. Fig. 1 shows an overview of state-of-the-art ADC architectures. Time-interleaved ADCs achieving sampling rate >20GS/s use high speed single-channel SAR ADCs to lower the complexity of their sample-and-hold networks [8]. On the other hand, oversampled ADCs clocked at GHz sampling rate use low latency multi-bit quantizers (either Flash or SAR ADCs) to meet stability requirements [9]. Multi-stage architectures are the preferred choice when both wide bandwidth (>50 MHz) and high dynamic range (DR>80 dB) are required [1-4]. Such systems use a coarse ADC (either Flash or SAR), a DAC and a continuous-time ΔΣ ADC to achieve high dynamic range, as well as inherent anti-alias filtering [1]. The ΔΣ ADC only converts a small residue (V_{IN}-V_{DAC}). However, the latency of the coarse ADC/DAC combination is critical and should be limited to one clock cycle. This is because more latency increases the amplitude of the residue signal and eventually overloads the ΔΣ ADC [3].

Flash ADCs have low latency and can deal with large input signals, but they are power hungry [1-2]. Recent work has shown the feasibility of high speed (>1 GS/s) and power efficient single-channel SAR ADCs [5-7]. However, their input common mode voltage is chosen close to the supply rail, severely limiting the maximum input signal amplitude. Furthermore, their latency is more than one clock cycle, due to the time needed to decode redundant bits [5] or to read lookup tables [7]. Such ADCs are not suitable for multi-stage ADCs.

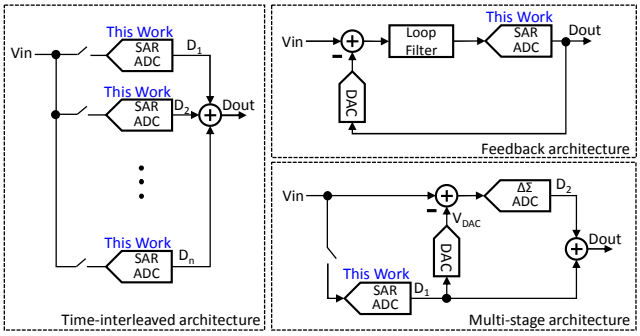

Fig. 1. Applications of high speed single-channel SAR ADCs.

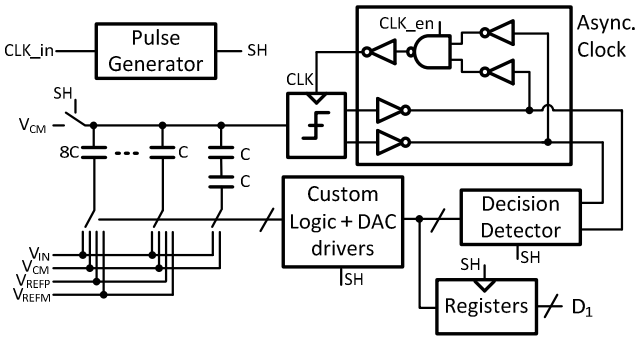

Fig. 2. Single-channel SAR ADC.

In this work, a 2 GS/s 5-b SAR ADC is presented with one clock cycle latency and rail-to-rail input capability (0.5*V_{DD} input common mode voltage) to push the limits of the data converters shown in Fig.1. High speed is enabled by a g_m-boosted StrongARM comparator. To handle 1.8 $V_{pp\text{-}dif.}$ input signals, bottom-plate, rather than top-plate, sampling is employed, at the cost of extra complexity and power consumption. The proposed design achieves the highest sample rate reported for a non-time-interleaved SAR ADC.

The paper is organized as follows: Section II describes the operation of the proposed SAR ADC. Section III discusses the operation of the g_m-boosted StrongARM comparator. Measurement results and a conclusion are reported in Sections IV and V respectively.

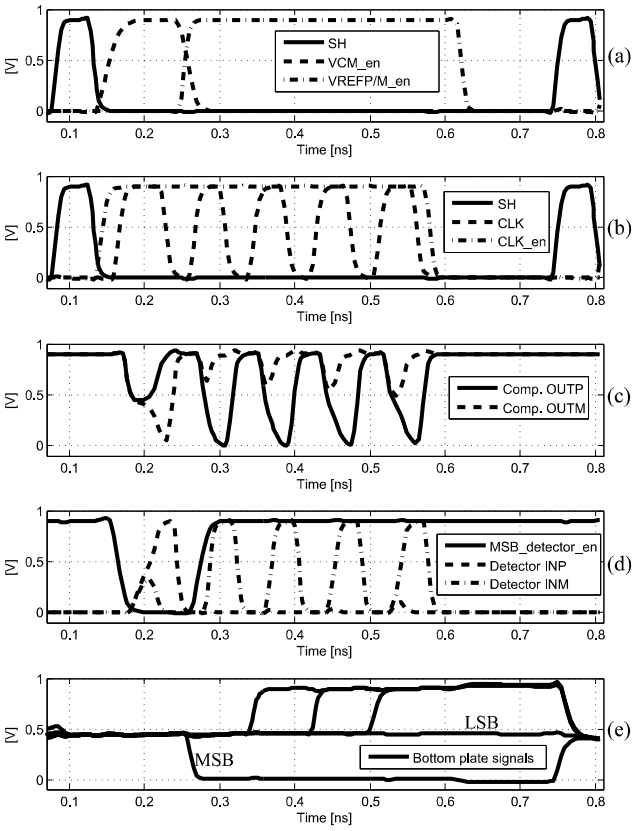

Fig. 3. ADC behavior.

II. PROPOSED SAR ADC DESIGN

The ADC's architecture is shown in Fig. 2, where the DAC is drawn single-ended for simplicity. All its internal clock phases are derived asynchronously from an external clock (CLK_in) with a 50% duty-cycle signal.

At the start of the sampling phase, the top plates of all the DAC capacitors are connected to common mode voltage V_{CM} while the bottom plates are connected to the input signal V_{IN} (all the sampling switches are implemented as pass-gates).

At the end of the sampling phase, CLK_en allows (via the NAND gate in Fig. 2) the asynchronous clock to toggle. At the same time, the bottom plates of all DAC capacitors switch from V_{IN} to V_{CM}, while the top plates switch from V_{CM} to $V_{CM} - (V_{IN} - V_{CM})$. The polarity of the input signal is then evaluated. In this step, DAC settling is not important, so the comparison can start immediately after the propagation delay of the NAND and NOT gates in Fig. 2. After the regeneration phase, a Decision Detector based on pre-charged logic [6] stores the comparator's decision and sends the differential information to a Logic block that updates the CAP-DAC via a DAC driver. At the same time, the asynchronous clock generator resets the comparator. The NAND gate in Fig. 2 senses when the comparator outputs are both higher than $0.5*V_{DD}$ and triggers a new comparison phase.

Since the comparator operates asynchronously it must be disabled after the fifth conversion and during each sampling phase. If it is active during the sampling phase it may not be ready for the first conversion phase or it may provide a wrong decision to the Decision Detector. CLK_en disables the comparator appropriately and also resets the Logic.

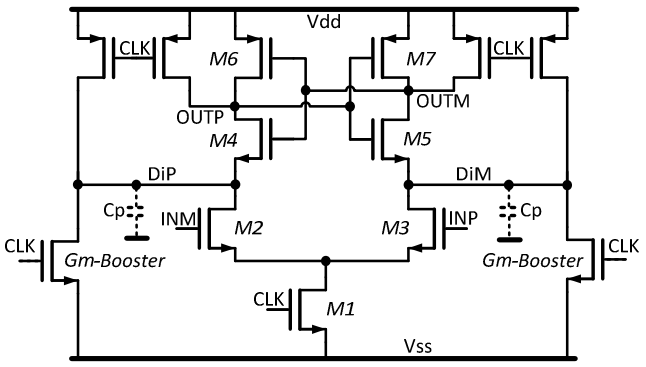

Fig. 4. Proposed g_m-boosted StrongARM comparator.

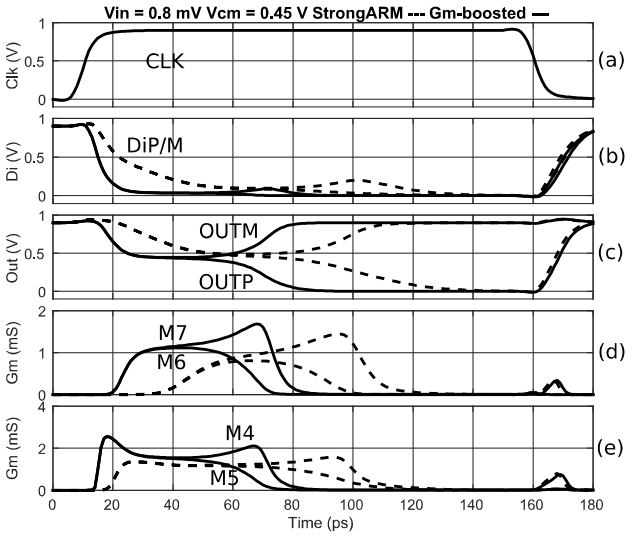

Fig. 5. Signals behaviors of StrongARM and g_m-boosted comparators with 0.8 mV input signal and $0.5*V_{DD}$ common mode voltage.

At the start of each sampling phase, the bottom plate switches are opened to ensure that V_{IN} is well isolated from the references. In this phase, the decision detector is reset.

Fig 3 depicts the aforementioned signals at a 1.5GHz sampling frequency. Fig. 3a shows the signals that enable the connection of the MSB bottom plate to the input signal, to common mode voltage and to V_{REFP} or V_{REFM}. Fig. 3b shows the sampling signal (SH), CLK_en and the asynchronous clock (CLK). Fig. 3c shows the outputs of the comparator, in this case it can be seen that the first conversion is longer than the others. Fig. 3d shows the input signals of the Decision Detector and the enable signal of the MSB detector (active low). In Fig 3e, the bottom plate signals are shown. In the proposed DAC scheme, the LSB bottom plate does not switch during the conversion phase.

Design for manufacturability concerns implies that custom sub-fF capacitors are undesirable. To reduce DAC area and settling time, its LSB consists of two minimum size capacitors (1.4 fF) in series (Fig. 2). This halves the total capacitance of the array from 43.4 fF to 21.7 fF.

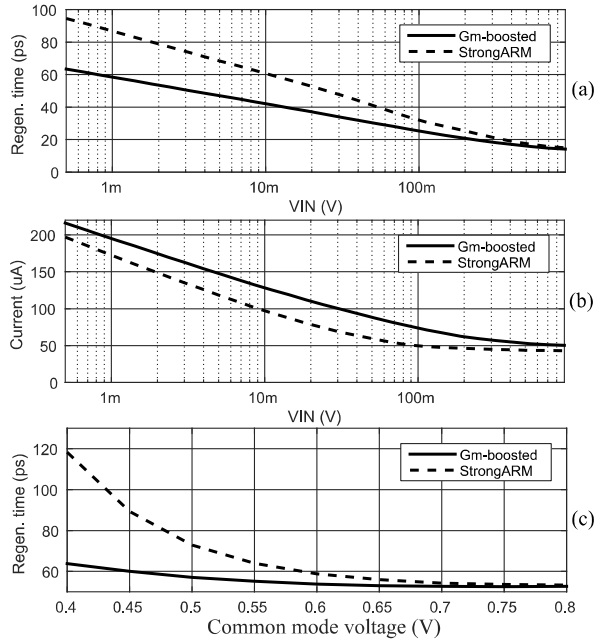

Fig. 6. Regeneration time and current consumption vs. input amp. (a, b), regeneration time vs. common mode voltage with 0.8 mV input amp. (c).

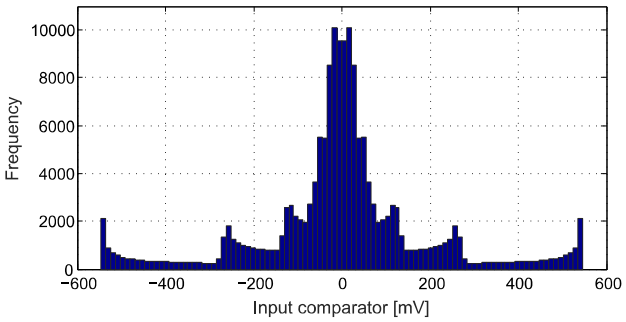

Fig. 7. Estimation of the comparator's input voltage with a 1.8 Vpp-dif. amplitude input signal.

Custom-made gates optimized for speed are used in the Logic block to reduce the propagation delay. This, together with the aforementioned series capacitors technique and g_m-boosted comparator (discussed in the next section), make it possible for the ADC to operate at very high sampling rates.

III. G_M-BOOSTED STRONGARM COMPARATOR

Fig. 4 shows the schematic of the g_m-boosted StrongARM comparator. The speed of a standard StrongARM comparator (i.e. without g_m-boosting) is determined by the size of its input pair M2/3 and by the input common mode voltage. On the rising edge of CLK, M2/3 turn on and discharge the parasitic capacitance Cp at nodes DiP/M (Fig. 5b). When they reach V_{DD}-V_{TH}, M4/5 turn on and the latch phase starts (Fig 5c). To speed-up the comparator, either the size of the input pair or its common mode voltage can be increased. The former increases Cp and the input capacitance, which in turn attenuates the output of the CAP-DAC. In [10], a double-tail sense amplifier generates a large current during the latch phase, but suffers from limited current in the slew phase.

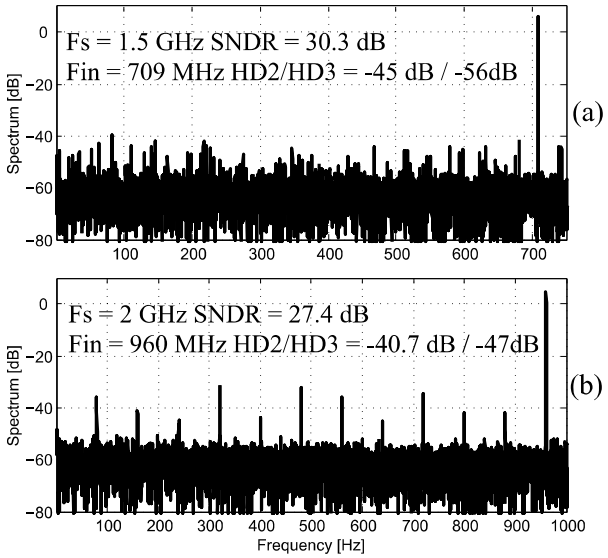

Fig. 8. Measured spectra for an input signal of 1.8 Vpp-dif. (a-b).

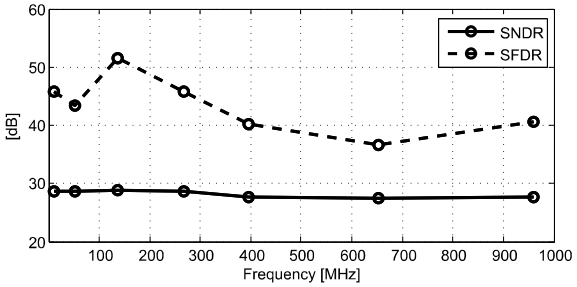

Fig. 9. SNDR and SFDR vs. fin at 2 GS/s and 1.8 Vpp-dif. amplitude.

In this design, transistors M2/3 are split into two parts. One part (¾) is connected to the input signal, while the other (¼) is driven by CLK. This results in two currents, one related to the input signal and an extra one that is the same in both comparator branches. This extra current drastically speeds up the slew phase (Fig. 5b), speeds up the latch phase (Fig. 5c) and effectively increases the g_m of M6/7 and M4/5 (Fig. 5d and 5e). With V_{IN} = 0.8 mV and a 0.5*V_{DD} input common mode voltage, the performance of the g_m-boosted StrongARM comparator is compared to that of the standard comparator (Fig. 6). For V_{IN} < 1 mV, the regeneration phase is more than 30% faster (Fig. 6a), while its power consumption only increases by 10% (Fig. 6b). Common mode variations (from 0.4 V to 0.8 V) cause a 65 ps change in regeneration time (from 118 ps to 53 ps) in the StrongARM comparator, but only 10 ps (from 63 ps to 53 ps) in the g_m-boosted comparator (Fig. 6c). This enables the use of advanced switching schemes that require the comparator to operate at low common mode levels.

For a 1.8 Vpp-dif. amplitude input signal, the distribution of the comparator's input voltage is estimated in Fig. 7. The CAP-DAC gain is calculated from post-layout simulations. This makes it possible to correlate the comparator's operating region with the regeneration times shown in Fig. 6a, and thus verify that the proposed architecture is about 25.7% faster than the StrongARM comparator with the same device dimensions.

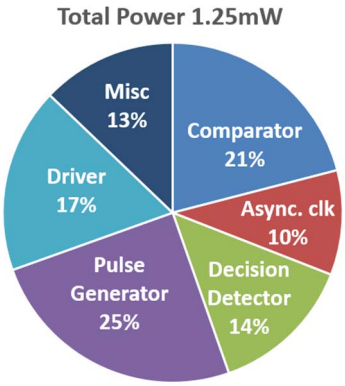

Fig. 10. Power composition of the proposed SAR ADC.

	This Work		[1]*	[2]*	[5]	[6]	[7]
Architecture	SAR		Flash+SD	Flash+SAR	TI-SAR	SAR	SAR
Technology	28 nm		28 nm	45 nm	28 nm	32 nm SOI	40 nm
Supply [V]	1	0.9	0.9	-	0.85/0.95	1	-
Sample rate [GS/s]	2	1.5	3.2	1.6	1.5	1.3	1
Latency [clock cycle]	1	1	1	1	2**	2**	1
Resolution [bits]	5	5	4	4	6	8	6
Vcm [V]	450 m		-	-	600 m	500-600 m	~VDD
Vcm input [V]	450 m		-	-	125 m	500-600 m	~VDD
Full scale amplitude [Vpp_dif]	1.8		-	-	500 m***	500 m	600 m
SNDR (HF) [dB]	27.4	30.3	25.8	25.8	34.8	39.3	34.6
SFDR (HF) [dB]	40.7	45	-	-	53.9	49.8	47.7
Power [mW]	2.12	1.25	11.75	6.1	1.43	3.1	1.26
FOM_W [fJ/conv.step]	55.4	31.2	229.5	238.3	21.2	34	28.7
Area [μm^2]	900		-	-	1500****	1500	580

* Only flash part is considered **Assuming 1 clock cycle to decode redundancy/lookup table
***Extracted from Vcm input ****Estimated from the reported photo

Table 1. Comparison Table.

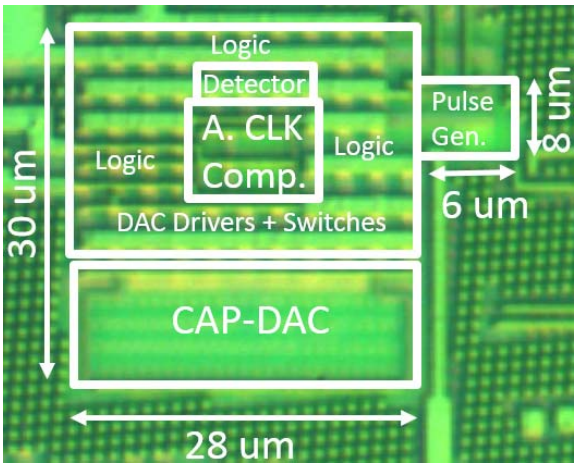

Fig. 11. Chip micrograph.

IV. Measurement Results

The prototype ADC is fabricated in 28 nm HPC CMOS and occupies an active area of 900 μm^2 (Fig. 11). When clocked at 1.5 GHz, it consumes 1.25 mW from a 0.9 V supply. Comparator and asynchronous clock consume 0.39 mW, decision detector, logic and DAC drivers consume 0.55 mW and the pulse generator consumes 0.31 mW. Fig. 10 shows the power consumption of the proposed ADC, where Misc includes the registers that hold the data after every conversion cycle and the logic block that generates CLK_en. Fig. 8a and 8b show the measured spectra (16k sample) for a 1.8 $V_{pp\text{-}dif}$ ($2*V_{DD}$) input signal and $0.5*V_{DD}$ common mode voltage. The ADC achieves 30.3 dB SNDR with a 1.5 GHz clock and 27.4 dB in the 2 GHz case. For the latter, Fig. 9 shows the SNDR and SFDR for input frequencies up to 960 MHz. As can be seen from Table 1, the proposed ADC achieves the highest sample rate for a non-time-interleaved SAR ADC, even though its full-scale amplitude is more than 3x higher than that of designs with comparable FOM_W.

V. Conclusion

This work demonstrates the implementation of a single-slice SAR ADC sampling at 2GS/s, the highest ever reported. This, together with a full-scale input amplitude of $2*V_{DD}$ and one clock cycle latency, makes the proposed ADC suitable for multi-stage, feedback and time-interleaved converter architectures. This result is enabled by a g_m-boosted StrongARM comparator, custom made SAR Logic and series capacitors. Even though it is optimized for state-of-the-art ADC architectures, its overall performance is among the state-of-the-art converters optimized for time interleaving.

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