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A Dynamically Reconfigurable Recursive Switched-Capacitor DC–DC Converter With Adaptive Load Ability Enhancement

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***Abstract*—Multiple voltage conversion ratio (VCR) recursive switched-capacitor (SC) dc–dc converters, based on several basic 2:1 converters, are widely used for on-chip power supplies due to their flexible VCRs for higher energy efficiency. However, conventional multiple VCR SC converters usually have one or more 2:1 converters unused for some VCRs, which results in lower power density and chip area wastage. This article presents a new recursive dc–dc converter system, which can dynamically reconfigure the connection of all on-chip 2:1 converter cells so that the unused converters in the conventional designs can be reused in this new architecture for increasing the load-driving capacity, power density, and power efficiency. To validate the design, a 4-bit-input 15-ratio system was designed and fabricated in a 180-nm BCD process, which can support a maximum load current of 0.71 mA and achieves a peak power efficiency of 93.1% with 105.3 μA/mm^2 chip power density from a 2-V input power supply. The measurement results show that the load-driving capacity can become 6.826×, 2.236×, and 2.175× larger than the conventional topology when the VCR is 1/2, 1/4, and 3/4, respectively. In addition, the power efficiency under these specific VCRs can also be improved considerably.**

***Index Terms*—DC–DC converters, fully integrated, multiple voltage conversion ratios (VCRs), recursive switched capacitor (RSC), switched-capacitor (SC).**

I. Introduction

In RECENT years, fully integrated power conversion systems have been favored by designers because of their smaller area and lower cost. Inductor, as a traditional energy storage device first caught the attention but soon the on-chip inductive power converter encountered some fatal problems. First, on-chip inductive converters require high-Q inductor for good efficiency, necessitating special masks and increasing manufacturing costs [1]. Second, integrating the inductor will introduce the large inductor's parasitic resistance and parasitic capacitance between the inductor and the silicon substrate, and also the skin effect in the windings [2], [3], [4]. Third, since the inductor-based converter requires complex control systems when supplying low power loads, the load power scaling is challenging, which limits the power efficiency. Capacitor, as another energy storage element, has shown better performance and it has been proved that capacitor-based dc–dc converters can achieve better power conversion efficiencies than integrated inductive converters [5], [6]. Hence, switched-capacitor (SC) power converters have successfully emerged as the best candidate to become the next generation of fully integrated on-chip power converters.

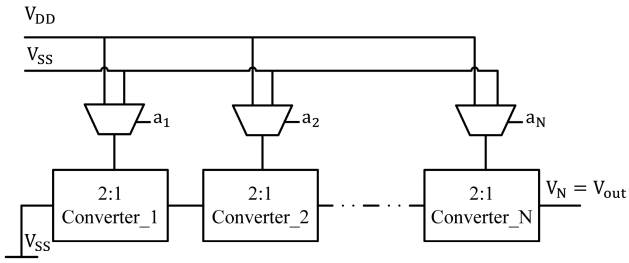

Fig. 1. Conventional recursive SC DC–DC converter [7].

However, the SC converters are only efficient at discrete ratios of input-to-output voltages, constricting efficient dynamic voltage scaling (DVS) to a small voltage range [8]. Using standard topologies to increase the voltage conversion ratio (VCR) numbers results in increased system complexity, power consumption, and extra switching elements [1]. Designing a circuit that can offer multiple VCRs has been proven to be a good solution (large DVS). In [9], a recursive switched-capacitor (RSC) dc–dc converter topology was proposed, which could realize high efficiency across a wide output voltage range by providing (2^N-1) conversion ratios using N 2:1 SC converter cells with minimal hardware overhead (VCR $= A/2^N$, A is the N-bit binary input VCR control signal and N is the cascaded stage number). Fig. 1 shows the principle diagram of the basic recursive SC converter. Based on this topology, Jung et al. [10] proposed a feedback

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TABLE I
RECONFIGURABLE VCR NUMBER OF DIFFERENT CASCADED STAGES

Cascaded Number (N)	VCR number	Reconfigurable VCR Number
1	1	0
2	3	1
3	7	1
4	15	3
...	...	...
N	2^N-1	$2^{int(N/2)}-1$

* int means round down.

loop using two separate sets of N-bit input control signals A and B, generating VCR $= A/(8+B)$. This design could have much more VCRs than the prior work. The aforementioned multi-VCR converter topologies can be employed in the modern System-on-Chips and Internet-of-Things devices to solve the battery degradation problem and then extend the battery lifetime.

Nevertheless, the 2:1 converter cells in an RSC-based dc–dc converter are typically not fully used under some specific VCRs; as a result, load-driving ability, power density, and power efficiency are limited. Considering the commonly used VCR $=$ 1/2 condition as an example, only the Nth converter operates, whereas the remaining $(N-1)$ converters are not in use. To address this problem, this article proposes a novel topology to make full use of every on-chip 2:1 converter in different VCRs. The connection of all on-chip 2:1 converters can be dynamically reconfigured, which means the unused converters in the conventional RSC designs can be reused and no converter cell is wasted. Compared with the conventional RSC converter, the equivalent output impedance of the proposed system can be improved significantly, resulting in a higher output power under some specific VCRs. The proposed converter has been designed and fabricated in a 180-nm BCD process. The measurement results show the dramatically increased load-driving capability and improved power conversion efficiency under certain VCRs.

The rest of this article is organized as follows. Section II gives the operation principle of the proposed system. Section III describes the detailed implementation of building blocks and highlights the theoretical analysis results. Then, the measurement results are presented in Section IV. Finally, Section V concludes this article.

II. PROPOSED TOPOLOGY

A. Operation Principle

This proposed topology aims to reconfigure the cascaded recursive converter topology into a paralleled converter circuit to make full use of every single-stage 2:1 converter. That means the more cascaded converter stages there are, the more VCR can be dynamically reconfigured. The relationship between the cascaded stage number and the reconfigurable VCR number is presented in Table I. For N cascaded stages, the reconfigurable VCR number could be generalized as follows:

$$RVN = 2^{\text{int}(N/2)} - 1. \quad (1)$$

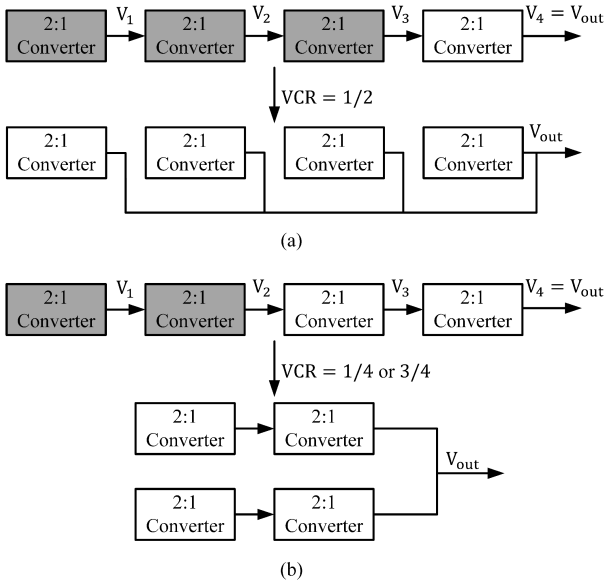

Fig. 2. Proposed dynamic reconfiguration scheme for (a) VCR $=$ 1/2 and (b) VCR $=$ 1/4 or 3/4.

Taking a four-stage cascaded recursive SC converter as an example, according to Table I, three VCRs can be dynamically reconfigured, which are VCR $=$ 1/2, 1/4, and 3/4, respectively. In these three specific VCRs in conventional RSC converters, only the last stage (VCR $=$ 1/2) or the last two stages (VCR $=$ 1/4 or 3/4) can be used, whereas the other converter cells are idle. Fig. 2 shows the reconfiguration process of the proposed system at these three VCRs, with the unused converter cells colored in gray. When VCR $=$ 1/2, this proposed converter is able to reconfigure the four-stage-series-connected converter system into a four-stage-parallel-connected converter system so that the previously unused converters can be fully used and, therefore, the load-driving capacity could be enhanced by at least four times. Similarly, when VCR $=$1/4 or 3/4, the topology also switches the series-connected system into a new parallel-connected system, and the load-driving capacity can be increased by at least two times. However, the real enhancement factor calculation is much more complicated because the unused converters affect the effective output impedance, although they are not outputting any power. Theoretically, if the unused converters are connected in parallel for VCR $=$ 1/4, 1/2, and 3/4 cases, the load-driving capacity should be enhanced by 2.125×, 5.3125×, and 2.125×, respectively. The detailed analysis is given in Section III-B.

A 4-bit 15-VCR converter system consisting of four 2:1 converter cells is designed to validate the proposed design. The top-level system architecture is shown in Fig. 3. The proposed system contains five main blocks: a four-level series 2:1 converter system, a converter-mode control block (VCR reconfiguration), a circuit reconfiguration control block, an output switch control block, and a CLK control block. The VCR of the system is controlled by an external 4-bit binary global input signal $\{a_{L4}, a_{L3}, a_{L2}, a_{L1}\}$. In these cases, the circuit reconfiguration control block produces a MUX control signal $\{\text{SW}_3, \text{SW}_2, \text{SW}_1\}$ to make the unused converter cells form new

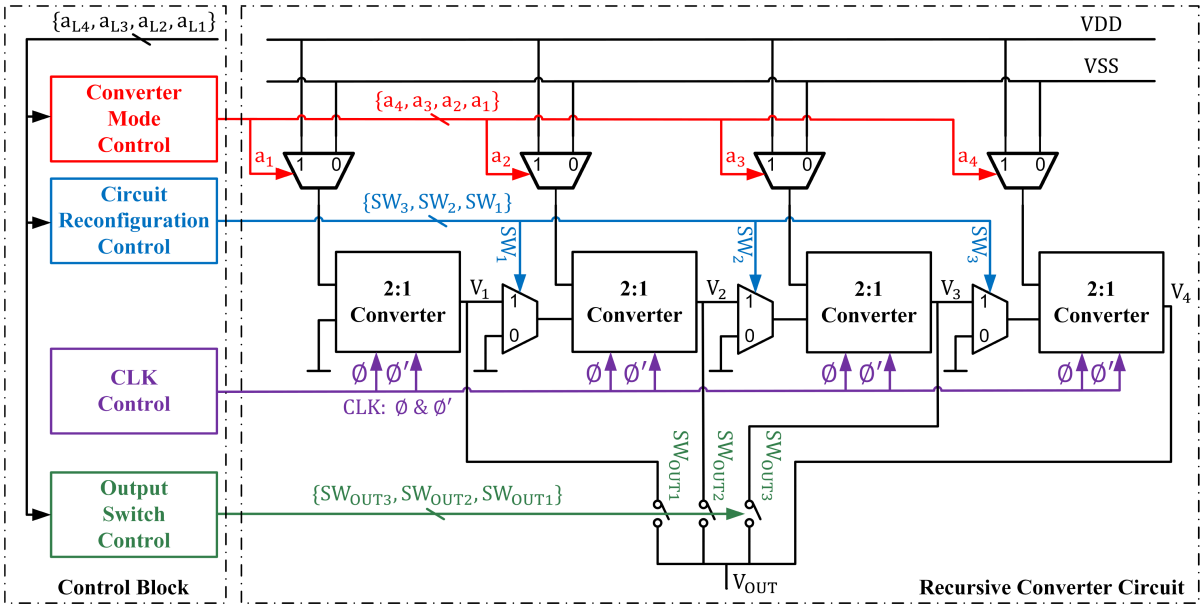

Fig. 3. Proposed system architecture.

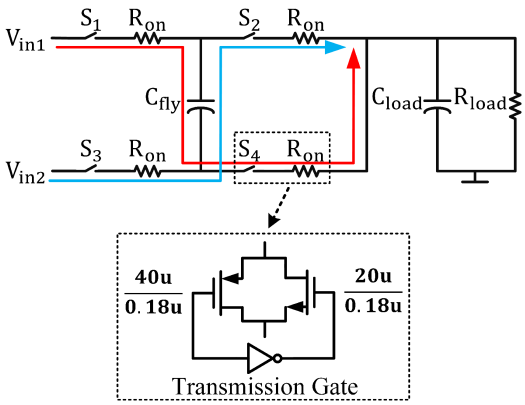

Fig. 4. 2:1 Converter cell.

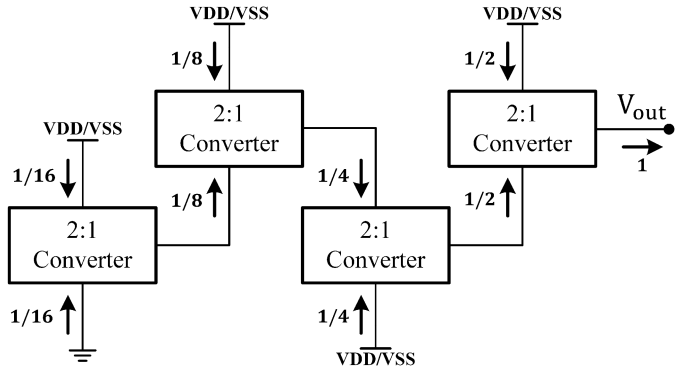

Fig. 5. Charge distribution of the conventional recursive SC [7].

submodules. Then, the converter-mode control block generates a new VCR control signal $\{a_4, a_3, a_2, a_1\}$ to control the conversion ratio of the new submodules. These processes could guarantee that all submodules have the same desired VCRs so that they can be reconfigured in parallel. The outputs of all 2:1 converters are connected to the total output V_{out} through a 3-bit controllable selecting signal $\{\text{SW}_{\text{out3}}, \text{SW}_{\text{out2}}, \text{SW}_{\text{out1}}\}$ to increase the total output current at specific VCRs, thus improving the system's load-driving capacity.

III. Circuit Implementation and Analysis

A. 2:1 SC Converter

1) Concept of the 2:1 SC Converter: In this section, the 2:1 SC converter unit is depicted in Fig. 4, which consists of a flying capacitor C_{fly} and four power switches with ON-state resistance R_{on}. The output consists of a decoupling capacitor C_{load} in parallel with the load resistor R_{load} [11]. Typically, the SC dc–dc converter operates in two phases under a pair of nonoverlapping gate control signals with a 50% duty cycle (could be slightly less than 50%, but the duty cycle of two phases should remain the same); the flying capacitor is switched between the charging phase 1 and the discharging phase 2 [12].

During the charging phase 1 shown as the red line in Fig. 4, the flying capacitor is in series between the input V_{in1} and the output V_{out} (switches S1 and S4 are ON). The charge from the input goes through C_{fly} that charges this capacitor up to $V_C = (V_{\text{in1}} - V_{\text{out}})$ and flows to the output [11].

During the discharging phase 2 shown as the blue line in Fig. 4, the flying capacitor is in parallel between another input V_{in2} and the output V_{out} (switches S2 and S3 are ON). The charge stored on C_{fly} in the previous phase is now transferred to the output. The V_{out} becomes the sum of the input and the capacitor voltage $(V_{\text{in2}} + V_C)$. Then, the overall output voltage can be determined as follows:

$$V_{\text{out}} = \frac{1}{2}(V_{\text{in1}} + V_{\text{in2}}). \tag{2}$$

Since the two inputs of the converter cell do not maintain the polarity during operations in this topology, transmission

TABLE II
R_{OUT} OF TOTAL SYSTEM

	VCR	R_{SSL}	R_{FSL}	$R_{out}=\sqrt{R_{SSL}^2+R_{FSL}^2}$	Enhancement factor $M_{Enhance}$
Original Recursive	$\frac{1\sim15}{16}$	$\frac{85}{256f_sC}$	$2.65625R_{on}$	$\sqrt{(\frac{85}{256f_sC})^2+(2.65625R_{on})^2}$	none
Proposed Design	$\frac{1}{2}$	$\frac{16}{256f_sC}$	$0.5R_{on}$	$\sqrt{(\frac{1}{5.3125})^2((\frac{85}{256f_sC})^2+(2.65625R_{on})^2)}$	5.3125
	$\frac{1}{4}$ or $\frac{3}{4}$	$\frac{40}{256f_sC}$	$1.25R_{on}$	$\sqrt{(\frac{1}{2.125})^2((\frac{85}{256f_sC})^2+(2.65625R_{on})^2)}$	2.125
	others	$\frac{85}{256f_sC}$	$2.65625R_{on}$	$\sqrt{(\frac{85}{256f_sC})^2+(2.65625R_{on})^2}$	1

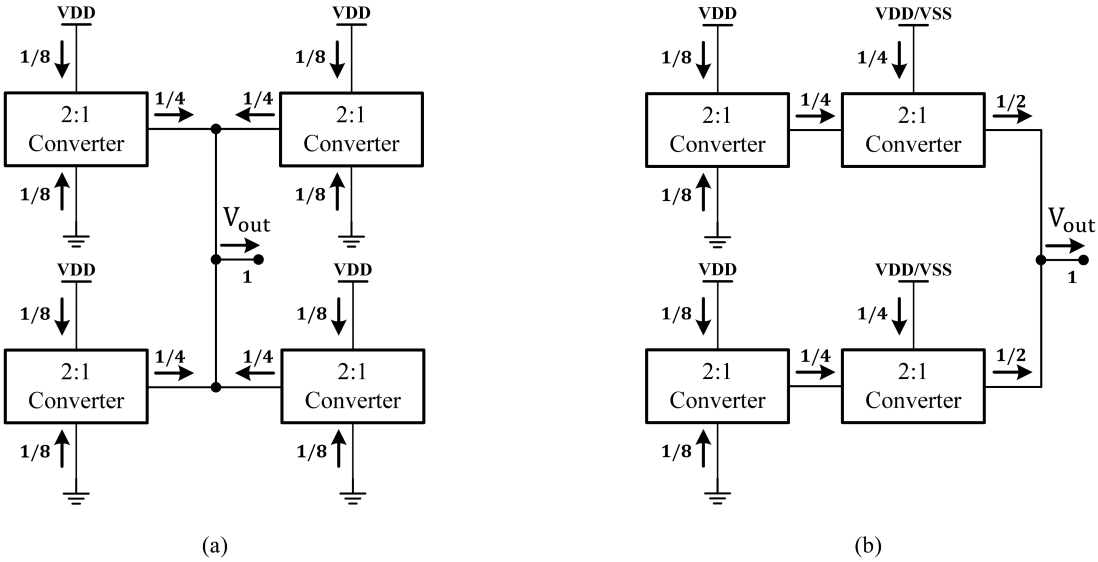

Fig. 6. Charge distribution of this reconfigurable recursive SC at (a) VCR = 1/2 and (b) VCR = 1/4 or 3/4.

gates with NMOS and PMOS switches, as shown in Fig. 4, are employed in this design to handle the different voltage polarities across the switches.

2) Analysis of Output Impedance: With the switching frequency f_s changes, the 2:1 converter will work in two asymptotic operating regions: the fast switching limit (FSL) and the slow switching limit (SSL) [13], [14]. By evaluating the power loss of these two operating regions when providing $I_{\text{load}} \neq 0$, the equivalent output impedance R_{out} can be found.

Assuming that the charge flows to the output in phase 1 and phase 2 is the same, equal to $0.5q_{\text{out}}$, the charge flowing through the flying capacitor C_{fly} and the load capacitor C_{load} is q_C and q_L, respectively. In the charging phase, the input V_{in1} charges these two capacitors and also contributes some charge to the output $q_{\text{in}} = q_C = 0.5q_{\text{out}} + q_L$. Note that, in steady state, the charge flowing through each of the capacitors must be of equal magnitude but opposite in both clock phases. That means in discharging phase, both of these two capacitors in this topology C_{fly} and C_{load} will contribute charge to the output as $0.5q_{\text{out}} = q_C + q_L$. Finally, the charge stored and released in the flying capacitor can be easily obtained as follows:

$$q_C = \frac{1}{2}q_{\text{out}}. \tag{3}$$

When analyzing the output impedance, here, the FSL would be considered first. That means the system is working in a very high switching frequency f_s, which will make the phase time much smaller than the time constant τ of this topology. In this mode, the flying capacitors only have a little time to be charged and discharged that means the capacitor's voltage can be modeled as constant and so does the current. The circuit power loss is related only to the conduction loss $P_{R_{\text{SW}}}$ when the charge flows through the ON-state resistance of the power switches [13]. By normalizing the conduction loss $\left(\sum_{i=1}^{4} 2R_i q_C^2 f_s\right)$ by the squared output current I_{out}^2, i.e., $(q_{\text{out}}f_s)^2$, the equivalent output impedance R_{FSL} could be given as (4). It is obvious that it is independent of switching frequency f_s and flying capacitance C_{fly}

$$R_{\text{FSL}} = 2R_{\text{on}}. \tag{4}$$

The SSL is just the opposite situation of the FSL. In this mode, the phase time is much larger than the time constant τ so that the capacitor could have enough time to be fully charged and discharged. In steady state, the current flowing through the capacitor becomes zero, so the energy loss when charging and discharging a capacitor is not related to the ON-state resistance of the power switch R_{on} anymore [13]. The total energy loss

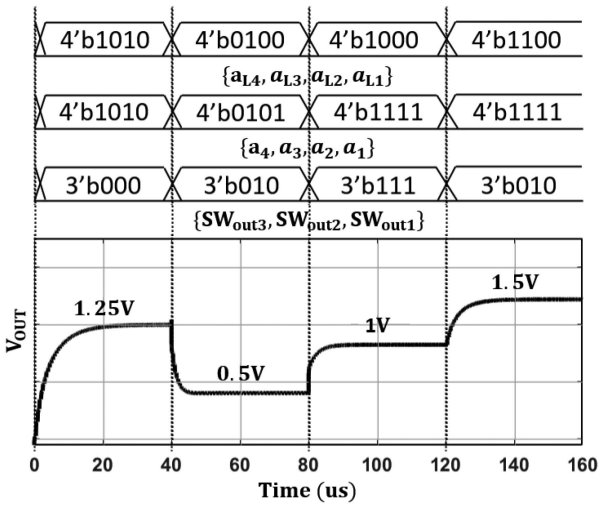

Fig. 7. Output voltage waveform.

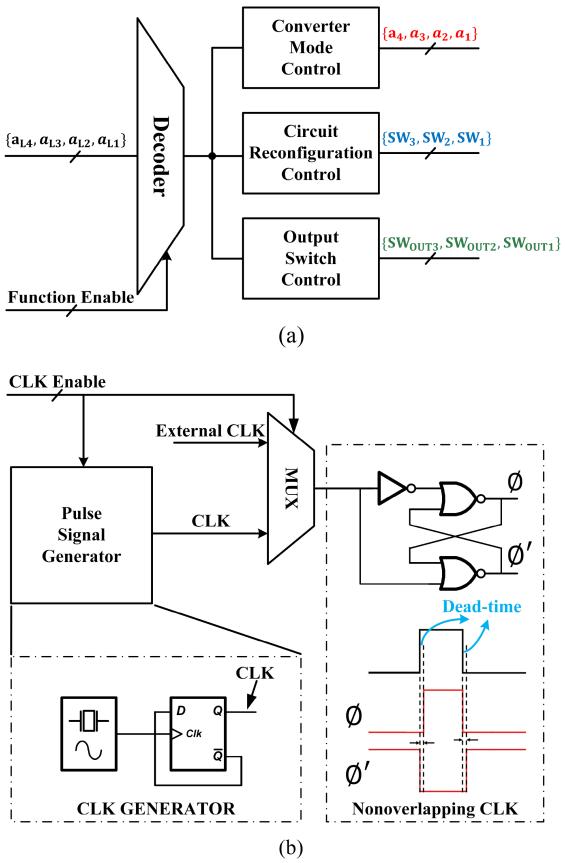

Fig. 8. Control block diagram. (a) Digital logic control signal generation block. (b) Gate-drive signal generation block.

through the converter can be found by adding the charge-sharing loss across each flying capacitor.

The practical flying capacitor used in circuits is not an ideal component with only capacitance. However, they can be treated to a very good approximation as being an ideal capacitor in series with a resistance and this resistance is defined as the equivalent series resistance R_{ESR} [15]. The charge-sharing loss $P_{C_{\text{fly}}}$ happens due to the conduction loss of the equivalent series

TABLE III
DIGITAL CONTROL BLOCK LOGIC

Voltage Conversion Ratio(VCR)	Global Input Signal	Converter Mode Signal	Circuit Reconfiguration Signal	Output Switch Signal
1/16	0001	0001	111	000
1/8	0010	0010	111	000
3/16	0011	0011	111	000
1/4	**0100**	**0101**	**101**	**010**
5/16	0101	0101	111	000
3/8	0110	0110	111	000
7/16	0111	0111	111	000
1/2	**1000**	**1111**	**000**	**111**
9/16	1001	1111	000	111
5/8	1010	1111	000	111
11/16	1011	1111	000	111
3/4	**1100**	**1111**	**101**	**010**
13/16	1101	1111	000	111
7/8	1110	1111	000	111
15/16	1111	1111	000	111

resistance R_{ESR} during converter operation [16], [17]. For the 2:1 converter topology, the charge-sharing loss can be simplified as q_C^2/C_{fly}. By also normalizing this loss by the squared output current I_{out}^2, the equivalent output impedance in SSL mode could be defined as follows:

$$R_{\text{SSL}} = \frac{1}{4f_s C_{\text{fly}}}. \tag{5}$$

B. Total System Analysis

The conventional recursive SC converter is based on a multistage 2:1 converter cascaded. Each flying capacitor, C_i, in the 2:1 converter cell has at least one input node connected to V_{DD} or V_{SS}. So, each converter has to load half of its output charge $q_C = 0.5q_{\text{out}}$ on the input from the previous converter cell and the power supply V_{DD} or V_{SS}. For an N-stage cascaded recursive converter, each converter stage is loaded with an output charge $q_{\text{out},i}$ that is divided by a binary weight of the total output charge q_{out}, which is $q_{\text{out},i} = q_{\text{out}}/\left(2^{N-i}\right)$[9]. By using the same analysis method from Section III.A-2, the SSL mode R_{SSL} and the FSL mode R_{FSL} of an N stage RSC system could be summarized as (6) and (7), respectively

$$R_{\text{SSL}} = \sum_{i=1}^{N}\sum_{j=1}^{4}\left(\frac{1}{2^{N-i+1}}\right)^2 \frac{1}{f_s C_i} \tag{6}$$

$$R_{\text{FSL}} = \sum_{i=1}^{N}\sum_{j=1}^{4}\frac{1}{2}\left(\frac{1}{2^{N-i}}\right)^2 R_{i,j}. \tag{7}$$

It is worth noting that for the conventional RSC converter system, as long as the number of recursion depth N is determined, the charge distribution of each stage can be fixed as Fig. 5. That means, no matter how the VCR changes, the equivalent output impedance would theoretically remain the same, which is presented in Table II.

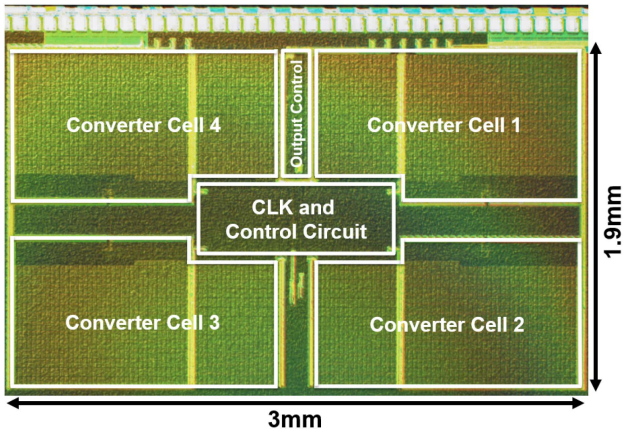

Fig. 9. Chip micrograph.

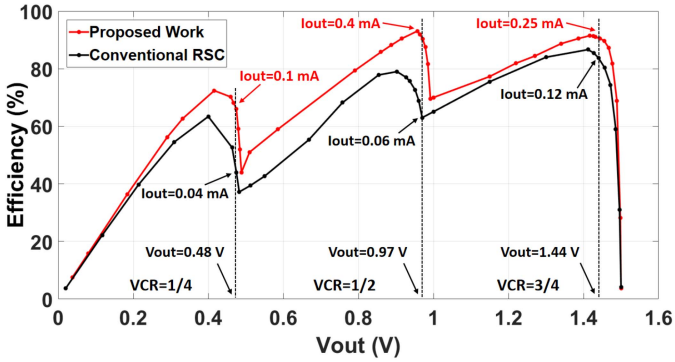

Fig. 10. Efficiency versus V_{out}.

While for the proposed design in this article, the originally fixed charge distribution is now changed by reconfiguring the circuit structure under some specific VCRs. Fig. 6 shows the new charge distribution at VCR = 1/2 (left) and VCR = 1/4 or 3/4 (right) when recursion depth $N = 4$. Through the identical equivalent impedance analysis method, the R_{SSL} and R_{FSL} of the reconfigured circuit can be calculated, as shown in Table II, where M_{Enhance} is the enhancement factor, which refers to the ratio of the equivalent output resistance between the conventional RSC system and this reconfigurable one. M_{Enhance} directly reflects the enhancement of the load-driving capacity under these three VCRs. Theoretically, for VCR = 1/2, the load-driving capacity is improved to 5.3125×, whereas for VCR = 1/4 or 3/4, a 2.125× increment is realized.

C. Control Block

1) Logic Control Block: The logic control blocks include the converter-mode control, the circuit reconfiguration control, and the output switch control blocks, as shown in Fig. 3. The output control signals of these three blocks are generated from the 4-bit global input signal $\{a_{L4}, a_{L3}, a_{L2}, a_{L1}\}$. This 4-bit global input gives the desired VCR for the proposed system. The three logic control blocks translate this 4-bit VCR signal into different configuration signals to determine the actual VCR for each 2:1 converter cell, the parallel-series circuit connections,

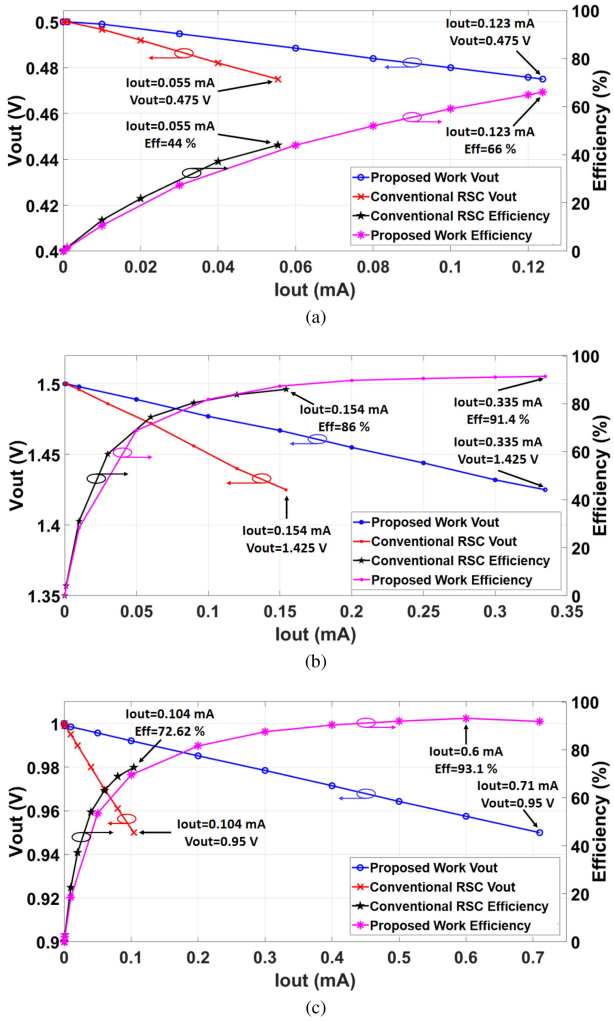

Fig. 11. V_{out} and efficiency versus load current.

TABLE IV
MEASUREMENT OF OVERALL OUTPUT IMPEDANCE R_{OUT}

	VCR	Conventional RSC	Proposed RSC	Theoretical Factor	Measured Factor
R_{out}	2:1	485Ω	71.05Ω	5.3125	6.826
	4:1	451Ω	201.7Ω	2.125	2.236
	4:3	486Ω	223.45Ω	2.125	2.175

and which converter cells are connected to the global output V_{out}, respectively.

Table III presents the signal translation of each logic control block for different VCRs. In this 15-VCR four-stage converter architecture, this proposed system can be dynamically reconfigured under three specific VCRs in bold to achieve higher load-driving ability.

The simulated waveform of the global 4-bit input signals, some key control signals, and the output voltage are shown in Fig. 7. At the first period, the global input signal is $\{a_{L4}, a_{L3}, a_{L2}, a_{L1}\} = 4'b1010$ (VCR = 10/16, $V_{\text{out}} = 1.25$ V), the output switching signal is $\{\text{SW}_{\text{out3}}, \text{SW}_{\text{out2}}, \text{SW}_{\text{out1}}\} = 3'b000$, and only the fourth 2:1 converter is connected to the global output and all the converter

TABLE V
STATE-OF-THE-ART COMPARISON

Design	This Work	2019 [18]	2018 [19]	2016 [10]	2015 [20]	2014 [9]	2013 [21]
Technology	180 nm	250 nm	130 nm	180 nm	250 nm	250 nm	180 nm
Topology	Reconfigurable Recursive	Asymmetrical Shunt	Fixed	Rational	Gear Train+ Charge Feedback	Recursive	Successive-approximation
Number of Ratios	15	187	3	79	24	15	117
Circuit Dynamical Configuration	Yes	No	No	No	No	No	No
Maximum Converter Reuse Times	4	1	1	1	1	1	1
Input Voltage	2 V	3.3 V	1.2 - 2.3 V	2 V	2.5 - 5 V	2.5 V	3.4 - 4.3 V
Output Voltage	0.12 - 1.8 V	0.4 - 2.8V	0.9 V	0.13 - 1.87 V	0.2 - 2 V	0.1 - 2.18 V	0.9 - 1.5 V
Max. Load Current	0.71 mA	10 mA	0.49 mA	N/A	60 mA	2 mA	0.3 mA
Capacitor Type	MIM On-Chip	MIM On-Chip	MOS On-Chip	MIM On-Chip	SMD Off-Chip	MIM On-Chip	MIM+MOS On-Chip
Peak Efficiency (η_{peak})	93.1%	87%	80.4%	95%	95.5%	85%	72%
Power Density @ η_{peak} ($\mu A/mm^2$)	105.3	1120.4	3550	71.4	2881.8 (Off-chip caps)	430.6	5.9
Chip Area (mm^2)	5.7	7.14	0.138	3.36	3.47	4.645	1.69

cells are connected in series. Then, the global input signal $\{a_{L4}, a_{L3}, a_{L2}, a_{L1}\}$ turns to $4'b0100$ (VCR = 1/4, $V_{\text{out}} = 0.5$ V), $\{\text{SW}_{\text{out3}}, \text{SW}_{\text{out2}}, \text{SW}_{\text{out1}}\}$ switches into $3'b010$, indicating that the system is split into two submodules (each submodule has a two-cascaded converter) and the output of the second and fourth converter cells V_2 and V_4 is connected to the global output. Finally, the converter-mode control signal $\{a_4, a_3, a_2, a_1\}$ becomes $4'b0101$ to make sure that the two new submodules could realize VCR = 1/4. Therefore, the load-driving capacity could be enhanced by 2.125× theoretically. The system should now operate as the reconfiguration, as shown in Fig. 2(b).

Then, $\{a_{L4}, a_{L3}, a_{L2}, a_{L1}\}$ becomes $4'b1000$ (VCR = 1/2, $V_{\text{out}} = 1$ V). The converter-mode control block creates a new input control signal $\{a_4, a_3, a_2, a_1\} = 4'b1111$ so that each converter achieves the VCR = 1/2. And $\{\text{SW}_{\text{out3}}, \text{SW}_{\text{out2}}, \text{SW}_{\text{out1}}\}$ changes into $3'b111$, which means all reconfiguration switches are used now. As a result, the proposed design makes full use of each 2:1 converter to increase the load-driving capacity by 5.3125×. This is the case shown in Fig. 2(a).

2) CLK Control Block: Fig. 8 bottom part presents the CLK control block that includes a pulse signal generator, CLK selector, and a nonoverlapping CLK generator. The pulse signal generator contains a ring oscillator and a D flip-flop. After the ring oscillator generates a sine wave with a suitable frequency f_s, the D flip-flop is used to shape it into a square wave with a duty cycle of 50%. Also, the D flip-flop only consumes very little energy, which is good for energy efficiency. In addition to the internal CLK from by pulse generator, this block also has an external CLK. These two CLKs can be selected by a 1-bit CLK Enable signal at the MUX. In the nonoverlapping CLK generation circuit, the selected CLK is translated into a pair of interleaved signals ϕ and ϕ' with sufficient deadtime to control the operation of the entire system. This can avoid the simultaneous conduction of power transistors during switching transitions so that the short-circuit power loss in converters can be eliminated.

IV. MEASUREMENT RESULTS

Fig. 9 shows the chip micrograph. The proposed system has been fabricated in a 180-nm BCD process, occupying 5.7 mm^2 active chip area (1.9 mm × 3 mm). The proposed system has been made fully on-chip integrated, and on-chip metal-insulator-metal (MIM) capacitors are used for flying capacitors, which are 4 nF in total (1 nF in each 2:1 converter cell). Finally, all measurements were tested under a clock frequency of 1 MHz and the overall input was a dc voltage of 2 V.

Fig. 10 illustrates the power transfer efficiency versus the output voltage change. Since the figures for the proposed design and conventional design are the same for the VCRs not needing reconfiguration, this figure only focuses on the reconfigurable VCRs, which are 1/4, 1/2, and 3/4. It can be seen from the curve that when the output voltage is the same, the load current of this work is much larger than that of the conventional RSC because the idle converter cells are fully used through reconfiguration. Besides, for these three VCRs, the power conversion efficiency of the proposed design has been comprehensively improved over the entire output voltage range. This is because the input and output power has been significantly improved while the energy loss of the entire system remains unchanged; as a result, the impact of nonideal energy loss on efficiency becomes smaller in this case.

The figures of the power transfer efficiency and the output voltage versus the change of the load current under VCR = 1/4, 1/2, and 3/4 are plotted in Fig. 11. Here, we define that the valid output should be larger than 95% of the desired output voltage. In Fig. 11(a), VCR = 1/4, when the efficiency reaches peak value and the output voltage is drawn down to near 95% of preferred output voltage (0.5 V), the load current of the proposed and conventional RSC converters are 123 μA and 55 μA, respectively. It can be seen that the load-driving capacity becomes almost 2.236× larger with the proposed design in this case. The VCR = 3/4 has a similar condition to the previous VCR, which is shown

in Fig. 11(b), but the measured load-driving enhancement is 2.175×. Fig. 11(c) gives the results when VCR = 1/2. When the efficiency achieves the peak value, the proposed work can attain 93.1% efficiency under $I_{\text{out}} = 600\,\mu$A and the conventional RSC can only have 72.62% efficiency under $I_{\text{out}} = 104\,\mu$A. In addition, when output voltage deteriorates to 950 mV (95% of preferred output voltage, 1 V), the load current of the proposed work is 710 μA, which is larger than 104 μA when using the conventional RSC. It can be seen that the load-driving capacity under VCR = 1/2 is improved by around 6.826×, thanks to the four converter cells reconfigured to be connected in parallel.

The load-driving capacity can be reflected by the equivalent output impedance R_{out} of the entire circuit. Based on the measurement results of V_{out} versus I_{out} in the previous paragraph, the equivalent output impedance under these three VCRs can be calculated and shown in Table IV. The factor, referring to the ratio of the equivalent output impedance between the conventional and proposed RSC converter, indicates the enhancement of the load-driving capacity. It can be found that for VCR = 1/4 and 3/4, the measured factors 2.236 and 2.175 are slightly larger than the theoretical factor 2.125, but they are still close. While for VCR = 1/2, the measured factor 6.826 is much larger than 5.3125. The reasons for these variations are explained as follows: First, in the total equivalent output impedance analysis, the ON-resistance of all switches used for the reconfiguration function must also be taken into account and will dramatically influence the overall impedance. In addition, in the layout design, the wire resistance and the parasitic capacitor introduced between different metal layers will also have a great impact on the final equivalent output impedance.

Table V gives the comparison of key performance between this work and conventional designs. One improvement of the proposed design is the dynamically reconfigurable connection of all 2:1 converter cells according to the desired VCR. The conventional RSC designs were fixed topology using four 2:1 converter cells in series, which results in lower load-driving capacity and unused on-chip area. In addition, the proposed design has a peak efficiency of 93.1%, which is among the highest in all fully on-chip integration designs. Only Jung et al. [10] realized a higher peak efficiency, but the output power at peak efficiency of the proposed design achieves almost four times larger than that design, thanks to the circuit reconfiguration function.

V. Conclusion

This article proposes a dynamically reconfigurable RSC dc–dc converter with adaptive load ability enhancement. The presented topology can make full use of each 2:1 converter of a multi-VCR system by dynamically reconfiguring the connection of all the 2:1 converter cells. The reconfigurable VCR number can be determined as $(2^{\text{int}(N/2)} - 1)$ for N cascaded recursive converter system. Through this method, the load-driving capacity under specific VCRs can be significantly enhanced; in addition, the power transfer efficiency can also be further improved.

A fully integrated dynamically reconfigurable four-stage recursive SC converter was designed and fabricated in a 180-nm BCD process to experimentally validate the enhancement of the load-driving ability and power efficiency. The measurement results show that the maximum load-driving current is around 0.71 mA and the power density of this converter system under a peak efficiency of 93.1% is 105.3 $\mu\text{A}/\text{mm}^2$. In addition, the proposed circuit has an energy efficiency greater than 80% over a wide output range. Most importantly, the load-driving capacity under some VCRs is significantly increased by up to 6.826× compared with the conventional RSC topology.

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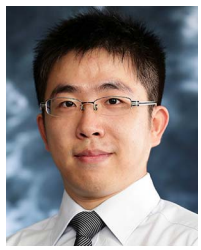

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