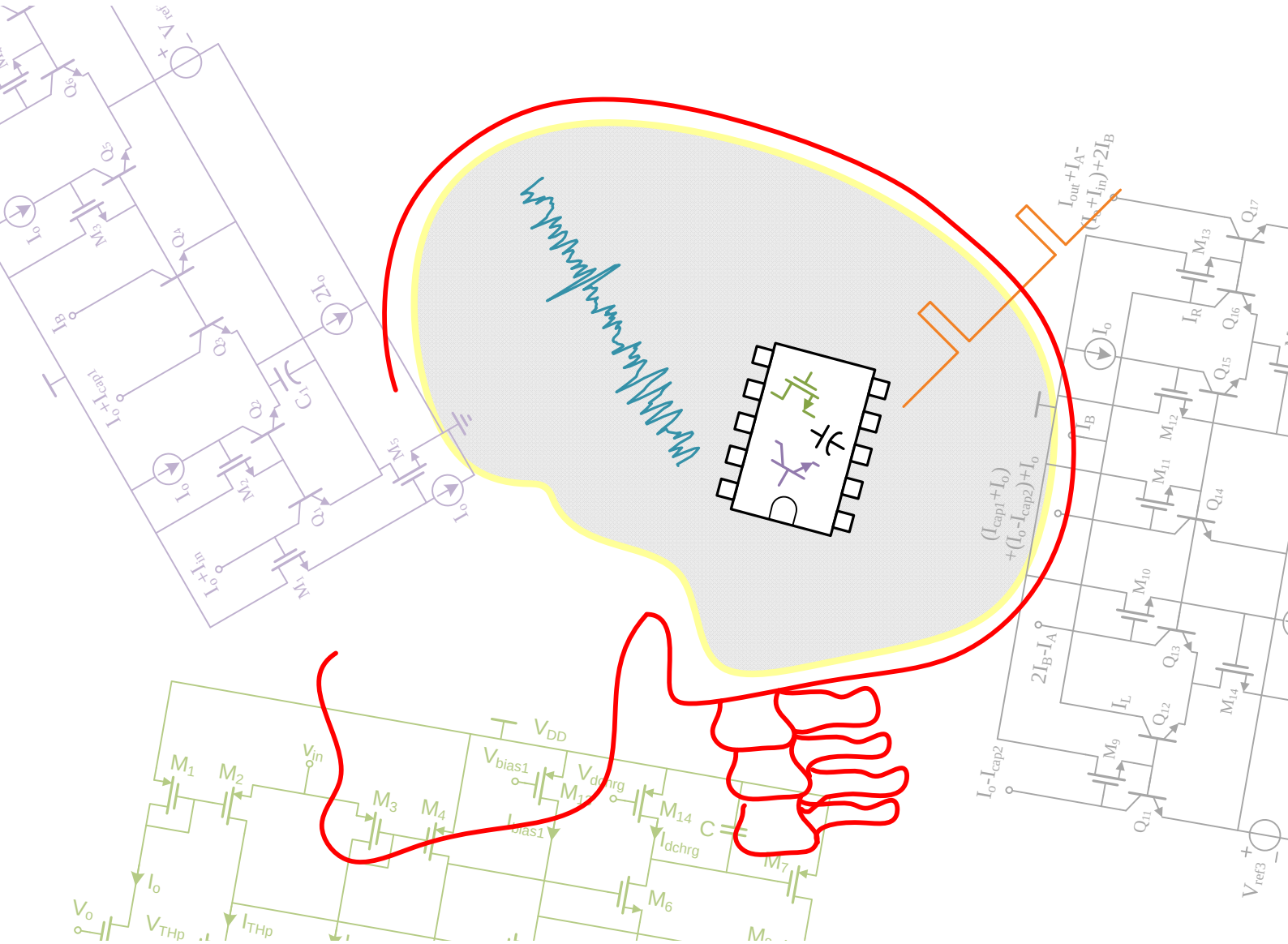
ULTRA LOW-POWER ANALOG INTEGRATED CIRCUITS FOR EXTRACELLULAR ACTION POTENTIAL DETECTION

SENAD HISENI



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ULTRA LOW-POWER ANALOG INTEGRATED CIRCUITS FOR EXTRACELLULAR ACTION POTENTIAL DETECTION

by

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A thesis submitted to the Department of Microelectronics,
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Education is what remains after one has forgotten what one has learned in school.

— Albert Einstein (1879 - 1955)

To My Parents

Mojim Roditeljima

ABSTRACT

An action potential or spike detector is an important part of neural recording implants. The detector performs on-chip data reduction by trying to capture only relevant information (real occurrences of the action potential) from the recorded signals. This data selection is indispensable since it helps reducing data rate as well as operating power for wireless data transmission of the neural sensor. This thesis explores the possibility of improving detections and reducing power consumption of neural spike detectors. As a result, two designs are presented in this thesis.

First, the dynamic translinear realization of the nonlinear second-order differential equation describing the nonlinear energy operator performing the real time energy detection of analog signals is presented. The spikes are isolated from the background noise as the energy of the spikes is considered to be different from the background noise. The quiescent power consumption equals 7.2 μW. The expected behavior of the designed nonlinear energy operator is demonstrated by means of simulations.

In addition, an ultra low-power CMOS analog circuit for detection of APs embedded in noisy signals is presented. The proposed strategy isolates APs by detecting subsequently a positive and a negative spike of each AP. An AP is detected only if the positive spike is detected within a short period of time after the negative spike was detected. The final circuit operates from a 1-V supply and consumes only 1.5 nA. The detector is verified by means of simulations with synthetic neural waveforms and is able to successfully detect APs in noisy signals. In addition, the 1.5 nW power dissipation is by far the smallest among action potential detectors reported in the literature.

ACKNOWLEDGMENTS

The work presented in this thesis could not have been done without the help and influence of many individuals.

First of all, I would like to express profound gratitude to my supervisor, Dr.ir. Wouter Serdijn, for his invaluable support, encouragement, supervision and useful suggestions throughout this research work. His importance for this thesis as for my personal development is inexpressible. Dr.ir Wouter Serdijn you are an amazing teacher and an example for me. You have shared with me your passion for science, your philosophy of life and your sense of humor. Thank you for everything!

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I wish to express my love and gratitude to my brother and sister for their understanding, support and love, especially through the duration of my studies.

My greatest thanks to my parents. Baba i mama, hvala Vam što ste insistirali da me izvedete "na pravi put", i u uslovima koji nisu bili uvijek idealni. Hvala Vam što uvijek vjerujete u mene.

Last but not least, words alone cannot express the thanks I owe to my wife, Aida. Her endless love, support, encouragement and assistance enabled me to complete this work. In particular, the previous sentence could not be put any better without her assistance.

Senad Hiseni

Delft, the Netherlands
January 8, 2010

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INTRODUCTION

1.1 MOTIVATION

The brain is the control center of the central nervous system. It is the most complicated organ in the human body. The human brain contains roughly 15-33 billion neurons depending on gender and age [6]. The property that makes neurons so important is that they are capable of sending signal pulses called Action Potentials (APs) to each other over long distances, and by doing so, they form neural networks. These networks are comparable to electrical circuits because they contain circuit elements (neurons) connected by biological wires (nerve fibers). Typically neurons connect to at least a thousand other neurons forming complex circuits. These highly specialized circuits make up systems which are the basis of our perception, different types of action, and other important functions. Because of this complexity and the fact that brain is the control center of the central nervous system we can conclude that even small deviations or defects in the brain can have huge impacts on human's health. Currently, diseases like depression, epilepsy, Parkinson's disease, Alzheimer's disease, dystonia and many others are treated conventionally using drugs and surgery. However, a drug does not have the same effect on everyone and they often produce harmful side effects. Recent advances in microprocessors, biocompatible materials, batteries, Radio Frequency (RF) communications and software are now combining to produce devices which can be used for neurostimulation in order to treat various diseases.

1.2 PURPOSE AND THE SCOPE OF THE RESEARCH

Neuroscientists and neuroprosthetic devices require often real-time monitoring of biopotential activity of multiple neurons. Due to advances in MicroElectroMechanical System (MEMS) electrode arrays technology and integrated Complementary Metal-Oxide-Semiconductor (CMOS) electronics, sensing devices of 100 or more electrodes are possible [7, 8, 9]. Fig. 1.1 shows a block diagram of such generic wireless neural recording device [1]. A bank of amplifiers must be used to boost the weak signal measured by each electrode. Differential amplifiers are used to measure the potential of each signal electrode with respect to a large, low-impedance reference electrode. In some recording applications, multiple reference electrodes are used, and a small number of signal electrodes are paired with a nearby high-impedance reference electrode.

Efforts to develop fully implantable sensing devices bring along several circuit design challenges. Such clinical devices need to be as less intrusive as possible. Recorded data needs to be transmitted wirelessly to avoid tissue infections. Yet the power consumption of small implantable devices needs to be minimized to prevent heating and damage to nearby cells. Safety, power consumption and limited area are important parameters that need to be satisfied.

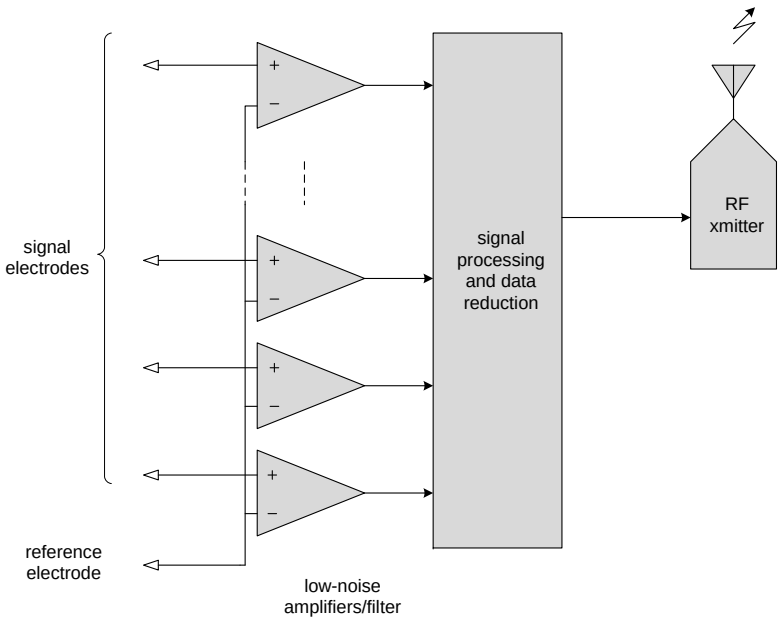


Figure 1.1: Block diagram of wireless neural recording device [1].

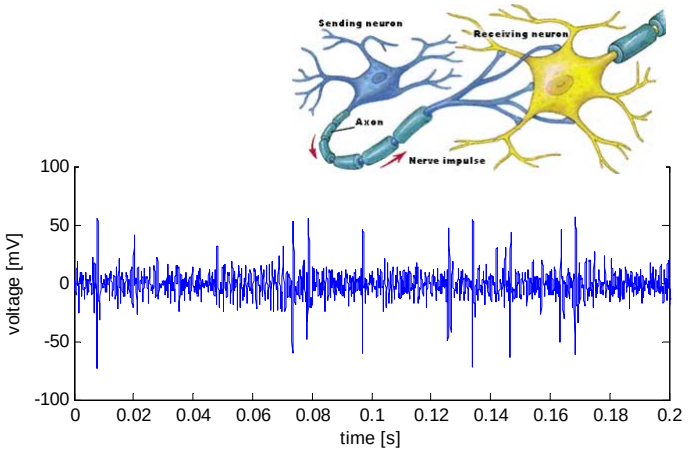
In modern recording systems, raw data rates of 15 Mb/s or more are easily produced [7]. Micropower wireless circuits cannot transmit information at such high rates, so data reduction must be performed in the implanted device. By detecting APs in low density neural waveforms and transmitting only relevant data, we can greatly decrease the power consumption of implantable devices [10]. Alternatively, automatic AP detection can be used to trigger recording around each AP [11]. By detecting APs close to the electrodes we can also help classifying APs and distinguish between different neurons. The remaining problem is how to perform this automatic AP detection from a noisy neural waveform in a small, low-power device.

1.3 THESIS ORGANIZATION

This thesis focuses on the design and implementation of a fully implantable AP detectors. Chapter 2 provides more detailed information about the nature of neural signals. Chapter 3 compares various spike detection algorithms, discusses previous work and the current approach. In Chapter 4, the dynamic translinear realization of the nonlinear second-order differential equation describing the nonlinear energy operator performing the real time energy detection of analog signals is presented. Chapter 5 concentrates on the circuit design of an ultra low-power circuit for dual threshold AP detection. Finally, Chapter 6 concludes the thesis with a summary of research results and discussion of future work directions.

2

THE NATURE OF NEURAL SIGNALS



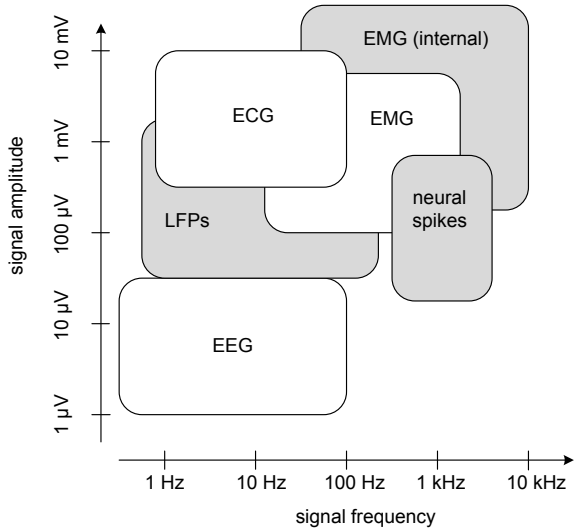


Figure 2.1: Approximate frequency content and amplitude distribution of common biopotentials recorded from the surface of the skin (white boxes) or internally (shaded boxes) [2].

Electrically active cells, in the human body, can produce a wide variety of electrical signals. The approximate frequency content and amplitude distribution of common biopotentials, which are of medical and scientific interest, are shown in Fig. 2.1. The frequency and amplitude of these signals span over more than four decades. The frequency can be found in the range from around 100 mHz to around 10 kHz and the voltage amplitude can be found in the range from 1 µV to over 10 mV. However, as this thesis concentrates on signals produced by neurons, ElectroCardioGraphy (ECG) and ElectroMyoGraphy (EMG) signals will not be treated.

The ElectroEncephaloGraphy (EEG) signal, produced by neurons, is easily recorded by using multiple electrodes placed on the scalp. Fig. 2.2 illustrates external electrodes used to measure the EEG. The main diagnostic application of the EEG is in the case of epilepsy, as epileptic activity can create clear abnormalities on a standard EEG study [12]. In contrast to EEG signals, Local Field Potentials (LFPs) signal and neural spikes or APs also produced by neurons need to be measured internally. Their internal voltages are in the order of 100 mV when compared to the extracellular space [13].

Using individually guided micro-electrodes, it is possible to obtain very precise intracellular recordings. However, in order to zoom in to more relevant data and to monitor greater area, it is necessary to use multielectrode arrays. Fig. 2.3 shows such a multielectrode array. By using multielectrode arrays, we measure the smaller extracellular potentials several micrometers from the cell. In that case, the contact between metal electrode tip and extracellular fluid creates an electrical double layer resulting in electrode-tissue interface behavior primarily as a capacitance for small voltages [14]. The capacitance values of the interface are between 150 pF – 1.5 nF, depending on electrode area and surface roughness. Fig. 2.4 shows a

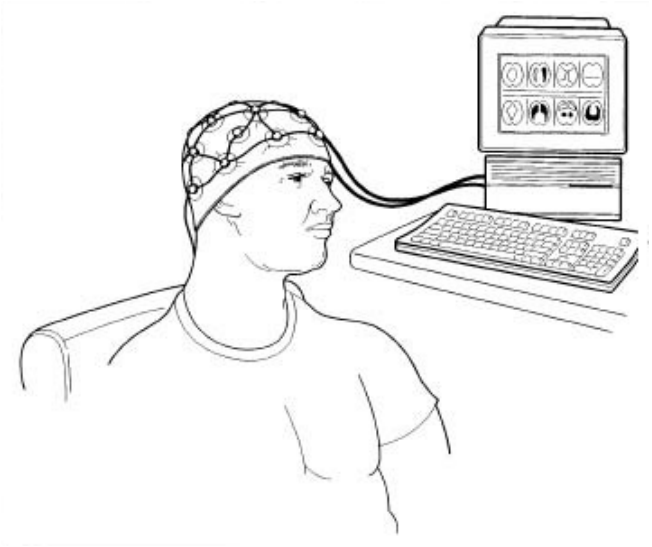


Figure 2.2: External electrodes to measure EEG [3]

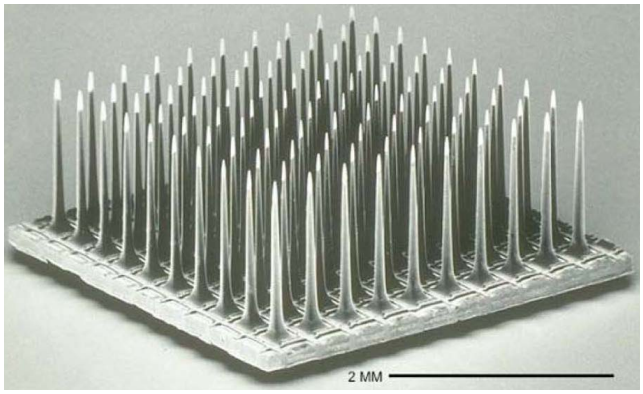


Figure 2.3: Scanning electron micrograph of silicon-based Utah Electrode Array [4]. The 100-electrode array measures 4 x 4 x 1.5 mm^3.

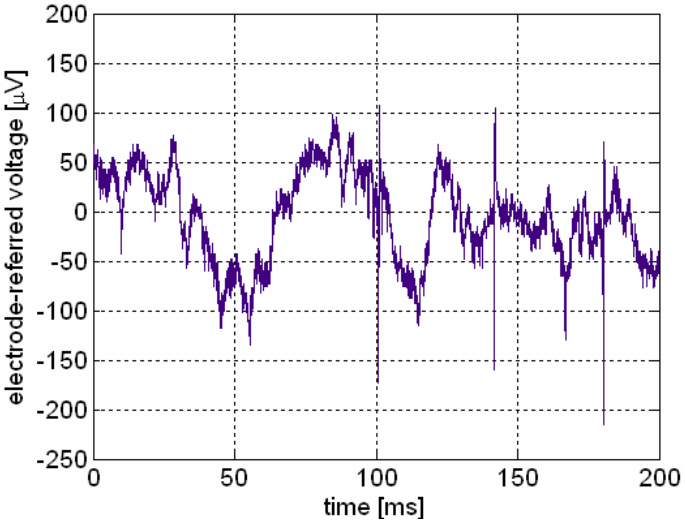


Figure 2.4: Neural recording from cat motor cortex using Utah Electrode Array.

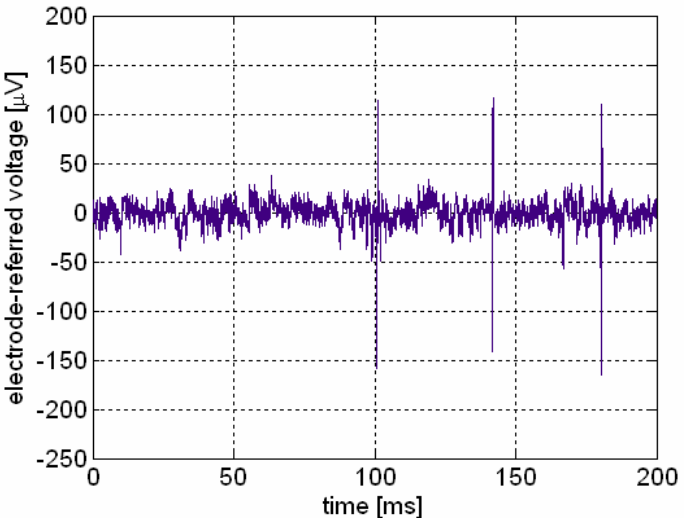


Figure 2.5: Data from Fig. 2.4 after a 300-Hz one-pole high-pass filter was applied in software to remove LFPs and preserve spikes.

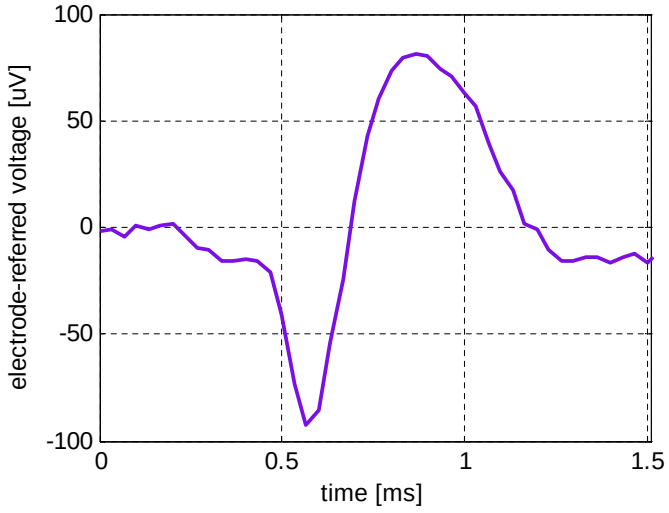


Figure 2.6: Single AP measured using multiple electrodes

typical trace from an extracellular neural recording. This waveform was recorded from the motor cortex of an awake cat using the Utah Electrode Array as depicted in Fig. 2.3 and contain both APs and LFPs. Since LFPs occupy frequencies range from approximately 100 mHz – 200 Hz, while APs have energy concentrated in the 300 Hz – 5 kHz range, linear filtering can be used to separate them. In Fig. 2.5 we can see a high-pass filtered neural waveform of the typical extracellular recording with the amplitude of the action potential signal in the order of 100 µV. At times t = [100, 140, 180] ms the APs from a adjacent neuron can be seen, while a more distant neuron fires APs at 10 ms and 167 ms.

2.1 LOCAL FIELD POTENTIALS

The LFPs have low-frequency, less than 200 Hz, oscillations. They emerge from the synchronous activity of many neurons in one region of the brain. The crowded noise of many neighboring neurons creates a large signal that is easily detected in comparison to the not resolvable individual APs from neurons that are too far from the electrode [15]. It has been demonstrated that the energy of LFP signals in the primate premotor and motor cortex, responsible for the sensory guidance of movement and control of proximal and trunk muscles of the body, correlates with specific arm movement such as direction, distance and speed. As a result, the LFP may be useful in neuroprosthetic applications [16, 17, 18, 19]. In comparision to the APs, the LFPs are a robust signal and this has been proven in some experiments, where electrode arrays were used. Scar tissues, which are formed around micro-electrode tips tend to attenuate spike signals from nearby neurons, however LFPs signals are less affected [20].

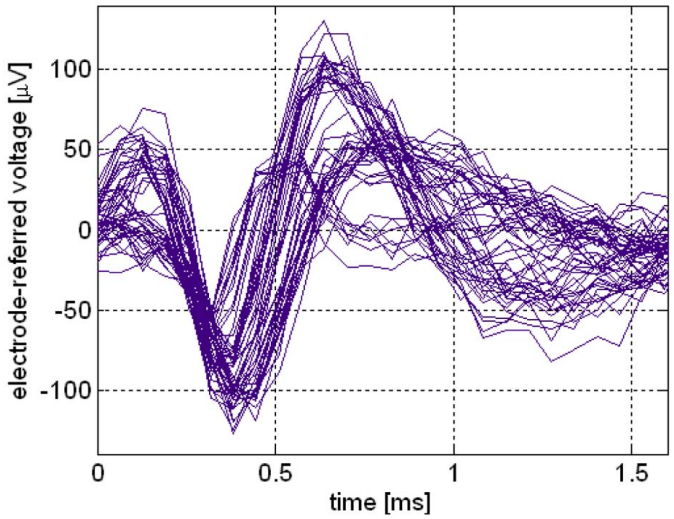


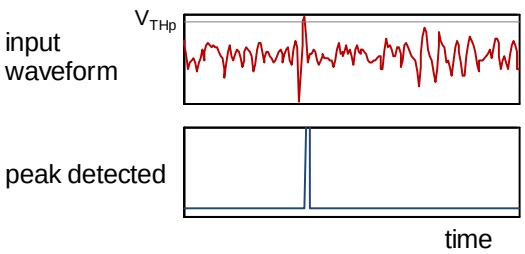
Figure 2.7: 51 time-aligned APs. Three distinct neurons are visible.

2.2 ACTION POTENTIALS

In extracellular recordings, the APs often appear biphasic and usually have durations of 0.3 ms – 1.0 ms. Typical shape of an AP recorded using multi-electrode arrays is shown in Fig. 2.6. Neurons rarely fire more than 100 APs per second. The firing rates are around 10 Hz which are typical for the cerebral cortex, the structure within the brain that plays a key role in memory, attention, perceptual awareness, thought, language, and consciousness. APs that are produced by neurons have nearly identical amplitude and duration, and information is encoded not in the shape but in the timing of APs [13]. Clearly, the APs can be considered as "digital" events. For multielectrode arrays, that are placed in the brain, it is common that some electrodes detect APs from two to four distinct neurons, while other electrodes may see no resolvable APs. 51 time alligned APs are shown in Fig. 2.7. Depending on the distance between neuron and the electrode different APs shapes can be recorded.

3

SPIKE DETECTION METHODS



3.1 INTRODUCTION

An important building block in the development of an neurostimulator or a Brain Machine Interface (BMI), will be a compact, low power fully implantable AP detector. [21]. It will allow the BMI to transmit only the APs waveforms and their respective arrival times instead of the sparse, raw signal in its entirety. The transmitted data per channel is reduced by this compression and results in an increased number of channels that may be monitored simultaneously [22]. In addition, AP detection can reduce the data rate if unsorted spike counts are transmitted instead of AP waveforms and will also be a necessary first step for any future hardware implementation of an autonomous AP sorter [23]. In order to realize a hardware of a AP detector in a wireless BMI, it must operate in real-time, be fully autonomous and function at realistic Signal to Noise Ratio (SNR).

Content of this chapter is based on existing APs detectors and studies. The focus will be to outline the choices which need to be made in order to design an appropriate AP detector. In Section 3.2, a number of known spike-detection methods are evaluated to determine which are best suited for hardware implementation in an AP detector with limited computational time and power resources. Section 3.3 discuss those spike-detection methods. Finally, conclusions are presented in Section 3.4.

3.2 DETECTION METHODS

To detect APs several methods can be utilized. Choosing the right detection method would be easy when the goal would be only spike detection. However, parameters such as performance, power consumption, speed and chip area must be considered. In this section general descriptions of four different AP detection methods are given.

3.2.1 *Simple Threshold Detectors*

In a typical AP detector, the signal is preprocessed to attenuate noise and to accentuate spikes. Subsequently, a threshold detector is used to determine the spike locations [24]. Similarly, adaptive thresholding can be added to simple threshold detectors. This mechanism monitors the background noise and automatically adapts the threshold according to the noise level [25, 26]. However, this feature increases the complexity and the size of the circuit. As an example of a simple threshold (ST) detector, an absolute value detector, is shown in Fig. 3.1. An absolute value pre-processor, followed by the comparator, is used to detect the APs. Fig. 3.2 shows MatLAB simulation of the ABS value pre-processor. We can see that negative values of the input signal are inverted by the absolute value pre-processor to positive values. Subsequently, APs are detected by comparing the pre-processed signal with

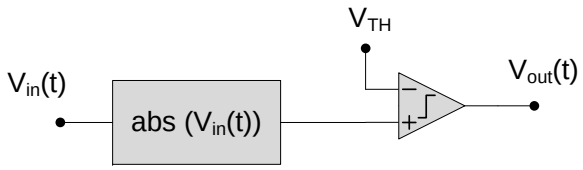


Figure 3.1: Block diagram of absolute value detector.

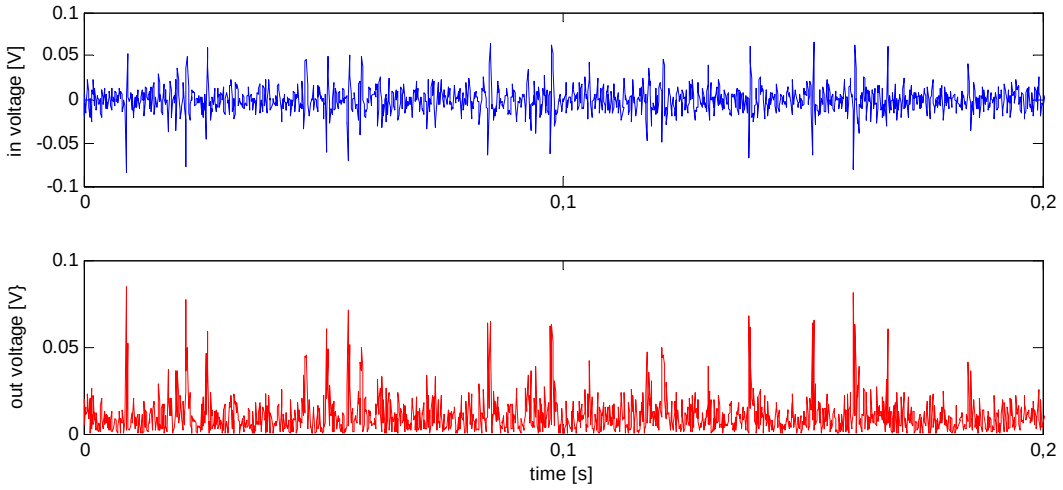


Figure 3.2: ABS value pre-processor MatLAB applied to a low pass filtered neural wave.

the threshold voltage. This is equivalent to applying both positive and negative thresholds simultaneously.

3.2.2 *Energy Based Detectors*

Energy Based (EB) spike detectors have also been used to detect APs [11, 27, 28, 29, 30, 31]. The Nonlinear Energy Operator (NEO), also called the Teager energy operator, first characterized by Kaiser [32], is defined as:

$$\Psi(x(t)) = \left(\frac{\partial x(t)}{\partial t}\right)^2 - x(t)\frac{\partial^2 x(t)}{\partial t^2}, \tag{3.1}$$

where $x(t)$ and $y(t)$ represent the input and the output signal, respectively.

By applying $x(t) = A\sin(\omega t)$ to the NEO, we obtain:

$$\begin{aligned}\Psi(x(t)) &= (A\omega\cos(\omega t))^2 - A\sin(\omega t)\left(A\omega^2\sin(\omega t)\right),\\ &= A^2\omega^2\left(\cos^2(\omega t) + \sin^2(\omega t)\right),\\ &= A^2\omega^2.\end{aligned} \tag{3.2}$$

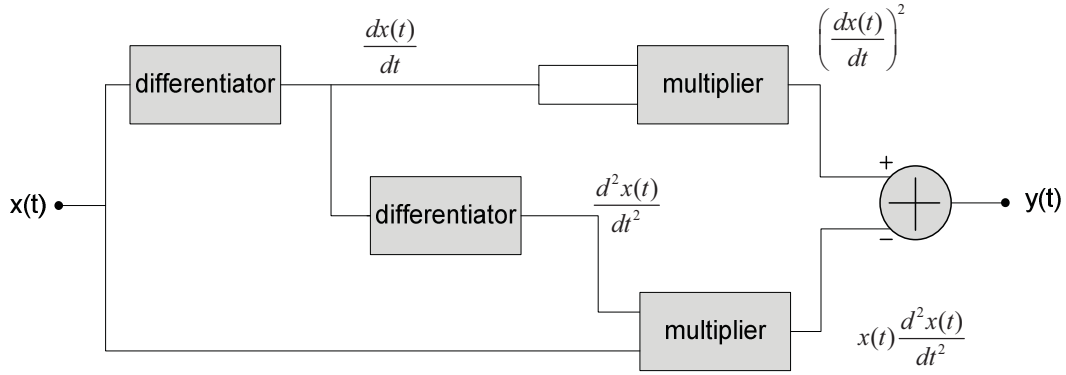


Figure 3.3: The NEO block diagram.

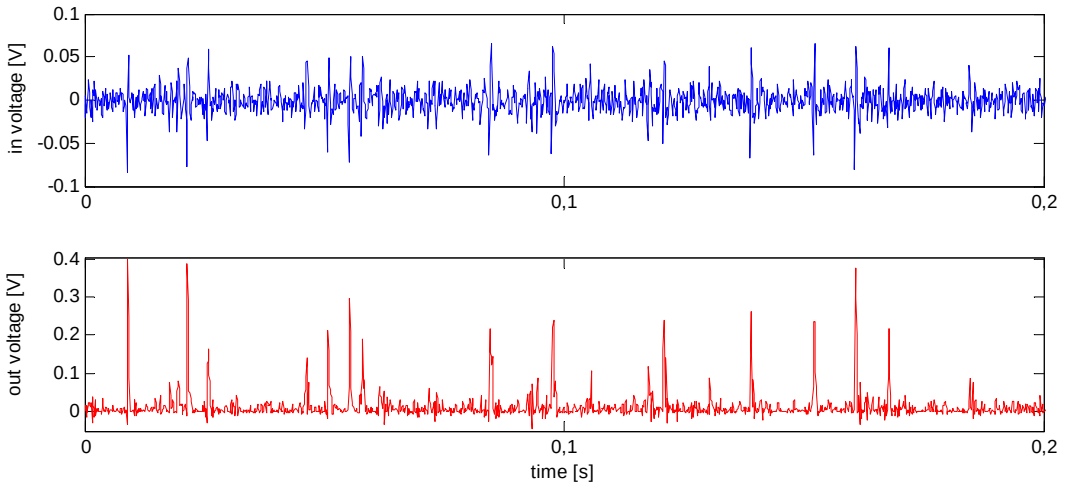


Figure 3.4: MatLAB simulation of the NEO applied to a low pass filtered neural wave. The output of NEO is showing the energy of the input signal.

Hence, the NEO estimates the square of the instantaneous product of amplitude and frequency of the input signal. In this regard, the NEO may be superior to other energy estimators as it explicitly takes frequency into account. The real-time occurrences of APs in noisy environments are easily found since the NEO is able to discriminate between the APs and the noise, their energies considered to be different [27]. In Fig. 3.3 the block diagram of the NEO is shown. It consist of two differentiators and two multipliers. In Fig. 3.4, a MatLAB simulation result demonstrates the NEO performance when applied to the neural wave signal.

3.2.3 *Matched Filter Detectors*

In AP Matched Filter (MF) detectors, template matching is used. By time-aligning several APs shapes, it is possible to select the averaged AP shape as template. Subsequently, this template can be used to detect APs in noisy signals [33]. The neural signal may also be filtered using the Wavelet Transform (WT) [34]. By using

a family of wavelets it is possible to extract details about signal energy in particular time-frequency windows. The feature extraction properties of this wavelet technique make it particularly useful when the goal is to sort spikes as well as to detect them [35, 36].

3.2.4 *Pulse Based Detectors*

Pulse Based (PB) detectors encode information about each AP in a biphasic pulse train in order to reduce the bandwidth required to transmit the spike trains. The APs are represented by pulse density modulated signal while the noise is mostly disregarded [5]. For instance, the frequency of submitted pulses increases as the amplitude of the signals increases. Data reduction is significant in low density neural waveforms. Fig. 3.5 shows block diagram of the PB detector. If $z(t)$, the output of the integrator $y(t)$ minus the leak, reaches the positive threshold of the comparator, θ, the output of that comparator becomes positive. Subsequently, delay element t_d from the feedback loop, will reset the integrator after a short delay. Similarly, if the $z(t)$, reaches the negative threshold, $-\theta$, the output of that comparator becomes negative and also resets the integrator after some delay. The cutoff frequency of the low-pass filter formed with the integrator is set by the leak value and allows efficiently filtering of the noise. By choosing the proper leak value together with the proper threshold value the system will dedicate most of the pulses to represent the neural spikes. The timing of two successive pulses is fixed with the following equation

$$\theta_i = \frac{1}{C} \int_{t_{i+td}}^{t_{i+1}} x(\triangle) e^{\frac{\triangle - t_{i+1}}{RC}} d\triangle, \tag{3.3}$$

where $\theta_i \in \{-\theta, \theta\}$, C is the integration capacitor and the R is related to the leak value.

After the pulse trains have been transmitted, a classifier can sort the spikes outside the body where power issues are not so critical. The encoded pulses for each spike serve as a spike signature and a pulse-based spike sorting algorithm is used to classify the spike.

3.3 DISCUSSION

The purpose of the evaluation of the algorithms discussed in this Chapter is to determine which is best suited for detecting neural action potentials in a wireless BMI.

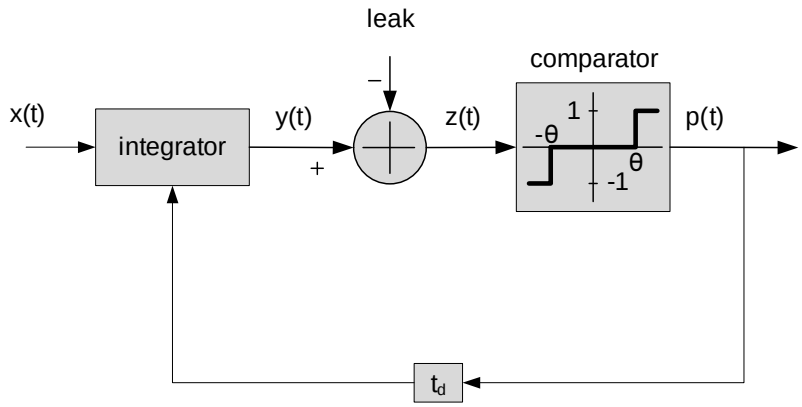


Figure 3.5: Block diagram of pulse based detector [5].

Table 3.1: AP detectors comparison

Detectors	power consumption	chip area
Matched filter	high	high
Pulse based	high	high
Energy based	moderate	moderate
Simple threshold	low	low

Even though ST and EB detectors tend to be sensitive to noise, but they still remain attractive for real-time implementations because of their minute computational time [27, 37]. The efficacy of simple and adaptive threshold detectors is reduced by overlapping spikes. However, when considering power consumption, EB detectors are outperformed by ST detectors.

MF detectors are particularly effective when the spike waveform to be detected is already known. Since this is often not the case, the user must manually select a template [33]. In systems where the goal is only spike detection, then the high power consumption may be prohibitive for real-time multichannel AP detection [24]. If the system is not limited by its power consumption, an MF with a non-specified template will be the detector of choice [38].

Pulse based detectors appears to be a good candidate to solve the data reduction problem and still allowing for spike sorting [5]. However, power consumption, computation time and chip area are much higher. Furthermore, spike sorting needs to be performed outside the body [39], which may preclude pulse based detectors in closed loop neural stimulator's.

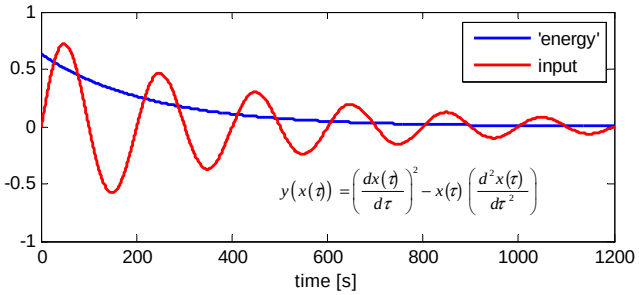
An comparison of the power consumption and chip area of different AP detectors is shown in Table 3.1.

3.4 CONCLUSION

In this Chapter, it is shown that not all AP methods are suitable for low-power, real-time, fully implantable AP detector. PB and MF detectors have high power-consumption and complex circuits. In addition, their computational time may prohibit them in real-time AP detectors. On the contrary, ST detectors operate in real-time, have compact circuits and consume very little power. It has been demonstrated that some ST detectors are effective pre-processors just as any EB or MF pre-processors [23, 38]. Therefore, it is logical to choose ST detectors as fully implantable AP. EB detectors are considered to have moderate power consumption and circuit size. Current implementations of the NEO detectors are bulky and tends to exceed power consumption in multichannel AP detectors. Improving the NEO designs can make EB detectors more attractive as AP detectors. The next Chapter will concentrate on improving, minimizing circuit area and power consumption, of the NEO detectors, followed by Chapter 5 where the design of an compact, low-power, real-time ST AP detector is demonstrated.

4

DYNAMIC TRANSLINEAR NONLINEAR ENERGY OPERATOR



The content of this chapter is adapted from:
Senad Hiseni, Chutham Sawigun, and Wouter A. Serdijn, "Dynamic translinear nonlinear energy operator," *Circuit Theory and Design, 2009. ECCTD 2009. European Conference on*, pp. 153-156, Antalya, Turkey, August 2009.

4.1 INTRODUCTION

The NEO provides real-time energy of the sign als using internal nonlinear dynamical mechanisms described by (3.1). Representing the NEO algorithm in terms of a block diagram can lead to a direct circuit realization. As shown in Fig. 3.3, the NEO block diagram comprises two differentiators, two multipliers, and a subtractor block. These blocks can be implemented in a low power fashion using analog circuits. Recentlty, based on the block diagram in Fig. 3.3, fully integrated NEO detectors have been reported in [11, 28] where a $G_m - C$ structure and Gilbert multipliers are employed to realize the differentiator and multiplier blocks. Obviously, using this topology the NEO detector performance is limited by the circuit blocks employed, i.e., a limited linear range of the G_m circuits affects the dynamic range of the differentiator and the Gilbert multiplier. To enhance the dynamic range the G_m cells need to be linearized and this unfortunately results in additional power consumption and chip area.

In this chapter, instead of following the block diagram, we move one step backward to design the NEO from equation (3.1) directly using the Dynamic Translinear (DTL) circuit principle. As it is widely known that DTL can be used to realize both linear and nonlinear differential equations from the exponential behavior of Bipolar Junction Transistor (BJT) and subthreshold Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) devices [40], using this approach, the detector performance is no longer related to the linear behavior of the G_m cell. Therefore, a NEO detector having lower power consumption and smaller chip area are expectable from our design. The static and dynamic translinear principles are reviewed in Section 4.2. In Section 4.3, the design of the NEO using the proposed synthesis method employing bipolar transistors is given. Section 4.4 discusses the simulation results of the corresponding design. Finally, the conclusions are presented in Section 4.5.

4.2 TRANSLINEAR PRINCIPLE

Translinear (TL) circuits are based on the exponential behavior of the bipolar transistor or the Metal-Oxide-Semiconductor (MOS) transistor operating in the subthreshold region. TL circuits are supposed to be a promising alternative in the area of low-voltage design, as the voltages in the translinear circuits are logarithmically related to the currents. Conventional, i.e., static, translinear circuits can be used to realize a wide variety of linear and nonlinear functions. By allowing capacitors in the translinear loops, DTL circuits can be used to implement linear and nonlinear differential equations [40]. As an extension of conventional translinear circuits, DTL circuits inherit the advantages of conventional translinear circuits. The main advantage is a high functional density, which makes translinear circuits suitable for low voltage, low-power applications.

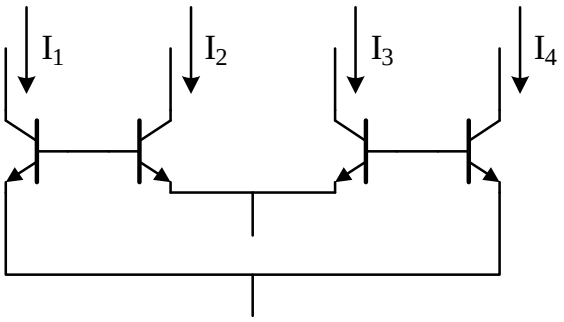


Figure 4.1: A four-transistor translinear loop.

TL circuits can be divided into Static Translinear (STL) and DTL circuits. Using STL circuits we can implement linear and nonlinear static transfer functions. Frequency-dependent (transfer) functions, i.e., Differential Equations (DEs) can be realized by DTL circuits. In this section we will review the STL and DTL principles by means of two examples.

4.2.1 *Static Translinear Principle*

The TL principle is based on the exponential behavior between voltage and current of the bipolar transistor and the MOS transistor in weak inversion region. In the following discussion, bipolar transistors are assumed. The collector current of bipolar transistors is given by

$$I_c = I_s e^{(V_{BE}/U_T)}, \tag{4.1}$$

where I_s is the zero-bias current, V_{BE} is the base-emitter voltage, $U_T = kT/q$ is the thermal voltage.

The TL principle applies to loops of semiconductor junctions, characterized by an even number of junctions [41, 42]. The number of devices with a clockwise orientation equals the number of counter-clockwise oriented devices. An example of a four-transistor TL loop is shown in Fig. 4.1. It is assumed that the transistors are biased at collector currents I_1 through I_4. When all devices are equivalent and operate at the same temperature, the TL loop is described by a simple static equation

$$I_1 I_3 = I_2 I_4. \tag{4.2}$$

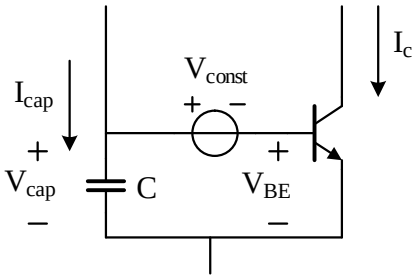


Figure 4.2: Principle of dynamic translinear circuits.

4.2.2 *Dynamic Translinear Principle*

By admitting capacitors in the TL loops, frequency-dependent transfer functions can be realized. The DTL principle can be explained with reference to the sub-circuit shown in Fig. 4.2. This circuit is described in terms of the collector current I_c and the capacitance current I_{cap} flowing through capacitance C. Note that the dc voltage source V_{const} does not affect I_{cap}. An expression for I_{cap} is easily be derived by taking the time derivative of (4.1)

$$I_{cap} = CU_t \frac{\dot{I}_c}{I_c}, \tag{4.3}$$

where the dot represents differentiation with respect to time. Equation (4.3) shows that I_{cap} is a function of I_c and its time derivative $\dot{I}_c$. By slightly rewriting equation (4.3)

$$CU_t \dot{I}_c = I_{cap} I_c, \tag{4.4}$$

we can directly state the DTL principle: *A time derivative of a current can be mapped onto a product of currents* [40]. From this point on, the product of currents on the right-hand side of (4.4) can easily be realized by the conventional STL principle. The DTL principle can be used to implement a wide variety of DEs, describing signal processing functions.

4.3 DYNAMIC TRANSLINEAR NEO OPERATOR

This section demonstrates the design of the NEO using the DTL structured synthesis method. Synthesis of a dynamic circuit, starts with a DE or with a set of DEs describing its function. The NEO operator can be described in the time domain by

$$y(\tau) = \left(\frac{\partial x(\tau)}{\partial \tau}\right)^2 - x(\tau)\frac{\partial^2 x(\tau)}{\partial \tau^2}, \tag{4.5}$$

where x and y represent the input and the output signal, respectively.

At first glance from (4.5), it seems like, in order to realize this function, differentiator, squarer and multiplier circuits are needed, which leads to a complex topology. Using the DTL structured synthesis method, (4.5) can be implemented by a very simple and compact topology of translinear loops circuit which will be shown shortly.

4.3.1 *Transformations*

An important difference between the mathematical and electronic domain is that the latter one is bounded by quantities having dimensions. To find an implementation of the mathematical equation we need to transform all time-varying signals in the DEs, i.e., the input signals, the output signals and the tunable parameters into currents [40]. Thus, the first step of dynamic structured synthesis is to add dimensions to the dimensionless mathematical equations. For the above expression, x and y can be transformed into the currents $I_{in} = xI_o$ and $I_{out} = yI_o$, I_o being the DC bias current that determines the absolute current swings. The dimensionless time τ, can be transformed into the time t with its usual dimension [s], using the equivalence relation given by

$$\left(\frac{\partial}{\partial\tau}\right)^k = \left(\frac{CU_t}{I_o}\right)^k \left(\frac{\partial}{\partial t}\right)^k. \tag{4.6}$$

Subsequently, dimensionless differential equation (4.5) is transformed into a current-mode differential equation

$$I_{out} I_o^3 = (C_1 U_t \dot{I}_{in})^2 - I_{in} (C_2 U_t)^2 \ddot{I}_{in}. \tag{4.7}$$

4.3.2 *Definition of the Capacitance Currents*

By introducing the capacitance currents we are able to implement DEs by translating time derivatives into products of currents. Note that (4.5) is a second-order differential equation, which means that we need to take the time derivative of the first capacitance current that already contains the time derivative in order to map this equation on silicon. Thus, we need two capacitance currents. Defining I_{cap1} and I_{cap2} as

$$I_{cap1} = C_1 U_t \frac{\dot{I}_{in}}{I_{in} + I_o} \tag{4.8}$$

and

$$\begin{aligned} I_{cap2} &= C_2 U_t \frac{\dot{I}_{cap1}}{I_{cap1} + I_o} \\ &= C_1 C_2 U_t^2 \frac{\ddot{I}_{in}(I_{in} + I_o) - \dot{I}_{in}^2}{(I_{in} + I_o)^2 (I_{cap1} + I_o)}. \end{aligned} \tag{4.9}$$

for $C_1 = C_2$, current-mode differential equation (4.7) yields a current-mode polynomial without derivatives:

$$I_{out} I_o^3 = I_{cap1}^2 (I_{in} + I_o)^2 - I_{in}(I_{in} + I_o)(I_{cap1} + I_o) I_{cap2} - I_{in}(I_{in} + I_o) I_{cap1}^2. \tag{4.10}$$

As we can see, the above DE is now described by a current-mode polynomial where the time derivatives and capacitances are hidden in the capacitance currents. Observe that input current I_{in} and both capacitance currents, I_{cap1} and I_{cap2} can be positive and negative. As a consequence, a bias current needs to be added such that the collector currents always remain positive. By doing so, (4.10) becomes (4.11)

$$\begin{aligned} I_{out} I_o^3 &= I_o (I_o + I_{in})(I_o + I_{cap1})^2 \\ &- I_o (I_o + I_{in})(I_o + I_{cap1})(I_o - I_{cap2}) \\ &- I_o (I_o + I_{in})^2 (I_o + I_{cap1}) + I_o^3 (I_o + I_{in}) \\ &+ (I_o + I_{in})^2 (I_o + I_{cap1})(I_o - I_{cap2}) \\ &- I_o^2 (I_o + I_{in})(I_o + I_{cap1}). \end{aligned} \tag{4.11}$$

Both sides of the above DE are now described by current-mode polynomials and from this point on, the synthesis procedure for static TL circuits can be used [42].

4.3.3 *Translinear Decomposition*

The next synthesis step is translinear decomposition. That is, the current-mode polynomial has to be transformed into one or more TL loop equations that are characterized by the general equation

$$\prod_{CW} J_{C,i} = \prod_{CCW} J_{C,i}, \tag{4.12}$$

$J_{C,i}$ being the transistor collector current densities in ClockWise (CW) or Counter-ClockWise (CCW) direction. As 'non-parametric' decomposition is not always possible, we can utilize 'parametric' decomposition of (4.11). It means that one or more intermediate currents need to be defined, introducing extra TL loops. If possible, extra TL loops should be included into existing TL loops, which will save us extra current branches and lower the total power consumption. Here, two intermediate

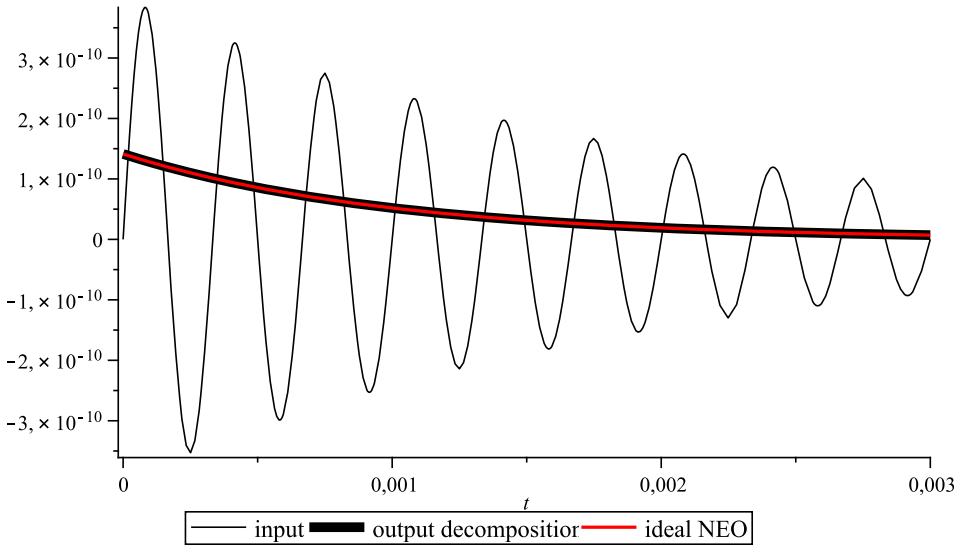


Figure 4.3: Verification of TL decomposition of (4.11).

currents I_A and I_B are defined. As a result, there will be four valid TL equations (4.13), (4.14), (4.15) and (4.16)

$$I_B I_o = (I_{in} + I_o)(I_{cap1} + I_o), \tag{4.13}$$

$$I_A I_o^2 = (I_{in} + I_o)^2 (I_{cap1} + I_o), \tag{4.14}$$

$$[I_{out} + I_A - (I_{in} + I_o) + 2I_B]I_o = [(I_{cap1} + I_o) + (I_o - I_{cap2}) + I_o]I_R, \tag{4.15}$$

$$(2I_B - I_A)(I_o - I_{cap2}) = [(I_{cap1} + I_o) + (I_o - I_{cap2}) + I_o]I_L, \tag{4.16}$$

with

$$I_L + I_R = I_B. \tag{4.17}$$

These functions are readily implemented in TL circuits [41, 42].

4.3.4 *TL Decomposition Verification*

Before the last synthesis step, it is convenient to verify the TL loop decomposition before introducing non-idealities from the circuit implementation. As verification, a short *Maple* code is written where the ideal NEO (4.7) is compared with the NEO

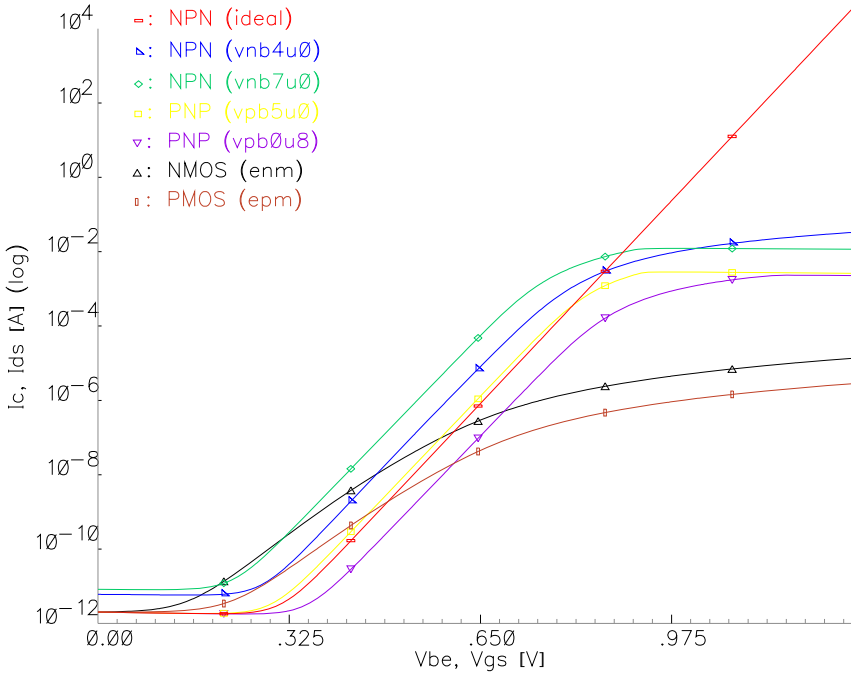


Figure 4.4: Exponential behavior of the available AMIS transistors models.

composed of TL loop equations (4.13), (4.14), (4.15), (4.16) and nodal equation (4.17), derived in previous synthesis step. The expected behavior of the TL decomposition is shown in Fig. 4.3. We can see that the black thick line that indicates the NEO composed of TL loop equations, follows the ideal NEO (4.7), represented by red line. And by doing so, they both represent the energy of the input signal, the black thin line. This step successfully verifies the DTL and STL loop decomposition. From this point on, the next synthesis step will be followed.

4.3.5 *CMOS vs BJT*

In the available Bipolar and Complementary Metal-Oxide-Semiconductor (BiCMOS) AMIS (Alcatel) technology, BJT and MOS transistors are provided.

The exponential behavior of the available transistors, an important parameter when considering TL circuits, is shown in Fig. 4.4. Also, the exponential behavior of an ideal transistor is shown. We can see that exponential behavior of BJT transistors span about ten decades, while the exponential behavior of MOS transistors biased in weak inversion is much less. As a consequence of low purely exponential behavior, it is not unusual to expect some errors from MOS transistors.

To identify the nature of those errors we use the circuit shown in Fig. 4.5. It is a simple four-transistor TL loop. Transistor models M_1 through M_4 are replaced by diode connected NPN and diode-connected N-channel Metal-Oxide-Semiconductor Transistor (NMOST) as shown in Fig. 4.6a and Fig. 4.6b, respectively. By using ideal component, the nullor, implemented by an ideal Voltage Controlled Current

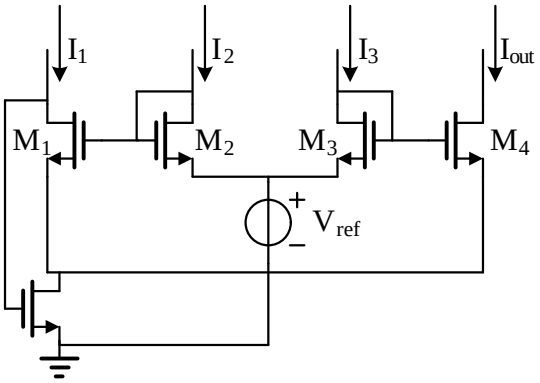


Figure 4.5: A four NMOS transistors in STL loop configuration.

Source (VCCS), we minimize the influence of V_{BC} (early effect) in case of BJT and V_{DS} (channel length modulation) in case of MOS transistor while still using the exponential behavior of both transistor models. This approach ensures that any error produced by the circuit is due to the (non)exponential behavior of the transistors. The currents applied, I_1 through I_3 in Fig. 4.5 have a realistic ratio between their values. For instance, $I_1 = I_{bias}$, $I_2 = 0.4 \cdot I_{bias}$ and $I_3 = 3 \cdot I_{bias}$, a similar ratio of static currents as in the case of (4.15). I_{out} is calculated according to

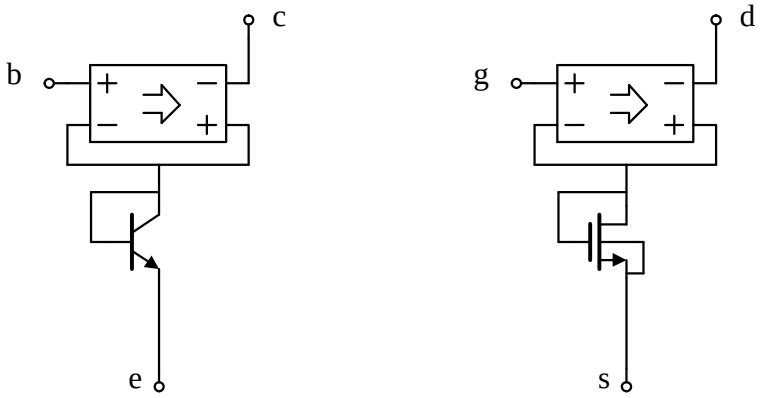
$$I_{out} = \frac{I_1 \cdot I_3}{I_2} \tag{4.18}$$

and compared with the simulated value for I_{out}. Next, the error is calculated according to

$$\text{error} = \frac{I_{out,\ calculated} - I_{out,\ simulated}}{I_{out,\ calculated}} \cdot 100\%. \tag{4.19}$$

The results for different I_{bias} bias currents is shown in Fig. 4.7. We can see that an error produced by using MOS transistors is larger than in case of using BJTs. The influence of this error on the NEO design will be evaluated and explained shortly.

As pointed out previously, the DTL NEO consists of four STL equations (4.13), (4.14), (4.15) and (4.16), and two DTL equations (4.8) and (4.9). This means that even a small error can have a big influence on the total design. However, it is very difficult to predict the error. For example, it is not easy to take a dynamic error into account. Hence, *Maple* is used to find the total NEO error in case of a 3% static error applied to STL loops, described by equations (4.15) and (4.16). Fig. 4.8 shows the result. The dashed green line shows the output of the NEO in case no static error is applied. The blue dashed line shows the output of the NEO in case the 3% static error is applied to one STL loop, described by (4.16) and in case the 3% static error is applied to two STL loops, described by (4.15) and (4.16), the red dashed line represents the output of the NEO. From this figure, Fig. 4.8, it seems that a small



(a) Nullor and diode-connected NPN as an implementation of a V_{BC} insensitive NPN transistor.

(b) Nullor and diode-connected NMOS transistor as an implementation of a V_{DS} insensitive NMOS transistor.

Figure 4.6: Transistor models used to point out an exponential error

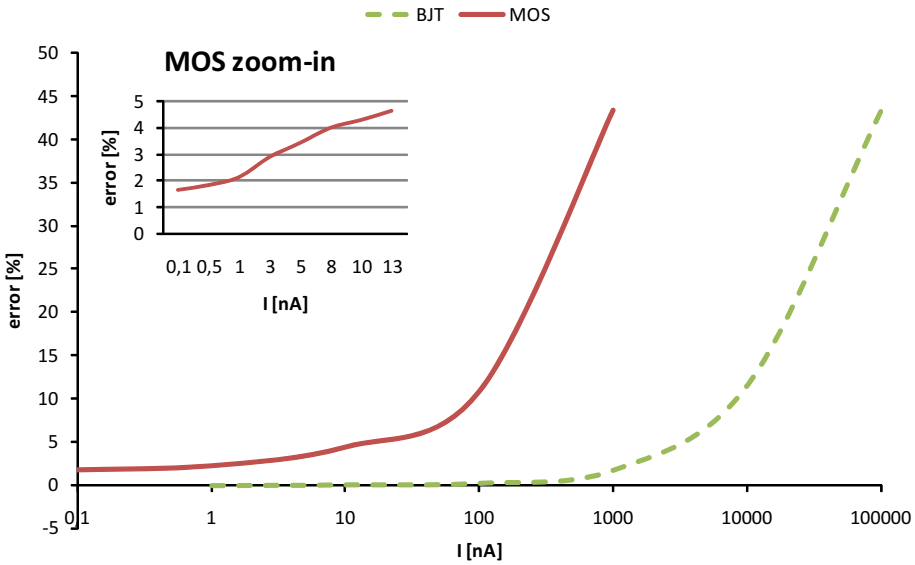


Figure 4.7: The four NMOS transistors STL loop error vs I_{bias} bias current.

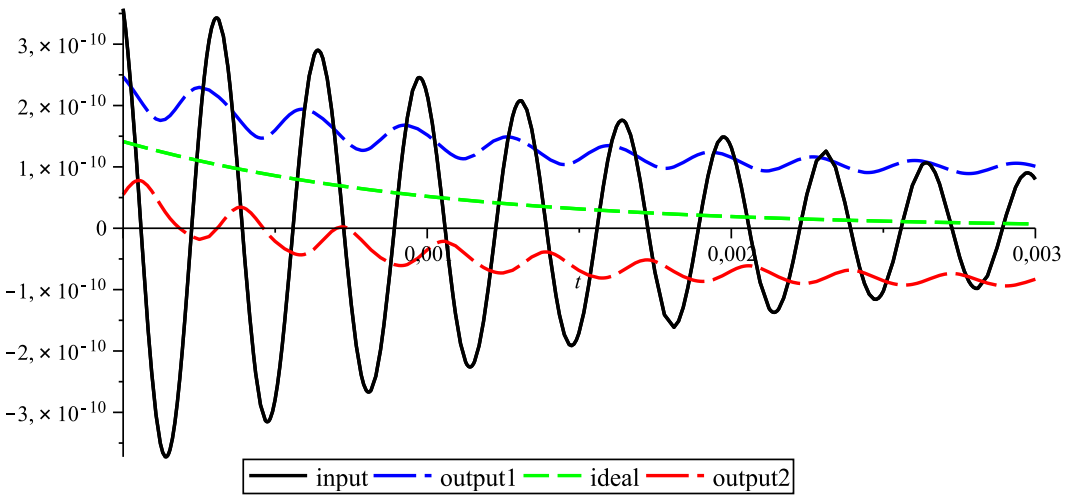


Figure 4.8: Output of the NEO after 3% static error by four STL loop transistors was introduced.

static error, applied to one small part of the NEO circuit, already disables the NEO to calculate the energy of the input signal. This suggests that in the real case, where static and dynamic errors exist in the NEO circuit, the result can only become worse. Consequently, it is decided to design the NEO using BJT transistors, which produce a very small, negligible error.

4.3.6 *Circuit Implementation*

The last synthesis step is the circuit implementation. The TL decomposition that was found during the synthesis step has to be mapped onto a TL circuit topology. A possible realization of the first capacitance current and intermediate currents is shown in Fig. 4.9. The TL loop formed by $Q_1 - Q_2 - C_1$, implements (8). Note that V_{BEQ_2} can be considered a constant voltage source. Transistors $Q_1 - Q_2 - Q_3 - Q_4$ and $Q_1 - Q_2 - Q_3 - Q_5 - Q_6 - Q_7$ implement (4.13) and (4.14), respectively. M_2 through M_4 provide feedback and minimize the base currents, which results in more accurate intermediate currents. M_1 and M_5 provide negative feedback to ensure that the correct collector current will flow through Q_1 and set the V_{CQ_1} to desired value. V_{ref_1} provides some headroom for M_5.

In Fig. 4.10, the circuit realizing the second capacitance current is shown. Loop $Q_8 - Q_9 - C_2$ implements (4.9). Voltage V_{be} across Q_9 is constant. M_6 and M_8 have the same function for Q_8 as M_1 and M_5 for Q_1. Function of M_7 is to minimize base currents. Headroom of M_8 is ensured by properly choosing V_{ref_2}.

Fig. 4.11 shows the circuit that implements (4.15) through (4.17). Transistors $Q_{11} - Q_{12} - Q_{13} - Q_{14}$ and $Q_{14} - Q_{15} - Q_{16} - Q_{17}$ implement (4.15) and (4.16), respectively. The function of MOS transistors M_9 through M_{15} is as discussed before.

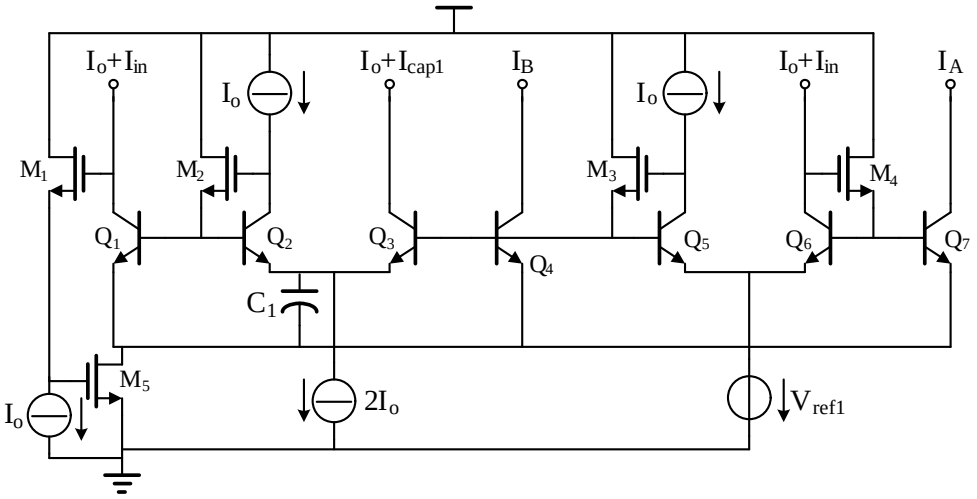


Figure 4.9: Implementation of the capacitance and the intermediate currents according to (4.8), (4.13) and (4.14).

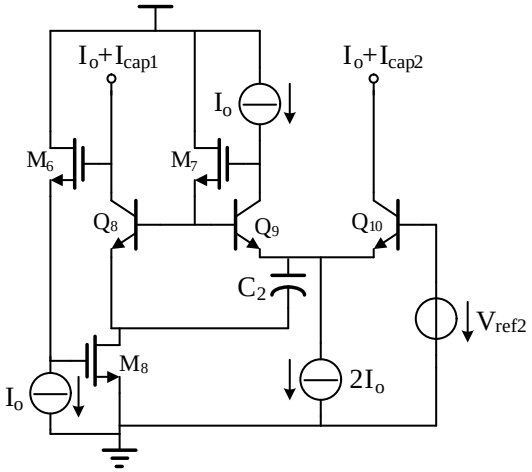


Figure 4.10: Implementation of the capacitance current according to (4.9).

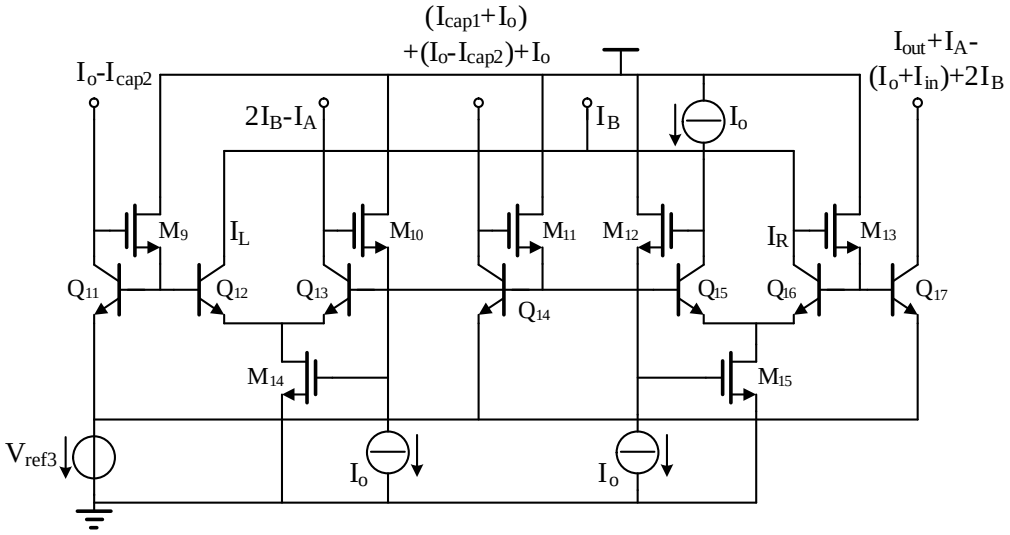


Figure 4.11: Implementation of the TL loops equations (4.15) through (4.17)

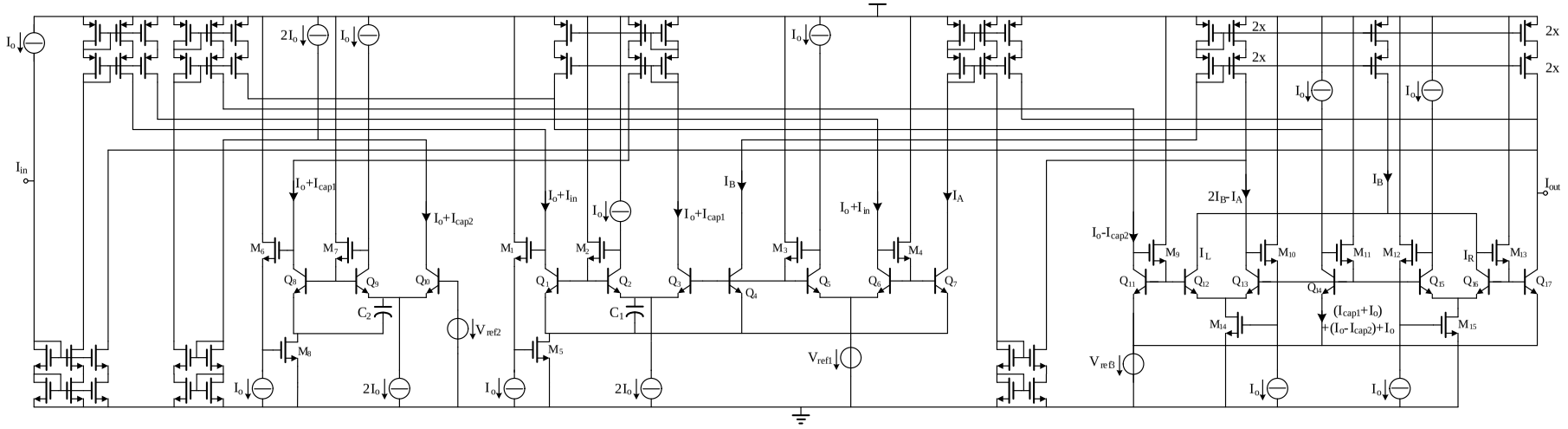


Figure 4.12: BiCMOS implementation of the complete NEO.

Table 4.1: The NEO MOS transistors sizes.

Transistor(s)	1-13	14	15
W / L [μm]	2 / 0.7	4 / 0.7	1 / 1

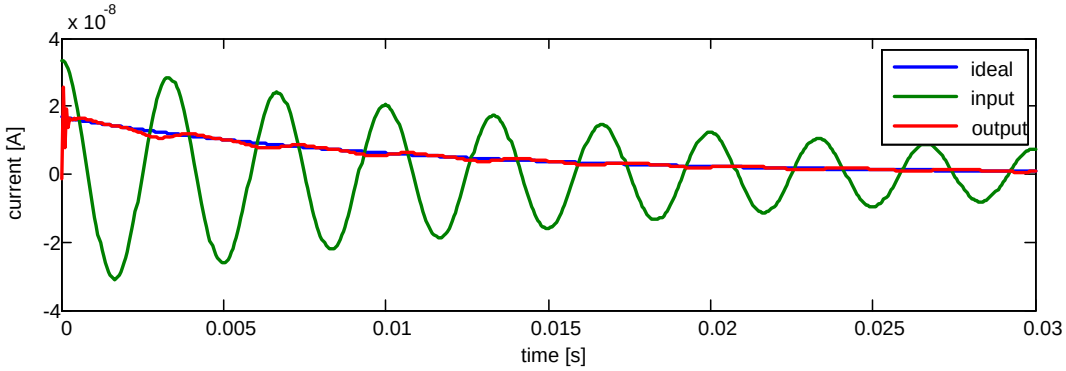


Figure 4.13: NEO applied to a damped sinusoidal signal. The output of NEO is showing the energy of the input sinusoidal.

V_{ref_3} lifts the drain voltage of M_{14} and M_{15} for proper biasing. The complete schematic of the BiCMOS implementation of the NEO is shown in Fig. 4.12.

4.4 SIMULATIONS RESULTS

The final circuit was verified in Cadence using RF spectre and AMIS 0.35 μm technology (I3T80). MOS transistor width (*W*) and length (L) were set according to Table 4.1. The NPN transistor emitter area is $16\,\mu m^2$. Supply voltage $V_{DD} = 2$ V, reference voltages $V_{ref_1} = 0.2\,V$, $V_{ref_2} = 0.72\,V$, $V_{ref_3} = 0.1\,V$ and bias current $I_o = 100\,nA$. The quiescent power consumption equals 7.2 μW.

Fig. 4.13 shows the transient response of the NEO in case a damped sinusoidal signal is applied to the input. The blue line represents the output current of the

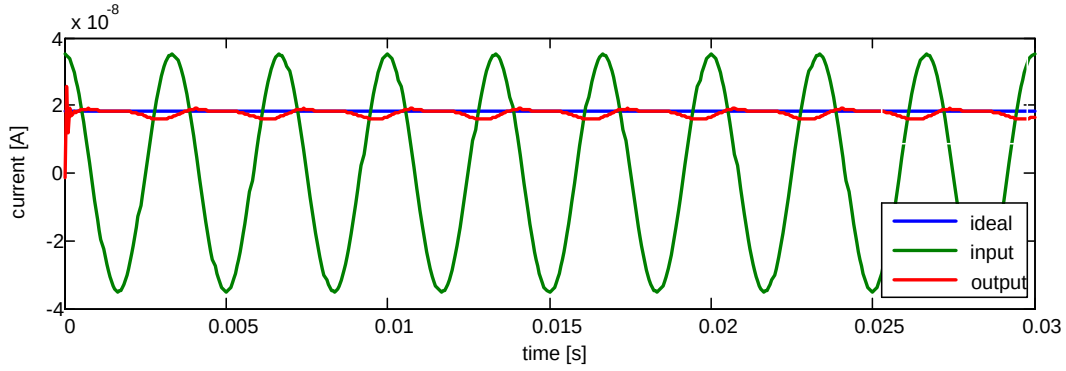


Figure 4.14: NEO applied to a constant sinusoidal signal. The output of the NEO has a constant magnitude when the input signal amplitude and frequency are constant.

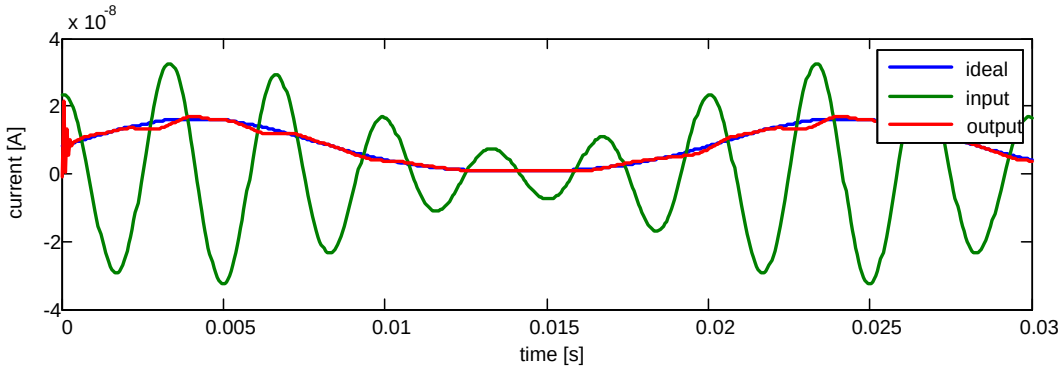


Figure 4.15: NEO applied to the sum of two sinusoids with different frequencies and the same amplitude. The output of the algorithm oscillates at a different frequency and amplitude is about the sum of the energies of the two sinusoids.

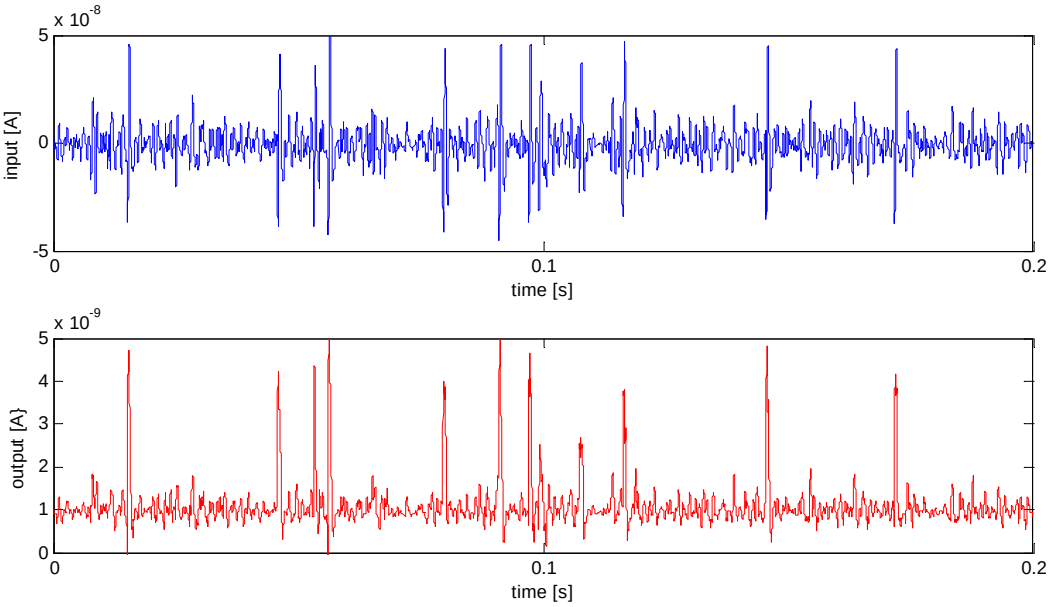


Figure 4.16: NEO applied to 200 ms of the neural wave signal. The output of the algorithm is showing different energies for the APs and the background noise.

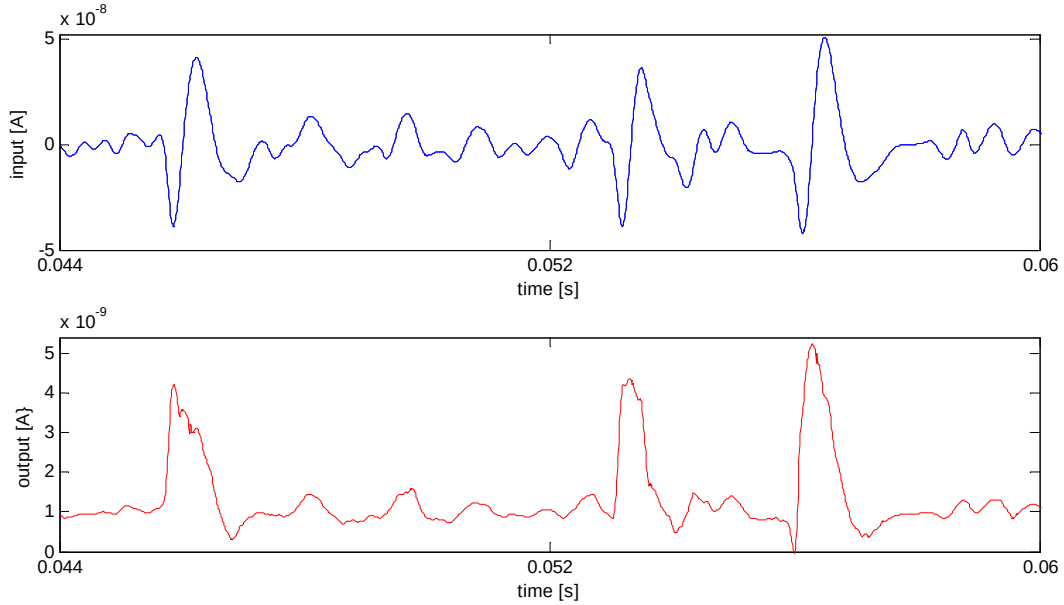


Figure 4.17: Transient NEO simulation zoom in.

NEO for the ideal case where (4.7) is applied directly to the input signal and the red line shows the output of the NEO circuit. The green line is the input. It can be seen that for larger input signal amplitudes, the output of the NEO is showing higher "energy". Lower energy occurs at a lower amplitude.

In the case of a constant amplitude and constant frequency sinusoidal input signal, the result is shown in Fig. 4.14. The blue line represents the output current of the NEO for the ideal case and the red line shows the output of the NEO circuit. The green line is the input. It can be seen that in this case the NEO circuit is able to detect the energy of the input signal with a small error resulting from nonideality effects in the form of a small ripple appearing at the output.

The output of the NEO, in case of an input signal consisting of two frequency components is shown in Fig. 4.15. The blue line represents the output current of the NEO for the ideal case and the red line shows the output of the NEO circuit. The green line is the input. The output signal also follows the real energy of the input signal with a small error.

The output of the NEO, in case of neural wave input signal used is shown in Fig. 4.16. The red line represents the output current of the NEO and the blue line shows the input neural wave of the NEO circuit. Although the output current has a ten time smaller amplitude, it is easy to see that the difference between spikes and the background energies has become bigger and therefore it is easier to isolate APs.

A zoom into the output of the NEO, in case neural wave input signal is used, is shown in Fig. 4.17. Here, the red line also represents the output current of the NEO and the blue line shows the input neural wave of the NEO circuit. For example, setting a threshold at 3 nA will detect APs at the times t = [0.046, 0.054, 0.057] s.

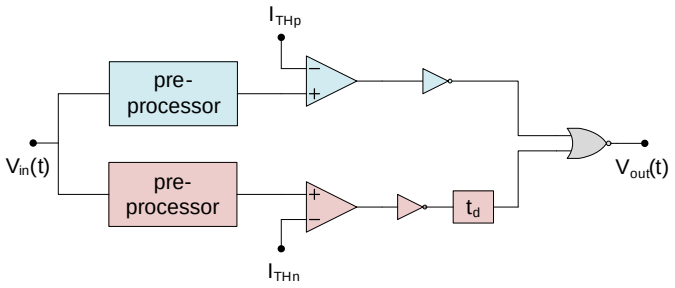
4.5 CONCLUSIONS

In this chapter, the application of the dynamic translinear principle to realize a nonlinear second order differential equation to be used in real-time energy detection has been shown. The BiCMOS version of the resulting circuit comprises two identical capacitors and a handful of transistors. Simulations shows that the proposed circuit is able to successfully detect the instantaneous energies of different kinds of input signals. Thanks to the DTL principle and its high functional density a compact circuit architecture is realized. However, due to the (non)exponential behavior of the MOS transistors, BJTs have been used what results in a less compact circuit. Furthermore, even though the static current consumption of DTL NEO is only 36 current branches times I_o per branche, the total NEO current consumption, with current technology, exceed the limitations of multichannel AP detectors due to high bias current $I_o$of the BJT transistors.

Taking into account that AP multichannel detectors need to be compact and consume very little power, a design of a very compact, nano-power AP CMOS detector is described in the next chapter.

5

A COMPACT, NANO-POWER CMOS ACTION POTENTIAL DETECTOR



The content of this chapter is adapted from:
Senad Hiseni, Chutham Sawigun, Wannaya Ngamkham, and Wouter A. Serdijn, "A Compact, Nano-Power CMOS Action Potential Detector," *IEEE Biomedical Circuits and Systems Conference, 2009. BioCAS 2009.*, pp. 97-100, Beijing, China, November 2009.

5.1 INTRODUCTION

Advantages of simple threshold detectors have been pointed out in Chapter 3. Simple threshold detectors provide compact, low-power, real-time detections. This makes them very attractive in high-count channel AP detectors. However, if only AP detection is the goal, MF detectors are preferred [38]. Clearly, a combination of the advantages of both type detectors will be the right choice.

As a consequence, the strategy presented in this Chapter combines the simplicity of a simple threshold detector with the performance of semi-MF detectors. In this algorithm, three predefined AP features are compared with the measured signal. The AP is detected only if a positive peak is detected in a predefined time after a negative peak was detected. This "dual threshold" AP detection algorithm was originally proposed in [43], including additional filtering.

In this chapter, we present an ultra low-power circuit for dual threshold AP detection. Its principle and system level design are reviewed in Section 5.2. In Section 5.3, the design of the AP detector circuit employing CMOS transistors operating in the subthreshold region is given. The bias circuit is described in Section 5.4. The Layout of the detector is treated in Section 5.5. Section 5.6 discusses the simulation results of the corresponding design. Finally, the conclusions are presented in Section 5.7.

5.2 PROPOSED DUAL THRESHOLD AP DETECTOR

The Dual Threshold Algorithm (DTA) attempts to detect APs in noisy signals by subsequently detecting the positive and the negative peaks of each AP. Occasional noise peaks will not trigger the AP detector and incidental detection of false positives and false negatives will be minimized.

Fig. 5.1 shows the block diagram of the detector. It comprises 8 building blocks: two simple pre-processors, two comparators, two inverters, a delay t_d and a NOR logical gate. The two nonlinear pre-processors extract the input signal, enhancing the difference between the peaks and the noise level. Comparators are used with threshold levels I_{THp} and I_{THn} that can be adjusted separately. A delay is applied to hold the detected negative peak signal for a particular time. Its time constant depends on the AP duration. Finally, the NOR gate performs a logical NOR on the inverted positive peak detected and the delayed output signal. It produces a logical "true" when an AP is detected. A logical "false" is produced in the absence of APs.

Fig. 5.2 illustrates the waveforms at the various stages in the detector. In Fig. 5.2a we see the input signal. Fig. 5.2b illustrates the detection of the negative peak. The inverted and delayed version of the detected negative peak signal is shown in Fig. 5.2c. Inverted, detection of the positive peak is shown in Fig. 5.2d. Detection of the AP is depicted in Fig. 5.2e.

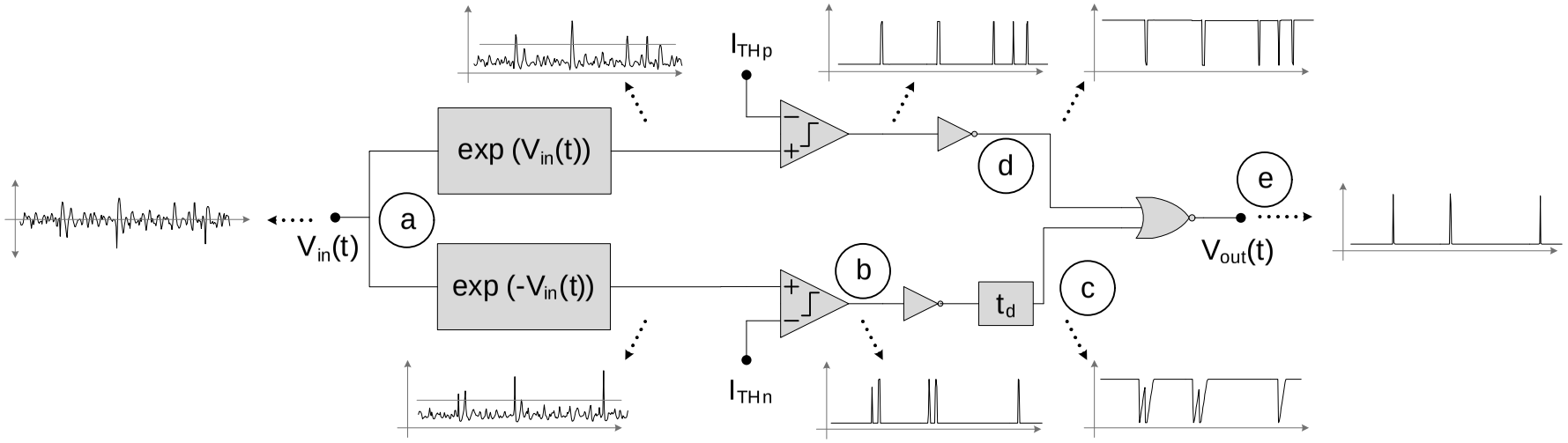


Figure 5.1: Blockdiagram of the proposed dual threshold AP detector.

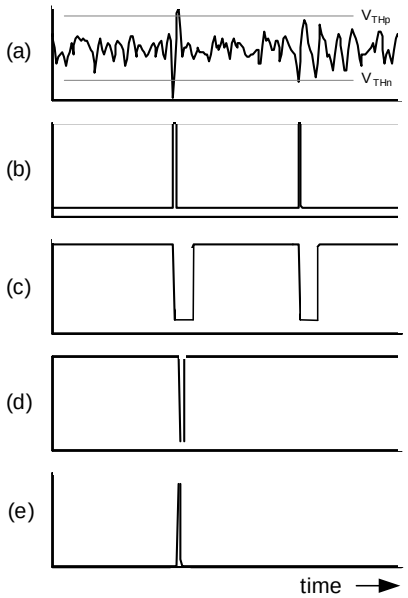


Figure 5.2: Waveforms at the various nodes in the AP detector. (a) Input neural waveform. (b) Negative peaks, lower than V_{THn} are detected. (c) Delayed detected negative peak. (d) Detection of a positive peak if the input signal is higher than V_{THp}. (e) In case (c) and (d) occur at the same time, an AP will be detected.

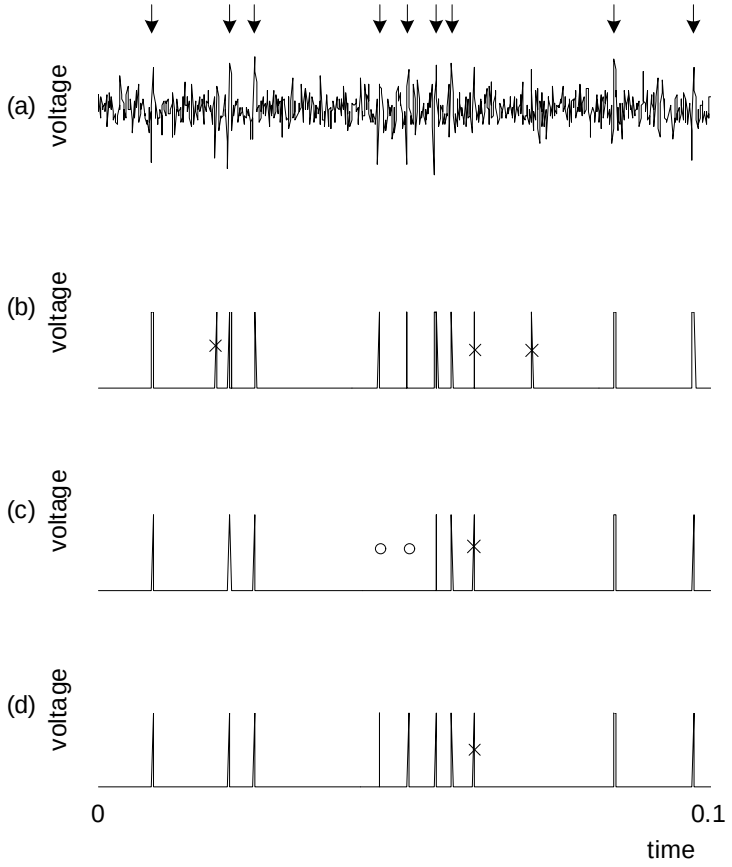


Figure 5.3: Transient response of three different algorithms. (a) Input neural waveform. (b) NEO response. (c) ATA response. (d) DTA response. O = false negative, X = false positive.

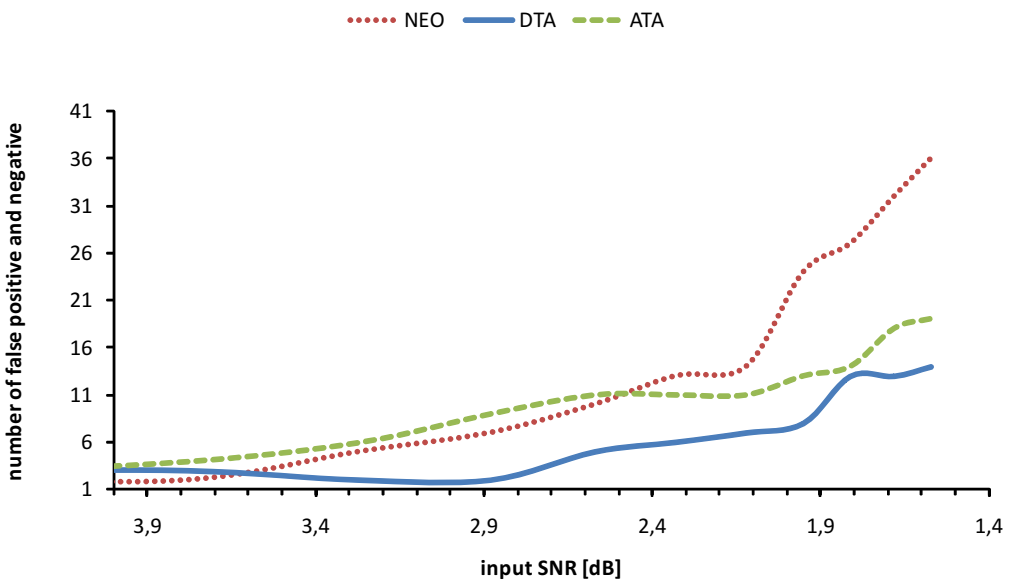
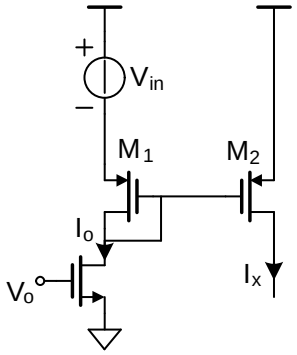


Figure 5.4: Performance comparison of three different algorithms.

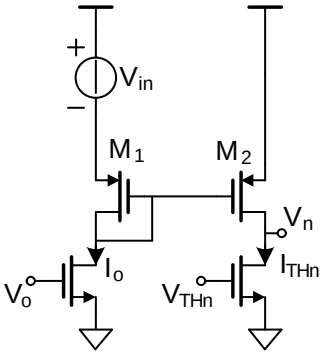
To verify the performance of the DTA, we compare it to the NEO and Adaptive Threshold Algorithm (ATA) as described in [25]. As test signal we use a synthetic signal made from a real waveform sampled at 30 kHz. AP shapes are extracted from the real waveform and randomly distributed according to the Poisson law with variable firing rates. Subsequently, white noise, band-limited at 7 kHz, is added to emulate various SNRs.

Fig. 5.3 shows the transient responses of the three algorithms. The signal of Fig. 5.3a has SNR of 2.9 dB and is applied to each algorithm. Fig. 5.3b represents the output of the NEO. The output of the ATA can be seen in Fig. 5.3c. Finally, in Fig. 5.3d, the output of the DTA, described in this chapter, is depicted. We can see that false detections of the DTA are less likely to occur than in the case of the NEO and the ATA.

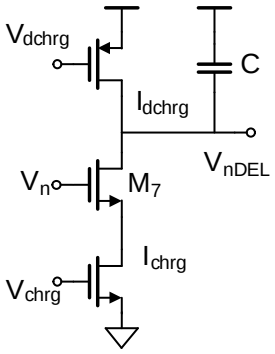
Fig. 5.4 indicates the performance of the different detectors as the SNR ratio is decreasing. At high SNR ratios, the NEO shows good performance. As the SNR decreases, the performance degradation of the NEO becomes more severe than that of the other two detectors. ATA and DTA have the same performance in case of high SNR. As the SNR decreases, we can see that DTA outperforms ATA.



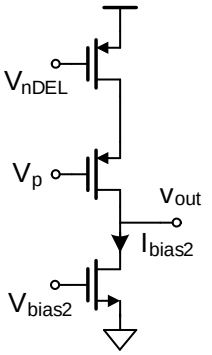
(a) Simple pre-processor performing mathematical exponential operation.



(b) Implementation of current comparator.



(c) Delay circuit.



(d) NOR-gate analog implementation.

Figure 5.5: Dual threshold detector building blocks

5.3 DUAL THRESHOLD DETECTOR BUILDING BLOCKS

5.3.1 *Pre-processors*

Fig. 5.5a shows the circuit implementation of the pre-processor. Using the exponential relationship of P-channel Metal-Oxide-Semiconductor Transistors (PMOSTs) operating in weak inversion [44], for $V_{DS} \geqslant 4U_T$ (a condition to keep the devices in weak inversion saturation) and $V_{SB} = 0$ (source and body terminals are connected), it follows

$$I_D = I_{Do} \exp\left(\frac{V_{SG}}{nU_T}\right), \tag{5.1}$$

where

$$I_{Do} = I_S\left(\frac{W}{L}\right) \tag{5.2}$$

and I_S is the zero bias current for a unit transistor, n is the sub-threshold slope factor and U_T is the thermal voltage while W, L, V_{SD}, V_{SB}, and V_{SG} have their usual meaning. From Fig. 5.5a we can find that

$$V_{SG2} = V_{SG1} + V_{in}. \tag{5.3}$$

Substituting (5.3) into (5.1) we get

$$I_x = I_o \exp\left(\frac{V_{in}}{nU_T}\right), \tag{5.4}$$

which clearly states the exponential relation between input voltage and output current scaled with bias current I_o, which is set by the voltage V_o.

5.3.2 *Current comparators*

Implementation of the current comparator is performed by adding a current source I_{THn}, set by V_{THn}, to the exponential pre-processor output node, as shown in Fig. 5.5b. In case $I_{THn} > I_x$, V_n will become 0V. Otherwise it will be V_{DD}, as illustrated in Fig. 5.2d.

5.3.3 *Delay circuit*

Fig. 5.5c shows the implementation of the delay circuit. Transistor M_7 acts as a switch. In case $V_n = 0$V, M_7 will be open and we have

$$I_{dchrg} = C\frac{dV_{nDEL}}{dt}. \tag{5.5}$$

Slightly rewriting (5.5), we can find the discharging slope

$$\frac{dV_{nLPF}}{dt} = \frac{I_{dchrg}}{C}. \tag{5.6}$$

In case $V_n = V_{DD}$, in charge mode, M_7 will be closed and we have a different situation. The charging slope is then defined as

$$\frac{dV_{nLPF}}{dt} = \frac{I_{chrg} - I_{dchrg}}{C}. \tag{5.7}$$

The threshold voltage of M_7 and the discharging slope determine the delay time t_d, where $I_{chrg} >> I_{dchrg}$. Voltages V_{chrg} and V_{dchrg} are setting I_{chrg} and I_{dchrg}, respectively.

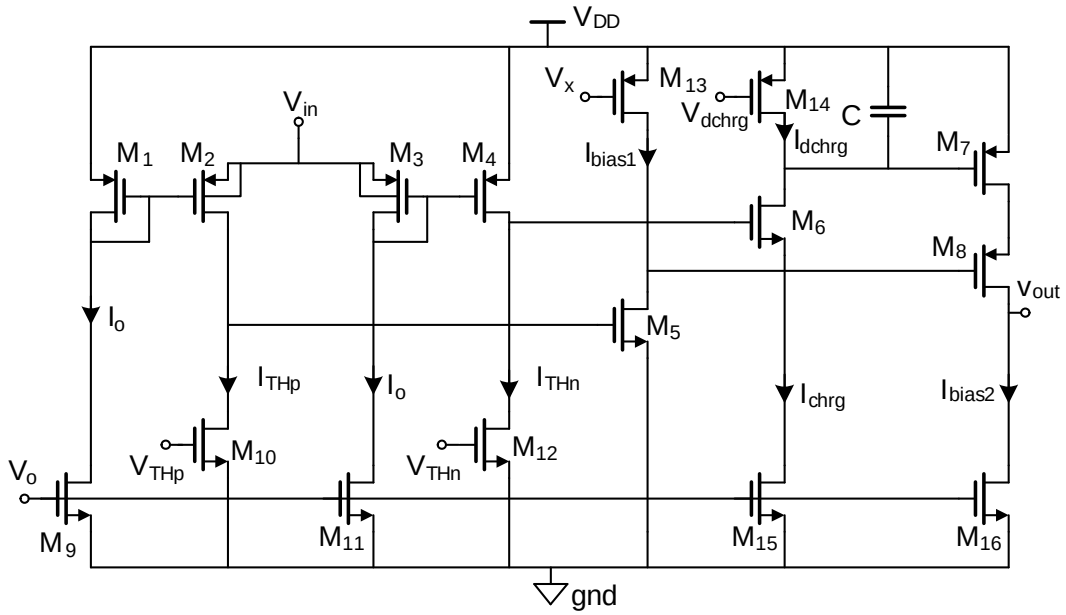


Figure 5.6: Dual threshold AP detector circuit.

5.3.4 *NOR-gate*

The circuit diagram of the NOR-gate is depicted in Fig. 5.5d. Current I_{bias2}, set by the voltage V_{bias2}, will flow only if both inputs V_p and V_{nDEL} are low. This will pull the voltage at V_{out} down and it becomes 0 V. Otherwise, current will not flow and $V_{out} = V_{DD}$. Fig. 5.2e illustrates the output of the NOR-gate.

The complete circuit diagram of the AP detector can be found in Fig. 5.6. It is a combination of the building blocks from Fig. 5.5a through Fig. 5.5d. An inverter, formed by M_5 and M_{13}, is inserted for pre-conditioning of the NOR gate to achieve the desired operation from the detector. It important to notice that all NMOST body terminals are connected to the ground, while PMOST body terminals are connected to V_{DD}, except body terminals of transistors M_2 and M_3. Their body terminals are connected to their sources in order to satisfy (5.1).

5.4 THE BIAS CIRCUIT

By using only one bias circuit for multiple AP detectors it is possible to save area and power consumption as the transistors and the current used to bias the bias circuit do not need to be repeated for every AP detector circuit. Fig. 5.7 shows the bias circuit. It consist of one current mirror and four diode transistors. Voltages V_o, V_x, V_{THn}, V_{THp} and V_{dchrg} are generated only once and can be easily connected to several AP detectors.

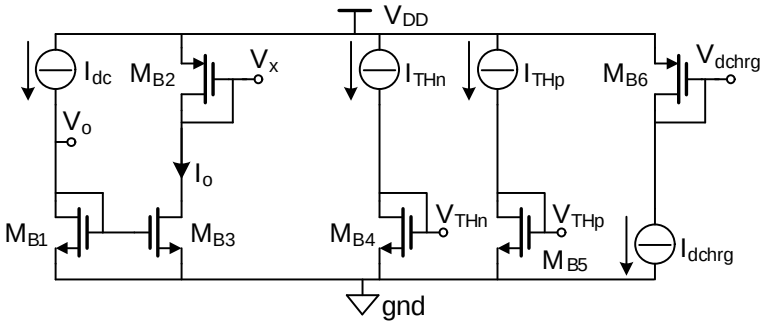


Figure 5.7: Dual threshold AP bias detector circuit.

Table 5.1: The DTD MOS transistors sizes.

Transistor(s)	1-8	9, 11	10, 12, 16	13	14	15
W / L * F [µm]	3 / 10	1 / 10	3 / 7	2.3 / 10	5.6 / 10	15 / 5 * 2

5.5 THE DETECTOR LAYOUT

The layout of the single AP detector is shown in Fig. 5.8. The connectors of the seven common voltages of each AP detector can be seen twice, on the top and on the bottom of the AP detector. The connectors for voltages V_{in} and V_{out}, which are unique for every AP detector, are on the left hand side of the same figure. This structure is chosen as the inter-connection of several AP detectors can be made easily by just placing AP detectors on the top of each other. An illustration of six AP detectors and one bias circuit is shown in Fig. 5.9. This structure provides extra safety. In case one of detectors fails to work, the voltages can reach other detectors by using the alternate voltage path.

5.6 SIMULATION RESULTS

The operation of the AP detector circuit was verified in Cadence using RF spectre and AMIS 0.35 µm technology (I3T80). MOS transistor width (W), length (L) and number of fingers (F) were set according to Table 5.1 for the detector and Table 5.2 for the bias circuit. Supply voltage $V_{DD} = 1$ V. At 37 °C the quiescent power consumption equals 1.5 nW and the average power consumption over 200 ms equals 1.8 nW. Capacitor C = 3 pF. The various current source values are given in Table 5.3. The threshold currents I_{THp} and I_{THn} are selected such that there is an almost equal minimum number of false positive and false negative detections over the time period of 200 ms.

Fig. 5.10 shows the transient response of the Dual Threshold Detector (DTD) circuit. It can be seen that the detector is able to successfully isolate APs from the noisy signal.

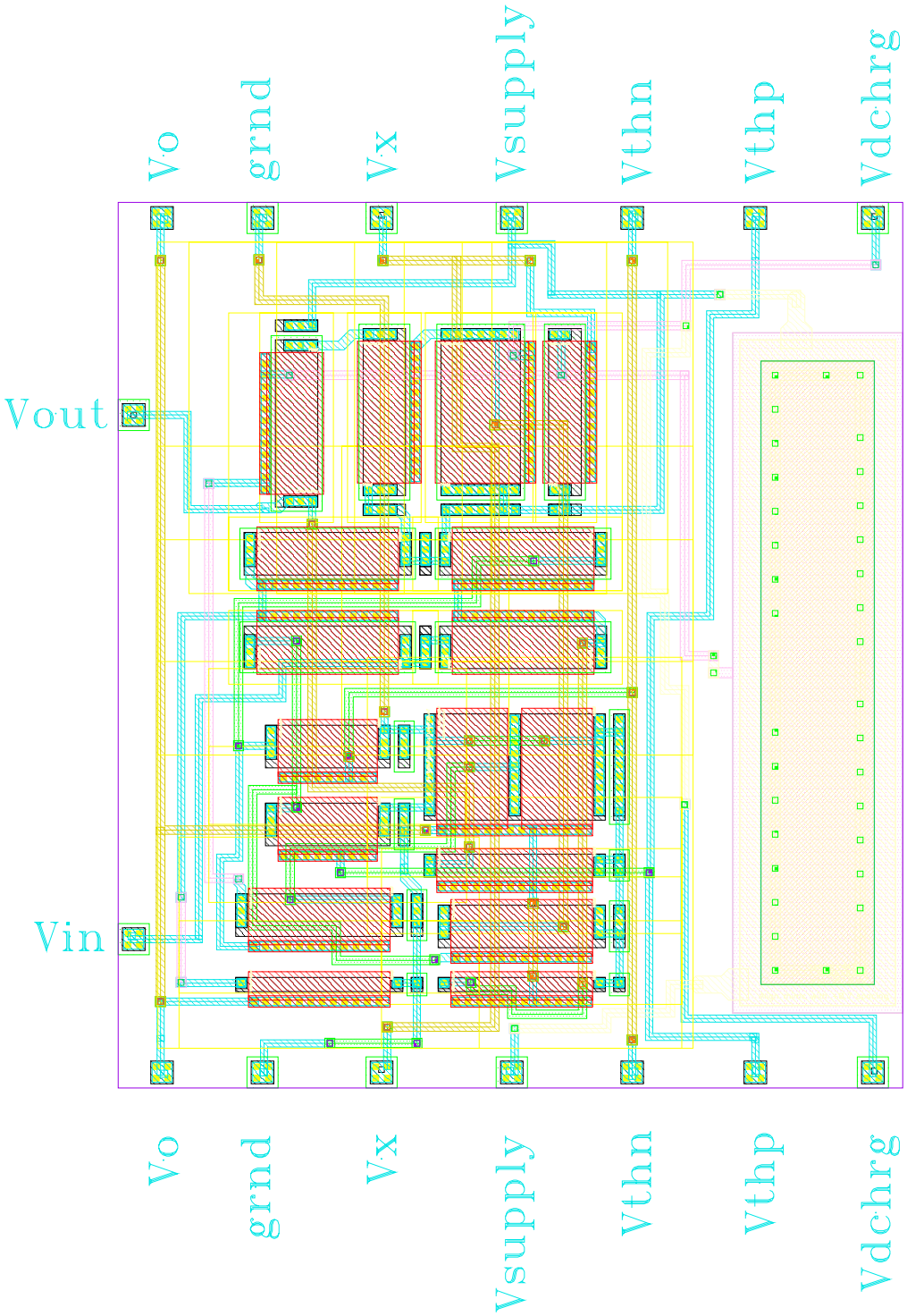


Figure 5.8: The layout of a single AP detector cell.

Table 5.2: The DTD MOS bias transistors sizes.

Transistor(s)	M_{B1}-M_{B3}	M_{B4}-M_{B5}	M_{B6}
W / L [µm]	3 / 10	3 / 7	5.6 / 10

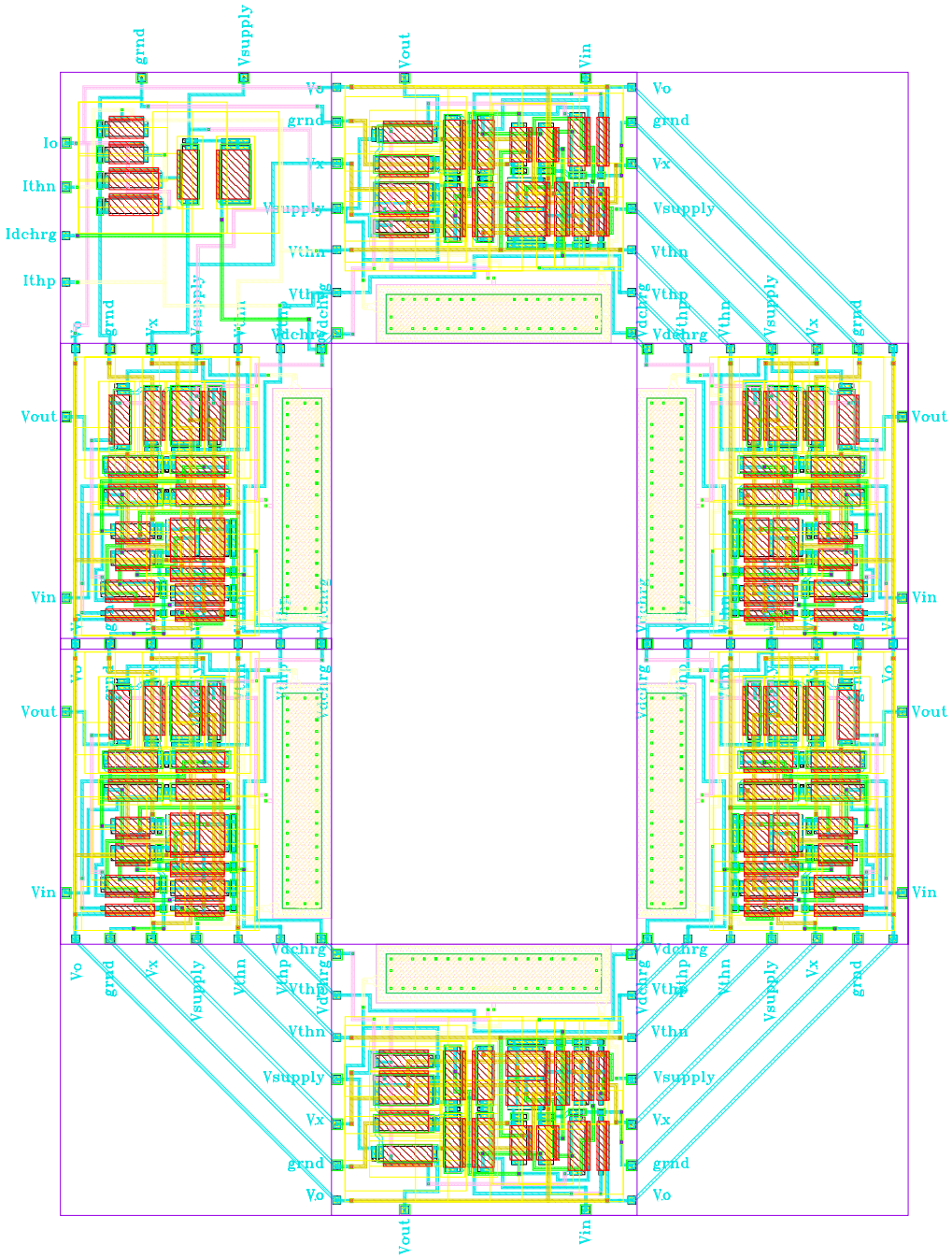


Figure 5.9: The DTD layout of 6 AP detector cells and their biasing circuitry.

Table 5.3: Current sources

source	I_o	I_{THp}	I_{THn}	I_{bias1}	I_{bias2}	I_{chrg}	I_{dchrg}
I [nA]	0.37	0.78	0.73	0.71	0.5	103	1.9

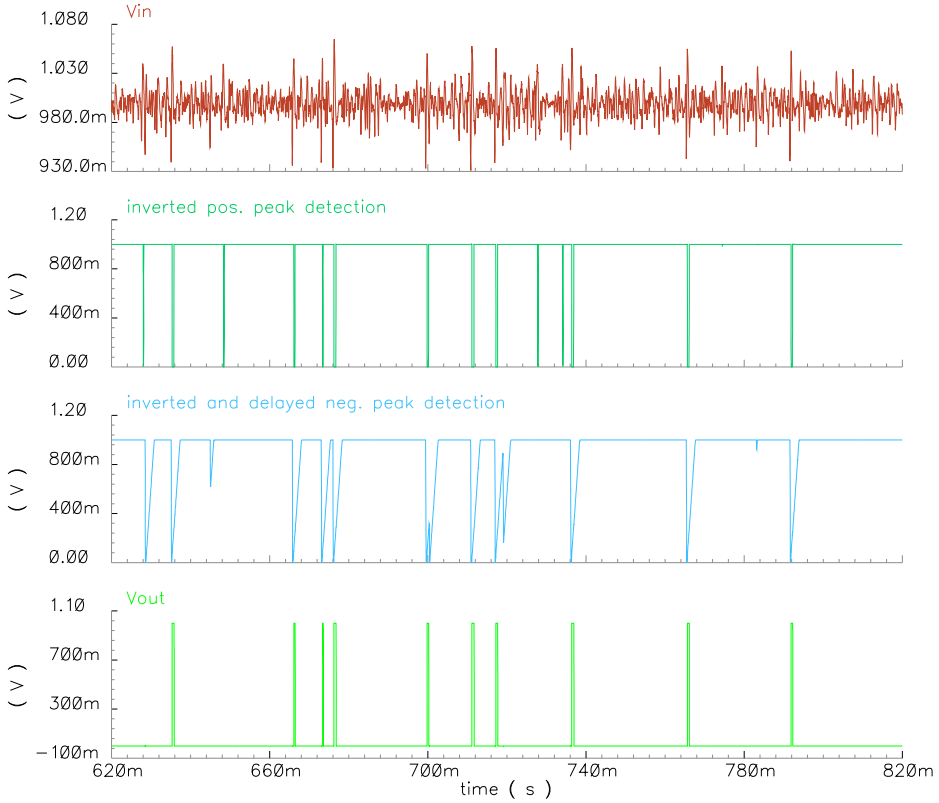


Figure 5.10: Transient response of the DTD. Input signal SNR of 6 dB.

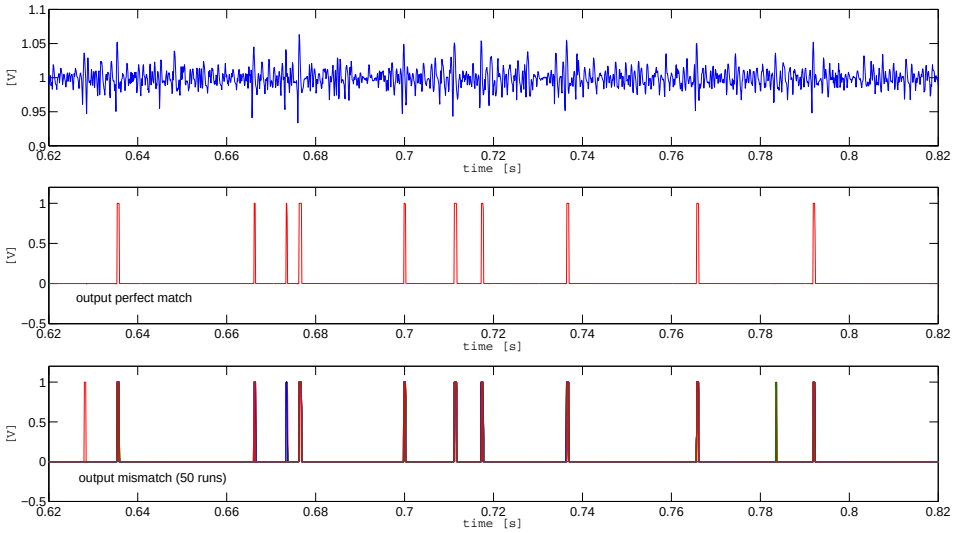


Figure 5.11: Transient response of the DTD [red] and output of Monte Carlo simulations. Input signal SNR of 6 dB.

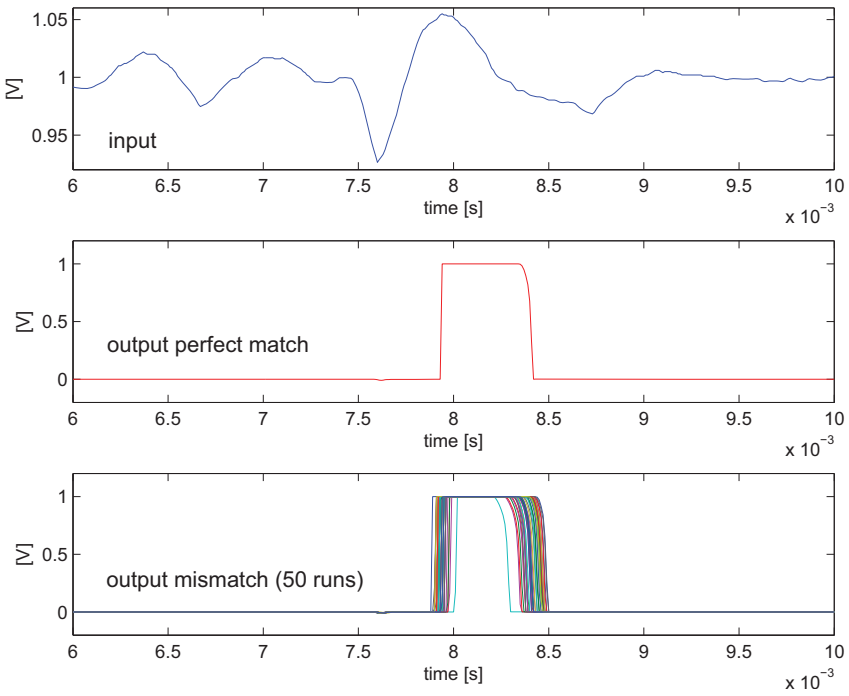


Figure 5.12: Monte Carlo simulation zoom in. Input signal SNR of 10.

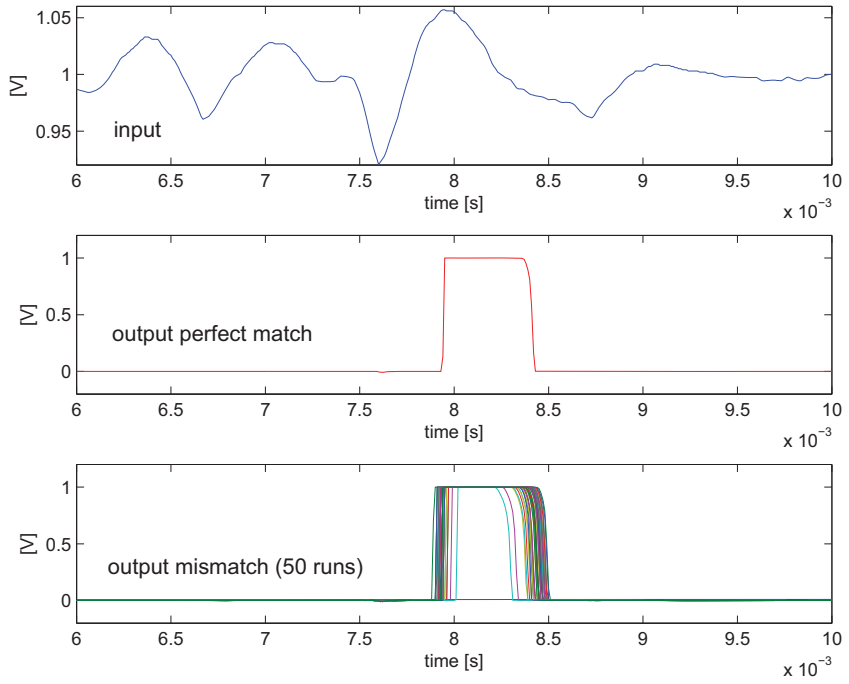


Figure 5.13: Monte Carlo simulation zoom in. Input signal SNR of 6.

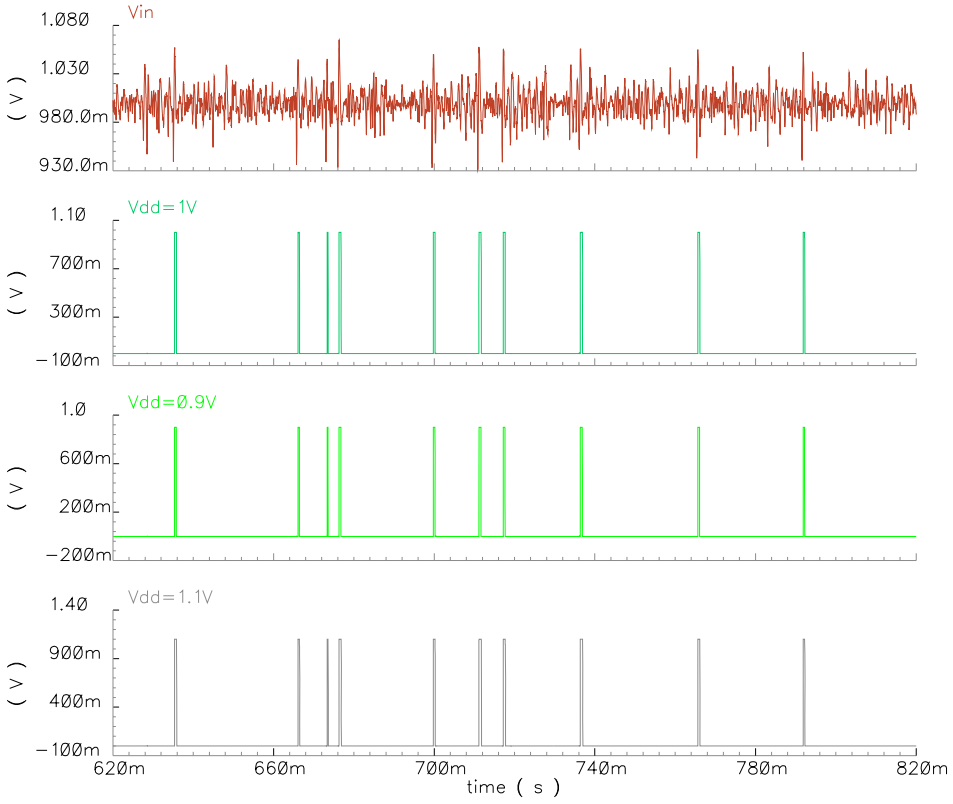


Figure 5.14: 10 % variations of the supply voltage. Input signal SNR of 6.

A Monte Carlo simulation of 50 runs over the period of 200 ms is performed. Zoomed-in versions of a single AP detection for two different input SNRs are depicted in Fig. 5.12 and Fig. 5.13. As we can see, mismatch variations have bigger influence on the circuit operation in case SNR decreases. For the input signal with SNR = 6, we can see that one false negative detection occurred in 50 runs.

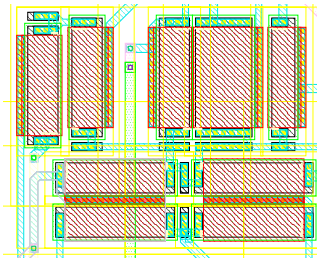
For 10 % supply voltage variations, in case of an input SNR=6, shown in Fig. 5.14, we see that there is no influence on the circuit operation.

5.7 CONCLUSIONS

A dual-threshold action potential detection circuit to be used in real-time applications has been presented. The CMOS version of the resulting circuit comprises one capacitor and a handful of transistors. Simulations show that the proposed circuit consumes very little power and is able to reliably detect the action potentials in the input signals even in case of very limited SNR. Due to the compact circuit architecture and the low power consumption, the proposed circuit is a good candidate for multi-electrode spike detection.

6

SUMMARY, CONCLUSIONS AND RECOMMENDATIONS



6.1 SUMMARY AND CONCLUSIONS

As an effective treatment against various diseases originating in the brain, electrical neurostimulation has great potential. Currently, neurostimulators are simply too big and have large power consumption to be implemented in the brain. Implementing such devices elsewhere in the human body necessitates the use if transcutaneous wires which can lead to several medical complications. Clearly, a small form factor and low power consumption of fully implantable medical devices are important parameters that need to be satisfied.

Fully autonomous AP detectors can greatly decrease the power consumption of neurostimulators by decreasing the wireless link data rate. Such detectors can also help to trigger automatic recording around each AP as well as help to classify and distinguish between different neurons. Reducing the power consumption also helps to make the battery size as small as possible.

In this thesis several AP detection methods have been investigated. It turns out that only energy based detectors ands simple threshold detectors satisfy the constrains of compact and low power multielectrode AP detectors. As a result, it was chosen to design dynamic translinear nonlinear operator as well as a simple dual threshold detector.

Subsequently, both of them, the dynamic translinear nonlinear energy operator circuit and a dual threshold detector circuit have been designed. From the simulation results of both detectors we can see that both detectors are successfully able to discriminate APs in noisy signals. Nevertheless, due to differences in the technology used, performance of the detectors, size and power consumption, it can be concluded that the dual threshold detector presented in Chapter 5 outperforms the nonlinear energy operator circuit in several ways. Namely:

1. The dual threshold algorithm outperforms the NEO algorithm as shown in Chapter 5.
2. The dual threshold circuit is much smaller than the NEO circuit.
3. The power consumption of the dual threshold detector circuit is much smaller than in case of the DTL NEO circuit.

The results from this thesis project have been presented at two international IEEE conferences. Scientific contributions made in this thesis are:

- The system level performance of several AP detection methods is compared in Chapter 3.
- The dynamic translinear principle has been successfully applied to design the NEO circuit [30].
- A very compact, nano-power AP detectors been proposed [45].

6.2 RECOMMENDATIONS

Based on the results found in this thesis project a couple of recommendations can be made for further research

- Although the dual threshold detector proposed in this thesis achieves good performance over wide range of input /acp SNR, there are still some open problems. How to choose right threshold values for certain input SNR? Having different threshold values for different /acp SNR the detector performance can be improved. A possible solution would be to use adaptive thresholding. However, introducing an adaptive thresholding mechanism will increase power consumption and make the circuit bigger. The trade-off between performance versus power consumption and circuit size should be investigated in more detail for this specific case.
- Due to limited time there are no experimental results reported in the thesis. Measurements on an actual chip could verify the correct operation of the dual threshold detector when implemented.

APPENDIX

A

TABLE OF ACRONYMS USED IN THE TEXT

AP Action Potential

ATA Adaptive Threshold Algorithm

ATD Adaptive Threshold Detector

BiCMOS Bipolar and Complementary Metal-Oxide-Semiconductor

BJT Bipolar Junction Transistor

BMI Brain Machine Interface

CMOS Complementary Metal-Oxide-Semiconductor

CCW Counter-ClockWise

CW ClockWise

DE Differential Equation

DTA Dual Threshold Algorithm

DTD Dual Threshold Detector

DTL Dynamic Translinear

ECG ElectroCardioGraphy

EEG ElectroEncephaloGraphy

EMG ElectroMyoGraphy

EB Energy Based

LFP Local Field Potential

MEMS MicroElectroMechanical System

MF Matched Filter

MOS Metal-Oxide-Semiconductor

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

NEO Nonlinear Energy Operator

NMOST N-channel Metal-Oxide-Semiconductor Transistor

PMOST P-channel Metal-Oxide-Semiconductor Transistor

PB Pulse Based

RF Radio Frequency

SNR Signal to Noise Ratio

ST simple threshold

STL Static Translinear

TL Translinear

VCCS Voltage Controlled Current Source

WT Wavelet Transform

B

TRANSLINEAR NEO DECOMPOSITION

In continuous time the NEO is defined as

$$y(\tau) = \left(\frac{\partial x(\tau)}{\partial \tau}\right)^2 - x(\tau)\frac{\partial^2 x(\tau)}{\partial \tau^2}. \tag{B.1}$$

The signals $y(\tau)$ and $y(\tau)$ can be transformed into the currents through the equations

$$I_{in} = xI_o \tag{B.2}$$

and

$$I_{out} = yI_o. \tag{B.3}$$

The dimensionless time τ can be transformed into the time t with dimension [s] through

$$\left(\frac{\partial}{\partial \tau}\right)^k = \left(\frac{CV_t}{I_o}\right)^k \left(\frac{\partial}{\partial t}\right)^k. \tag{B.4}$$

Applying the above transformations, the resulting differential equation becomes

$$I_{out} I_o^3 = (C_1 V_t \dot{I}_{in})^2 - I_{in} (C_2 V_t)^2 \ddot{I}_{in}. \tag{B.5}$$

Defining I_{cap1} as

$$I_{cap1} = C_1 V_t \frac{\dot{I}_{in}}{I_{in} + I_o} \tag{B.6}$$

or, alternatively written,

$$\dot{I}_{in} = \frac{I_{cap1}(I_{in} + I_o)}{C_1 V_t} \tag{B.7}$$

and I_{cap2}

$$I_{cap2} = C_2 V_t \frac{\dot{I}_{cap1}}{I_{cap1} + I_o} = C_1 C_2 V_t^2 \frac{\ddot{I}_{in}(I_{in} + I_o) - \dot{I}_{in}^2}{(I_{in} + I_o)^2 (I_{cap1} + I_o)} \tag{B.8}$$

or, alternatively written,

$$\ddot{I}_{in} = \frac{I_{cap2}(I_{in} + I_o)(I_{cap1} + I_o)}{C_1 C_2 V_t^2} + \frac{I_{cap1} I_{in}}{C_1 V_t} \tag{B.9}$$

in case of

$$C_1 = C_2 \tag{B.10}$$

the above differential equation (B.5) transforms into

$$I_{out} I_o^3 = I_{cap1}^2 (I_{in} + I_o)^2 - I_{in}(I_{in} + I_o)(I_{cap1} + I_o) I_{cap2} - I_{in}(I_{in} + I_o) I_{cap1}^2. \tag{B.11}$$

Adding terms (B.12) through (B.17) to (B.11) we eliminate negative transistor currents

$$(-I_o)(I_{in} + I_o)(I_{cap1}^2) \tag{B.12}$$

$$I_o(I_{in} + I_o)(I_o + I_{cap1})(-I_{cap2}) \tag{B.13}$$

$$(I_{in} + I_o)^2 (I_o + I_{cap1}) I_o \tag{B.14}$$

$$I_o^2 (I_{in} + I_o)(I_o + I_{cap1}) \tag{B.15}$$

$$I_o^2 (I_{in} + I_o)(-I_{cap1}) \tag{B.16}$$

$$-I_o^2 (I_{in} + I_o)(I_{cap1} + I_o) \tag{B.17}$$

and obtain following equation

$$\begin{aligned} I_{out}I_o^3 &= I_o(I_o+I_{in})(I_o+I_{cap1})^2 - I_o(I_o+I_{in})(I_o+I_{cap1})(I_o-I_{cap2}) \\ &- I_o(I_o+I_{in})^2(I_o+I_{cap1}) + (I_o+I_{in})^2(I_o+I_{cap1})(I_o-I_{cap2}) \\ &- I_o^2(I_o+I_{in})(I_o+I_{cap1}) + I_o^3(I_o+I_{in}). \end{aligned} \tag{B.18}$$

Defining I_A and I_B as

$$I_A = \frac{(I_{in}+I_o)^2(I_{cap1}+I_o)}{I_o^2} \tag{B.19}$$

and

$$I_B = \frac{(I_{in}+I_o)(I_{cap1}+I_o)}{I_o} \tag{B.20}$$

we obtain four valid TL loop equations (B.21) through (B.24)

$$I_{out}I_o = I_B(I_o+I_{cap1}) - I_B(I_o-I_{cap2}) - I_AI_o + I_o(I_o+I_{in}) + I_A(I_o-I_{cap2}) - I_BI_o \tag{B.21}$$

$$I_o\left[I_{out}+I_A-(I_{in}+I_o)+2I_B\right] + (I_o-I_{cap2})(2I_B-I_A) = I_B(I_{cap1}+3I_o-I_{cap2}) \tag{B.22}$$

$$I_R = \frac{\left[I_{out}+I_A-(I_{in}+I_o)+2I_B\right]I_o}{(I_{cap1}+I_o)+(I_o-I_{cap2})+I_o} \tag{B.23}$$

$$I_L = \frac{(2I_B-I_A)(I_o-I_{cap2})}{(I_{cap1}+I_o)+(I_o-I_{cap2})+I_o} \tag{B.24}$$

with

$$I_L + I_R = I_B. \tag{B.25}$$

C

MAPLE CODES

C.1 TRANSLINEAR DECOMPOSITION VERIFICATION

```
restart;
# parametar definition

f:=3e3:
C1:=10e-12:
C2:=10e-12:
Vt:=25.9e-3:
Iin:=400e-12*sin(2*Pi*f*t)*exp(-500*t):
Io:=3e-9:

# ideal NEO

NEO:=((C1*Vt*diff(Iin,t))^2-Iin*(C2*Vt)^2*diff(diff(Iin,t),t))/Io^3:

# intermediate currents

IA:=(Iin+Io)^2*(Io+Icap1)/Io^2:
IB:=(Iin+Io)*(Io+Icap1)*Io/Io^2:

# capacitance currents

Icap1:=C1*Vt*diff(Iin,t)/(Iin+Io):
Icap2:=C2*Vt*diff(Icap1,t)/(Icap1+Io):

# TL decomposition (and plot)

Iout_STL:=(IB^2*(Icap1+3*Io-Icap2)-IB*(Io-Icap2)*(2*IB-IA))/(IB*Io)-IA-2*IB+(Iin+Io):
plot([Iin, Iout_STL,NEO ], t=0..3e-3, color=[black, black, red], style=[line, line, line],
thickness=[1, 3, 5], legend=["input","output decomposition", "ideal NEO"]);
```

C.2 4 TRANSISTORS STL LOOP ERROR INTRODUCED

```
restart;

# parametar definition

f:=3e3:
C1:=10e-12:
C2:=10e-12:
Vt:=25.9e-3:
Iin:=400e-12*sin(2*Pi*f*t+90)*exp(-500*t*1):
beta:=1:
Io:=3e-9:
error_in_percent1:=3:
error_in_percent2:=0:
Y:=Io*(C1*Vt/Io)^2*((diff(Iin/Io,t))^2-Iin/Io*diff(diff(Iin/Io,t),t)):

# capacitance currents

Icap1:=C1*Vt*diff(Iin,t)/(Iin+Io):
Icap2:=C2*Vt*diff(Icap1,t)/(Icap1+Io):

# intermediate currents

IA:=(Iin+Io)^2*(Io+Icap1)/Io^2:
IB:=(Iin+Io)*(Io+Icap1)/Io:

# STL part 1

IL:=(2*IB-IA)*(beta*Io-Icap2)/((Icap1+Io)+(beta*Io-Icap2)+beta*Io):
IL_error:=IL-IL/100*error_in_percent1:

# STL part 2

IR_errorIL:=IB-IL_error:

STL2_error:=((Icap1+Io)+(beta*Io-Icap2)+beta*Io)*IR_errorIL/Io:
Iout_error:=STL2_error-STL2_error/100*error_in_percent2-(beta*IA-(Iin+Io)+2*IB):

plot([Iin, Iout_error,Y], t=0..3e-3, color=[black, red, green, yellow, orange, violet],
legend=["input","output", "ideal"],linestyle=[solid, longdash, dash],
thickness=[2, 2, 2, 1]);
```

D

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Dynamic Translinear Nonlinear Energy Operator

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***Abstract*—The dynamic translinear principle, in contrast to the conventional, i.e., static, translinear principle, can be used for the realization of frequency dependent transfer functions. Using the dynamic translinear principle we can realize both linear and nonlinear differential equations. This paper presents the dynamic translinear realization of the nonlinear second-order differential equation describing the nonlinear energy operator performing the real time energy detection of analog signals. The expected behavior of the designed nonlinear energy operator is demonstrated by means of simulations.**

***Index Terms*—nonlinear energy operator, structured synthesis, dynamic translinear circuits, non-linear, analog integrated circuits, low power, low voltage**

I. Introduction

Translinear circuits are based on the exponential behavior of the bipolar transistor or the MOS transistor operating in the sub-threshold region. Translinear circuits are supposed to be a promising alternative in the area of low-voltage design, as the voltages in the translinear circuits are logarithmically related to the currents. Conventional, i.e., static, translinear circuits can be used to realize a wide variety of linear and nonlinear functions. By allowing capacitors in the translinear loops, the dynamic translinear circuits can be used to implement linear and nonlinear differential equations [1]. As an extension to conventional translinear circuits, dynamic translinear circuits inherit advantages of conventional translinear circuits. The main advantage is a high functional density, which makes translinear circuits suitable for low voltage, low-power applications.

To monitor the real-time energy of neural signals, including action potentials (spikes) and local field potentials [2], [3], the nonlinear energy operator (NEO) [4] is considered a good candidate since it is capable of discriminating between the desired pulse and the background noise as their energies are considered differently [5]. The NEO implements a nonlinear second order differential equation which is can directly put on silicon by using dynamic translinear circuit techniques.

In this paper, we apply the structured synthesis method for dynamic translinear circuits [6] to design the NEO. The static and dynamic translinear principles are reviewed in Section 2. In Section 3, the design of the NEO using the proposed synthesis method employing bipolar transistors is given. Section 4 discusses the simulation results of the corresponding design. Finally, the conclusions are presented in Section 5.

II. Translinear Principle

Translinear (TL) circuits can be divided into static (STL) and dynamic (DTL) circuits. Using STL circuits we can implement linear and nonlinear static transfer functions. Frequency-dependent (transfer) functions, i.e., differential equations (DEs) can be realized by DTL circuits. In this section we will review the STL and DTL principles by means of two examples.

A. Static Translinear Principle

The TL principle is based on the exponential behavior between voltage and current of the bipolar transistor and the MOS transistor in weak inversion region. In the following discussion, bipolar transistors are assumed. The collector current of bipolar transistors is given by

$$I_c = I_s e^{(V_{be}/V_T)}, \tag{1}$$

where I_s is the zero-bias current, V_{be} is the base-emitter voltage, $V_T = kT/q$ is the thermal voltage.

The TL principle applies to loops of semiconductor junctions, characterized by an even number of junctions [7], [8]. The number of devices with a clockwise orientation equals the number of counter-clockwise oriented devices. An example of a four-transistor TL loop is shown in Fig. 1. It is assumed that the transistors are biased at collector currents I_1 through I_4. When all devices are equivalent and operate at the same temperature, the TL loop is described by a simple static equation

$$I_1 I_3 = I_2 I_4. \tag{2}$$

B. Dynamic Translinear Principle

By admitting capacitors in the TL loops, frequency-dependent transfer functions can be realized. The DTL principle can be explained with reference to the sub-circuit shown

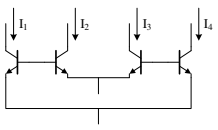

Figure 1. A four-transistor translinear loop.

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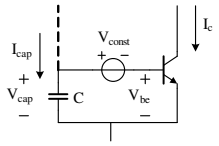

Figure 2. Principle of dynamic translinear circuits.

in Fig. 2. This circuit is described in terms of the collector current I_c and the capacitance current I_{cap} flowing through capacitance C. Note that the dc voltage source V_{const} does not affect I_{cap}. An expression for I_{cap} is easily be derived by taking the time derivative of (1)

$$I_{cap} = CV_t\frac{\dot{I}_c}{I_c}, \tag{3}$$

where the dot represents differentiation with respect to time. Equation (3) shows that I_{cap} is a function of I_c and its time derivative $\dot{I}_c$. By slightly rewriting equation (3)

$$CV_t\dot{I}_c = I_{cap}I_c, \tag{4}$$

we can directly state the DTL principle: *A time derivative of a current can be mapped onto a product of currents* [6]. From this point on, the product of currents on the right-hand side of (4) can easily be realized by the conventional STL principle. The DTL principle can be used to implement a wide variety of DEs, describing signal processing functions.

III. Dynamic Translinear NEO Operator

This section demonstrates the design of the NEO using the DTL structured synthesis method. Synthesis of a dynamic circuit, starts with a DE or with a set of DEs describing its function. The NEO operator can be described in the time domain by

$$y(\tau) = \left(\frac{\partial x(\tau)}{\partial \tau}\right)^2 - x(\tau)\frac{\partial^2 x(\tau)}{\partial \tau^2}, \tag{5}$$

where x and y represent the input and the output signal, respectively.

At first glance from (5), it seems like, in order to realize this function, differentiator, squarer and multiplier circuits are needed, which leads to a complex topology. Using the DTL structured synthesis method, (5) can be implemented by a very simple and compact topology of translinear loops circuit which will be shown shortly.

A. Transformations

An important difference between the mathematical and electronic domain is that the latter one is bounded by quantities having dimensions. To find an implementation of the mathematical equation we need to transform all time-varying signals in the DEs, i.e., the input signals, the output signals and the tunable parameters into currents [6]. Thus, the first step of dynamic structured synthesis is to add dimensions to the dimensionless mathematical equations. For the above expression, x and y can be transformed into the currents $I_{in} = xI_o$ and $I_{out} = yI_o$, I_o being the DC bias current that determines the absolute current swings. The dimensionless time τ, can be transformed into the time t with its usual dimension [s], using the equivalence relation given by

$$\left(\frac{\partial}{\partial \tau}\right)^k = \left(\frac{CV_t}{I_o}\right)^k \left(\frac{\partial}{\partial t}\right)^k. \tag{6}$$

Subsequently, dimensionless differential equation (5) is transformed into current-mode differential equation

$$I_{out}I_o^3 = (C_1V_t\dot{I}_{in})^2 - I_{in}\left(C_2V_t\right)^2\ddot{I}_{in}. \tag{7}$$

B. Definition of the Capacitance Currents

By introducing the capacitance currents we are able to implement DEs by translating time derivatives into products of currents. Note that (5) is a second-order differential equation, which means that we need to take the time derivative of the first capacitance current that already contains the time derivative in order to map this equation on silicon. Thus, we need two capacitance currents. Defining I_{cap1} and I_{cap2} as

$$I_{cap1} = C_1V_t\frac{\dot{I}_{in}}{I_{in}+I_o} \tag{8}$$

and

$$\begin{aligned} I_{cap2} &= C_2V_t\frac{\dot{I}_{cap1}}{I_{cap1}+I_o} \\ &= C_1C_2V_t^2\frac{\ddot{I}_{in}(I_{in}+I_o)-\dot{I}_{in}^2}{(I_{in}+I_o)^2(I_{cap1}+I_o)}. \end{aligned} \tag{9}$$

for $C_1 = C_2$, current-mode differential equation (7) yields a current-mode polynomial without derivatives:

$$\begin{aligned} I_{out}I_o^3 &= I_{cap1}^2(I_{in}+I_o)^2 \\ &- I_{in}(I_{in}+I_o)(I_{cap1}+I_o)I_{cap2} \\ &- I_{in}(I_{in}+I_o)I_{cap1}^2. \end{aligned} \tag{10}$$

As we can see, the above DE is now described by a current-mode polynomial where the time derivatives and capacitances are hidden in the capacitance currents. Observe that input current I_{in} and both capacitance currents, I_{cap1} and I_{cap2} can be positive and negative. As a consequence, a bias current needs to be added such that the collector currents always remain positive. By doing so, (10) becomes (11)

$$\begin{aligned} I_{out}I_o^3 &= I_o(I_o+I_{in})(I_o+I_{cap1})^2 \\ &- I_o(I_o+I_{in})(I_o+I_{cap1})(I_o-I_{cap2}) \\ &- I_o(I_o+I_{in})^2(I_o+I_{cap1}) + I_o^3(I_o+I_{in}) \\ &+ (I_o+I_{in})^2(I_o+I_{cap1})(I_o-I_{cap2}) \\ &- I_o^2(I_o+I_{in})(I_o+I_{cap1}). \end{aligned} \tag{11}$$

Both sides of the above DE are now described by current-mode polynomials and from this point on, the synthesis procedure for static TL circuits can be used [8].

C. Translinear Decomposition

The next synthesis step is translinear decomposition. That is, the current-mode polynomial has to be transformed into one or more TL loop equations that are characterized by the general equation

$$\prod_{CW} J_{C,i} = \prod_{CCW} J_{C,i}, \tag{12}$$

$J_{C,i}$ being the transistor collector current densities in clockwise (CW) or counter-clockwise (CCW) direction. As 'non-parametric' decomposition is not always possible, we can utilize 'parametric' decomposition of (11). It means that one or more intermediate currents need to be defined, introducing extra TL loops. If possible, extra TL loops should be included into existing TL loops, which will save us extra current branches and lower the total power consumption. Here, two intermediate currents I_A and I_B are defined. As a result, there will be four valid TL equations (13), (14), (15) and (16)

$$I_B I_o = (I_{in} + I_o)(I_{cap1} + I_o), \tag{13}$$

$$I_A I_o^2 = (I_{in} + I_o)^2 (I_{cap1} + I_o), \tag{14}$$

$$\begin{gathered}[I_{out} + I_A - (I_{in} + I_o) + 2I_B] I_o \\ = \\ [(I_{cap1} + I_o) + (I_o - I_{cap2}) + I_o] I_L,\end{gathered} \tag{15}$$

$$\begin{gathered}(2I_B - I_A)(I_o - I_{cap2}) \\ = \\ [(I_{cap1} + I_o) + (I_o - I_{cap2}) + I_o] I_R,\end{gathered} \tag{16}$$

with

$$I_L + I_R = I_B. \tag{17}$$

These functions are readily implemented in TL circuits [7], [8].

D. Circuit Implementation

The last synthesis step is the circuit implementation. The TL decomposition that was found during the previous synthesis step has to be mapped onto a TL circuit topology. A possible realization of the first capacitance current and intermediate currents is shown in Fig. 3. The TL loop formed by $Q_1 - Q_2 - C_1$, implement (8). Note that V_{BEQ2} can be considered a constant voltage source. Transistors $Q_1 - Q_2 - Q_3 - Q_4$ and $Q_1 - Q_2 - Q_3 - Q_5 - Q_6 - Q_7$ implement (13) and (14), respectively. M_2 through M_4 provide feedback and minimize the base currents, which results in more accurate intermediate currents. M_1 and M_5 ensure that the correct collector current will flow through Q_1 and set the V_{CQ1} to desired value. $V_{\rm ref1}$ provides some headroom for M_5.

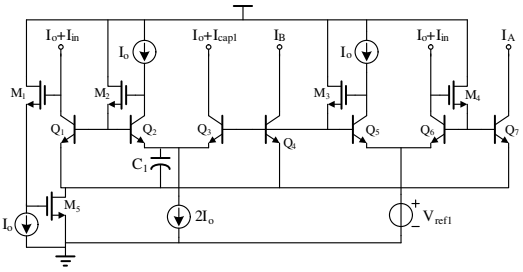

Figure 3. Implementation of the capacitance and the intermediate currents: (8), (13) and (14)

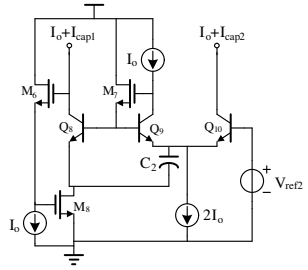

Figure 4. Implementation of the capacitance current: (9)

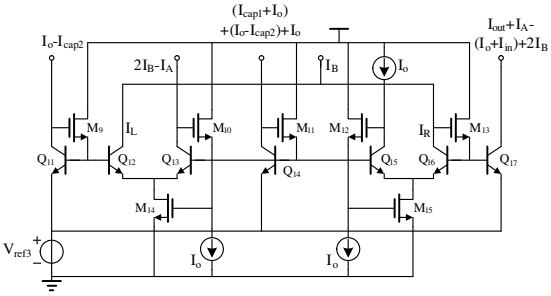

Figure 5. Implementation of the TL loops equations (15) through (17)

In Fig. 4, a circuit realizing the second capacitance current is shown. Loop $Q_8 - Q_9 - C_2$ implements (9). Voltage V_{be} across Q_9 is constant. M_6 and M_8 have the same function for Q_8 as M_1 and M_5 for Q_1. Function of M_7 is to minimize base currents. Headroom of M_8 is ensured by properly choosing $V_{\rm ref2}$.

Fig. 5 shows the circuit that implements (15) through (17). Transistors $Q_{11} - Q_{12} - Q_{13} - Q_{14}$ and $Q_{14} - Q_{15} - Q_{16} - Q_{17}$ implement (15) and (16), respectively. The function of the MOS transistors M_9 through M_{15} is as discussed before. $V_{\rm ref3}$ lifts the drain voltage of M_{14} and M_{15} for proper biasing.

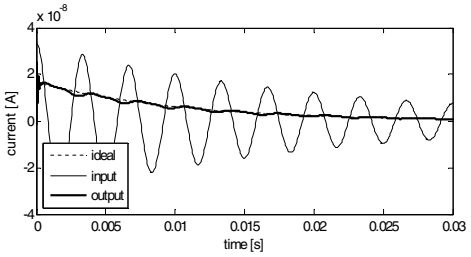

Figure 6. NEO applied to a damped sinusoidal signal. The output of NEO is showing the energy of the input sinusoidal.

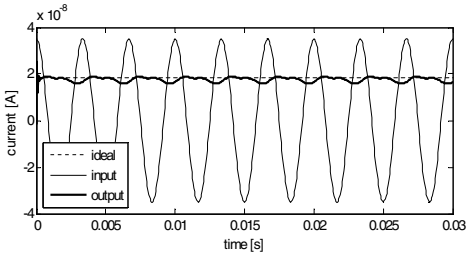

Figure 7. NEO applied to a constant sinusoidal signal. The output of the NEO has a constant magnitude when the input signal amplitude and frequency are constant.

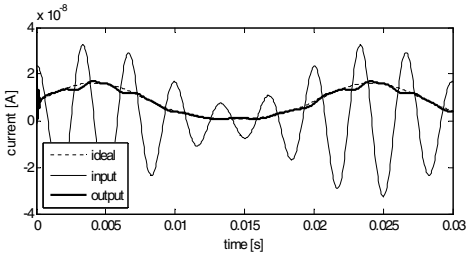

Figure 8. NEO applied to the sum of two sinusoids with different frequencies and the same amplitude. The output of the algorithm oscillates at the different frequency, about the sum of the energies in the two sinusoids.

IV. Simulation Results

The final circuit was verified in Cadence using RF spectre and AMIS 0.35 μm technology (I3T80). MOS transistor width (W) and length (L) were set as $W/L_{1-13} = 2\mu\text{m}/0.7\mu\text{m}$, $W/L_{14} = 4\mu\text{m}/0.7\mu\text{m}$ and $W/L_{15} = 1\mu\text{m}/1\mu\text{m}$. NPN transistor area is $16\mu\text{m}^2$. Supply voltage $V_{DD} = 2\text{V}$, reference voltages $V_{\text{ref1}} = 0.2\text{V}$, $V_{\text{ref2}} = 0.72\text{V}$, $V_{\text{ref3}} = 0.1\text{V}$ and bias current $I_o = 100\text{nA}$. The quiescent power consumption equals $7.2\mu\text{W}$.

Fig. 6 shows the transient response of the NEO in case a damped sinusoidal signal is applied to the input. The dashed line represents the output current of the NEO for the ideal case where (7) is applied directly to the input signal and the thick solid line shows the output of the NEO circuit. The thin solid line is the input. It can be seen that for larger input signal amplitudes, the output of the NEO is showing higher "energy". Lower energy occurs at a lower amplitude.

In the case of a constant amplitude and frequency sinusoidal input signal, the result is shown in Fig. 7. The dashed line represents the output current of the NEO for the ideal case and the thick solid line shows the output of the NEO circuit. The thin solid line is the input. It can be seen that in this case the NEO circuit is able to detect the energy of the input signal with small error resulting from nonideality effects in the form of a small ripple appearing at the output.

The output of the NEO, in case of an input signal consisting of two frequency components is shown in Fig. 8. The dashed line represents the output current of the NEO for the ideal case and the thick solid line shows the output of the NEO circuit. The thin solid line is the input. The output signal also follows the real energy of the input signal with a small error.

V. Conclusions

In this paper, the application of the dynamic translinear principle to realize a nonlinear second order differential equation to be used in real-time energy detection has been shown. The BiCMOS version of the resulting circuit comprises two identical capacitors and a handful of transistors. Simulation shows that the proposed circuit consumes very little power and is able to detect the instantaneous energies of different kinds of input signals. Thanks to the compact circuit architecture and the low power consumption, the proposed circuit is a good candidate for local field potential and spike detection.

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E

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A Compact, Nano-Power CMOS Action Potential Detector

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***Abstract*—Real time action potential (AP) detection is an important requirement for development of fully implantable neuroprosthetic devices. We present an ultra low-power CMOS analog circuit for detection of APs embedded in a noisy signal. The proposed strategy isolates APs by detecting subsequently a positive and a negative spike of each AP. An AP is detected only if the positive spike is detected within a short period of time after the negative spike was detected. The proposed circuit has been designed to be implemented in AMIS 0.35 μm technology (I3T80) and has been verified in Cadence using RF spectre. The final circuit operates from a 1-V supply and consumes only 1.5 nA. The detector is verified by means of simulations with synthetic neural waveforms and is able to successfully detect APs in noisy signals.**

***Index Terms*—analog integrated circuits, action potential detector, biomedical signal processing, CMOS, extracellular recordings, low-voltage, multichannel recordings, prosthetic devices, ultra low-power**

I. Introduction

Neuroscientists and neuroprosthetic devices require often real-time monitoring of biopotential activity of multiple neurons. Due to advances in microelectrode array technology, sensing devices of 100 or more electrodes are possible [1]. Efforts to develop fully implantable sensing devices bring along several circuit design challenges. Such clinical devices need to be as less intrusive as possible. Recorded data needs to be transmitted wirelessly to avoid tissue infections. Yet the power consumption of small implantable devices needs to be minimized to prevent heating and damage to nearby cells. Safety, power consumption and limited area are important parameters that need to be satisfied.

In scientific and neuroprosthetic devices, there is a need to automatically detect APs from each electrode. By detecting APs in low density neural waveforms and transmitting only relevant data, we can greatly decrease the power consumption of implantable devices [2]. Alternatively, automatic AP detection can be used to trigger recording around each AP [3]. By detecting APs close to the electrodes we can also help classifying APs and distinguish between different neurons. The remaining problem is how to perform this automatic AP detection from a noisy neural waveform in a small, low-power device.

In a typical AP detector, the signal is preprocessed to attenuate noise and to accentuate spikes. Subsequently, a threshold detector is used to determine spike locations [4]. Adaptive threshold spike detectors monitor the background noise and automatically adapt the threshold according to the noise level [5], [6]. Although simple thresholding detectors tend to be sensitive to noise, they remain attractive for real-time implementations because of their minute computational time. The efficacy of simple and adaptive threshold detectors is reduced by overlapping spikes.

Energy based spike detectors have also been used to detect APs [3], [7], [8], [9], [10], [11]. The nonlinear energy operator (NEO), also called the Teager energy operator, first characterized by Kaiser [12], estimates the square of the instantaneous product of amplitude and frequency of the input signal. In this regard, the NEO may be superior to other energy estimators as it explicitly takes frequency into account. However for low power multichannel applications, it is outperformed by simple threshold AP detectors [13].

Matched filter (MF) detectors are particularly effective when the spike waveform to be detected is already known. Since this is often not the case, the user must manually select a template [14]. Moreover, these detectors tend to exceed the limited chip area and power consumption. Besides, their computation time may preclude them in real-time multichannel detectors [4]. If the system is not limited by its power consumption, a matched filter with a non-specified template will be the detector of choice. [13].

Our strategy is to combine the simplicity of a simple threshold detector with the performance of semi MF detectors. We compare three predefined AP features with the measured signal. The AP is detected only if a positive peak is detected in a predefined time after a negative peak was detected. This "dual threshold" AP detection algorithm was originally proposed in [15], including additional filtering.

In this paper, we present an ultra low-power circuit for dual threshold AP detection. Its principle and system level design are reviewed in Section 2. In Section 3, the design of the AP detector circuit employing CMOS transistors operating in the subthreshold region is given. Section 4 discusses the simulation results of the corresponding design. Finally, the conclusions are presented in Section 5.

II. Proposed Dual Threshold AP Detector

The dual-threshold algorithm attempts to detect AP's in noisy signals by subsequently detecting the positive and the negative peaks of each AP. Occasional noise peaks will not

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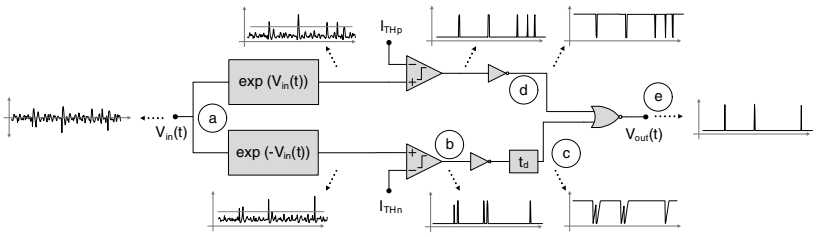

Figure 1. Blockdiagram of the proposed dual threshold AP detector.

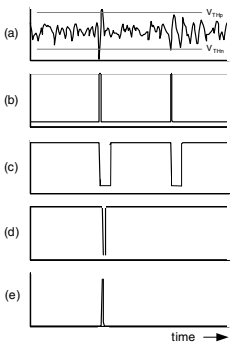

Figure 2. Waveforms at the various nodes in the AP detector. (a) Input neural waveform. (b) Negative peak, lower than V_{THn} is detected. (c) Detected negative peak LP filtered. (d) Detection of positive peak if the input signal is higher than V_{THp}. (e) In case (c) and (d) occur at the same time, an AP will be detected.

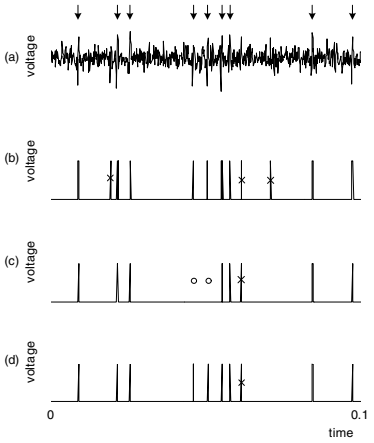

Figure 3. Transient response of three different algorithms. (a) Input neural waveform. (b) NEO response. (c) ATA response. (d) DTA response. O = false negative, X = false positive.

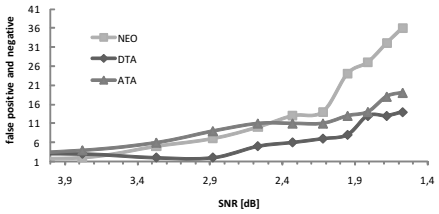

Figure 4. Performance comparison of three different algorithms

trigger the AP detector and incidental detection of false positives and false negatives will be minimized.

Fig. 1 shows the block diagram of the detector. It comprises 8 building blocks: two simple pre-processors, two comparators, two inverters, a delay t_d and a NOR logical gate. The two nonlinear pre-processors extract the input signal, enhancing the difference between the peaks and the noise level. Comparators are used with threshold levels I_{THp} and I_{THn} that can be adjusted separately. A delay is applied to hold the detected negative peak signal for a particular time. Its time constant depends on the AP duration. Finally, the NOR gate performs a logical NOR on the inverted positive peak detected and the delayed output signal. It produces a logical "true" when an AP is detected. A logical "false" is produced in the absence of AP's.

Fig. 2 illustrates the waveforms at the various stages in the detector. In Fig. 2a we see the input signal. Fig. 2b illustrates the detection of the negative peak. The inverted and delayed version of the detected negative peak signal is shown in Fig. 2c. Inverted detection of the positive peak is shown in Fig. 2d. Detection of the AP is depicted in Fig. 2e.

To verify the performance of the dual threshold algorithm (DTA), we compare it to the NEO and adaptive threshold algorithms (ATA) as described in [5]. As test signal we use a synthetic signal made from a real waveform sampled at 30 kHz. AP shapes are extracted from the real waveform and randomly distributed according to the Poisson law with variable firing rates. Subsequently, white noise, band-limited at 7 kHz, is added to emulate various SNR's.

Fig. 3 shows the transient responses of the three algorithms. The signal of Fig. 3a has SNR of 2.9 dB and is applied to each algorithm. Fig. 3b represents the output of the NEO. The output of the ATA can be seen in Fig. 3c. Finally, in Fig. 3d, the output of the DTA, described in this paper, is depicted. We can see that false detections of the DTA are less likely to occur than in the case of the NEO and the ATA.

Fig. 4 indicates the performance of the different detectors as the SNR ratio is decreasing. At high SNR ratios, the

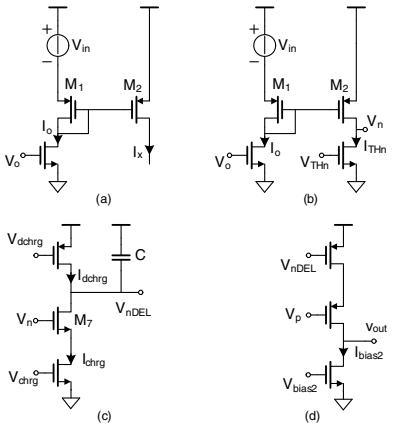

Figure 5. (a) Simple pre-processor performing mathematical exponential operation. (b) Implementation of current comparator. (c) Delay circuit. (d) NOR-gate analog implementation.

NEO shows good performance. As the SNR decreases, the performance degradation of the NEO becomes more severe than that of the other two detectors. ATA and DTA have the same performance in case of high SNR. As the SNR decreases, we can see that DTA outperforms ATA.

III. Dual Threshold Detector Building Blocks

A. Pre-processors

Fig. 5a shows the circuit implementation of the pre-processor. Using the exponential relationship of PMOSTs operating in weak inversion [16], for $V_{DS} \geq 4U_T$ (a condition to keep the devices in weak inversion saturation) and $V_{SB} = 0$ (source and body terminals are connected), it follows

$$I_D = I_{D0} \exp\left(\frac{V_{SG}}{nU_T}\right), \tag{1}$$

where

$$I_{D0} = I_S \left(\frac{W}{L}\right) \tag{2}$$

and I_S is the zero bias current for a unit transistor, n is the sub-threshold slope factor and U_T is the thermal voltage while W, L, V_{SD}, V_{SB}, and V_{SG} have their usual meaning. From Fig. 5a we can find that

$$V_{SG2} = V_{SG1} + V_{in}. \tag{3}$$

Substituting (3) into (1) we get

$$I_x = I_o \exp\left(\frac{V_{in}}{nU_T}\right), \tag{4}$$

which clearly states the exponential relation between input voltage and output current depending on bias current I_o, which is set by the voltage V_o.

B. Current comparators

Implementation of the current comparator is performed by adding a current source I_{THn}, set by V_{THn}, to the exponential pre-processor output node, as shown in Fig. 5b. In case $I_{\text{THn}} > I_x$, V_n will become 0V. Otherwise it will be V_{DD}, as illustrated in Fig. 2d.

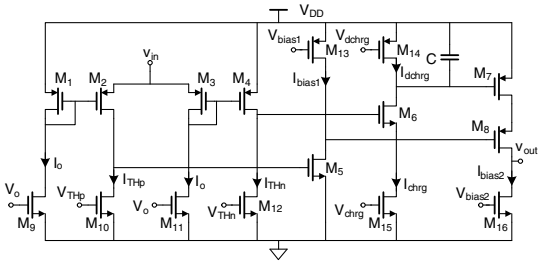

Figure 6. Dual threshold AP detector circuit.

C. Delay circuit

Fig. 5c shows the implementation of the delay circuit. Transistor M_7 acts as a switch. In case $V_n = 0$V, M_7 will be open and we have

$$I_{dchrg} = C\frac{dV_{\text{nDEL}}}{dt}. \tag{5}$$

Slightly rewriting (5), we can find the discharging slope

$$\frac{dV_{\text{nLPF}}}{dt} = \frac{I_{dchrg}}{C}. \tag{6}$$

In case $V_n = V_{DD}$, in charge mode, M_7 will be closed and we have a different situation. The charging slope is then defined as

$$\frac{dV_{\text{nLPF}}}{dt} = \frac{I_{chrg} - I_{dchrg}}{C}. \tag{7}$$

The threshold voltage of M_7 and the discharging slope determine the delay time t_d, where $I_{chrg} >> I_{dchrg}$. Voltages V_{chrg} and V_{dchrg} are setting I_{chrg} and I_{dchrg}, respectively.

D. NOR-gate

The circuit diagram of the NOR-gate is depicted in Fig. 5d. Current I_{bias2} , set by the voltage V_{bias2}, will flow only if both inputs V_p and V_{nDEL} are low. This will pull down the voltage at V_{out} and it becomes 0 V. Otherwise, current will not flow and $V_{out} = V_{DD}$. Fig. 2e illustrates the output of the NOR-gate.

The complete circuit diagram of the AP detector can be found in Fig. 6. It is a combination of the building blocks from Fig. 5. An inverter, formed by M_5 and M_{13}, is inserted for pre-conditioning of the NOR gate to achieve the desired operation from the detector.

IV. Simulation Results

The operation of the AP detector circuit was verified in Cadence using RF spectre and AMIS 0.35 μm technology (I3T80). MOS transistor widths (W) and lengths (L) were set as $W/L_{1-8} = 3\,\mu\text{m}/10\,\mu\text{m}$ and $W/L_{9-16} = 3\,\mu\text{m}/7\,\mu\text{m}$. Supply voltage $V_{DD} = 1$ V. At $37\,^{\circ}C$ the quiescent power consumption equals 1.5 nW and the average power consumption over 200 ms equals 1.8 nW. Capacitor $C = 3$ pF.

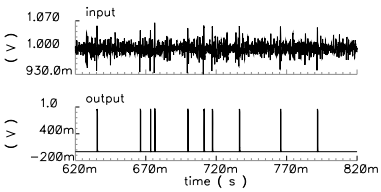

Figure 7. Transient response of the DTD in case input signal SNR of 6 is used.

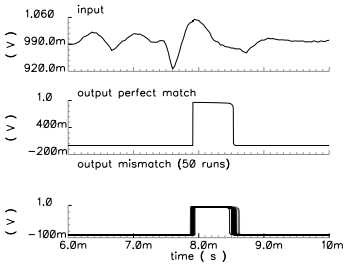

Figure 8. Monte Carlo simulation zoom in. Input signal SNR of 10.

The various current source values are given in Table 1. The threshold currents I_{THp} and I_{THn} are selected such that there is an almost equal minimum number of false positive and false negative detections over the time period of 200 ms.

Fig. 7 shows the transient response of the dual-threshold detector (DTD) circuit. It can be seen that the detector is able to successfully isolate APs from the noisy signal.

A Monte Carlo simulation of 50 runs over the period of 200 ms is performed. Zoomed-in version of a single AP detection for two different input signal-to-noise ratios (SNR) are depicted in Fig. 8 and Fig. 9. As we can see, mismatch variations have bigger influence on the circuit operation in case SNR decreases. For the input signal with SNR = 6, we can see that one false detection occurred in 50 runs.

V. Conclusions

In this paper, a dual-threshold action potential detection circuit to be used in real-time applications has been presented. The CMOS version of the resulting circuit comprises one capacitor and a handful of transistors. Simulations show that

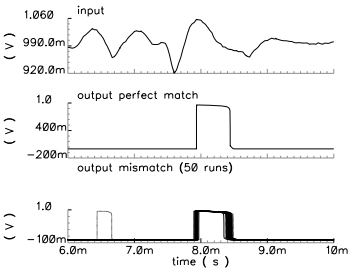

Figure 9. Monte Carlo simulation zoom in. Input signal SNR of 6.

Table I
Current sources

source	I_{o}	I_{THp}	I_{THn}	I_{bias1}	I_{bias2}	I_{chrg}	I_{dchrg}
I [nA]	0.37	0.85	0.72	0.71	0.5	103	1.9

the proposed circuit consumes very little power and is able to reliably detect the action potentials in the input signals even in case of very limited SNR. Thanks to the compact circuit architecture and the low power consumption, the proposed circuit is a good candidate for multi-electrode spike detection.

Acknowledgment

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Analog Complex Gammatone Filter for Cochlear Implant Channels

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***Abstract*— According to recent physiological experiments, the envelope and phase of speech signals are required to enhance the perceptive capability of a cochlear implant processor. In this paper, the design of an analog complex gammatone filter is introduced in order to extract both envelope and phase information of the incoming speech signals as well as to emulate the basilar membrane spectral selectivity. The gammatone impulse response is first transformed into the frequency domain and the resulting 8th-order transfer function is subsequently mapped onto a state-space description of an orthonormal ladder filter. Using this approach, the real and imaginary transfer functions that share the same denominator can be extracted using two different C matrices. This results in a compact filter structure. The proposed filter is designed using G_m-C integrators and sub-threshold CMOS devices in AMIS 0.35μm technology. Simulation results using Cadence RF Spectre confirm the design principle and ultra low power operation.**

I. INTRODUCTION

Cochlear Implants (CI) are prosthetic devices that restore hearing function in profoundly deaf patients by bypassing damaged parts of the inner ear and directly stimulating the remaining auditory nerve fibers in the cochlea with electrical pulses. To do so, the CI contains a speech processor that plays an important role in converting the original speech signal into electrical stimuli. Traditionally, the processor decomposes the frequency band of the incoming speech into several sub-bands and extracts the envelope of each sub-band for generating amplitude modulated pulses to stimulate the nerve fibers [1].

To realize the spectral analysis in an analog speech processor, band-pass filter designs based on 2nd order filters in the form of log-domain [2-3] and G_m-C [4] filters using CMOS circuits operating in weak inversion have been reported. These filter circuits are successful in terms of power consumption but lack operation that is analogous to a real cochlea. Besides, in conventional speech processors [2-4], the envelopes are extracted by a full-wave rectifier and a low-pass filter that may provide compact hardware implementation, yet their high frequency information is corrupted [5-6].

It was found in [7] that, observing a cochlear nucleus after electrical stimulation, a gammatone function could closely describe the resulting cochlear impulse responses. As a consequence, the gammatone filter has been popularly used in cochlear modeling [8] and speech recognition [9]. Also it has been suggested in [5-6] that, in order to preserve the high frequency information of speech signals, the Hilbert transform should be employed instead of the simple rectifier combined with the low-pass filter.

Recently, partially driven by the motivation mentioned above, a realization of a gammatone filter has been introduced [10]. The design is based on a class-AB log domain circuit using signal splitting and cascaded class-A biquad sections. The filter successfully emulates the pseudo-resonance behavior of the basilar membranes and provides a very high dynamic range of 120dB. This paves the way for high performance bio-inspired analog filter design for new generations of cochlear implants.

In order to develop further, this paper creates a bio-realism of the cochlear channels by combining the gammatone impulse response with the Hilbert transform within a compact frequency selective circuit. The design methodology starts with Laplace transforming the gammatone function into two band-pass transfer functions which represent the real and imaginary signal of the complex gammatone filter. To synthesize the filter, the transfer functions are mapped onto an orthonormal ladder structure which provides good dynamic range, minimum sensitivity to component variations and high sparsity [11]. A sub-threshold G_m-C filter is selected to realize the filter in order to verify the feasibility of the complex gammatone filter at very low power operation.

II. SPECTRAL ANALYSIS IN COCHLEAR IMPLANTS

A. Temporal Envelope and Fine Structure

Applying the Hilbert transform to an incoming speech signal, which is considered a real signal, $x_{re}(t)$, results in an imaginary signal $x_{im}(t)$ which can be combined to create the analytic signal

$$s(t) = x_{re}(t) + jx_{im}(t). \quad (1)$$

In the psychoacoustic literature [5], temporal envelope and fine structure (phase information) are respectively defined by

$$a(t) = \sqrt{x_{re}^2(t) + x_{im}^2(t)}, \quad (2)$$

and $\cos(\phi(t))$, where

$$\phi(t) = \tan^{-1}\left(\frac{x_{im}(t)}{x_{re}(t)}\right) \quad (3)$$

is the phase of the analytic signal. The temporal fine structure is critical for speech recognition in background noise and music perception. In [12], it has also been recognized that the temporal fine structure is more important for pitch recognition than the temporal envelope.

B. The Gammatone Auditory Filter Bank

The gammatone filter function describes the impulse responses of the mammalian cochlea and is defined by

$$g(t) = at^{(n-1)}e^{(-2\pi bt)}\cos(2\pi f_c t + \phi)\ ;\ (t > 0). \qquad (4)$$

The parameter n is the order of the filter, b is the bandwidth of the filter, f_c is the centre frequency of the filter, a is a constant and ϕ is the starting phase.

In the case of n = 4 and b is 1.019 times the Equivalent Rectangular Bandwidth (*ERB*), (4) can represent the human auditory filter [13]. The *ERB* is a psychoacoustic measure of the width of the auditory filter at each point along the cochlea. In [14], human data on the *ERB* of the auditory filter has been summarized and can be approximated as

$$ERB = 24.7(4.37 f_c/1000 + 1). \qquad (5)$$

Together, (4) and (5) define the gammatone auditory filter bank. An example of the centre frequencies of 16 cochlear channels and their *ERB* is shown in table I.

III. TRANSFORMATION OF GAMMATONE FILTER

A. Laplace Transform of Complex Gammatone Filter

For convenience, we set a=1 and ϕ=0. Then (4) can be modified for a complex tone as

$$g_c(t) = t^3 e^{-2\pi bt}\cdot e^{j\omega t}$$

$$= t^3 e^{-2\pi bt}\cos(\omega t) + jt^3 e^{(-2\pi bt)}\sin(\omega t). \qquad (6)$$

Converting (6) into the frequency domain using the Laplace transform properties, we obtain

$$G_{re}(s) = \frac{N_{re}(s)}{D(s)} = -\frac{d^3\left(\dfrac{s+B}{(s+B)^2+\omega^2}\right)}{ds} \qquad (7)$$

and

$$G_{im}(s) = \frac{N_{im}(s)}{D(s)} = -\frac{d^3\left(\dfrac{B}{(s+B)^2+\omega^2}\right)}{ds}, \qquad (8)$$

where $B = 2\pi b$ and $\omega = 2\pi f_c$. $G_{re}(s)$ and $G_{im}(s)$ are the transfer functions of the real and imaginary signals, respectively. Note that the denominators of both transfer functions are the same, facilitating a compact hardware implementation which will be illustrated shortly.

To exemplify the case of a centre frequency of 1 kHz and an *ERB* of 132.64 Hz, we have

$$N_{re}(s) = -1.022\times10^{12}s^4 - 3.473\times10^{15}s^3 + 2.377\times10^{20}s^2\cdots$$
$$+4.088\times10^{23}s - 1.769\times10^{27} \qquad (9)$$

$$N_{im}(s) = -2.638\times10^{16}s^3 - 6.721\times10^{19}s^2 + 9.844\times10^{23}s\cdots$$
$$+8.683\times10^{26} \qquad (10)$$

$$D(s) = s^8 + 6794s^7 + 1.781s^6 + 8.389\times10^{11}s^5 + 1.11\times10^{16}s^4\cdots$$
$$+3.372\times10^{19}s^3 + 2.878\times10^{23}s^2 + 4.413\times10^{26}s\cdots$$
$$+2.611\times10^{30} \qquad (11)$$

B. Orthonormal State Space Representation

In order to implement the complex gammatone filter, both real and imaginary transfer functions are mapped onto a state space orthonormal ladder structure. A detailed explanation of the procedure to derive the orthonormal ladder form can be found in [11, 15-16]. The state space description as **A**, **B** and **C** matrices of the example transfer function are given by

$$\mathbf{A} = \begin{bmatrix} 0 & 6201 & 0 & 0 & 0 & 0 & 0 & 0 \\ -6201 & 0 & 778.5 & 0 & 0 & 0 & 0 & 0 \\ 0 & -778.5 & 0 & 6093 & 0 & 0 & 0 & 0 \\ 0 & 0 & -6093 & 0 & 1608 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1608 & 0 & 5788 & 0 & 0 \\ 0 & 0 & 0 & 0 & -5788 & 0 & 3350 & 0 \\ 0 & 0 & 0 & 0 & 0 & -3350 & 0 & 7391 \\ 0 & 0 & 0 & 0 & 0 & 0 & -7391 & -6794 \end{bmatrix}, \qquad (12)$$

$$\mathbf{C_{re}} = [-39.48 \quad 10.71 \quad 4.833 \quad -0.324 \quad -0.1534 \quad 0 \quad 0 \quad 0], \qquad (13)$$

$$\mathbf{C_{im}} = [10.95 \quad 39.63 \quad -1.029 \quad -2.461 \quad 0 \quad 0 \quad 0 \quad 0], \qquad (14)$$

and

$$\mathbf{B^T} = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 46.5]. \qquad (15)$$

The **A** matrix determines the centre frequency of the filter, the **B** matrix scales the input signal and the real and imaginary **C** matrices contain the coefficients required to form the real and imaginary outputs of the filter.

IV. CIRCUIT IMPLEMENTATION

Fig. 1 shows the topology of the complex gammatone filter corresponding to the above state-space representation. The frequency responses (only for the real output) of a 16 channels gammatone filter according to the parameters in table I are shown in Fig. 2.

TABLE I. *ERB* AND CENTRE FREQUENCY OF 16 COCHLEA CHANNELS

Channels	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ERB(Hz)	40.89	50.55	62.48	77.23	95.46	118.00	145.86	180.30	222.87	275.49	340.53	420.93	520.31	643.16	795.01	982.71
f_c (Hz)	150.0	239.4	350.0	486.7	655.6	864.4	1122.5	1441.6	1835.9	2323.4	2926.0	3670.9	4591.6	5729.7	7136.5	8875.5

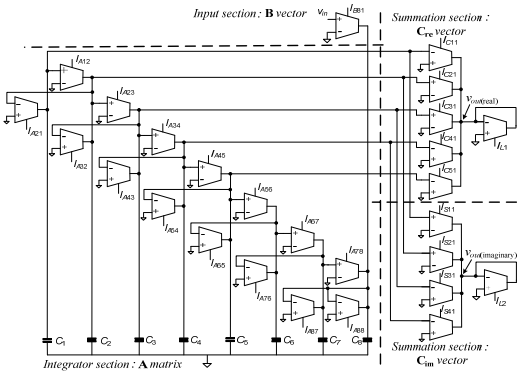

Figure 1. Circuit of the complex gammatone

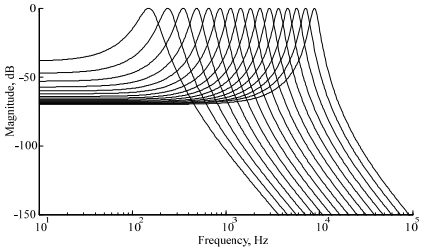

Figure 2. Frequency responses of 16 real gammatone filter channels

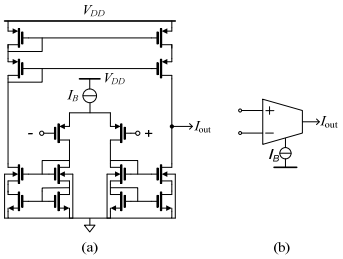

Figure 3. Subthreshold *Tanh* transconductor (a) circuit (b) symbol

The circuit design of the filter is based on the G_m-C integrator approach using identical simple sub-threshold differential transconductors, shown in Fig. 3, as main building blocks. The voltage to current relationship of the transconductor is given by

$$I_{out} = I_B \tanh \frac{V_d}{2nU_T}, \qquad (16)$$

where n and U_T are the sub-threshold slope factor and thermal voltage, respectively [17]. The small signal transconductance, $g_m = I_B / 2nU_T$ can be found from the first term of the Taylor series expansion of (16). The integrator time constants in the **A** matrix are defined by ($\tau = C / g_m$) where C=C_i= 20pF. The bias current of each transconductor is set according to the coefficients in the matrices. The centre frequency and the gain of the filter can be varied by scaling the bias currents of the transconductors of matrices **A** and **B** and **C**, respectively.

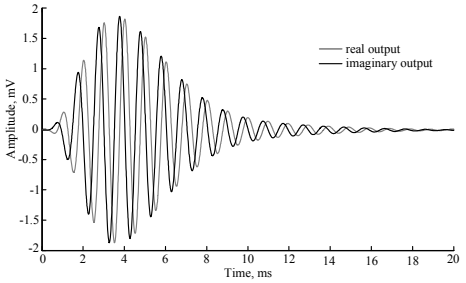

Figure 4. Simulated impulse response at f_c=1kHz

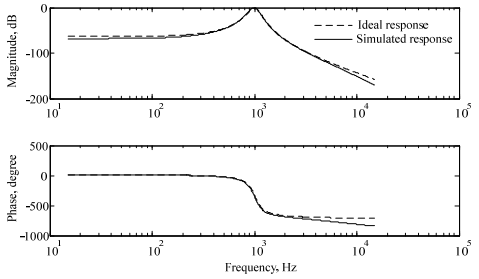

Figure 5. Frequency responses of the real output at f_c=1 kHz

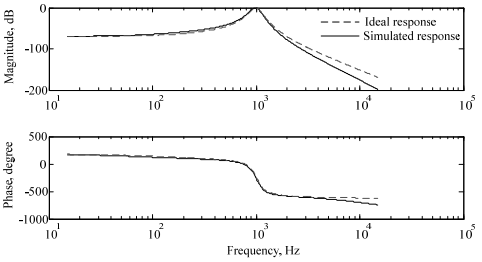

Figure 6. Frequency responses of the imaginary output at f_c=1 kHz

V. SIMULATION RESULTS

The concept of the complex gammatone filter was verified in Cadence using RF spectre and AMIS 0.35μm technology. The dimensions equal W/L=6μm/6μm and 6μm/2μm for the PMOS differential pair and all transistors in the cascoded current mirrors, respectively. Supply voltage V_{DD} = 2V and the common mode voltage reference was set at the mid supply. The quiescent power consumption equals 4.71μW.

Fig. 4 shows the impulse response of the filter at 1 kHz centre frequency by applying a positive pulse signal, with an amplitude of 10 mV and a pulse width equal to 100μs. The common mode signal has been removed for clarity.

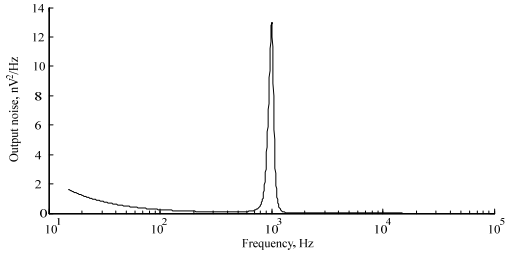

Figure 7. The output noise (PSD)

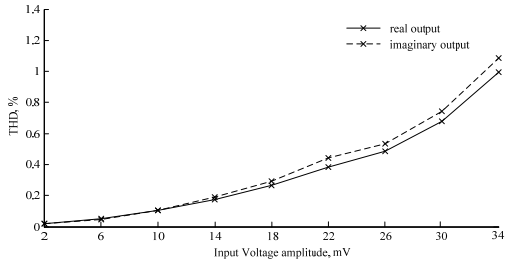

Figure 8. Total harmonic distortion of the proposed filter

The frequency responses of the filter are shown in Fig. 5 and 6 for the real and imaginary outputs, respectively. It is clear that, in the pass-band, the results are close to the ideal case. Fortunately, errors induced from non-idealities of the transconductor occurred mainly in the stop-bands and do not harm the filter's functionality.

The integrated output noise power over the range from 15 Hz to 15 kHz is $2\mu V^2$ and the noise power spectral density (PSD) is shown in Fig. 7. The total harmonic distortion (THD) of the real and imaginary outputs when sinusoidal inputs ranging from 2mV to 34mV are applied at the centre frequency are shown in Fig. 8.

VI. CONCLUSIONS

The theory and design of a complex gammatone filter for cochlear implant channels has been proposed in this paper. The key features for speech intelligibility including temporal envelope and the phase information can be extracted from a compact G_m-C poly-phase band-pass filter circuit. This work is considered to be useful for developing the next generation of cochlear implants.

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PUBLICATIONS AND PRESENTATIONS

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Wannaya Ngamkham, Chutham Sawigun, **Senad Hiseni** and Wouter A. Serdijn, "Analog Complex Gammatone Filter for Cochlear Implant Channels," *Circuits and Systems, 2010. ISCAS 2010. IEEE International Symposium on, 2010.* accepted

Senad Hiseni, Chutham Sawigun, Wannaya Ngamkham, and Wouter A. Serdijn, "A Compact, Nano-Power CMOS Action Potential Detector," *Biomedical Circuits and Systems Conference, 2009. BioCAS 2009. IEEE*, pp. 97-100, November 2009.

Senad Hiseni, Chutham Sawigun, and Wouter A. Serdijn, "Dynamic translinear nonlinear energy operator," *Circuit Theory and Design, 2009. ECCTD 2009. European Conference on*, pp. 153-156, August 2009.

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"Dynamic translinear nonlinear energy operator," *TU Delft course ET4252: Analog Integrated Circuit Design*, Delft University of Technology, Delft, the Netherlands, December 2, 2009.

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