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PV to Virtual Bus Parallel Differential Power Processing Architecture for Photovoltaic Systems

Afshin Nazer, Olindo Isabella, and Patrizio Manganiello

***Abstract*—This article introduces an innovative parallel differential power processing (PDPP) architecture designed to mitigate the effect of mismatch among photovoltaic (PV) strings. The proposed PV to virtual bus PDPP architecture leverages a virtual bus as the input for all string-level converters. Notably, this approach allows for a reduction in the voltage rating of components since the virtual bus voltage can be set lower than the main bus or PV strings voltage. In this architecture, crucial requirements for the string-level converters (SLCs) include the capability to generate positive and negative output voltages and to provide isolation. To fulfill these requirements, a dual active bridge converter connected to a bridgeless converter as the PDPP SLCs is considered. In this architecture, while SLCs ensure maximum power point tracking (MPPT) for each PV string using conventional MPPT algorithms, the central converter controls the virtual bus voltage. Experimental results validate the performance of the proposed PV to virtual bus PDPP architecture with a system efficiency ranging from 96.4% to 99%.**

***Index Terms*—Differential power processing (DPP), maximum power point tracking (MPPT), photovoltaic (PV) system, photovoltatronics.**

I. Introduction

PHOTOVOLTAIC (PV) systems, developed over half a century, offer a compelling solution to rising electricity demand. They are favored for their access to free solar energy, eco-friendly operation, longevity of over 25 years, easy installation, low maintenance, and suitability for remote areas [1], [2], [3]. The early approach to connecting PV arrays to the grid was the centralized architecture where PV modules are connected in series to form PV strings; then, PV strings are connected in parallel at the input of a central inverter, as shown in Fig. 1(a). While cost-effective and simple, they suffer from demerits such as high-voltage DC cables, diode losses, limited serviceability, and scalability concerns [4], [5]. Additionally, mismatches caused by shading, different tilt angles, dust, degradation, light variations among PV modules, a short-circuited PV module, and so on, reduce system efficiency [6], [7].

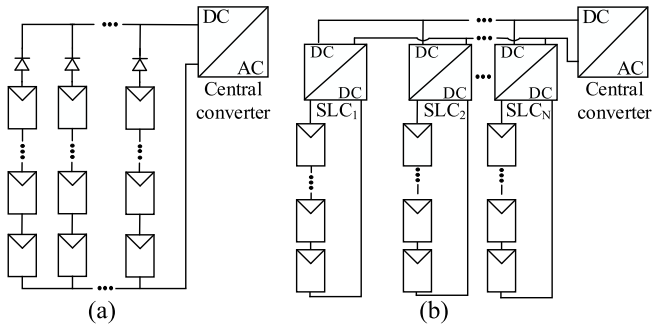

Fig. 1. PV system using. (a) Centralized. (b) Multistring architectures.

To mitigate mismatch losses and optimize energy yield various distributed maximum power point tracking (DMPPT) architectures have been developed, offering solutions at different levels of granularity. These range from multistring inverters [1], which track the maximum power point (MPP) of PV strings individually [Fig. 1(b)], to PV optimizers or microinverters, which perform MPPT at the module level [7], [8], [9], [10], [11], [12], [13], [14]. DMPPT architectures can generally be divided into full power processing (FPP) and differential power processing (DPP) categories. Although FPP architectures, such as multistring architectures [Fig. 1(b)], are mature, proven, and consolidated technologies with a wide variety of power converters already available in the industry, they process all the power generated by the PV strings. Besides, the voltage and current rating for the converters' components used in these FPP architectures are determined by the voltage and current of the PV strings/modules, which deteriorates power conversion efficiency, size, reliability, and cost [6], [15]. To solve these problems, differential power processing (DPP) [7], [10], [11], [12], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25] has been introduced. DPP architectures provide the advantage of processing only a portion of the power generated by PV modules, allowing the majority of power to be directly delivered to the output. This offers two key advantages: 1) it reduces operational time and increases system efficiency, even if DPP converters' efficiency is lower than that of FPP, 2) it alleviates stress on components, resulting in

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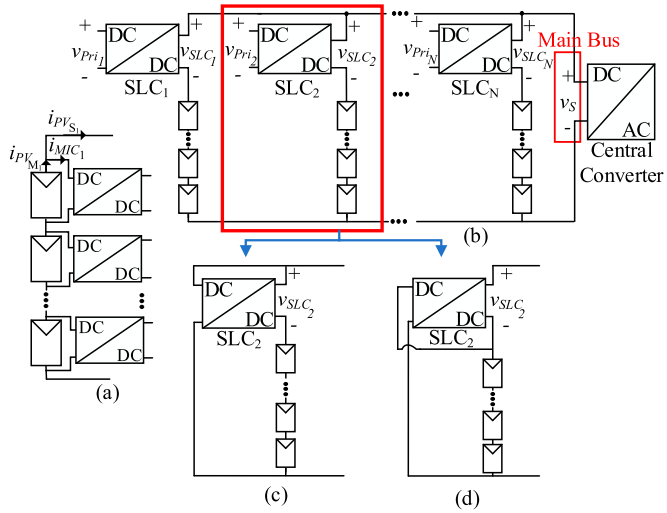

Fig. 2. PV system using. (a) General SDPP architecture. (b) General PDPP architecture with primary side connection. (c) Main bus (PV2B-I PDPP architecture). (d) PV string (PV2B-II PDPP architecture).

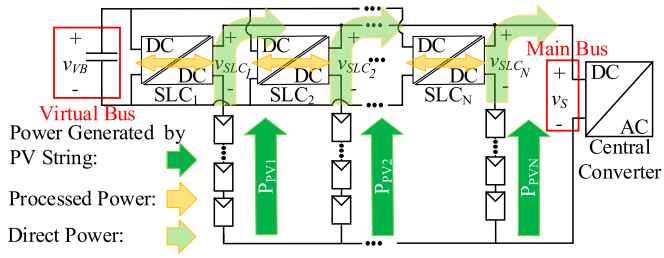

Fig. 3. PV systems using the proposed PV2VB PDPP architecture.

improved reliability and lifespan [10], [26]. DPP architectures typically fall into two categories: series DPP (SDPP) [7], [10], [11], [12], [13], [14] and parallel DPP (PDPP) [16], [17], [18], [19], [20], [21], [22], [23], [24], [25].

As shown in Fig. 2(a), SDPP architectures regulate the differential current between individual PV modules ($i_{PV_{M_j}}$) and the PV string current ($i_{PV_{S_j}}$), effectively mitigating mismatch-related losses within series-connected PV elements. Yet, they are insufficient in addressing mismatch losses among parallel-connected PV strings [27], [28]. Thus, the concept of PDPP has emerged [Fig. 2(b)] [16], [17], [18], [19], [20], [21], [22], [23], [24], [25]. PDPP architectures compensate for the differential voltage between PV strings and a main bus, eliminating mismatch losses among parallel PV strings. Despite all the current from the j^{th} PV string flowing through the respective string level converters (SLC), the voltage across the j^{th} SLC (v_{SLC_j}) may be lower than the PV string voltage. This suggests that the power handled by the SLCs may be less than that of conventional FPP multi-string architecture, allowing for potential reduction in converter rating and conversion losses.

PDPP architectures are categorized based on the connection of the primary side of the SLCs. Typically, PV to bus (PV2B) architectures are analyzed and reported, which are further classified into PV2B-I [17], [18], [19], [20], [21] and PV2B-II [22], [23], [24], [25]. In PV2B-I, the primary side of the SLCs is connected to the main bus [Fig. 2(c)], while in PV2B-II, the primary side of the SLCs is connected to the PV strings [Fig. 2(d)]. The most suitable architecture for a given application is the one leading to the lowest maximum power processing [29]. In [22], a buck-boost converter has been selected as the SLC for the PV2B-II architecture. While the SLCs compensate for the differential voltage between the PV strings and the main bus, they also have to handle the full current generated by the PV strings. Additionally, the components must withstand the PV string voltage, resulting in SLCs with power ratings equivalent to those of FPP converters. In [17], [21], [23], a flyback converter is utilized in both PV2B-I and PV2B-II architectures. Flyback converters are advantageous due to their simplicity, but their application is generally limited to power outputs of a few hundred watts. Consequently, other studies [18], [19], [20], [23], [24], [25] have employed different topologies to increase power handling capability, albeit at the cost of simplicity.

Although high efficiency has been reported for PV2B architectures, directly connecting SLCs to the main bus or PV strings presents three main disadvantages. First, the voltage rating of SLCs is determined by the PV strings or main bus voltage. Second, the scalability of the PV system is limited: adding PV modules to a PV string increases the string's voltage, necessitating SLCs with higher voltage ratings. These first two issues also exist in FPP SLCs. Lastly, PV2B PDPP requires SLCs with high-voltage conversion ratio (v_{SLC}/v_S). To address the challenges of both PV2B PDPP and conventional FPP architectures, we have proposed a novel PV2VB PDPP architecture [16]. This article provides a comprehensive analysis and presents experimental validations to demonstrate the performance of the architecture proposed [16].

As shown in Fig. 3, PV2VB PDPP is a novel architecture where SLCs inputs are connected to a common isolated DC bus called the virtual bus instead of the main bus. One key advantage is the flexibility to select a lower voltage for the virtual bus compared to the main bus, leading to a potential reduction in initial and repair cost of SLCs. Additionally, the use of low-blocking voltage semiconductors in the PV2VB architecture enables the use of MOSFETs instead of IGBTs, enabling higher switching frequencies, reducing the size of passive components and improving the converter's power density. Moreover, there will be less challenge in designing EMI/EMC filters for low-voltage converters which simplifies compliance with electromagnetic compatibility standards [30], [31]. Besides, this architecture can mitigate the high voltage conversion ratio required for SLCs in PV2B architectures.

This innovative architecture also offers superior scalability compared to conventional counterparts. In the proposed PV2VB architecture, the SLC input voltage corresponds to virtual bus voltage not the PV string nor main bus voltage. Therefore, the proposed architecture offers flexibility to incorporate new PV modules into strings, making it a more adaptable and versatile solution. This scalability enables its use for a wide range of PV string lengths, facilitating mass production and lowering manufacturing costs. A comparison between PV2B and proposed PV2VB PDPP architectures is presented in Table I.

TABLE I
COMPARISON OF PDPP ARCHITECTURES

Feature / Ref.	Architecture	SLCs Topology	Bidirectional SLCs	Isolated SLCs	CVR	Scalability	VCR	Power Level	Reported Efficiency (%)
[17]	PV2B-I	Flyback	No	Yes	High/low	Low	High	50 W	89-97
[18]	PV2B-I	Series resonant converter	No	Yes	High/low	Medium	Medium	4 kW	97.75-98.82
[19]	PV2B-I	Current fed resonant push-pull	Yes	Yes	High/low	Low	High	2.2 kW	97.8-98.8
[20]	PV2B-I	Current-fed full-bridge	Yes	Yes	High/low	Low	High	2.2 kW	95.5-98.2
[21]	PV2B-I	Flyback	No	Yes	High/low	Low	High	25 W	98.5
[22]	PV2B-II	Buck-boost	No	No	High	Low	High	3.5 kW	96-98.9
[23]	PV2B-II	Flyback	No	Yes	High/low	Low	High	100 W	70-90
[24]	PV2B-II	Full-bridge	No	Yes	High/low	Low	High	821 W	98-99
[25]	PV2B-II	Full-bridge/Push-pull	Yes	Yes	High/low	Low	High	750 W	98.6-99.58
	PV2B-II	Full-bridge	No	Yes	High/low	Low	High	750 W	98.8
Proposed	PV2VB	DAB/BL	Yes	Yes	Low	High	Low	4 kW	96.4-99

CVR: Components' voltage rating; VCR: voltage conversion ratio; High/low: There exist components with high and low voltage ratings.

The proposed architecture performs string-level maximum power point tracking (MPPT) while processing only a fraction of the power generated by PV strings. The power processed by the SLCs varies based on environmental conditions, PV module specifications, string length, and the number of PV strings in operation. To address this variability, this article introduces a power flow analysis method. This method simplifies determining SLC power processing under different scenarios with multiple PV strings and helps identify the required power rating for SLCs under predefined environmental conditions or worst-case shading scenarios.

The remainder of this article is structured as follows: Section II provides an in-depth analysis of the steady-state operation of both the central converter and SLCs and elucidates their respective control objectives. In Section III, the article derives the equations governing the processed power to determine SLCs rating and to compare it with that of the conventional FPP architectures. Section IV describes the different operational regions of the PV2VB PDPP architecture, and Section V presents experimental results that validate the architecture's capability for string-level MPPT, substantiating its inherent advantages. Finally, Section VI concludes this manuscript.

II. OVERVIEW OF THE PV2VB PDPP ARCHITECTURE

As shown in Fig. 3, in the proposed PV2VB PDPP architecture, SLCs inputs are connected to a shared, isolated DC bus called the virtual bus. To ensure smooth and stable operation, maintaining a power balance within the virtual bus is essential to prevent fluctuations in its voltage. Thus, while certain PV strings inject energy into the virtual bus through the SLCs, others must draw energy from it. This architecture has two primary objectives: (i) maintaining the virtual bus voltage at a constant level, a task overseen by the central converter, and (ii) independently tracking the MPP of each PV strings, a responsibility entrusted to the SLCs. The subsequent sections will provide an in-depth description of the converters and their respective control principles.

A. Central Converter

In a PV2VB PDPP architecture, the central converter regulates the main bus voltage (v_S) by its duty cycle. However, this control action is aimed at ensuring the stability of the virtual bus voltage (v_{VB}). This subsection delves into understanding the relationship between the main bus and virtual bus voltage. Two assumptions are considered for the sake of simplicity: 1) lossless converters, and 2) the capacitive virtual bus is the main storage element in the system. Then, the power relationship for the PV2VB architecture can be derived as follows:

$$p_{VB} = p_{\text{out}} - p_{\text{in}}. \tag{1}$$

In the context of the proposed architecture, p_{VB}, p_{out}, and p_{in} represent the instantaneous virtual bus power, power delivered to the main bus, and power generated by the PV strings, respectively; these values can be computed as follows:

$$p_{VB} = C_{VB} \times v_{VB} \times \frac{dv_{VB}}{dt} \tag{2}$$

$$p_{\text{out}} = v_S \times i_S = v_S \times \sum_{j=1}^{N_{PV}} i_{PV_j} \tag{3}$$

$$p_{\text{in}} = \sum_{j=1}^{N_{PV}} v_{PV_j} \times i_{PV_j} \tag{4}$$

where C_{VB}, i_S, v_{PV_j}, i_{PV_j}, and N_{PV} are the virtual bus capacitance, main bus current, j^{th} PV string's current, j^{th} PV string's voltage, and number of PV strings, respectively; the following equation can be obtained by substituting (2)–(4) in (1)

$$p_{VB} = \frac{dv_{VB}}{dt} \times C_{VB} \times v_{VB} = \sum_{j=1}^{N_{PV}} v_{PV_j} \times i_{PV_j} - v_S \times i_S. \tag{5}$$

While it may appear that there are numerous actuators to regulate virtual bus power, it is important to note that PV strings' current and voltages are controlled by SLCs to make PV strings operate at their MPPs. Besides, the main bus current is inherently equal to the summation of the individual PV strings'

currents. Thus, the sole variable available for controlling virtual bus power and, consequently, virtual bus voltage is the main bus voltage. When the average power of the virtual bus is maintained at zero, the following equation is derived:

$$P_{VB} = 0 \rightarrow V_S^* = \frac{\sum_{j=1}^{N_{PV}} V_{PV_j} \times I_{PV_j}}{\sum_{j=1}^{N} I_{PV_j}}, \quad V_{VB} = \text{const} \tag{6}$$

where V_S^* is the equilibrium main bus voltage at which the virtual bus voltage is constant. It should be noted that capital letters indicate steady-state value of the variables. Combining (5) and (6), the following equation, which describes the instantaneous rate of change of virtual bus voltage as a function of bus voltage can be derived

$$\frac{dv_{VB}}{dt} = \frac{\sum_{j=1}^{N_{PV}} V_{PV_j} \times I_{PV_j}}{C_{VB} \times v_{VB}} \times \left(1 - \frac{v_S}{V_S^*}\right). \tag{7}$$

Equation (7) shows the virtual bus voltage rises when the main bus voltage drops below the equilibrium level, and vice versa.

Realizing this control mechanism and ensuring the effective integration of it with MPPT algorithms in the architecture necessitates a careful approach. To prevent interference between the controller and to enable the MPPT algorithms to autonomously seek the MPP of the PV string, it is recommended to implement a discrete controller whose sampling time exceeds the perturbation period of the MPPT algorithms. This design consideration ensures that the MPPT algorithms have the required independency for their operation, unburdened by premature or conflicting control actions from the central controller. Such harmony is needed for maintaining precise MPP tracking and overall PV system performance.

B. SLCs

In the PV2VB PDPP architecture, the primary goal of SLCs is to ensure that PV strings operate at their MPP. To accomplish this, SLCs must also establish a path for the efficient transfer of power to and from the virtual bus. It is possible to apply a variety of topologies as the SLCs as long as they exhibit three crucial features. First, they must operate effectively within both the first and fourth quadrants of the voltage-current (V-I) curve. To elaborate further, the output voltage of the j^{th} SLCs can be expressed as

$$v_{\text{SLC}_j} = v_S - v_{PV_j}. \tag{8}$$

By substituting (8) into (5), in steady state we have

$$P_{VB} = \sum_{j=1}^{N_{PV}} V_{\text{SLC}_j} \times I_{PV_j} = \sum_{j=1}^{N_{PV}} P_{\text{SLC}_j} = 0. \tag{9}$$

Which means that the total output power of all SLCs sums to zero, indicating that SLCs solely facilitate power exchange among themselves. Furthermore, given that I_{PV_j} is consistently positive, (9) shows that some SLCs must produce negative output voltage while others must generate positive output voltage to maintain a constant virtual bus voltage during steady-state operation. Second, to fulfil the requirements of the architecture, SLCs must function as voltage-source converters to enable their connection to the virtual bus. Eventually, isolation is imperative

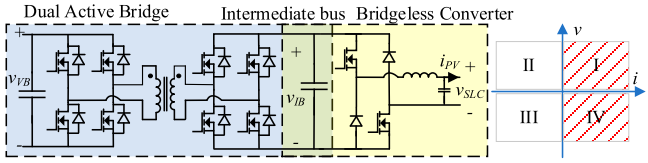

Fig. 4. Proposed SLCs topology for PV2VB PDPP architecture: A DAB converter followed by a BL converter.

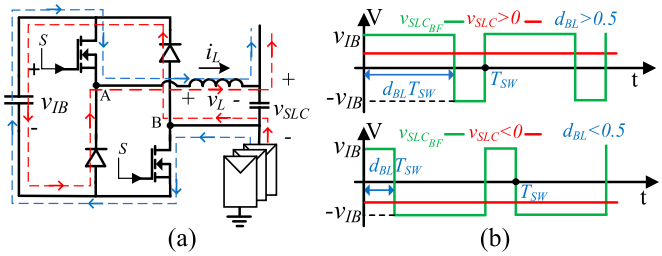

Fig. 5. Operation of the BL converter. (a) Topology. Blue dashed line: operation during on-state, red dashed line: operation during off-state. (b) Its waveforms. The voltage difference between points A and B is the voltage of BL converters before LC Filter ($v_{\text{SLC}_{BF_j}}$).

to enable independent control of PV strings' voltage and to that ensure the current from the j^{th} PV string exclusively flows through the j^{th} SLC [16].

In [16], a bidirectional flyback converter followed by a bridgeless (BL) converter was proposed and simulated. While bidirectional flyback converters are well-suited owing to their attributes such as simplicity and galvanic isolation, their use is typically limited to power outputs up to a few hundred watts. Beyond this power level, it is advisable to explore alternative topologies better suited for higher power applications [32]. This study replaces bidirectional flyback with dual active bridge (DAB) converters as the first stage of the SLCs due to their suitability for high-power applications, while the second stage remains unchanged (Fig. 4).

As depicted in Fig. 4, the proposed topology for the SLCs comprises two stages: a DAB converter followed by a BL converter whose performance is decoupled by intermediate bus capacitors. The second stage of the SLC topology is the BL converter, providing both negative and positive output voltage essential for PV strings to operate at their MPP, as well as a current path for the PV string current (Fig. 5). Switches are controlled using conventional carrier frequency pulse width modulation, and the duty cycle of the BL converter in the j^{th} SLC $\left(d_{BL_j}\right)$ is determined by the MPPT algorithm. As shown in Fig. 5, during the ON state of the switches, the voltage polarity before the j^{th} LC output filter $\left(v_{\text{SLC}_{BF_j}}\right)$, aligns with the j^{th} intermediate bus voltage $\left(v_{IB_j}\right)$, leading to the intermediate bus capacitor discharge with power equal to

$$p_{C_{IB_{j1}}} = v_{IB_j} \times i_{PV_j}. \tag{10}$$

Conversely, when the switches are OFF, the BL converter inverts the intermediate bus voltage, and the capacitor is charged

$$p_{C_{IB_{j2}}} = v_{IB_j} \times \left(-i_{PV_j}\right). \tag{11}$$

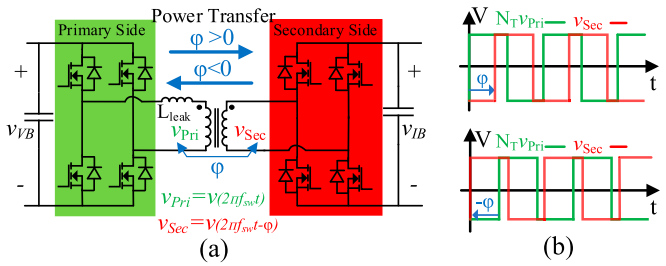

Fig. 6. DAB converter operation. (a) Topology. (b) Its waveforms.

Considering (10) and (11), the average power over a switching period (T_{sw}) of intermediate bus capacitor the BL converter will be

$$P_{C_{IB_j}} = \frac{1}{T_{sw}}\int_0^{d_{BL_j}\times T_{sw}} p_{C_{IB_{j1}}} + \frac{1}{T_{sw}}\int_{d_{BL_j}\times T_{sw}}^{(1-d_{BL_j})\times T_{sw}} p_{C_{IB_{j2}}} = \left(2d_{BL_j}-1\right)\times V_{IB_j}\times I_{PV_j} = V_{SLC_j}\times I_{PV_j} \quad (12)$$

where $P_{C_{IB_j}}$ is the power transferred from/to intermediate bus to/from the string. To make the average power flow from the virtual bus to the string, which corresponds to adding a positive voltage to the PV string, it is essential to maintain a duty cycle greater than 0.5 in the BL converter. When the duty cycle falls below this threshold, the direction of average power flow reverses, moving from the PV string back to the virtual bus, and a negative voltage is added to the PV string.

To ensure the stability of the intermediate bus voltage (v_{IB}), DAB converters facilitate the transfer of power between the virtual bus and an intermediate bus, primary and secondary sides, respectively. While various modulation techniques are available for DAB converters, this study employs single phase shift (SPS) modulation [33]. In SPS modulation, all switches operate at a constant frequency with a duty cycle of 50%, and the diagonal switches switch ON and OFF in unison, resulting in a square wave output. The power transfer is controlled by adjusting the phase shift (φ) between two ac voltage waveforms across the windings of the isolation transformer. The relationship between the phase shift (φ) and the DAB average output power (P_{DAB}) is expressed as follows:

$$P_{DAB} = \frac{V_{VB}\times V_{IB}\times \varphi\times(\pi-\varphi)}{N_T \times f_{sw} \times L_{leak}} \quad (13)$$

where N_T, f_{sw}, L_{leak} are the DAB transformer ratio, switching frequency, and leakage inductance, respectively. A controller such as proportional-integral (PI) controller receives the error value of the intermediate capacitor voltage and adjusts the phase shift accordingly to ensure that the necessary power for the BL stage the variable P_{BL_j} (as written in equation 14) is supplied

$$P_{DAB_j} = P_{BL_j} = P_{C_{IB_j}}. \quad (14)$$

To transfer the energy from the virtual bus to the intermediate bus, DAB converter primary side leads its secondary side ($\varphi > 0$). If the energy transfer direction is reversed, the primary side bridge lags behind the secondary ($\varphi < 0$) (Fig. 6). In other words, power flows from the leading to the lagging bridge.

III. Processed Power and Converters Rating

The power processed by converters represents a crucial parameter with implications for systems' efficiency, availability, and cost. In a PV systems based on PDPP architectures, part of the power generated by the PV strings is processed by the SLCs, which determines the power, voltage, and current rating of these converters.

A. DAB Converters Processed Power

In the PV2VB architecture, the primary objective of DAB converters is to maintain a constant voltage across the intermediate bus through controlled power exchange. This critical function ensures stability within the system. The power transferred between the virtual bus and j^{th} intermediate bus results in the processed power by the associated DAB converter, which considering (14), it is equal to

$$P_{DAB_j} = P_{BL_j} = V_{SLC_j}\times I_{PV_j} = \left(V_S - V_{PV_j}\right)\times I_{PV_j} \quad (15)$$

by considering (6) in the steady-state condition ($P_{VB}=0$) and substituting it into (15), we have

$$P_{DAB_j} = \left(\frac{\sum_{j=1}^{N_{PV}} V_{PV_j}\times I_{PV_j}}{\sum_{j=1}^{N_{PV}} I_{PV_j}} - V_{PV_j}\right)\times I_{PV_j}. \quad (16)$$

As shown by (16), the processed power of the j^{th} DAB is not exclusively dependent on the current and voltage of its own PV string, but also depends on the current and voltage of other PV strings. In a PV system consisting of N_{PV} PV strings, let k of these PV strings be shaded, producing voltage and currents of

$$I_{PV_j}|_{j=1,2,..,k} = I_{PV_{sh}},\quad V_{PV_j}|_{j=1,2,..,k} = V_{PV_{sh}}. \quad (17)$$

The remaining unshaded strings generate a current and a voltage of

$$I_{PV_j}|_{j=k+1,...,N_{PV}} = I_{PV_{un}},\quad V_{PV_j}|_{j=k+1,...,N_{PV}} = V_{PV_{un}}. \quad (18)$$

Considering (16)–(18), the power processed by DAB converters connected to the shaded and unshaded PV strings are determined by (19) and (20), respectively

$$P_{DAB_{sh}} = \frac{(N_{PV}-k)\times I_{PV_{un}}\times\left(V_{PV_{un}}-V_{PV_{sh}}\right)}{\left((N_{PV}-k)\times I_{PV_{un}} + k\times I_{PV_{sh}}\right)}\times I_{PV_{sh}} \quad (19)$$

$$P_{DAB_{un}} = \frac{k\times I_{PV_{sh}}\times\left(V_{PV_{sh}}-V_{PV_{un}}\right)}{\left((N_{PV}-k)\times I_{PV_{un}} + k\times I_{PV_{sh}}\right)}\times I_{PV_{un}}. \quad (20)$$

Figs. 7(a) and 8(a), generated using (19), depict the impact of voltage and current variations among PV strings on the processed power of DAB converters connected to shaded PV arrays. On the other hand, Figs. 7(b) and 8(b), based on (20), illustrate the same effect on the processed power of DAB converters connected to unshaded PV strings. It is important to note that in the figures, the sign of normalized powers indicates the direction of power flow: a positive sign signifies power transfer from the virtual bus to the PV string, while a negative sign indicates the opposite.

As previously discussed, the DPP architectures in PV systems are designed to reduce processed power as the severity of mismatch conditions decreases. When the difference between shaded and

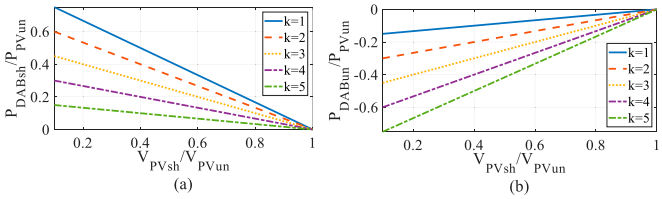

Fig. 7. Influence of voltage difference among PV strings on processed power of DAB converters. (a) Connected to the shaded PV strings. (b) Connected to the unshaded PV strings $\left(N_{PV}=6, \frac{I_{PV_{sh}}}{I_{PV_{un}}}=1\right)$.

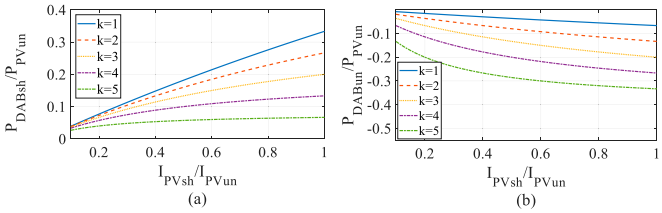

Fig. 8. Influence of current difference among PV strings on processed power of DAB converters. (a) Connected to the shaded PV strings. (b) Connected to the unshaded PV strings $\left(N_{PV}=6, \frac{V_{PV_{sh}}}{V_{PV_{un}}}=0.6\right)$.

unshaded voltages approaches 0 $\left((V_{PV_{sh}}/V_{PV_{un}})\rightarrow 1\right)$, it signifies a decrease in the severity of shading within the PV system. This reduction in shading severity leads to a decrease in both $P_{\mathrm{DAB}_{sh}}$ and $|P_{\mathrm{DAB}_{un}}|$, as illustrated in Fig. 7.

As depicted in both Figs. 7 and 8, an increase in the number of shaded PV strings (k) consistently leads to a reduction in $P_{\mathrm{DAB}_{sh}}$ and a concurrent increase in $|P_{\mathrm{DAB}_{un}}|$. This behavior is attributed to the main bus voltage. As the number of shaded PV strings rises, the influence of the shaded PV string voltage becomes more pronounced, causing the main bus voltage to approach the shaded PV string voltage while moving further away from the unshaded PV string voltage. Consequently, given that P_{DAB_j} is proportional to the difference between the main bus voltage and the voltage of the j^{th} PV string, as per (15), $P_{\mathrm{DAB}_{sh}}$ decreases, while $|P_{\mathrm{DAB}_{un}}|$ increases. Furthermore, as illustrated in Figs. 7 and 8, $P_{\mathrm{DAB}_{un}}$ is negative, while $P_{\mathrm{DAB}_{sh}}$ is positive. This emphasizes the power transfers from the unshaded PV strings to the virtual bus, while the shaded strings draw power from the virtual bus.

Fig. 8 demonstrates an increase in current leads to a higher processed power output for all DAB converters, whether connected to shaded or unshaded PV strings. To delve deeper into this observation, we can turn to (6), which describes the balancing of the bus voltage as a weighted average of all PV strings' voltages, with the PV string currents serving as the weighting factors. This means that a PV string with a higher current exerts a more substantial influence on the bus voltage.

In scenarios where the voltages of PV strings remain constant, an increase in the current of shaded PV strings pushes the bus voltage closer to the voltage of shaded PV string while simultaneously moving it further away from the unshaded PV strings' voltage. This initially might suggest that $P_{\mathrm{DAB}_{sh}}$ decreases, while $|P_{\mathrm{DAB}_{un}}|$ increases. However, it is essential to recognize that the impact of increasing the shaded PV strings' current outweighs the effects of the mentioned phenomenon on $P_{\mathrm{DAB}_{sh}}$. Thus, both $P_{\mathrm{DAB}_{sh}}$ and $|P_{\mathrm{DAB}_{un}}|$ experience an increase.

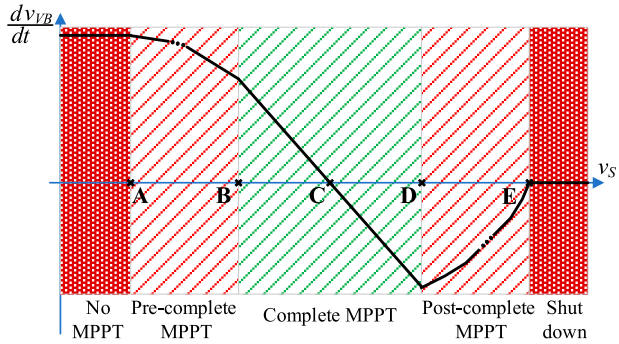

Fig. 9. Operational regions of the PV2VB PDPP architecture.

To define the power rating of the converters, the worst-case practical scenario should be considered. The theoretical worst-case scenario occurs when $I_{PV_{sh}}$ equals $I_{PV_{un}}$ and $V_{PV_{sh}}$ equals 0, with k equal to 1. Considering (19), the ratio of the DAB converters power rating to the PV string's peak power, with the latter defining the power rating of FPP SLCs in multistring architectures, is

$$\frac{P_{\mathrm{DAB}}}{I_{PV_{un}}\times V_{PV_{un}}}=\frac{(N_{PV}-1)}{N_{PV}}. \tag{21}$$

Equation (21) reveals that, when the PV string count is 2, 3, 4, or ∞, the power rating of DAB converters is 50%, 66%, 75%, and 100% of that of FPP converters, respectively for the theoretical worst-case scenario. However, this scenario is exceedingly stringent and rarely, if ever, occurs. Thus, DAB converters can be designed with power ratings as a fraction of the PV string's peak power, reducing both size and cost.

B. BL Converters

BL converters have distinct ratings compared to DAB converters, and determining their rating is a straightforward process. BL converters must continually provide a path for the current from their associated PV string, and this characteristic defines the current rating of the BL converters. Additionally, the voltage of the intermediate buses plays the role in determining the voltage rating of the components within the BL converters. Since there is flexibility in choosing the voltage of the intermediate buses, it becomes feasible to opt for a voltage lower than the PV string voltage. Consequently, the component rating of the BL converter can be lower than PV strings rating, which defines the power rating of FPP SLCs.

IV. Design SLC's Voltage

Restricting the virtual bus and intermediate bus voltage to a fraction of the PV strings' voltage offers several advantages associated with a low voltage converter. However, it can lead to ineffective MPPT during severe shading scenarios, since these voltage defines the SLCs maximum voltage $(\pm V_{\mathrm{SLC}_{\max}})$.

Fig. 9 illustrates five operational regions of PV2VB PDPP architecture, which analysis allows understanding the importance of selecting an appropriate virtual bus and intermediate bus voltage to ensure effective functionality.

1) In region 1, called *No MPPT*, the main bus voltage falls within the range of

$$0 \le v_S < \mathrm{A} = \left(V_{PV_{\mathrm{MPP}_{\min}}} - V_{\mathrm{SLC}_{\max}}\right), V_{PV_{\mathrm{MPP}_{\min}}} > V_{\mathrm{SLC}_{\max}} \tag{22}$$

where $V_{PV_{\mathrm{MPP}_{\min}}}$ is the minimum MPP voltage amongst all PV strings. Such a low v_S results in all SLCs operating at their maximum inverted voltage ($-V_{\mathrm{SLC}_{\max}}$). Therefore, none of the PV strings operate at their MPP, but instead, their voltages align with the voltage specified by the SLCs

$$v_{PV_{\mathrm{i}}} = V_{\mathrm{SLC}_{\max}} + v_S. \tag{23}$$

Therefore, PV strings operate within their constant current region on their I-V curves, continuously charging the virtual bus. Assuming a perfectly constant current, the instantaneous rate of change of the virtual bus voltage can be expressed as

$$\frac{dv_{VB}}{dt} = \frac{V_{\mathrm{SLC}_{\max}} \sum_{i=1}^{N_{PV}} I_{PV_{SC_i}}}{C_{VB} \times v_{VB}} \tag{24}$$

where $I_{PV_{SC_i}}$ represents the short-circuit current of the i^{th} PV string. This indicates that the virtual bus voltage is consistently increasing, leading to a lack of equilibrium point in this region. Moreover, none of the PV strings are operating at their MPP.

2) As v_S increases and reaches point A, the architecture enters the region *precomplete MPPT*

$$A = \left(V_{PV_{\mathrm{MPP}_{\min}}} - V_{\mathrm{SLC}_{\max}}\right) \le v_S < B = \left(V_{PV_{\mathrm{MPP}_{\max}}} - V_{\mathrm{SLC}_{\max}}\right) \tag{25}$$

where $V_{PV_{\mathrm{MPP}_{\max}}}$ is the maximum MPP voltage amongst all PV strings. At point A, the PV string with the lowest voltage initiates MPPT while maintaining its SLC voltage within the permitted range, whereas other PV strings still remain in the constant current region of their I-V curves. With the gradual increase of the main bus voltage, PV strings sequentially beginoperating at their respective MPP. In this region, N_1 PV strings with MPP voltage lower than $(v_S - V_{\mathrm{SLC}_{\max}})$ achieve their MPP, while N_2 PV strings with MPP voltage higher than $(v_S - V_{\mathrm{SLC}_{\max}})$ remain in their constant current region of I-V curve. Simultaneously, the continuous charging of the virtual bus persists according to the following rate of change:

$$\frac{dv_{VB}}{dt} = \frac{\sum_{i=1}^{N_1}(V_{PV_{\mathrm{MPP}_i}} - v_S) I_{PV_{\mathrm{MPP}_i}} + V_{\mathrm{SLC}_{\max}} \sum_{i=1}^{N_2} I_{PV_{SC_i}}}{C_{VB} \times v_{VB}},\ N_1 + N_2 = N_{PV} \tag{26}$$

where $V_{PV_{\mathrm{MPP}_i}}$ and $I_{PV_{\mathrm{MPP}_i}}$ are the operating MPP voltage and MPP current of the i^{th} PV string. In this region, although some PV strings may operate at their MPP, the absence of an equilibrium point persists due to the continuous charging of the virtual bus.

3) When v_S rises and stays within the following range:

$$B = \left(V_{PV_{\mathrm{MPP}_{\max}}} - V_{\mathrm{SLC}_{\max}}\right) \le v_S < D = \left(V_{PV_{\mathrm{MPP}_{\min}}} + V_{\mathrm{SLC}_{\max}}\right) \tag{27}$$

the architecture enters in *complete MPPT* region where all PV strings can work at their MPP. Based on the voltage of main bus, the virtual bus can be charged or discharged by the following rate of change:

$$\frac{dv_{VB}}{dt} = \frac{\sum_{i=1}^{N_{PV}}(V_{PV_{\mathrm{MPP}_i}} - v_S) I_{PV_{\mathrm{MPP}_i}}}{C_{VB} \times v_{VB}}. \tag{28}$$

In this region, an equilibrium point, point C where all strings work at their MPP and virtual bus voltage remains constant, exists.

4) In the *postcomplete MPPT* region, when the voltage surpasses point D

$$D = \left(V_{PV_{\mathrm{MPP}_{\min}}} + V_{\mathrm{SLC}_{\max}}\right) \le v_S < E = \left(V_{PV_{OC_{\max}}} + V_{\mathrm{SLC}_{\max}}\right) \tag{29}$$

where $V_{PV_{\mathrm{OC}_{\max}}}$ is the maximum open circuit voltage amongst all PV strings, an increase in v_S results in a rise in the voltage of the PV string with the lowest MPP voltage, causing it to no longer operate at its MPP. With further escalation of v_S, more PV strings deviate from their MPP, some even reaching the open circuit state. In essence, within this region, N_3 PV strings reach the open circuit voltage, N_4 PV strings operate at $(v_S - V_{\mathrm{SLC}_{\max}})$, which is between their open circuit voltage and their MPP voltage, and N_5 PV strings operate at their MPP. Consequently, the virtual bus undergoes continuous discharge described by the rate

$$\frac{dv_{VB}}{dt} = \frac{-V_{\mathrm{SLC}_{\max}} \sum_{i=1}^{N_4} I_{PV_i} + \sum_{i=1}^{N_5}(V_{PV_{\mathrm{MPP}_i}} - v_S) I_{PV_{\mathrm{MPP}_i}}}{C_{VB} \times v_{VB}} \tag{30}$$

where $N_3 + N_4 + N_5 = N_{PV}$. The PV strings at open circuit voltage no longer contribute to discharging the virtual bus, and there is no equilibrium point in this region.

5) Once the voltage exceeds point E, all PV strings operate at open circuit, resulting in no current flow within the circuit (*shut-down* region). Thus, there's no energy transfer through the circuit, leading to a zero change rate of the virtual bus voltage.

The system displays all five regions only when point A is positive and points B, C, D, and E are sequentially positioned ($0 < \mathrm{A} < \mathrm{B} < \mathrm{C} < \mathrm{D} < \mathrm{E}$). However, the focus and interest lie on the complete MPPT region, where an equilibrium point exists. Therefore, it is imperative for point D to be positioned to the right of Point B, which means that:

$$V_{\mathrm{SLC}_{\max}} \ge \frac{V_{PV_{\mathrm{MPP}_{\max}}} - V_{PV_{\mathrm{MPP}_{\min}}}}{2}. \tag{31}$$

Based on (31), it is possible to increase the MPPT range $\left[V_{PV_{\mathrm{MPP}_{\min}}}, V_{PV_{\mathrm{MPP}_{\max}}}\right]$ by increasing the virtual bus or intermediate bus voltage, since they define $V_{\mathrm{SLC}_{\max}}$. Furthermore, it is crucial to ensure that the main bus voltage does not surpass point E. Failure to do so might lead to controller failure and an inability to reach the desired equilibrium point (point C). On the contrary, regarding the virtual bus's charging/discharging, there exists no specific constraint on the minimum main bus voltage limit. Yet, for the central converter to function properly, its input voltage must exceed a certain threshold, thereby imposing a minimum limit.

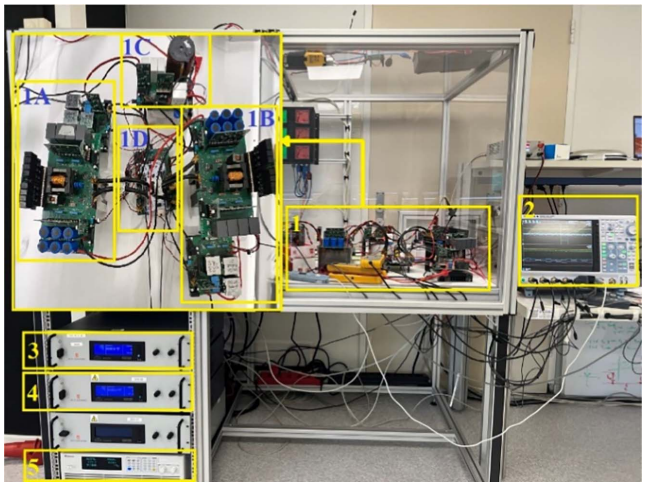

Fig. 10. Photograph of the PV2VB PDPP architecture prototype. 1A: SLC_1, 1B: SLC_2, 1C: central converter, 1-D: microcontroller, 2: YOKOGAWA DLM5038 oscilloscope, 3 and 4: SM1500-CP-30 bidirectional dc power supplies, 5: 6210H-600S programmable dc power supply.

TABLE II
ELECTRICAL SPECIFICATIONS AND COMPONENT PARAMETERS OF THE SYSTEM

	Parameter	Symbol	Value
Electrical specifications	PV system rated power	P_{sys}	3.9 kW
	Virtual bus voltage	V_{VB}	200 V
	Nominal MPP voltage	V_{MPP}	390 V
	Nominal MPP current	I_{MPP}	10 A
	SLC rated current	I_{SLC}	5 A
	SLC rated voltage	V_{SLC}	200 V
	Number of PV strings	N_{PV}	2
	Switching frequency	f_{sw}	100 kHz
Components parameters	Virtual Bus Capacitance	C_{VB}	11.2 mF
	BL inductance	L_{BL}	660 µH
	BL capacitor	C_{BL}	3 µF
	DAB leakage inductor	$L_{DAB_{Leak}}$	22 µH
	Boost inductor	L_S	510 µH
	Bus capacitor	C_S	6.6 µF

V. EXPERIMENTAL RESULTS

This section highlights the ability of the proposed architecture to perform MPPT at the string level without processing the full power generated by the PV strings. While the prototype of the proposed the PV2VB PDPP architecture is depicted in Fig. 10, its detailed electrical specifications and component values are summarized in Table II. Indoor experiments utilized one 6210H-600S programmable dc supply as one PV string and two SM1500-CP-30 bidirectional dc power supplies as the other PV string and the dc output voltage of the central converter (V_{out} in Fig. 12). Evaluation of the system's operation and performance was based on two different PV string curves shown in Fig. 11. I-V curve 1 represents a uniform PV string, while I-V curve 2 represents a PV string operating under partially shaded conditions.

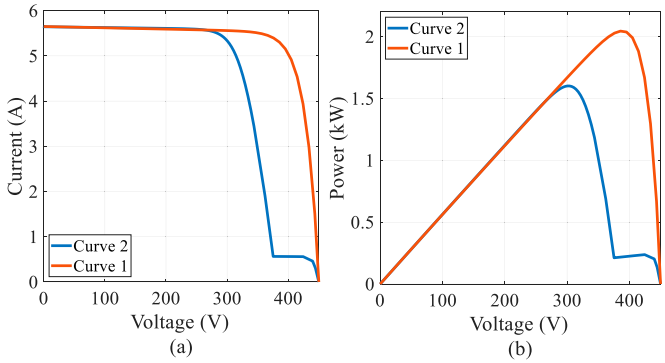

Fig. 11. PV string's. (a) I-V curves. (b) P-V curves were used in the experiments.

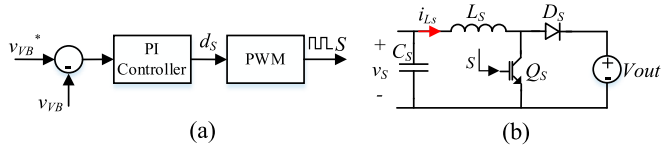

Fig. 12. The dc-dc stage of the central inverter. (a) Block diagram of the controller. (b) Topology.

A. String-Level MPPT

In the proposed architecture, the central converter regulates the virtual bus voltage, while the SLCs track the MPP of the PV strings. Three scenarios were examined to evaluate system performance. In all scenarios, PV string 2 consistently exhibits I-V curve 1. On the other hand, PV string 1 transitions from generating I-V curve 1 to 2 in scenario I, whereas in scenario II, it reverts from I-V curve 2 to 1. Lastly, scenario III was considered to verify the performance of the proposed PV2VB PDPP architecture under irradiance variations. In this scenario, both PV strings are subject to uniform conditions, hence they exhibit I-V curves similar to I-V curve 1 (with a single power peak). However, while PV string 2 consistently generates I-V curve 1, which represents the case of a PV string under 1000 W/m^2 irradiance, the irradiance over PV string 1 decreases over time to 700 W/m^2 and then to 500 W/m^2, before increasing back to 1000 W/m^2.

1) Central Converter: Here, a boost converter among various possible topologies has been chosen as the central converter to regulate the virtual bus voltage via a PI controller with a sampling time of 60 ms (Fig. 12). It controls the virtual bus by controlling its input voltage, which is the main bus voltage. Figs. 13 and 14 illustrate the central converter's capability to control the virtual bus voltage via the main bus voltage. In Fig. 13, the scenario I is depicted, demonstrating that after transitioning from I-V curve 1 to curve 2, the virtual bus reaches the desired value of 200 V in about 1 s. This is achieved by decreasing the main bus voltage according to (6) after PV string 1 changes from I-V curve 1 to I-V curve 2. Conversely, upon implementing the scenario II, the main bus voltage increases and reverts to its initial state (Fig. 14). Additionally, as depicted in Fig. 15 and expected from (6), when both PV strings have identical MPP voltages (uniform condition), the main bus voltage closely matches that of the PV strings.

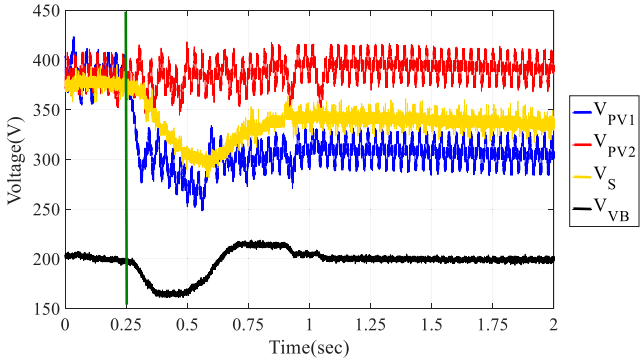

Fig. 13. Voltage waveforms. Scenario I: PV string 2 stays at I-V curve 1, whereas PV string 1 transitions from I-V curve 1 to I-V curve 2 at 0.25 s.

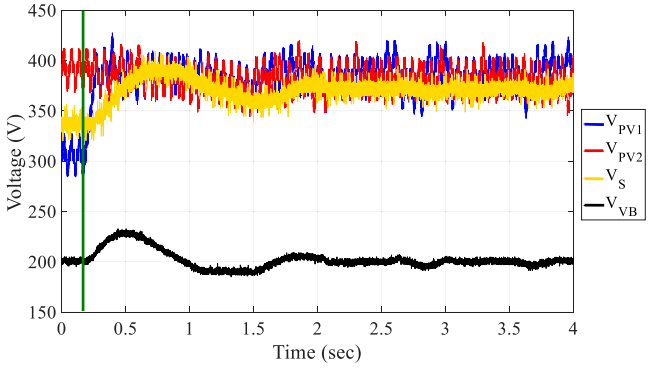

Fig. 14. Voltage waveforms. Scenario II: PV string 2 stays at I-V curve 1, whereas PV string 1 transitions from I-V curve 2 to I-V curve 1 at 0.2 s.

The irradiance level primarily influences the current generated by the PV string, exhibiting a linear relationship. In Scenario III, the irradiance over PV string 1 changes from 1000 to 700 W/m^2, then to 500 W/m^2, back to 700 W/m^2, and finally returns to 1000 W/m^2 at 0.6, 2.7, 4.9, and 6.7 seconds, respectively. As depicted in Fig. 15, the SLCs can track the MPP rapidly, while the central controller adjusts the virtual bus voltage more gradually. This indicates that the slower response of the central controller does not adversely affect the MPPT efficiency.

2) SLC Converters: A 1:1 conversion is feasible, allowing symmetrical implementation with low-voltage devices on both the primary and secondary sides of the DAB converter. The primary ports of DAB converters are connected in parallel. In turn, the distribution of the virtual bus capacitor at the inputs of the DAB converters is possible. Similar to industrial FPP multistring inverters [34], in the proposed PV2VB PDPP architecture, SLCs can be integrated within the same inverter unit.

Here, SLC_1 is connected to the partially shaded PV string, while SLC_2 is connected to the unshaded PV string. Fig. 16 shows that the DAB converter phase shift related to SLC_1 (DAB_1) is positive, indicating power is drawn from the virtual bus and transferred to PV string 1. Conversely, the phase shift of the DAB converter related to SLC_2 (DAB_2) is negative, signifying that PV string 2 injects power to the virtual bus, compensating for the power being drawn by string 1.

The task of finding the MPP of PV strings falls upon the BL converters. Here, a Perturb and Observe (P&O) algorithm with

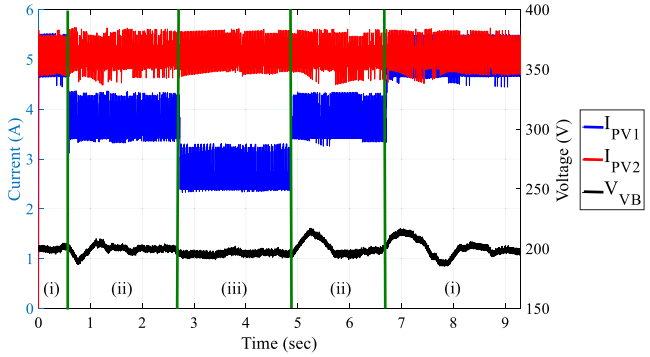

Fig. 15. Voltage waveforms. Scenario III: PV string 2 stays at I-V curve 1, whereas PV string 1 transitions from I-V curve 1 with 1000 to 700 W/m^2 and then to 500 W/m^2, before increasing back to 1000 W/m^2. (i) 1000 W/m^2, (ii) 700 W/m^2, and (iii) 500 W/m^2.

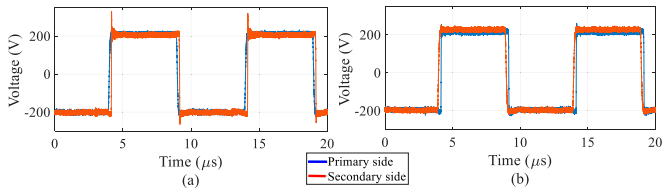

Fig. 16. DAB operation. (a) DAB_1. (b) DAB_2. Primary and secondary sides refer to the sides connected to the virtual bus and intermediate bus, respectively.

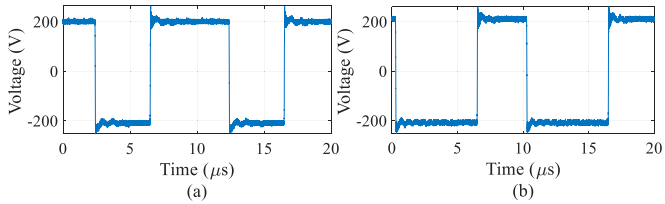

Fig. 17. Voltage of BL converters before LC filter. (a) BL_1. (b) BL_2.

a perturbation period of 15 ms and a perturbation step size of duty cycle of 3.5% is employed. Figs. 13–15 prove the system's ability to independently find the MPP of both PV strings with the typical behavior of P&O MPPT. When transitioning from I-V curve 1 to I-V curve 2, the MPP voltage of PV string 1 shifts from 390 to 300 V, while PV string 2 remains at the same voltage level, as there are no changes affecting PV string 2. Moreover, as illustrated in Fig. 17, the BL converter associated with SLC_1 exhibits a duty cycle higher than 0.5, indicating that, according to (12), it provides a positive voltage to deliver power from the intermediate bus to the string.

The other BL converter operates in the opposite manner, transferring power from the unshaded PV string to the virtual bus. Thus, power can be efficiently exchanged with the virtual bus through the SLCs, ensuring stability at the desired voltage. Finally, Figs. 16 and 17 reveal that the switches of the DAB and BL converters only need to withstand the virtual bus voltage of 200 V, even though the system operates under 390 V.

B. DAB Converter Processed Power

To analyze the power processed by the DAB converters, the MPP voltage of PV string 2 is kept constant at 390 V while

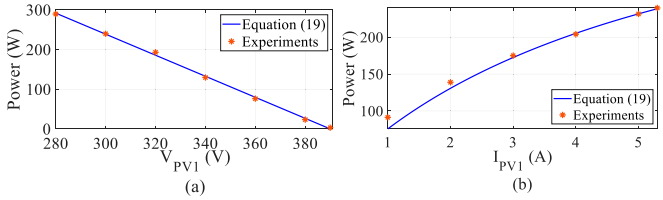

Fig. 18. Influence of (a) voltage difference between PV string 1 and PV String 2 ($I_{PV_1} = I_{PV_2} = 5.3$ A, $V_{PV_2} = 390$ V). (b) Current difference between PV string 1 and PV string 2 ($V_{PV_1} = 300$ V, $V_{PV_2} = 390$ V, $I_{PV_2} = 5.3$ A) on processed power of DAB_1 (connected to the partially shaded PV string).

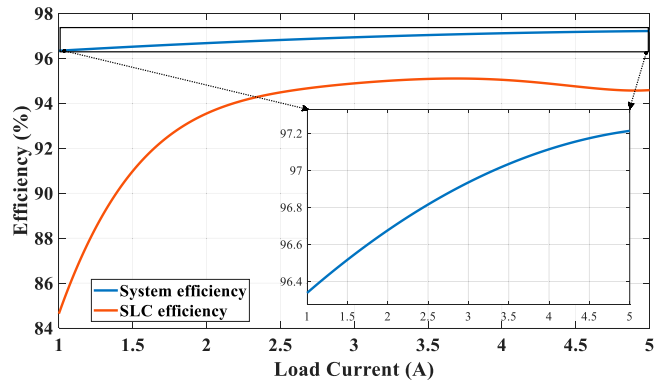

Fig. 19. Averaged system and a single SLC efficiency for load voltage from −55 to 55 V as a function of load current.

varying the MPP voltage of PV string 1 from 280 to 390 V. The current of both PV strings is kept at 5.3 A. In another experiment, the MPP voltages of PV string 1 and 2 are kept constant at 300 and 390 V, respectively, and the current of

PV string 2 is kept at 5.3 A while varying the MPP current of PV string 1 from 1 to 5.3 A. Fig. 18 shows that the power processed by the DAB_1, as determined by experimental results, closely aligns with the values predicted by (19). This result serves as validation for the equation and the explanations provided in Section III.

C. Conversion Efficiency of the PV2VB PDPP Architecture

The efficiency of the SLCs was measured under the following conditions: 200 V input (virtual bus) voltage, load voltage between −55 and 55 V, and varying load current between 1 and 5 A. Fig. 19 illustrates that, under these conditions, the average efficiency of a single SLC ranges from 84.4% to 95.1%. Similarly, the efficiency of the PV2VB PDPP architecture was measured, with the SLCs in the same conditions mentioned before. This is achieved by keeping PV string 2 constant at 390 V and 5.3 A, while adjusting the MPP voltage of PV string 1 from 280 to 390 V, corresponding to the SLC voltage range of −55 to 55 V. The averaged measured conversion efficiency of the PV2VB PDPP architecture shows an efficiency ranging from 96.4% to 97.2%. These results confirm that the system efficiency exceeds that of a single SLC. Notably, when no mismatches occur among PV voltage strings, deactivating the SLCs results in 99% system efficiency. The high system efficiency, combined with the other advantages of the PV2VB PDPP architecture, demonstrates significant potential to reduce the levelized cost of energy (LCOE).

Ultimately, the central converter consistently adjusts the main bus voltage to maintain a steady virtual bus voltage, irrespective of the number of PV strings. Each SLC operates independently to track the MPP of its respective PV string. Therefore, adding more PV strings does not introduce additional complexity from a control standpoint.

VI. Conclusion

The article presented a novel PV2VB PDPP architecture designed specifically for string-level MPPT. The innovation lay in the architecture where integrate SLCs with a capacitive virtual bus and a dual-loop control strategy. In this approach, SLCs operated in a swift inner loop for MPPT, while a central converter (e.g., boost converter) effectively regulated the virtual bus voltage. The static performance of both the central converter and SLCs was thoroughly analyzed, revealing the major SLCs requirement in being able to operate in the first and fourth quadrants of the V-I curve. To address this, the article suggested using a DAB converter followed by a BL converter. The study demonstrated that SLCs handle a fraction of the power generated by the PV strings and need to tolerate lower voltages. The experimental results confirmed the performance and theoretical explanations outlined in the sections detailing the MPPT of the proposed PV to virtual bus PDPP architecture at string level with efficiency from 96.4% to 99%.

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