WAFER BACKSIDE SURFACE MODIFICATION

Deposition of Hydrophobic Monolayers and their impact on electrical properties

Censored version

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Wafer Backside Surface Modification; Deposition of hydrophobic monolayers and their impact on electrical properties

By

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Abbreviations

AIMD - Ab Initio Molecular Dynamics
CA - Contact Angle
CMOS - Complementary Metal Oxide Semiconductor
CVD - Chemical Vapor Deposition
C_xH_y - Hydrocarbons
DIM - Di-iodomethane
DIW - Deionized Water
DUV - Deep Ultra Violet
ESVM - Electrostatic Voltmeter
F-SAM - Fluorocarbon based Self-Assembled-Monolayer
H_3O^+ - Hydronium Ion
HF - Hydrofluoric Acid
HMDS - Hexamethyldisilazane
IC - Integrated Circuit
IC-Integrated Circuit
IEP - Isoelectric Point
LPCVD - Low Pressure Chemical Vapor Deposition
LPD - Liquid Phase Deposition
MSA - Mobile Surface Analyzer
OWRK - Owen, Wendt, Rabel and Kaelble
PECVD - Plasma Enhanced Chemical Vapor Deposition
RH - Relative Humidity
SAM - Self Assembled Monolayer
SEM - Secondary Electron Microscope
SFE - Surface Free Energy
Si - Silicon
Si_3N_4 - Silicon Nitride
SI-ATRP - Surface-Initiated Atom Transfer Radical Polymerization
SiC - Silicon Carbide
$Si\text{-}NH_2$ - Silicon Amine
SiO_2 - Silicon oxide
Si-OH - Silanol
SiSiC - Silicon Infiltrated Silicon Carbide
SKPM - Scanning Kelvin Probe Microscope
TMAH - Tetramethyl Ammonium Hydroxide
UV - Ultra-Violet
WT - Wafer Table
XPS - X-Ray Photoelectron Spectroscopy

Abstract

Microchips are made from circular silicon discs called wafers and are manufactured with photolithography. A critical step of a photolithography process is when a wafer with a photoresist is placed on a wafer table (WT) and exposed to light to form patterns that build up components of an integrated circuit (IC). The dimensions of the IC are in nanometer scale and are becoming increasingly smaller. Any changes to the wafer table can contribute to alignment issues or increasing overlay between successive exposures and is dependent on interaction with the wafer backside.

Common wafer backside materials are silicon, silicon oxide and silicon nitride, which are hydrophilic, so they readily interact with water, adsorb it from the atmosphere and their surface conductivity is highly dependent on relative humidity (RH). Additionally, silicon oxide and silicon nitride generate surface charge from single-wafer wet spin tools that are part of the critical toolset for advanced IC fabrication.

A charged wafer backside in presence of water is able to conduct unwanted current through the surface that can affect the performance and yield of components the wafer backside comes in contact with during photolithography.

This thesis studies reducing the charge generation and surface conductivity of a hydrophilic silicon and silicon nitride wafer backside by depositing hydrophobic self-assembled monolayers (SAM) with silane coupling agents, which are less likely to form surface charge and have lower surface conductivity. The hydrophobic monolayers that are studied are deposited from hexamethyldisilazane (HMDS) and a non-disclosed fluorinated molecule, called F-SAM. HMDS is already used in photolithography on the wafer frontside to promote adhesion to the photoresist and fluorinated molecules are known to be hydrophobic, inert and with high electrical resistance.

This surface modification tackles both the water content on the surface and charging via single wafer wet-spin tools. The monolayers are characterized with regard to the surface chemistry, surface free energy, wear resistance, zeta potential, surface charge and conductivity. Lastly, the charge diffusion is measured when a wafer is put in contact with a wafer table in an experimental setup, where the discharge current is registered.

The outcome of this study shows that modified surfaces are found to be homogenous to a sub nanometer level and uniform. Compared to typical silicon nitride wafers, the surface conductivity is lowered by a factor of 1000 and is not affected by RH. This results in the total measured charge diffused to a wafer table to be reduced by at least a factor of 17 and is considered a promising option in reducing any unwanted current leakage from a wafer backside to surrounding components.

1. Introduction

ASML manufactures photolithography systems that are essential for patterning the structure of microchips. Microchips are manufactured from thin circular silicon discs called wafers, which go multiples times through the circular fabrication step of photolithography to create a microchip [1]. A crucial step of the photolithography process is when a photoresist has been deposited on the surface of the wafer and the wafer is exposed to a light to form patterns. The patterns build up the Integrated Circuit's (IC) components, such as transistors, diodes and more [2].

The dimensions of the ICs are becoming smaller and ASML state of the art products have reached a resolution of < 40 nm [3]. Therefore, the exact positioning of the wafer on top of the wafer table becomes critical to cope with the alignment and the overlay. Overlay is the in-plane deviation between successive exposures. As it increases, the structure of the integrated circuits that are being created become skewed until the integrated circuit becomes defective. The overlay tolerance is in the range of nanometers [4, 5].

Interaction between the wafer and the wafer table (WT) during the exposure is one of the main contributors to overlay [5]. The exact contact points between the surfaces are over single asperities and this interaction can cause wear of the WT, which in turn, results in larger overlay and alignment issues [6] [4, 5].

The interaction is highly dependent on the materials used. The wafer table is commonly made out of silicon carbide, SiC and silicon-infiltrated silicon carbide, SiSiC These materials are known for being hard and chemically inert [7].

The wafer is commonly made out of silicon, but dielectric layers are often deposited, such as silicon oxide (SiO_2) or silicon nitride (Si_3N_4), as protection from contaminants in the atmosphere and to inhibit diffusion of doping agents in the silicon core. Silicon oxide and silicon nitride are ceramics that are known for being chemically and electrically resistant [8, 9, 10]. These materials are hydrophilic, that is, have a strong affinity to water. They adsorb water from the atmosphere and form surface charge when submerged in it. Before a wafer is placed onto the wafer table, it is often rinsed with water with a wet spin rinse tool, including the backside. When rinsed with water, the hydrophilic wafers generate a streaming potential on the surface [11, 12]. Additionally, the surface conductivity is highly dependent on relative humidity (RH) so the generated charge can conduct and migrate over the surface. When the charged wafer is placed on the wafer table, these charges can diffuse to it and affect its performance and yield [13, 14].

To reduce this charge diffusion, it has been proposed to modify the surface of the wafer backside by depositing hydrophobic monolayers. Less water will adhere to a hydrophobic surface and spread over smaller areas. Hydrophobic surface sites do not form surface charge when submerged in water and could reduce the surface conductivity by blocking hydrophilic and conductive surface sites with hydrophobic and non-conductive surface sites [15].

Two types of monolayers are of interest, a monolayer formed from the precursor hexamethyldisilazane (HMDS), and a layer formed from a non-disclosed fluorocarbon molecule, C_xF_y, (F-SAM). They are known for being hydrophobic and electrically insulating and therefore show promise in limiting the adsorbed water, charge generation on the surface and charge migration from the wafer backside to the wafer table [16, 17].

HMDS is already used within the microchip industry where it is deposited on the frontside of the wafer to make it hydrophobic, which improves adhesion of photoresist to the surface. Therefore, a new material would not be introduced to the IC fabrication [17].

These monolayers have somewhat been studied with regard to electrical and tribological properties. However, limited literature is available to estimate the performance of a hydrophobic surface for this specific application.

Therefore, a study has been conducted to characterize monolayers deposited from the HMDS and fluorocarbon molecules on hydrophilic surfaces of silicon nitride and bare silicon. The whole characterization includes general characterization of surface chemistry, surface free energy and wear resistance of the monolayer. Electrical properties that affect the charge generation and diffusion were studied, which include zeta potential measurements, surface charging, charge decay and wafer table current measurements. The results from these studies were used to estimate and predict the effect a hydrophobic layer will have prior to being studied in real conditions.

The study shows that the monolayers deposited reduce significantly the charge mobility by a factor of 1000 and hence limit the charge diffusion to the wafer table and other components it comes in contact with.

2. State of the art

2.1 Photolithography process

To manufacture microchips, the wafers go through a circular fabrication step where different stacks are fabricated, and where the photolithography process is a key element as it defines the size of the integrated circuit's components, such as transistors, diodes and more [2]. ASML is the main supplier of these complex photolithographic systems [1]. The patterning of a material by a single photolithography step can be seen in *Figure 2. 1*. A masking film of metal/insulator/semiconductor is deposited on the wafer frontside, SiO_2/Si_3N_4. A thin film of HMDS is sometimes deposited on the front-side of the wafer for adhesion enhancement for photoresist during preparation (step 1). The photoresist is deposited on top of the layer in step 2 and the resist is dried out with a pre-bake step. After alignment, the wafer front-side is exposed to a light beam on predetermined areas that drives a chemical reaction to form a pattern (step 3). For Deep Ultra Violet (DUV) systems, the predetermined area for exposure is defined by a mask. After exposure, and a post bake, the area that was exposed is then developed, for example with tetramethyl ammonium hydroxide (TMAH), to remove the exposed or unexposed resist (step 4). In this figure, the exposed photoresist is removed. The exposed area can now be treated selectively as compared to the unexposed areas, and a fabrication process step (i.e. etching, implanting or other) can be realized in only these areas (step 5). Finally, the residual resist on the unexposed area is stripped away and the predetermined pattern of SiO_2/Si_3N_4 is left (step 6). An integrated circuit forms when this process is repeated multiple times with a final product of a microchip [2, 18]. To make small 3D structures both the alignment and overlay are critical parameters, which are primarily determined by accurate positioning of the wafer onto the wafer table.

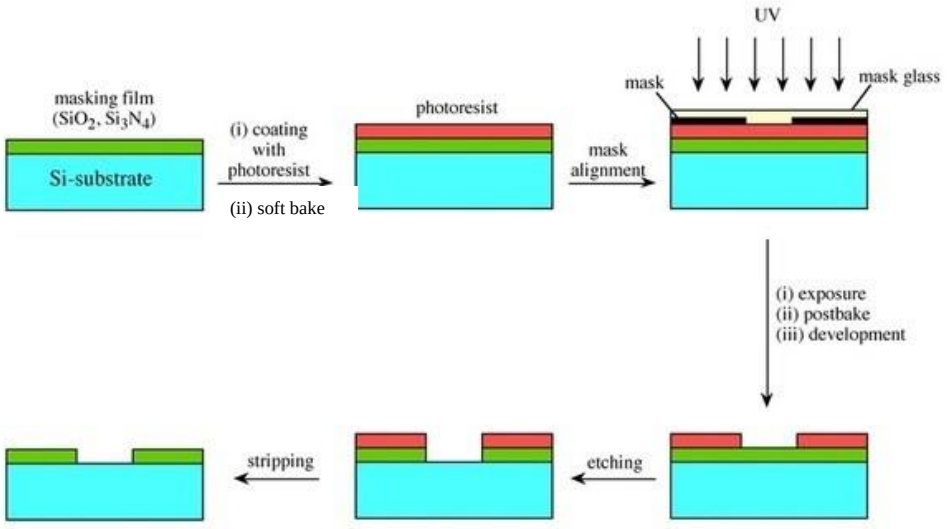

Figure 2. 1: A schematic of a photolithographic cycle. A Si wafer is prepared with a masking film of SiO_2/Si_3N_4 (step 1) and a photoresist is deposited on top (step 2). The wafer is loaded onto a wafer table and exposed to light through a mask at a specific to create a specific pattern in the photoresist (step 3). After exposure, the exposed photoresist is removed with development (step 4) and the area now of SiO_2/Si_3N_4 can be treated selectively to the unexposed area. In this schematic is etched away (step 5). The residual photoresist is removed (step 6) [2, 18].

2.2 Overlay

There is constant demand to reduce the sizes of microchips. A factor that is becoming increasingly important as feature sizes decrease, is overlay. Overlay is the in-plane deviation between successive

exposures during wafer processing, see *Figure 2. 2* [4]. As the IC become smaller, the tolerance for the overlay decreases drastically in time. Currently an ASML NXT:2050i scanner can reach overlay as low as 2.5 nm [3].

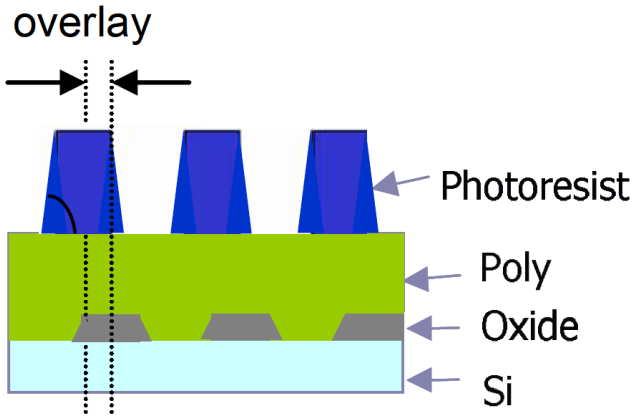

Figure 2. 2: Schematic of a silicon wafer with silicon oxide, poly silicon and deposited photoresist layer. The silicon oxide and photoresist have been exposed to form a specific pattern with the overlay indicated as the deviation between the identical patterns [4].

Figure 2. 2 shows a silicon substrate with an oxide, polysilicon and a photoresist layer. The photoresist and the oxide layer have been developed and etched to form the same pattern. The overlay is defined as the alignment difference between the oxide and photoresist layer. As the overlay increases the pattern becomes increasingly uneven until the circuit being created will not function. Overlay and other factors are influenced by the interaction between the wafer backside and the wafer table, when placing the wafer for exposure [4].

Accurate alignment of the wafer onto the WT for multiple exposures is key. During a 40-100 step of processing a single wafer, which can take several months, the wafer table and wafer backside interaction change in time, which can result in deviations for exact alignment. [5].

2.3 Wafer table (WT)

General designs of a WT from ASML and Canon can be seen in *Figure 2. 3* [6].

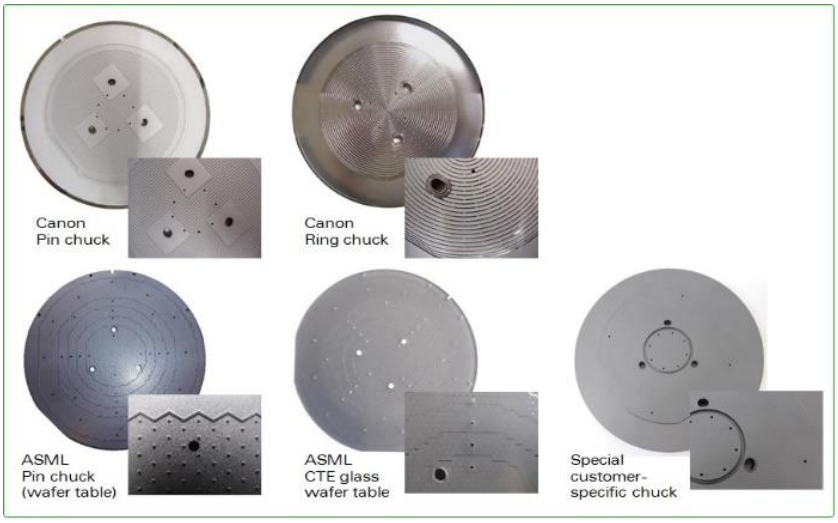

Figure 2. 3: Different wafer table/chuck designs from ASML and CANON. The wafer is placed and loaded on the WT/chuck during exposure in a lithography process [6].

As seen in *Figure 2. 3*, a WT design is often covered in small outstanding pins on micrometer scale that come in contact with the wafer backside. These outstanding pins are not completely flat, so the actual contact is over single asperities on nanometer scale, see scheme in *Figure 2. 4* [6]. These pins are used to minimize the contact area and adhesion between a wafer and the WT.

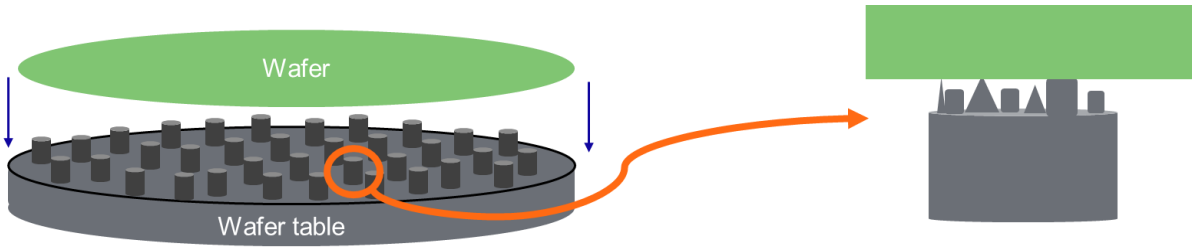

Figure 2. 4: Schematic showing contact points between the wafer backside and single asperities on wafer table outstanding pins [6].

The wafer table can be made out of Silicon Carbide (SiC) and Silicon Infiltrated Silicon Carbide (SiSiC). These materials are known for their high hardness and excellent chemical-, thermal-, corrosion- and wear resistance. The hardness of SiC makes it difficult to machine in challenging shapes so complex wafer table` designs are often made from SiSiC [7, 19].

SiSiC usually contains a free Si phase and a primary and secondary SiC phase since it is fabricated from a mixture of a SiC preform, free carbon and silicon. The SiC phase from the preform is called primary SiC and the one formed from the free carbon and liquid silicon is the secondary SiC. The SiC phases stick a bit out of the free Si phase. *Figure 2. 5* shows Secondary Electron Microscope (SEM) images of a SiSiC material where it shows how the SiC phase is within the free Si phase. The secondary and primary SiC phase cannot be distinguished from each other in the figure [7, 19].

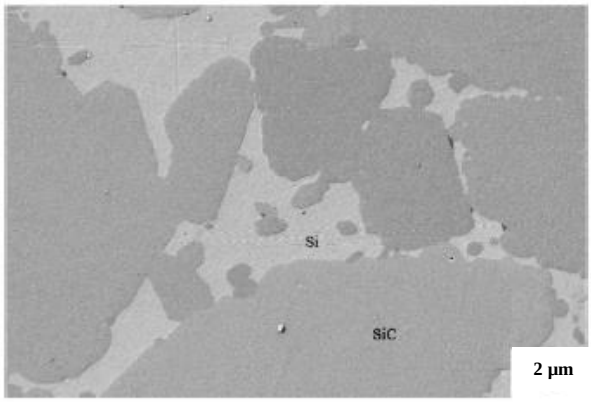

Figure 2. 5: SEM figure of a SiSiC surface showing the SiC phases in the free Si phase. [7] .

2.4 The Wafer Backside

The wafer frontside goes through all the lithography steps. It originally needs to be flat with a minimum of atomic defects and contamination. The wafer backside comes in contact with all the stages that the wafer goes through during the IC fabrication and interacts with all of them. The wafer backside needs to be able to withstand the physical contact with all these components without jeopardizing the quality on the frontside and minimize wear on surrounding components, like the wafer table [2, 20, 21].

A wafer is often made from crystalline silicon Si that can be doped to adjust the conductivity of the material. The ceramic layers Silicon oxide (SiO_2) and Silicon Nitride (Si_3N_4) can be deposited on the wafer as a protection layer from surroundings and to inhibit diffusion of doping agents and general contamination. These ceramics are also used on the frontside of a wafer, as dielectrics in capacitors and gate insulators in Complementary Metal Oxide Semiconductor (CMOS) [8, 9, 10] .

The SiO_2 and Si_3N_4 are known for high refractive index, transmittance and can be selectively etched for IC fabrication. Their properties are highly dependent on their deposition methods, such as thermally grown oxide, Plasma Enhanced Chemical Vapor Deposition (PECVD) or Low-Pressure Chemical Vapor Deposition (LPCVD) [22, 23, 24].

2.4.1 Surface sites of bare Si, SiO_2 and Si_3N_4

When silicon, silicon oxide and silicon nitride is stored in ambient conditions, a self-limiting native oxide starts to form.

Silicon oxide is commonly deposited with thermal oxidation, which mainly forms the hydrophobic surface sites siloxane, Si-O-Si. When these sites are exposed to water, the siloxane groups are hydroxylated into hydrophilic silanol sites, Si-OH, see *Equation 2. 1*. Bare silicon with the native oxide formation will mostly have silanol sites Si-OH on its surface [25].

Equation 2. 1: Silanol formation from hydroxylation of siloxane.

$$Si - O - Si(s) + H_2O\ (l)\ \rightarrow 2Si - OH\ (s)$$

The silicon oxide surface passivation layer on Si_3N_4 and bare Si develops from both oxygen and water that adsorbs to the surface when it is exposed to atmospheric conditions. The native oxide that forms has been estimated to be circa 3 nm thick [26].

The surface chemistry of Si_3N_4 is a bit more complex than SiO_2 and Si. The near-surface region is composed of Si-N, Si-N-O and Si-O bonds. It transitions from almost pure Si-N in the bulk, to intermediate Si-N-O

and Si-O as the oxide layer thickness increases, leaving the surface almost completely chemically equivalent to silica (SiO_2) at the surface [26].

Accepted form of chemical reactions that occur from Si-N bonds to silanol bonds, predominantly Si_3N, are seen in *Equation 2. 2* below [26].

Equation 2. 2: Formation of Amine and Silanol on Si_3N_4 surface from hydroxylation.

$$Si_3N\ (s) + 2H_2O\ (l) \rightarrow Si - NH_2(s) + 2Si - OH(s)$$

$$Si - NH_2(s) + H_2O(l) \rightarrow Si - OH(s) + NH_3(g)$$

A silicon nitride surface that has been exposed to air for a long time can be estimated to have fully formed a native oxide layer and to be covered > 95% with silanol sites and < 5% of primary amine groups ($Si\text{-}NH_2$) [27, 28].

Therefore, when studying the surface properties of Si, SiO_2 and Si_3N_4, it can depend on the time that has passed since the dielectric was deposited and the relative humidity the surface has been exposed to. For example, if the surface is submerged in water, the oxidation rate will be accelerated compared to when it is stored in atmospheric conditions. The samples within this study had all been in stored in atmospheric conditions of 40-60% RH for several months.

Figure 2. 6 shows how the surface of a thermally grown SiO_2 (left) and Si_3N_4 deposited with LPCVD (right) change over time. The bonds on the Si_3N_4 are solely Si_3N for simplicity. When in pristine conditions right after deposition (t_0) the surfaces are mostly covered in either siloxane bonds on the thermally grown silicon oxide or Si_3N bonds on the silicon nitride surface. After some time, the surfaces start to hydroxylate and form silanol or silanol and amine sites (t_1) [25, 26]. Finally, after a long time in storage, the surfaces can be estimated to be mostly covered in silanol sites with a low fraction of residual amine sites on the silicon nitride (t_2) [27, 29, 25] .

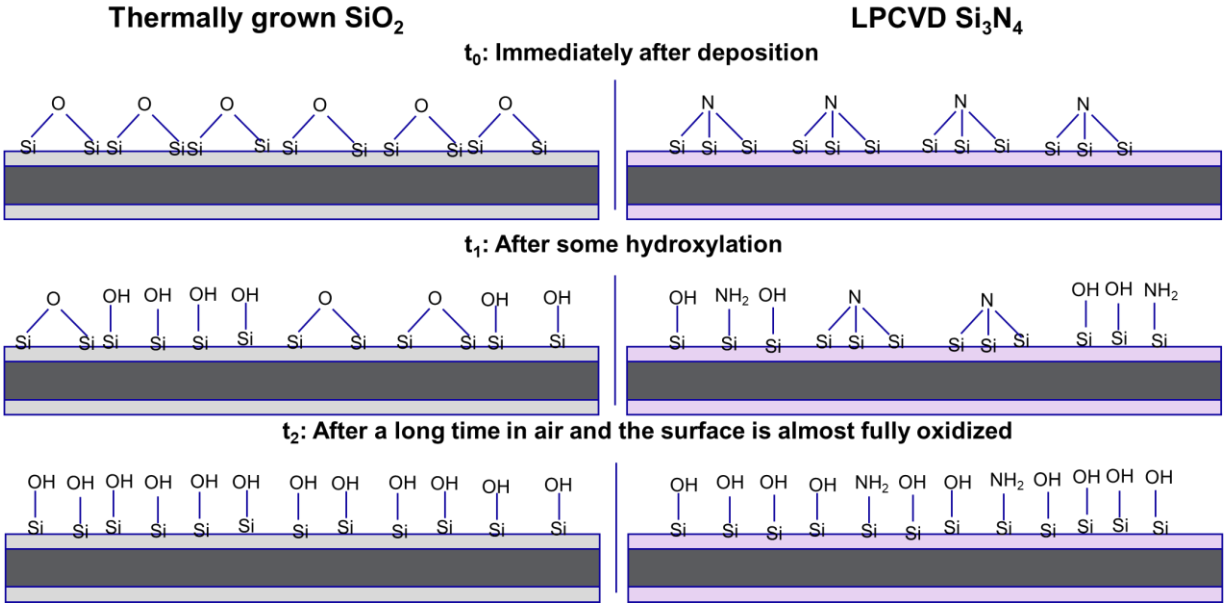

Figure 2. 6: Schematic shows the evolution of surface sites on a thermally grown SiO_2 (left) and LPCVD Si_3N_4 immediately after deposition (t_0), after some time in air where the surfaces have hydroxylated a bit (t_1) and after a long time when it can be estimated that the surfaces are highly oxidized (t_2) [25, 26, 27].

2.5 Electrical properties in presence of water

Charge can accumulate on a wafer and diffuse to surrounding components in photolithography. There are two main ways that water adsorbs to a wafer. Firstly, water will adsorb to the wafer from the air where it is stored in controlled relative humidity [26, 25]. Secondly, a wafer needs to be cleaned before placing it on the wafer table, to minimize the amount of particles. Therefore, it is rinsed with Deionized Water (DIW) through a single wafer wet spin, where a liquid is dispensed while the wafer rotates and continues to rotate to dry when the liquid has stopped dispensing [30, 12].

2.5.1. Surface charge

When a hydrophilic surface is submerged in water, active groups on the surface can dissociate and the surface becomes charged, see *Figure 2. 7(left)* [26]. At the solid-liquid interface, an electrical double layer is formed. The electrical properties within this sub 100 nm layer are divided into a Stern layer of immobile counterions (sub nm) and a thicker diffuse layer composed of mobile counterions to the surface charge, see *Figure 2. 7(right)*. The zeta potential, ζ, is defined at the location where the ions shear (move) over immobile Stern layer. The zeta potential estimates the surface charge and streaming potential [11, 31].

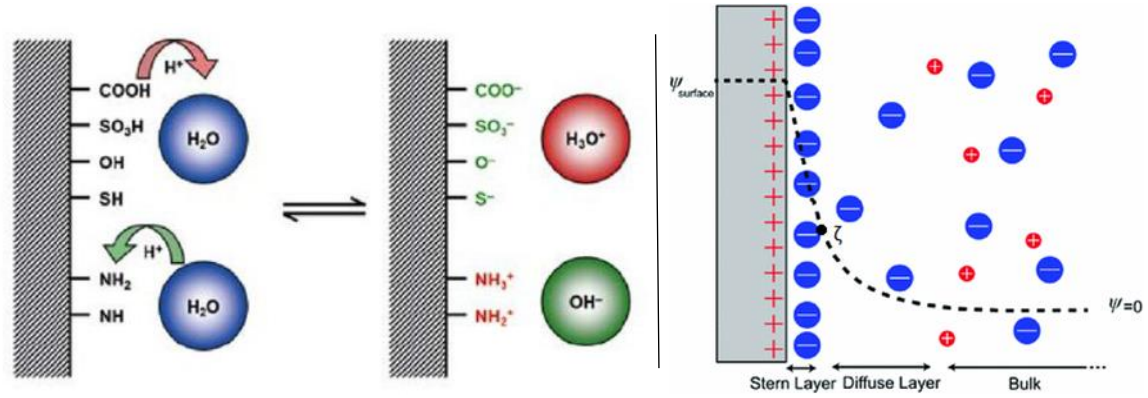

Figure 2. 7: Schematic representation of charge formation on a solid-liquid interface from the interaction between water and hydrophilic surface sites (left) [15]. Electrical Double Layer composed of the Stern and diffuse layer (right). The zeta potential indicates the barrier between the two layers [31].

The pH level where the zeta potential is zero is defined as the Isoelectric Point (IEP) and the pH level where the surface charge is zero is called the point of zero charge. Differences between these properties are present when there is a strong adsorption of anions or cations, which is not present in water. [11, 27, 15].

The IEP of silicon oxide is on the range of pH 2-4, depending on the oxidation of the surface. Pure silicon nitride has IEP at pH 7-9 but as it oxidizes over time, the IEP decreases to the range of silicon oxide. A silicon nitride that has been in storage under atmospheric conditions for a long time has IEP at pH 4 [11, 27, 26].

The isoelectric point determines whether a surface will protonate or deprotonate when submerged in liquid. For example, a silicon oxide surface that only has silanol sites will deprotonate when submerged in liquid in the range of pH 5-7, like water. DIW theoretically has pH 7 but if exposed to air it can dissolve carbon dioxide from the air, increasing the acidity up to circa pH 5.5. However, depending on the oxidation status of the silicon nitride surface, the surface might protonate more rather than deprotonate depending on its hydrophilic surface sites, see *Figure 2. 7 (left)*. When the deprotonation of the silanol sites exceed the protonation of the amine sites, the surface generates a negative zeta potential [15, 27].

Silanol and amine sites are hydrophilic sites that react via acid-based reactions when submerged in water and form the following surface sites [26].

Equation 2. 3: Deprotonation and protonation of silanol and amine surface sites

$$Si - OH_2^+(s) \leftrightarrow Si - OH(s) + H^+(aq)$$

$$Si - OH(s) \leftrightarrow Si - O^-(s) + H^+(aq)$$

$$Si - NH_3^+(s) \leftrightarrow Si - NH_2(s) + H^+(aq)$$

The protonation of silanol groups is unlikely to occur unless in highly acidic conditions and can be excluded for the regime of pH 5-7.

The surface sites of oxidized Si/SiO_2 and Si_3N_4 surfaces in dry and wet conditions can be seen on *Figure 2. 8.* The surfaces are assumed to be almost fully oxidized (t_2 in *Figure 2. 6*) The Si/SiO_2 surface are covered in silanol sites that deprotonate in DIW (pH ~7) since the IEP is in the range of pH 2-4, leaving the surface negatively charged. The Si_3N_4 surface both has silanol sites and remaining amine sites. In water, the silanol sites deprotonate but the amine sites protonate, and even pick up protons from the surrounding deprotonating silanol sites. In this way, the total surface charge is lower than on the Si/SiO_2 surface but is highly dependent on the oxidation of the surface [25, 26, 27, 28, 29, 12].

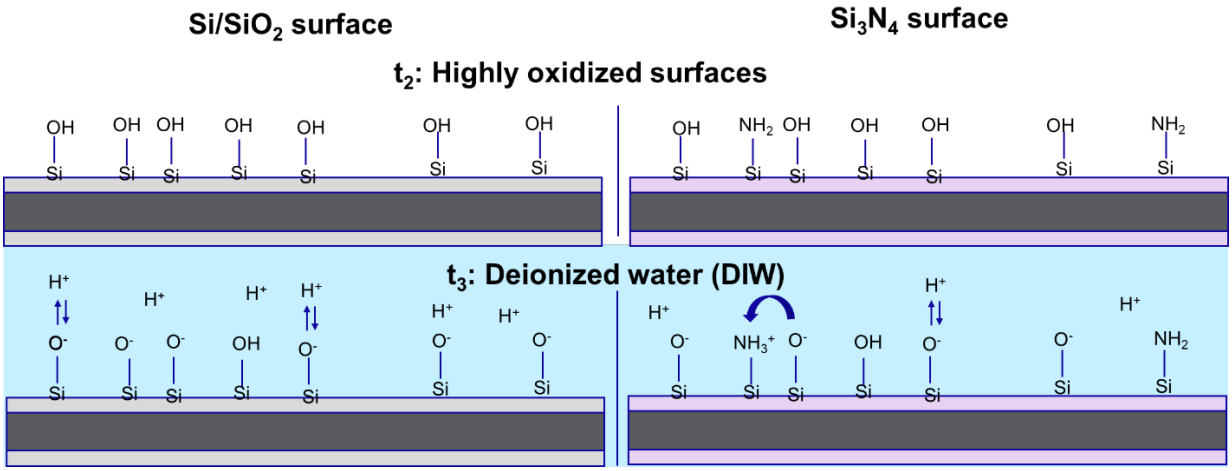

Figure 2. 8: Graph show a surface of oxidized silicon/silicon oxide to the left and an oxidized silicon nitride surface to the right in t_2 that are immersed in water at t_3. The silicon/silicon oxide surface (left) is solely covered in silanol sites and silicon nitride has both silanol and amine sites. Under wet conditions, the silanol sites deprotonate while the amine sites protonate [12, 25, 26, 27, 28, 29].

2.5.2 Streaming potential

A streaming potential is generated over a surface by a tangential flow of liquid over a solid surface [11]. The generation of streaming potential can be seen in *Figure 2. 9.* The electrical double layer is created when the surface is submerged in liquid and is shown in static equilibrium between the surface charge and its counter ions (A). When pressure is applied to the system to force a liquid flow, the mobile ions flow along with the liquid flow (B). This generates a potential difference when the mobile counter ions have transferred to the edge of the surface (C), which results in a backflow current of ions to counteract the potential (D).

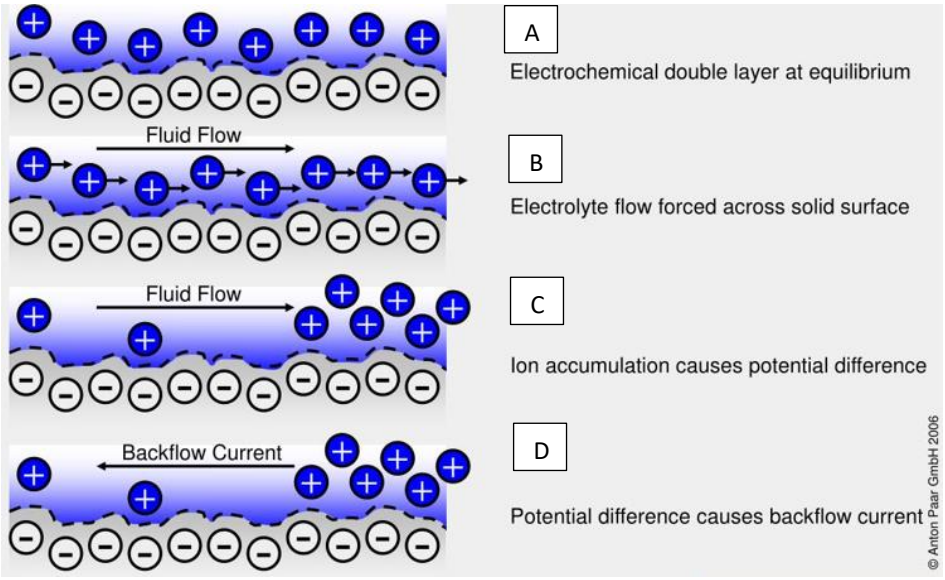

Figure 2. 9: Scheme of the generation of a streaming potential shown in several steps. Schematic (A) shows a surface submerged in water that has formed an equilibrium with the electrical double layer. Then the liquid starts flowing along the surface (B) and the counterions diffuse with the liquid flow (C). The ion accumulation at the edge of the surface creates a potential (C) that results in a backwards current of counter ions (D) [32].

An expression to calculate the streaming potential is the following:

Equation 2. 4: Streaming Potential

$$V = \frac{\varepsilon_0 \varepsilon_r \zeta \Delta P}{\eta \kappa_e}$$

Parameters ε_0 and ε_r are the dielectric constant of vacuum and dielectric constant of the liquid, respectively. The viscosity and conductivity of the liquid are the parameters η and κ_e and the pressure gradient between the inlet and outlet is ΔP. The pressure gradient is a function of the volume flow rate and geometry of the channel [11]. During a wet spin rinse the geometry would be liquid flow over a flat surface [12]. Furthermore, ΔP is a function of spin speed, ω, and duration of water dispense, t_w. Increasing either one of these variables will increase the streaming potential [12] [33].

A substantial surface charge is known to form on a SiO_2 or Si_3N_4 wafer backside from a wet spin rinse. Bare Si wafer does not accumulate similar charge due to its high relative conductivity [12].

Figure 2. 10 shows a streaming potential generation on oxidized SiO_2 and Si_3N_4 surfaces. Schematic at t_3 shows the surface charge formation when submerged in water. When the liquid starts flowing in a specific direction, t_4, the protons (H^+) flow along with the liquid flow, creating a potential where the protons have accumulated on one side of the surface and negatively charged surface sites are on the other site. The immobile counterions in the Stern layer have been left out for simplicity. This potential generation creates a backflow current that has not been included in the schematic. The final schematic at t_5 shows that the liquid has been removed and the surface is dry. It is assumed that the liquid is removed by the continuous liquid flow. This leaves the surface with negative surface sites on the left side of the surface while the other side is bonded with the proton, or they have been removed with the water. Since the silanol and amine sites can interchange their protons, the total surface charge on Si_3N_4 is lower than on SiO_2 [15, 11].

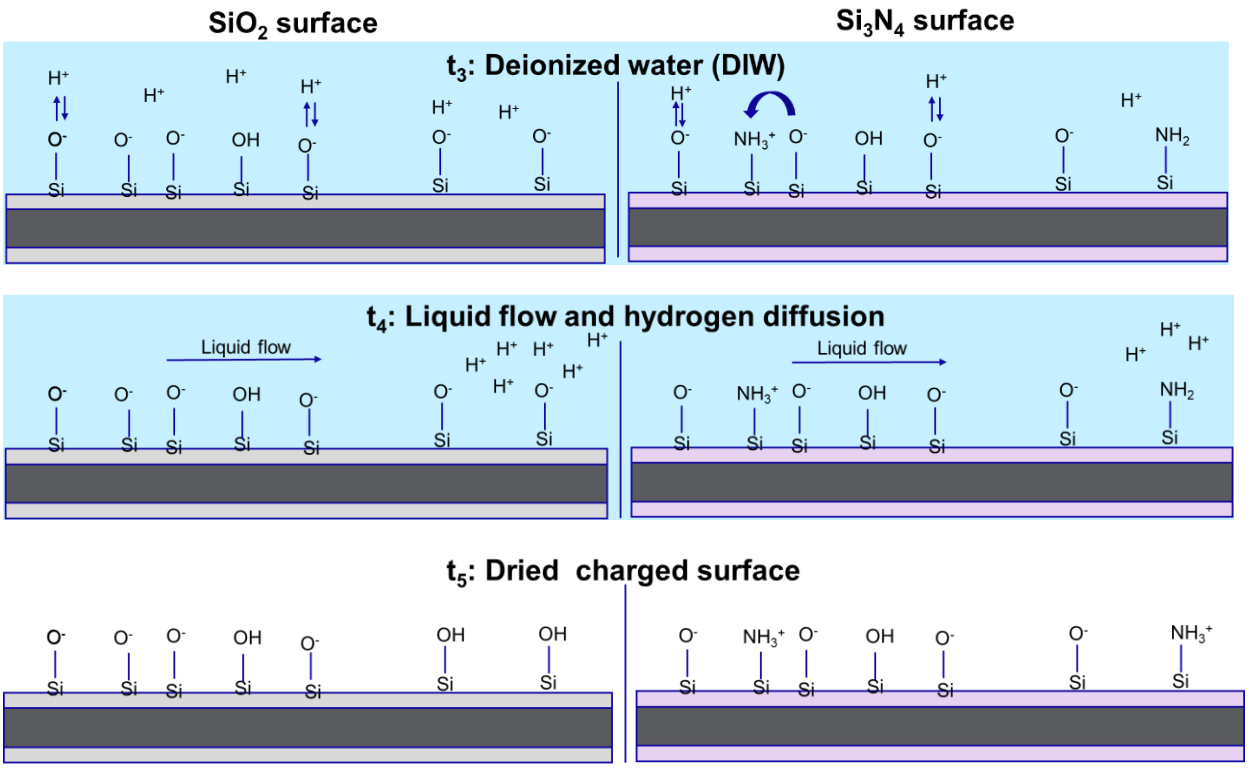

Figure 2. 10: Graph shows a simplified schematic of changes to SiO_2 (left) and Si_3N_4 (right) surfaces. The surface is submerged in water where silanol and amine sites deprotonate and protonate (t_3), generating a streaming potential when the liquid flows along the surface diffusing the protons along with the liquid (t_4). The liquid is then removed, leaving a charged dry surface (t_5) [25, 26, 11].

2.5.3 Surface charging from single-wafer wet-spin process

Single wafer wet processing tools have become a part of the critical tool-set in advanced IC manufacturing. The most common ones operate with a nozzle-type dispense of liquid chemicals positioned over the wafer.

Surface charge formation on SiO_2 wafers via wet spin rinse with water dispense in the center has been studied. The surface potential was mapped out with a ChemetriQ 5000 non-visual defect inspector system from Qcept Technologies. The potential generated was negative since there were only silanol sites on the surface that deprotonate in DIW [12].

Figure 2. 11 shows a 2D surface potential of a 300 nm SiO_2 wafer rinsed in the center for 90 s while rotating at 300 rpm (a), a control wafer that was not rinsed (b) and a color bar indicating the scale of the measured voltage (c). The profile in (a) shows a negative peak at the center where the water was dispensed and a positive peak at the edge. The profile at the edge is typically observed from a wet spin rinse and is not a result of the spin tool used. The potential of the control wafer was -1 V, which can be due to charges within the bulk of the dielectric layer rather than the surface [12].

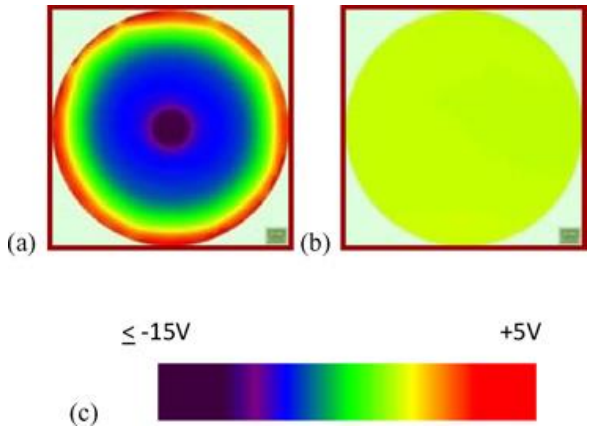

Figure 2. 11: A 2D surface potential map obtained from (a) spin rinse process with DIW, (b) reference wafer that was not rinsed and (c) a color bar that indicated the scale of the measured potential [12].

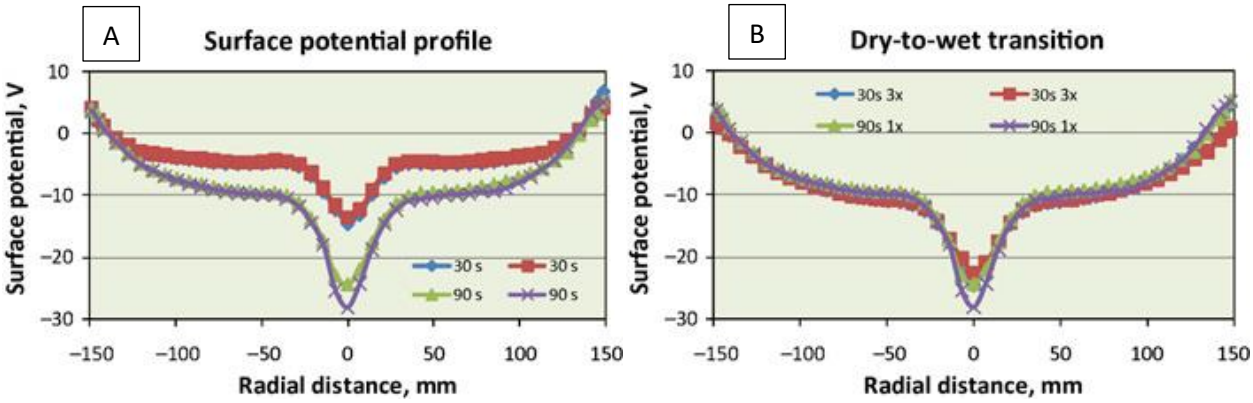

Figure 2. 12: Graph (A) shows the 1D surface potential profile of a SiO_2 wafers rinsed at 300 rpm for 30 s and 90 s showing the difference in profiles with variating process parameters. Graph (B) shows SiO_2 wafers charged for 3 x 30 s and 1 x 90 s at 300 rpm. The profiles after 3 x 30 s and 1 x 90 s rinse are almost identical showing that charging is a cumulative process [12].

Figure 2. 12 shows a 1D surface potential profile of SiO_2 rinsed at 300 rpm for 30 s and 90 s (A) and 3 x 30 s and 1 x 90 s (B). Graph A shows how the variating dispense time affects the charge generation. The edge and central peaks are larger and the overall local charge over the wafer is more negative after 90 s rinse rather than 30 s. This confirms the effect the process parameters have on the charge generation. The ΔP of the streaming potential is a function of the dispense time, so with increasing dispense time a larger streaming potential will be generated. Graph B shows that there is negligible difference in the surface potential profile after a wafer has been rinsed for 3 x 30 s and 1 x 90 s, concluding that the charging mechanism is a cumulative process rather than being dependent on the number of times the wafer is rinsed and dried [12].

2.5.4 Surface conductivity, σ

When a surface is charged, these charges can diffuse over the surface. Surface conductivity is an indication of whether charges are mobile and can migrate over a surface. It is enhanced in the presence of adsorbed water in liquid or vapor form on SiO_2 and Si_3N_4 [14].

Microscale

Surface conductivity of a hydrophilic surface can somewhat be explained by proton diffusion (H^+), which has been studied via modelling and simulations of ab initio molecular dynamics (AIMD) [34, 35]. The

charge diffusion process on a wafer is driven by the concentration and electrical field gradients. The main diffusion mechanism of protons in amorphous SiO_2 has been related to cross-ring hopping, see in *Figure 2. 13* [36].

The figure shows silicon in yellow and oxygen in red. The white caps around the oxygen sites are the sites where a proton can access when excited by at most 0.4 eV from its equilibrium position. These sites are comparable to siloxane surface groups on a pristine thermally grown silicon oxide surface that form silanol groups when hydroxylated [37].

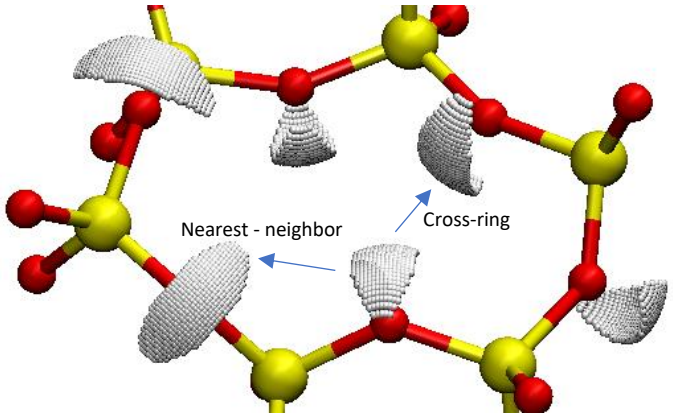

Figure 2. 13: Competitive proton hopping mechanisms in amorphous SiO_2. Si atoms are yellow and oxygen red. The white caps around the O atoms schematically delimit the regions accessible to protons. Cross-ring hopping is found to be the dominant hopping mechanism. On a surface, these caps would equal to the sites that form silanol groups from siloxane surface groups on a pristine thermal silicon oxide surface [37].

Simulations have also shown the importance of lattice vibration contribution to proton diffusion in dry conditions as it decreases the distance between the proton and another oxygen atom it might hop to. Literature states that proton diffuses from one oxygen atom to another when the distance between the two oxygen atoms is 2.3 Å. Typical distances between two oxygen atoms are typically 2.5-4 Å, indicating that both thermal energy and transition energy for structural relaxation is needed for proton hopping in dry conditions [37].

A typical hopping event of proton from O_I to O_{II} can be seen in *Figure 2. 14.* Before the hop, the proton is bonded to O_I with a bond length of about 1 Å, while O_{II} is far away. Then due to lattice vibrations the distance to O_{II} decreases and becomes about equal to O_I. The proton is then shared between the O atoms for about 0.1 ps (from 2.03-2.13 ps) forming the intermediate structure $O\text{-}H^+\text{-}O$. This ensues the breaking of the $O_I\text{-}H^+$ strong bond and the distance increases while the distance to O_{II} becomes about 1 Å. The breaking of $O\text{-}H^+$ strong bonds have been found in proton diffusion in water as well [37].

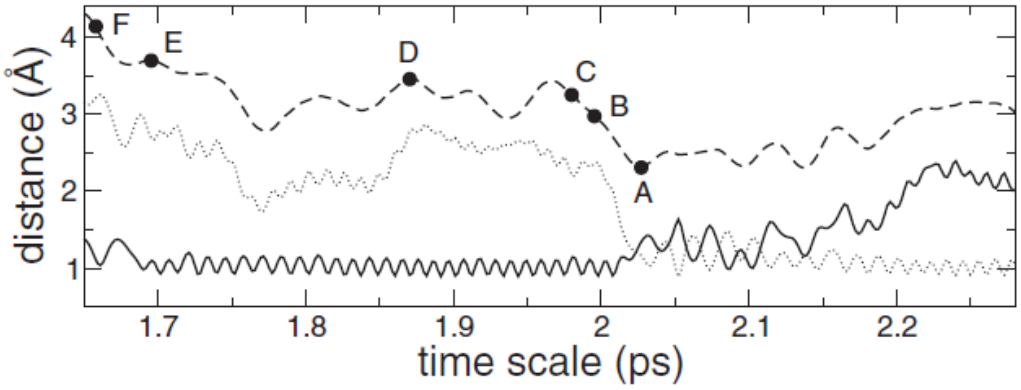

Figure 2. 14: Proton hopping between oxygen atoms O_I and O_{II}. It shows the evolution of O_I-H^+ (solid line), O_{II}-H^+ (dotted line), and O_I-O_{II} (dashed line) distances vs time. At first the proton is bonded to O_I and O_{II} is far away. Due to vibrations in the system, the distance decreases until the distance O_I-H^+ and O_{II}-H^+ is about the same and the proton is shared between the atoms until the O_I bond breaks [37].

The proton hopping that has been described here was in a simulation at elevated temperature, 1500 K. It is assumed that proton hopping would happen more seldomly in dry conditions at room temperature as the atoms would not have sufficient activation energy that was provided by thermal energy in literature [37].

In water the proton can hop between water molecules, which enables protons to diffuse much faster than other ions in water. Proton hopping is induced by the concerted multi-water molecule hydrogen bond rearrangement that occurs in pure water [34].

In a simplified physical picture, the fundamental event is a proton transfers in bulk water from a hydronium or Eigen cation (H_3O^+, $H_9O_4^+$) to another water molecule to which it is hydrogen bonded. The newly formed H_3O^+ ion then transfers a proton, which is not necessarily the same proton, to another water molecule [34]. A single proton hop studied within a quantum mechanics and molecular mechanics has been found to occur within 0.5 ps. Therefore, within water, the proton diffusion becomes faster compared to in the dry amorphous silicon oxide where it occurred after about 2 ps in elevated temperature [35]. Proton hopping in dry conditions at room temperature is therefore considered unlikely or a very slow process.

Proton diffusion at the interface of silica and water has also been studied. It found that many sites can be formed by proton diffusion at the interface, such as, Si-OH, H_3O^+, $SiOH_2^+$, Si-OH^+-Si. The lifetime of the H_3O^+ ion has a lower lifetime closer to the interface rather than in bulk water. Since the proton is able to hop between both the silicon oxide surface sites and between water molecules, the diffusion becomes much faster than in dry circumstances. Therefore, within a larger scale, the surface conductivity of a hydrophilic surface is increased with relative humidity or the presence of water [38].

Figure 2. 15 shows AIMD simulation of proton diffusion when an amorphous silicon oxide surface is exposed to water. Water is adsorbed to a silanol sites (a), a hydronium ion is formed, H_3O^+ (b), and a proton is exchanged to another water molecule that forms another hydronium ion (c). Finally, a new silanol site is formed from an active O^- ion site on the silica surface [38, 35].

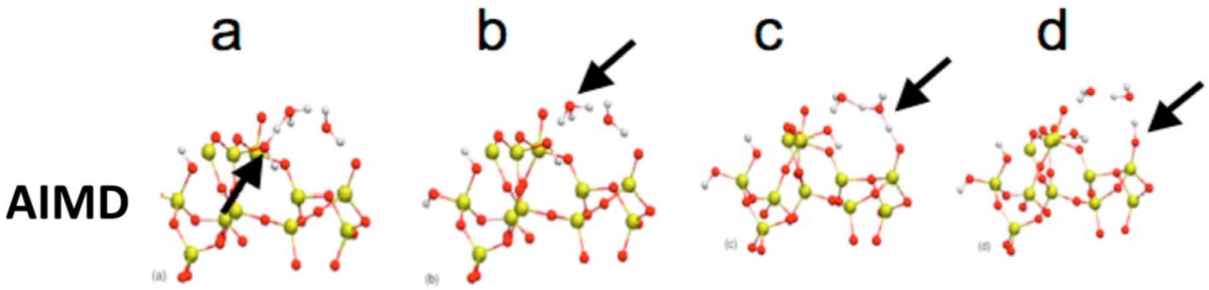

Figure 2. 15: Graph shows AIMD simulation of proton diffusion when surface of amorphous silica is exposed to water vapor. Arrows point to a silanol site where a water adsorbs to (a), a hydronium ion is formed H_3O^+ (b) with a proton exchange to another water molecule (c). In the last schematic (d), a new silanol site is formed [38].

Figure 2. 16 shows the proton diffusion on a charged and oxidized SiO_2 (left) and Si_3N_4 (right) surfaces when water adsorbs from the atmosphere. Schematic at t_5 shows the charged surface when the liquid from t_4 in *Figure 2. 10* has been removed and the surface is dry. Schematic at t_6 shows the proton diffusion mechanism when water from the atmosphere has adsorbed to the surface. A proton from a silanol or amine site can hop between water molecules that form hydronium ion until it finds an active Si-O^- or Si-NH_2 surface site it can react to. That is how the surface conductivity can be increased with relative humidity on hydrophilic surfaces. Proton hopping at room temperature in dry conditions is considered a slow process and is therefore does occur in the schematic.

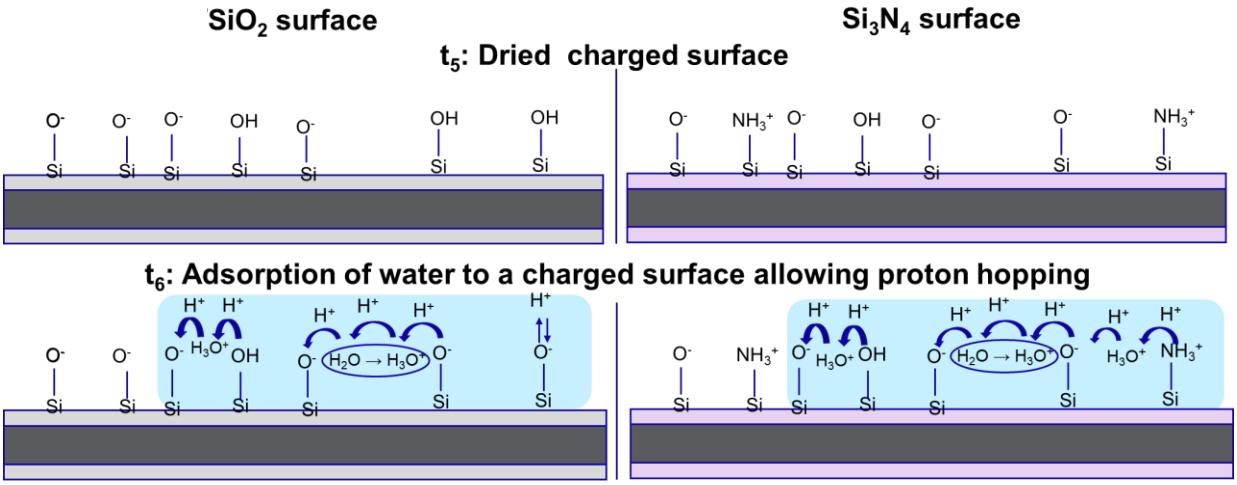

Figure 2. 16: Graph shows a simplified schematic of changes to oxidized Si/SiO_2 (left) and Si_3N_4 (right) the proton diffusion when water is adsorbed to a charged surface. The schematic at t_5 shows a dry charged surface from liquid flow over the surface at t_4 in Figure 2. 15. Schematic at t_6 shows the proton hopping mechanism from a silanol and amine site between 1-2 water molecules turned into hydronium atoms before bonding to another surface site [11, 15, 25, 26].

Macroscale

A model for surface conductivity has been proposed that assumes that surface conductivity is determined by the hopping of electrons/protons between adsorbed water spots across bare regions without adsorbed water [14, 13].

From that, an equation has been proposed that estimates the surface conductivity of SiO_2 as a function of relative humidity [14].

Equation 2. 5: Surface conductivity of SiO_2 as a function of Relative Humidity

$$\sigma = \sigma_0 \exp\left[-\alpha\left(\frac{1-h}{Ch}\right)^{0.5}\right]$$

Variable σ_0 is the surface conductivity of silicon dioxide in 100% RH, h is the relative humidity, α is a constant, which depends on electron mass, the diameter of the adsorbed spots and energy of the electrons on the silicon dioxide surface. Variable C is a dimensionless constant, which in previous studies has been determined to be in the range of 0.01-0.06 [14, 13].

The surface conductivity, $\sigma_{\square}$, of silicon oxide and silicon nitride is considered to be around $\sigma_{\square} = 10^{-12}\ S$ at 100% RH and are classified as electrical insulators. Figure 2. 17 shows the surface conductivity of SiO_2 vs RH based *Equation 2. 5* here above where all other variables are kept constant [14].

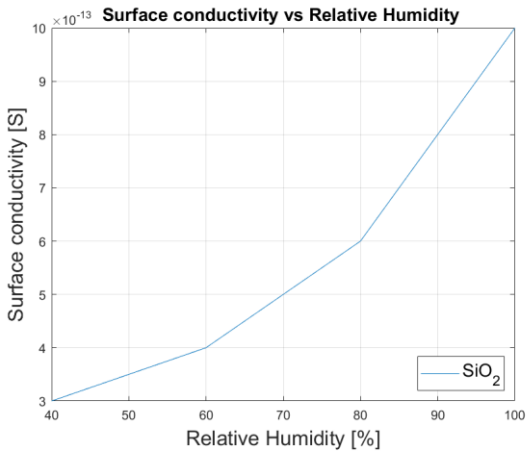

Figure 2. 17: Graph shows the modelled surface conductivity [S] of SiO_2 vs Relative humidity [%] where it is 10^{-12} S at 100% RH. All other factors in the model are kept constant [14].

2.5.5 Charge diffusion to a wafer table

Charge can be diffused to a wafer table when a charged wafer is loaded and clamped onto it. There needs to be a close proximity between the table and wafer backside and presence of water for proton diffusion.

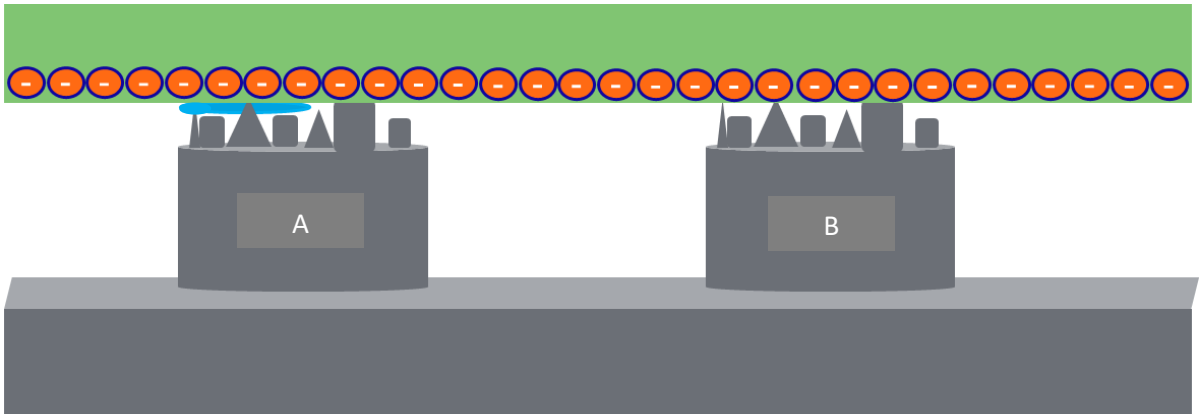

Figure 2. 18: Schematic of a charged wafer backside loaded on a WT with two outstanding pins visible, A and B. Though the outstanding pins are identical, there is no water presence on B. Therefore, charge dissipation can only occur on pin A to the asperities where water is present [37, 38].

Figure 2. 18 shows schematics of interaction happening over outstanding pins and their asperities when in contact with a charged wafer backside. The schematic on *Figure 2. 18* shows two identical outstanding pins, *A* and *B*, in contact with a charged wafer. As there is no water on *B*, the charge diffusion can only occur on *A*. The charge diffuses to the asperities that are in contact with water.

A silicon oxide or silicon nitride wafer will accumulate charge during a cleaning procedure with spin rinsing of water [12]. In humid environment these charges have a high surface conductivity on hydrophilic wafer backsides [14]. Hence, when the wafer is placed onto the wafer table, these charges diffuse over the wafer backside towards the asperities on the outstanding pins of the wafer table [21].

2.6 Reducing hydrophilic nature of a wafer backside

As aforementioned, the hydrophilic nature of silicon oxide and silicon nitride drive the conditions needed for charge generation and diffusion in humid conditions. Therefore, a proposed solution would be to modify the wafer backside to make it more hydrophobic. A hydrophobic surface is less likely to form surface charge when submerged in water and therefore less likely to generate charge during a spin rinse procedure. This is due to hydrophobic surfaces not having active functional groups that protonate or deprotonate when submerged in liquid, so no surface charge is formed [15].

On hydrophobic surfaces, water is less likely to be adsorbed. Hence, even when a hydrophobic surface is charged, the charges cannot diffuse over the wafer backside, as the charge transporting medium (water) is hardly present. With less water on the surface, the medium to transfer protons has been removed and the charge diffusion is prevented [21, 13, 14].

There are several ways to remove hydrophilic surface sites. An example is a baking step or thermal activation. At elevated temperature the silanol sites form strained siloxane sites, which becomes stable when the temperature exceeds 400 ^{o}C. This is, however, considered to be too energy consuming and might affect the IC quality on the wafer frontside. Therefore, it is not considered a viable option [2, 39, 25].

Another way to remove silanol sites is with hydrofluoric acid (HF) etching, which is known to remove native oxide. The silanol sites are replaced with Si-F and Si-H sites. The downside is that HF would etch away native oxide and continue to etch the thermally grown silicon oxide. The effect is also not permanent in atmospheric conditions and silanol sites will reform on the surface with adsorption of water. Furthermore, HF is a highly toxic and a hazardous material, which would increase the hazard involved in wafer processing [22, 40, 41].

Surface modification can also be done by deposition of numerous types of molecules that generally have a similar structure. They are constructed with a functional group -*R* that controls the surface properties, an anchoring molecule that bonds with the surface and an active group that during the deposition will react or dissociate as a byproduct. The types of molecules considered the best option for a surface covered in silanol sites are silanes, molecules with silicon as anchoring groups, and alkynes/alkenes, with double-bonded carbon as anchoring groups. An example of a silane can be seen on *Figure 2. 19*. A typical silane has a functional group -*R*, anchoring atom Si bonded to the -*R* group, sometimes with an organic linker and bonded to the three active sites that will hydrolyze [42]. Silanes and alkynes/alkenes have the best adhesion compatibility with silanol covered surfaces. However, alkyne/alkenes are mostly deposited via irradiation while common deposition methods in the semiconductor industry is spin coating or chemical vapor deposition (CVD). Silanes are the molecules most studied with regard to adhesion to Si-OH covered surfaces and have known compatible deposition methods to the wafer processing with CVD [43].

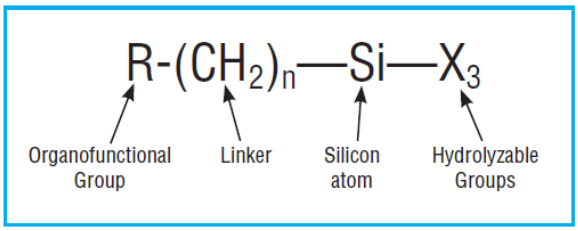

Figure 2. 19: An example of a silane that can be used to modify a surface. It has organofunctional group R that controls the properties, an organic linker $(CH_2)_n$, silicon base/anchoring group and an active or in this case a hydrolysable group that will react during deposition [42].

The surface modification of a wafer backside with hydrophobic monolayers from silanes is therefore considered the preferred method and molecule than the others. It produces a hydrophobic surface that stays hydrophobic instead of reverting back to hydrophilic silanol sites, it consumes less energy than a baking step at temperature above 400 ^{o}C and does not introduce similar hazard as etching with HF might. Furthermore, deposition via CVD is a known method within the semiconductor industry to introduce layers on the frontside of wafers so would be relatively easy to implement on a wafer backside without high risk of compromising the quality of the product on the frontside [21].

2.7 Silanes of interest

Two types of silanes are considered of interest, hexamethyldisilazane (HMDS) $[(CH_3)_3Si]_2NH$, where the functional group of the molecule is trimethyl silyl (Si-$[CH_3]_3$), and a precursor where the functional group is a non-disclosed and an unknown fluoropolymer, (C_xF_y).

A known deposition method is by CVD where HMDS and the fluoropolymer is used as a precursor. The precursor is hydrolyzed so the active groups form silanol groups on the molecule. The hydrolyzed molecule then reacts with the already hydrolyzed surface covered in silanol groups during condensation and forms a covalent bond. The deposition of a fluorocarbon molecule is shown on *Figure 2. 20* [44]. The deposition of HMDS is similar except that the reaction happens in two steps since the molecule is branched and each side reacts with a surface site.

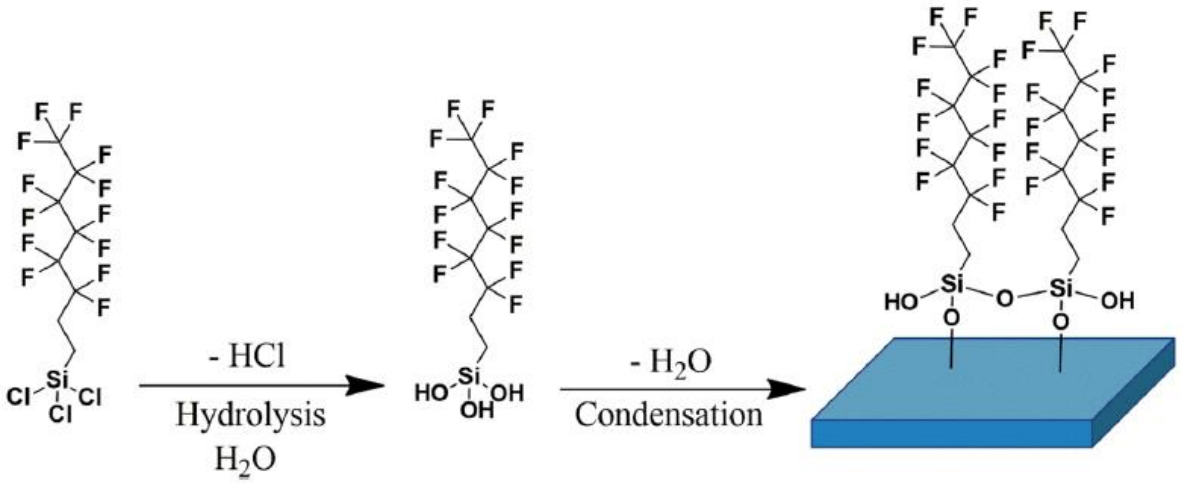

Figure 2. 20: Schematic of a fluoropolymer reacting to oxidized surface. The active sites are hydrolyzed creating hydrochloric acid byproduct, then during condensation the hydrolyzed surface sites bond with the -OH groups of the molecule with water as byproduct [44].

HMDS is already used in the semiconductor industry to reduce hydrophilic properties of a wafer front-side before a photoresist is deposited. Photoresist does not bond well with hydrophilic surfaces, so a HMDS monolayer is deposited [17]. This monolayer is already incorporated into the semiconductor industry so its properties and interaction with the wafer backside materials is somewhat known, and it will not introduce any unknown risks to the processing on the frontside.

HMDS deposited by Liquid Phase Deposition (LPD) on SiO_2 has been found to decrease surface conductivity of SiO_2 by a factor for 1000. The change in surface conductivity when HMDS is deposited via CVD on Si_3N_4 is now known. It can be identified as a knowledge gap but it is assumed the reduction will be similar [17, 14].

Fluoropolymers, F-SAM for example, are known for being very hydrophobic, with low conductance, chemically inert and with excellent tribological properties that could improve the mechanical interaction between wafer backside and WT during loading and clamping [16].

Fluoropolymer brushed silicon surfaces deposited with Surface-Initiated Atom Transfer Radical Polymerization (SI-ATRP) have lower adhesion pull-off force and friction coefficient as the fluorination of the molecules attached to the surface increases [45]. It is assumed that fluoropolymer monolayers of coupling agent also have a low friction coefficient and adhesion pull-off force as is common with most fluoropolymers [46, 47].

As aforementioned, the focus of this study is changes in electrical properties of a wafer backside. To estimate the overall changes and interaction with surrounding components, a separate study was done on tribological properties, to relate to the mechanical interaction. Both monolayers showed significant improvement in adhesion and friction to a clean silicon sample. The mechanical interaction has therefore been de-risked prior to study on charge diffusion.

A study was conducted on hydrophobic SAMs deposited on SiO_2 gate between source and drain in an organic field-effect transistor. The molecules used within that study were $(CF_3)(CF_2)_7(CH_2)_2Si(OC_2H_5)_3$, $(CH_3)(CH_2)_9Si(OC_2H_5)_3$ and $(NH_2)(CH_2)Si\ (OC_2H_5)_3$ and were referred to as F-, CH_3, NH_2-SAM. On top of the SAMs a semiconductor was deposited so the drain current of the transistor could be measured as a

function of the gate bias to estimate the threshold voltage. After the test, the semiconductor was subsequently peeled off. The local surface potential of the monolayers was measured with a scanning Kelvin-probe microscopy (SKPM) before and after the semiconductor was deposited and after it was peeled off [36].

The local surface potential profiles of the SAMs can be seen in *Figure 2. 21*. The figure shows the surface potential of the monolayers before (A) and after (B) the drain current measurements. The slight misalignment around the edges of the graphs (at distance < 0 µm and > 10 µm) can be related to an effect of the source and drain. Before the semiconductor was deposited, the local surface potential was in the range of 1 V. CH_3-SAM had a local surface potential of 0 V while F-SAM had about -1 V and NH_2-SAM had a potential of about 1 V. The local surface potential of F-SAM and NH_2-SAM was theorized to be due to a possible dipolar contribution of the ordered molecules vertical to the surface since N-H and C-F bonds are polar and C-H is not [48]. After the drain current measurement, the CH_3-SAM remained unchanged and uncharged with no profile while F-SAM and NH_2-SAM local potential had both shifted and generated a large profile with a peak in the largest distance from the source and drain. The study showed that a fluorinated surface can generate a negative surface potential, a site with NH_2 surface sites will charge positively as described earlier and that the CH_3-SAM covered surface might not generate a potential [36].

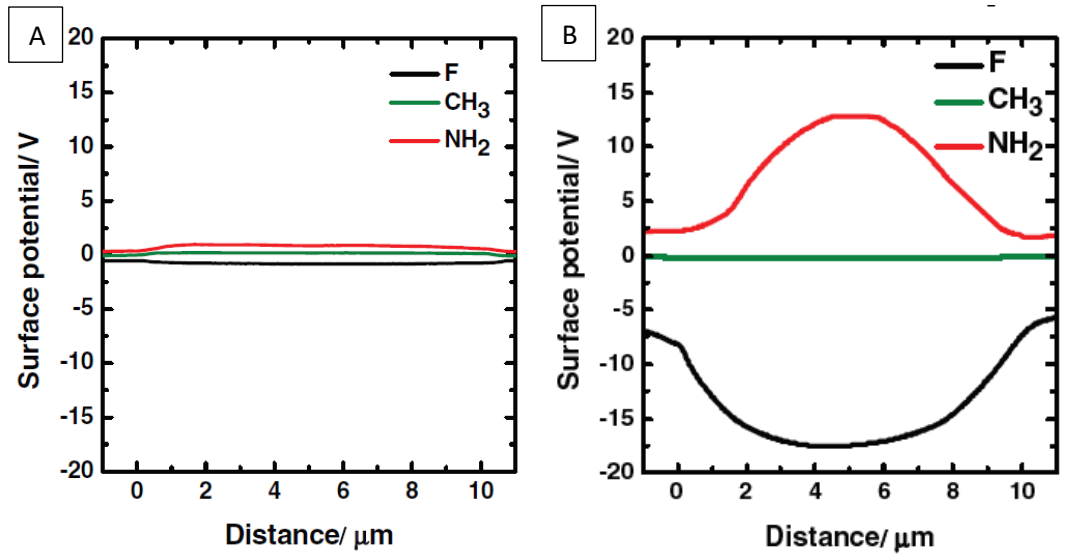

Figure 2. 21: Graph shows the local surface potential of F-SAM, CH_3-SAM and NH_2-SAM before (A) and after (B) the SAMs had been used as gates in a transistor. The misalignment at the edges is likely due to the interface with the source and drain in the transistor structure. The figures show the F-SAM and NH_2-SAM have a shifted potential profile before being charged that increases significantly when they have been charged as a part of the transistor. In contrast, the CH_3-SAM has no profile both before and after the drain test [36].

How a fluorinated modified surface might generate a surface potential from a spin rinse tool and how the surface conductivity will change due to the modification is unknown and can be identified as a knowledge gap.

Literature on how the modification and change surface sites will affect proton hopping is unknown and can be identified as a knowledge gap.

It is expected that the HMDS and fluorinated molecule will block out the silanol sites that deprotonate and hinder proton diffusion. The expected change in charge generation from liquid flow or wet spin rinse on a Si_3N_4 surface can be seen in *Figure 2. 22.* It shows the highly oxidized Si_3N_4 surface (left) and a modified

Si_3N_4 surface where HMDS has been deposited on the surface, replacing two silanol sites (t_2 and $t_{2.5}$). Schematic at t_3 shows the surfaces submerged in DIW. The silanol sites deprotonate and the amine sites protonate but the trimethylsilyl sites do not interact with the protons resulting in lower surface charge on the modified surface. At t_4 the liquid starts flowing over the submerged surface and protons diffuse in the direction of the liquid flow. The current flow is smaller on the modified surface due to less surface sites to provide protons to the water. The water is then removed, and the surface is dry at t_5 leaving the surfaces charged where the modified surface is less charged than the unmodified one.

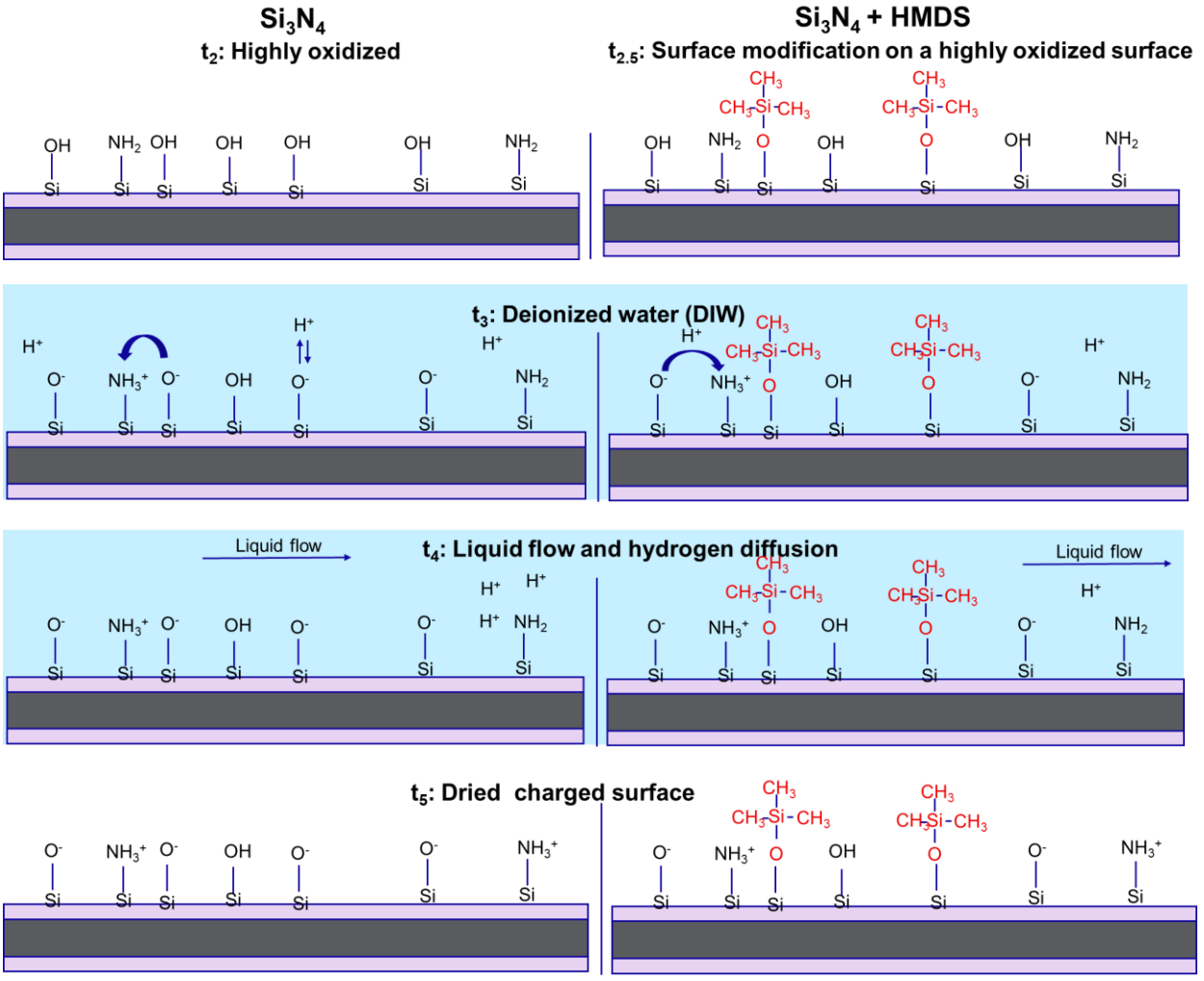

Figure 2. 22: Schematics show the difference in charge generation via liquid flow over a surface on a highly oxidized Si_3N_4 surface and a modified Si_3N_4 with HMDS surface. At t_3 the surfaces are submerged in DIW where the hydrophilic surface sites protonate or deprotonate. The trimethyl silyl groups do not react with the water, reducing the total surface and streaming potential generated with liquid flow. Therefore, the modified surface should charge less than the unmodified one (t_5) [11, 15, 36].

Figure 2. 23 shows how the proton hopping should be reduced on the modified surfaces with HMDS in comparison to the unmodified Si_3N_4. The surfaces are charged from the liquid flow on *Figure 2. 22* at t_4. When water is adsorbed to the surface, t_6, the hydrophilic surface sites react with the water again and protons start to hop between water molecules, forming hydronium ions (H_3O^+), and active surface sites. The pink proton on the unmodified surface can hop between several surface sites. This is limited on the modified surface where a silanol has been replaced by a trimethyl silyl group, which blocks the proton from diffusing

further. The green proton is also limited by the modification and cannot diffuse to any surrounding silanol sites.

Figure 2. 22 and *Figure 2. 23* show how the charge generation and migration will be limited by the modification in theory.

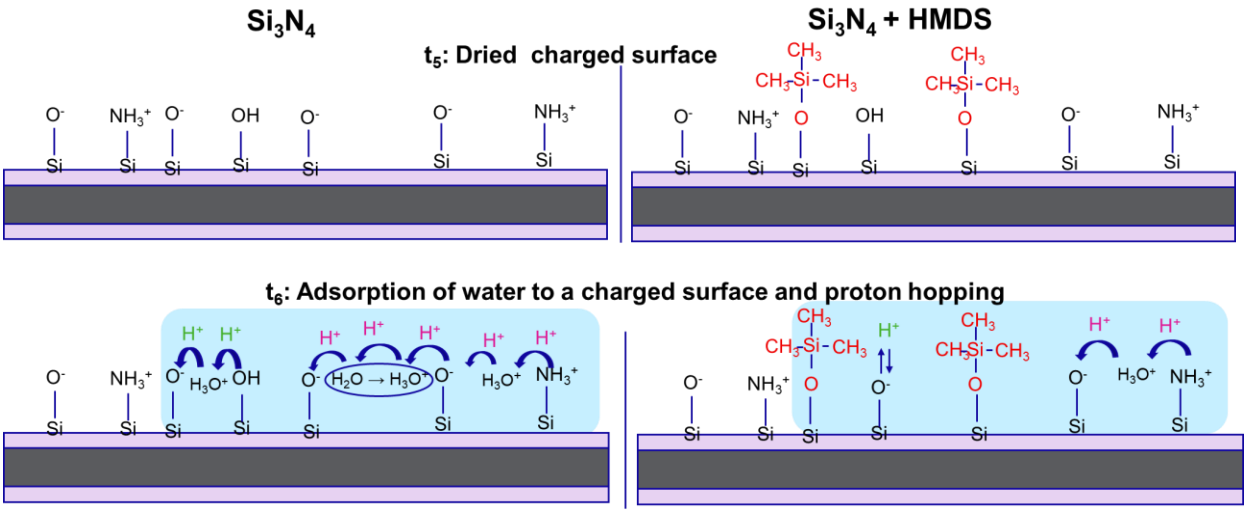

Figure 2. 23: The schematics show the difference in proton hopping on an unmodified charged and oxidized Si_3N_4 surface and a modified Si_3N_4 with HMDS. The surfaces are charged, t_5, from the liquid flow. When water adsorbs from the atmosphere, t_6, proton hopping occurs between active hydrophilic sites. The pink proton on the unmodified surface can hop between several hydrophilic sites but the hopping is reduced on the modified surface due to the trimethyl silyl groups. The proton cannot hop any further. The green proton can also not hop between any surface sites as it is surrounded by hydrophobic inactive sites. Charge diffusion over the surface is therefore limited on a modified surface [34, 35, 38, 36].

2.8 Research objective

In this master thesis, HMDS and a non-disclosed fluorocarbon polymer monolayers are compared when deposited on bare Si and Si_3N_4, see *Figure 2. 24*. They are compared by characterization tests whose results will be related to their estimated performance with regard to charge diffusion to surrounding components, especially the wafer table, and to fill in the identified knowledge gaps.

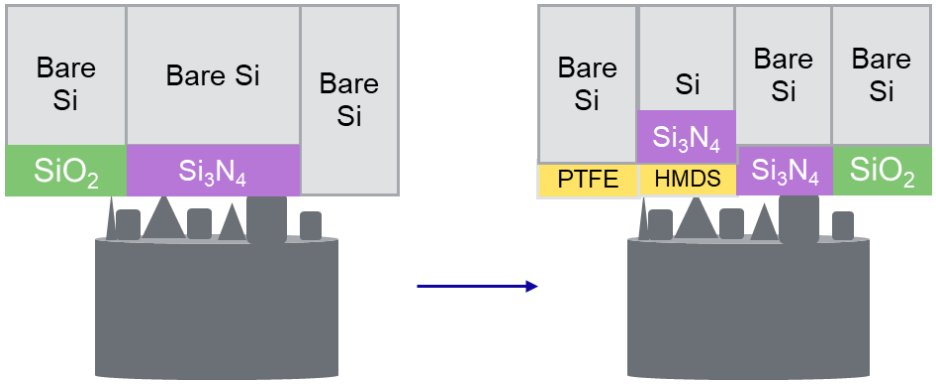

Figure 2. 24: The proposed solution and research project entails depositing HMDS and fluoropolymer monolayers on bare Si and silicon nitride wafer backsides

The following research questions have been proposed:

1. How will surface charge and potential generation on modified wafers differ from the unmodified wafers and how can it be related to the properties of the monolayers?
2. How will the surface conductivity change on modified wafers in comparison to unmodified surfaces and can it be related to the properties of the monolayers?
3. Are there any risks introduced into the photolithography process with the surface modification?
4. Which wafer backside material is considered the best choice and why?

The characterization includes measuring surface free energy (SFE), surface chemistry, wear resistance, surface charge formation from a wet spin rinse process, surface conductivity and estimation of charge diffusion from backside to WT. Characterization will be related to the performance of the different wafer backsides with regard to charge diffusion to surrounding components.

3. Experimental Details

This section discusses the specimen used, experiments and experimental setup for the characterization of the monolayers.

3.1 Specimen

Figure 3. 1 shows a cross-section of the structure of the thin films deposited on the samples used within the study. The substrates were bare Si (grey) and bare Si with a 60 nm Si_3N_4 layer (purple) deposited by LPCVD. The bare Si wafer samples had a 50.8 mm diameter and the bare Si with Si_3N_4 (60 nm) samples had a 300 mm diameter.

The wafers were stored in atmospheric conditions at 21 ± 2 °C and 40% relative humidity (RH). The auto-oxidation of silicon nitride and silicon is included in the schematic as native oxide (green) in *Figure 3. 1* (green). The monolayers were deposited by CVD at an elevated temperature. The deposition of the fluoropolymer took ten times longer than the deposition of HMDS.

The fluorocarbon- based monolayer will be referred to as F-SAM.

For comparison reference samples were used without the monolayers for characterization.

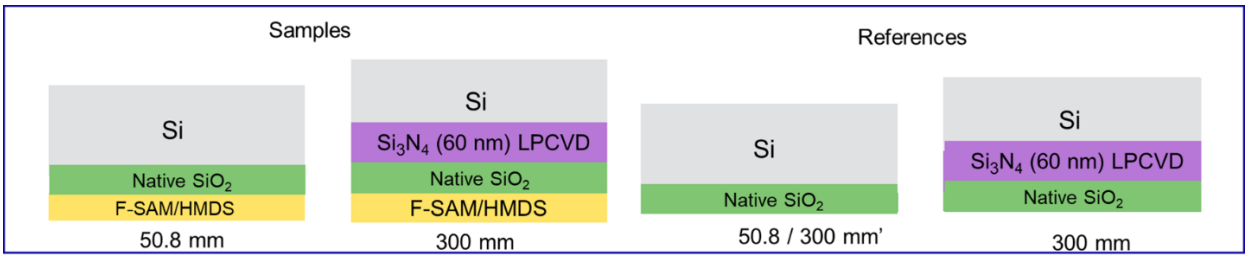

Figure 3. 1. A schematic of the cross-section of the structure of coatings on samples used. The base for all samples and references is bare Si. One type of specimen was 50.8 mm in diameter and the other 300 mm in diameter. The 300 mm diameter specimens had a 60 nm Si_3N_4 LPCVD dielectric (purple). It is assumed that a native oxide layer has formed from storage in atmosphere (green). HMDS or fluorocarbon monolayers were deposited on the samples (yellow) to be characterized with the references for comparison. The layer thickness is not up to scale.

Figure 3. 1 shows a homogenous structure of the thin films while in might not be as homogenous, and uniform as seems. The layers are not up to scale. The expected surface sites of the modified surface (right) and the unmodified reference (left) can be seen in *Figure 3. 2.*

The passivation layer prior to deposition has formed where water has adsorbed to the surface and is uneven or scattered over the surface. During the deposition of the monolayers, the precursor molecules are hydrolyzed in proximity to the surface. The hydrolysis results in acceleration in formation of a native oxide on the surface, which is also necessary for the deposition as the hydrolyzed precursor molecules react with the silanol sites on the surface [42].

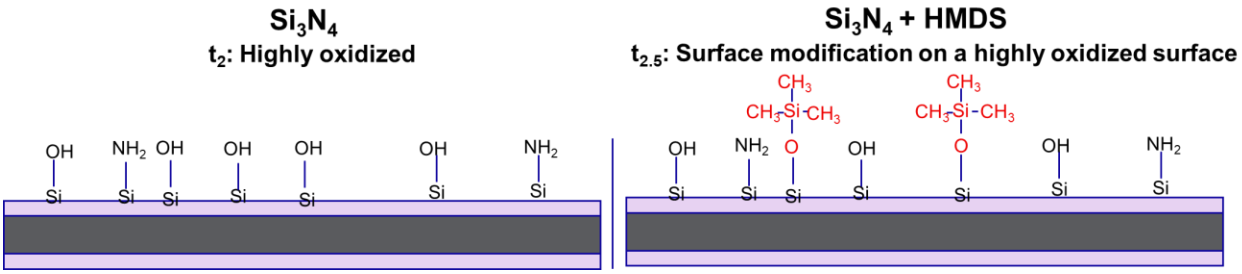

Figure 3. 2: The surface sites expected to be present of the surface of an unmodified Si3N4 and modified surface after deposition of HMDS (right). The unmodified surface is considered to be covered in silanol sites with some residual amine sites while the modified surface has silanol, amine and modified surface sites (this case trimethyl silyl) that has replaced some silanol groups.

The substrates, Si and Si_3N_4, can have different interaction with the monolayers. The bare Si has lower roughness than Si_3N_4 and only has silanol surface sites, which is easier to study than a surface with two types of surface sites. However, silicon nitride is more widely used in IC fabrication, so it is considered more relevant to study silicon nitride substrates.

The bare Si specimens were provided by the supplier. History of specimen, surface treatments and properties were not provided. Their state of oxidation and possible contaminants adsorption is therefore unknown.

3.2 Single wafer wet spin toolset

As aforementioned, a single wafer wet spin toolset has become a critical part in IC fabrication and is commonly constructed of a rotating wafer and liquid dispense. The setup used in this study is similar to the schematic seen in *Figure 3. 3 (left)* but the water is dispensed on backside where the wafer is held by a chuck [30, 49]. Only deionized water (DIW) was used, and it was dispensed at around 80 mm radius.

The potential can then be mapped out by an electrostatic voltmeter (ESVM) that gives a surface potential profile as can be seen in *Figure 3. 3 (right)*, which shows a charged hydrophilic wafer. Potential peaks form at 80 mm radius since the water comes in contact there and the profile spreads to the edges with the water flow. The center is not charged as no water comes in contact there and can act as a baseline.

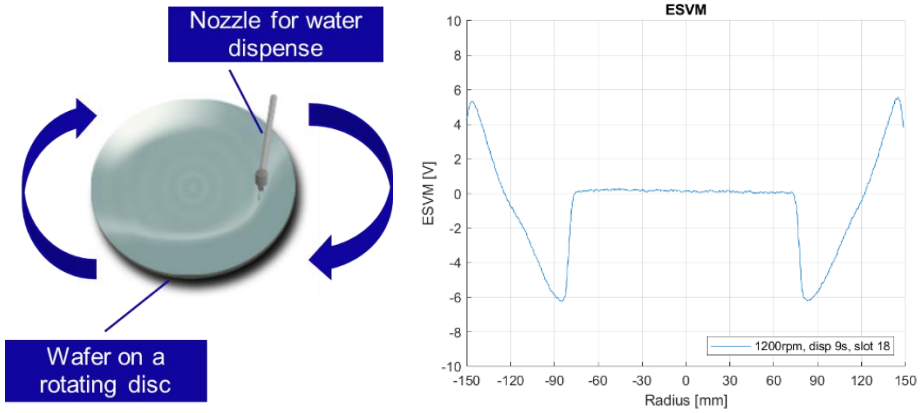

Figure 3. 3: A simple schematic of a wet wafer spin procedure (left). The liquid is dispensed at 80 mm radius from the center [49]. The surface potential profile is mapped with an ESVM (right), showing a peak where the water comes in contact with the surface while the center is not charged.

The spin rinse tool used was solely for 300 mm wafers. For a study with a wet spin rinse tool, only the silicon nitride wafers were used.

3.3 Experimental methods and setup

The properties that need to be studied to determine the quality of a coating and its performance were mentioned in the previous chapter and are surface chemistry, surface free energy, wear resistance, and electrical properties that include zeta potential, surface charge, surface conductivity and charge diffusion from wafer backside to the wafer table.

Samples used in each characterization test can be seen in *Table 3. 1*.

Table 3. 1: Listing of samples used, the characterization they underwent and their sample history.

Samples	Characterization	Sample history
Bare Si reference	Surface Chemistry, Surface Free Energy, ζ-potential	Unused, stored in atmosphere for unknown time with increased hydrocarbons
Bare Si + F-SAM		Unknown
Bare Si + HMDS		Unknown
Si_3N_4 reference	Surface Chemistry, Surface Free Energy, ζ-potential, Wear study, Charge study, Surface conductivity, Charge diffusion	Unused, stored in atmosphere for several months
Si_3N_4 + F-SAM		Unused, hydrolyzed deposition and storage for several months.
Si_3N_4 + HMDS		Unused, hydrolyzed deposition and storage for several months.

3.3.1 Surface free energy (SFE)

Contact angle measurements were carried out to estimate the Surface Free Energy (SFE) and general affinity to water. Measurements were done with a Krüss Mobile Surface Analyzer (MSA) where di-iodomethane (DIM) and DIW droplets of 1 mL came in contact with the surface of the sample and the contact angle measured. The device can be seen in *Figure 3. 4* [50]. The Owens, Wendt, Rabel and Kaelble (OWKR) method was then used to estimate the SFE [21, 51].

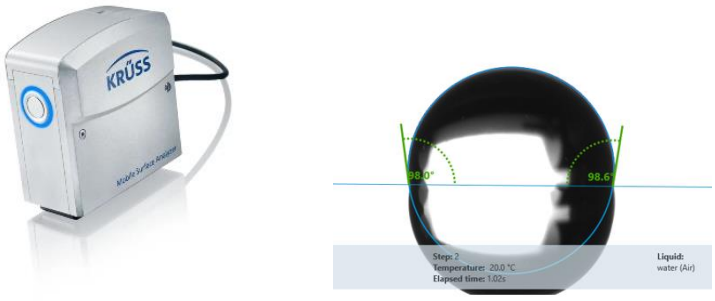

Figure 3. 4: Krüss Mobile Surface Analyzer (left) and a contact angle measurement from the device (right) [50].

Contact angle with water when HMDS has been deposited on Si, SiO_2 and Si_3N_4 via CVD has been measured in the range 65-75° where the temperature and deposition time was unknown [52]. The contact angle with water has been found to be in the range of 86°-112° when fluorinated self-assembled films were deposited on a Si substrate [53].

3.3.1 Surface Chemistry with XPS

X-ray Photoelectron Spectroscopy (XPS) was done to estimate surface chemistry, coverage, quality of coating on an unused wafer [54]. A simple schematic of the XPS analysis can be seen on *Figure 3. 5* [55].

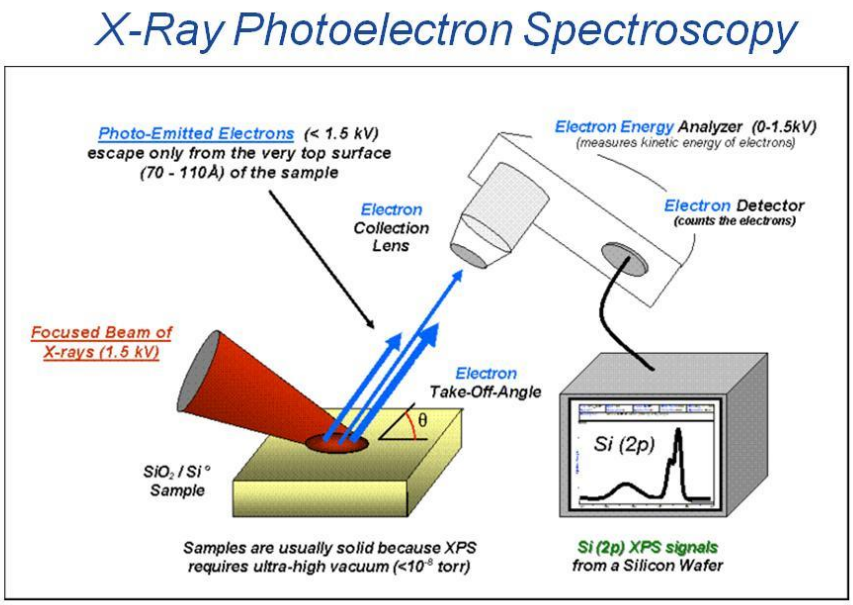

Figure 3. 5: Simplified figure of XPS. A surface is scanned with X-rays that hit atoms and generate photo-emitted electrons. Only electrons generated in the first few atomic layers are detected. The energy of the detected photoelectrons is analyzed and provides both elemental and chemical information of the surface.

During sample preparation, the wafer specimens were broken into smaller pieces of maximum size 1x1 cm^2, rinsed with isopropanol, dried and stored within aluminum foil to minimize accumulation of contaminants. Prior to sample preparation the samples were stored in atmospheric conditions.

The locations where the XPS was conducted can be seen on *Figure 3.6*. Two points were measured on two locations on the bare Si specimen, the center and the edge. Two points on nine locations were measured on the 300 mm samples. Four locations at equally distributed distance from the edge and other four at equally distributed locations at the midpoint from the center to the edge. The ninth location was the center itself.

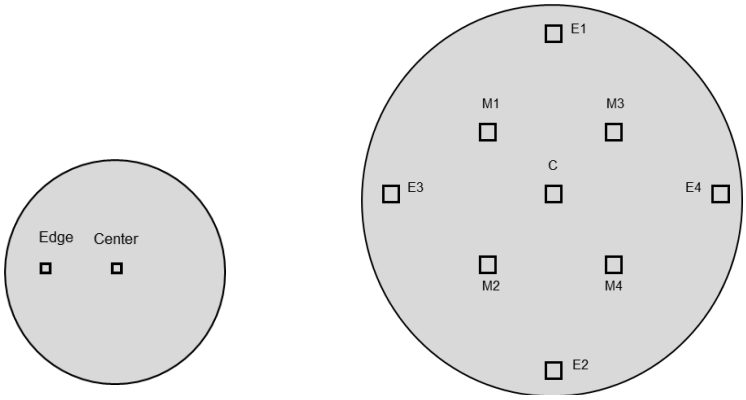

Figure 3.6: On bare Si two points were measured on two specimens at the center and in the edge/midpoint. On the 300 mm sample, two points were measured on four specimens at similar distance from the center such as at the edge (E1, E2, E3 and E4) and middle (M1, M2, M3, M4). Two points were measured at the center.

The measurements were conducted in Quantera Hybrid from ULVAC-PHI (Q1) and performed using monochromatic AlKα-radiation (100 W) at a takeoff angle, Θ, of 45 °. The angle range is 25-65°, which affects the accuracy from the exact location where the signals come from. At 45°, the information depth is up to 7 nm and a spot of 100 µm was scanned across an area of 1200 x 500 µm. Apparent concentrations were derived by quantification of the peak areas and normalizing the total sum of all elements to 100 at%. The results were then used to estimate the thickness of each layer present in the 7 nm depth. The elements of interest were Carbon C, Fluor (F), Nitrogen (N), Oxygen (O), Silicon (Si), and Zinc (Zn) [56, 57, 58].

3.3.3 Wear resistance

To estimate the quality and wearability of the monolayers, the wafers were rinsed by a wet spin rinse procedure that includes scrubbing and polishing. This procedure is considered the harshest conditions the wafer might go through where it is most likely that the monolayer might wear off. Therefore, the wear resistance test was defined as whether the monolayer would alter or be removed after being processed with this scrubbing and polishing procedure. [33].

The changes before and after the harsh rinsing was estimated by measuring SFE and conducting an XPS surface analysis on the hydrophobic modified wafers before and after processing. This setup was only available for 300 mm wafers, so the test was only performed on the 300 mm wafers with Si_3N_4 layer.

3.3.4 Zeta potential measurements

Zeta potential measurements are conducted similarly as shown in *Figure 2. 9* [59]. A streaming potential is generated over a surface by a liquid flow and measured with a voltmeter. The zeta potential can then be calculated with *Equation 2. 4*. It is also possible to measure the streaming current from the liquid flow and calculate the zeta potential similarly [11].

The zeta potential was measured with SurPASS 3 instrument, see in *Figure 3. 7*, in a standard electrolyte solution 1 mM KCl. Acid 50 mM HCl and base 50 mM KOH were used to adjust the pH in the range of pH 2-7. The electrolyte solution was purged with Nitrogen gas at 6 bar to prevent dissolution of carbon dioxide. A pH scan was performed on all samples to estimate the IEP of the samples, that is, the pH level where the zeta potential is zero. [60].

The IEP of the surface of the wafer backside material can be related to the pH of the rinsing fluid used in a wet wafer spin rinse. If the pH of the rinsing fluid is lower than the IEP of the surface, positive charges appear of the wafer backside. But if the rinsing fluid has a pH above the IEP, then negative charges appear on the wafer backside.

Figure 3. 7: Surpass 3 instrument [59].

3.3.5 Surface Charging and Conductivity

Surface charge and generation of streaming potential was studied by charging the wafers by a spin rinse process with DIW and the profile was mapped with an ESVM, see **3.2 Single wafer wet spin toolset** [12, 33].

The available spin rinse modules were designed for wafers with diameter 300 mm. Therefore, the charge study and surface conductivity estimation were conducted and calculated for the 300 mm wafer specimens with 60 nm Si_3N_4 layer.

Surface conductivity was estimated by charging wafers with a spin-rinse process and doing repeated ESVM measurements for 2 weeks at day 0, 1, 2, 7 and 14. The change in charge profiles between days estimates the movement of charge as a function of time. Between measurements the wafers were stored in atmospheric conditions at 21 ± 2 ^{o}C and RH 40 %.

3.3.6 Wafer table current measurements

An experimental setup was used to estimate the amount of charge dissipated through a WT when a charged wafer is clamped on a wafer table. This setup measures the current a charged wafer that is discharged onto the wafer table. In the setup, the discharging parameters can be studied, for example, the clamping time, the relative humidity, the type of a wafer backside and type of the wafer table. This study focuses on charge diffusion of different wafer backsides, and their discharging towards the wafer table.

The process of the WT current measurements can be seen on *Figure 3. 8*. A wafer with a specific backside is charged by a spin rinse. The surface potential profile is measured with the ESVM. The wafer is then placed on the setup where it is clamped on a WT. The current is then measured until it seems to saturate, or the signal becomes stable. Optional is the setting for the relative humidity: Humid air is provided on the setup to ensure uniform RH up to ~90%. The wafer is then unclamped, and post-voltage mapping is done with the ESVM to get the change in the surface potential profile before and after the wafer has conducted current to the WT.

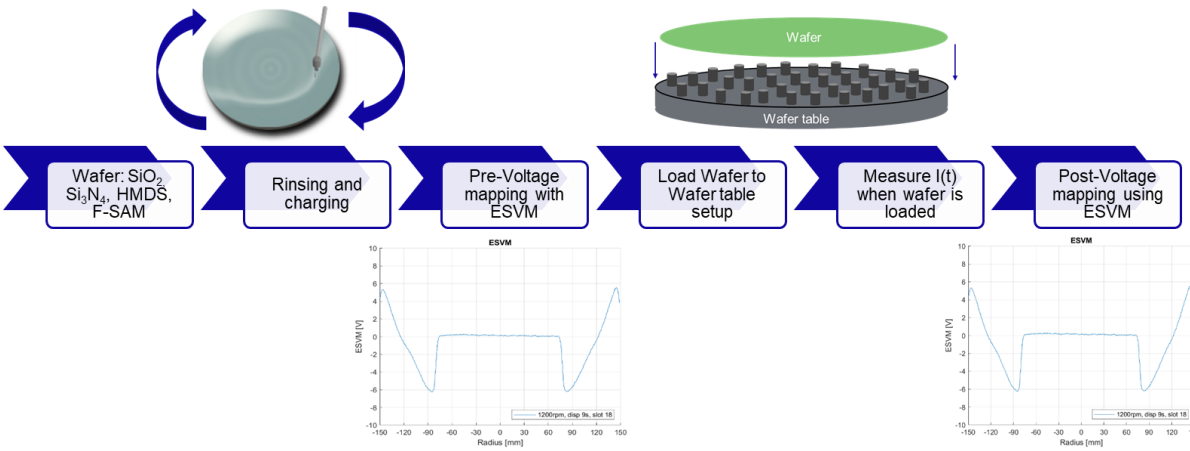

Figure 3. 8: The process of a WT current measurement. Wafers are charged with a spin rinse and the charge is measured with an ESVM. The charged wafer is then placed upon a setup that measures the current flowing from the wafer and through the WT as a function of time. Afterwards the charge profile is measured again with the ESVM, mapping the difference in profile before and after the setup.

Due to lack of wafers with F-SAM and HMDS monolayers, the wafers were placed and clamped on the WT twice for measurements to check reproducibility. *Table 3. 2* shows how the wafers were charged with the spin rinse each time they were clamped.

Solely the absolute value of the total charge diffused was used to compare the performance of different wafer backsides.

Table 3. 2: Wafers used and charging conditions for the WT current measurements.

Wafer type	Wafers	Clamp 1 – Spin Rinse w. 2400 rpm	Clamp 2 – Spin Rinse w. 2400 rpm	WT current measurement
Repeatedly used Si_3N_4 (60 nm)	1	1 x 30 s	-	1x
New Si_3N_4 (60 nm)	1	2 x 30 s	2 x 30 s	2x
HMDS + new Si_3N_4 (60 nm)	1	2 x 30 s	0 x 30 s	2x
F-SAM + new Si_3N_4 (60 nm)	1	1 x 30 s 1 x 16 s	2 x 30 s	2x

4. Results

4.1 Surface free energy (SFE)

The SFE was measured by contact angle measurements with DIM and DIW. OWRK method uses dispersion and polar terms of these liquids to estimate the SFE [61, 62, 63] [21]. *Figure 4. 1* shows the contact angle measurements with DIW (A) and DIM (B) droplets.

A 'clean' bare Si 300 mm wafer was included to provide a better comparison. The difference between 'dirty' and 'clean' refers to the amount of hydrocarbons or contaminants that might have adsorbed to the surface. Hydrocarbons are present in the atmosphere and can adhere to surfaces. Hydrocarbons generally have hydrophobic properties due to low polarity or symmetry of molecule, which increases the contact angle (CA) when they adhere to a surface.

The graph shows substantial difference in affinity to water. As a standard reference, an Ultra Violet (UV) ozone cleaned reference wafer with no monolayer has 100% Si-OH groups. Therefore, it has a contact angle of 0^{o}, and shows high affinity to water. For a slightly contaminated reference where hydrocarbons from the atmosphere have adhered to the surface, the contact angle increases slightly as is seen on the clean Si and Si_3N_4 references up to values of CA around 40^{o}.

The sites of Si and Si_3N_4, silanol and amine sites, want to adhere to surrounding molecules and water. The contact angle increases significantly with the 'dirty' Si, which was stored in conditions with higher number of hydrocarbons. The CA measurements of HMDS coated samples are in the same range as the dirty bare Si since the trimethyl-silyl sites that are deposited are similar to hydrocarbons from the surroundings that adhere to the surface. The F-SAM samples have the highest contact angle with water as was expected due to the strong hydrophobic natures of fluorocarbons.

The CA of HMDS on Si_3N_4 is around 66^{o}, which is within range found within literature [52]. It is possible that the number of hydrophilic amines on the surface might reduce the contact angle in comparison with a bare silicon or silicon oxide.

F-SAM is classified as a material with a strong, hydrophobic surface. The CA of F-SAM 100^{o}-110^{o} on both substrates. The CA is in the range found in literature [53] [64].

The CA with DIM shows a similar trend but with lower variations between monolayers and substrates, especially from the clean samples. DIM is a nonpolar liquid, so the sole contribution of polar terms is introduced by water terms.

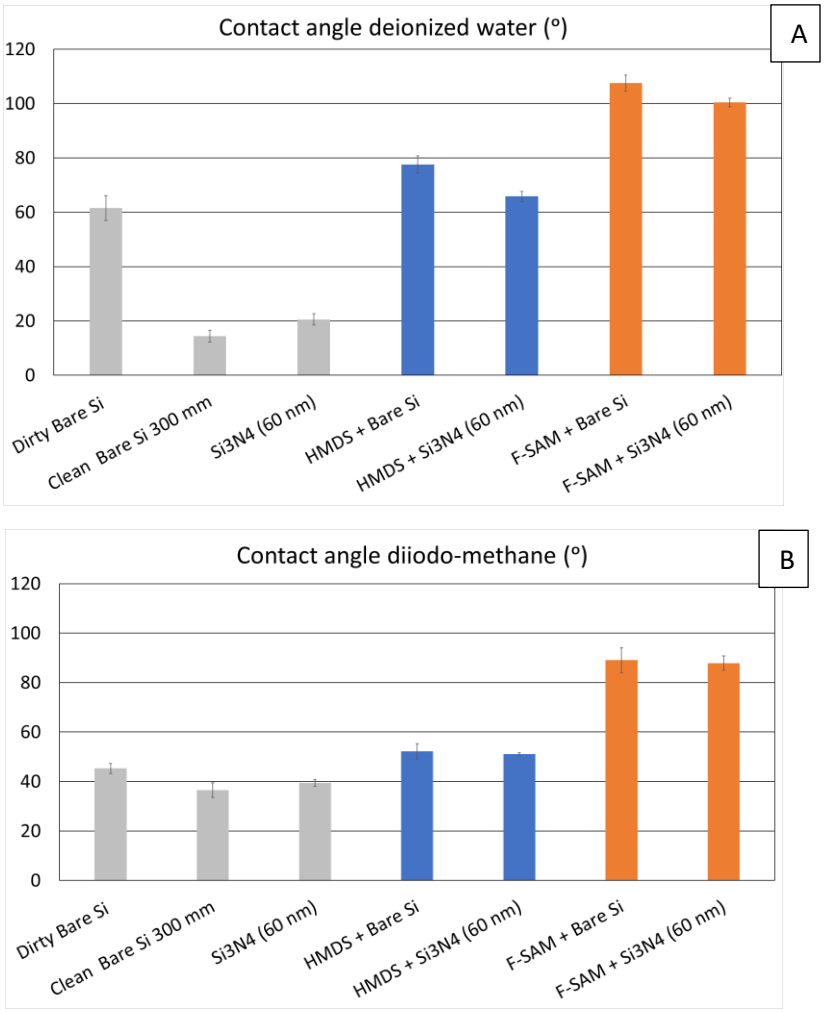

Figure 4. 1: Contact angle measured with DIW (A) and DIM (B). Clean references Si and Si_3N_4 have the lowest CA with minimum hydrocarbons and atmospheric contaminants adhering to the surface. The CA increases for the dirty Si as more hydrocarbons have adhered to the surface. The HMDS covered samples are in the same range as the dirty Si since the HMDS surface sites are similar to hydrocarbons from the atmosphere. The F-SAM covered samples have the highest CA as expected due to their highly hydrophobic nature

The slight difference in SFE and CA with water between the different substrates Si and Si_3N_4 might be explained by the increased quantity of hydrocarbons similarly as the Dirty Bare Si sample that confirms that CA increases with more hydrocarbons on the surface. This will be discussed further when looking into the surface chemistry with the results of the XPS.

Figure 4. 2 shows the calculated SFE from with the OWKR method. It shows a similar trend but inverted to the contact angle measurements with water.

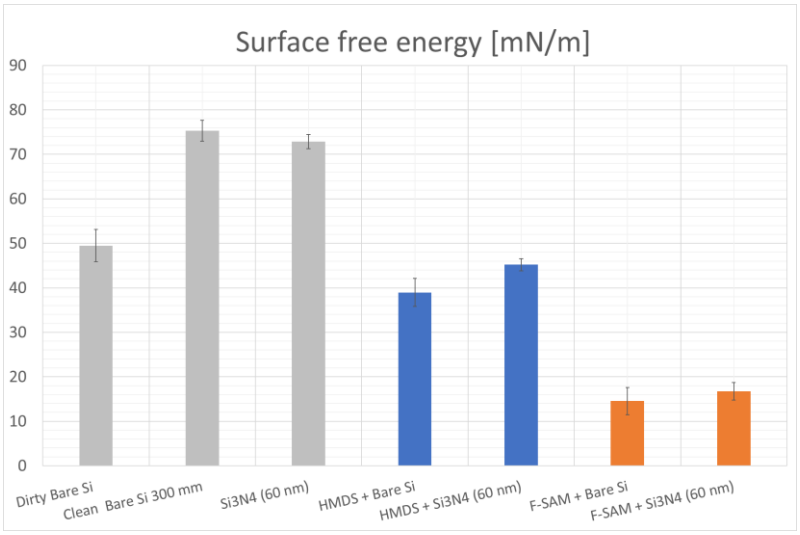

Figure 4. 2: SFE calculated with OWRK from the CA with DIM and DIW. They show the same trend but reversed as the contact angle measurements with water. The lowest CA with water leads to the highest SFE.

The CA and SFE results confirm that the modified surfaces have undergone surface modification. Furthermore, the affinity to water decreases substantially when the monolayers HMDS and F-SAM are deposited in comparison to surfaces without the monolayer.

4.2 Surface Chemistry

4.2.1 Atomic percentage

Surface chemistry was estimated with XPS where the surface was scanned to 7 nm depth. *Table 4. 1* and *Table 4. 2* show the results from the XPS on silicon and silicon nitride substrates, respectively. They show the estimated atomic percentage *at%* of C 1s, F 1s, N 1s, O1s and Si 2p bonds detected on the surface. The bonds relate to hydrocarbons, C_xH_y, carbon bonded with fluor, and the substrates Si, Si_3N_4 and SiO_2.

Carbon bonds, **C 1s**, are in the region of 284.8 eV – 294 eV. The hydrocarbons, **C_xH_y**, carbon oxide, **CO** and carbon nitride, **CN** have binding energy of 284.8 eV and 286.6 eV and are related to organic carbon-based contaminants adsorbed to the surface from the atmosphere. Carbon **C 1s** connected with fluor was measured from 288.8 eV-293.1 eV and might be related to carbon-fluor based contaminants on the surface.

Carbon-Fluor bonds linked to the F-SAM monolayer was related to the **F 1s C-F** measurement at 689 eV.

The surface site that remains from HMDS deposition is trimethylsilyl, Si-$(CH_3)_3$, which cannot be distinguished from hydrocarbons adsorbed to the surface. Therefore, the estimation of HMDS coverage is cumbersome.

Table 4. 1: Apparent concentrations (in at%) of the hydrophobic layers deposited on bare Si substrate and a Si reference.

	C 1s					F 1s	N 1s	O 1s	O 1s	Si 2p	
	284.8	286.5	288.9	291.5	293.7	689	400.5	532.5	536	99.2	103
	C_xH_y	CO, CN	OC=O, CF	CF_2, O-C-F_x	CF_3, O-C-F_x	C-F	C-N	SiO_2	O-C-F_x	el	SiO_2
Si Reference	12.7	4.5	1.4	0.0	0.0	0.0	0.4	37.3	0.0	33.0	10.5
F-SAM + Bare Si	4.7	1.8	0.7	2.6	7.0	28.3	0.7	22.2	4.7	19.6	7.8
HMDS + Bare Si	9.7	2.6	0.5	0.0	0.0	0.0	0.3	39.8	0.0	34.3	13.0

Table 4. 2: Apparent concentration (in at%) of the hydrophobic layers deposited on Si_3N_4 substrate and a Si_3N_4 reference.

	C 1s					F 1s	N 1s	O 1s	O 1s	Si 2p	
	284.8	286.6	288.8	291.5	293.1	689	397.4	532.5	536	101.5	103
	C_xH_y	CO, CN	OC=O, CF	CF_2, O-C-F_x	CF_3, O-C-F_x	C-F	Si_3N_4	SiO_2	O-C-F_x	Si_3N_4	SiO_2
Si3N4 (60 nm) edge	2.3	0.9	0.6	0.0	0.0	0.0	41.0	20.5	0.0	29.3	5.3
Si3N4 (60 nm) center	1.9	0.6	0.2	0.0	0.0	0.0	41.2	21.6	0.0	28.8	5.9
Si3N4 (60 nm) mid	1.4	0.6	0.3	0.0	0.0	0.0	42.4	20.7	0.0	29.5	5.2
F-SAM +Si3N4 (60 nm) edge	1.4	0.7	0.6	1.1	4.7	18.7	27.2	16.5	3.6	20.2	5.2
F-SAM + Si3N4 (60 nm) center	1.6	0.8	0.9	2.0	6.6	26.5	22.4	13.4	4.4	17.3	4.3
F-SAM + Si3N4 (60 nm) mid	1.5	0.8	0.7	1.6	6.2	23.3	24.2	14.6	4.1	18.3	4.6
HMDS + Si3N4 (60 nm) edge	3.1	0.4	0.2	0.0	0.0	0.1	42.3	18.8	0.0	29.3	5.8
HMDS + Si3N4 (60 nm) center	3.3	0.5	0.2	0.0	0.0	0.1	41.5	20.4	0.0	28.5	5.8
HMDS + Si3N4 (60 nm) mid	3.2	0.5	0.2	0.0	0.0	0.1	41.5	19.5	0.0	29.0	6.0

The distribution of detected bonds and atomic percentage at each location on the 300 mm samples with Si_3N_4 layer is small. This indicates that the monolayers are relatively uniform and homogeneous.

The hydrocarbons and other contaminants are in significantly larger quantity on the Si substrate than Si_3N_4 substrate, ~ 10 at%, which explains the higher CA with water on the modified Si surfaces. As mentioned before, the Si modified samples with monolayers were provided by suppliers. No information was provided on surface properties or history of the samples.

It is possible that the Si modified samples contained already some hydrocarbons prior to deposition of the monolayers, giving a rise to large **C_xH_y**, **CO** and **CN** values for both HMDS and F-SAM modified bare Si surfaces. The roughness might also be larger on the Si substrate, which increases the surface where both molecules can be deposited on but also where hydrocarbons and contaminants can adsorb to. The history of the surface of bare Si reference was known, and it was confirmed that it had been stored under conditions that could results in high adsorption of hydrocarbons and contaminants. This indicates that the surfaces with unknown history were stored in similar conditions.

The **CF_x** bonds in the range of 191.5-193.1 eV are likely byproducts from the deposition of the F-SAM monolayer that adhered to the surface or were not flushed away during the process. These bonds are almost negligible on HMDS modified samples and references. It is not known whether these molecules will transfer when wafer is rinsed. It would need to be studied further to confirm.

The difference in hydrocarbon quantity between HMDS + Si_3N_4 and Si_3N_4 reference is small. It seems the reference has adhered contaminants up to a 1.4-2.3 at% range, which the HMDS increases to ~3.2 at%.

However, the difference is too small to make a deliberate distinction between the modified surface and the reference.

4.2.2 Monolayer thickness and coverage

The position of exactly where the signal is coming from during XPS measurements is not completely known due to the width of the angles, between 25°-65° but it is possible to roughly estimate coverage and layer thickness of a monolayer with a simple layered model.

The estimated thickness of the monolayers can be seen in *Table 4. 3* and

Table 4. 4. The thickness of the F-SAM layer is estimated to be 1.0-1.5 nm thick while the HMDS layer is 0.2 nm thick when deposited on Si_3N_4 substrate and 0.4 nm on a Si substrate. The difference is explained from the fact that the HMDS monolayer solely forms the bond Si-$[CH_3]_3$ while the F-SAM monolayer is expected to be from a fluorinated molecule with a chain of carbon bonds.

A rough estimation on coverage can be done by comparing a modelled surface density of the samples with monolayers with the magnitude of silanol sites per unit area of a fully hydroxylated silica surface, which is about $4.6 \cdot 10^{14}$ at/cm^2 [39].

Table 4. 3 and

Table 4. 4 show a rough estimate of the coverage modelled for the following layers $CF_3(CF_x)_y(CH_n)_m$ / SiO_2 / Si & Si_3N_4 for F-SAM and *C+Si (as SAM) / SiO_2 / Si & Si_3N_4* with *Si (SAM) = 1/3C* for HMDS. The fluorinated molecule fitted for the F-SAM was found in literature.

The coverage ratio of fluorinated molecules is large, 89%-122% and there seems to be a large shift between areas, showing the best coverage in the center. Above 100% coverage values are reached, which can be ascribed to inaccuracy of the XPS signal due to large angle width of 25°-65°. It could also be due to the size of the fluorinated molecule that might be detected as a higher coverage.

The high coverage could be due to its the relatively long deposition time to HMDS, that the fluorinated molecule is more likely to find a vacant silanol site to react with. When the deposition begins, the reaction occurs all over the surface. As the deposition continues, the vacant surface sites decrease, and the occurrence of a reaction decreases significantly but with sufficient amount of time, most vacant site will be found.

The estimation is rough, and the fluorinated molecule is unknown, but the surface seems to have good coverage and the fitted surface site might be similar to the real surface site. Further study would be recommended by depositing a molecule that leaves the same surface site via CVD and conduct similar characterization to estimate the properties.

The coverage of HMDS on Si_3N_4 seems to be ~21%. The deposition time of HMDS is 10 times shorter than for the F-SAM, which might explain the difference in coverage. Furthermore, the deposition of HMDS happens in two steps, which might increase the difficulty of a precursor molecule to find two available surface sites in proximity to one another.

Table 4. 3: Thickness and coverage of reference, F-SAM and HMDS monolayers on Bare Si. The thickness and coverage of the organic and native oxide layer was estimated by assumption of a homogenous and uniform layers. Estimation for HMDS coverage was not provided.

Sample	Organic overlayer (nm)	SiO_2 (nm)	**Coverage atom/cm2**	**Ratio**

Si Reference	0.6	0.9	-	-
F-SAM + Bare Si	1.4	1.1	$4.1 \cdot 10^{14}$	89%
HMDS + Bare Si	0.4	1.0	Not provided	-

Table 4. 4:. Thickness and coverage of reference, F-SAM and HMDS monolayers on Si_3N_4 substrate. The thickness and coverage of the organic and native oxide layer was estimated by assumption of a homogenous and uniform layers.

Sample	Organic overlayer (nm)	SiO_2 (nm)	**Coverage atom/cm2**	**Ratio**
Si_3N_4 (60 nm) edge	0.3	0.5	-	-
Si_3N_4 (60 nm) center	0.3	0.5	-	-
Si_3N_4 (60 nm) mid	0.2	0.5	-	-
F-SAM + Si_3N_4 (60 nm) edge	1.0	0.7	$4.1 \cdot 10^{14}$	89%
F-SAM + Si_3N_4 (60 nm) center	1.5	0.7	$5.6 \cdot 10^{14}$	122%
F-SAM + Si_3N_4 (60 nm) mid	1.3	0.7	$4.9 \cdot 10^{14}$	104%
HMDS + Si_3N_4 (60 nm) edge	0.1	0.5	$9.5 \cdot 10^{13}$	21%
HMDS + Si_3N_4 (60 nm) center	0.2	0.5	$1.0 \cdot 10^{14}$	22%
HMDS + Si_3N_4 (60 nm) mid	0.2	0.5	$1.0 \cdot 10^{14}$	21%

4.3 Wear resistance

The wear resistance test was not defined by a standard testing but by conditions that would be most likely to wear off the monolayer during the photolithography process. The step is a wet spin rinse with brushing and polishing as described in **3.3.3 Wear resistance**. The XPS results before and after the cleaning can be found in **Appendix B - Table 1 and 2**. The XPS data before rinsing with polishing is the same as in **4.2 Surface Chemistry**.

Comparison between the XPS data shows no significant difference in the atomic percentage before and after the surface has been brushed and polished in a spin rinse module.

It was expected that the hydrocarbons might be reduced by the rinsing by cleaning off the adsorbed hydrocarbons but due to the time between the processing and the XPS, atmospheric hydrocarbons have sufficient time to adsorb to the surface again. The fluorinated carbon bonds that had been related to contamination or byproducts after the deposition remained within the same range. Therefore, it was considered unlikely that they might rub off and be introduced to the system. This decreases the risk of increased contamination in the photolithography process by modifying the surfaces that related to the third research question of this study.

It is also possible that backside rinsing on a hydrophobic surface can compromise the cleaning efficiency and particle removal [30]. If the water is repelled from the surface, the cleaning quality might be reduced, which could affect the quality of the IC fabrication. This was not within the scope of this project but would need to be studied.

The same fluorinated molecule was fitted for the F-SAM surface, yielding comparable results as a non-rinsed and polished F-SAM wafer.

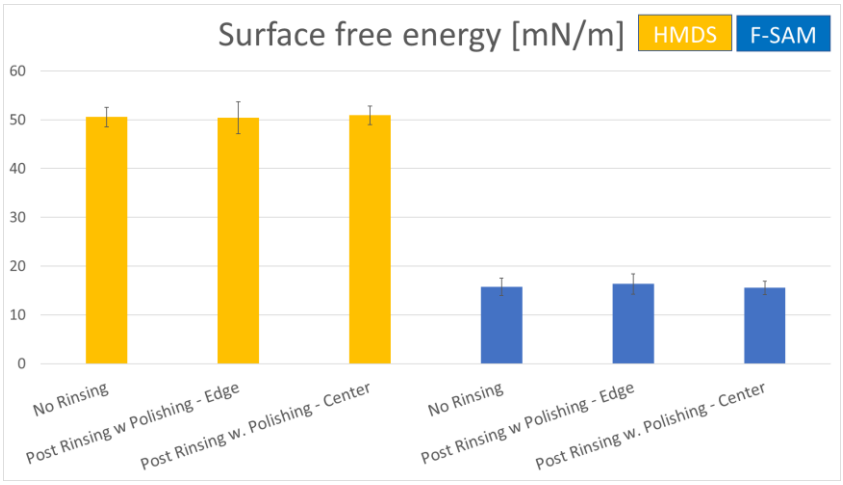

Figure 4. 3: SFE measurements done on substrates before and after rinsing with brushing and polishing. No difference identified before and after.

Figure 4. 3 shows SFE measurements before and after cleaning module with polishing. No difference was identified in SFE before and after the polishing.

Therefore, from the XPS and SFE measurements it can be concluded that a rinsing with brushing and polishing seems not to wear the monolayer off.

Other processing steps that could remove the layers would include baking steps at high temperature. At high enough temperature for sufficient amount of time, the activation energy of the bonds could be reached. However, it is unlikely that this condition is reached during the photolithography process since such high temperature could affect the quality of the IC on the frontside.

Another wear test that could be performed that was not within scope of this study is a hydrolytic stability test to estimate if the monolayer might degrade from exposure to hydrolysis.

4.4 Zeta potential measurements

Zeta potential, IEP and point of zero charge depends on condition and history of the sample and during measurement a few atomic layers are being measured.

The IEP has been measured for various samples. *Table 4. 5* shows the IEP results from previous studies on Si, SiO_2, Si_3N_4 and SiO_2 + HMDS.

Table 4. 5: The IEP of reference samples done previously.

References from previous IEP within ASML	IEP – pH
Bare Si	2.2
Thermal SiO_2 (150 nm)	3.3
Thermal SiO_2 (150 nm) + HMDS	3.3
Old Thermal SiO_2 (150 nm)	2.0
LPCVD Si_3N_4 (60 nm)	3.7

On a bare Si surface, the native silicon oxide layer forms and is covered in silanol sites. Silanol sites deprotonate when submerged in liquid, that is, Si-OH becomes $Si\text{-}O^-$, and the zeta potential becomes increasingly negative when the solution is in the basic regime. The isoelectric point is found in the acidic

regime, around pH 1.7-4 for SiO_2 [65, 25]. The IEP measured on Bare Si Reference was pH 2.2, which is within the range offered by literature and suggest a highly oxidized surface with a lot of Si-OH groups.

Newly thermally grown SiO_2 has a very stable structure with few active silanol sites (less than 10%). Therefore, less sites deprotonate, and the IEP is estimated at a pH ~ 4.0. However, as the thermal silicon oxide becomes older, native oxide forms with increasing amount of silanol sites on the surface. Therefore, the IEP decreases to a more acidic pH point, ~1.7 [65]. The IEP of two thermally grown SiO_2 (150 nm) wafers were measured. One wafer was relatively fresh while the other was old and had been long in storage. The IEP of the relatively new wafer was at pH 3.3, which indicates that oxidation had hardly occurred on the surface. The old wafer had IEP at pH 2.0 indicating substantial oxidation.

A Si_3N_4 is covered in silanol, amine or Si_3N sites. The IEP of a new silicon nitride wafer with no oxide layer is found at pH 7-9 [26, 27]. As the silicon nitride becomes older, it starts to oxidize to form native oxide. An old Si_3N_4 is found to have about > 95-98% of silanol groups (Si-OH) and rest are amine groups ($Si-NH_2$). Then the IEP shifts to a lower value of IEP = 2-3 [15, 27]. Hence, as the surface changes from IEP of pH 9 ($Si-NH_2$, Si_3N dominating surface) towards an IEP 2-4 (Si-OH dominating surface), the impact of rinsing fluid can change. Initially it can make a wafer backside charge positively, while at a later stage it can make it negatively charged, respectively.

The Si_3N_4 reference was unused but had been in storage for about half a year. The IEP = 3.7 which indicates some oxidation of the nitride occurred that results in the shift in IEP.

Lastly, a HMDS layer was deposited on a relatively fresh wafer with thermally grown SiO_2 making the surface more hydrophobic. Hydrophobic surfaces do not interact with water molecules and do not have functional groups, so their zeta potential is determined by interaction with ions. They generally prefer adhesion to hydroxide ions (OH^-) and therefore have a negative zeta potential when submerged in aqueous solutions [15].

The IEP of Teflon is about 3.7 but no literature was found regarding a surface with trimethyl silyl sites [66].

The previous study showed that the sample with HMDS had the exact same IEP as its substrate, at IEP 3.3. This indicates that the IEP might be similar for surfaces with and without monolayers. Therefore, zeta potential measurement to estimate the IEP might not show the effect of the monolayer but more likely the state of oxidation on the samples after the deposition. The surfaces of the modified samples do still have some active silanol and amine sites. The dominant factor that could be measured on the surfaces are the remaining hydrophilic sites rather than the inactive hydrophobic sites that do not form surface charge when submerged in liquid. This could explain why the IEP of the hydrophobic surfaces are in the range of a highly oxidized silicon oxide substrate.

Table 4. 6 shows the IEP measured on samples with the hydrophobic monolayers of this study. Graphs of zeta potential vs pH can be found in the **Appendix C: Zeta potential measurements.**

The bare silicon samples had IEP at < 1.8 indicating a highly oxidized surface, which is similar to the bare Si reference in *Table 4. 5* with IEP of pH 2.2.

Table 4. 6: Isoelectric point of samples with hydrophobic monolayers

Specimen	IEP – pH
HMDS + Bare Si	< 1.8
F-SAM + Bare Si	< 1.8
HMDS + Si3N4 (60 nm)	2.6
F-SAM + Si3N4 (60 nm)	2.0

The silicon nitride wafers had been in storage for about 1 year prior to deposition of the monolayers so a native oxide had formed during storage. The oxidation might have been accelerated during the deposition of the hydrophobic monolayers. Hydrophobic samples on Si_3N_4 substrates had IEP pH 2.0 for F-SAM and IEP pH 2.6 for HMDS.

It shows how significantly the samples had oxidized. The lower IEP for the F-SAM sample compared to HMDS on Si_3N_4 might be due to the length of the deposition process. The sample is longer under the humid conditions that accelerate the native oxide formation while the monolayer is also being deposited.

Literature states that a zeta potential measurement should be the best suitable to monitor the quality of the self-assembled monolayers as it would measure the zeta potential of the monolayers and not the substrate. That is in contrast to what has been found within this study and could be due to the remaining hydrophilic surface sites that contribute to the outcome of the zeta potential measurements [15].

However, it would be recommended to repeat this test and include a reference wafer from the same lot, which should have oxidized to a similar degree. Furthermore, it would be recommended to test a surface that has a known IEP that does not change with time to confirm that the experiment was conducted correctly, such as polytetrafluoroethylene (PTFE) that has IEP pH 3.7 [66].

4.5 Surface charge and conductivity with spin rinsing

As mentioned in **3.3.5 Surface Charging and Conductivity**, the surface charge formation and generation of a streaming potential was estimated by charging the sample with a spin rinse toolset at 80 mm and the surface potential profile was measured with an ESVM.

It was of interest to see if it would be possible to generate a charge profile on the wafers with monolayers. It was suspected that the HMDS wafers might generate lower charge than the F-Sam and reference wafers since they had less active surface sites than the reference and no dipole moment of orientated molecules vertical to the surface as the F-SAM [36]. It was also expected that the F-SAM would generate less charge than the reference due to less active surface sites to form surface charge when submerged in water, as discussed in the state of art **2.7 Silanes of interest** [12, 15].

To estimate a surface's ability to charge, it was rinsed once with a DIW at 1200 rpm for 9 s. Subsequently, the wafers were repeatedly rinsed to achieve similar profiles with sharp local peaks at 80 mm and estimate the surface conductivity over 2 weeks.

4.5.1 Surface charging

Figure 4. 4 shows the initial ESVM measurements of all the wafers. Two wafers of each type were used. The graph shows that all wafers had a flat electrostatic voltage (ESVM) profile before the rinsing. The HMDS + Si_3N_4 (60 nm) and Si_3N_4 (60 nm) wafers had a local uniform charge at the surface of about -0.05 V while the F-SAM wafers had a local uniform charge of about -0.3 V. This is similar as was found within literature where a fluorinated modified surface had a negative local surface potential of -1 V prior to charging while the CH_3 modified surface had a local surface potential ~ 0 V [36].

The peak on the F-SAM 2 wafer at radius of -150 mm is likely due to an artifact of the ESVM as it is at the edge of the measurement.

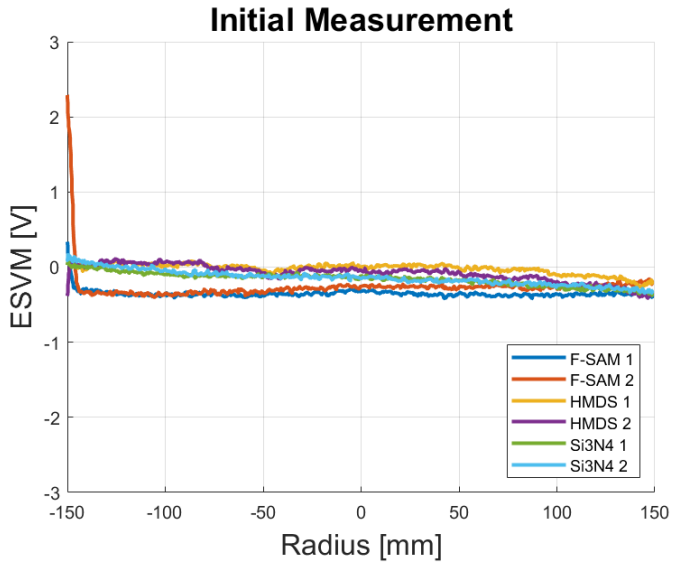

Figure 4. 4: Initial ESVM measurements on specimen prior to rinsing.

Figure 4. 5 shows the ESVM profiles of each type of wafer after 1 x spin rinse. The Si_3N_4 wafers have a negative peak of about -1.0 V at +/- 80 mm radius. The peak then slowly diverges to the 0 V baseline along the wafer though with a curved profile. The negative charge seems to be compensated with a sharp positive peak of about 2.2 V at the edge, which fits results found in literature [12].

The positive peak at the edge could be a visual representation of the streaming potential generation from *Figure 2. 9*. A surface charge and the electrical double layer is formed when the surface is submerged in water. The centrifugal forces during spin rinsing creates a liquid flow so the mobile counterions to the surface flow with the liquid. When the liquid reaches the edge and mostly flies off, the counter ions might reside at the edge with the residual liquid creating a compensating peak with the opposite sign to the peak formed at 80 mm radius.

The F-SAM and HMDS wafers in *Figure 4. 5* have two distinct positive and negative peaks at +/- 80 mm radius. These double peaks have been attributed as an artifact of the spin rinse tool. These peaks were not measured when wafers were rinsed with other spin rinse tools. The charges seem to have such low mobility even in 100% RH that the double peaks that likely collapse on the reference wafer can be identified on the F-SAM and HMDS wafers.

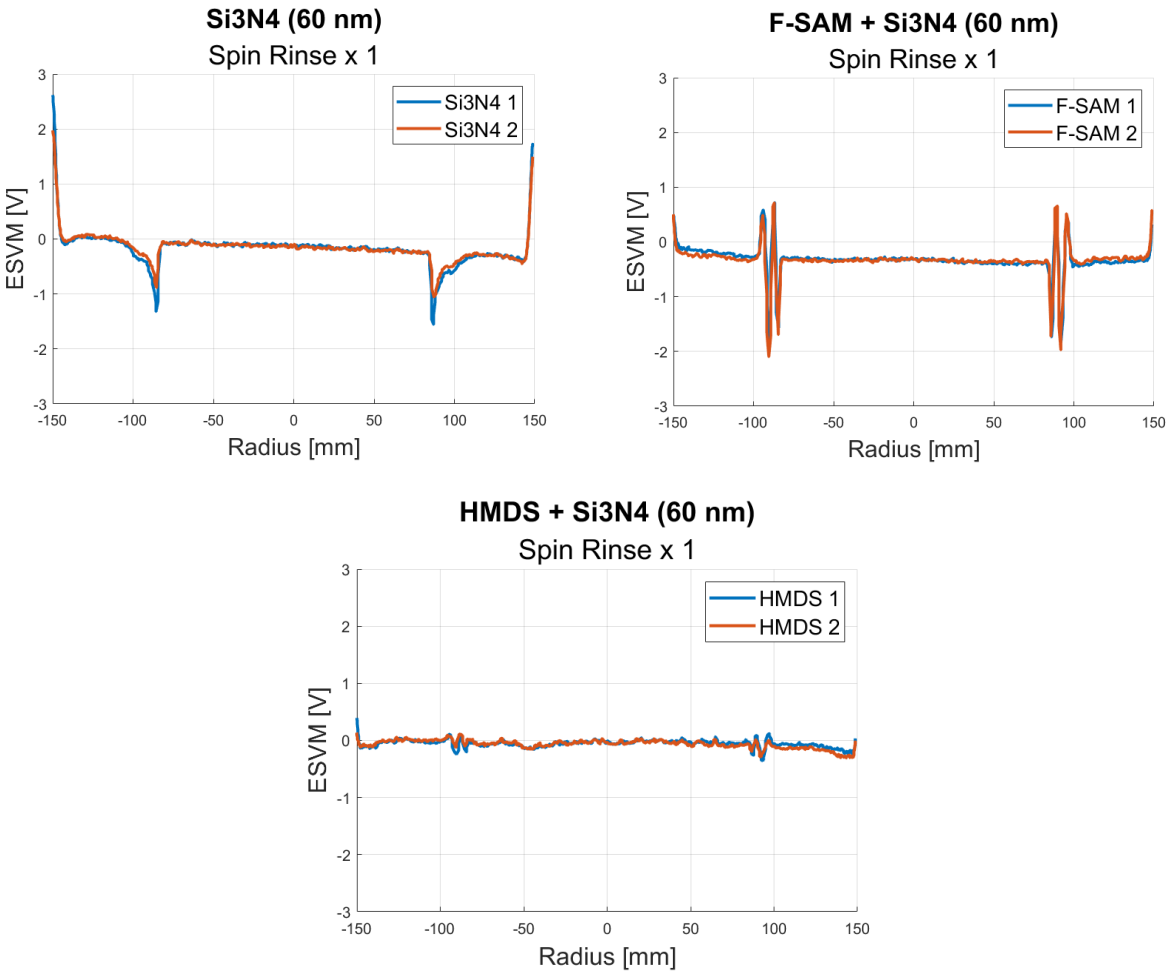

Figure 4. 5: Surface potential profiles of all wafer types, Si_3N_4, F-SAM and HMDS, after they have been gone through a 1 x Spin Rinse with DIW, 1200 rpm and 9 s.

It is concluded that it is possible to charge the wafers with both the F-SAM and HMDS monolayers that seem to have low charge mobility. HMDS generates the smallest profile, as suspected from literature [36]. The small profile of HMDS is promising with regard to reduction of charge diffusion. If no potential forms over the surface, no charge is present to conduct to surrounding components.

The coverage of HMDS and F-SAM, limits any charge distribution over the surface so the profile is localized to the peaks at the water dispense and the edges. Additionally, the hydrophobic nature limits or repels the contact with the water. Therefore, the charge profile is relatively flat except where the water is dispensed and at the edge where the counter ions of the electrical double layer have accumulated.

4.5.2 Surface conductivity study

Previous studies of rinsing 300 mm SiO_2 surfaces with water, shows that charging a surface with spin rinsing is cumulative [12]. The modified wafers and the references continued to be charged by spin rinsing to obtain about a -10 V peak at +/- 80 mm radius. *Figure 4. 6* shows the ESVM profiles of the wafers when charged to obtain a -10 V peak and *Table 4. 7* shows the peak magnitude measured at +/- 80 mm radius.

The surface material of the rinsed wafer impacts the charging behavior drastically. Both wafers of each wafer type charged similarly so the charge profile is highly reproducible.

The Si_3N_4 reference wafers were able to obtain a peak of -9.3 V after eleven rinses and a profile that spread from 80 mm radius to the edge and fits the schematic of surface sites described in *Figure 2. 10*.

Table 4. 7: Charge peaks generated after several spin rinses prior to surface conductivity studies.

Wafer type	Spin Rinse x X	Δ Potential at double peaks [V]	Peak at +/- 80 mm [V]
Si3N4 (60 nm)	11		-9.3
F-SAM + Si3N4 (60 nm)	6	9.3	-5.9
HMDS + Si3N4 (60 nm)	20	1.8	-1.8

The charge peak amplitude increased on the F-SAM similarly as the reference. It was expected from literature that the F-SAM surface would generate a larger potential profile than HMDS [36]. The double peaks on the F-SAM remained and increased in magnitude as the wafers continued to be rinsed up to six times. The peak at +/- 80 mm was about -6.0 V but the differences between the positive and negative peaks reached 9.3 V.

Interestingly, there is hardly any increase in charging of the HMDS modified wafers, even when rinsed up to twenty times, yielding a maximum charge peak of -2.0 V. This is in line with the results found in literature of the CH_3-SAM deposited on SiO_2 gate in a transistor, which did not generate any local surface potential after drain-current measurements [36].

In theory, this could be explained by the fact that a fraction of the silanol sites have been replaced by trimethyl silyl groups, which do not charge. It is therefore difficult to balance the positively charged amine sites with the remaining negatively charged silanol sites. It pushes the point of zero charge to a higher level of pH, which could be at the level of the DIW. This could be tested by charging the wafer through the same process with a liquid at a lower pH level to see if the wafer will charge positively.

However, the silanol sites are also replaced undergo the same changes when deposited with F-SAM. The HMDS deposition is shorter, which could reduce the amount of amine sites being hydroxylated by the hydrolysis during the deposition. Furthermore, C-H bonds are nonpolar unlike C-F bonds that have dipole moments and partial charge. It is possible that when the F-SAM surface is rinsed that the dipole moment of the C-F bonds in the molecule is increased, increasing the surface charge.

Peaks started forming on the center of the HMDS wafers, within 80 mm radius, after continuous rinsing. These peaks also formed on the reference wafer and are therefore attributed as an artifact of continuous rinsing.

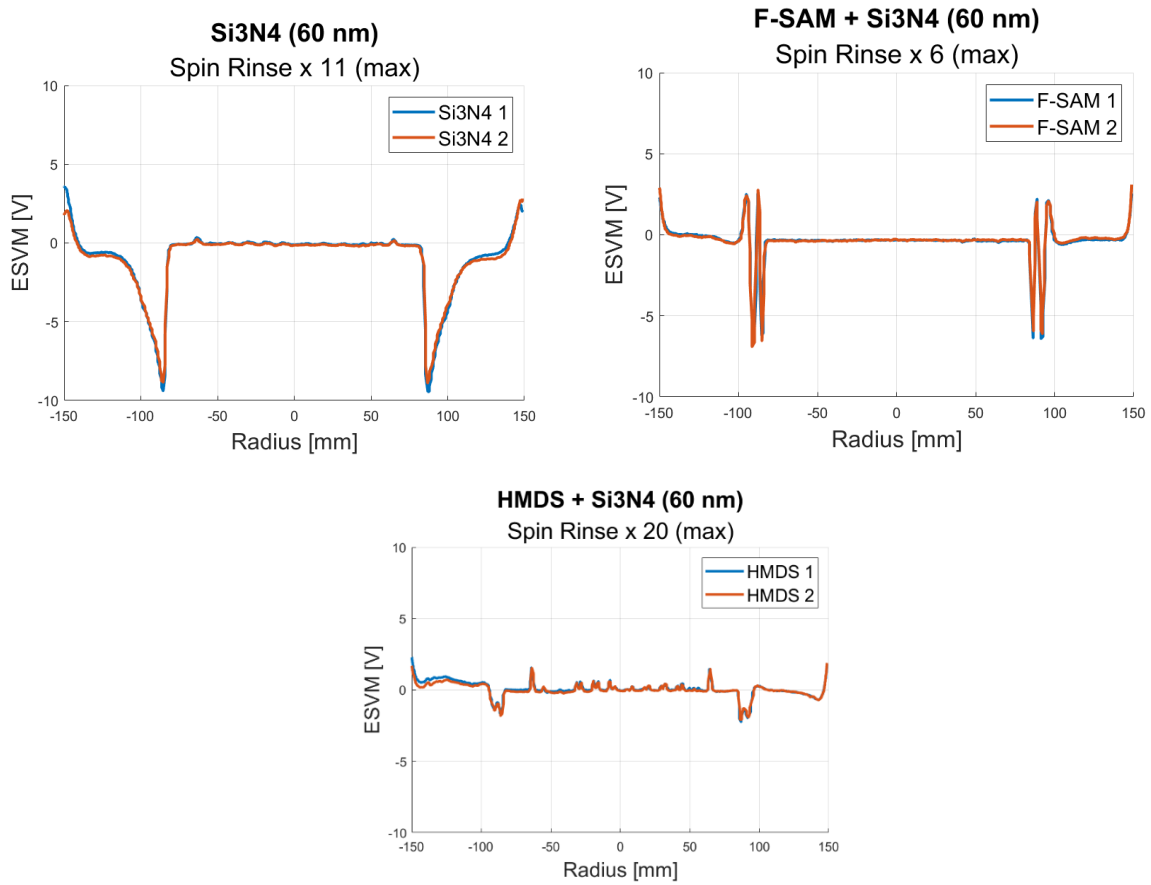

Figure 4. 6: ESVM profile of the wafers, Si_3N_4, F-SAM and HMDS, after being charged by the spin rinse module several times to obtain a peak of around -10 V. The Si_3N_4 obtained the profile after 11 rinses with a distinct profile at around 80 mm. The double peak of the F-SAM wafers continue as the wafers are charged more and the voltage differences was obtained after 6 spin rinses. The HMDS wafers went through the spin rinse module twenty times and the largest peak did not exceed -1.8 V.

After the wafers were charged as has been described, an ESVM measurement was done at 0 h, 24 h, 48 h, day 7 and day 14 from the original charging. In between measurements the wafers were stored in RH 40% and 21 ± 2 ^{o}C.

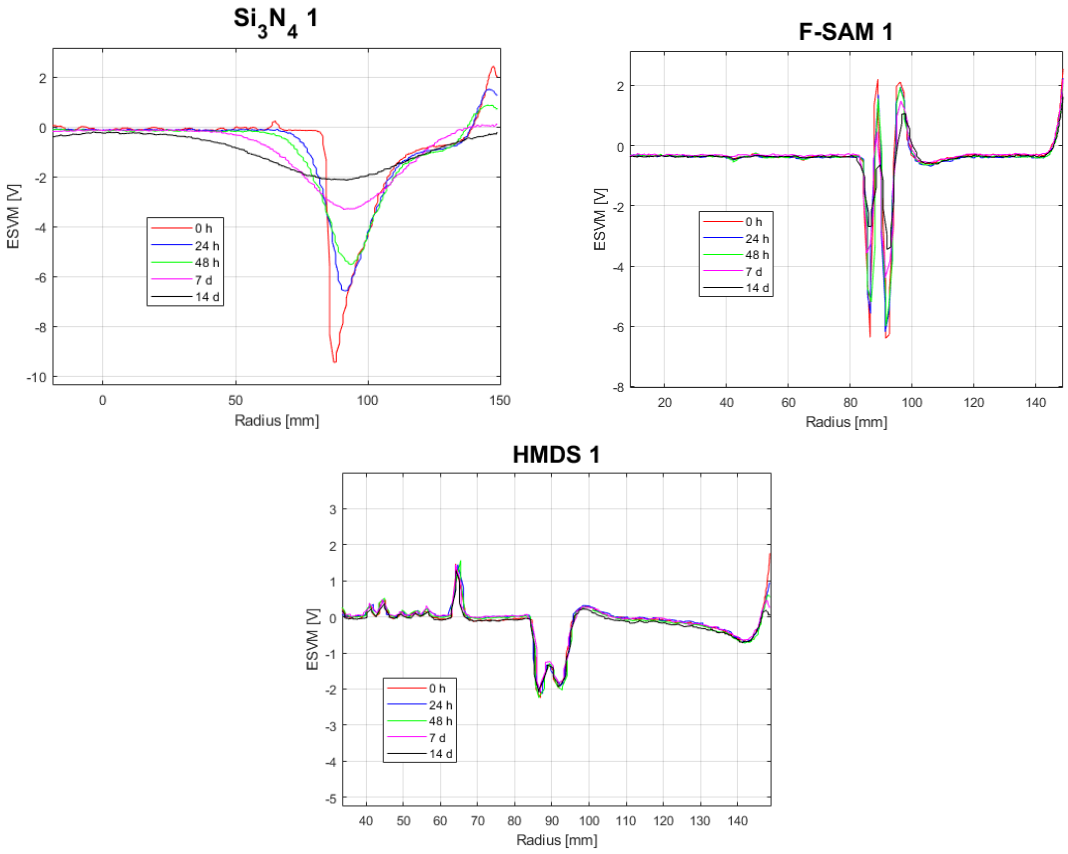

Figure 4. 7: Charge decay on Si3N4 reference, F-SAM and HMDS wafers. Charge on Si_3N_4 degrades substantially over the 14 days showing how the charge spreads over the wafer, including the previously uncharged center. The peaks of the F-SAM wafer deteriorate over time without affecting other areas, such as the center. Finally, no change is identified in the charge profile of the HMDS wafer.

Figure 4. 7 shows how the charge profiles change over 14 days. The profile on Si_3N_4 wafers change significantly. It seems that the charge migrates over all the wafer, including the previously uncharged center. The center then slowly becomes negatively charged. This is in line with literature found on proton hopping that occurs on the hydrophilic surface when water adsorbs that contributes to the charge being spread over the surface and can be seen in *Figure 2. 23* [37, 34, 35, 38].

The double peaks on the F-SAM wafers deteriorate over the two weeks, but no other change is identified in the charge profile of F-SAM. This indicates that the charge is not conducting over the surface but perhaps recombining between the peaks at 80 mm radius or with particles/ions in the air [36].

No difference was identified in charge profile on HMDS wafers after 2 weeks. The charge seems to be completely trapped.

The surface conductivity was estimated with a lumped circuit model. Derivation on how the modelling was done can be found in **Appendix D: The derivation of surface resistance** [14, 13].

The results of modelling the surface conductivity can be seen in *Table 4. 8*. An estimation on silicon oxide and silicon nitride surface conductivity is about $3 \cdot 10^{-13}$ S at 40% RH according to literature, which fits the results of this study [13, 14]. A material is considered to be an insulator if the conductivity is less than 10^{-8} S/cm [67]. All these surfaces are considered insulating though the surfaces with the hydrophobic monolayers are significantly more insulating than the reference.

The surface conductivity is reduced by a factor if 1000 when the hydrophobic monolayers are deposited on the nitride surface, which is the same reduction as was found within literature for HMDS deposited on SiO_2 [14].

Table 4. 8: Fitted surface conductivity at 40% RH fitted from a lumped circuit model.

Wafer type	Surface conductivity 40% RH, σ [S]
Si_3N_4 60 nm	$\sim 5 \cdot 10^{-13}$
F-SAM + Si_3N_4 60 nm	$\sim 5 \cdot 10^{-16}$
HMDS + Si_3N_4 60 nm	$< 10^{-16}$

4.6 WT current measurements

WT current measurements were used to estimate the absolute diffusion of charge from a wafer backside to a wafer table. The wafers were charged with a spin rinse module, their ESVM profiles were mapped and then placed on the WT where the current discharge was measured as a function of time. Afterwards, their ESVM profiles were mapped again. The total diffusion of charge was calculated and the change in the wafer's charge profile compared.

There are two regimes that are considered to contribute to charge migration when the wafer is clamped. These regimes can be seen in *Figure 4. 8A,* which shows the current signal when a 150 nm silicon oxide wafer is placed on the WT setup.

The first regime, I, is during clamping and unclamping of the wafer. Significant signal can be detected in this regime. It is considered likely that before the clamping, the gap between the wafer and the WT acts as a capacitor with the voltage difference, ξ, due to the charged backside. The formula for a capacitor is defined with the following equation.

Equation 4. 1: Capacitance for a parallel plate.

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

The variable A is area, ε_r is relative permittivity, ε_0 is the permittivity constant in vacuum and d is the distance between the plates. When the wafer is clamped the distance d goes to zero and the capacitance becomes very large, leading to a large charge Q, and current I, *Equation 4. 2* and *Equation 4. 3*, conducts from the wafer backside to the WT as they have now become connected. The capacitor is then recreated when the wafer is unclamped from the wafer resulting in a significant signal again.

Equation 4. 2: Charge calculated from potential

$$Q = C\xi$$

Equation 4. 3: Current defined as change in charge over time

$$I = \frac{dQ}{dt}$$

The second regime (II) is the signal picked up while the wafer is clamped and originates from diffusion of charges over the wafer backside. The mechanism is due to continuous charge diffusion from the backside to the WT. This second regime of charge harvesting is influenced or enhanced when humid air is provided to the surface, which increases surface conductivity on the hydrophilic surfaces [13].

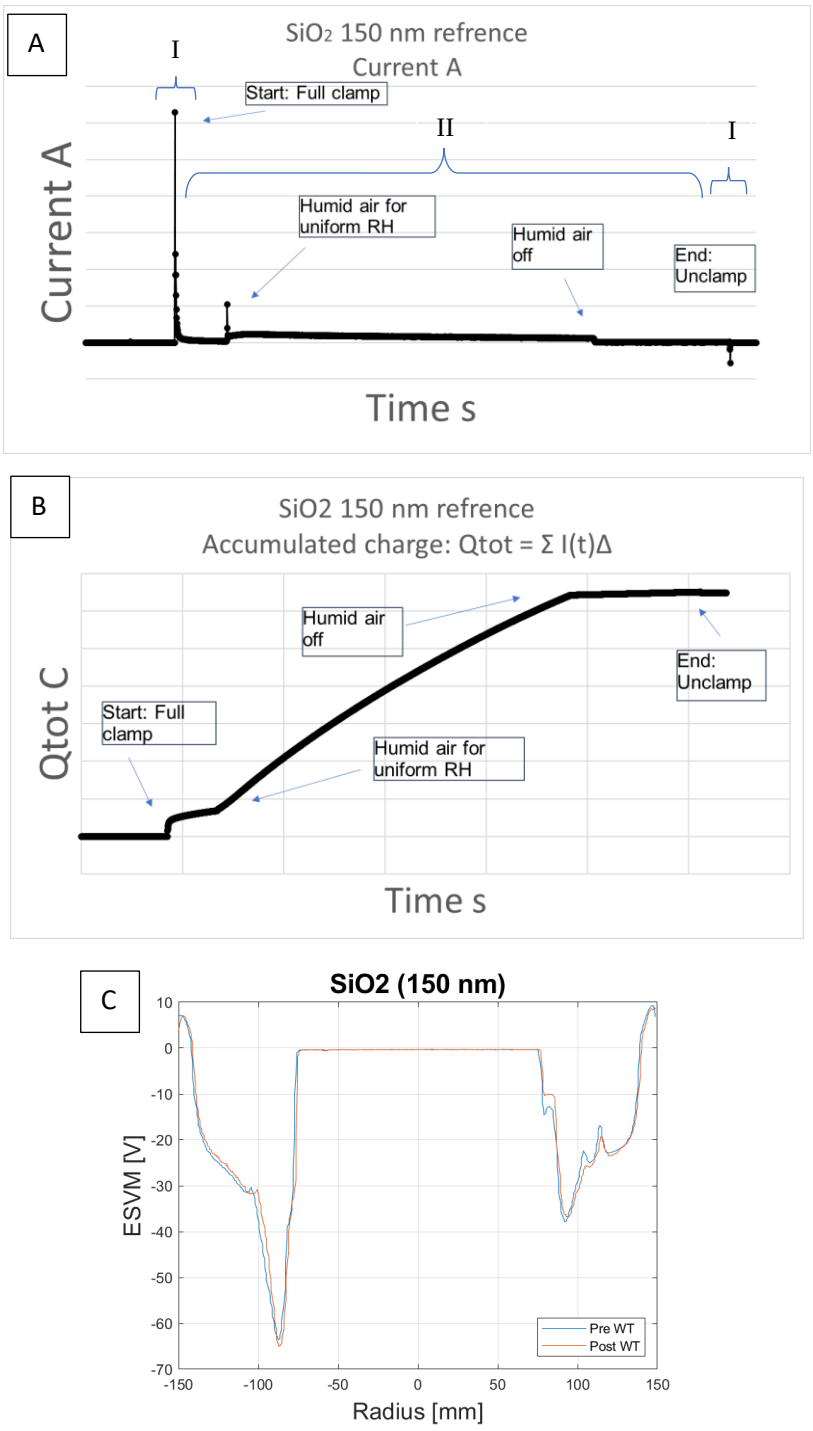

Figure 4. 8: Graph A shows the current signal from 150 nm silicon oxide reference wafer showing each regime of the WT current measurements, Regime I is when the wafer is clamped and unclamped. Regime II is the duration when the wafer is clamped. An increase in signal is seen when humidity is increased. Graph B shows the accumulated charge over time when the wafer is clamped. The charge diffusion rate is largest when the humidity is high. Graph C shows the ESVM profile before and after the wafer is placed on the table. The wafer had been charged some days before the measurement so the charge profile had started to degrade, which left the peaks uneven. Minor changes are identified between the profiles. It was not possible to charge the silicon nitride wafers similarly due to difference in thickness of layers and relative permittivity.

Figure 4. 8 shows the current signal (A), accumulated charge that had diffused from the silicon oxide wafer to the wafer table (B) and comparison between the ESVM profiles before and after testing (C). The main current signal (A) from regime I is a large peak during clamping and a small peak during unclamping. In regime II, a stable positive signal is detected that is increased when humid air is provided to the system and decreases immediately when it is turned off. Graph B shows the accumulated diffused charge over time from the wafer backside onto the WT, see *Equation 4. 4*. Graph B confirms that the predominant mechanism is charge migration and diffusion in regime II when the wafer is clamped in humid conditions. Graph C then shows the ESVM before and after the wafer is clamped onto the WT setup. It shows the changes in the local charge profile before and after the current measurements. The changes are not large but detectable, confirming the diffusion when the wafer was clamped.

Equation 4. 4: Accumulated charge over time from current signal over time

$$Q_{tot} = \sum_{i} I_i \Delta t_i$$

The output of the current measurement can be used to see which regime is predominant when the wafer is clamped, accumulated charge and how the charge migration is influenced by relative humidity.

For the hydrophilic SiO_2 reference, the main charge diffusion occurred during regime II, when the wafer was clamped and the diffusion rate was increased significantly with increased humidity, as expected from literature [14, 13].

For simplistic comparison solely the absolute value of the total charge diffused was used to compare the performance of different wafer backsides.

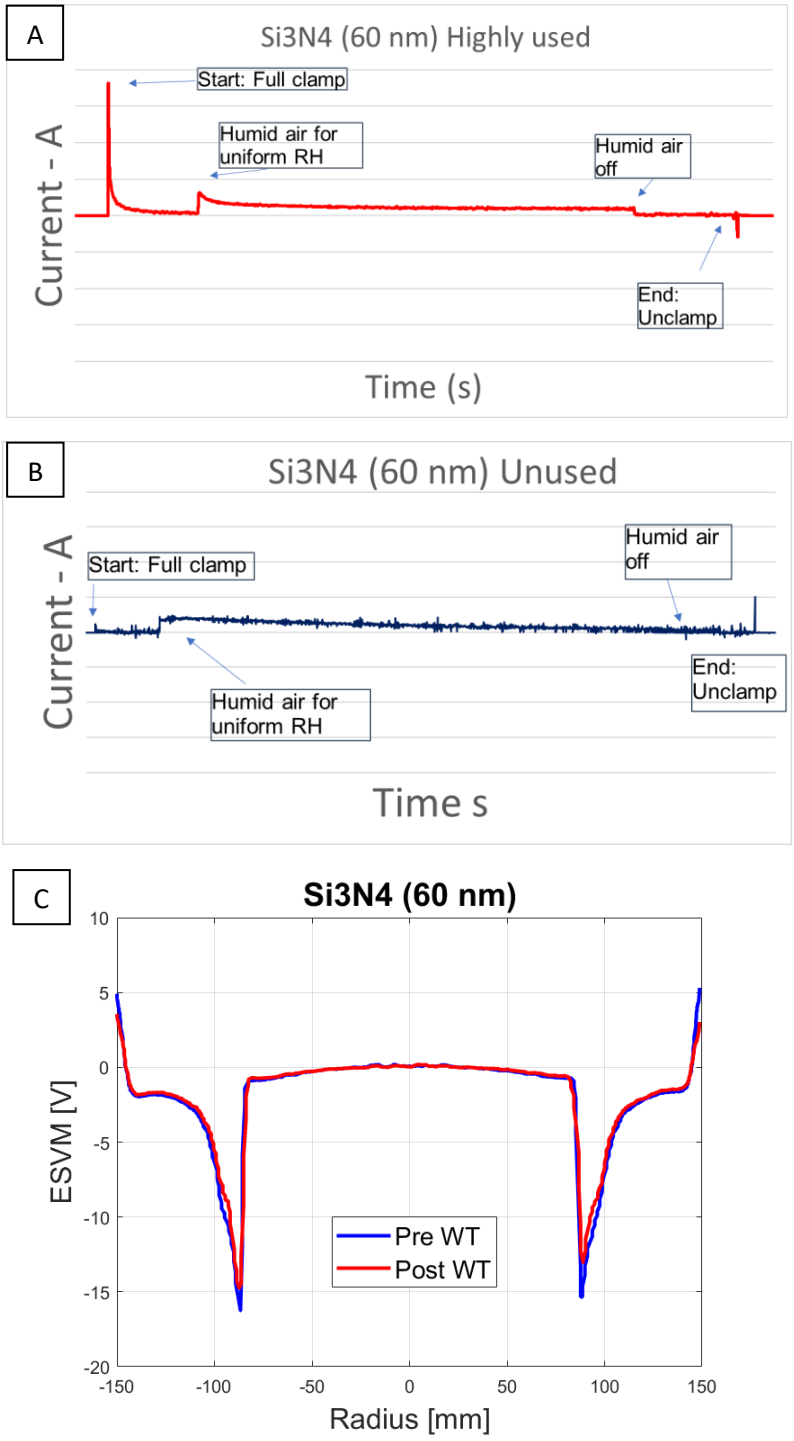

Figure 4. 9: Graphs A and B show the current signals coming from a highly used Si_3N_4 (60 nm) reference wafer and a new, unused wafer that is partially oxidized. Graph C shows the change in the local surface potential measured with the ESVM before and after the new unused reference wafer was placed on the wafer table. The highly used wafer shows a clear signal in both regimes (I & II). The new wafer does not show large peaks during loading and unloading and the signal when loaded increases when humidity is applied but degrades over time. The local surface potential in graph C shows how the profile of the unused wafer has altered and decreased in magnitude after being placed on the wafer table setup, especially at the peaks.

Figure 4. 9 A and *B* show the current signal of a highly used Si_3N_4 (60 nm) reference and a new and unused reference. The old wafer shows a clear signal in both regimes (I & II). A clear peak is picked up when the

wafer is clamped and unclamped. Furthermore, there is a clear signal detected when clamped, which increases and stabilizes when humid air is provided. For the new and unused wafer, a small signal is detected during clamping, but a larger one is identified when unclamped. When clamped the main signal is at noise level until humid air is provided. The signal increases to begin with but decreases slowly until the only signal is again at about noise level. The difference in the measured current signal is likely from the condition of the wafers. The old wafer is highly oxidized and perhaps with some minor damages that would drive the diffusion from the backside to the wafer table. The new wafer has likely started oxidizing but to a less extent than the old one, so it has smaller surface conductivity and larger fraction of amine sites that interact with the silanol sites.

Figure 4. 9 C shows the local surface potential of the wafer backside before and after the wafer was placed on the wafer table. It shows how the large peaks at 80 mm radius and at the edges have decreased a bit, confirming that charge diffusion has occurred from the wafer backside towards the wafer table.

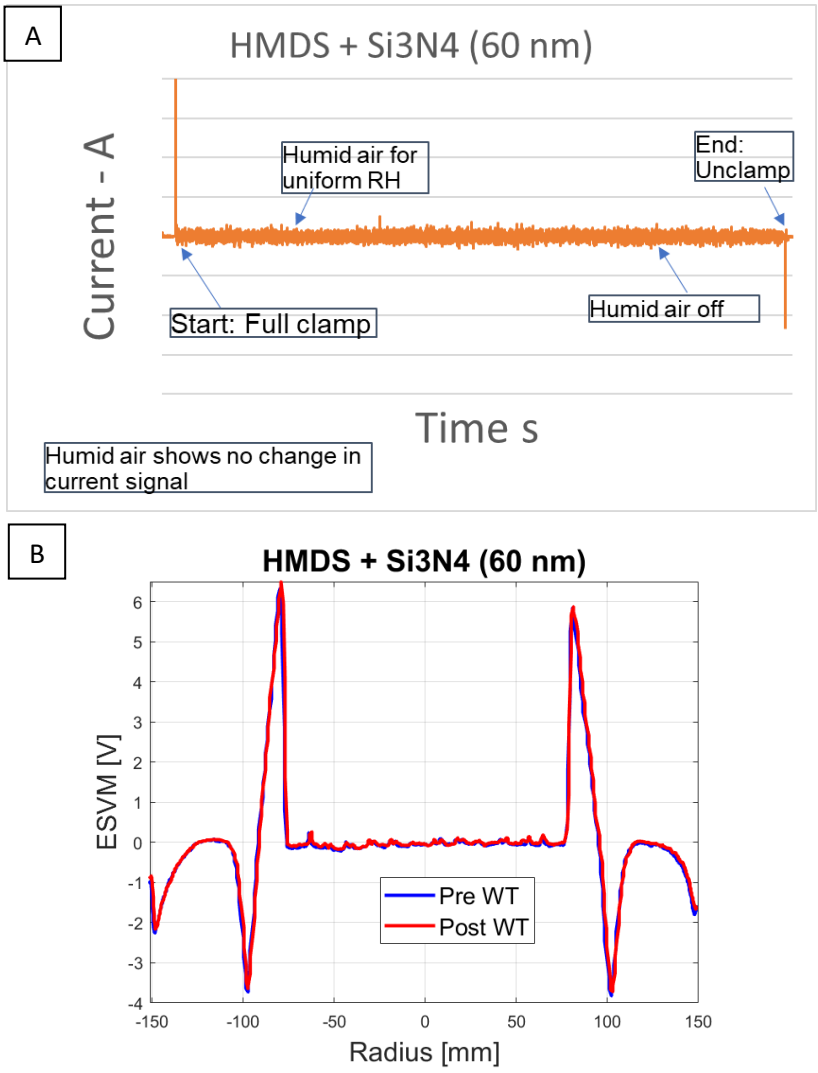

Figure 4. 10: The figure shows the current signal (A) and local surface potential (B) from an HMDS wafer. It shows large current signal peaks during clamping and de-clamping. When clamped, the current signal is very small, and no difference is identified when humid air is provided to the system. The local surface potential shows no difference in the profile before and after the current measurements. Both the current signal and ESVM profile indicate that little to no charge diffusion has occurred.

Figure 4. 10 shows the current signal and the local surface potential of a HMDS hydrophobic wafer. The main signal is from clamping and unclamping. The current signal during clamping and de-clamping is not fully understood and seems to vary each time the wafer is clamped, see current signal graphs in **Appendix E: WT current measurements**. The signal when the wafer is clamped is noisy and no difference is seen when the humid air is provided or removed from the system. This suggests that the main contribution of charge that migrates from the wafer to the WT is due to clamping. The charge diffusion is extremely low and unaffected by change in humidity. The local surface potential from the ESVM seems to support this theory as negligible change can be seen in the charge profile before and after the measurement. This is also in line with the results from the surface conductivity measurements and literature that suggests that charge diffusion would be significantly reduced [14].

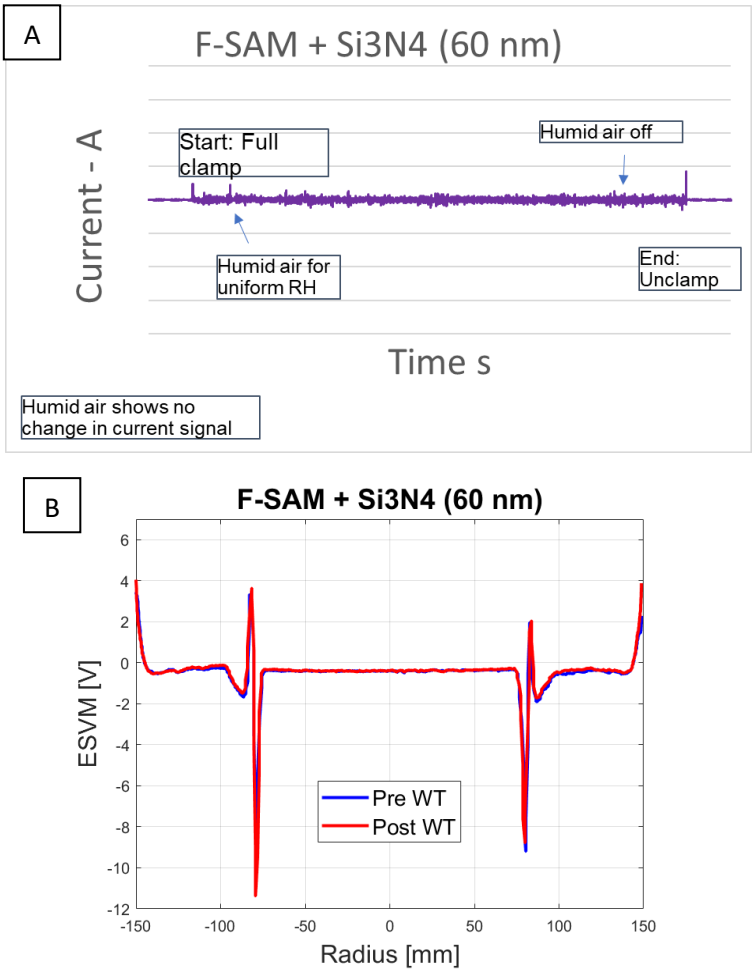

Figure 4. 11: The figure shows the current signal (A) and local surface potential (B) from an F-SAM wafer. The F-SAM current peaks during clamping are significantly smaller than the HMDS peaks in Figure 4. 10. When clamped, the current signal is within noise range, and no difference is identified when humid air is provided to the system similarly to the HMDS wafer. Negligible change can be identified in the ESVM profile before and after the measurements. Interestingly, minor increase at the edge and 80 mm charge peaks profile suggests that the charge might be flowing from the WT to the wafer.

Figure 4. 11 shows the current signal (A) and the local surface potential (B) for the F-SAM hydrophobic wafer. The current signal (A) has smaller clamping peaks than the HMDS wafer but the main signal during clamping is very similar to HMDS. It is noisy and does not change with increased humidity in the system suggesting negligible charge diffusion. This is supported by the ESVM profile (B), which shows negligible change in the local surface potential before and after the measurement. Interestingly though, minor increase

at the edge and 80 mm peaks in the profile suggests that the charge might be flowing from the WT to the wafer. The absolute current was inspected within this project, but further study would have to be conducted to estimate exactly the direction of the current on a F-SAM modified surface.

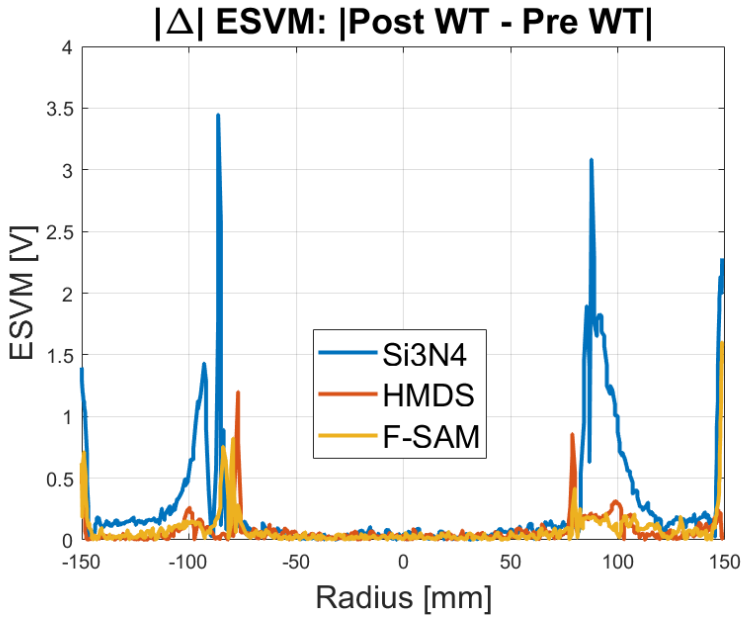

Figure 4. 12: Graph shows the absolute difference in the surface potential profiles of all the samples before and after being placed on the WT. Si_3N_4 reference (blue) shows the largest potential difference that spreads over the surface from where charge is present. The HMDS (red) and F-SAM (yellow) show some very localized difference in the delta potential profile.

Figure 4. 12 shows the absolute difference between the surface potential profiles on all the samples $|\Delta| = |Post\ WT\ ESVM - Pre\ WT\ ESVM|$. No change is detected in the center where no charge is present to diffuse. The main difference in the profiles is seen at the largest peaks at the edges and at 80 mm where the water is dispensed. The largest change in profile is on the new silicon nitride reference (blue) and it shows how charge diffusion has occurred all over the wafer where a streaming potential was generated. There is change in the profile identified on the hydrophobic surfaces HMDS (red) and F-SAM (yellow), but it is very localized, only where the water was dispensed and at the edges. These changes on the hydrophobic monolayers can be attributed to the large, concentrated charge that was able to diffuse from the direct contact but not continue to diffuse due to low surface conductivity. It could even be attributed to a small misalignment of the wafer between measurements that could affect how the profiles are mapped with the ESVM.

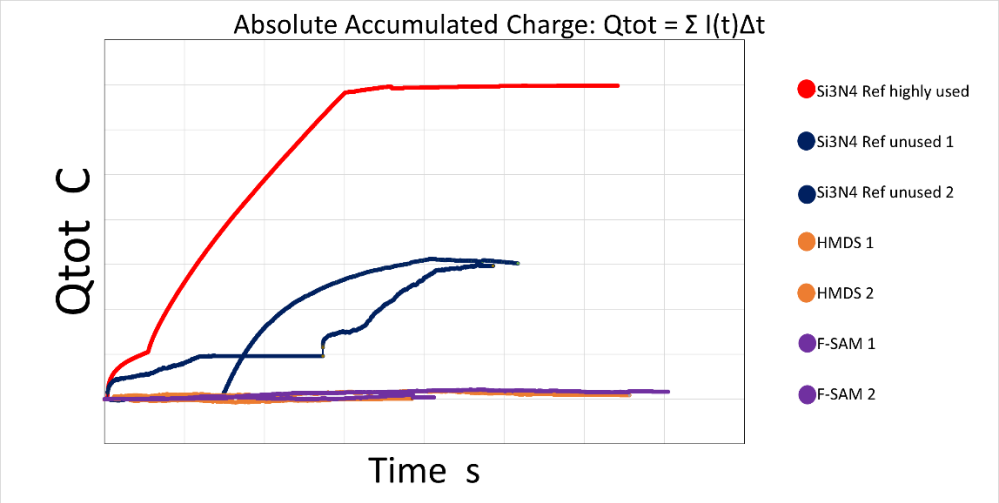

Figure 4. 13: Graph shows the accumulated charge for all the wafer types from the WT current measurements. It shows that the old nitride wafer (red) diffuses the most charge over time. The new nitride wafer (dark blue) diffuses at least a factor two less than the old wafer. The wafers with hydrophobic monolayers however diffuse a factor of 17 less Coulombs than the wafers without.

To estimate the total accumulation of charge each time a wafer was placed on the WT, the current was calculated to charge with *Equation 4. 3* and Equation *4.* 4.

Figure 4. 13 shows the accumulated charge of all the wafers measured. The most charge migrated from the old nitride wafer (red). The new nitride wafer migrates similar amount of charge during both clamps (dark blue), about half of what the old nitride diffused. This shows that the condition of the wafer might be important. The older wafer is likely highly oxidized and might have some defects from previous use, which increases the surface conductivity.

The figure also shows that the total charge dissipated from hydrophobic wafers, both HMDS and F-SAM modified wafer, is at least 17 times less than is dissipated from an unmodified hydrophilic wafer.

The final conclusion of the WT measurements is that the wafers with hydrophobic coatings diffuse substantially less charge than hydrophilic surfaces, which is in line with the reduction in surface conductivity. Their main signal is from clamping and de-clamping from the WT, which seems to variate between each clamp. However, when clamped, the hydrophobic wafers show only noise signal with no change when the humidity is increased, which in the case of hydrophilic surfaces increases the surface conductivity. The modification does not seem to slow down proton hopping but rather to almost prevent it entirely. Therefore, the hydrophobic layers seem very promising with regard to preventing discharging toward the wafer table since the low mobility of charge would limit the charge diffused to the outstanding pins on the wafer table. This was confirmed both in the surface conductivity measurements and WT current measurements.

5. Discussion

Contact angle measurements confirmed the modification from a hydrophilic nature to a hydrophobic nature with deposition of HMDS and F-SAM. The modified surfaces had significantly higher contact angles with water and less surface free energy than unmodified references. Contact angle with water of HMDS + Si_3N_4 was measured around 66°, which was within the range found in the literature [52]. The CA measured on HMDS + Si was significantly higher. This is attributed to more hydrocarbons that had accumulated on the substrate prior to deposition, which was confirmed by the XPS analysis. The contact angle with water of F-SAM substrates were 100°-110°, which is similar to the values for fluorinated SAM layers found in literature [53].

The XPS data showed a small difference in atomic percentages on different locations on the modified samples, which indicated a homogenous distribution of monolayers on a sub nanometer scale and a good deposition process. Furthermore, negligible difference was identified between reference and sample with HMDS. This is due to the surface site that is formed from HMDS being a trimethyl silyl, which has the same atoms as hydrocarbons that are commonly adsorbed from the atmosphere and considered a contaminant. The difference between hydrocarbons atomic percentage on the silicon and silicon nitride substrates can be attributed to contaminants but a lack of knowledge of the history of Si substrates make it difficult to conclude. The high concentration of fluorocarbon-based bonds on the F-SAM samples could indicate the amount of byproducts that have adsorbed to the surface during deposition or lack of purging to remove the byproducts from the surface. The good coverage from the rough layer model indicated high coverage of F-SAM and that it might be similar in structure or length of the fitted molecule found within literature. The high coverage of F-SAM could also be attributed to the size F-SAM molecule simply being larger than expected, blocking surrounding surface sites and increasing the coverage ratio. The coverage of HMDS on the modified surfaces was estimated to be around 20%.

Wear resistance test of a wet spins rinse with scrubbing and polishing showed negligible difference in XPS and SFE measurements. Hence it is assumed that the quality of the monolayer will not be affected by this rinsing procedure nor that it might wear off the wafer and onto the brushing and polishing tools, introducing contaminants to the processing. Therefore, negligible risk is introduced to the photolithography process by a wet spin rinse process with polishing and brushing, relating to the third research question of this project.

Zeta potential measurements did not seem to estimate the isoelectric point of the monolayers deposited on the surface but rather the substrate underneath. This can possibly be attributed to the fact that the hydrophobic surface sites do not protonate or deprotonate when submerged in liquid. Therefore, a testing procedure like the zeta potential measurement is likely to estimate the surface potential generated from the remaining hydrophilic surface sites. It is recommended to redo the tests to confirm the results are not due to the experimental setup.

The results of the charge study answer the first research question of the thesis. It was possible to generate a surface charge from spin rinsing procedure on both F-SAM and HMDS modified surfaces.

The F-SAM formed big distinct charge peaks similar in amplitude as the Si_3N_4 reference, but no charge seemed to be distributed over the surface and the profile was relatively flat. The peaks were mainly negative as had been seen in literature [36]. The fluorinated molecules do not dissociate so it is likely that some residual hydrophilic silanol sites are becoming charged or due to dipole moment of C-F bonds with negative dipole on the fluor atoms facing outwards. The XPS estimated a high coverage of F-SAM (> 85%) so due to the chemical inertness of the fluorinated sites and low conductivity of the surface, the charge that had been generated could not conduct along the surface (prevent proton hopping), leaving a flat profile [38].

Furthermore, the hydrophobic nature of the surface could result in the water flowing over the surface being repelled, limiting the immersion in water and generation of a streaming potential over the surface. If the water is repelled off the surface, the cleaning efficiency of a wet spin rinse procedure could be compromised. That can introduce a risk to the photolithography process, which relates to the third research question of this project.

HMDS showed almost no charge after the first spin rinse. After the wafers were rinsed twenty times, the largest charge peak reached -1.8 V and a small profile from radius ± 80 – 150 mm, which was not present on the F-SAM. This behavior is clearly different as compared to pure Si_3N_4 wafers that can be charged up to much larger values. Apparently, HMDS has a much lower top level to which it can be charged. The low voltage could be explained by the state of surface sites but it is also in line with results found within literature on CH_3-SAM deposited on SiO_2 [36]. During the deposition, the silanol sites are replaced by trimethylsilyl sites. XPS estimated that the coverage was about 21%. The trimethyl silyl sites do not dissociate to form surface charge and C-H bonds are nonpolar. Therefore, surface charge is highly dependent on the ratio and interaction of silanol sites and residual amine sites when submerged in water. The amine sites protonate while the silanol sites deprotonate. Therefore, the pH of the water might be close to the isoelectric point of the modified surface that is not observed in zeta potential, which examines a few atomic layers and HMDS is only one atomic layer.

The difference in charging behavior of the F-SAM and HMDS on a surface site level is not fully understood but are likely due to the C-F bonds being polar and C-H bonds being nonpolar.

The results of the charge decay study over 2 weeks answer the second research question.
The profile on Si_3N_4 wafers changed significantly over 14 days as the charge seemed to diffuse equally over the surface to even it out, including the previously uncharged center that slowly became negatively charged. These findings were in line with findings in literature suggesting that proton hopping at the surface occurred easily with adsorption of water [37, 34, 35, 38].

The surface potential peaks on the F-SAM wafers deteriorated over the two weeks but no other change was identified in the charge profile of F-SAM. This indicated solely a localized interaction, for example, recombination between the differently charged peaks or with ions from the atmosphere but no general charge migration over the surface [36].

No difference was identified in charge profile on HMDS wafers after 2 weeks. The charge seemed to be completely immobile.

The surface conductivity had decreased by a factor of 1000 on the modified wafers compared to the unmodified Si_3N_4, which was the same reduction as was found within literature for HMDS deposited on SiO_2 [14].

The wafer table current measurement found that the wafers with hydrophobic coatings diffused factors less charge than hydrophilic surfaces. When the wafer was clamped, the only current signal identified from the hydrophobic surfaces were within noise level and increase in the humidity had no effect on the charge diffusion. The hydrophobic surfaces diffused 17 times less charge than an unmodified silicon nitride reference.

The results of this study would then conclude that the hydrophobic surface modification is successful in reducing charge diffusion of a wafer backside to surrounding components. The findings seem to confirm the effect of the surface sites shown in *Figure 2. 23*. The schematic showed when the hydrophilic surface

sites are replaced by hydrophobic surface sites, the surface charge generation is smaller and proton hopping is reduced. It seems, however, that proton hopping is almost completely prevented**.**

Both HMDS and F-SAM modified surfaces reduced the surface conductivity of a factor 1000 and showed little to no charge diffusion to a wafer table during clamp experiment. However, the HMDS generated significantly lower surface potential profile than the F-SAM, had 10 times shorter deposition time and is already used within microchip manufacturing process. The HMDS is therefore considered the best wafer backside material to prevent charge diffusion to surrounding components, which answers the fourth and last research question of this project.

6. Conclusions

This thesis studied two hydrophobic monolayers, F-SAM and HMDS, deposited on hydrophilic Si and Si_3N_4 surfaces. Deposition was at elevated temperature and F-SAM deposition was 10 times longer than HMDS. The surfaces were made hydrophobic in order prevent charge diffusion from a charged wafer backside to surrounding components that could affect their performance and yield. It was suggested that hydrophobic surface sites would generate less surface charge during a wet spin rinse process and reduce proton hopping on the surface and thereby decreasing the surface conductivity.

General characterization with XPS and SFE showed that the layers seem to be homogenous and uniform on the sub-nanometer over the whole wafer. The contact angle measurements of modified surfaces were 66^o for HMDS on Si_3N_4, and 100^o-110^o on F-SAM modified surfaces. Rough layer modelling of the F-SAM with a molecule found in literature showed good coverage, which was either attributed to a good fit with the model or the size of the fluorinated molecule is large enough to block neighboring sites and increase the coverage ratio. The coverage of a HMDS surface with the same model showed about 20% coverage.

Rinsing with scrubbing and polishing indicated that it is unlikely that the monolayer will be worn off nor affected by temperature, as baking steps are commonly used to decrease the amount of water within the layers.

It was possible to charge the hydrophobic monolayers from a wet spin rinse process. The F-SAM generated a similar surface potential in magnitude as the reference sample but the potential was limited to the area where the water had been dispensed. The HMDS generated the smallest surface potential profile, even after going through the spin rinse several more times than the F-SAM and HMDS. The difference in how the modified surfaces charge is not fully understood but is likely attributed to C-H bonds being nonpolar and C-F being polar with a dipole moment.

Over the course of 2 weeks, the charge peaks of F-SAM wafer deteriorated but the charge did not distribute over the surface like the reference charge. No change was identified in the HMDS charge profile. The surface conductivity was reduced by a factor of 1000 on the hydrophobic surfaces, indicating that the charge diffusion would be reduced due to hydrophobic surface sites that prevent proton hopping in high relative humidity. The WT current measurements confirmed that the charge diffusion from a wafer backside onto a wafer table was almost completely prevented and not affected by changes in humidity.

The hydrophobic surface modification is therefore considered to prevent charge diffusion from a wafer backside onto surrounding components it comes in contact with. The HMDS is considered the best material option since it generated the smallest potential profile and prevented charge diffusion. Furthermore, its deposition time was 10 times shorter than the F-SAM monolayer and it is already used within photolithography, so it introduces no new materials to IC fabrication.

7. Recommendations

It would be recommended to conduct further tests on the WT current measurement setup with hydrophobic and hydrophilic wafers. Exact mechanisms of charge diffusion need to be studied further to confirm the detected trends and reproducibility.

The difference in charge behavior between F-SAM and HMDS is not fully understood. The difference was expected, [36], and can like be attributed to C-H bonds being nonpolar and C-F bonds being polar, but it was not studied in depth with regard to the different surface sites of these monolayers.

The quality of the deposition could be explored further. For example, it is of interest to know where at the edge the HMDS layer stops during deposition and confirm that it does not spread to the frontside, affecting the IC structures.

Another wear test that but was not within scope of this study is a hydrolytic stability to estimate if the monolayer might degrade from exposure to hydrolysis.

Furthermore, it would be recommended to estimate the efficiency of the particle removal on the hydrophobic surfaces as commonly the wafer backside is rinsed to remove contaminants and particles.

It would be recommended to repeat the zeta potential test and include a reference wafer from the same lot, which should have oxidized to a similar degree. Furthermore, it would be recommended to test a surface that has a known IEP that does not change with time to confirm that the experiment was conducted correctly, such as polytetrafluoroethylene (PTFE) that has IEP of 3.7 [68].

Lastly, it would be advised to conduct a similar study on monolayers deposited on thermally grown silicon oxide substrates. Silicon nitride was chosen due to its popularity, and the characterization results on a silicon oxide modified surface will likely be similar to silicon nitride. However, the silicon oxide has only one type of surface sites, which could provide vital information and even help explain further the results found within this study.

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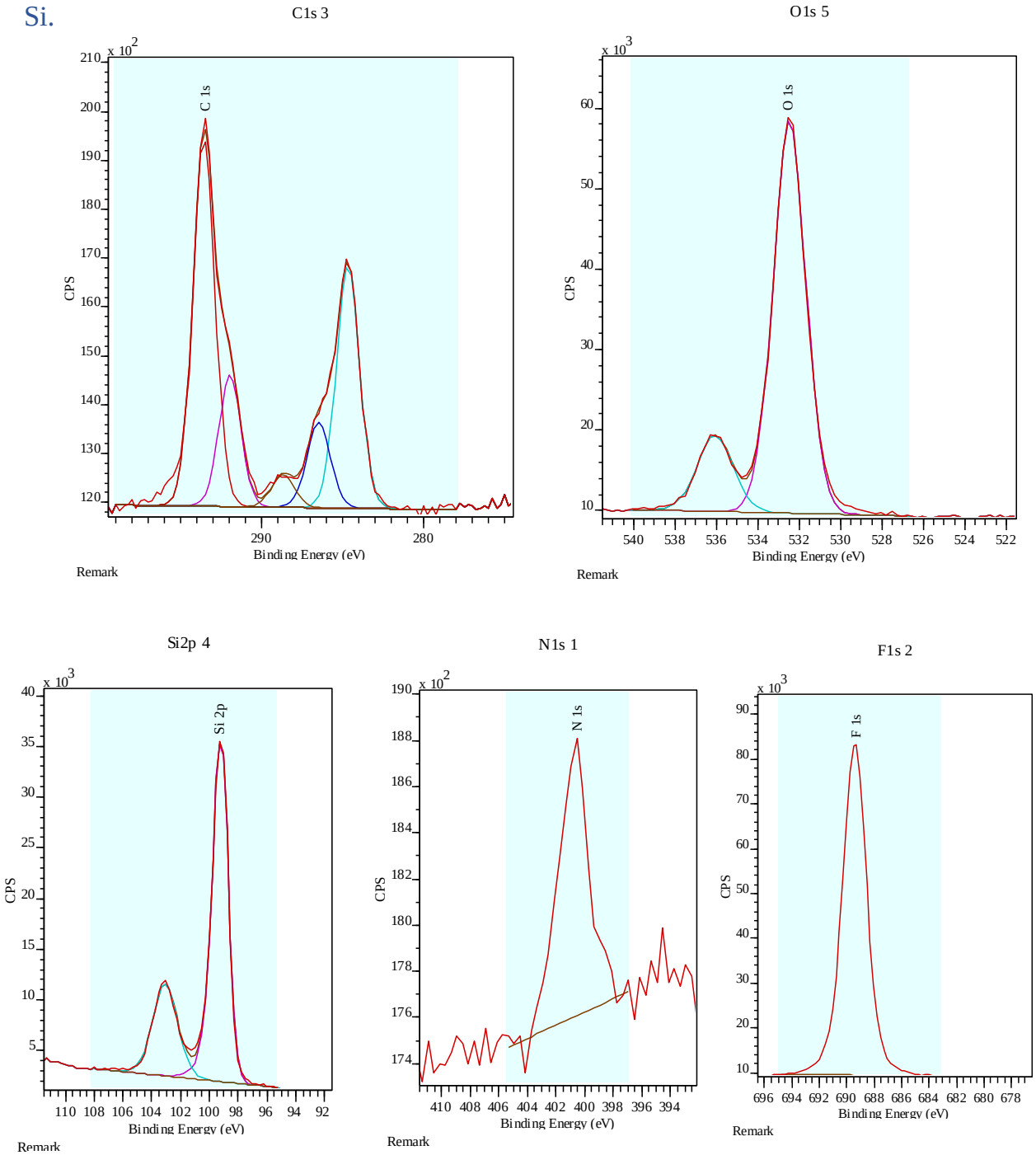
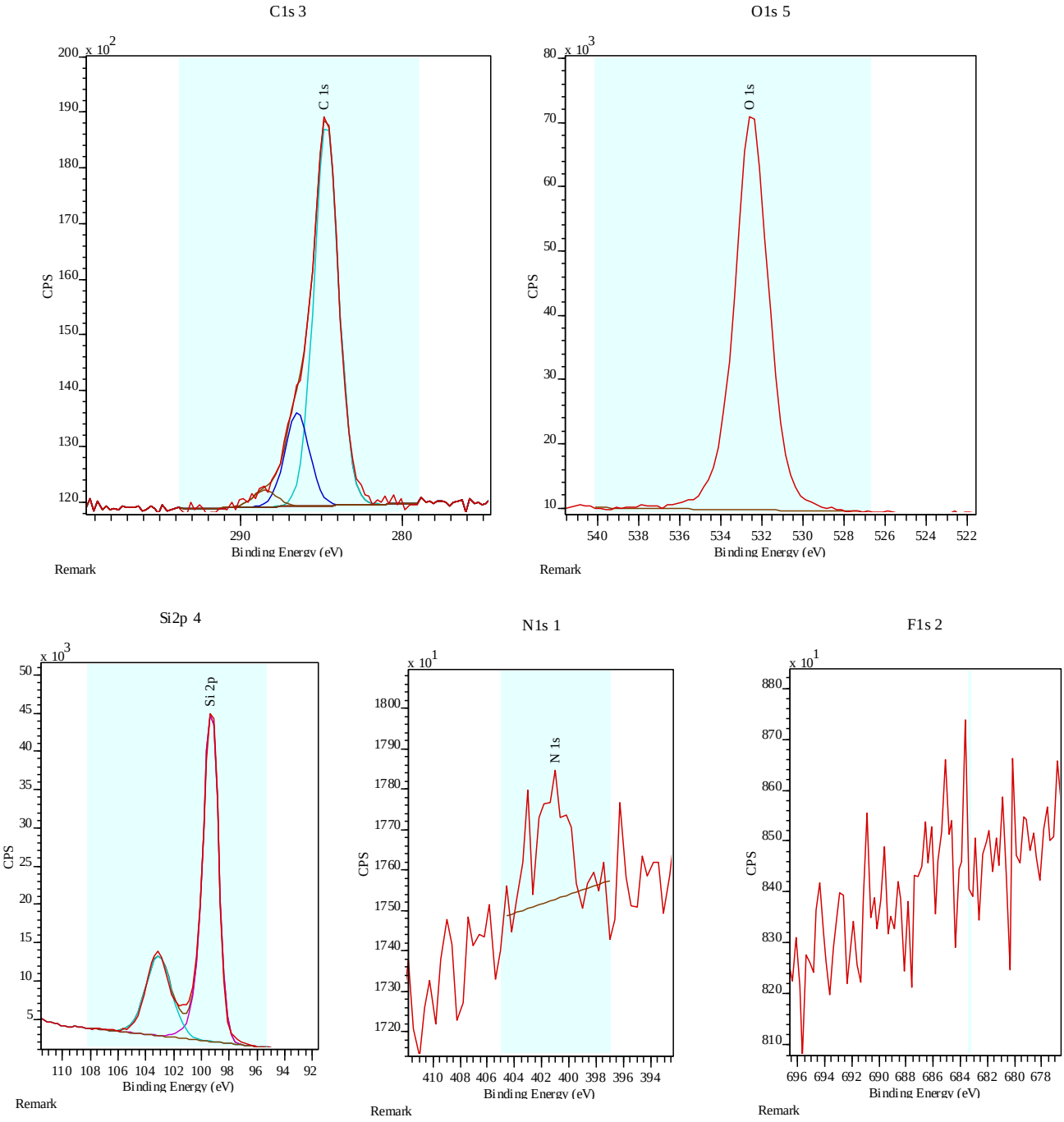
Appendix

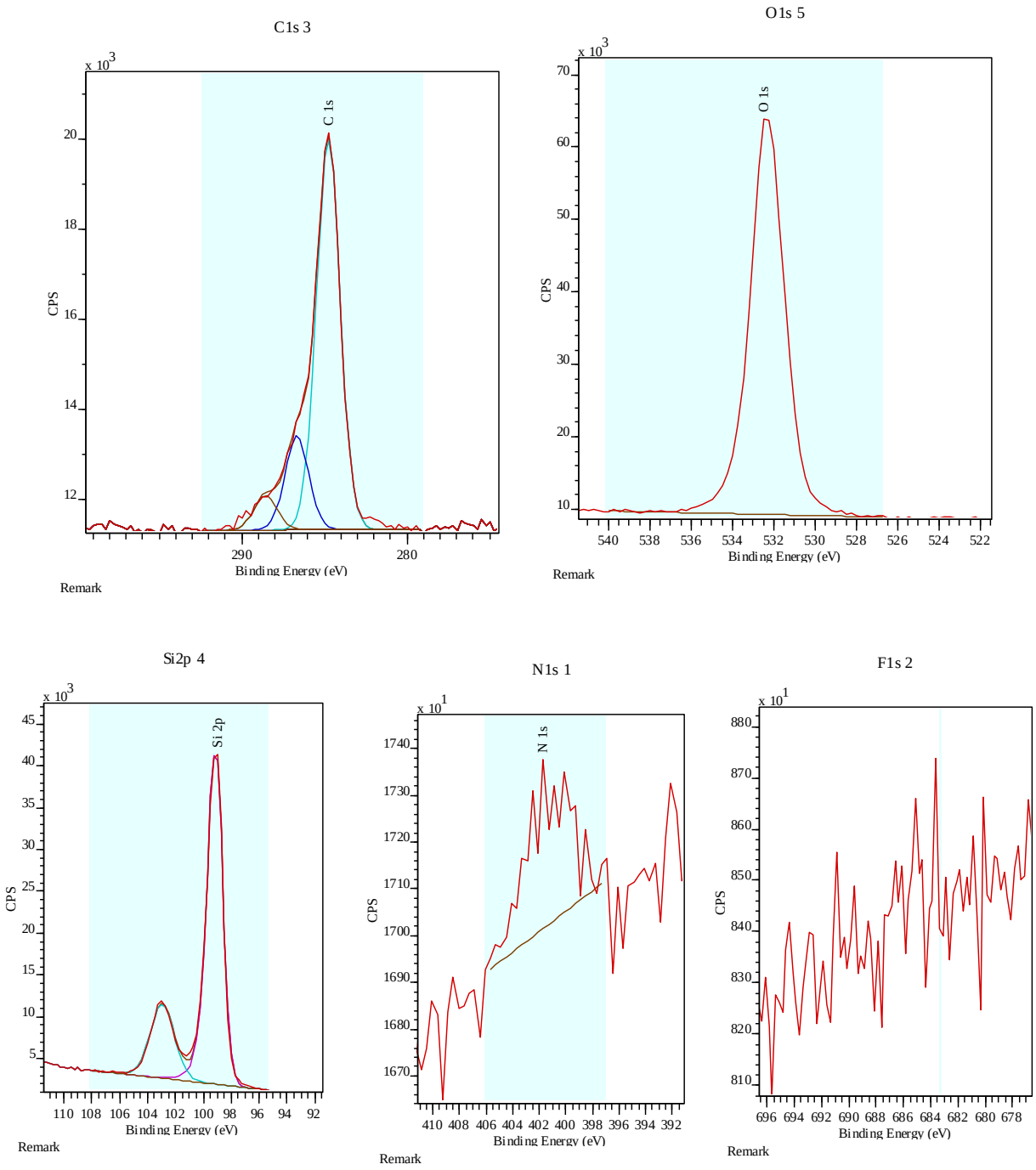
Appendix A: C1s, O1s, Si 2p, N1s and F1s peaks of sample PFTE + Si, HMDS + Si, REF Si.



Appendix A - Figure 1: *C1s, O1s, Si 2p, N1s and F1s peaks of sample PFTE + Si.*



Appendix A - Figure 2: C1s, O1s, Si 2p, N1s and F1s peaks of sample HMDS + Si.



Appendix A - Figure 3: C1s, O1s, Si 2p, N1s and F1s peaks of Si reference.

Appendix B: Wear Resistance

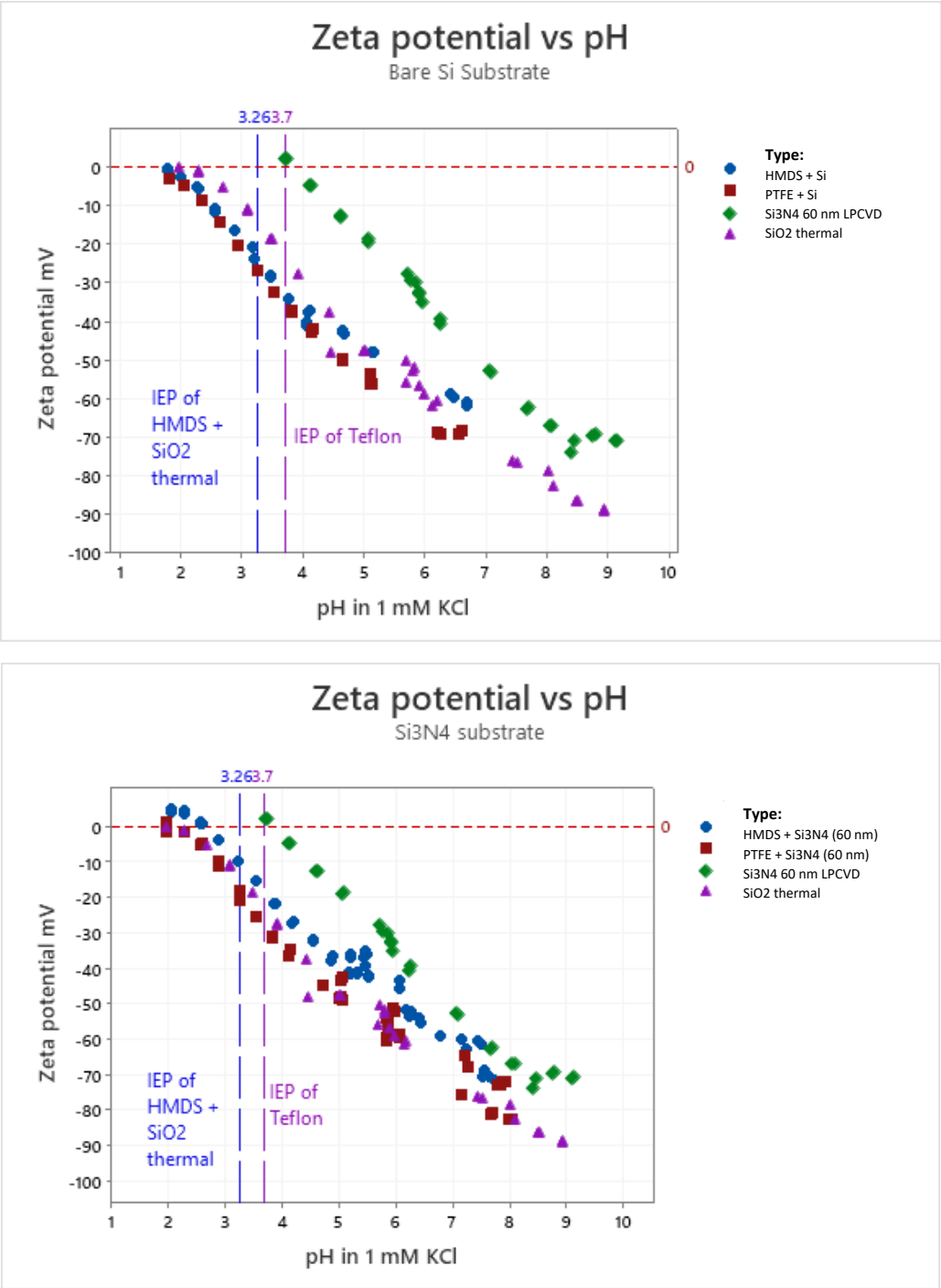
Appendix B - Table 1: Comparison of XPS data before and after wet spin rinsing process with polishing on F-SAM + Si_3N_4 samples

Sample: F-SAM + Si3N4	C 1s					F 1s	N 1s	O 1s	O 1s	Si 2p		Organic overlayer (nm)	SiO2 (nm)	Coverage atom/cm2	Ratio
	285	286.6	288.8	291.5	293.1	689	397	533	536	102	103				
	C_xH_y	CO, CN	OC=O, CF	CF_2, O-C-F_x	CF_3, O-C-F_x	C-F	Si_3N_4	SiO_2	O-C-F_x	Si_3N_4	SiO_2				
Edge No Rinsing Process	1.4	0.7	0.6	1.1	4.7	18.7	27.2	16.5	3.6	20.2	5.2	1.0	0.7	4.1E+14	60%
Center No Rinsing Process	1.6	0.8	0.9	2.0	6.6	26.5	22.4	13.4	4.4	17.3	4.3	1.5	0.7	5.6E+14	83%
Middle No Rinsing Process	1.5	0.8	0.7	1.6	6.2	23.3	24.2	14.6	4.1	18.3	4.6	1.3	0.7	4.8E+14	71%
Edge Post Rinsing w. Polish	1.4	0.6	0.8	2.0	5.8	25.3	23.4	14.5	4.3	17.6	4.4	1.5	0.7	4.8E+14	70%
Center Post Rinsing w. Polish	1.7	0.8	1.0	3.2	6.6	29.3	21.1	12.0	4.6	16.5	3.3	1.8	0.6	7.6E+14	111%

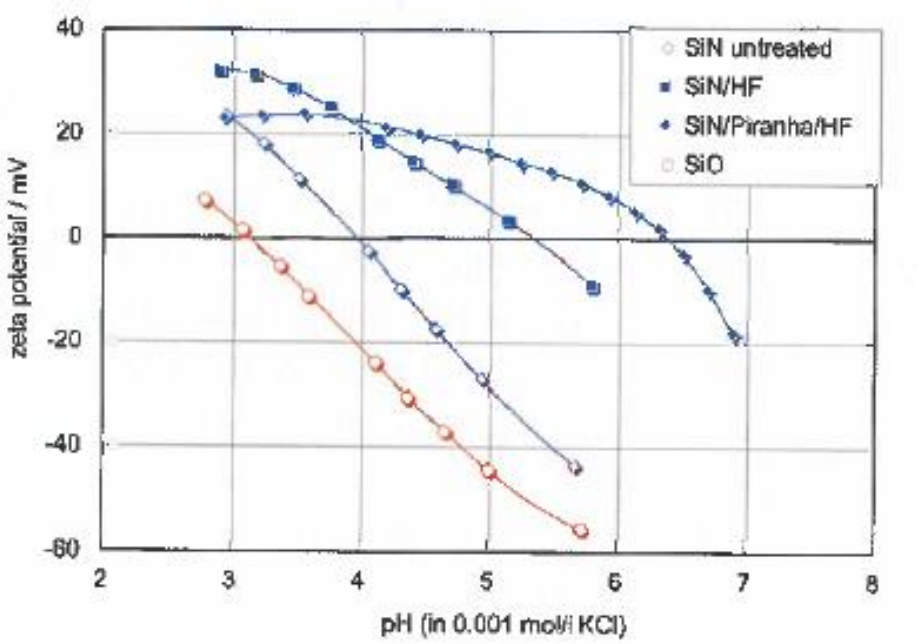
Appendix B - Table 2: Comparison of XPS data before and after wet spin rinsing processing with polishing on HMDS + Si_3N_4 samples

Sample: HMDS + Si3N4	C 1s					F 1s	N 1s	O 1s	O 1s	Si 2p		Organic overlayer (nm)	SiO2 (nm)	Coverage atom/cm2	Ratio
	285	286.6	288.8	291.5	293.1	689	397	533	536	102	103				
	C_xH_y	CO, CN	OC=O, CF	CF_2, O-C-F_x	CF_3, O-C-F_x	C-F	Si_3N_4	SiO_2	O-C-F_x	Si_3N_4	SiO_2				
Edge No Rinsing	3.1	0.4	0.2	0.0	0.0	0.1	42.3	18.8	0.0	29.3	5.8	0.1	0.5	9.5E+13	21%
Center No Rinsing Process	3.3	0.5	0.2	0.0	0.0	0.1	41.5	20.4	0.0	28.5	5.8	0.2	0.5	1.0E+14	22%
Middle No Rinsing Process	3.2	0.5	0.2	0.0	0.0	0.1	41.5	19.5	0.0	29.0	6.0	0.2	0.5	9.9E+13	21%
Edge Post Rinsing w. Polish	2.8	0.4	0.3	0.0	0.0	0.0	41.3	20.6	0.0	29.0	5.7	0.1	0.5	8.65E+13	19%
Center Post Rinsing w. Polish	2.5	1.8	4.2	9.7	35.9	50.4	33.1	16.6	21.1	19.8	3.3	0.1	0.5	8.20E+13	18%

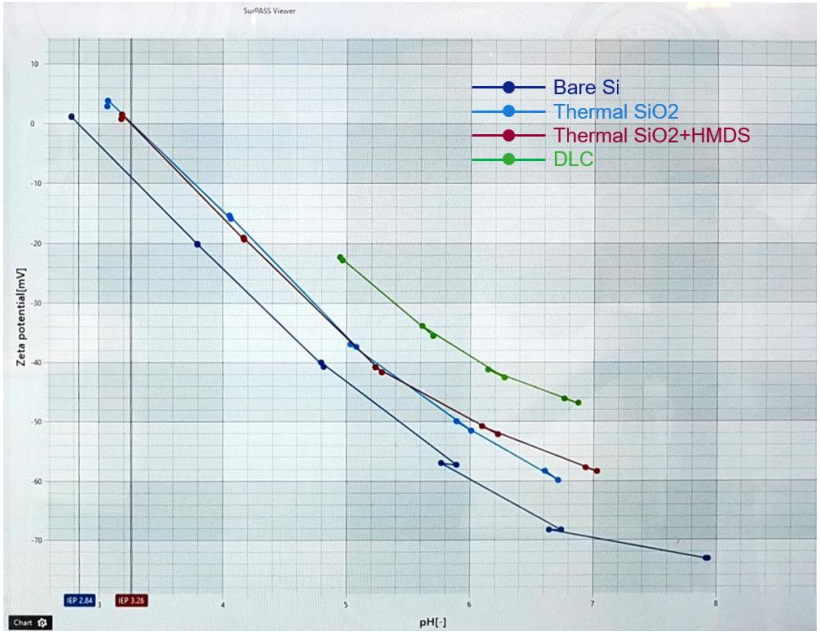
Appendix C: Zeta potential measurements



Appendix C - Figure 1: The zeta potential vs pH for the F-SAM and HMDS samples on each substrate.



Appendix C - Figure 2: Zeta potential vs pH scan of treated and untreated silicon nitride showing different IEP for each surface [15].



Appendix C - Figure 3: Inhouse study within ASML showing zeta potential as a function of pH for relevant samples [69].

Appendix D: The derivation of surface resistance

Appendix D - Figure 1 shows the structure of a circuit model on the surface of a charged wafer. A dielectric layer of thickness t_{ox} and relative permittivity constant ε_r has an intrinsic surface resistance $R\square$ per unit area and capacitance $C\square$ per unit area, which is given by the expression:

Appendix Equation 1: Sheet Capacitance per unit area

$$C\square = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}}$$

The capacitance over a segment of length l in y-direction and Δx in the x-direction becomes:

Appendix Equation 2: Capacitance from sheet capacitance

$$C = C\square l \Delta x$$

The resistance over the same segment is:

Appendix Equation 3: Resistance from sheet resistance

$$R = R\square \frac{\Delta x}{l}$$

When the oxide/dielectric surface is polarized, it is assumed that the charge can move along the surface and into the volume.

The Kirchhoff's current law states that all currents that flow through point V(x) can be summed up to zero. The currents through point V(x) are composed of the currents flowing along the surface and through the volume of the dielectric layer. It gives the following expressions [70] [13]:

Appendix Equation 4: Currents flowing through point V(x) along the surface

$$I_C = I_1 - I_2 = \frac{V(x-\Delta x) - V(x)}{R} - \frac{V(x) - V(x+\Delta x)}{R}$$

Appendix Equation 5: Current flowing through point V(x) through the dielectric layer

$$I_C = C\frac{dV(x)}{dt}$$

With substitution of Taylor expansion,

Appendix Equation 6: Taylor Expansion

$$V(x \pm \Delta x) = V(x) \pm \Delta x \frac{dV(x)}{dx} + \frac{1}{2}(\Delta x)^2 \left(\frac{dV(x)}{dx}\right)^2$$

The equation is simplified to one-dimensional Fick's second law of diffusion with diffusion constant D:

Appendix Equation 7: Fick's second law of diffusion

$$\frac{dV(x)}{dt} = D\frac{d^2V(x)}{dx^2}, \qquad D = \frac{(\Delta x)^2}{RC} = \frac{t_{ox}}{R\square \varepsilon_0 \varepsilon_r}$$

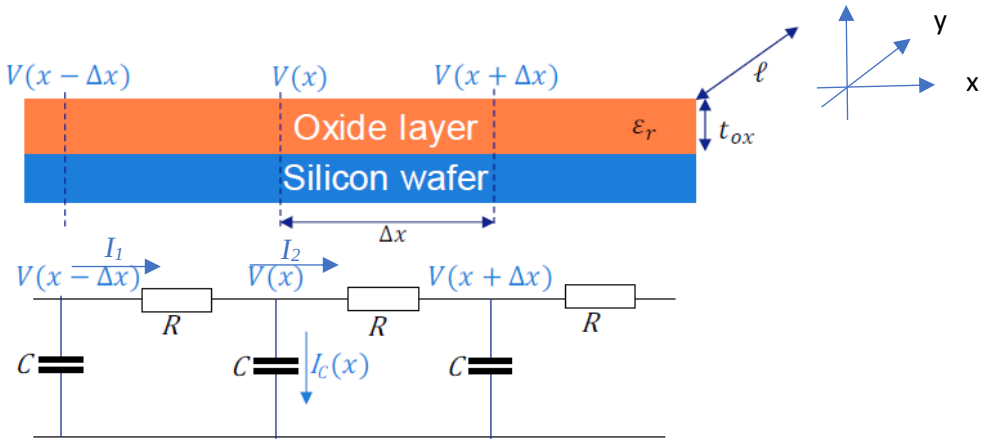
The equation can be generalized for all three dimensions.

In the case of a wafer with diameter of a and an initial charge at time t = 0, the conditions for a solution V(x,t) become $-a/2 \leq x \leq a/2, V(x,0) = f(x)$ and $V(x,0) = V(x,L) = 0$.

There are many solutions to Fick's 2nd law. If the voltage over the wafer in one-dimensional case is denoted into a vector, $\vec{V}(t)$, the equation becomes [70]:

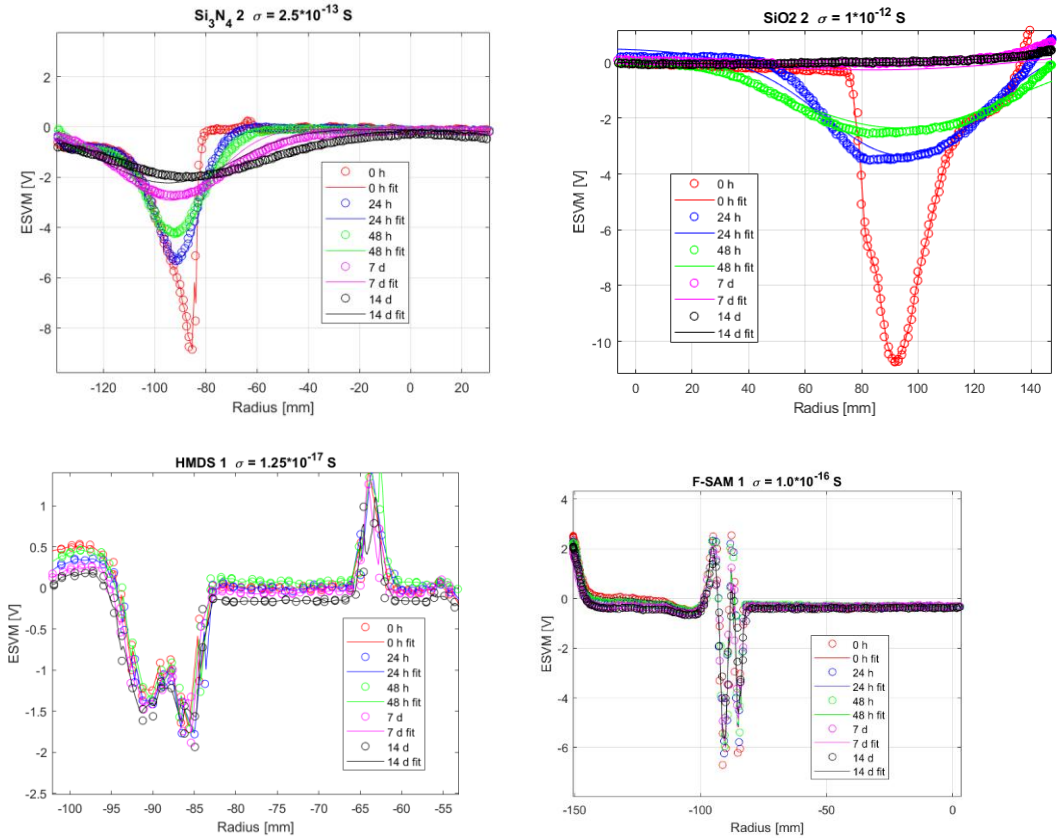
Appendix Equation 8: Solution to 1D Fick's second law

$$V(t+\Delta t) = \left(I + \frac{\Delta t}{RC} D\right)^{\frac{t}{\Delta t}}$$



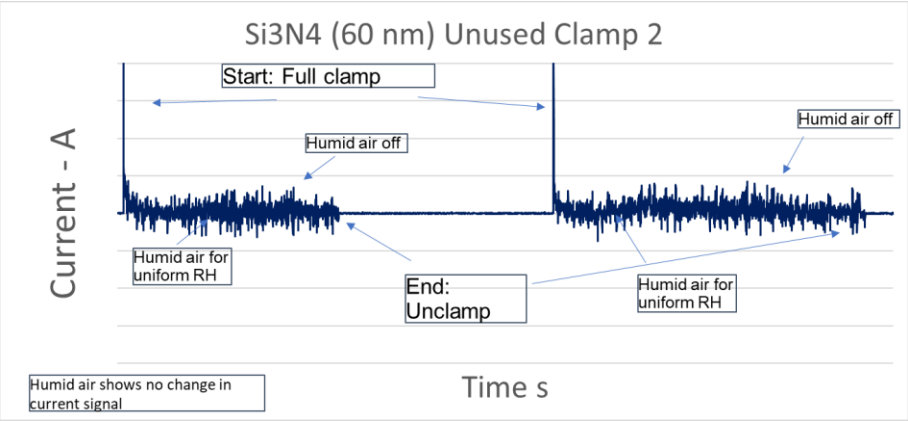
Appendix D - Figure 1: Surface conductivity model of an dielectric layer with (semi)conductive surface [70] [13].

A code was written to estimate the surface conductivity by fitting the model to the data measured over the 2 weeks [70].

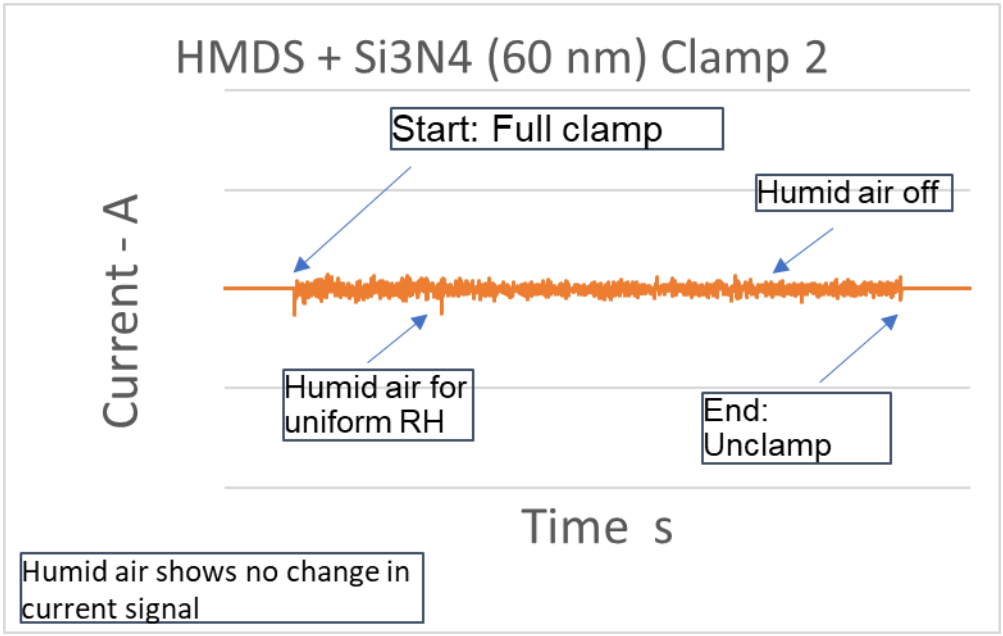


Appendix D - Figure 2: Graphs showing surface charge decay over 2 weeks fitted with the lumped circuit model described above. The σ (1/R□) was fitted to estimate the surface conductivity.

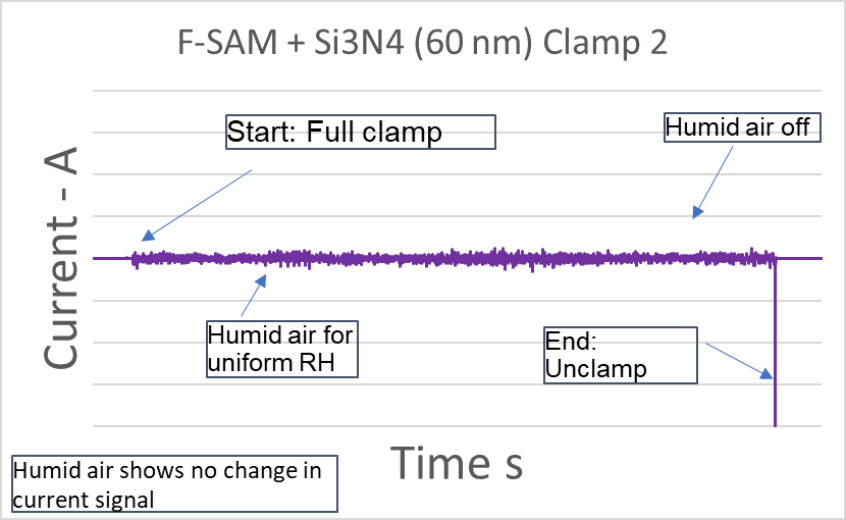
Appendix E: WT current measurements



Appendix E - Figure 1: Graph shows current signal of Si_3N_4 (60 nm) unused reference wafer in its second time it was placed on the wafer table. The wafer was clamped twice due to adjustment to the settings of the humid air. The main signal identified is from the clamping. The signal is very noisy but seems to be generally a bit above 0.



Appendix E - Figure 2: Current signal of HMDS + Si_3N_4 (60 nm) wafer. The clamping peaks are very small and the signal when clamped is within noisy. No difference is identified when humid air is provided to the system.



Appendix E - Figure 3: Graph shows the current signal when the F-SAM + Si_3N_4 (60 nm) wafer was clamped for the second time. Here the clamping peak is negligible, but the unclamping peak is negative and quite large. The signal during loading is within noise level and the effect of humid air is negligible.