

Full Duplex CMOS Duplexer Passive Self-Interference-Cancellation

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List of Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter
ADS	Advanced Design System (<i>Agilent EEsof</i>)
BOM	Bill of Materials
CCG	Common centroid geometry
CM	Common Mode
CMOS	Complementary Metal-Oxide Semiconductor (<i>transistor type</i>)
DAC	digital-to-analog converter
DC	Direct Current
DR	Dynamic Range
DRC	Design Rule Check
DUT	Device under test
EMI	Electromagnetic Interference
FDD	Frequency-division Duplex
FET	Field-Effect Transistor
HD	Half Duplex
IC	Integrated Circuit
IMEC	Interuniversity Micro Electronics Center (<i>research institution, Leuven,</i>
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LNA	Low Noise Amplifier
LTE	Long Term Evolution (<i>3GPP 4G technology</i>)
MAC	Media Access Control
MIM	Metal-Insulator-Metal
MIMO	Multi-Input Multi-Output
MM	Mixed Mode
MOS	Metal-Oxide Semiconductor
NF	Noise Figure
NMOS	Negative-Channel Metal Oxide Semiconductor
PA	Power amplifier
PCB	Printed Circuit Board
PEX	parasitic extraction
PIFA	Planar Inverted-F (<i>type</i>) Antenna
PIN	Positive - intrinsic - negative (diode type)
PMOS	Positive-Channel Metal Oxide Semiconductor
QAM	Quadrature Amplitude Modulation
RF	Radio frequency
Rx	Receiver
SIC	Self-interference cancelation
TDD	Time-division Duplex
TEM	Transverse Electromagnetic

Tx	Transmitter
UMC	United Microelectronics Corporation
VDD	Voltage Drain Drain (<i>semiconductors</i>)
VNA	Vector network analyser
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

List of symbols

α	autotransformer tap location
β	power ratio
γ	body effect parameter
μ_n	electron mobility
C	capacitance
ΔC	capacitance step
F	noise factor
f	frequency
g_m	transconductance
i	current
IL_{Rx}	receiver insertion losses
IL_{Tx}	transmitter insertion losses
ISO_{Tx}	transmitter isolation
k_m	magnetic coupling coefficient
L	self-inductance
M	mutual inductance
n	turns ratio
n_{eff}	effective turns ratio
N	number of turns
P	power
Q	quality factor
R_{Ant}	resistance at Antenna port
R_{Bal}	resistance at Balance port
v	voltage
Z_{Ant}	impedance at Antenna port
Z_{Bal}	impedance at Balance port
Z_{Rx}	impedance at Receiver port
Z_{Tx}	impedance at Transmitter port

Preface

Jiayuguan or Jiayu Pass is the first pass at the west end of the Great Wall of China, near the city of Jiayuguan in Gansu province. The pass is also known by the name the “First and Greatest Pass Under Heaven” (天下第一雄关). Construction of this fortress began sometime around 1372.

According to legend, when Jiayuguan was being planned, the official in charge asked the designer to estimate the exact number of bricks required and the designer told him 1.359.648 bricks. The official questioned his judgment, asking him if that would be enough, so the designer added one brick. When Jiayuguan was finished, there was one brick left over, which was placed loose on one of the gates where it remains today.



(a) Jiayuguan



(b) the left over stone

One day, I would like to leave the remaining stone above the gate of my design.

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Abstract

To accommodate the growing demand for wireless communications, new techniques are required to increase throughput of wireless networks. One technology aiming to increase the spectral efficiency of wireless devices is full duplex (FD) radios. These systems are capable of single carrier transmission and reception and could ideally double the spectral efficiency of future wireless systems. To make such systems a commercial reality, self-interference cancellation (SIC) techniques are required to suppress transmitter leakage into the receiver. This work investigates the level of SIC an integrated hybrid transformer can provide to make FD a reality.

This work also includes an investigation in the SIC capabilities of an integrated hybrid transformer operating with a commercially available planar inverted-F antenna (PIFA) and presents the design and evaluation of a prototype in UMC 180nm RFCMOS. The prototype consists of a transformer, a tunable impedance and a LNA. Measurement results on this prototype showed isolation peaks of 80 dB, with an isolation band width of 1 MHz for 60 dB isolation and a Tx insertion loss, measured gain and NF of 3.5 dB, 5dB and 9dB, respectively, while providing a IIP3 of 0dBm at the LNA output and a common-mode Tx isolation at the input of the LNA of 20 dB.

The measurements also showed that the duplexer can be made self-tunable by using search algorithms that converge within 150 measurements. The relation between isolation and impedance resolution is derived and proven to be 6dB every time the absolute difference between the impedances at both sides of the transformer is halved.

Chapter 1

Introduction

In wireless, it is generally considered technically impractical to simultaneously transmit and receive over a single carrier frequency [1]. The main problem of concurrent operation over a single frequency is that it is difficult to prevent part of the high power transmit (Tx) signal from leaking into the receiver (Rx). The power level of the Tx signal is usually orders of magnitude larger than the Rx signal, as this signal is expected to incur significant losses before arriving at its destination. Therefore the Tx power level lies far outside of the dynamic range (DR) of the receiver's circuitry. This Tx leakage problem is illustrated in Figure 1.1, where both the desired and undesired signals flowing between the antenna and transceiver front-end are illustrated. If the power level of the Tx signal leaking into the receiver is too high, the analog stages of the receiver will overload, preventing proper reception. Therefore, any transceiver requires a scheme to isolate the receiver from the brunt power of its own Tx signal.

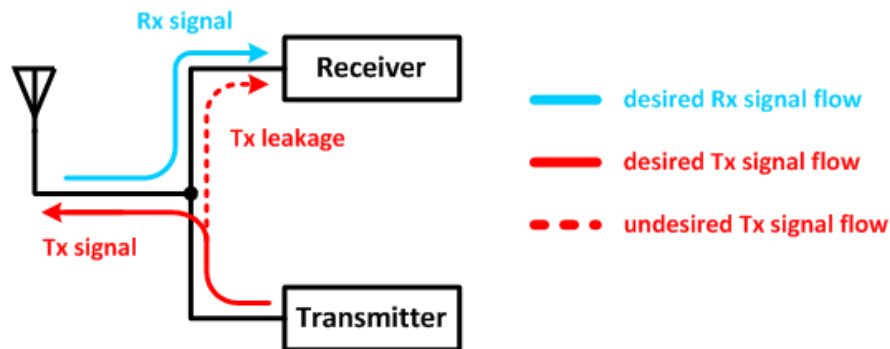


Figure 1.1 Radio front-end signal flows

To provide isolation, most conventional bi-directional wireless systems use either time-division duplexing (TDD) or frequency-division duplexing (FDD), to separate up- and downlinks in time or frequency, respectively. In TDD systems, isolation is provided using a switch to prevent a direct path between transmitter and receiver by connecting them to the antenna at different time slots. In FDD systems, the Tx and Rx use different carrier frequencies. This allows separation using filters. As TDD and FDD schemes separate Tx and RX in time or frequency both are not able to establish a bi-directional wireless link across a single channel, and can therefore be considered half-duplex (HD).

With the demonstration of a full-duplex (FD) radio in 2009, this conventional presumption that Tx and Rx required separation in time or frequency, was overturned [2]. A FD radio is a wireless system able to transmit and receive simultaneously over a single carrier. The conceptual difference in time and frequency utilization for TDD, FDD, and FD systems is given in Figure 1.2, together with block diagrams of their possible front-end implementation. From frequency time plots in Figure 1.2, it can be observed that FD requires only a single frequency band to transmit and receive simultaneously. Therefore, ideal FD doubles the throughput of an HD system when provided with equal spectral resources. The front-end implementation for FD shows the symbol of a hybrid transformer, which is proposed in this work to cancel the undesired Tx-leakage.

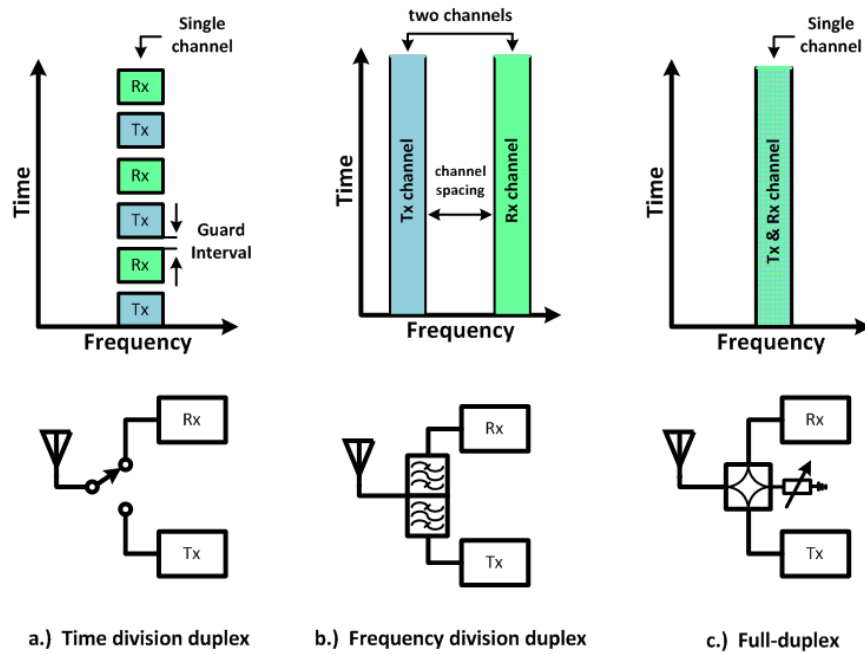


Figure 1.2 Duplexing (a) time division (b) frequency division (c) full duplex

However, to realise FD capability, the negative impact of self-generated Tx-interference has to be cancelled. Recent implementations of FD prototypes combine antenna, analog circuit, and digital processing techniques to provide up to 100dB of cancellation [2] [3]. These techniques are referred to as self-interference cancellation (SIC) techniques. The SIC techniques used in these FD prototypes and their effectiveness in attenuating Tx-interference is illustrated in Figure 1.3. These prototypes demonstrated that a combination of SIC techniques throughout the receiver chain can push a 0dBm self-interference signal below the noise floor of the receiver, where it no longer degrades receiver sensitivity.

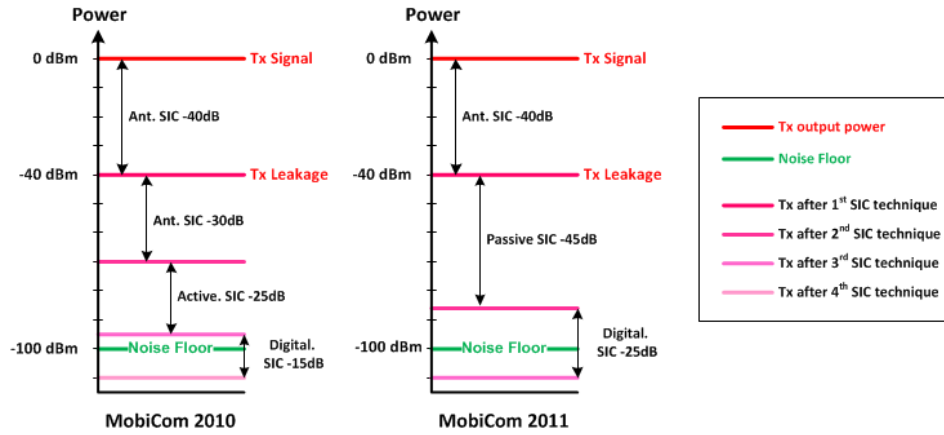


Figure 1.3 Combined SIC techniques to suppress TX leakage

SIC techniques can be classified into four categories: antenna, passive, analog, and digital. A comparison of these categories in terms of noise, dynamic range, form factor, and main drawback is given in Table 1.1. Using these properties, the sequence of SIC techniques with the least impact on receiver performance and maximum SIC can be surmised. If Tx signal is insufficiently attenuated before the analog-to-digital converter (ADC), it becomes desensitized to the Rx signal, because its resolution is squandered on coding the Tx interference. This results in a digitized Rx-signal with insufficient resolution to provide effective digital cancellation. Active SIC stages require preceding gain as the active devices used in their implementation generate additional $1/f$ noise. They also require proceeding SIC as their dynamic range is limited by the supply voltage and linearity, causing them to compress or saturate.

Table I SIC technique comparison

SIC domain	Noise	DR	Int.level	Main drawback
Spatial/Antenna	thermal	High	off-chip	Requires multiple antenna
Passive	thermal	High	on-chip	Insertion losses degrade transceiver performance
Active	active	Limited	on-chip	Requires preceding SIC and Gain stage
Digital	quantization	Number of bits	on-chip	Performance depends on proper operation of the receiver and ADC

As no SIC technique provides sufficient cancellation, a combination of several SIC techniques is required to enable FD capability. A possible SIC distribution in the receiver chain is given in Figure 1.4. Here active SIC is placed after the antenna and (or) passive SIC as it becomes less effective when subjected to high powers. It should

also be located after the LNA to reduce its noise contribution. Digital SIC become ineffective when preceding stage compress or saturate as the digitized signal it receives from the ADC is corrupted. So both active and digital SIC techniques, requires a high dynamic range SIC stage in the front-end to isolate them from the unattenuated Tx-signal. This implies either antenna or passive cancellation. The problem with antenna SIC is that it requires multiple antennas to implement [2] [3]. This increases the bill-of material (BOM), and thus the cost of an implementation. Other drawbacks of antenna SIC are that antennas operating at 2.45 GHz are large ($\frac{1}{4}$ wavelength ≈ 3 cm) and require spatial distance between antennas (40 cm). These drawbacks exclude multiple antenna FD systems as a means to provide FD capability to commercial handheld devices. Therefore the development of a passive SIC stage allows a realization of a competitive FD product.

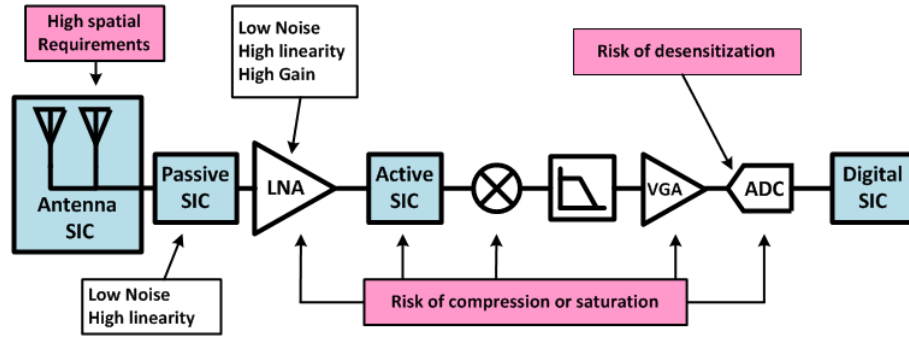


Figure 1.4 Surmised SIC distribution receiver chain

However passive isolation in FD front-end cannot to be realized using filters or switches, and directional isolation provided by circulators are difficult to integrate as their operation is wavelength dependent. If integrated isolation is desired another solution is required. A circuit that can provide isolation in an integrated form and allow concurrent operation over a single frequency is the hybrid transformer [4]. Figure 1.5 gives the symbol of this four port device. In this figure, the four ports are designated as A, B, C, and D are divided in two conjugate pairs A D & B C. Where the term conjugacy as used here has nothing to do with complex math, but instead refers to a conjugate pair consisting of two ports (say A D). This means that these ports can be electrically isolated from each other and also have similar but opposite signal transfers to the other conjugate pair (B C), provided the impedances used to terminate the other conjugate pair (B C) are equal. The degree of conjugacy between the ports (A D) depends on the difference in the impedances connected to ports B and C (or vice versa).

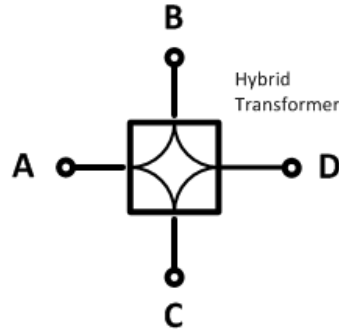


Figure 1.5 A Hybrid transformer with ports A B C D

So if the ports A and D are connected to the transmitter and the receiver, the receiver is isolated from transmitter if equal impedances are connected to ports B and C. This effectively makes the hybrid transformer a duplexer as it allows bi-directional communications across a single medium (frequency band).

1.1 Thesis Topic

The subject of this thesis is the development of a CMOS Duplexer for a single antenna wireless FD system, which operates in conjunction with a commercially available planar inverted-F antenna (PIFA) resonating at 2.45GHz [5]. This duplexer has two main tasks. The first is to provide connectivity between the antenna, receiver, and transmitter. The second is to provide front-end SIC in order to isolate following receiver stages from the main power of the Tx-signal. It should perform these tasks with minimum impact on overall transceiver performance.

1.2 Motivation

Figure 1.6 shows the exponential growth in wireless communication data during the last decade and the projected growth until 2020 [5]. As this growth continues, the spectrum available for data communications will become increasingly congested. This makes it socially and economically attractive to develop techniques and evolve standards to increase the data throughput capabilities of wireless infrastructure. The previously mentioned FD duplexer can help enable future wireless networks to accommodate the increasing demand, by facilitating the development of FD wireless networks. Where FD capability, ideally promises to double the spectral efficiency of established wireless networks.

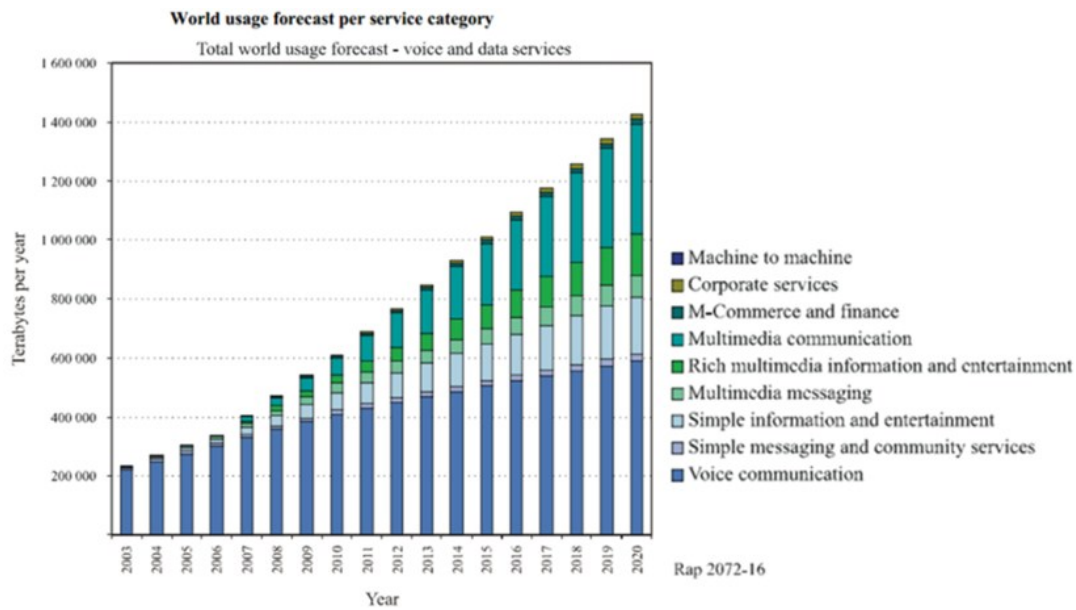


Figure 1.6 World data usage forecast per service category [5]

1.2.1 Advantages of Full Duplex

The ability to simultaneously transmit and receive over a single carrier has a number of advantages for wireless networks. At the physical layer, FD theoretically increases spectral efficiency of HD systems. For TDD, an FD radio has demonstrated an 84% medium throughput gain over a HD equivalent [2]. In this experiment the theoretical 100% was not reached due to the limited processing speed of the setup. FDD networks benefit, as FD allows reuse of spectral resources. This will free up frequency bands to allow more users within a given spectrum, or allow more bandwidth to the same number of users providing them with more capacity.

Improvements in the data-link layer result from three factors. Firstly, data transmission latency is reduced, as nodes no longer have to divide their time between data communications and network control signalling. Secondly, receiving nodes are able to transmit a busy signal while receiving a packet. This reduces packet collisions, as both the transmitting node and receiving node can inform neighbouring devices of an on-going transmission. In TDD systems this is not possible, as the receiving node cannot transmit during reception. This inability results in a situation where only the nodes within the range of the transmitting device can be informed of an on-going transmission. Thirdly, a receiving node can immediately start forwarding an incoming packet after resolving its destination. As this transfer has already been allocated the

required spectral resources, these same resources can be reused for immediate forwarding by following nodes. This allows packets to rapidly flow through a network.

These three factors provided increased performance when implemented in a FD medium access control (MAC) protocol operating in conjunction with FD capable nodes [3]. The MAC protocol instructs nodes to immediately start relaying packets after resolving their header. Through this immediate retransmission three objectives are accomplished. A sending node is informed of proper reception. All nodes in range of both the receiving and sending nodes are informed of an on-going transmission, and the packet is forwarded to the next node. The controlled experiments showed an 88% reduction in collisions. It also demonstrated a 10% increase in fair distribution of network resources, and an up- and download throughput gain of 110% and 15%, respectively, were achieved. The asymmetry was caused by limitations in the hardware.

Also FD multiple-input multiple output (MIMO) models were found in a survey of the literature [6] [7] [8]. MIMO systems use multiple antennas to increase throughput by multiplexing or beam forming [1]. Although beyond the scope of this work, these works are noted to complete the list of works concerning FD development. All three works reported simulation results that showed increased performance with FD capable devices. Reference [6], however notes that these results were obtained using model simulations. Therefore, more practical research is required to evaluate the negative impact of practical FD system imperfections. Although FD seems promising, actual field tests have not been reported. Therefore the actual benefits of FD are still to be proven in a practice.

The main drawback of FD systems is the range limitation imposed by the SIC provided in the receiver. The range of a transceiver is for a large part governed by its output power. If the Tx-power increases to the extent that the SIC provided in the receiver is not capable of attenuating the resulting interference, proper reception is prevented. Therefore the range of a FD system can only be extended by improving receiver SIC performance. Each additional SIC stage requires resources to develop, implement, and operate. Therefore, the price of a FD system increases with its range, limiting the range at which FD capability proves economical, or physically possible. Therefore only short range applications really stand to benefit unless significant advances can be made in SIC techniques.

1.2.2 Commercial Applications

Besides the technical merits of developing circuits that enable future networks to support the growing demand for wireless communications, there is also a commercial incentive. Wireless devices such as smartphones, tablets, and laptops have become very popular in recent years. These come with significant a processing capability which allows them to be used for a variety of applications other than telephone calls. These applications such as music, video, social media, and browsing require more data capacity to support, and thus data usage has increased dramatically with the introduction of 3G broadband and 4G long term evolution (LTE) [9]. To many people, the benefits provided by these mobile devices and the networks supporting them, have become an indispensable part of life. This trend is expected to continue; commercial opportunities await any party able to accommodate this continued growth.

However, because of its limited transmission range, FD capability may initially only find its way into applications, which require high throughput over short range. One could think of applications, such as femto cell access points used in 3G and 4G networks, in areas such as major transport hubs, shopping malls, festivals or other location with a large user density. This small cell market is forecasted to be worth 2.7 billion dollars by the year 2017 [10]. In order to connect to FD networks mobile devices need to be fitted with FD capability. With the total mobile devices shipped across the world in 2013 being 2.3 billion units this provides a sizable market [11].

However, the size and cost constraints on mobile device are severe. This is especially true for small devices such as phones and dongles, which cannot accommodate multiple antennas. These applications would therefore benefit from isolation provided by integrated passive SIC techniques such as electrical balance based solutions. Moreover, passive SIC solutions could be utilized in fixed access points to increase the overall receiver SIC performance and extend the range of their transmitters.

In areas which do not merit the installation of the more expensive FD infrastructure, due to low data demand and large area coverage, FD capability is less likely to be adopted. At these locations HD networks will continue to dominate by providing more range for less cost. Figure 1.7 presents an example of FD capable devices integrated within the existing wireless infrastructure.

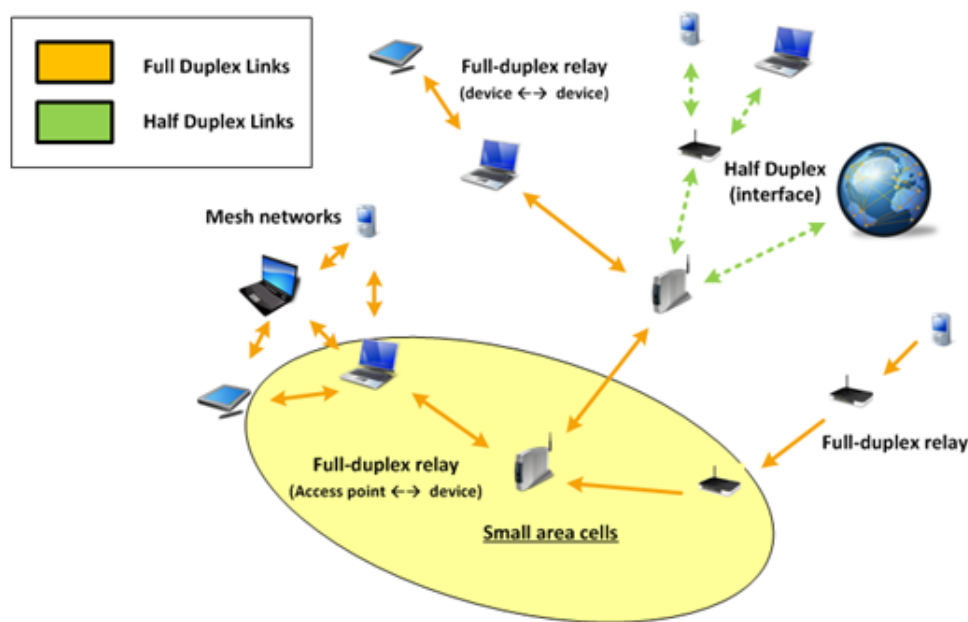


Figure 1.7 Possible Full-Duplex Applications

1.2.3 Hybrid Transformer Duplexer

The development of a hybrid transformer as a means to provide Tx-to-Rx-isolation in the front-end of a FD system is motivated by three factors. First, a hybrid transformer is a relatively simple circuit consisting of only a transformer and a tuneable impedance. The second factor is the passive nature of both this impedance and the transformer. Passive components only generate thermal noise, and therefore the noise contribution of the hybrid transformer is minimal compared to active solutions. Passive components also behave very linearly. This minimum noise contribution and high dynamic range allow the hybrid transformer to provide front-end SIC while having a minimum impact on the transceivers performance. The final factor, which makes it attractive for FD, is its ability to allow concurrent operation over the same frequency by providing isolation using the conjugate properties of its four ports.

Three implementations of hybrid transformer have demonstrated their potential to provide isolation. The first was a discrete circuit providing 50dB peak isolation at 863 MHz [12]. Later two integrated circuits used electrical balance to provide 55dB [13] and 70 dB [14] isolation around 1.9GHz for wideband code division multiple access (W-CDMA) applications.

There are however two disadvantages of the hybrid transformer as a duplexer. First the transformer requires a substantial chip area to implement which makes it costly to integrate. Secondly, conjugate properties of the hybrid transformer which allow it to isolate ports, also come with inherent Tx and Rx insertion loss. But provided sufficient SIC could be obtained these power losses can be acceptable for certain low output power transceivers.

1.2.4 Single Antenna Prototype

Although multiple antennas, allow the utilization of antenna cancellation in order to isolate the receiver from the unattenuated Tx-signal, they also significantly impact the size and cost of a system. Antenna size is determined by the wavelength of operation. In most cases they cannot be made significantly smaller than $\frac{1}{4}$ of the wavelength of operation. Each additional antenna also requires additional resources to connect and operate the antenna. This impacts the bill-of-materials and the assembly cost of a final product. In a survey of the literature, two publications on single antenna FD systems were found. Both of these describe discrete implementations. In [15], a dedicated two feed antenna, a passive cancellation stage, and an active cancellation stage, realised 59dB of isolation at 950MHz. The second FD wireless system functioned using a general antenna, a passive circulator followed by a passive tuned cancellation circuit. This circuit consisted of a coupler, phase shifter, attenuator, and combiner. The complete SIC chain provided 75 dB isolation across a 10MHz bandwidth at 2.45GHz [16].

1.2.5 Integration

All previous FD setups used off the shelf hardware, or discrete components. However if FD is ever to become an alternative to the established HD wireless networks, their performance versus cost trade-off has to be competitive. Therefore FD capability will have to be provided in a similar level of integration in order to benefit from the same reduced BOM and assembly cost. As HD duplex products are commercially available in dedicated integrated circuits, the only way for to compete is to provide FD capability in integrated circuits.

1.2.6 CMOS

CMOS technology is favoured by consumer electronics for its low cost, higher yield, and its ability to co-integrate analog and digital circuits on the same die. Therefore, if CMOS is able to provide sufficient performance this will be the process of choice. Previous implementations of integrated duplexers using the hybrid transformer were implemented in 40nm [17], 65nm [18], 90nm [14] CMOS. This work presents a design in 180nm because electrical balance duplexers consist mostly of large area passives whose performance is not dependent on small feature size. The challenges using 180nm CMOS will be the realization of high quality passives with 1P-6M metal stack in combination with the 10-20 Ω substrate resistivity common to RF CMOS processes. Furthermore, the feature size of the process will constrain the R_{on} of the active devices, and the minimum available capacitance value needed to implement the tunability in the duplexer.

1.3 Thesis Objectives

The objective of this thesis is to investigate how much isolation and isolation bandwidth can be obtained with a CMOS hybrid transformer and a commercially antenna. This is done by investigating three aspects. The first aspect is how hybrid transformers provide isolation. The second aspect is how the level of isolation trades-off with other RF performance characteristics. The third aspect is how these trade-offs are related to technology parameters. The investigation is done by evaluating the design of duplexer prototype fabricated in UMC 180nm MM/RF CMOS technology [19].

1.4 Thesis Outline

The organization of this thesis is as follows. Chapter 2 discusses prior art in FD radios and integrated duplexers. After this, the chapter continues to describe the proposed RF aspects of FD radio and finishes with a description of the different concepts used in the design. In Chapter 3, the design of a duplexer prototype in UMC 180nm RF CMOS is presented. This is followed by chapter 4, where the layout of the test circuit is shown together with the impact of the layout on circuit behaviour. Then in chapter 5, the measurement setup and the experimental results are presented and discussed. Finally, Chapter 6 draws conclusions and provides suggestions for future work.

Chapter 2

Electrical Balance Duplexer

This chapter presents the theoretical background of this thesis. It starts with a description of the electrical balance duplexer, which consists of a transformer and a tunable impedance. First the transformer will be explained. The discussion will then continue with the tunable impedance, which will be referred to as the balancing circuit. This name follows from the fact that the tunable impedance balance with the antenna impedance to provide isolation.

2.1 Electrical Balance Duplexer

A tunable electrical balance duplexer is realized by connecting a balancing circuit to one of the port of a transformer, while connecting the other three ports to an antenna, a transmitter, and a receiver as shown in Figure 2.1.

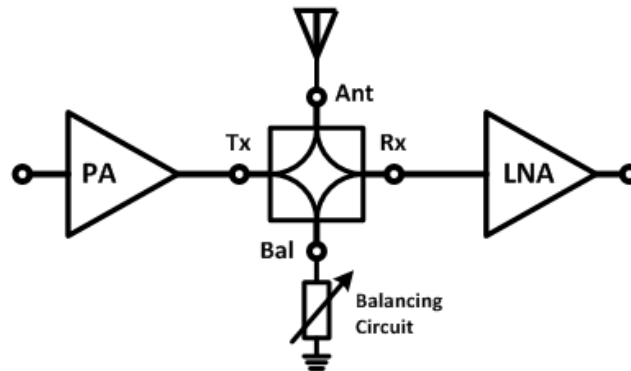


Figure 2.1 Hybrid transformer as duplexer

In order to ease the discussion on the duplexer, these four ports of the transformer will be referred to as the Tx, Rx, Ant (antenna), and Bal (balancing circuit) port. Isolation is provided between the Tx and Rx ports, if the impedance at the Bal port is equal to the impedance at the Ant port, i.e., the balance condition. The amount of Tx-to-Rx isolation is related to the accuracy with which the two impedances match each other. To isolate the LNA from the PA, the impedance provided by the balancing circuit should mimic the antenna impedance accurately across all operating conditions.

2.2 Hybrid Transformer

The section starts with a general discussion on transformer behaviour. Then two transformer structures are given that have been used to implement hybrid transformers. This is followed by stating how the ports of these transformers have to be terminated to obtain the four unique properties of the hybrid transformer. After this, these four unique properties are discussed in sequence. This starts by explaining bi-conjugacy between ports and how this allows all four ports to be matched simultaneously. Then the ability to split power in any desired ratio and a single inverted signal transfer are discussed.

2.2.1 Transformers

A transformer is a passive device with two or more conductive windings located in close proximity. Magnetic flux generated by an alternating (AC) current in one of the windings induces currents in the other windings. The flux couples the windings magnetically, allowing the induction of currents and generation of voltages from one winding to the other. Figure 2.2 shows the schematic symbols of an inverting and a non-inverting transformer, and illustrates the dot convention which defines the polarity of voltages from one side of a transformer to the other. By the dot convention, current entering the dotted terminal of the primary winding (P) will induce current flowing out of the dotted terminal of the secondary winding (S).

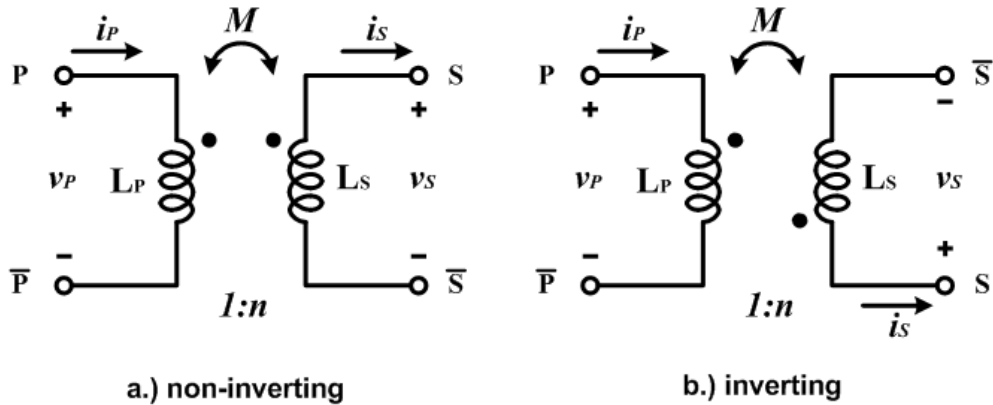


Figure 2.2 Transformers & the dot convention (a) non-inverting (b) inverting

The important electrical characteristics of a transformer are the turns ratio and the magnetic coupling coefficient k_m . The turn ratio relates the ratios of current and voltage

between the primary (P) and secondary (S) sides of the ideal transformer, and is given by:

$$n = \frac{v_S}{v_P} = \frac{i_P}{i_S} = \sqrt{\frac{L_S}{L_P}}, \quad (2.1)$$

where the voltages are given by v , the currents by i , and subscripts s , and p denote either the primary or secondary side of the transformer, as given in Figure 2.2. Furthermore, L_p and L_s are the self-inductances of primary and secondary windings, respectively.

The magnetic coupling coefficient k_m relates the ratio between the flux coupling two windings and the total magnetic flux generated by an AC excitation. The value of this coefficient lies between zero and one, and is given by the following equation:

$$k_m = \frac{M}{\sqrt{L_p L_s}}, \quad (2.2)$$

where, M is the mutual inductance between the primary and secondary windings. The mutual inductance relates the voltage change across a winding due to a corresponding change in the current through one of the windings.

Using the magnetic coupling coefficient, the effective turns ratio n_{eff} between two windings can be obtained by using:

$$n_{\text{eff}} = k_m \sqrt{\frac{L_s}{L_p}} = k_m n, \quad (2.3)$$

which takes flux leakage into account. This is relevant to monolithic circuits, as the physical layout and construction of transformers does not confine the magnetic flux tightly. Therefore, the magnetic coupling coefficient in conventional monolithic transformers is always less than one, which reduces the effective turns ratio.

2.2.2 The Autotransformer

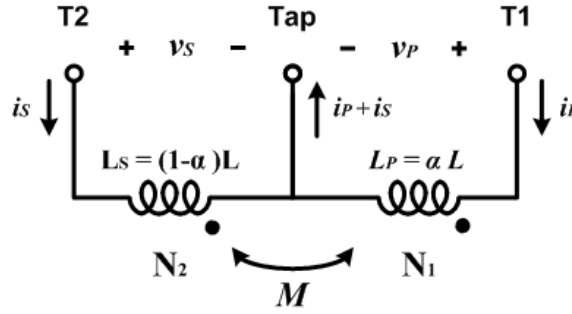


Figure 2.3 Schematic symbol autotransformer

Figure 2.3 shows the schematic symbol of an autotransformer. This device consists of a single winding with inductance L and a tap at some point along the length of the winding. The division between the primary and secondary is made at the location of the tap. Here, the symbol α is used to relate the location of a tap and is a number between one and zero. It equals one if the tap is located at terminal T2 and zero if the tap is located at terminal T1. Using α , the inductance of the primary L_p and secondary L_s of the autotransformer can be given as:

$$L_p = \alpha L \quad (2.4)$$

$$L_s = (1 - \alpha)L \quad (2.5)$$

The mutual-inductance between the two sections of the autotransformer winding is given by the voltage change across one of the winding due to a voltage change in the other. After the mutual inductance is obtained, the turns ratio and the coupling coefficient of the transformer can be found by substituting Eqs. (2.4) and (2.5) into Eqs. (2.2) and (2.3).

2.2.3 Hybrid Autotransformer & Hybrid Transformer

The schematic symbols of an autotransformer and a double tapped transformer are presented in Figure 2.4. Both of these transformers have been used as a hybrid transformer circuit to implement an electrical balance duplexer. The autotransformer given in Figure 2.4a is used in [20], and the double tapped transformer shown in Figure 2.4b is used in [12] [21] [22].

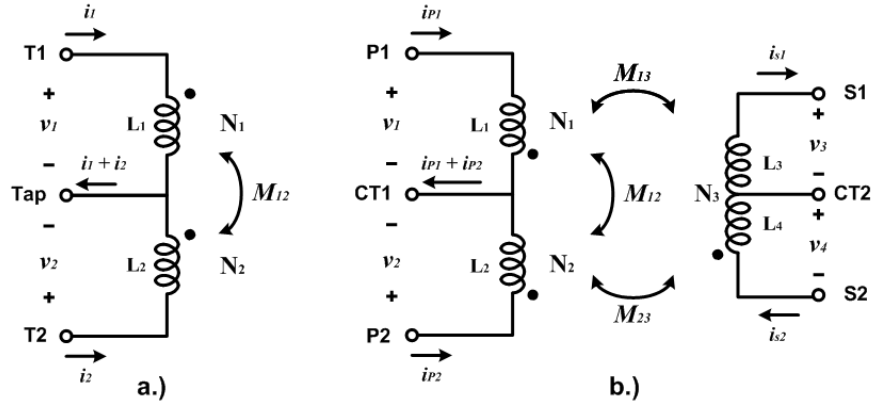


Figure 2.4 (a.) autotransformer (b.) double tapped transformer

The implementation of a hybrid transformer circuit using the autotransformer is shown in Figure 2.5a. Four impedances are connected to the transformer terminals. Three are connected from terminals T1, T2, and Tap to ground, and the fourth is connected differentially between terminals T1 and T2. The windings of the autotransformer will be referred to as N_1 and N_2 as depicted in Figure 2.5a. The mutual inductance between these windings is given by M_{12} .

The termination of the tapped transformer is given in Figure 2.5b. Three impedances are connected from the autotransformer terminals P1, P2, and CT1 to ground. The windings of the autotransformer are referred to as N_1 and N_2 and the mutual inductance between these windings is given by M_{12} . The fourth impedance is connected differentially across winding N_3 , the secondary centre tap CT2 is fixed to ground, and the mutual inductances between the opposing windings are given by M_{13} and M_{23} .

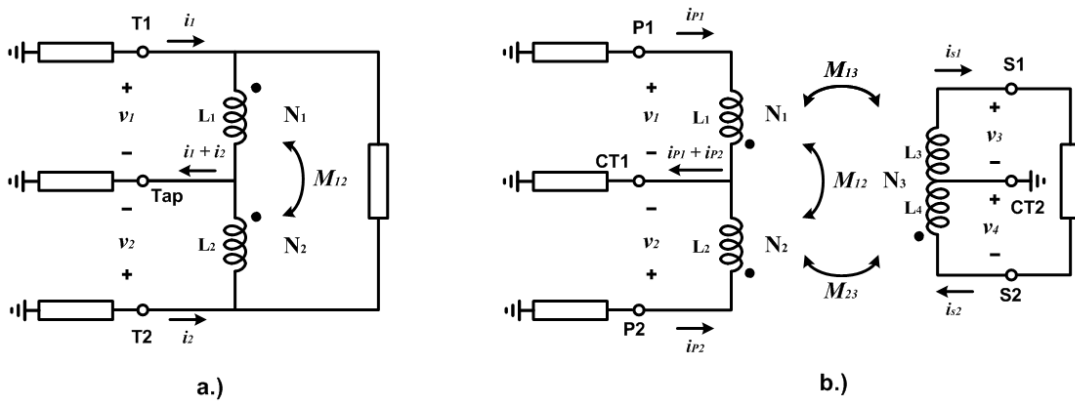


Figure 2.5 Transformer terminations

The properties of the hybrid transformer will first be explained using this topology and the explanation is then extended to the double tapped transformer. However before this explanation starts, the term bi-conjugacy is defined.

2.2.4 Bi-conjugacy

Contrary to the common use of conjugacy in circuit design or math, here the term bi-conjugacy does not refer to a complex conjugate of a complex number. In the context of hybrid transformers, two ports are bi-conjugate if their respective location in the circuit electrically isolates them from each other, and if they have an equal but opposite signal transfers to the other ports of the circuit. This behaviour is achieved by using balanced voltages or currents to place the two ports that form a bi-conjugate pair in an electric null with respect to any signal generated by the other. The next two sections will give examples of how this electrical isolation is obtained, and Section 2.2.7 explains the opposite signal transfer.

2.2.5 Wheatstone Bridge

The Wheatstone bridge is presented in Figure 2.6 and it can be used to explain the isolation property between bi-conjugate ports [23]. The Wheatstone bridge has six branches and three bi-conjugate impedance pairs. The three pairs are numbered 1 to 3, and are indicated with different shades of grey in Figure 2.6. When all six branches contain an equal amount of resistance, a voltage generated across one of the branches (say A), will produce an equal voltage change across the four adjacent branches (C, D, E, and F). The conjugate will then be the non-adjacent branch (B), which is in a null position with respect to the signal generated in branch A (and vice versa). As both are located in a null position with respect to a signal generated by the other, these impedances are electrically isolated. The same applies for the other two bi-conjugate pairs (C D and E F) in the circuit.

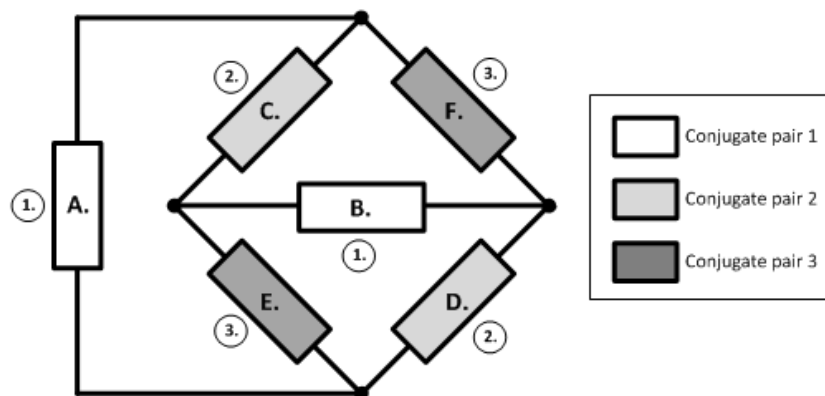


Figure 2.6 The three conjugate pairs of a Wheatstone bridge

2.2.6 Bi-conjugacy of the Hybrid Autotransformer

The hybrid transformer circuit has two bi-conjugate pairs. This bi-conjugacy behaviour is obtained through a balanced condition, which is achieved when the four ports of the transformer are connected to impedances with a specific proportional relation. For a centre-tapped hybrid transformer circuit, this relation is given by [4]:

$$Z_{Ant} = Z_{Bal} = 2Z_{Tx} = \frac{Z_{Rx}}{2}. \quad (2.6)$$

The antenna impedance Z_{Ant} is taken as the reference, as it is usually fixed to 50Ω . When this relation is satisfied, the hybrid transformer is electrically balanced and the bi-conjugacy between the ports (Tx&Rx and Ant&Bal) is obtained.

Figure 2.7 illustrates how the specific relation given by eq. (2.6) results in electrically isolated ports. In this figure, the bi-conjugate pairs are numbered as 1 (white) and 2 (grey). The ports of the first pair (depicted in white) are electrically isolated from each other through balanced voltages, just as in the Wheatstone bridge. The mechanism through which the ports of the second pair are isolated is, however, not through balanced voltages, but through balanced currents.

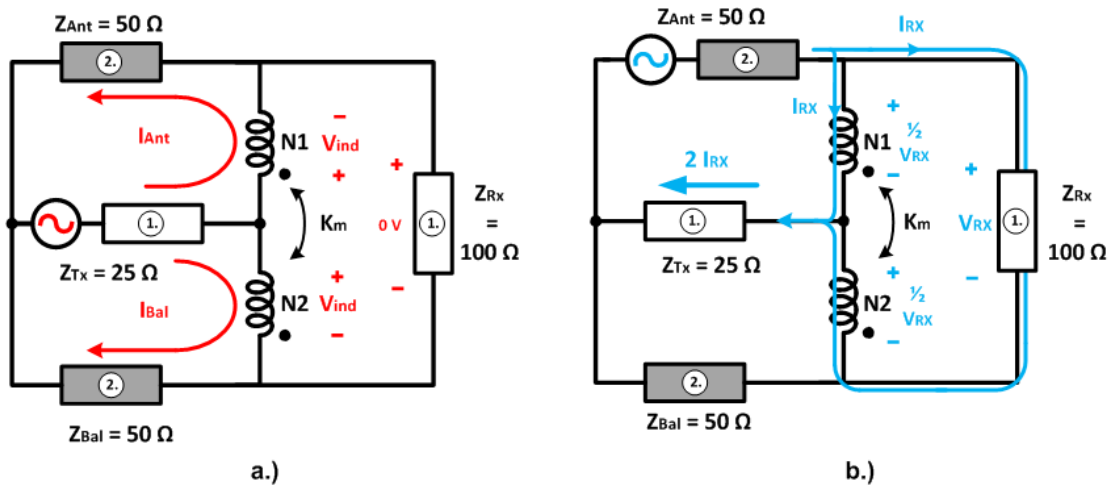


Figure 2.7 (a) Tx bi-conjugacy (b) Rx bi-conjugacy of hybrid autotransformer

The bi-conjugacy of the first pair (this example Tx and Rx) is achieved as shown in Figure 2.7a. In the hybrid autotransformer, two arms are formed by the windings of the autotransformer N_1, N_2 and the impedances Z_{Ant} and Z_{Bal} . For any signal generated across Z_{Tx} , the arms are formed by Z_{Ant}, N_1 and Z_{Bal} and N_2 , and for any signal generated across Z_{Rx} the arms are formed by N_1, N_2 and Z_{Ant}, Z_{Bal} . Provided there is a balanced condition, $N_1 = N_2$ and $Z_{Ant} = Z_{Bal}$, a zero potential appears across both Z_{Tx} and Z_{Rx} , effectively isolating these ports from each other.

The ports of the second bi-conjugate pair (Ant and Bal) are electrically isolated from each other through balanced currents as illustrated in Figure 2.7b. A signal generated at the Ant port produces an equal voltage across the autotransformer and Z_{Rx} , as they are connected in parallel. With a centre-tapped autotransformer, the voltage between N_1 and N_2 is exactly half the voltage across Z_{Rx} or the autotransformer. Then, provided ideal coupling ($k_m=1$) between windings N_1 and N_2 , any AC current flowing through the primary N_1 will generate magnetic field, which induces an anti-phase current in the secondary N_2 . If at the same time eq. (2.6) is satisfied so that Z_{Rx} (100Ω) is four times Z_{Tx} (25Ω) and the voltage at the centre-tap is exactly half of the voltage across the Z_{Rx} , the current entering Z_{Tx} ($2I_{Rx}$) equals the current delivered by the antenna. Therefore, both Kirchhoff's current law and voltage law (KCL and KVL) are satisfied. This leaves no current to flow through the Bal impedance, isolating this port from the Antenna.

However, to obtain isolation between Z_{Ant} and Z_{Bal} , the autotransformer has to provide an anti-phase copy of the current entering winding N_1 , in winding N_2 . This means that the autotransformer must provide sufficient magnetic flux to induce this copy. An inability to do so, results in a misdirected power flow to the balancing circuit, and thus reduces power delivered to the Rx port. This is illustrated in Figure 2.9, where the red line indicates the ideal -3dB Rx loss ($L=\infty$ & $k_m=1$) in a symmetric hybrid transformer. The other lines show the Rx losses with different values for L_1 and L_2 ($k_m=1$). It can be seen that insufficient self-inductance results in less power flowing to the Rx port.

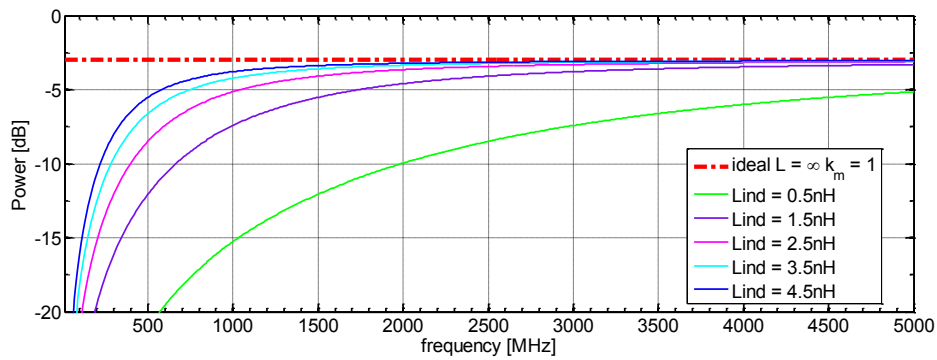


Figure 2.8 Rx power flow with different self-inductance values

Figure 2.9 show the effect of non-ideal coupling on the Rx losses with a given self-inductance. From the graphs it can be concluded that coupling helps Rx power flow but sufficient self-inductance is essential.

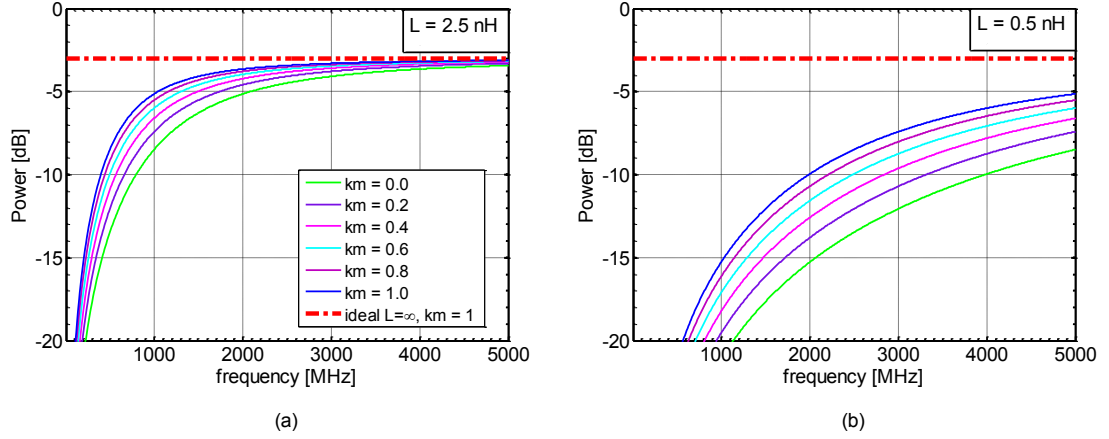


Figure 2.9 Rx power flow with different coupling coefficients
 (a) self-inductance of 2.5 nH (b) self-inductance of 0.5 nH

2.2.7 Power Splitting

This section explains how a hybrid transformer splits power in a desired ratio to the ports of the other bi-conjugate pair and how the ports of one bi-conjugate pair have an equal but opposite signal transfers to the other port of the other bi-conjugate pair. These signal transfers are given in Figure 2.10. As a redirection of the power to reduce either the Tx or Rx insertion losses results in a new termination ratio at the transformer port, this section introduces the variable power ratio β to describe this new proportionality.

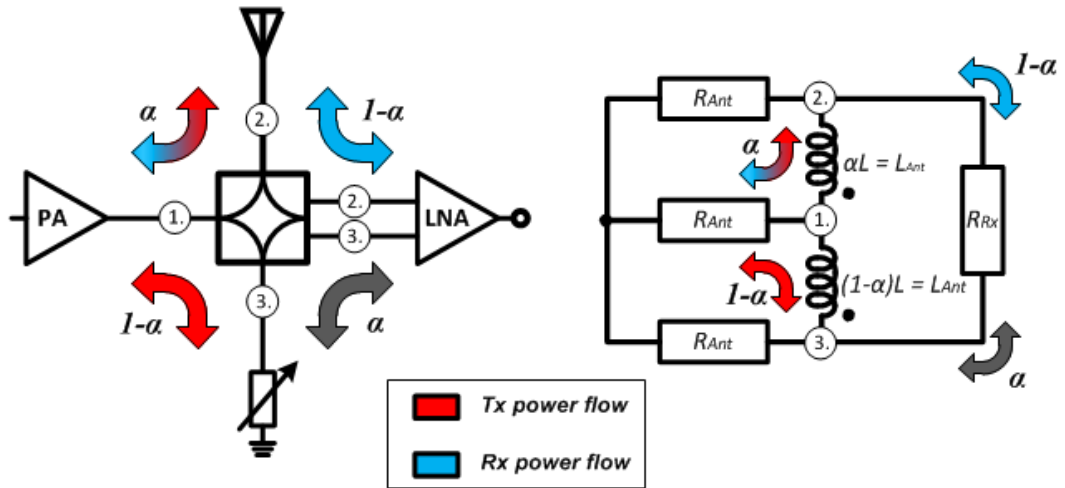


Figure 2.10 Hybrid transformer power splitting

As explained in the previous section, when a hybrid transformer is balanced the conjugate ports are isolated from each other. Therefore any power inserted into, say the Tx port, will flow to the antenna, and balancing circuit. If a centre tapped autotransformer is used, the power to the Ant and Bal ports splits equally. This results in

an inherent 3dB power loss when using a hybrid transformer as a duplexer. If this is unacceptable for a given application, the ratio between the power flowing to the Ant port and the Bal port can be altered by changing the location of the autotransformer tap (location = α , Section 2.2.2).

By skewing the tap of the autotransformer in favour of either the antenna or the balancing circuit, the injected power can be divided in any desired ratio, as is depicted in Figure 2.10. However to remain balanced in this skewed condition, the termination impedances at the ports should also be adapted. Assuming ideal coupling ($k_m = 1$), the relation between power ratio β , the tap location α , the inductance of the autotransformer is given below [12]:

$$\beta = \frac{P_{Ant}}{P_{Bal}} = \frac{Z_{Ant}}{Z_{Bal}} = \sqrt{\frac{L_{Ant}}{L_{Bal}}} = \sqrt{\frac{\alpha}{(1-\alpha)}} \quad (2.7)$$

Here P_{Ant} is the power flowing to the Ant port, P_{bal} is the power flowing to the Bal port. Z_{Ant} and Z_{Bal} are the impedance values connected to the Ant and Bal ports of the transformer. To obtain a balance in a skewed condition eq. (2.6) changes to [4]:

$$Z_{Ant} = \frac{Z_{Bal}}{\beta} = \left(\frac{1+\beta}{\beta}\right) Z_{Tx} = \left(\frac{1}{1+\beta}\right) Z_{Rx} \quad (2.8)$$

As the transformer is a passive structure it is also reciprocal. This means that the trade-off for skewing comes in the form of increased insertion losses for the other transfer. Therefore reducing the Tx insertion losses (IL_{Tx}) increases the Rx insertion losses (IL_{Rx}) proportionally. These losses are given by [22]:

$$IL_{Tx} = 10 \log_{10} \left(\frac{P_{Ant,out}}{P_{Tx,in}} \right) = 10 \log_{10} \left(\frac{1+\beta}{\beta} \right) + Loss \quad (2.9)$$

$$IL_{Rx} = 10 \log_{10} \left(\frac{P_{Rx,out}}{P_{Ant,in}} \right) = 10 \log_{10} (1+\beta) + Loss \quad (2.10)$$

In eq. (2.9) and (2.10), P stands for power, and the subscripts denote, whether power is flowing in or out of a port. The factor *Loss* denotes any additional losses incurred in a practical circuit. The trade-off between the two insertion losses from eq. (2.9) and (2.10) is illustrated in Figure 2.11. This reciprocity also causes opposite but equal signal transfer as can be seen in Figure 2.10, that is a characteristic of the bi-conjugate pairs of a hybrid transformer (Tx Rx and Ant Bal).

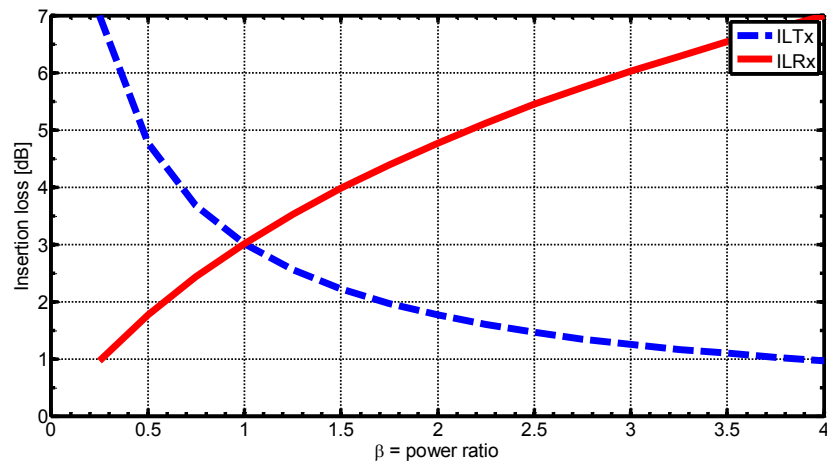


Figure 2.11 Tx Rx Insertion-loss trade-off electrical balance duplexer [22]

2.2.8 180° Phase inversion

One of the four transmission ratios from one conjugate pair to the other has a 180° phase shift [4]. The phase of the transfers between the conjugate pair is illustrated in Figure 2.12. This property is however not utilized and is added for completeness.

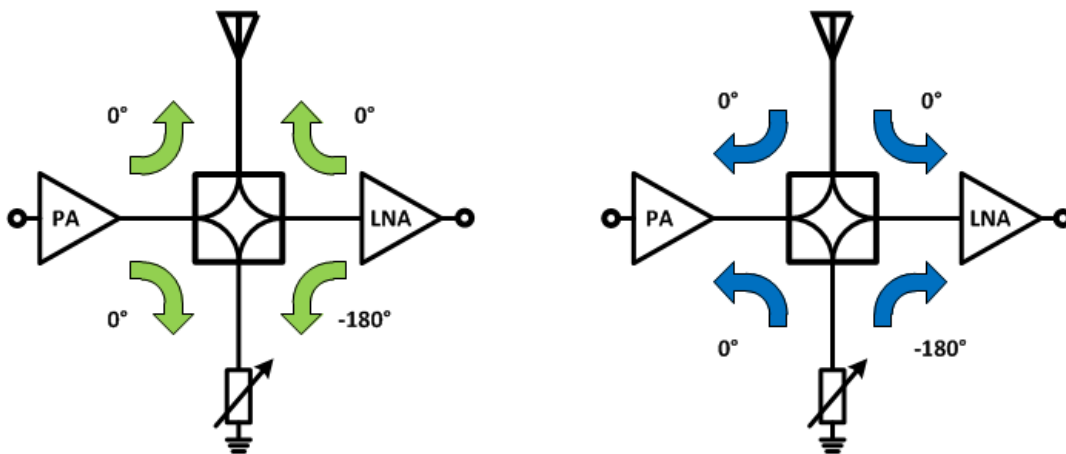


Figure 2.12 Single 180° phase shift in signal transfer

2.2.9 Noise Matched LNA

Another feature of the integrated duplexer is that both the duplexer and the LNA are implemented on chip. Therefore at 2.45GHz, the connection between these two circuits will be shorter than $1/10^{\text{th}}$ of the wavelength of operation (2.45GHz). This means that no impedance match is required to maximize power transfer. Therefore the noise of the duplexer and LNA combination can be optimized through noise matching. If this is done, the NF of the combined duplexer and LNA can be predicted with the following equation [22]:

$$F_{diff} \cong 1 + \beta + \frac{R_{Ant}}{\left(\omega L_1 Q_1 \parallel \frac{\omega L_2 Q_2}{n_{eff}^2}\right)} (1 + \beta)^2 + \frac{4\gamma}{g_m R_{ant}} \left(\frac{1}{n_{eff}^2}\right) \left[1 + R_{Ant}(1 + \beta) \left(\frac{\omega L_1 L_2 Q_1 Q_2}{n_{eff}^2 L_1 Q_1 + L_2 Q_2}\right)\right]^2 \quad (2.11)$$

This equation is rewritten from its original form and follows from a single-ended analysis. It assumes a balanced condition ($R_{Ant} = R_{Bal}$) so that the presence of Z_{Tx} , can be ignored. The variables L_1 and L_2 are the self-inductance of the primary and secondary windings, respectively. Q_1 and Q_2 are the respective Q-factors of the windings, β and n_{eff} are the power ratio and the effective turn ratio as given in previous section of this chapter. The first two terms originate from the inherent losses of an ideal duplexer, the second term comes from additional losses in a particle transformer and the last term shows that the noise contribution can be lower by increasing n_{eff} of the transformer.

2.2.10 Hybrid Transformer

The hybrid transformer differs from the hybrid autotransformer because the Rx branch is no longer connected directly to the terminals of the autotransformer. It is now connected to a third winding (N_3) of a double-tapped transformer as is illustrated in Figure 2.13. Therefore, the Rx branch is now magnetically coupled to the autotransformer by a third winding with inductance value L_3 , as depicted in Figure 2.13. Due to the impedance transformation and assuming $k_m=1$, eq. (2.6) now changes to [4]:

$$Z_{Ant} = Z_{Bal} = 2Z_{Tx} = 2 \left(\frac{N_1 + N_2}{N_3} \right)^2 Z_{Rx} . \quad (2.12)$$

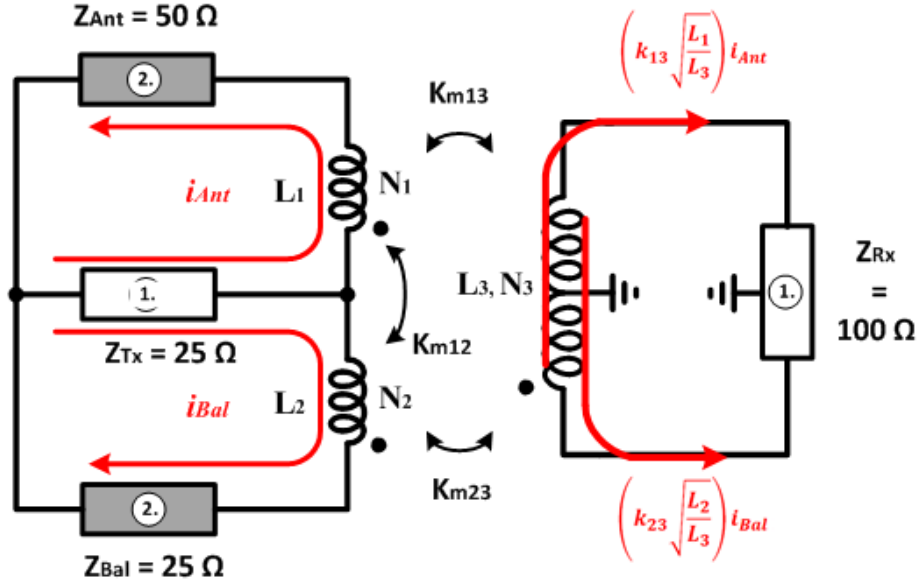


Figure 2.13 Hybrid Transformer

The benefit of this topology is increased Tx-CM-isolation, as the CM-signal generated across the Z_{Rx} branch will be partly cancelled by the opposing magnetic fields generated by windings N_1 and N_2 . Given a symmetric structure, the AC currents in N_1 and N_2 will induce equal but opposite currents in the opposing winding N_3 , which effectively cancel out each other. Only an imbalance in the induced currents in winding N_3 will now generate a common-mode voltage at the terminals of the Rx branch. Drawback of this configuration is the increased Rx insertion losses due to flux leakage between N_1 , N_2 and N_3 , and due to additional ohmic losses in the secondary winding N_3 .

Also this topology can be skewed. The power ratio between the Ant and Bal ports is again given by eq. (2.7). However impedances are transformed as a function of the turns ratio of the transformer, therefore, the proportional relation between the impedance connected to the port changes to [4]:

$$Z_{Ant} = \frac{Z_{Bal}}{\beta} = \left(\frac{1 + \beta}{\beta} \right) Z_{Tx} = \left(\frac{1}{1 + \beta} \right) \left(\frac{N_1 + N_2}{N_3} \right)^2 Z_{Rx} . \quad (2.13)$$

The electrical balance duplexer with all previous impedances now changed to the circuits that will eventually be connected to them is given in Figure 2.14. This figure

also illustrates the currents and voltages in the circuit during Tx and Rx operation. It should be noted that in an FD transceiver both modes operate concurrently. It can be observed that during Tx operation, the Tx signal appears in common-mode at the input of the LNA, which is connected differentially to the winding opposing the autotransformer. In Rx operation, the Rx signal appears differentially at the input of the LNA. Therefore, the differential Rx port is blind to any signal generated at the Tx port by a PA, and is only able to sense signals originating at the antenna port.

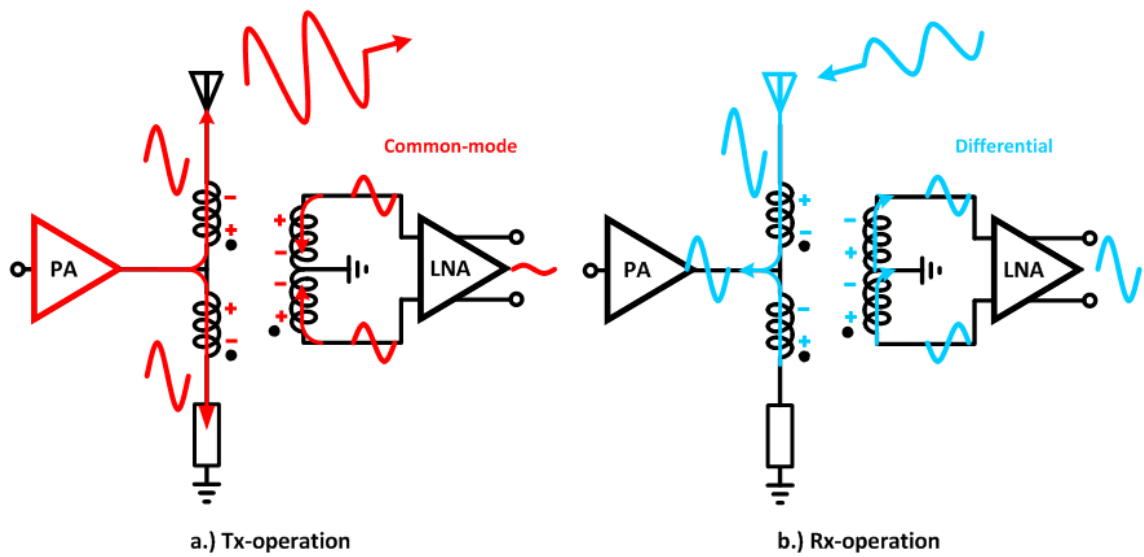


Figure 2.14 Hybrid transformer operation Tx & Rx modes

2.3 Balancing Circuit

For isolation, the balancing circuit needs to mimic the impedance at the ANT port of the transformer in the desired frequency range. This requires four characteristics. Firstly, centre impedance, equal to the nominal impedance of the antenna and intermediate interconnect as seen at the ANT port. Secondly, it requires sufficient tuning range to track perturbations of the antenna impedance. Thirdly, the resolution needs to be high to provide an accurate approximation of the antenna impedance. Lastly, the frequency behaviour of the balancing impedance should resemble the impedance at the ANT port over a wide frequency range to provide adequate isolation bandwidth.

Two balancing circuits used in integrated electrical balance duplexer have been reported in detail [24] [22]. The first is presented in Figure 2.15. A digitally-controlled 10-bit binary resistor bank provides an impedance range from 60 to 100 Ω in 0.3 Ω

steps, and two 5-bit binary capacitor banks on either side of the transformer each provide a capacitance value between 0 to 200 fF [24].

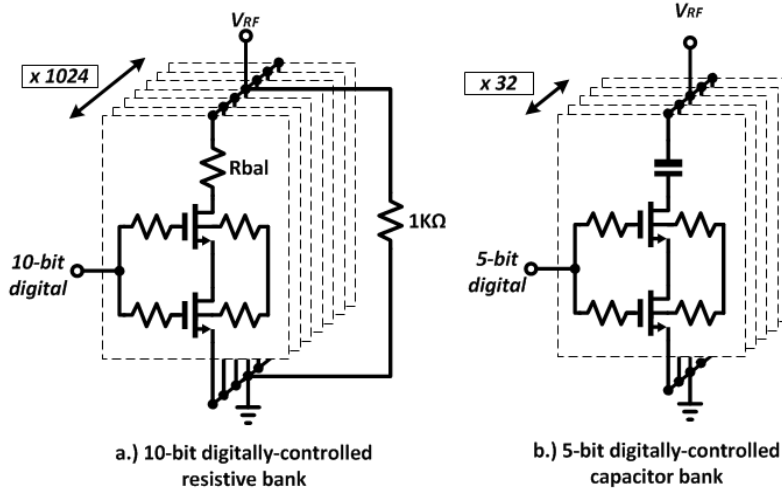


Figure 2.15 Example of a digitally-controlled balancing circuit [24]

All the switches are implemented using stacked FETs, in a floating well structure [25]. This prevents device breakdown resulting from exposure to the high Tx powers used in FDD application (max 33 dBm). The stack needs to be taller to divide down the voltage across each device in order to prevent distortion due to non-linear switch resistance. This duplexer uses a skewed transformer to reduce Tx losses. Due to the skewing, the balanced condition is no longer realized with $50\ \Omega$, but with $80\ \Omega$ at BAL port. Therefore the nominal resistance of the tunable circuit is $80\ \Omega$. The reason for locating a capacitor bank on both sides of the transformer is to be able to balance impedances located in both the upper and lower half of the smith chart. The drawback of placing a capacitor bank with finite Q-factor in the Tx path is additional losses.

The second balancing circuit is presented in Figure 2.16. It consists of a tuneable resistance with a nominal value of $50\ \Omega$. No skewing is applied, so a tuning range from 40 to $60\ \Omega$ is sufficient. The capacitance ranges from 150 to 200 fF. The resolution of both is limited by noise and electromagnetic interference (EMI) on the control lines. To allow high power operation, the tuneable part of the resistance is implemented using four stacked parallel resistor FET pairs in series with a $40\ \Omega$ resistance as shown in Figure 2.16a. This divides down the voltage swing seen across each pair. RF floating gates were realized by resistors placement at the gates in order to divide down voltage swing on the gates between the C_{gd} and C_{gs} of each individual device. Similarly, the voltage swing across the varactor given in Figure 2.16b, used in the tuneable capacitance

is reduced by placing a MIM capacitor in series with the varactor. These high voltage precautions reduce the achievable impedance range of the balancing circuit, and increase the die area. The resistor connected between the MIM capacitor and the varactor is used to set the voltage between both devices at 0 V.

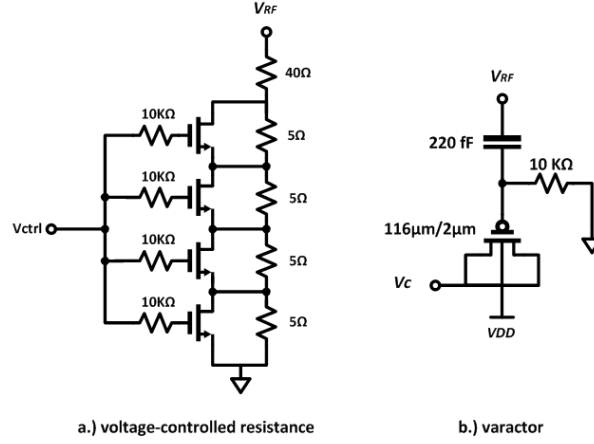


Figure 2.16 Example of analog-controlled balancing circuit [22]

2.3.1 Balancing region

The balancing region conveys the impedance range the balancing circuit is able to cover at a given frequency. Figure 2.17, shows the balancing regions for the balancing circuits described in the previous section. These areas are illustrated on the Smith chart, as this chart conveys the complete impedance plane in a bounded figure. The red dot indicates the expected nominal impedance of the antenna. The yellow area outlined by a blue line is the reported balanceable area, and the green line show the additional range implemented as derived from the actual circuit implementation given in [24].

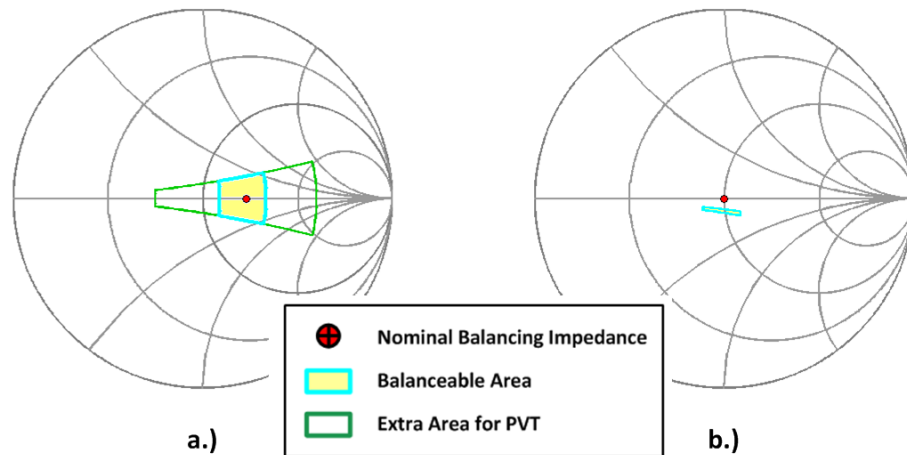


Figure 2.17 Balancing region (a.) circuit in [21] (b.) circuit in [22]

2.3.2 Isolation

The level of isolation provided by an electrical balance filter can be predicted using the circuit given in Figure 2.18. Assuming ideal components and perfect symmetry, the following equation accurately relates the level of isolation,

$$ISO_{TX} = -20 \log_{10} \left(|Z_{Ant} - Z_{Bal}| \left| \frac{Z_{ind,p}}{(Z_{Ant} + Z_{ind,p})(Z_{Bal} + Z_{ind,p})} \right| \times V_x \right) \quad (2.14)$$

Here Z_{Ant} and Z_{Bal} are the antenna and balancing impedances, respectively. The parameters $Z_{ind,p}$ and $Z_{ind,s}$ are the self-inductances of the autotransformer windings, and V_x is the voltage swing at the autotransformer centre tap.

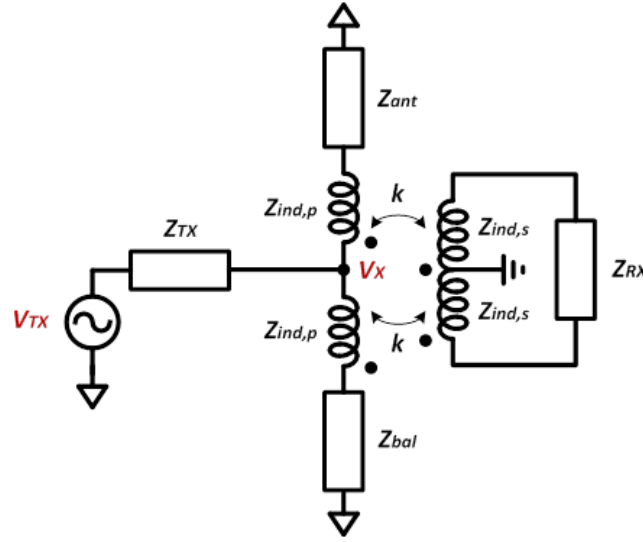


Figure 2.18 Isolation electrical balance filter

The first term of eq. (2.14), $|Z_{ant} - Z_{bal}|$ is the most interesting, as it shows that isolation is provided by minimizing the absolute value of the difference distance between Z_{ant} and Z_{bal} in the complex plane. It is also interesting to note that this term expresses a circle around the value of the antenna impedance in the complex impedance plane, with radius equal to the absolute value of the difference between the balancing impedance and the antenna impedance. From this, a number of properties can be concluded. Firstly, all impedance points with a certain difference with respect to the antenna impedance will provide approximately equal isolation. Secondly, every time the value of the absolute difference between Z_{Ant} and Z_{Bal} is halved, this should result in a 6dB improvement of the isolation.

This equation was compared to Cadence simulations with ideal components. The impedance circles given in Figure 2.19 have constant radius around 50Ω . These were used in both the circuit and Matlab simulations, and the resulting isolation between the TX and RX ports is given in Figure 2.20 and Figure 2.21. The first figure shows a global minimum with isolation pattern around it. In the second figure these perimeters have been averaged, and it can be observed that the two curves agree with each other and confirm the 6 dB slope.

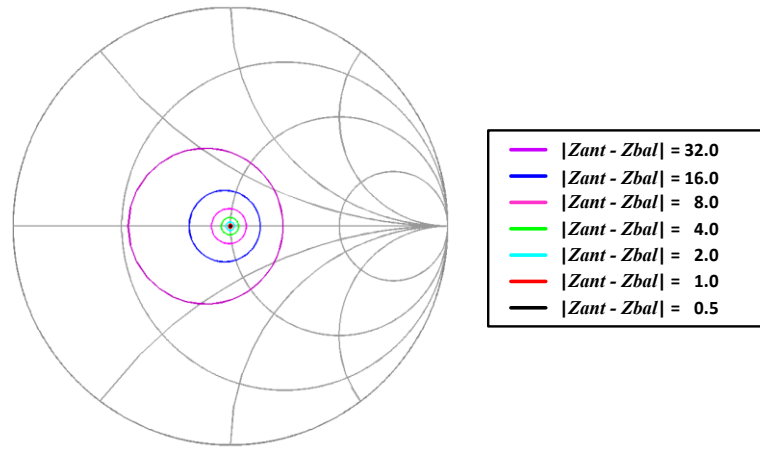


Figure 2.19 Impedance circles around $Z_{Ant} = 50 \Omega$ at 2.45GHz

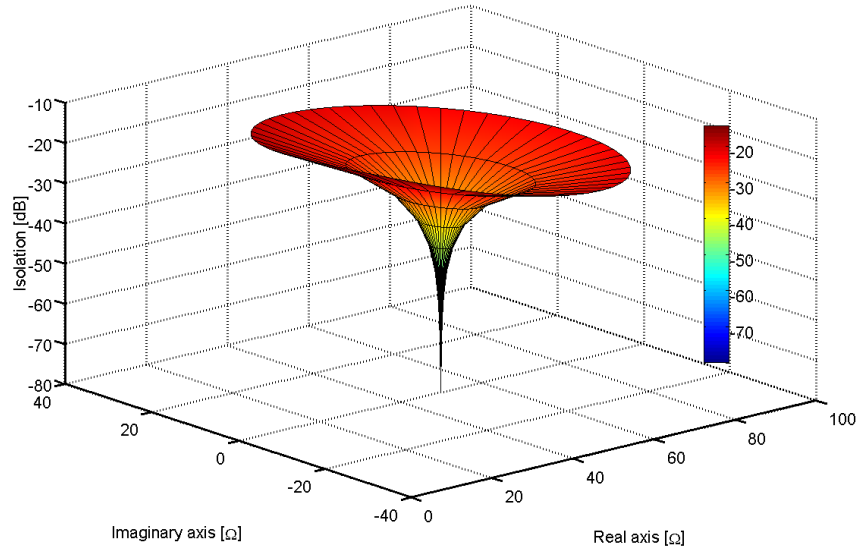


Figure 2.20 Isolation pattern around $Z_{Ant} = 50 \Omega$ at 2.45GHz

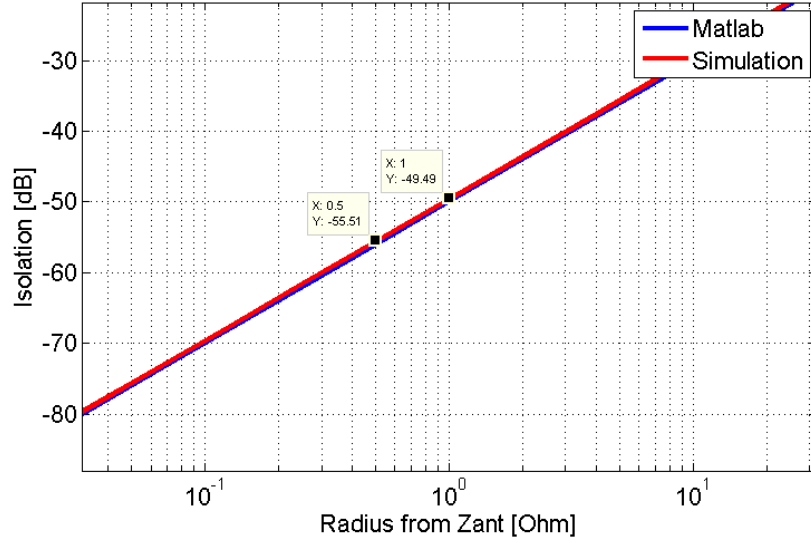


Figure 2.21 Simulated and calculated Tx- isolation (Z_{ant}) 2.45GHz

2.3.3 Balancing Resolution

A higher resolution in the balancing circuit allows a more accurate replica of the impedance presented at the Ant port. As impedances are located in the complex impedance plane, the balancing circuit requires resolution in the imaginary as well as the real part of the impedance. The resolution of the digitally-controlled balancing circuit shown in Figure 2.15 was 0.3Ω in the resistor bank and 6 fF in the capacitor bank. The resolution provided by these values in the complex impedance plane can be calculated using:

$$Re\{Z_{bal}\} = \frac{R}{1 + (\omega RC)^2} , \quad (2.15)$$

$$Im\{Z_{bal}\} = \frac{\omega R^2 C}{1 + (\omega RC)^2} , \quad (2.16)$$

where R is the resistive step, and C is the capacitive step. Using eqs. (2.15) and (2.16) balancing circuit resolution is 0.3Ω real and a 0.15Ω imaginary. The resulting impedances of this balancing circuit around the 80 Ohm goal (pink dot) are presented in by the blue dots. The green dot gives the impedance farthest from any of the tuning setting and therefore location within the balancing range that would give the lowest isolation. If the resolution of both the imaginary and real part is increased with 1-bit, the tuning settings provide a finer grid illustrated with the red dots. The greatest difference

from settings is now given by the black dot and the worst-case distance is reduced by half, which according to eq.(2.14) increases isolation with 6dB.

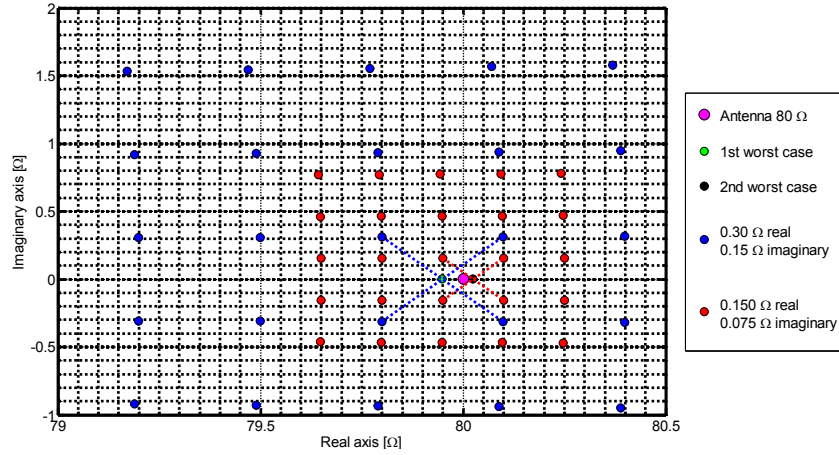


Figure 2.22 Balancing resolution

2.3.4 Isolation Bandwidth

The isolation bandwidth is defined as the bandwidth over which a specified level of isolation is given [21]. An example of an isolation curve across frequency is illustrated in Figure 2.23. This simulated curve shows a bandwidth of 10 MHz for -50 dB of isolation. The bandwidth is primarily dependent on absolute difference between the impedance presented at the Ant port and the balancing impedance across frequency. The relationship between the two is given by:

$$ISO_{Tx}(\omega) \propto -20 \log_{10} |Z_{ant}(\omega) - Z_{bal}(\omega)|. \quad (2.17)$$

Here $ISO_{Tx}(\omega)$ is the isolation across frequency, $Z_{ant}(\omega)$ is the antenna impedance across frequency, and $Z_{bal}(\omega)$ the impedance provided by the balancing circuit across frequency

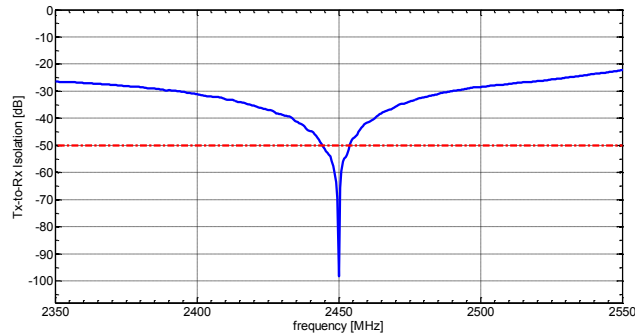


Figure 2.23 Isolation bandwidth for -50dB of isolation

2.4 Electrical Balance Duplexer Implementations

Recent years have seen four implementations of electrical balance duplexers. One is discrete and three are integrated. The discrete duplexer is illustrated in Figure 2.24, and it was implemented with a hybrid transformer having a turns ratio of three ($n = 3$). A tunable varactor diode at the antenna port was combined with a PIN diode at the Bal port to obtain the balanced condition [12]. The measured peak isolation at 863 MHz was -50 dB, and 5 MHz of isolation bandwidth was reported for -30 dB of isolation, while incurring -2 dB Tx and -10 dB Rx insertion losses.

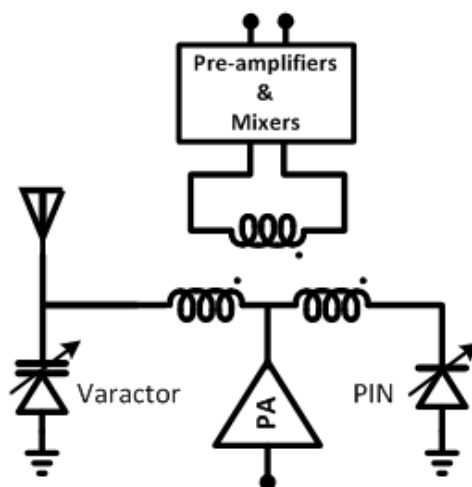


Figure 2.24 The discrete electrical balance duplexer

The three integrated electrical balance duplexers are presented in Figure 2.25. Each of these will be discussed in order from left to right. The first integrated electrical balance filter was presented in an Rx skewed and a non-skewed version. Both were integrated with an LNA. As presented in Figure 2.25a, the configuration of these circuits differ from the analysis presented in the previous section on the hybrid transformer, as the LNA and PA conjugate pair is swapped with the Antenna and balancing conjugate pair. This configuration reduces Tx and Rx insertion losses through the transformer, which allows the realization of a transformer with higher coupling, more self-inductance. This realised -4.2dB Tx and -4.2 Rx insertion losses in the non-skewed circuit. It further obtained a peak isolation of -70 dB at 1.95 GHz, with a 5 MHz isolation bandwidth at -50 dB. The Rx skewed version obtained -5.9 dB Tx and -2.9 dB Rx insertion loss, while the other performance metrics remained similar. The non-skewed circuit realised a gain of 23 dB, and a NF of 6.3 dB at the output of the LNA. The skewed version showed a gain of 24 dB, and a NF of 7.4 dB.

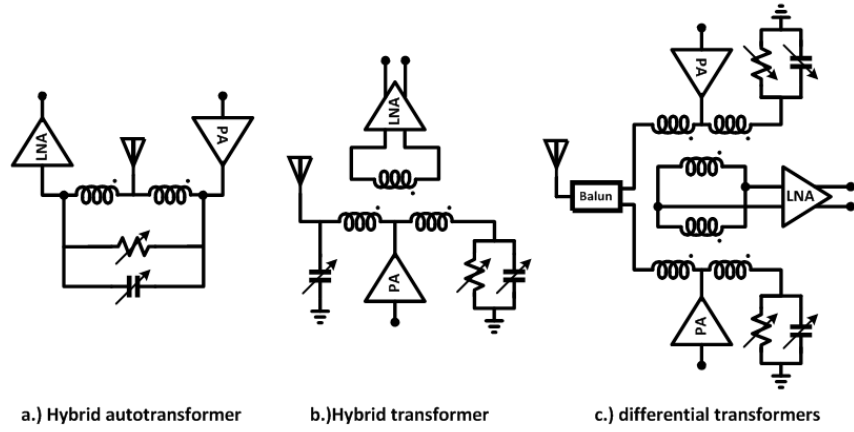


Figure 2.25 Integrated electrical balance filters

The previous duplexer provided narrowband isolation and suffered from high insertion losses. The duplexer presented in Figure 2.25b, addressed these problems by using a new architecture, and co-integration with a noise matched LNA [21]. This configuration has no voltage difference across the autotransformer therefore no self-inductance current will flow through the autotransformer, preventing the generation of voltage across the balancing network. Furthermore, phase shift caused by the self-inductance that limits the isolation bandwidth a phase shift was also remedied. In order to reduce the Tx insertion loss to -2.5 dB, the tap of the autotransformer tap was skewed to favour the Tx port. However, this necessitates noise matching the LNA and maximizing the voltage gain through the transformer and resulted in a combined NF of 5dB and a 27 dB gain. The isolation performance of this circuit was a peak isolation of -65 dB at 1.7 GHz, and 250 MHz isolation bandwidth over -55 dB isolation with an ideal 50 Ω . Figure 2.25c presents the last implementation. It consists of a differential electrical-balance duplexer integrated along with a differential LNA [22]. The differential topology realized a common-mode isolation of -60 dB and relaxes the voltage strain across the balancing circuit by a factor two, at the cost of requiring a second balun and hybrid transformer. The LNA is noise matched to the filter and the combination realized a 17 dB gain, and 5.9 dB NF. This work further reports a Tx insertion loss of 3.9 dB. The peak isolation is -70 dB at 1.95 GHz, with an isolation bandwidth of 190 MHz, at -40 dB isolation were obtained using an off-chip a 50 Ω at the Ant port. The performance of the previously-discussed duplexer is summarized in table 2.1, together with some other metrics e.g. technology, area, and power consumption.

The main difference between this work and previous integrated duplexers is that this one is intended for FD instead of WCDMA. As FD is still under development no standard is available with specified design requirement. In the absence of a standard, a FD environment is proposed, that could be achievable given the current state of SIC development. This environment assumes a -10 dBm output power in order to relax receiver SIC requirements. Secondly, it assumes 10 MHz bandwidth and a receiver NF of 9.5 dB. This results in a noise floor at -95 dBm ($10\log10[k_i t] + NF$). To compete with HD systems, higher modulation schemes should be supported. These require around 30 dB of SNR making the minimum received signal strength -65 dBm (SNR for WLAN 64-QAM 54 Mbps is 27 dB [27]). This allows 55 dB of free space path loss, assuming 2 dBi antenna gain for PIFA antenna's [28], this allows a 10 m transmit range (). These considerations, combined with achieved performance in previous literature lead to the design goals presented in the last column of Table II Performance of integrated duplexers reported in recent literature.

Table II Performance of integrated duplexers reported in recent literature

Parameter	Discrete Hybrid Trans. [12]	Asym. Autotrans. [20]	Sym. Autotrans [20]	Hybrid Transformer [21]	Diff. Hybrid Transformer [22]	Design Goals
Tx power	20 dBm	24 dBm	24 dBm	24 dBm	33 dBm	-10 dBm
Op. freq.	863 MHz	1.9 GHz	1.95 GHz	1.9 GHz	1.95 GHz	2.45 GHz
-1 dB CP	-	-	-	-	-	-5 dBm
IIP3	-	-	-	-	-	0 dBm
RX IL	10 dB	2.9 dB	4.2 dB	-	-	4.0 dB
TX IL	2 dB	5.9 dB	4.2 dB	2.5 dB	4.7 dB	3.5 dB
Iso. Diff.	>30 dB	> 50.0 dB	> 50.0 dB	> 55.0 dB	>70 dB	40-70 dB
Iso. CM.	-	-	-	-	60 dB	30 dB
Iso. BW	5 MHz	5 MHz*	5 MHz*	250 MHz*	190 MHz*	10 MHz
Cas. NF	-	6.1 dB	7.4 dB	5 dB	5.9 dB	6.5 dB
Gain	-	23 dB	24 dB	27 dB	17dB	6.0dB
Aggr. BW.	15 MHz	1.5 to 2.4 GHz	1.5 to 2.5 GHz	1.8 to 1.8 GHz	0.5 GHz	150 MHz
Current	-	7 mA	6 mA	10 mA	-	-
Technology	discrete	40 nm	40 nm	65 nm	90 nm	180 nm
Supply Voltage	-	1.2 V	1.2 V	1.2 V	-	1.8V
Area	PCB	0.2 mm ²	0.2 mm ²	0.2 mm ²	0.6 mm ²	0.2 mm ²

*reference impedance during e valuation was 50Ω

Chapter 3

Duplexer Design

To evaluate the isolation performance of an electrical balance duplexer operating with a commercial antenna, a prototype duplexer was designed and fabricated in 180nm RFCMOS [29]. The prototype consists of a transformer, a balancing circuit, and a low noise amplifier (LNA). This LNA was added by IMEC. A simplified diagram of the different circuit blocks on the prototype die is illustrated in Figure 3.1.

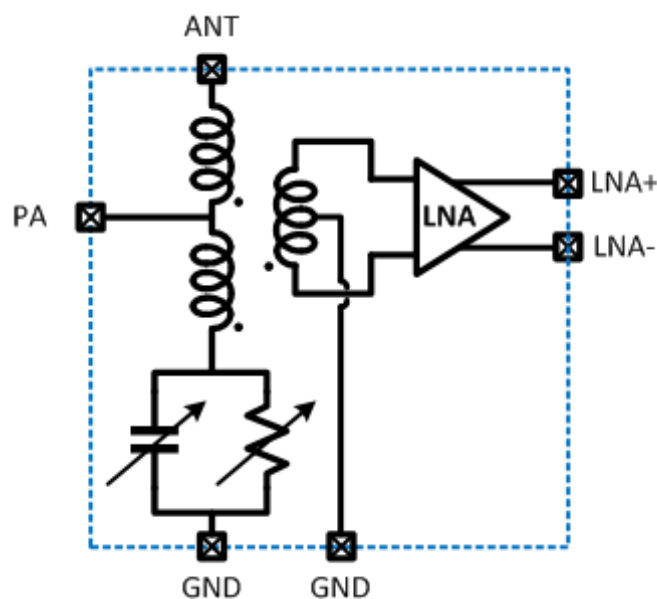


Figure 3.1 Simplified schematic of the integrated prototype

This chapter presents the design of the electrical balance duplexer. It starts with the chosen circuit topology and continues with the design of the transformer and balancing circuit. After this, the performance metrics of the IMEC LNA are noted.

The transformer described in this work was not exclusively designed for the FD project. The design was also reused in a parallel FDD project which aimed to provide a highly linearity duplexer for WCDMA application (Tx output power 33dBm). This dual role impacted some of the trade-offs made in its implementation.

3.1 Duplexer Topology

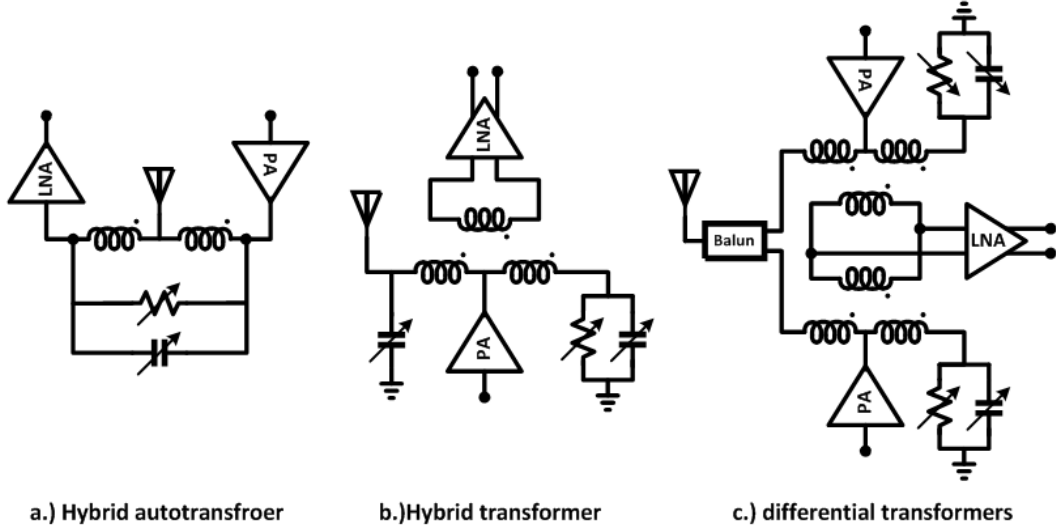


Figure 3.2 Integrated electrical balance filters [18] [22] [23]

Figure 3.2 presents three different electrical balance duplexers: 1) an autotransformer, 2) a single transformer, and 3) one using two transformers. The trade-off between these three configurations is insertion losses versus common-mode (CM) Tx isolation and die area. The implementation shown in Figure 3.2a requires the least amount of area and theoretically has the lowest Rx insertion losses. The drawback of this configuration is the absence of any CM Tx isolation before the LNA. The hybrid transformer illustrated in Figure 3.2b provides CM Tx-isolation as the Rx is no longer directly connected to the Bal and Ant ports, but is magnetically coupled through an extra winding. This winding requires area and increases Rx insertion loss due to flux leakage and additional ohmic losses in the metal. The double transformer of Figure 3.2c provides high CM Tx-isolation, however both the Tx and Rx suffer from increased insertion losses as it requires an additional balun and this topology requires the largest as two transformers are required.

The topology choice depends upon two aspects, which conjugate pair provides Tx-to-Rx isolation, and which circuit configuration to choose. The voltage balanced pair provides the best Tx-to-Rx isolation. Placing the Tx and Rx at the location of the current-balanced conjugate pair (i.e., terminals of autotransformer) results in a voltage drop across the autotransformer. This induces an inductive current which creates a voltage across the balancing circuit and causes a phase shift that limits the bandwidth of the duplexer [22]. To minimize this effect, the port generating the biggest signal (PA)

should be placed at the tap of the autotransformer, as this avoids a large voltage swing across the autotransformer.

Due to the -10 dBm output power of the proposed FD environment no CM Tx isolation is required to isolate the LNA from a large input swing at its input ($0.2 V_{pp}$ with 50Ω). This suggests that a hybrid autotransformer can be used which has the lowest insertion losses of the three topologies. Also transmitter efficiency is less important at low output powers, as overall power consumption is not dominated transmitter efficiency. This suggests non-skewed is required to avoid disproportional power losses. So a non-skewed hybrid autotransformer seems the topology of choice.

However, as the transformer design is to be reused in a parallel project involving a high output power WCDMA application (33 dBm) and because there was insufficient time to design multiple transformers, only a single transformer was designed for both applications. As the parallel project required CM Tx isolation to isolate the LNA from the 15 V across both the antenna and the balancing circuit, hybrid transformer topology illustrated in Figure 3.2b was chosen for both projects [25].

3.2 Electrical Balance Duplexer

The performance characteristics of an electrical balance duplexer can be divided into two categories: characteristics that depend on the balancing circuit, and the characteristics that depend on the transformer. The balancing circuit determines the isolation properties and the linearity. The linearity is limited by the non-linearity of the FETs used to implement tunability (primarily of the drain source resistance). The transformer determines the insertion losses and the CM Tx isolation. Tx losses reduce transmitter efficiency, Rx losses degrade receiver sensitivity and the CM Tx isolation is depends on symmetry of the circuit.

3.3 Technology

The UMC180nm CMOS MM-RF 1P-6M 1.8V/3.3V technology was used for the prototype implementation [31]. The substrate resistivity of this technology ranges from 15 to 25 Ω -cm. The components used in the design are MIM capacitors, resistors and MOSFETs. Both radio frequency (RF) and mixed-mode (MM) device models are available for design. The RF models in the library include parasitic inductances, and the effect of shielding, diffusion rings, etc., in the physical layout. The transformer was

custom designed for this application. A simplified cross section of the metal stack (not to scale) provided in this technology is presented in Figure 3.3. It consist of six interconnect metals including a thick top metal, and a capacitor layer to implement metal-insulator-metal (MIM) capacitors.

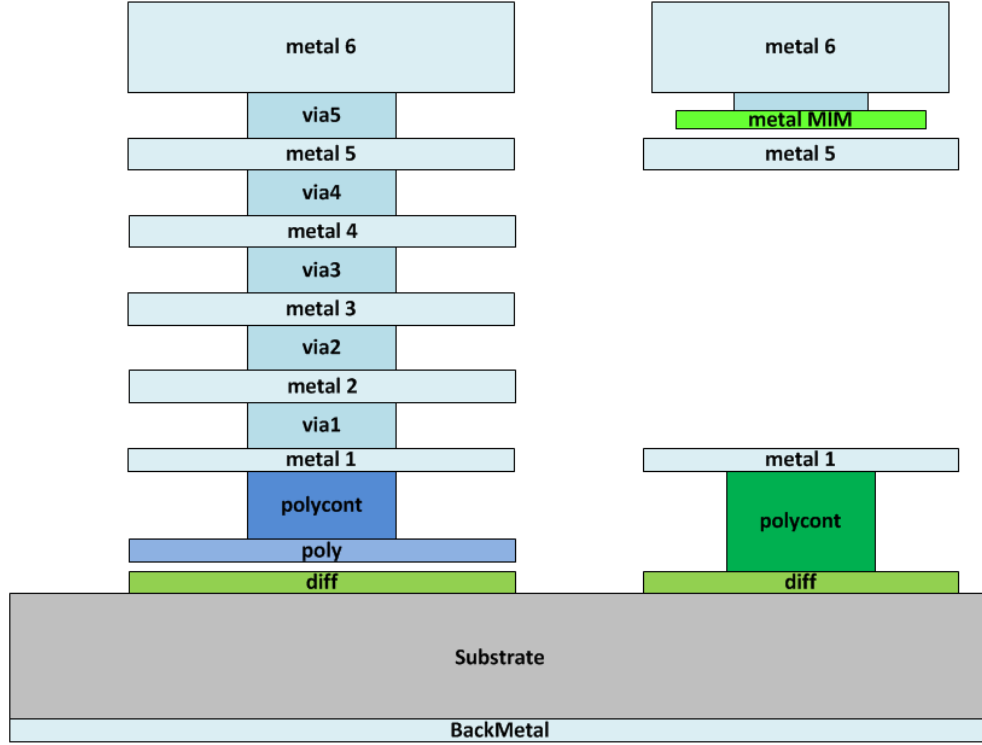


Figure 3.3 Cross section of the metal stack for UMC's 180nm technology

3.4 Transformer design

The electrical properties of monolithic transformers depend on the fabrication process, geometry and frequency. The system specifications set the frequency and the fabrication process fixes the substrate resistivity and the metal stack. Therefore, a designer is left with the geometry to obtain a desired electrical performance, which implies a desired bandwidth, with a minimum of losses and die area.

In the following section the design considerations for the transformer are presented. It first discusses transmission lines, as these are used to implement monolithic transformers. After the design consideration are presented and the last section is transformer tuning. The electromagnetic-simulator EMX is used to evaluate and optimize the performance of the transformer [32].

3.4.1 Monolithic Microstrip

Monolithic transformers are implemented using the metal layers provided by a fabrication process to realize transmission lines. In integrated circuits, these microstrip transmission lines consist of a metal strip above a conducting (or ground) plane with the substrate and intermetal oxide layers sandwiched between the two. To be able to design a transformer it is necessary understand both the behaviour of these microstrip structures, and their interaction with the substrate through electric and magnetic fields. A simplified magnetic and electric field distribution around the microstrip is illustrated in Figure 3.4a.

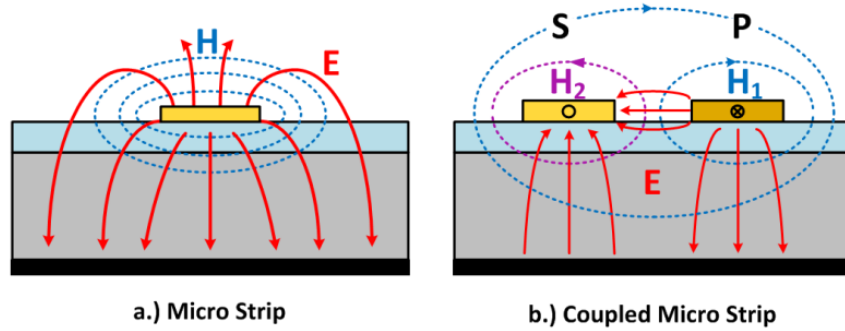


Figure 3.4 Microstrip Transmission Lines

When two strips are placed in close proximity and one is excited by a signal, part of this signal will couple to the other strip and to the substrate. This is illustrated in Figure 3.4b, where a current entering the microstrip P generates a magnetic field H_1 that induces a current that flows out of strip S. The figure also illustrates the electric fields, where it is assumed that P is at a higher potential than S. This interaction can be modelled using coupled inductors and capacitors, which results in the circuit shown in Figure 3.5. A monolithic transformer is implemented by configuring the coupler to obtain a desired electrical behaviour.

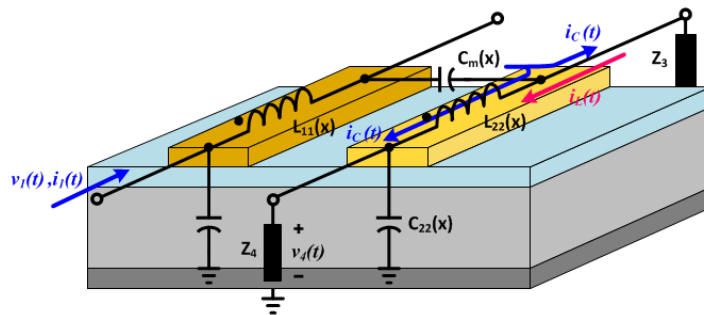


Figure 3.5 Microstrip Coupler

The previous figure neglected loss. A practical coupled line, however suffers signal attenuation through resistive losses and electrical and magnetic coupling via lossy materials. The resistive losses in microstrip are caused by ohmic losses, the skin, edge, and proximity effects, capacitive and magnetic coupling to the substrate [33]. At low frequencies the finite conductivity ($\sigma \neq \infty$, $\rho \neq 0$) of the metal determines the resistance of a microstrip. Above the MHz range the resistance will deviate from the low frequency resistance as frequency dependent losses increases. At these frequencies, induced electromagnetic fields start to influence the current distribution (proximity and edge effect) [34] [33]. Due to the electric fields generated by excess charges the current will start to concentrate at the sharp edges of the conductor. This results in reduced cross-sections for the current flow, which increases the overall resistance. The magnetic field generated by current flow also influence the current distribution through the proximity effect. In the GHz range the skin effect starts to affect the resistance of the microstrip [34]. As frequency increases, the charge carriers are push out of the centre of the conductor resulting in a current flow near the surface of the conductor. These frequency dependent effects were approximated using the EM-simulator.

A microstrip also exhibit losses through magnetic and electric coupling to the substrate. The extent of these losses depends on frequency and substrate resistivity. The substrate resistivity of the fabrication process lies between 15-25 $\Omega\text{-cm}$ and the operating frequency is at 2.45 GHz. Therefore, the propagation mode of the microstrip will lie between slow-wave and Quasi-TEM modes [35]. This means that the electric field below the strip penetrates the substrate as free electron there are no longer able to completely screen the electric field at the oxide-silicon interface. As the wave travels through both the oxide and substrate (which acts as lossy dielectric), signal loss will occur that is proportional to width of the line. As the resistive losses are proportional with width, a microstrip line that supports a wave traveling through the substrate has resistive losses that are inversely proportional and dielectric losses that are proportional to width. Therefore the width of such a microstrip lines will have an optimum were it has the lowest losses. Due to the high resistivity the magnetic losses in substrate are negligible compared to other sources of loss. The high resistivity substrate prevents the occurrence of magnetically induced eddy currents in the silicon substrate [36].

3.4.2 Transformer Design

The turns ratio, winding style and symmetrical octagonal geometry were chosen after doing preliminary EM-simulation on different structures. The width, spacing and inner diameter were optimized through numerous iterations using the EM-simulator EMX [37]. The final transformer obtained through these iterations is presented in Figure 3.6. The octagonal transformer is a symmetric interwound geometry [38] [39] [40] [41]. Both the primary and secondary windings are implemented in top metal to reduce resistance and capacitance to the substrate. The primary winding is denoted with the yellow line, and the secondary with a green line. A physical turns ratio of $N=3$ is realized by using two turns in parallel for the primary and three turns for the secondary. The primary winding has a self-inductance L_{11} of 0.5 nH and a Q-factor of 10. The self-inductance L_{22} of the secondary winding is 3.5 nH with a Q-factor of 10.61. The coupling coefficient between the windings is $k_m = 0.74$. These values combined with the non-ideal coupling result in an effective turn ratio of $N_{\text{eff}} = 2$. These parameters were realized with an outer diameter of $324\text{ }\mu\text{m}$, a strip width of $w = 10$, a spacing of $s = 3$ and an inner diameter is $200\text{ }\mu\text{m}$, and a total area of approximately 0.105 mm^2 . To ease the top-level layout, both centre taps are placed on one side of the transformer and the winding terminals on the other. To obtain much structural symmetry as possible, the metal cross-over sections are a mirror image of each other so that both windings have similar DC resistance.

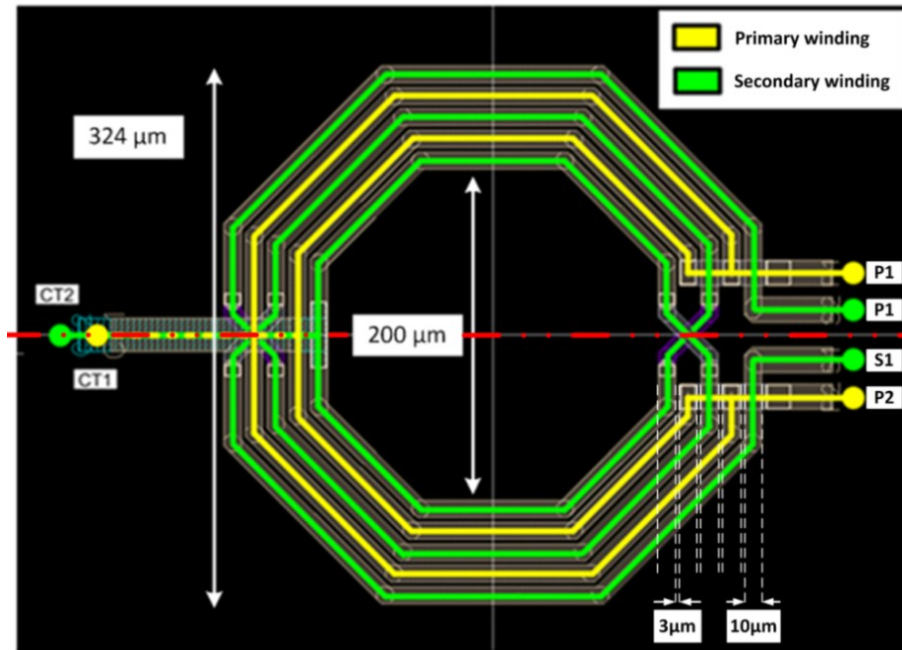


Figure 3.6 The monolithic transformer

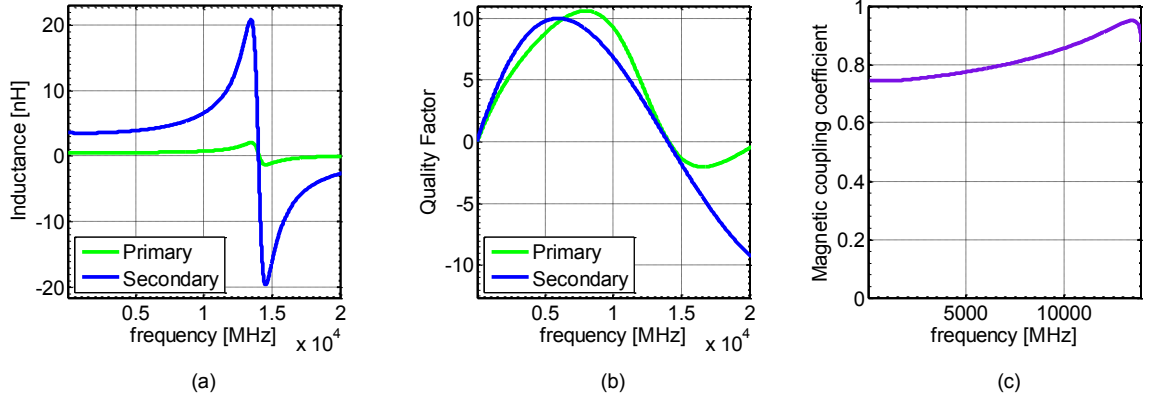


Figure 3.7 Transformer performance

(a) self-inductance of primary and secondary windings vs. frequency

(b) Q-factor of primary and secondary windings vs. frequency (c) magnetic coupling coefficient

Graphs presenting the Q-factor of the two windings were obtained by dividing the imaginary part by the real part of Z_{11} . This ratio is a pessimistic estimate of the actual quality factor. A better approximation can be obtained using the graphs presented Figure 3.8 and the following equation:

$$Q = \frac{f_{peak}}{\Delta f} \quad (3.1)$$

Where f_{peak} is the peak of the frequency response and Δf is the -3dB bandwidth. Using this equation, the Q-factor of the primary winding $Q_p = 13.5$ and secondary winding $Q_s = 13.7$. This Q-factor found using eq. (3.1) is approximately 29 % higher.

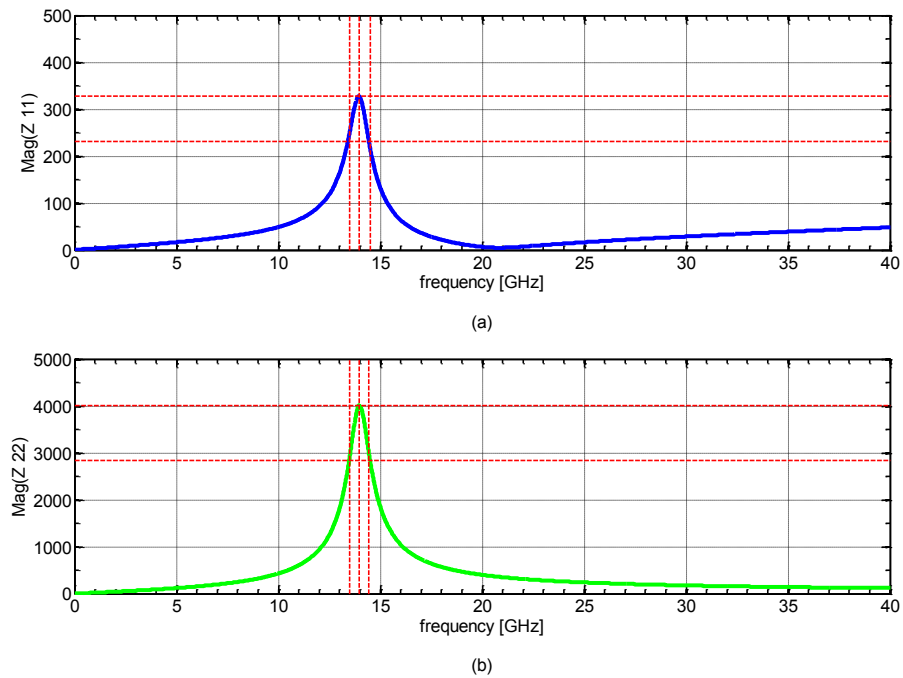


Figure 3.8 (a) Z_{11} vs. frequency (b) Z_{22} vs. frequency

3.4.3 Differential & Single-ended Drive

The hybrid transformer in this work is driven single-ended by the Tx signal, while it is driven differentially by the Rx signal. As the electrical behaviour of a symmetrical winding is dependent on the way the structure is excited, it is important to know how the behaviour of the transformer is changed, depending on either differential or single-ended drive [42]. The difference in the effective self-inductance of the winding is given by:

$$L_{CM} = 2L(1 - k_m) \quad (3.2)$$

$$L_{Diff} = 2L(1 + k_m) \quad (3.3)$$

Also the substrate parasitics perceived by a differential signal differs from the one perceived by single-ended signal. Therefore one should take care to simulate the transformer properly as the frequency behaviour can differ substantially.

3.4.4 Frequency behaviour and tuning

Using the EMX simulator, the transformer can be characterised as a differential structure or as a single-ended structure. The values obtained from these simulation are however not directly applicable to describe the frequency behaviour of the transformer when used as a hybrid transformer. As a hybrid transformer, both in the Rx and Tx operation the frequency behaviour is that of a transformer which has half the self-inductance of the actual transformer. The low frequency equivalent model of a transformer is given in Figure 3.9. The frequency behaviour of the hybrid transformer is such that the self-inductance sensed by the both the Tx and Rx signals is only one-half of the self-inductance of each winding. Therefore, the inductance values that should be inserted in the equivalent transformer model to model its frequency behaviour are given by:

$$L_{Tx} = \frac{L_{CM}}{2} = L(1 - k_m), \quad (3.4)$$

$$L_{Rx} = \frac{L_{diff}}{2} = L(1 + k_m), \quad (3.5)$$

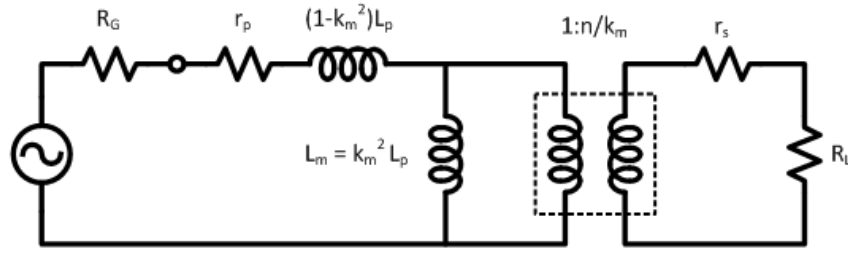


Figure 3.9 Transformer equivalent circuits, low frequency model

To maximize power transfer through the transformer, a capacitor is placed in shunt with each winding. These are tuned so that impedance mismatch between the internal nodes of the transformer is minimized [38]. The effect of these tuning capacitors is illustrated in Figure 3.10. The left graph shows the transfer through a resonant tuned and a non-tuned differentially driven transformer and the right graph shows the same for Rx signal transfer through the hybrid transformer (Rx insertion losses). It is seen that losses are reduced by resonating the transformer. However, because the transformer in a hybrid configuration operates as half a transformer, it is being operated below its lower -3dB cut-off frequency. Although tuning reduces the losses by 14 dB, the losses of the device remain significant (13.5 dB).

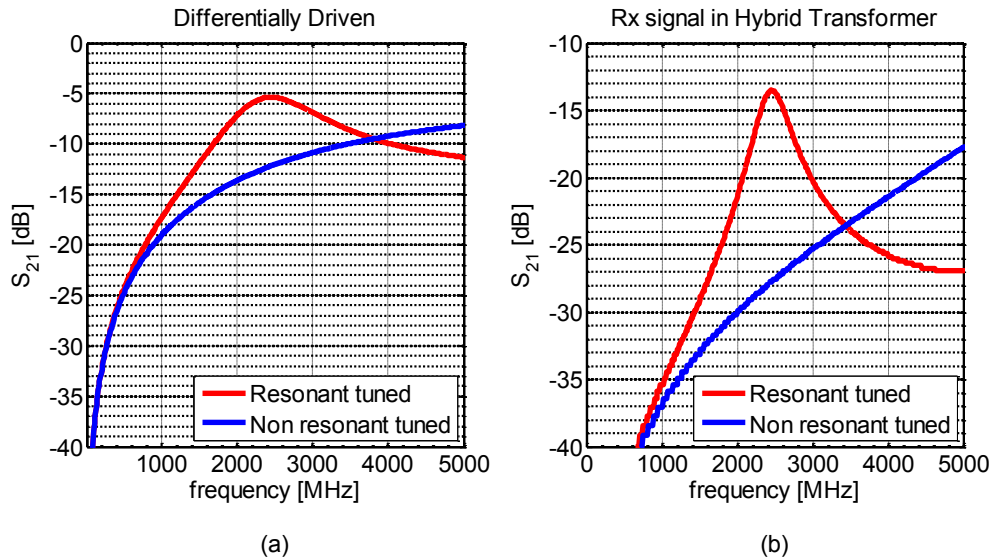


Figure 3.10 Resonant tuned transformers

(a) Differentially driven (b) Hybrid transformer Rx operation

A comparison between EMX simulations and the lumped model is given in Figure 3.13. The top graph compares the magnitude of Z_{11} for both the s-parameters and the lumped model from 10MHz to 40GHz. The middle graph does the same for Z_{22} , and the bottom graph shows the percentage of error between the lumped model and the s-parameters. At the desired frequency of operation (2,45 GHz) this error is less than 3%.

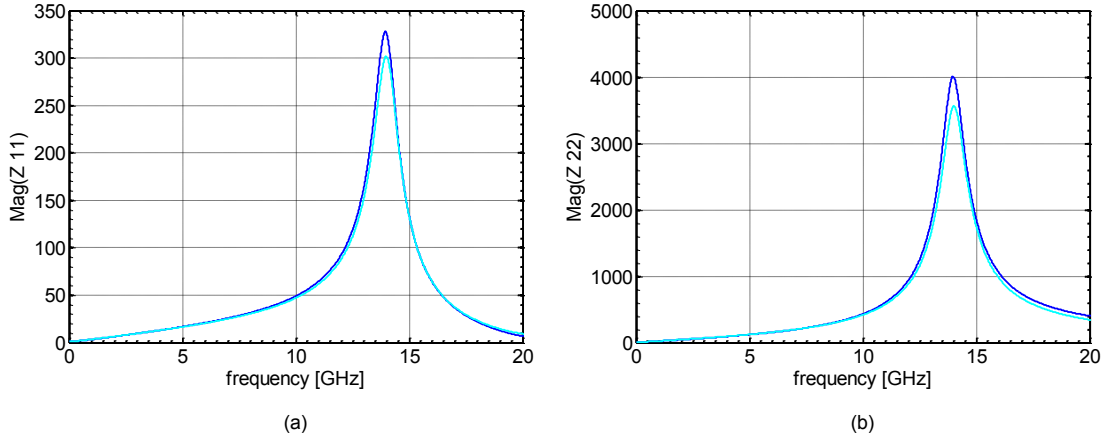


Figure 3.12 S-parameter and lumped model comparison

(a) Z_{11} comparison (b) Z_{22} comparison

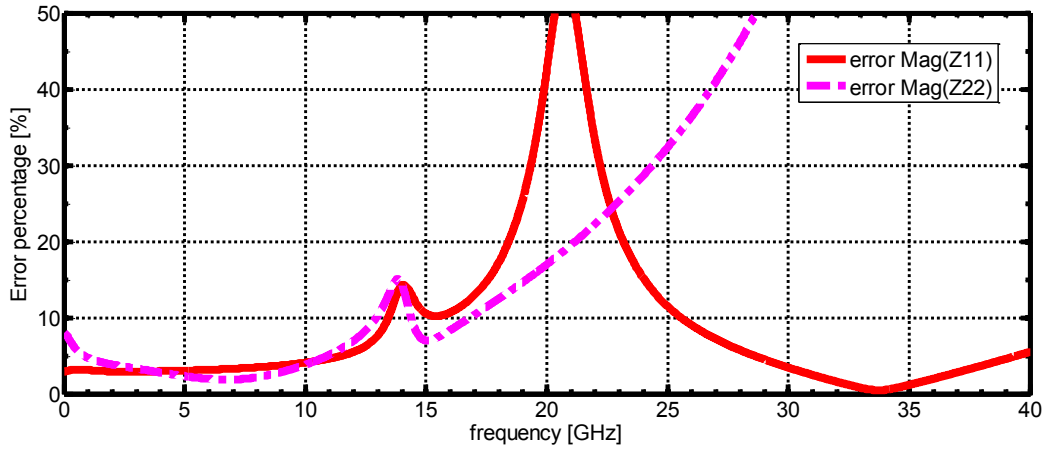


Figure 3.13 Comparison S-parameters and Lumped Model

3.5 Balancing Circuit

In order to design the balancing circuit, two properties of the antenna have to be quantified. The nominal value of the antenna impedance at the frequency of operation, and the maximum excursions of this value due to changes in the antenna's environment are needed. The nominal impedance of the antenna gives the required centre impedance of the balancing circuit, and the maximum excursions relate the impedance range the balancing circuit needs, in order to track the antenna impedance.

An ideal antenna provides a $50\ \Omega$ impedance. However, practical antennas only approximate this impedance at resonance. Another complication is the fact that the impedance of a practical antennas shifts due to changes in the surrounding environment. Both of these non-idealities have to be accounted for to ensure that the balancing circuit is able to mimic the antenna impedance. In order to connect the on-chip duplexer to the off-chip antenna, some form of interconnect is also required. The presence of this interconnect also needs to be taken into account in the design of the balancing circuit, as its presence can change the antenna impedance as seen from the perspective of the duplexer. Therefore the design of a balancing circuit starts with the characterization of the antenna and its intermediate interconnects.

Depending on the output power of the transceiver, precautions need to be taken to prevent damage to the switches used to implement tunability of the duplexer and to prevent non-linear behaviour. The proposed FD environment of this work assumes a Tx output power of -10 dBm. In a $50\ \Omega$ system, the voltage swing across the balancing circuit should never exceed 1 Vp-p. This means no precautions are needed to prevent device breakdown or to mitigate linearity problems.

All components in the duplexer are passive except for the FETs used to implement tunability. The extent to which these device limit linearity depends on the output power of the transmitter and the voltage swing this power generates across the non-linear devices. As output power is a system requirement, linearity can only be improved by reducing the voltage swing across these non-linear components.

3.5.1 Antenna characteristics

The measured interconnect and a lumped model of an antenna is presented in Figure 3.14. The interconnect consist of an on-chip pad capacitance C_{ic} , the bondwire L_{bond} , the PCB pad C_{pad} , and the transmission line to the antenna.

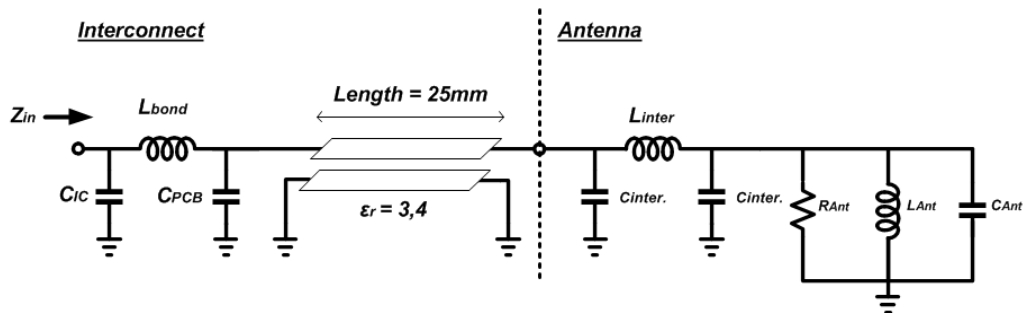


Figure 3.14 Expected interconnect to the antenna

The measurement results close to the design frequency are presented in Figure 3.15. All curves relate the impedances obtained after combining the interconnect and the antenna measurements. The dark blue line and the red curve result from measurements in a controlled environment. The purple and light blue curves are obtained by putting different metal objects near the antenna during measurements. The measured impedance values at 2.45 GHz are presented in Table IV

Table IV Measured antenna impedances

Measurement	Z_{Ant} at 2.45GHz
Min. excursion	16.68 –j11.27 Ω
typical	20.70 –j15.66 Ω
Max. excursion	21.33 –j27.34 Ω

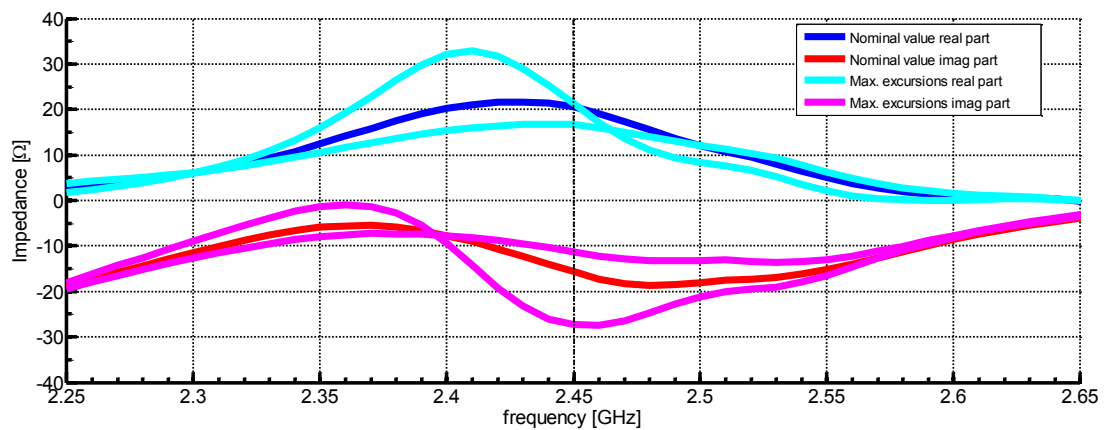


Figure 3.15 Antenna impedance over frequency

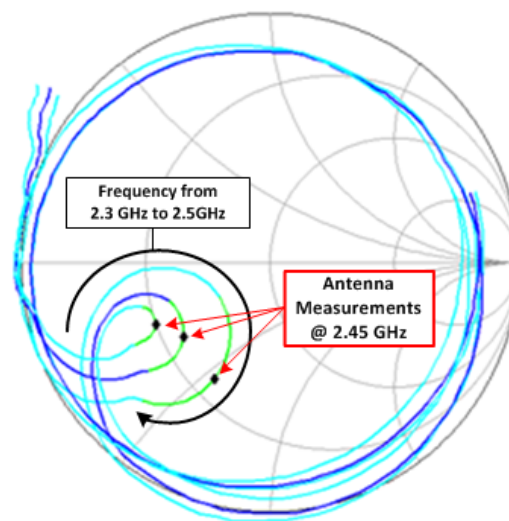


Figure 3.16 Antenna impedance over frequency plotted on a Smith chart

3.5.2 Required Balancing Range

Using the measurements of the previous section, the required range of the balancing circuit can be derived. The location of nominal antenna impedances and the minimum and maximum excursions at 2.45GHz are illustrated on the Smith chart presented in Figure 3.17.

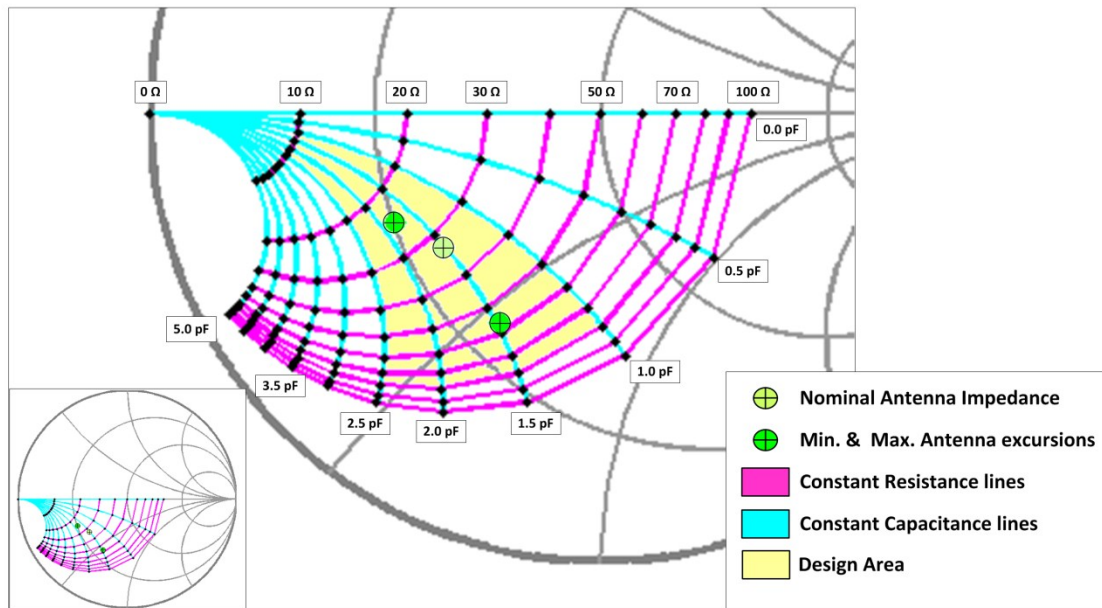


Figure 3.17 Required Balancing Range

As the measured impedances are located in the lower part of the Smith chart, the antenna can be mimicked by a parallel RC network. This hypothesis is confirmed with simulations of an ideal parallel RC network. The results of the simulations are presented in Figure 3.17 as the blue and purple lines. The blue lines were generated with fixed capacitance values and a varying the resistance from 0 Ω to 100 Ω . The purple lines are generated with a fixed resistance and a varying capacitance from 0 pF to 5.0 pF. This grid is used instead of Eqs. (2.15) and (2.16) to simplify analysis.

The generated grid shows that the nominal impedance values of the antenna and the impedance excursions to this impedance can be covered at 2.45 GHz, if the balancing area is implemented with a variable resistance between 10-to-80 Ω and a variable capacitance from 1.0-to-2.5 pF.

3.5.3 Balancing circuit requirements

In the previous section it is analysed that the balancing circuit requires a capacitive tuning range from 1-to-2.5 pF and a resistive tuning range of 10-to-80 Ω .

However, the resistive and capacitive part of the balancing circuit cannot be designed independently because circuits and components come with unwanted parasitics, shown in Figure 3.18. In this figure C_{par} denotes the parasitic capacitance of the tuneable resistance R_{TR} . The parameter C_{off} is the off capacitance and R_{par} is the parasitic resistance of the tuneable capacitance C_{TC} .

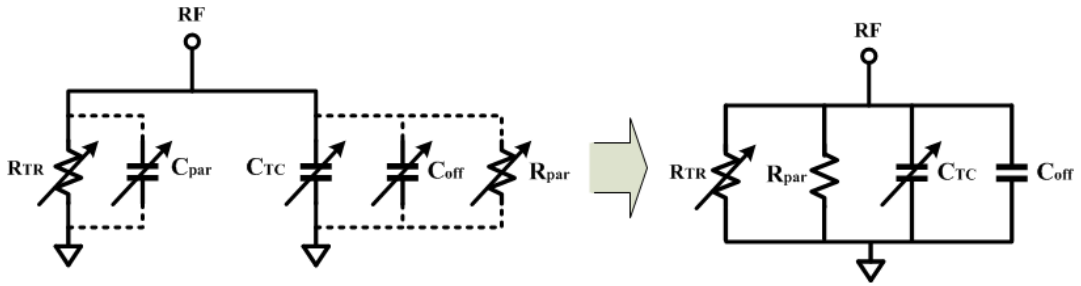


Figure 3.18 Parallel RC network with parasitics

Therefore, the tuning ranges of both the tuneable capacitor and resistance have to be designed in such a way that they absorb the parasitics of their counterpart. For the tuneable resistance, this implies that tuning range has to be extended so that it can absorb the equivalent parallel resistance of the capacitor bank. This is done by extending the range of the resistive part from 10-to-80 Ω to 10-to-100 Ω . Using these values the minimum equivalent parallel resistance R_p of the capacitor bank can be calculated using:

$$R_{Parallel} = \frac{R_{TR} R_{eq}}{R_{TR} - R_{eq}} \quad (3.6)$$

Here R_{TR} is the highest value of the tuneable resistance, and R_{eq} is the desired maximum value for the tuning range. For $R_{TR} = 100\Omega$ and $R_{eq} = 80\Omega$, it follows that R_p becomes 400 Ω . The R_p can be combined with the desired maximum capacitance value C_{max} to find the minimum required quality factor of the capacitor bank Q_{CB} by using:

$$Q_{CB} = 2\pi f R_{Parallel} C_{max} , \quad (3.7)$$

where f is the frequency of operation. In this particular design the required quality factor is $Q_{CB}=15.4$.

To be able to absorb the capacitive parasitics of both the tuneable resistance and the capacitance, these must be lower or equal to the desired C_{off} , which equals the minimum desired capacitance value of the balancing circuit $C_{min} = 1\text{pF}$. Therefore, the boundary condition for the parasitic capacitances is given by:

$$C_{OFF,eq} = C_{res,max} + C_{cap,off}. \quad (3.8)$$

Counter to this desire to have low parasitic capacitance, is the desire to ensure good agreement between simulations and the fabricated circuits. The RF models available in the library are characterized at higher frequency, include inductive parasitics, and have controlled capacitive parasitics by ensuring a given environment. Their drawback is their larger footprint and more constraints for the design rule check (DRC). Because the predictable behaviour of the tuneable resistance is critical to the performance of the balancing circuit and thus the duplexer, the devices used to implement the large range tunability of the balancing circuit are implemented using RF instead of mixed-mode models.

3.5.4 Resistive Part

The tuneable resistance dominates the real part of the balancing impedance as is given in eq. (2.15). To be able to absorb the parasitic resistance of the capacitor bank it requires a range from 10-100 Ω . The parasitic capacitance of the resistance should be minimized, as the total C_{off} of the balancing circuit is bounded.

A tuneable resistance can be implemented as an active [42] or a passive circuit. An active circuit is dismissed as the additional noise they generate makes them unsuitable for radio front-ends. A passive tuneable resistance can be realized as a; digitally switched resistor bank as in [24], as an analog controlled parallel transistor resistor pairs as used in [22], or a combination of both. However the critical requirement for the tuneable resistance is a low C_{off} . This requirement conflicts with the desire to use RF models to implement the dominant part of the tuning range.

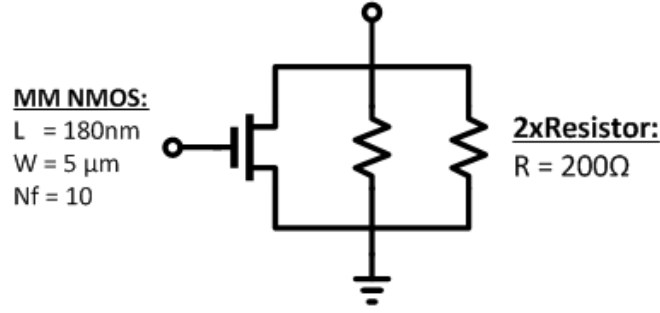


Figure 3.19 Resistive part of balancing circuit

Eq. (3.6) is used to calculate the required R_{ds} to obtain a minimum resistance of $10\ \Omega$ with the parallel $100\ \Omega$ of the resistor and the $400\ \Omega$ of the tuneable capacitance. This results in an R_{ds} of approximately 10Ω . This requires a 10 finger RF transistor is parallel with 100Ω as can be seen in Figure 3.20. The expected C_{par} from the transistor brings along $160\ \text{fF}$ capacitance. The $100\ \Omega$ resistor is implemented using two $200\ \Omega$ resistors in parallel, because $100\ \Omega$ RF resistors were not available in the library.

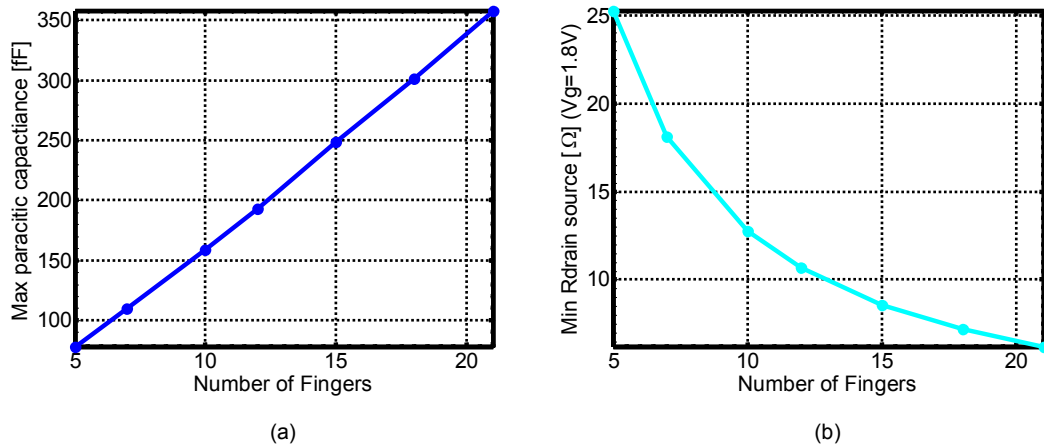


Figure 3.20 RF NMOS sizing

(a) R_{ds} vs. number of fingers (b) maximum $C_{paracitic}$ of RF NMOS vs. number of fingers

Figure 3.20 also explain why the tuneable resistance is implemented with such a simple topology. The use of the single tuneable RF device uses about $1/10^{\text{th}}$ of the of the total C_{off} budget of the complete balancing circuit. The obtained tuning range is given in Chapter 4, were it is presented together with the behaviour of the circuit after layout.

3.5.5 Capacitive Part

The tuneable capacitance should have a maximum C_{off} of $1.0\ \text{pF}$, a tuning range ΔC_{total} of 1.5pF , a quality factor higher than 16 and the resolution should be as high as possible without violating the previously stated requirements.

Tuneable capacitances can be made with switched capacitors or with digital or analogue-controlled varactors. Analogue tuning provides high resolution, but digital control is easier to implement and more robust. The smallest MIM capacitor provides ΔC_{MIM} of 2 fF, and the smallest MOS varactor gives a $\Delta C_{\text{MOS}} = 0.23$ fF. Using eq. (2.16) with $R = 85$ (worst-case R), this results in an imaginary impedance steps of 220 m Ω and 25 m Ω , respectively. If 25 m Ω steps are provided along real axis as well, eq. (2.14) predicts 95 dB isolation. As high isolation can be obtained digitally, a digitally switched topology is chosen to implement the tuneable capacitance.

The tuneable capacitance consists of three 4-bit binary controlled capacitor banks. These three 4-bit banks are combined to form the 12-bit bank depicted in Figure 3.21. This bank has a 1.575 pF tuning range from 0.7 pF to 2.275 pF with a minimum step of 0.7fF. To prevent gaps in tuning range the 20% overlap is ensured. The coarse and the fine bank are designed using MIM capacitors and provide unit step of 105 fF and 8.5 fF, respectively. The super-fine bank uses MOS varactors and provides 0.7fF steps. The Q-factor of the combined 12-bit bank is 17.

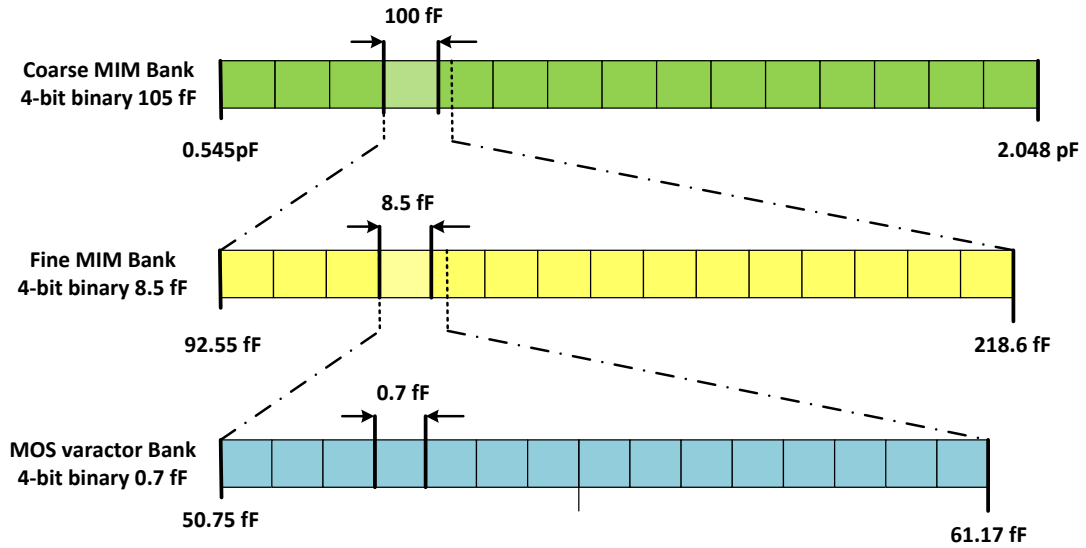


Figure 3.21 Structure of 12-bit binary controlled tuneable capacitance

3.5.1 MIM Capacitor Banks

The coarse and the fine banks are implemented using switched MIM capacitors. The circuit used is presented in Figure 3.22a and consists of a NMOS, a MIM capacitor and a resistor. The N-MOSFET implements the switch, the MIM capacitor provides the capacitance, and the resistor is added to reduce the capacitance in the OFF-state. The

NMOS is placed below the MIM capacitor with its source fixed to ground in order to minimize the modulation of the transistors drain-source resistance.

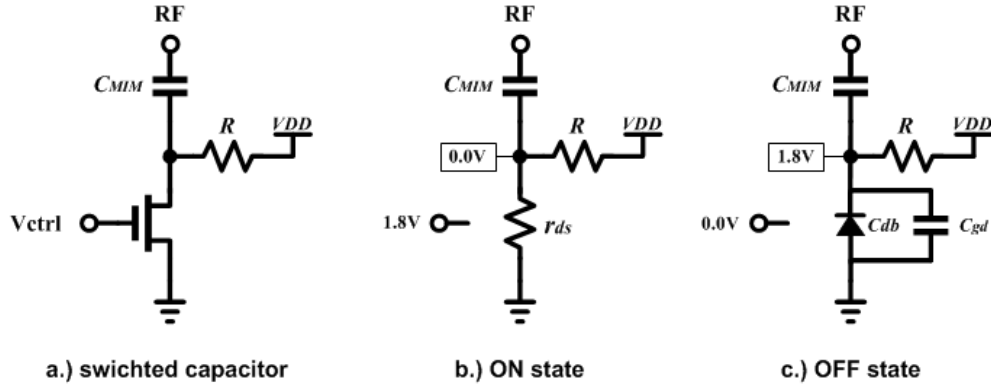


Figure 3.22 (a.) switched capacitor circuit (b.) ON-state (c.) OFF-state

The key characteristics of switched capacitors are their quality factor in the ON-state and the capacitance ratio between the ON and OFF state. This capacitance ratio is needed to realize 1.5 pF tuning range. The quality factor must be higher than 16 so that the restive tuning range of the balancing circuit is not degraded.

A switched capacitor has an OFF and ON state. In the ON state, no current flows through the transistor as it is blocked by the capacitor. No current implies no drain-source voltage across the device, thus the transistor is operating in triode region and can be modelled a resistor r_{ds} as presented in Figure 3.1b. The value of r_{ds} is given by [44]:

$$r_{ds} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{gs} - V_t)} \quad (3.9)$$

Here μ , C_{ox} , W , and L are the electron mobility, gate oxide capacitance per area, width and length of the transistor, respectively. As μ and C_{ox} are fixed by the technology, only W and L can be used to achieve a desired performance. Using this r_{ds} , the quality factor Q of the switched capacitor is given by [44]:

$$Q = \frac{1}{2\pi f C_{MIM} r_{ds}}, \quad (3.10)$$

where f is frequency and C_{MIM} is the capacitance of the MIM capacitor. These two equations show that a high quality factor can be achieved by using a high aspect ratio, because it has lower resistance as can be seen in Figure 3.23 Decreasing R_{ds} with larger . However, increasing the width of the device increases the parasitic capacitance of the device in the OFF-state as shown in Figure 3.24.

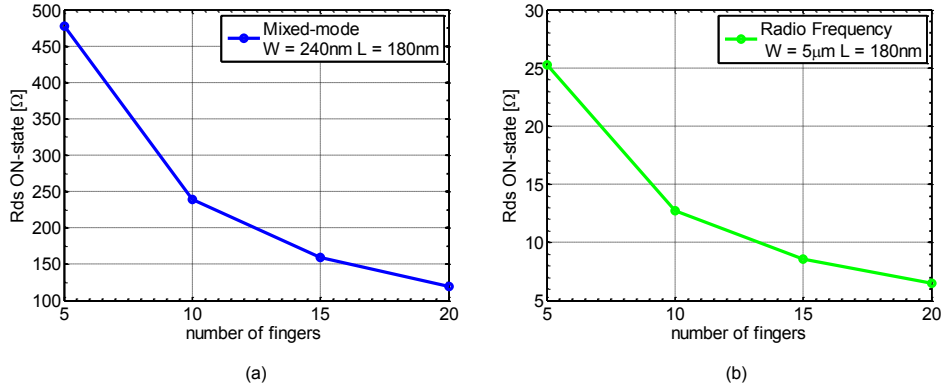


Figure 3.23 Decreasing R_{ds} with larger width
(a) fine capacitor bank (b) coarse capacitor bank

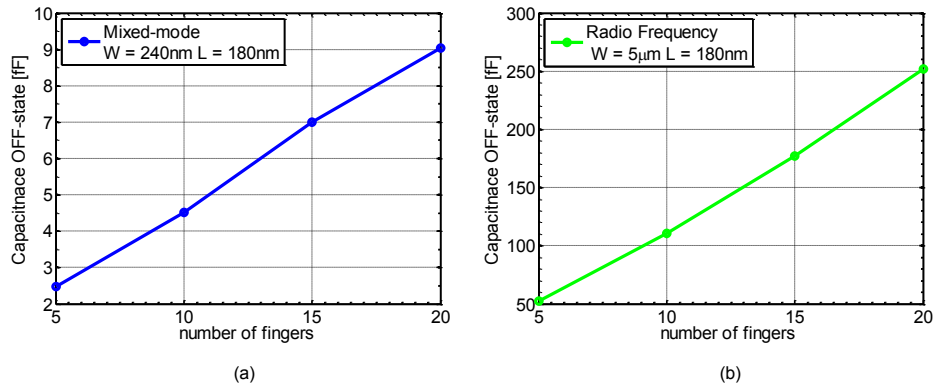


Figure 3.24 Increasing C_{par} with larger width
(a) fine capacitor bank (b) coarse capacitor bank

In the OFF-state presented in Figure 3.25a, the resistance of the device is large. The impedance seen by the signal is therefore dominated by the drain-to-bulk capacitance C_{jbd} and drain-gate capacitance C_{gd} . The drain-bulk capacitance comes from the pn-junction formed by the p-doped substrate and the n-doped drain. The gate-drain capacitance comes from the drain and gate overlap as shown in Figure 3.25b. In this figure the RF signal path through the switch is given for both the ON and OFF states.

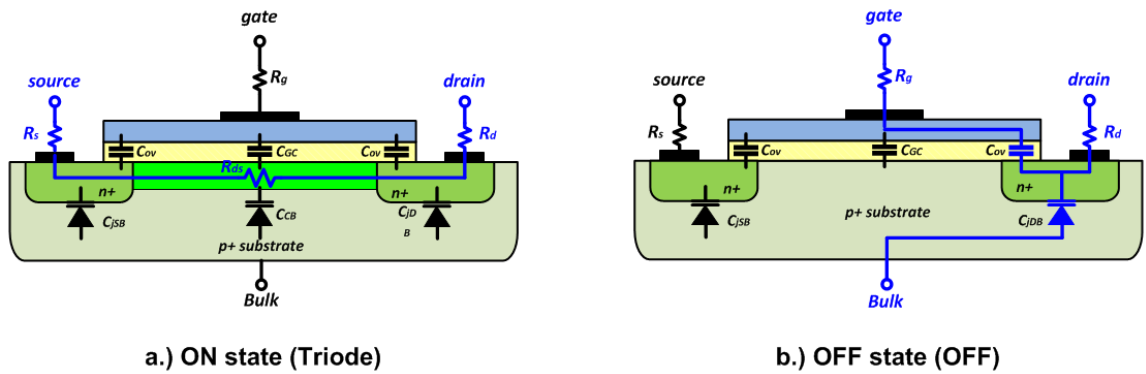


Figure 3.25 Model during ON and OFF state of the switch

The capacitance seen by the RF-signal in the OFF-state is thus the series connection of the MIM capacitor and the parasitic capacitance at the drain of the switching device. Thus the equivalent capacitance in ON and OFF state are given by:

$$C_{off} \approx \frac{C_{MIM}(C_{jdb} + C_{gd})}{C_{MIM} + (C_{jdb} + C_{gd})} \quad (3.11)$$

$$C_{on} \approx C_{MIM} \quad (3.12)$$

The parasitic capacitance of the device is proportional to the width. The main trade-off in the design of the switched capacitor is between Q-factor and tuning range [43].

The trade-off can be relaxed by adding a large resistor from the drain to Vdd. In the OFF-state, this fixes the drain bias voltage to Vdd, and thereby reduces the capacitance due to the reversed biased drain-bulk junction [43]. The improvement from adding the resistors is shown in Figure 3.26. The figure shows the quality factor and tuning range of a reverse biased drain-bulk pn-junction and a non-biased junction. The graph is obtained using a fixed 11 fF MIM capacitor and a NMOS with $L = 180$ nm and $W = 750$ nm and sweeping the number of fingers for both the biased and unbiased case. The red line in the graph indicates a tuning step ΔC of 8.5 fF. Where the curves of the biased and unbiased case intersect the required number of fingers is found to provide the desired 8.5 fF step. The right graph shows a bigger tuning step for the reverse biased C_{jdb} . This allowed a wider transistor for a given tuning range, which results in a higher quality factor. The desired tuning range of 8.5 fF is obtained with 3 fingers with no bias, and 4 fingers when reversed biased. This gave a 33% higher the quality factor as it went from 24 to 32. The 100 fF switched capacitor showed a 16% improvement.

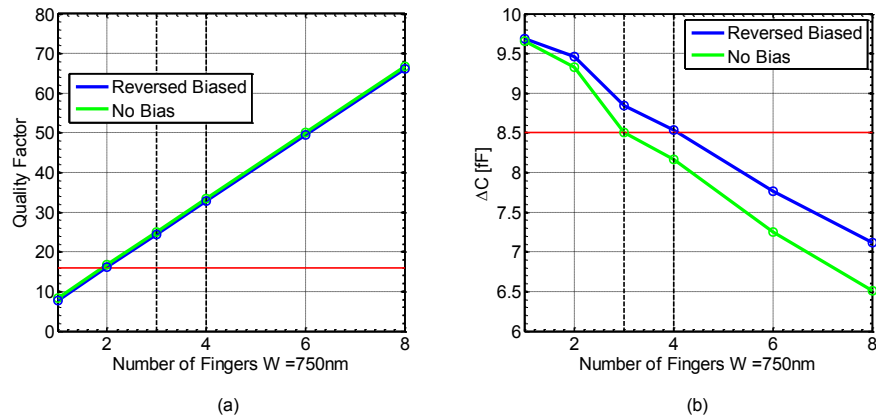


Figure 3.26 Biased vs. unbiased switched capacitor

(a) Q-factor vs. number of fingers (b) capacitive tuning step vs. number of fingers

Using the considerations above and after layout iterations, the MIM capacitor banks are implemented as given in Figure 3.27. The coarse MIM bank consists of a 15 unit cells constructed with a 133.4 fF RF MIM capacitor, a 74.5 k Ω resistor, and a 5 finger, 5 μ m wide, minimum length RF NMOSFET. The fine MIM bank consists of a 11.53 fF MIM capacitor, a 21.26 k Ω resistor, and a 4 finger 750nm wide minimum length MM NMOSFET. Resulting characteristics of both unit cells and both banks are given in Table V.

Table V MIM Unit Cell and MIM capacitor Bank characteristics

Unit Cells	Coff	Con	ΔC	Q	Rp
100 fF	35.5 fF	135.7 fF	100.2 fF	19	9.3 K Ω
8.5 fF	4.6 fF	13.0 fF	8.4 fF	25	128.9 K Ω

MIM Cap. Banks	Coff	Con	ΔC	Q	Rp
100 fF	0.65 pF	2.13 pF	1.48 pF	18.5	0.56 K Ω
8.5 fF	92.5 fF	218.6 fF	126.0 fF	27	8.08 K Ω

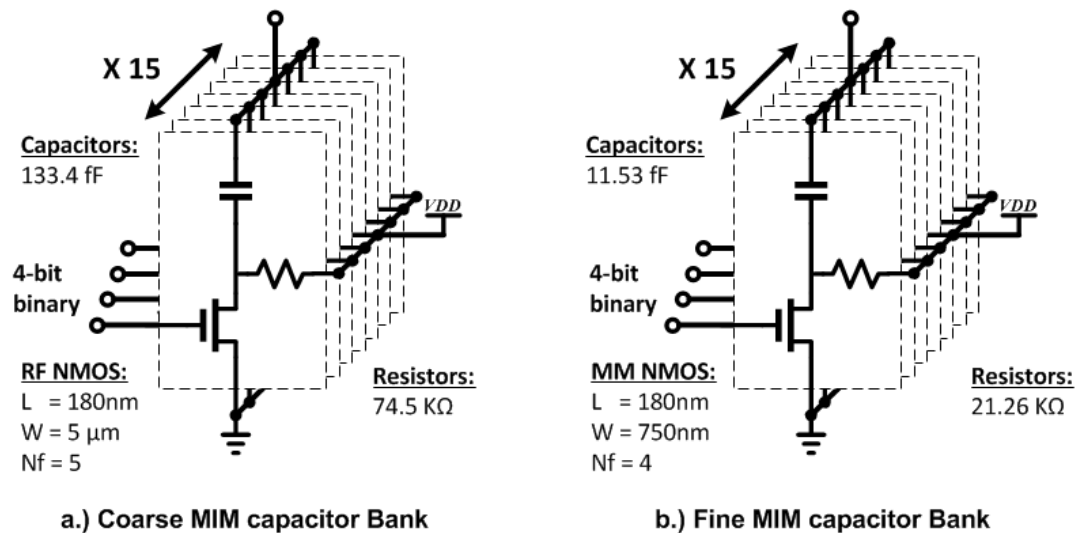


Figure 3.27 The MIM capacitor banks (a.) Coarse 100fF (b.) Fine 8.5fF

3.5.2 MOS Capacitor Bank

The finest resolution of the balancing circuit is realized using a MOS varactor bank. This bank uses inversion-mode PMOS varactors because these can be controlled with the available supply voltage to switch between inversion and weak inversion modes. The desired tuning range of the varactor bank is 10.5 fF (8.5fF plus 20%) which means a capacitance step of 0.7 fF is required. As stated in the previous section the Q-factor should be 17.

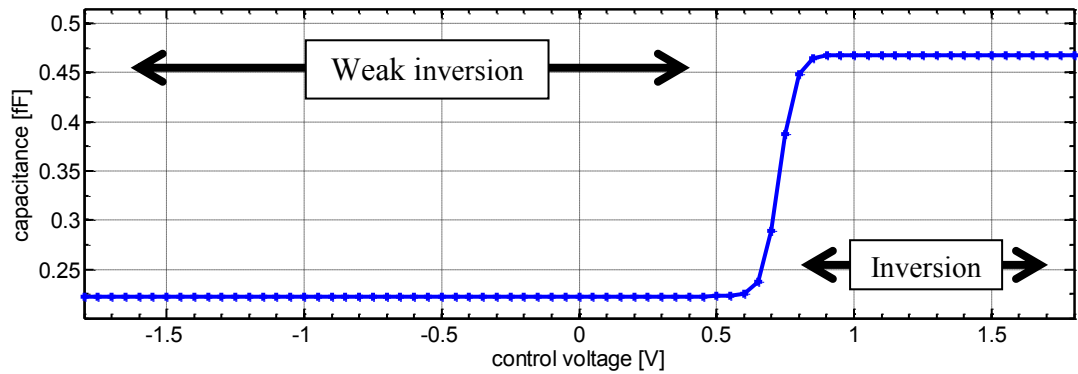


Figure 3.28 C-V curve PMOSFET

The MOS varactor can be controlled digitally. The signal path through the device in the both states is illustrated Figure 3.29.

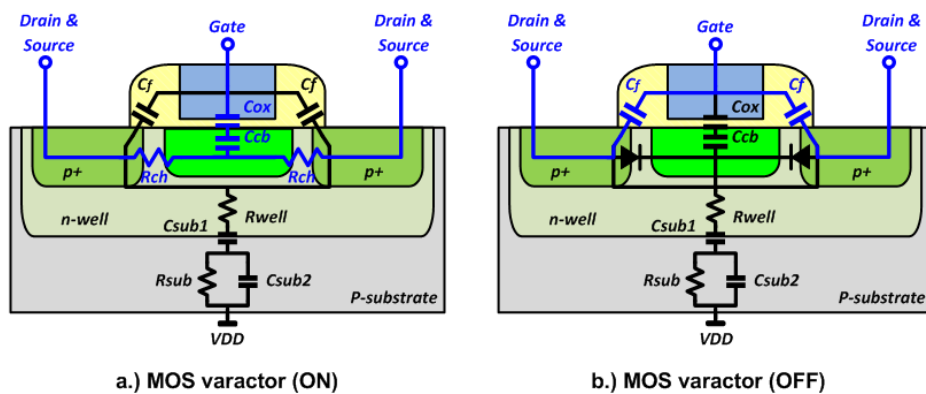


Figure 3.29 MOS varactor (a) inversion (b) weak inversion

In the ON state, the drain and source are at a high potential relative to the gate, the pn-junction between the source drain and channel are therefore forward biased and can be modelled as resistors. The signal at the gate therefore sees channel-to-bulk

capacitance C_{cb} in series with the channel resistance R_{ch} . The quality factor in the ON state is therefore given by [44]:

$$Q_{ON} = \frac{1}{2\pi f C_{cb} R_{ch}} , \quad (3.13)$$

where R_{ch} is proportional to the length of the device and C_{cb} , is proportional to the gate area. The highest quality factor is obtained using minimum length device to implement the varactors because R_{ch} is proportional to length.

In the OFF-state, the source and drain are at same potential as the gate, which implies that the device is not biased and the resistance of the pn-junction is relatively large. The signal at the gate travels the path of least impedance, therefore it sees the fringing capacitance between the gate and drain-source terminals. Thus, in the OFF-state the off capacitance C_{off} of the varactor is given by:

$$C_{OFF} \approx 2C_f , \quad (3.14)$$

where C_f is the fringing capacitance, which is proportional to the width of the device. Increasing the gate area by increasing the width also increases the C_{off} proportionally. To achieve high Q , the length of the device should be minimized, and to achieve a large tuning range a large gate area is required which requires a large length. To compute the Q -factor of a MOS varactor bank, the channel resistance of the device is required. The equivalent circuit in Figure 3.30a models the resistance and capacitance under the gate, which results into an equivalent R_{ch} that can be related to the drain-source resistance by [44] [45]:

$$R_{ch} \approx \frac{R_{ds}}{12} \quad (3.15)$$

The R_{ch} which approximates losses in the channel can be inserted into the lumped model given in Figure 3.30b. This method is used to obtain the graphs presented in Figure 3.31. The left graph gives the on-capacitance C_{on} in light blue and the off-capacitance in darker blue. The difference between the lines in Figure 3.31a shows the tuning step and which increases with device length. The middle graph shows R_{ch} which increases with length. The right graph shows the declining quality factor with device length, where it can be seen that the length has to be kept below 500nm.

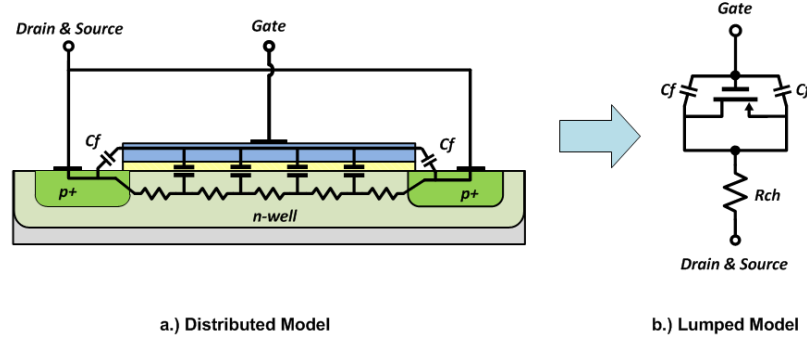


Figure 3.30 PMOS varactors (a) distributed model (b) lumped equivalent circuit [35]

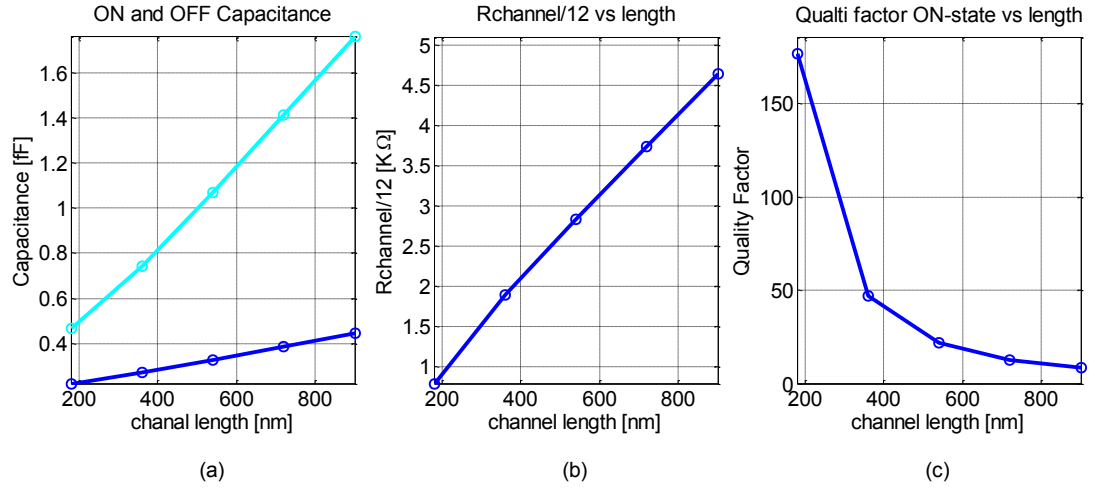


Figure 3.31 MOS varactor device sizing

(a) C_{ON} & C_{OFF} vs. channel length (b) $R_{channel}$ vs. channel length (c) Q-factor vs. channel length

The MOS varactor bank that resulted after layout is given in Figure 3.32. Each unit cell consists of a one finger, square PMOS transistor with a length and width of 360 nm. The bulk is connected to VDD, the gate to the RF signal, and the source and to the control line through two minimum size inverters. In the ON-state, these inverters provide a low ohmic connection to VDD so that Q-factor is not degraded by the resistance of the control line. The first inverter provides a short path from the drain source terminal to VDD in the ON-state. A second inverter avoids confusion in control signal polarity. The final characteristics of the bank are given in Table VI.

Table VI MOS varactor unit cell and bank characteristics

MOS varactor	Coff	Con	ΔC	Q	Rp
Unit Cell	0.65 pF	2.13 pF	1.48 pF	18.5	0.56 K Ω
Bank	92.5 fF	218.6 fF	126.0 fF	27	8.08 K Ω

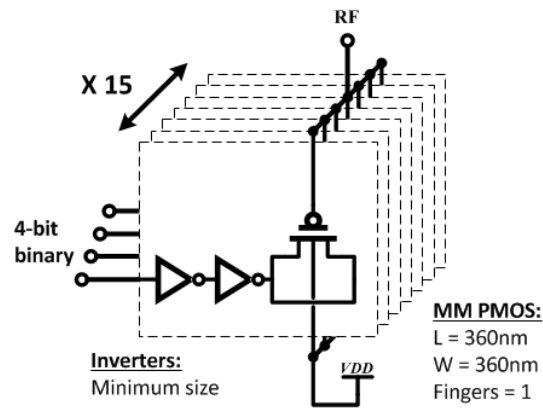


Figure 3.32 MOS varactor bank

3.6 Low noise amplifier

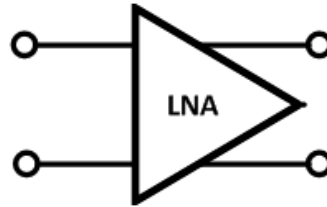


Figure 3.33 Symbol differential LNA

A symbol for the LNA provided by IMEC is presented in Figure 3.33 Symbol differential LNA. As the performance of the LNA affects measurement results, its performance relevant characteristics are listed stated in Table VII LNA Performance metrics.

Table VII LNA Performance metrics

Parameter	Value @ 2.45GHz
Gain	6.5 dB
Reverse Isolation	-26 dB
Z_{in}	$15 - j225$
Z_{out}	$80 - j110$
NF	4.4 dB
NF_{min}	0.7 dB
-1dB gain compression at input	2.3 dBm
IIP3	16 dBm

3.7 Schematic design

The complete duplexer design is presented in Figure 3.34. It includes the lumped model of the transformer, the capacitors that resonates the transformer, the balancing circuit, and the LNA. The balancing circuit consist of the two MIM capacitor banks, the MOS varactor bank and the tuneable resistance. The performance of this complete circuit is described in the next chapter where both pre- and post-layout simulation are compared.

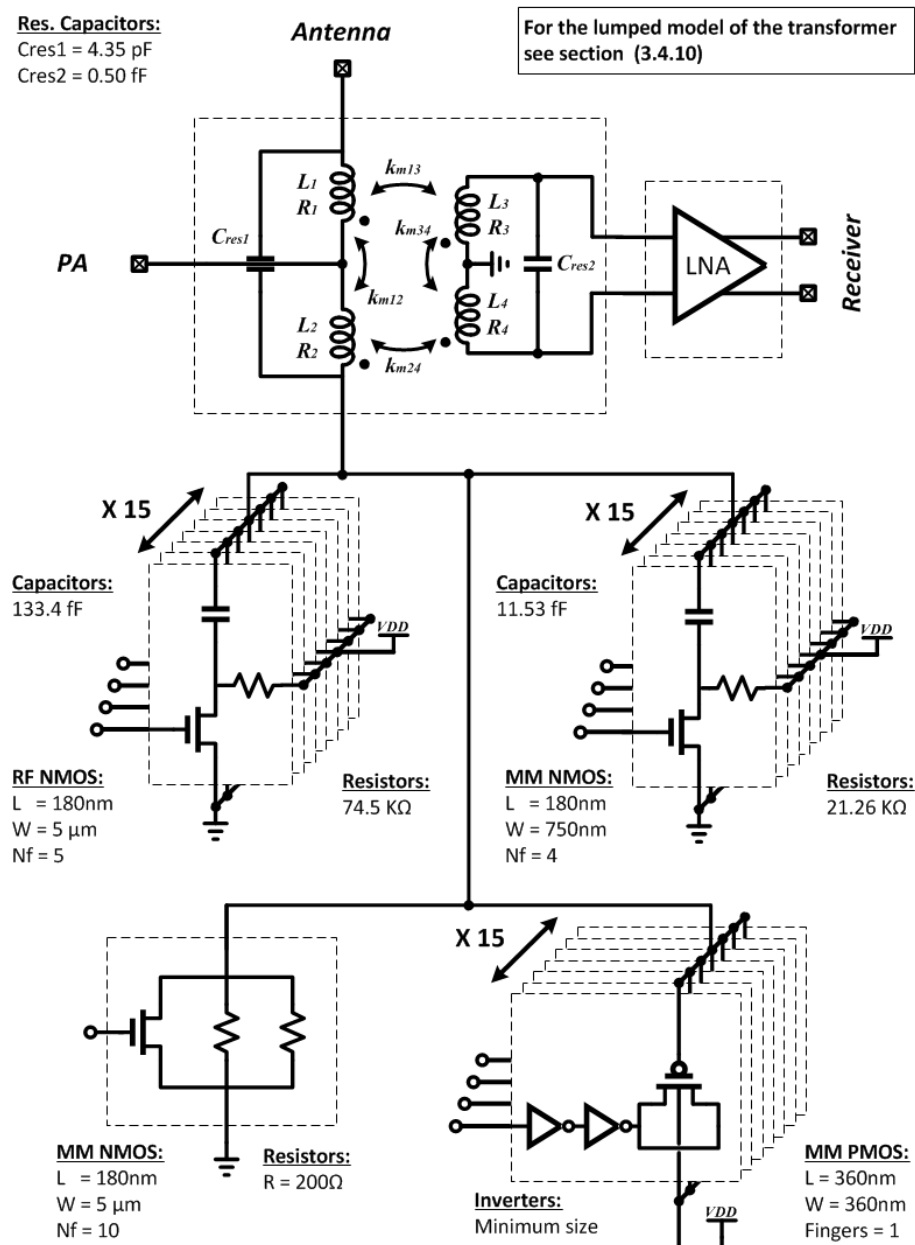


Figure 3.34 Electrical Balance duplexer circuit schematic

Chapter 4

Physical Layout

This chapter describes the physical layout of duplexer prototype. It starts with the complete layout and works its way down to the individual sub-circuits. For each block, the effect of the layout on the performance is given. The chapter ends with a comparison of pre- and post-layout simulation of the complete duplexer performance.

4.1 The Complete Layout

The complete layout of the electrical balance duplexer and the IMEC LNA is presented in Figure 4.1. The location of the transformer, the balancing circuit, the LNA and the shift registers are indicated by the pink outlines. Decoupling capacitors cover the remaining area, except for an area occupied by an IMEC test structure. An area breakdown of the different sub-circuits is given in Table VIII Sub-circuit area breakdown.

Table VIII Sub-circuit area breakdown

Sub Circuit	Dimensions	Area
Transformer	$475\mu\text{m} \times 475\mu\text{m}$	0.225mm^2
Resonator Caps	$230\mu\text{m} \times 100\mu\text{m}$	0.023mm^2
Balancing Circuit	$325\mu\text{m} \times 355\mu\text{m}$	0.115mm^2
Noise matched LNA	$120\mu\text{m} \times 280\mu\text{m}$	0.033mm^2
Shift Register	$80\mu\text{m} \times 120\mu\text{m}$	0.001mm^2
	Total	0.397 mm^2

Symmetry around the transformer was maintained as much as possible in the layout, so that the desired balance condition would not be disturbed. This meant symmetric interconnect and a symmetric environment around the transformer, so that any undesired parasitics would balance out across the transformer. The second concern was

any possible shift of the balancing region due to layout parasitics in the balancing circuit. The introduced parasitics of the initial schematic circuit caused a significant shift in the balancing region, therefore an extra iteration between pre- and post-layout was needed to absorb most of the layout parasitics. For the schematic circuit to absorb the layout parasitics, the component values needed to be reduced. This is the reason why post-layout simulations show the desired behaviour and pre-layout values seem too small.

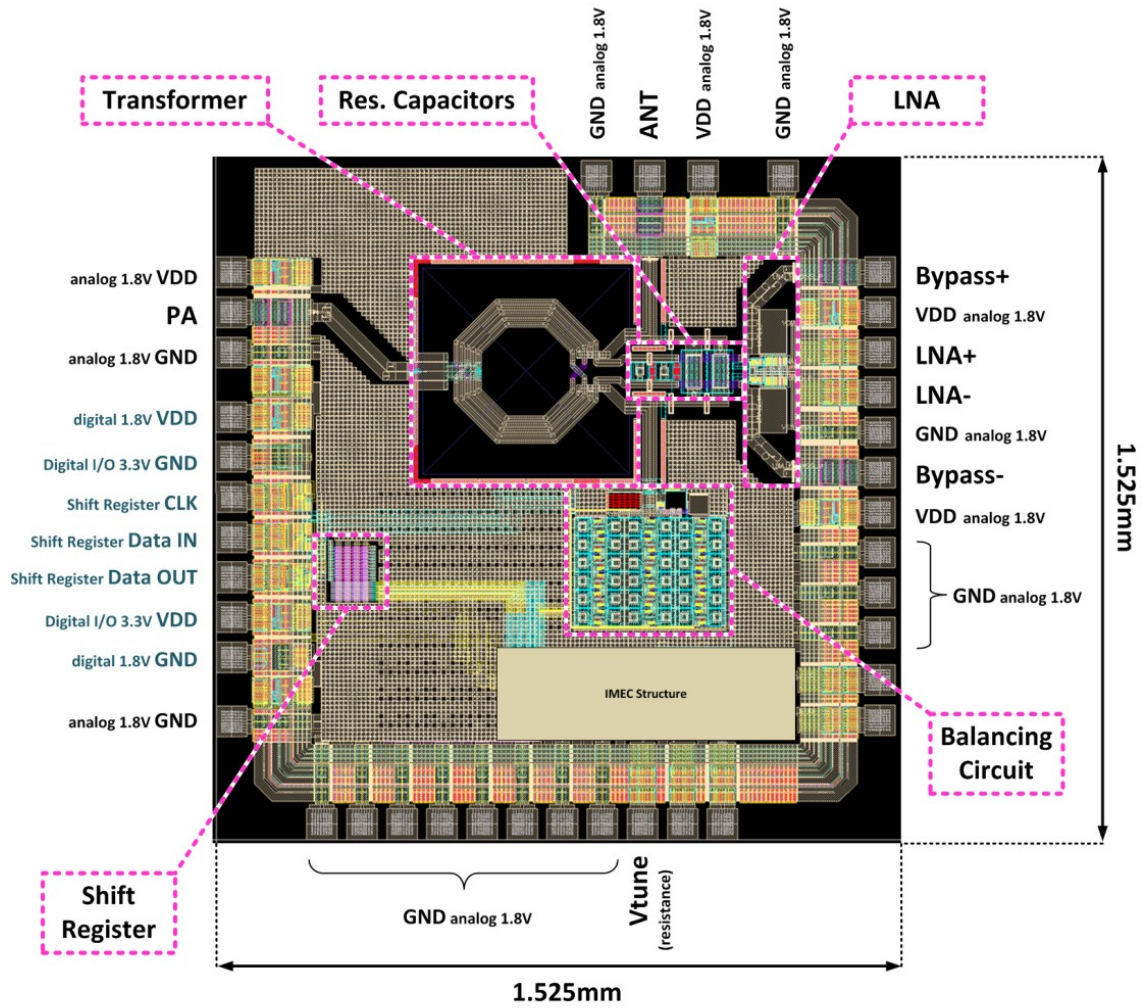


Figure 4.1 Layout of complete duplexer test chip

4.2 Hybrid Transformer

Figure 4.2, details the transformer, the resonant capacitors and the interconnect to the other circuit blocks. To absorb the capacitive parasitics due to the interconnect, the value of the resonant capacitors were reduced in value. The final value of the resonant

capacitor on the primary side is 4.35 pF, and on the secondary side it is 300 fF. The transformer is surrounded by a grounded ring that extends from the diffusion to the top metal in order to isolate it from the rest of the circuit. The secondary winding of the transformer connects to the LNA, and to bypass pads. Using these bypass pads the LNA can be bypassed allows circuit evaluation both with and without the LNA. The resistance of the connection between the centre tap of the secondary is kept below 1Ω , in order not degrade CM Tx isolation.

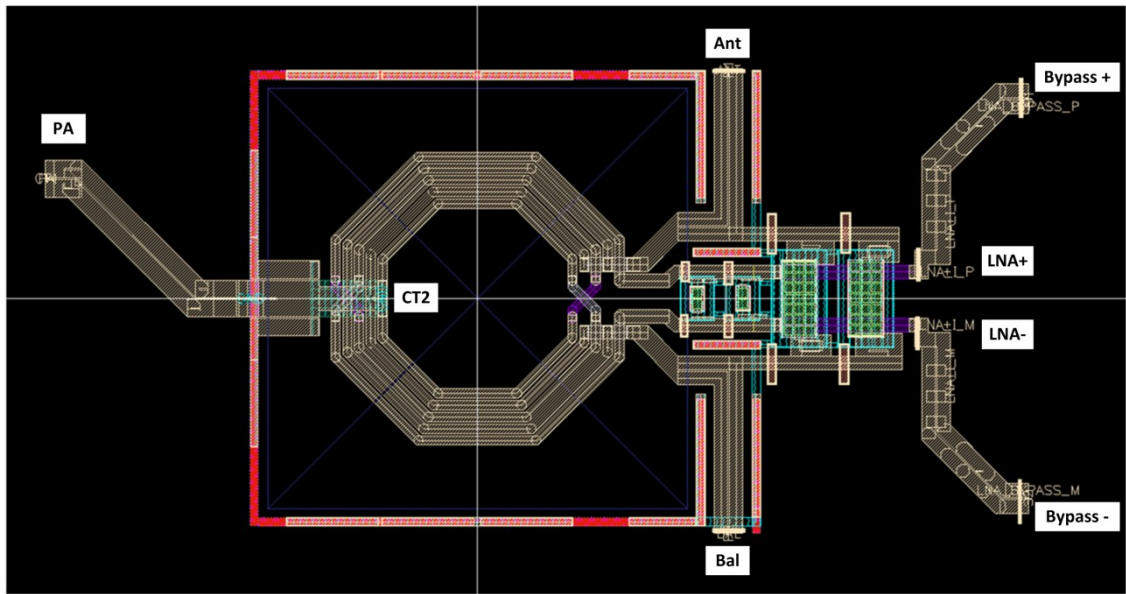


Figure 4.2 Transformer interconnects

4.3 Balancing Circuit

The layout of the balancing circuit is given in Figure 4.3. The locations of the three capacitor banks, the tuneable resistance, and the gate filter are indicated by dotted pink outlines. In order to keep the shift of the balancing region to a minimum, the inputs of the capacitor banks and tuneable resistance are placed close to the input terminal of the balancing circuit, and the connection between these circuits and the input is realised with two wide lines to reduce resistive and inductive parasitics. The remaining area is filled with decoupling capacitors. The area breakdown of the different sub-circuits is given in Table IX Area breakdown for the balancing circuit, and Figure 4.4 provides layout views of the top metal (a), components (b), and ground plane (c).

Table IX Area breakdown for the balancing circuit

Sub-circuit	Dimensions	Approx. Area
Coarse capacitor bank	$350\mu\text{m} \times 250\mu\text{m}$	0.088mm^2
Fine capacitor bank	$80\mu\text{m} \times 45\mu\text{m}$	0.004mm^2
MOS capacitor bank	$50\mu\text{m} \times 50\mu\text{m}$	0.003mm^2
Tuneable resistance	$35\mu\text{m} \times 20\mu\text{m}$	0.001mm^2
Gate Filter	$50\mu\text{m} \times 45\mu\text{m}$	0.003mm^2
	Total	0.115 mm^2

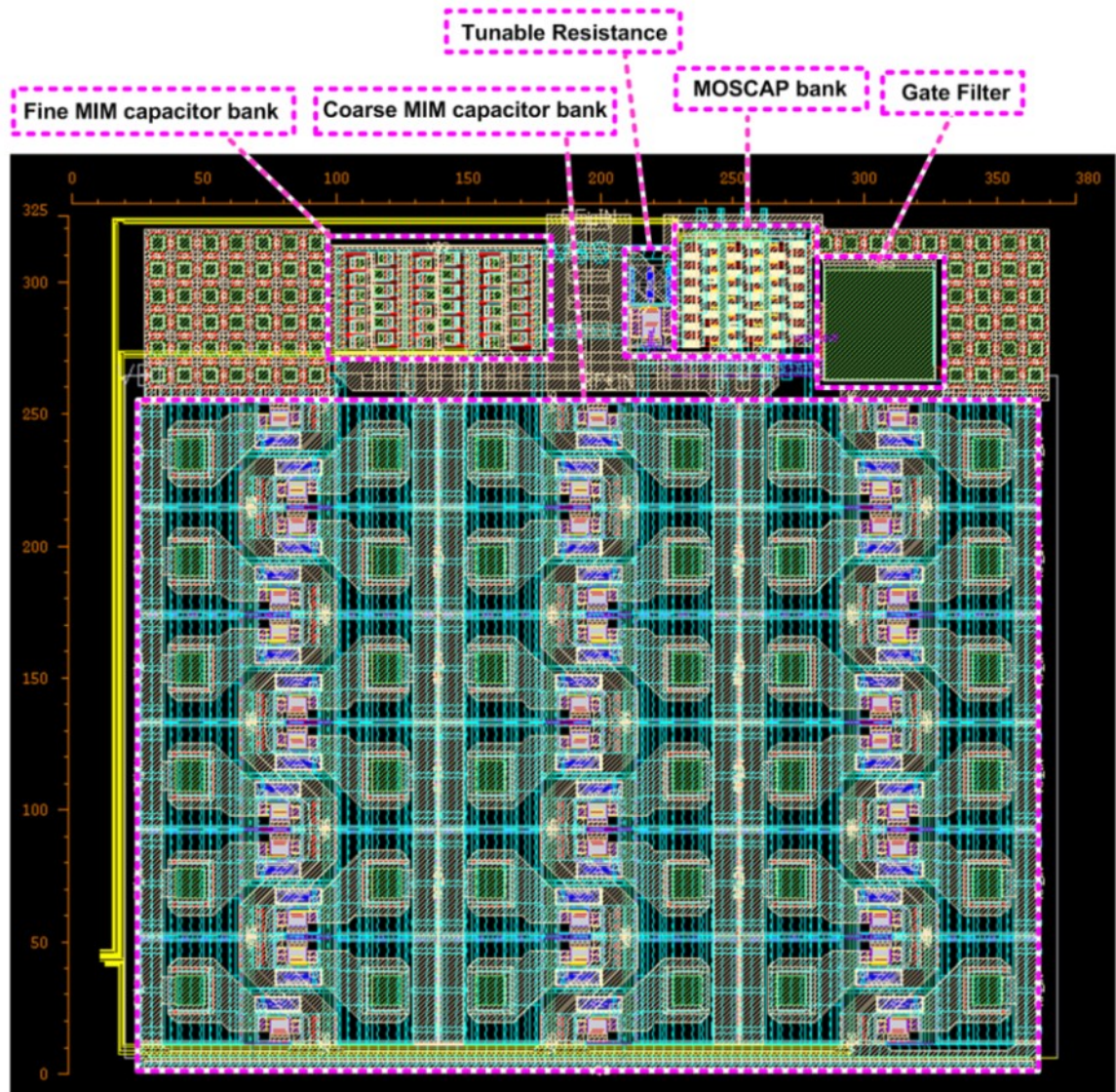


Figure 4.3 Layout balancing circuit

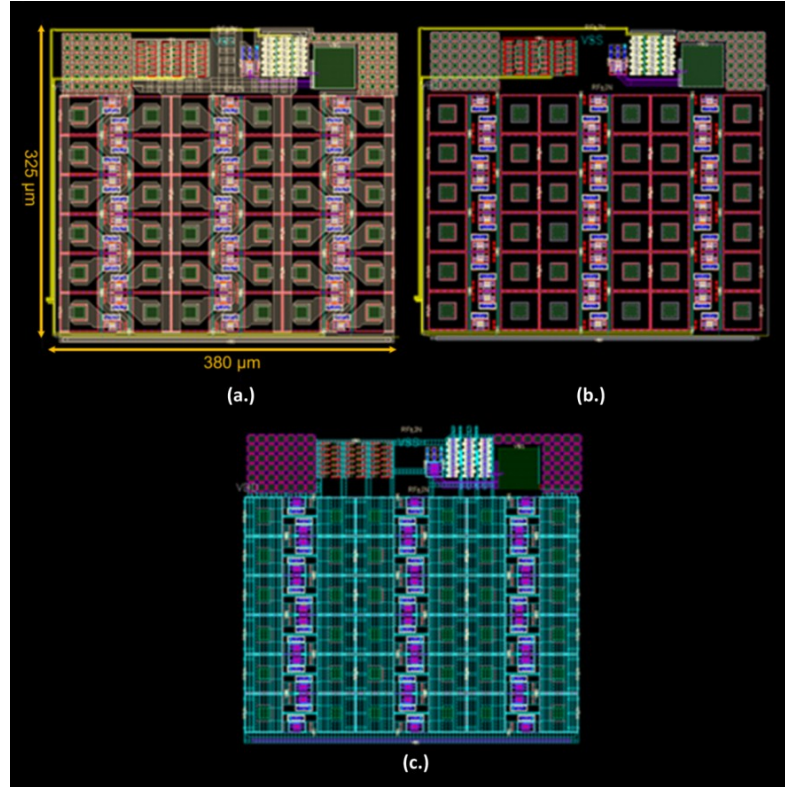


Figure 4.4 Balancing circuit (a.) top view (b.) control view (c.) bottom view

The balancing region provided by the balancing circuit is given later in section 4.6.6. The initial component values were changed after the layout was completed as parasitics caused a significant shift in the balancing region. By resizing the components to absorb the layout parasitics, the balancing region was placed around the expected antenna impedances with a comfortable margin. The effect of these layout parasitics will later be presented in the figures that accompany the individual sub-circuits of the balancing network.

4.4 Capacitor Banks

In the layout of the three banks of the tuneable capacitance, the main concern was to keep the off-state capacitance low, and to provide equal capacitance steps across the tuning range. To decrease any mismatch between the unit cells of each bank due to gradients across the die, and in order to average out parasitics effects of the interconnect, all banks were laid out using the common centroid geometry (CCG) shown in Figure 4.5. The numbers 1-to-4 in the squares indicate which bit of the 4-bit digital control word controls the particular unit cells. The CCG configuration was also lined by a dummy periphery (grey squares indicated with letter D) to provide each unit-cell with a similar environment in the surrounding layout, and reduce the systematic

mismatch between cells. Both techniques should lower differential nonlinearity across the tuning range. The drawback of this was the increase in area required, as each bank now consists of 30 unit cells of which only 15 cells are used.

D	D	D	D	D	D
D	4	4	3	4	D
D	3	2	1	4	D
D	4	D	2	3	D
D	4	3	4	4	D
D	D	D	D	D	D

Figure 4.5 Capacitor bank common centroid layout

4.4.1 Coarse Bank

The layout of the coarse MIM capacitor bank is presented in Figure 4.6. This bank constitutes 75% of the total area used for the balancing circuit. This significant area resulted from using the RF-MIM-capacitor and RF-NMOS library cells from the library that should be accurate at higher frequencies, to ensure that the fabricated bank would behave as simulated. However, due to their large physical size, lengthy interconnections are required to and from the bank. These interconnections introduce resistive parasitics which degrade the Q-factor of the bank. To counter these effects, wide lines were used in the both RF and ground paths. Corners in the layout were mitred where possible in order to limit the parasitic capacitance that these wide lines introduce.

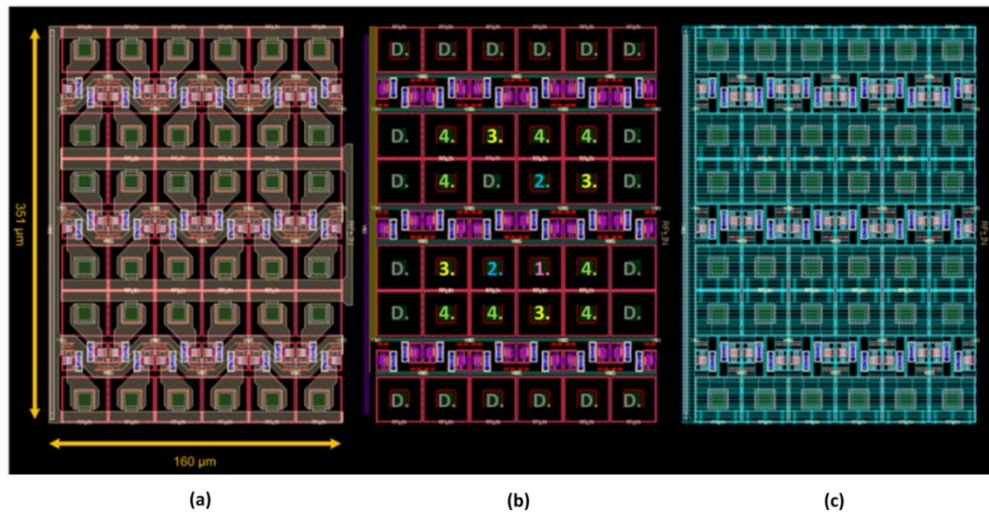


Figure 4.6 Coarse bank layout

(a) RF and ground connections (b) components and control lines (c) ground plane

Lengthy interconnections became a concern as these could introduce non-negligible inductive parasitics which are not considered by parasitic extraction (PEX) tools, but could affect frequency behaviour of the bank. The effect of parasitic inductance was estimated by simulating a bank in which 1 pH was added for each μm length of interconnect. The result of this simulation (blue), and the simulations before (green) and after PEX (red) are given in Figure 4.7. The upper left graph shows the capacitance value versus decimal control code. It can be observed that the tuning step is constant, and that parasitic extraction and the addition of inductive elements only affected the off-capacitance of the bank. The upper right graph shows that the equivalent parallel resistances of the bank is $560\ \Omega$, which does not degrade the resistive tuning range of the balancing circuit beyond the margin added in design (i.e., $R_{p,\text{total}} = 400\ \Omega$). The bottom two graphs show the capacitive and resistive values across frequency when all cells are ON. The behaviour of all three is similar, except for the bank with additional inductive parasitics where the effective capacitance increases with frequency.

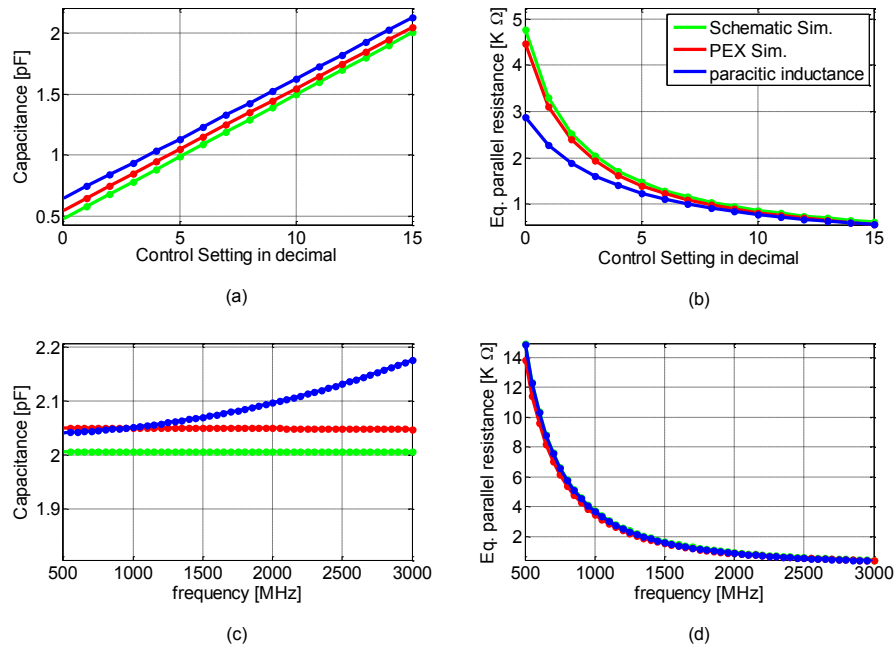


Figure 4.7 Pre- and post-layout behaviour of the coarse bank

(a) Capacitance vs. control setting (b) eq. parallel resistance vs. control setting
 (c) ON & OFF capacitance vs. frequency (d) ON & OFF eq. parallel resistance vs. frequency

The 100 fF bank consists of two switched capacitors, as the combination of the RF MIM capacitor and FET do not allow a single square unit cell, shown in Figure 4.8. The double unit cells is implemented so that all control lines, signal interconnects, and ground plane connect along the edge to adjacent placements. This double unit cell eases

bank layout, reduces systematic mismatch and decreases area. The pre- (green) and post layout (red) simulations are presented in Figure 4.9. Except for a 2 fF increase in C_{off} , the layout had little impact on the performance.

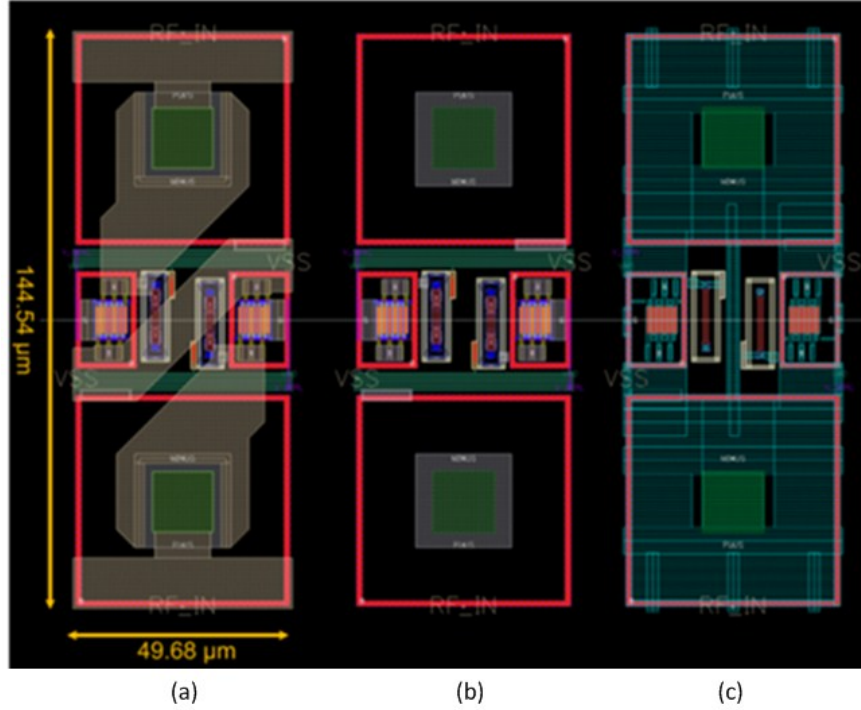


Figure 4.8 Double 100fF MIM capacitor unit cell

(a) RF and ground connections (b) components and control lines (c) ground plane

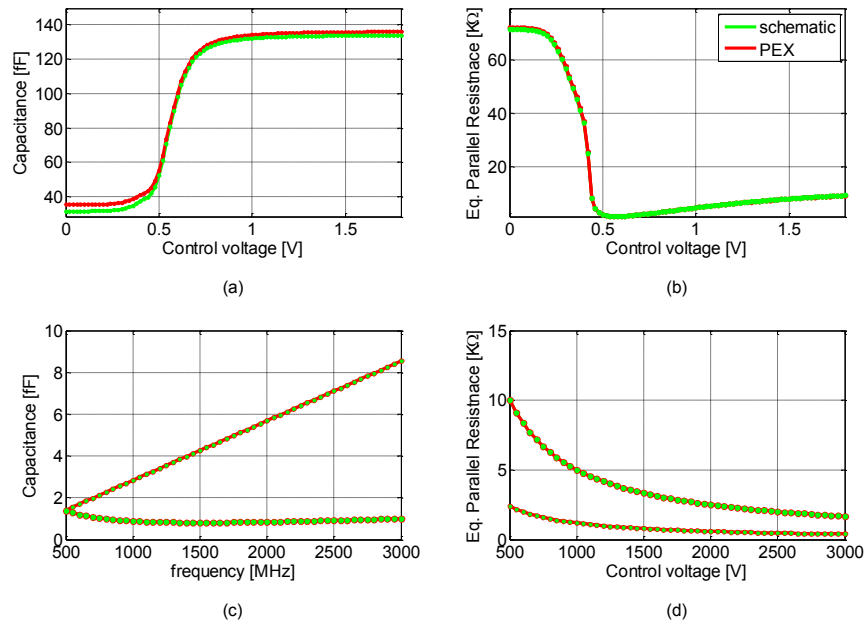


Figure 4.9 Pre- and post-layout behaviour of 100fF unit cell

(a) Capacitance vs. control voltage (b) eq. parallel resistance vs. control voltage
(c) ON & OFF capacitance vs. frequency (d) ON & OFF eq. parallel resistance vs. frequency

4.4.2 Fine MIM Bank

The layout of the 8.5 fF fine MIM capacitor bank is presented in Figure 4.10. It is again constructed using unit cells and follows the CCG layout with a dummy ring. As Mixed-mode MIM capacitor models were used, the area of this bank is 22 times smaller than the coarse MIM bank while the capacitive step is 11 times smaller. Also, no additional simulations were done to account for possible inductive parasitics as the interconnects are on the order of several μm in length.

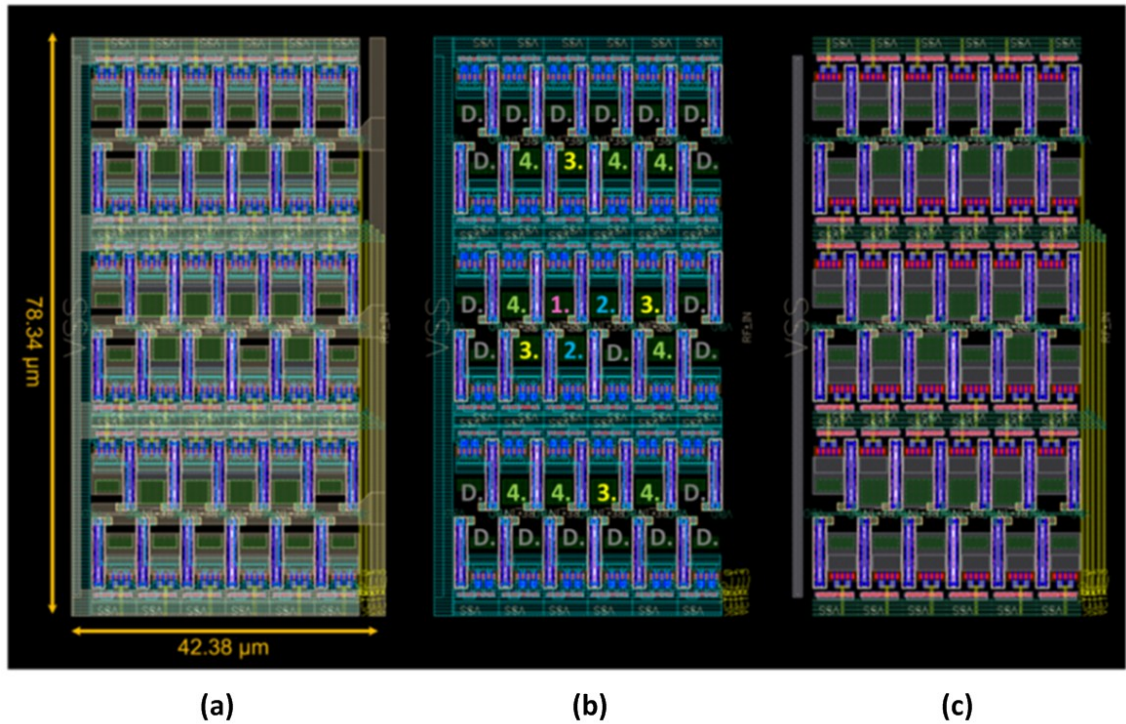


Figure 4.10 Fine MIM capacitor bank

(a) RF and ground connections (b) ground plane (c) components and control lines

A comparison of the performance before and after layout is given in Figure 4.11. Pre-layout is again given in green, while post-layout is given in red. As this bank provided much smaller capacitance values, the effect of layout is much more pronounced. This can be seen from by the 2.5x increase in the bank's off-capacitance (i.e., from 36 fF to 92 fF) in the upper left graph, and in the upper right graph where the eq. R_{parallel} suffers. However, all stayed within margin for the design as the Q of the bank is 25 which is higher than the desired value of 17.

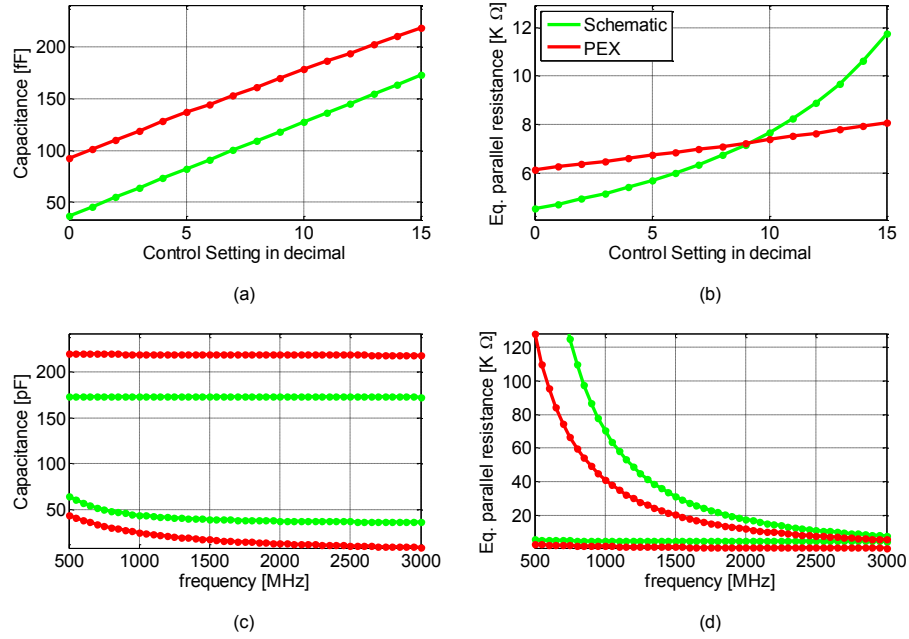


Figure 4.11 Pre- and post-layout behaviour of the 8.5 fF MIM bank

(a) Capacitance vs. control setting (b) eq. parallel resistance vs. control setting
(c) ON & OFF capacitance vs. frequency (d) ON & OFF eq. parallel resistance vs. frequency

Three different views of the 8.5fF unit cells are given in Figure 4.12. The left view shows the top metal which is used to prevent degradation of the Q-factor by providing a low ohmic connection to the RF signal and to ground. The middle view shows the control signals, and components, and the right view shows how the first metal layer provides wide connections to and from the source of the transistor to ground.

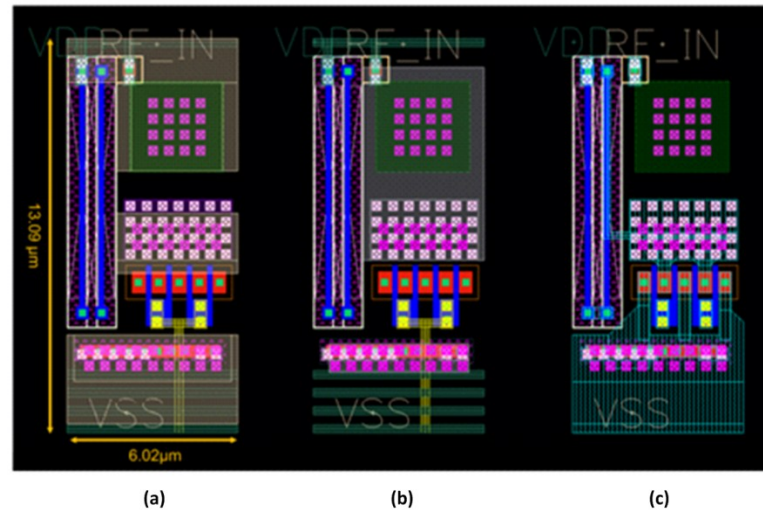


Figure 4.12 8.5fF MIM capacitor unit cell

(a) RF and ground connections (b) components and control lines (c) bottom metal to ground

Pre- (green) and post-layout (red) simulations of this unit cell are shown in Figure 4.13. Again the upper left graph shows that the off-capacitance has increased with layout. This cell required an extra iteration to find the right component values that would absorb layout parasitics and provide the desired tuning step.

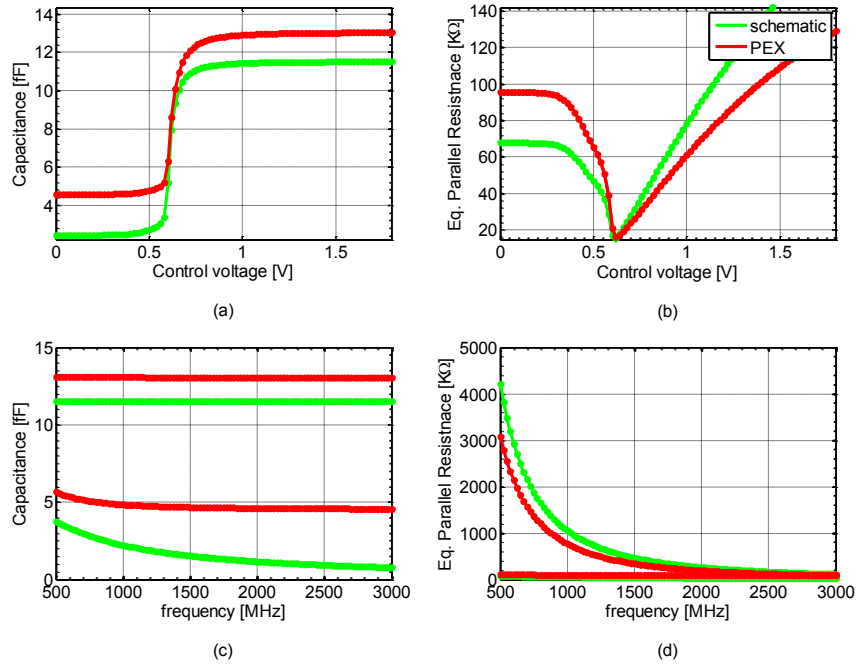


Figure 4.13 Pre- and post-layout behaviour of the 8.5fF unit cell

(a) Capacitance vs. control voltage (b) eq. parallel resistance vs. control voltage

(c) ON & OFF capacitance vs. frequency (d) ON & OFF eq. parallel resistance vs. frequency

4.4.3 MOS Varactor Bank

The MOS varactor bank is presented in Figure 4.14, where again the top view (left), component view (middle), and bottom metal views are given. This bank also follows the CCG layout style described previously and includes a dummy ring. Bank performance is given in Figure 4.16, where again the main difference between pre- and post-layout simulations is the off capacitance. The increase is more pronounced as the varactor bank provides smaller capacitance values.

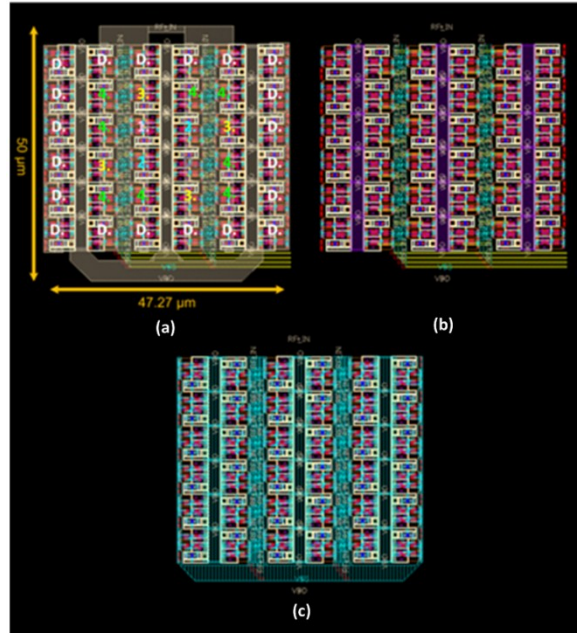


Figure 4.14 Layout MOS varactor bank

(a) RF and ground connections (b) components and control lines (c) ground plane

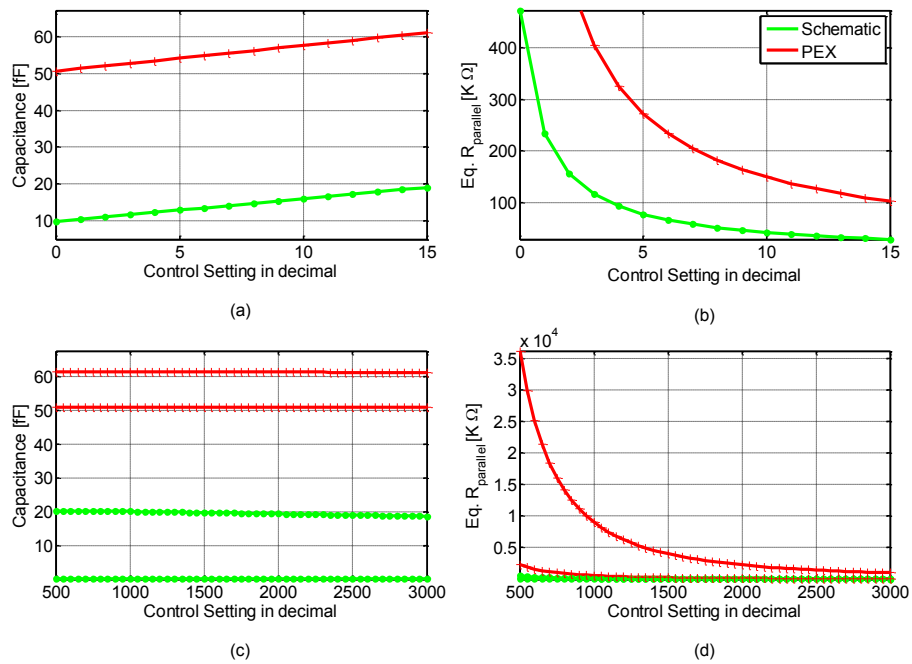


Figure 4.15 Pre- and post-layout behaviour for the MOS varactor bank

(a) Capacitance vs. control setting (b) eq. parallel resistance vs. control setting

(c) ON & OFF capacitance vs. frequency (d) ON & OFF eq. parallel resistance vs. frequency

The layout of the MOS varactor unit cell is given in Figure 4.16. The left view shows how the top metal is used to provide low ohmic connections to the RF signal and ground. The middle view shows the two inverters, the MOS varactor, and the control lines. The right view shows the lower metal layer, and how it provides a short and wide

path through the one inverter to VDD in order to prevent degradation of the unit cell Q-factor. This figure also shows that the small varactor has a significant area overhead to control and connect it.

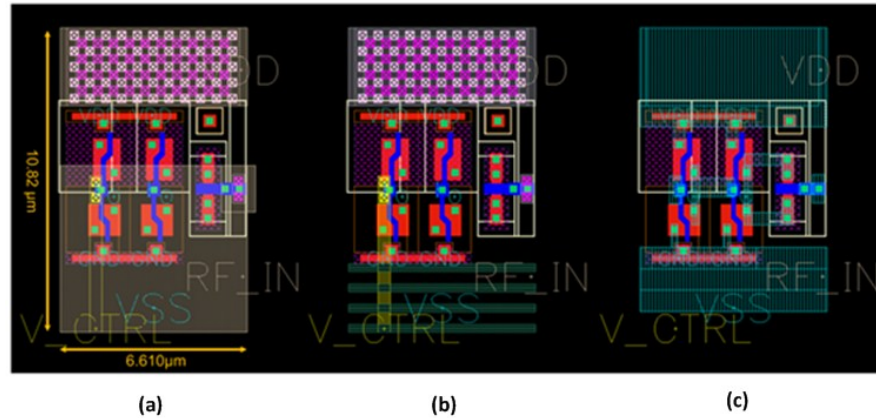


Figure 4.16 Layout for the MOS varactor 0.7fF unit cell

(a) RF and ground connections (b) components and control lines (c) ground plane

The performance of the cell is given in Figure 4.17, where again only the off-capacitance shows a significant difference as it changes from 0.4 fF to 2.3 fF (a 5.7x increase). However as the capacitance these cells provide is so small this hardly affects balancing circuit performance.

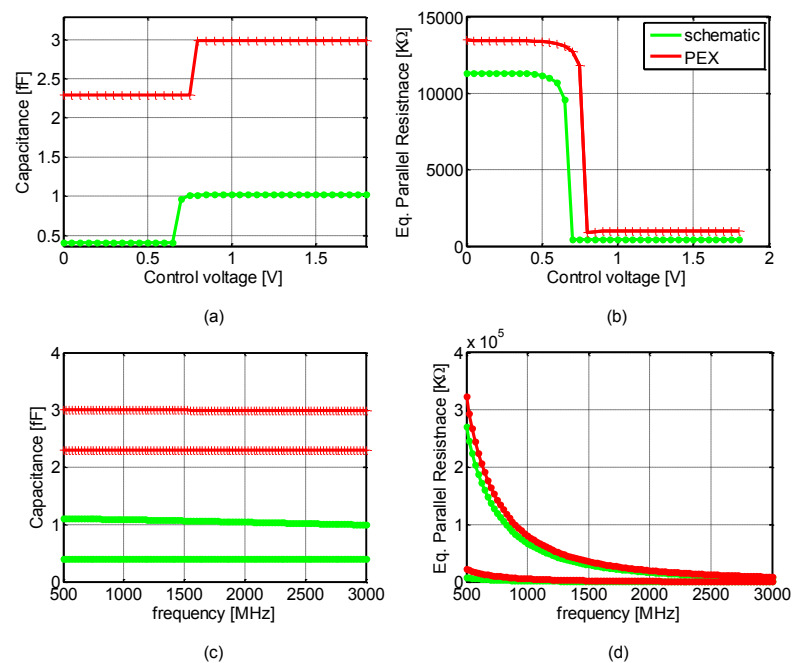


Figure 4.17 Pre- and post-layout behaviour of the 700aF unit cell

(a) Capacitance vs. control voltage (b) eq. parallel resistance vs. control voltage
(c) ON & OFF capacitance vs. frequency (d) ON & OFF eq. parallel resistance vs. frequency

4.5 Tuneable Resistance

The layout of the tuneable resistor is given in Figure 4.18. The left view shows the top metal, and the right view shows the two resistors and the transistor used to implement the circuit. Top metal connections are used to keep parasitic resistances small and 45° mitring of corners in the routing were used to keep parasitic capacitance of the interconnect to a minimum.

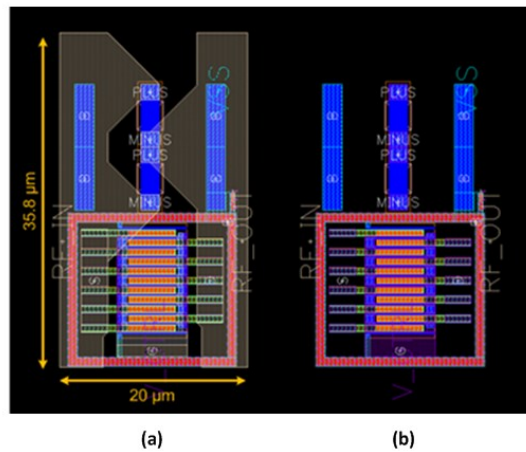


Figure 4.18 Layout tuneable resistance (a) RF and ground connections (b) components

4.5.1 Gate Filter

The gate filter was added quite late in the design, as it was inserted after concerns were raised about the effect of noise and interference on the stability of the tuning resistance. As most of the balancing circuit was already set, the filter could not be placed adjacent to tuneable resistance where it would provide the best performance. To minimize the parasitic resistance to the filter, efforts were taken to keep the interconnect parasitic at a minimum by making the connection wide and using large numbers of vias (total introduced resistance less than $2\ \Omega$). The 1.7 pF capacitance in shunt and 400 Ω in series give the filter low-pass cut-off frequency of 230 MHz.

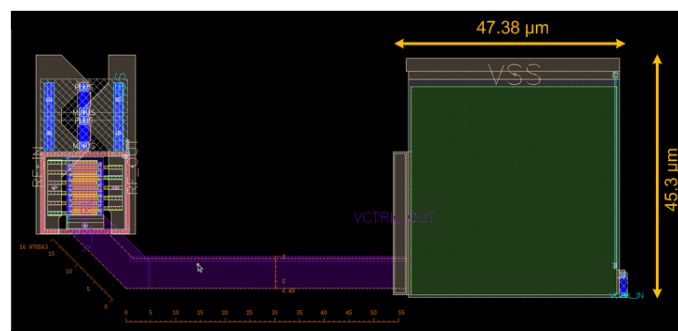


Figure 4.19 Layout gate filter and interconnect to tuneable resistance

4.6 Duplexer Performance

In this section the performance simulation of the complete duplexer circuit are presented. All simulation are done after PEX unless stated otherwise.

4.6.1 Reflection Coefficients

The simulated post-layout reflection coefficients at all ports are at or below -10 dB at 2.45 GHz. This simulation was done using ideal terminations at the Tx, Ant, and Bal ports, while adding the input impedance of the LNA at the Rx port. The Duplexer was simulated with the with the s-parameters extracted from EMX.

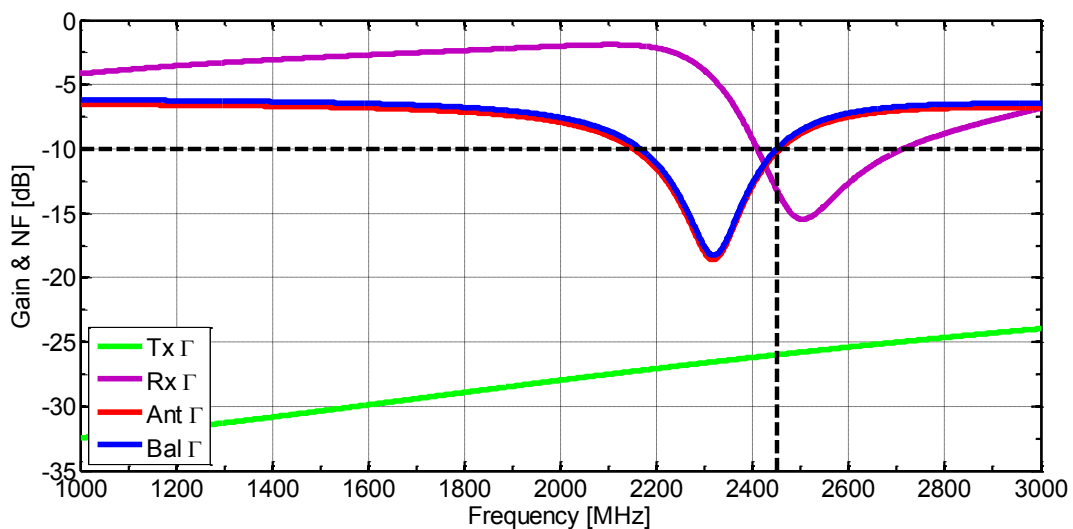


Figure 4.20 Simulated reflection coefficient using ideal terminations

4.6.2 Insertion Losses

The Tx-insertion losses at 2.45 GHz after layout is 3.22 dB and the Rx insertion loss is -10.61 dB, The Tx insertion losses are very good compared to other integrated duplexer implementations, the Rx insertion losses are however significant. The imbalance between both insertion losses is out of balance resulted from inaccurate modelling of the transformer behaviour during the design stage. This left the primary winding of the transformer with inadequate self-inductance to provide the desired frequency behaviour in the lower frequency range.

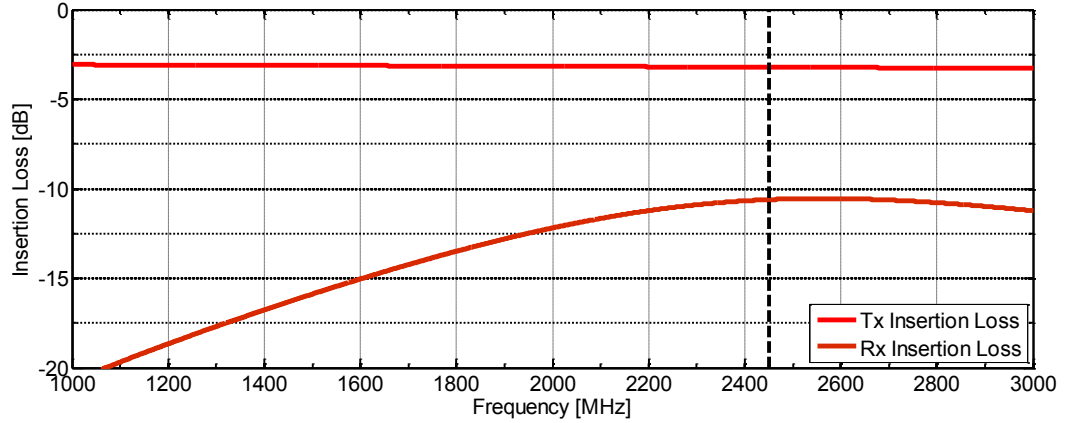


Figure 4.21 Simulated Tx and Rx insertion losses

4.6.3 Gain and NF

The duplexer/LNA cascade has a gain of 9.25 dB and a NF of 9.1 dB at 2.45 GHz. Note that the peak gain is located at 2.3 GHz, and not at 2.45 GHz as desired. The value of the shunt capacitors C_{res1} and C_{res2} (Figure 3.34) used to resonate the transformer is therefore chosen too large. A follow-up prototype should be fitted with a smaller value and should also be margined against processing variations. The simulated NF consumes the entire budget allocate to the receiver, and is therefore far too high for a practical application. The insertion losses in the Tx and Rx paths should be modified to reduce the receiver NF, this action will increase Tx insertion loss, but a ± 1 dB additional loss for the TX could be traded more than ~ 3 dB improvement for the Rx (Figure 2.8).

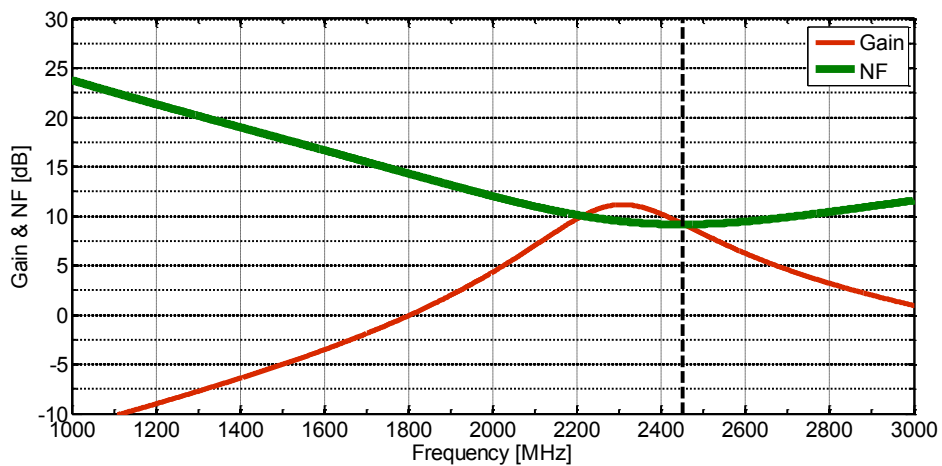


Figure 4.22 Simulated gain and noise figure ($Z_{ant} = 50 \Omega$)

4.6.4 Common-mode Tx isolation

The simulated common-mode Tx isolation before (green) and after (red) layout are given in Figure 4.23. The figure shows that both provide around 20 dB isolation at 2.45 GHz. This is short of the desired goal of 30 dB. The CM Tx isolation depends of a low ohmic connection of the secondary centre tap of the transformer and the symmetry of the transformer. As the centre tap was provided with a low resistive connection to ground, the CM- Tx isolation can be improved by better symmetry in the transformer. The main source of the asymmetry are the crossover section of the transformer, these could be improved using the symmetrical crossover structure presented in [47].

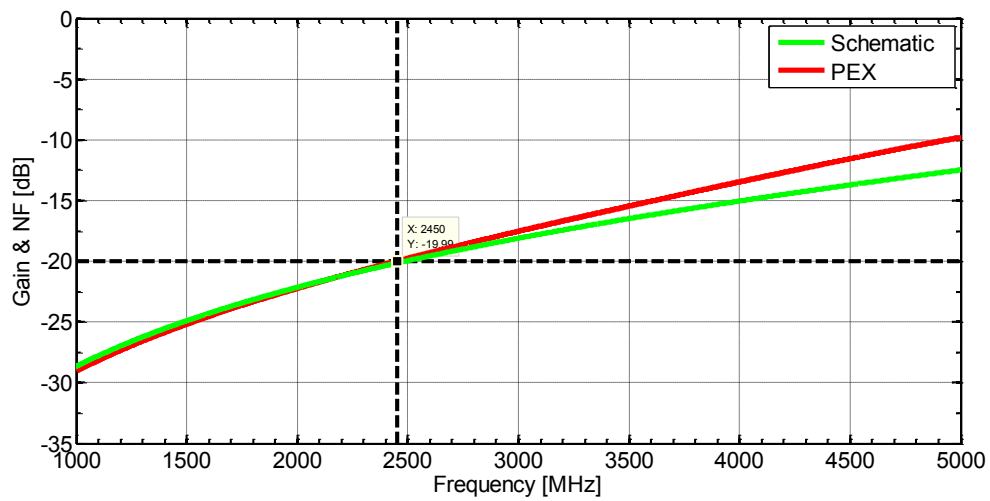


Figure 4.23 Pre- and post-layout CM Tx Isolation

4.6.5 Balancing Circuit

The complete tuning range of the capacitor bank versus the binary control code (in decimal) is plotted in Figure 4.24. One zig-zag cycle comes from the 20 % overlap of smaller banks. A small zoom-in is provided to show that the MOS varactor bank also has sufficient overlap.

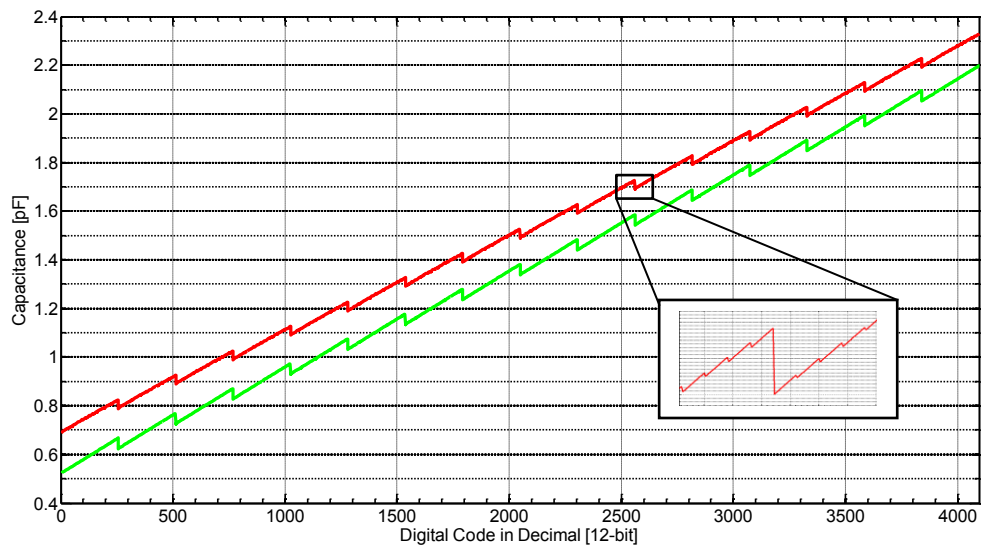


Figure 4.24 Tuning capacitor range

The tuning range of the tuneable resistance is given in Figure 4.25. It shows that the resistive tuning range goes from 10 Ω to 100 Ω . However, the tuning range provided is non-linear and a large part of the range is situated in a narrow voltage interval.

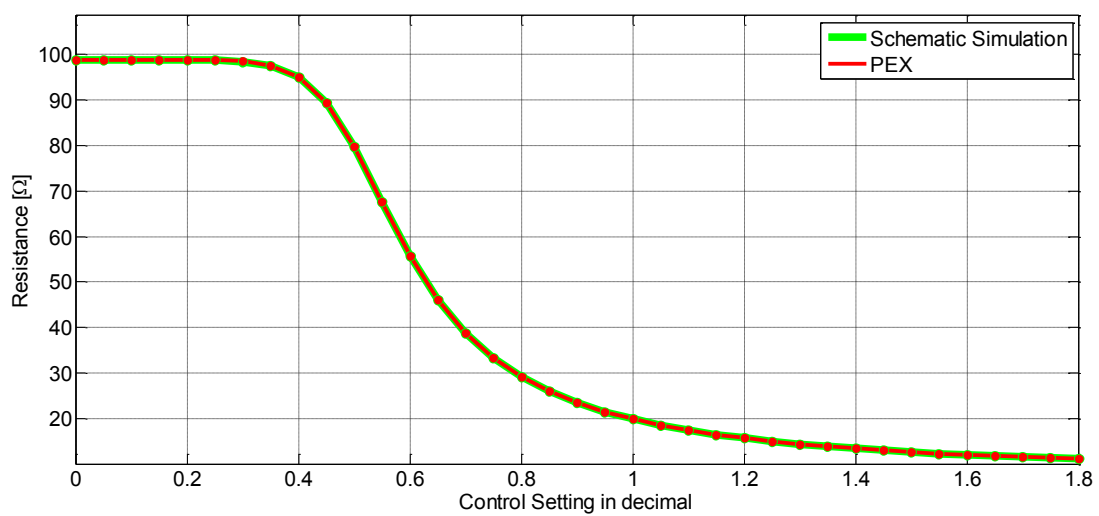


Figure 4.25 Resistance versus control voltage tuneable resistor at 2,45GHz

4.6.6 Balancing Region

A comparison of the balancing region before and after layout is given in Figure 4.26. In the figure, the measured antenna impedances are plotted using the black dots. However, the antenna impedance is located in the balancing region with a margin 300 fF on all sides as can be seen from the simulations (green in the figure) after parasitic extraction. This simulation does not take into account the parasitic inductances introduced by the long interconnection required to realise the coarse MIM capacitor bank. Simulation of the coarse bank with a model for the interconnect parasitics showed an addition of 100fF of the balance region. As there is around 600fF margin on that side no further precautions were taken.

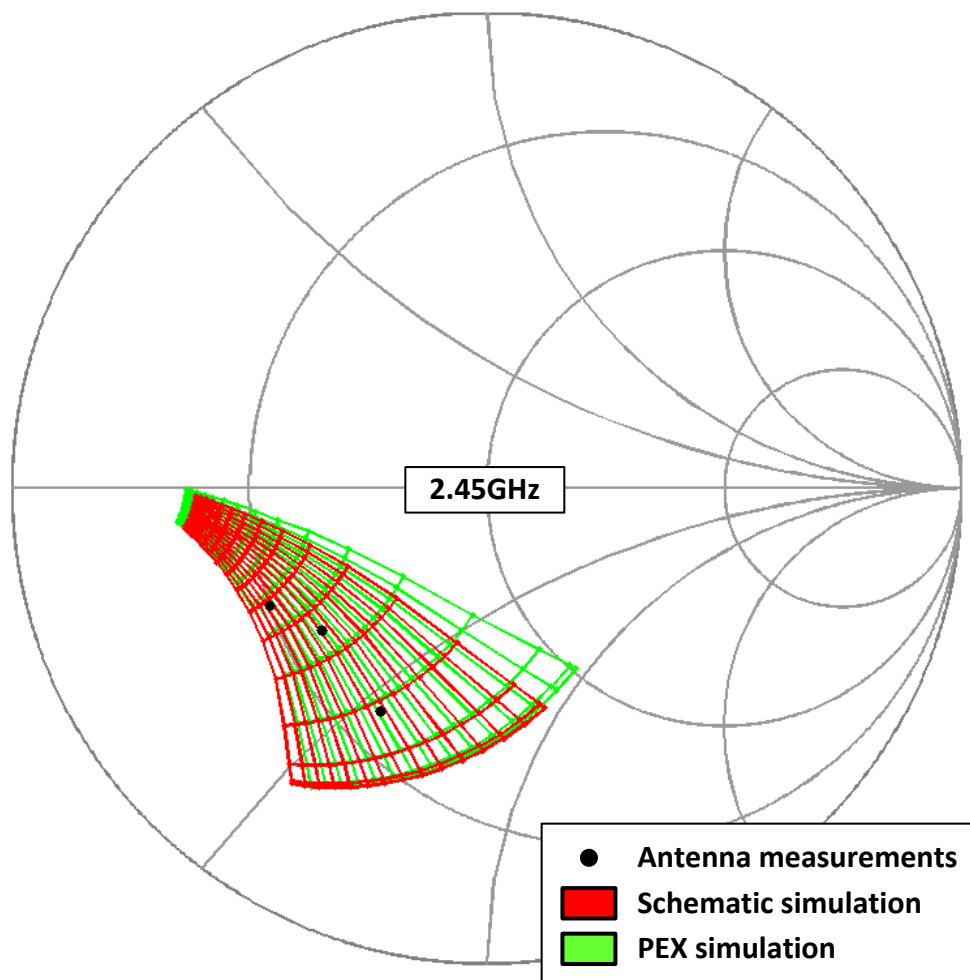


Figure 4.26 Simulated balancing area after layout

4.6.7 Isolation

The isolation across frequency for the pre- and post-layout designs at the bypass and the LNA are given in Figure 4.27. The simulation are limited by the resolution of the antenna measurements, which were taken with a 10 MHz frequency step. This is the reason why the zoom-in shows few points near the peak isolation. The settings that correspond to these isolation curves are given in Table X. At the bypass ports and the LNA out 2 MHz isolation bandwidth is found at 60 dB and 40 dB isolation, respectively.

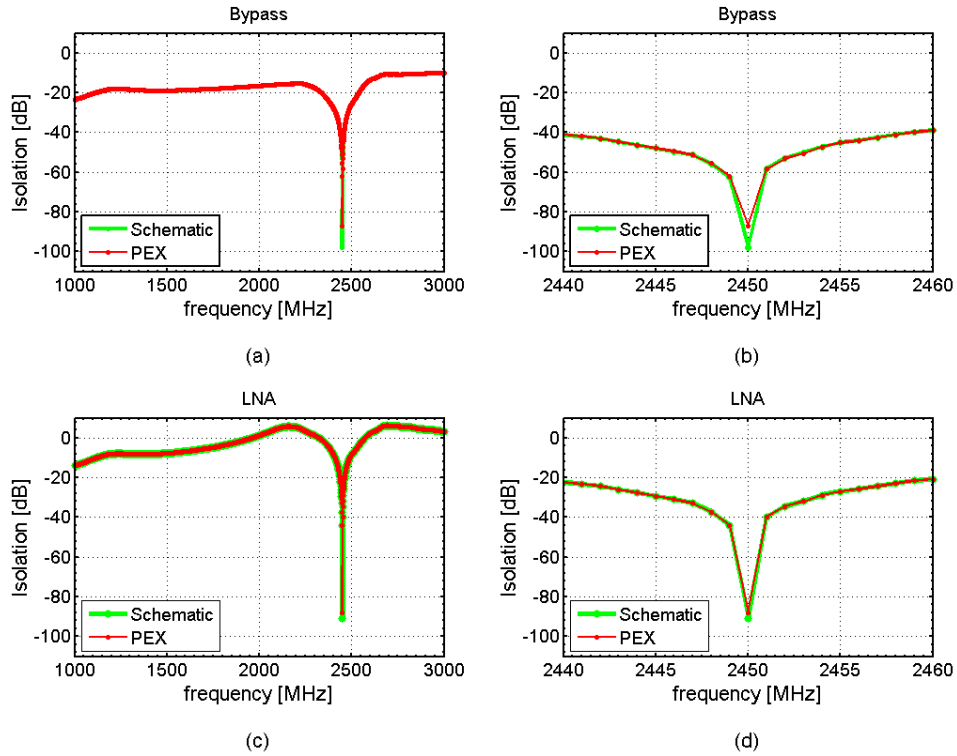


Figure 4.27 Isolation characteristic across frequency

- (a) simulated isolation at bypass ports vs. frequency (b) zoom-in Figure 4.27a around 2.45 GHz
(c) simulated isolation at LNA ports vs. frequency (d) zoom-in Figure 4.27c around 2.45 GHz

Table X Balancing circuit settings used to obtain curves of Figure 4.27

Bypass output	CC	FC	MOSC	Vctrl. Res.
Schematic	3	11	2	786.2 mV
PEX	2	6	2	797.4 mV

LNA output	Coff	Con	ΔC	Vctrl. Res.
Schematic	3	11	2	786.7 mV
PEX	2	6	2	797.9 mV

4.6.8 Aggregated Bandwidth

The aggregated bandwidth of the duplexer is presented in Figure 4.28. The figure is obtained by finding the tuning setting of the balancing circuit that provides high peak isolation at frequencies spaced 10 MHz apart. The aggregated bandwidth around 2.45 GHz that provided 50 dB isolation is 100 MHz, and ranges from 2.41 GHz to 2.52 GHz. The additional bandwidth provided around 2.34 GHz can be explained using Figure 4.29, in which both the frequency behaviour of the antenna and the schematic balancing circuit is presented. It can be seen that the antenna and balancing regions coincide twice across frequency.

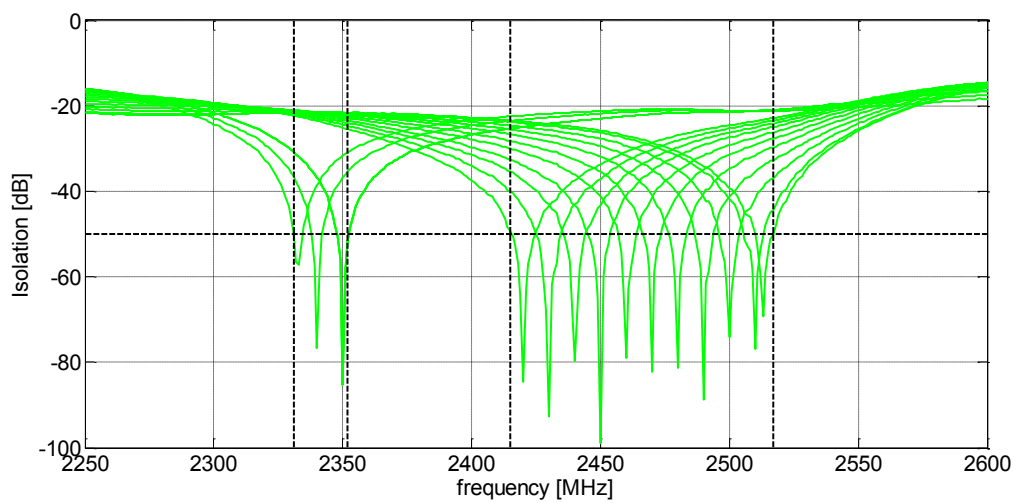


Figure 4.28 Aggregated bandwidth

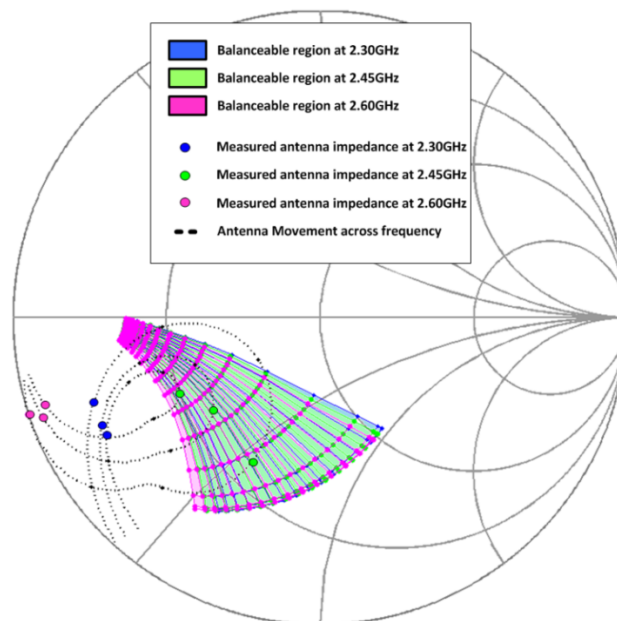


Figure 4.29 Antenna & balancing region shift with frequency

4.6.9 Simulation Conclusions

The reflection coefficients at all four port are around -10 dB. The IL_{Tx} is 3.5 dB which is very good for an un-skewed hybrid transformer (ideal 3dB). However the price for the low IL_{Tx} is a IL_{Rx} of 10.61 dB. This results in NF of 9.1 dB, which uses the entire noise budget of the receiver. The Gain of the duplexer LNA cascade is 9.61 and the CM- Tx isolation is 20 dB, this is lower 10 dB lower than the goal, but as the goal was set arbitrarily and this is mostly due to the asymmetry of the transformer not much could have been done to improve this.

The balancing region of the prototype covers the antenna impedance with margin and the peak isolations of 90 dB are found within this region. The aggregated bandwidth of the balancing circuit around 2.45 GHz is 100 MHz for 50 dB isolation. The remaining problem of the isolation characteristics is the isolation bandwidth, which is 2 MHz for 60 dB isolation at the bypass ports and 40 dB isolation at the LNA output. The main cause for this is the frequency behaviour of the antenna, as the impedance presented by this device has a large frequency dependence and the RC network in the balancing circuit is not able to track it.

Chapter 5

Experimental Results

This chapter presents the results of the experimental measurements on the fabricated prototype. It starts by showing the fabricated chip and the printed circuit boards (PCBs) used during the measurements and then proceeds with measurements. Each measurement is accompanied by its measurement setup, the measurement plan and a summary of the results.

5.1 Fabricated Prototype

The micrograph of the fabricated duplexer is presented in Figure 5.1. The sub-blocks are outlined with the pink lines. The analog pads are denoted in black and the digital pads in blue.

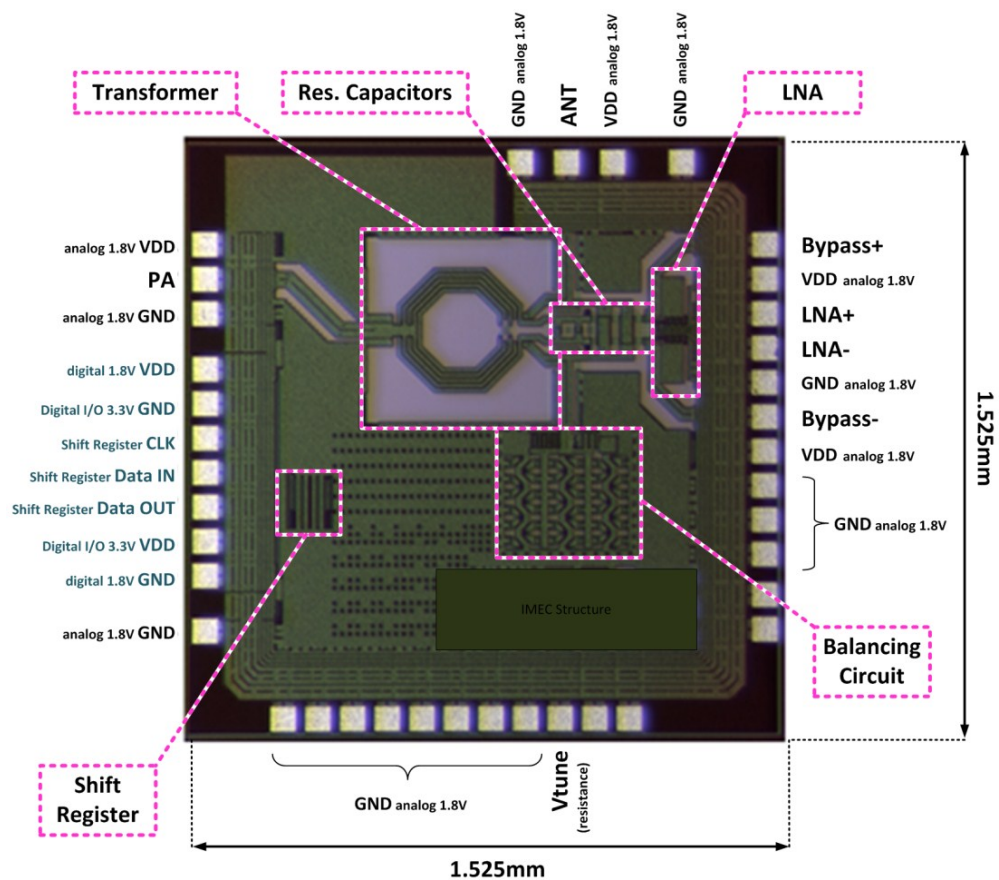


Figure 5.1 Prototype Micrograph

5.2 The Printed Circuit Boards

The fabricated chips are mounted on two different PCBs. The mounted IC is depicted in Figure 5.2 and a picture of the two PCBs is shown in Figure 5.3. The difference between the two is that PCB-2 has an additional network between the antenna port of the DUT and the antenna port of the PCB required to match with $50\ \Omega$ measurement equipment, while PCB-1 does not.

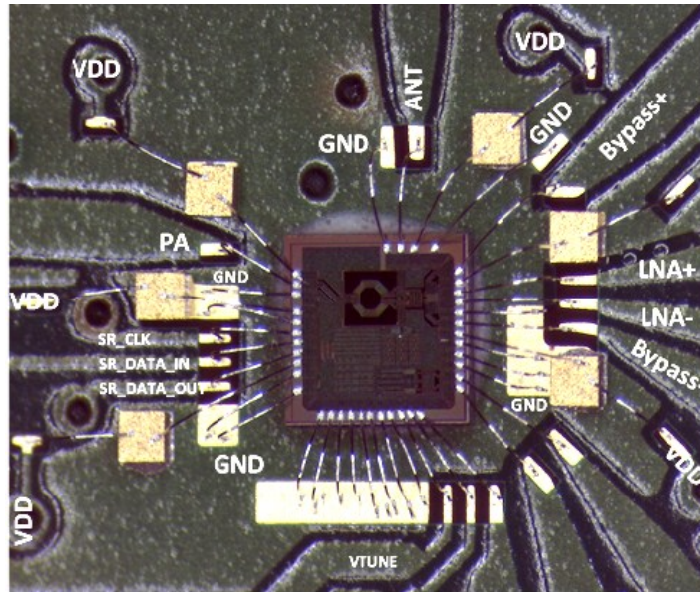


Figure 5.2 The interconnection between chip and PCB

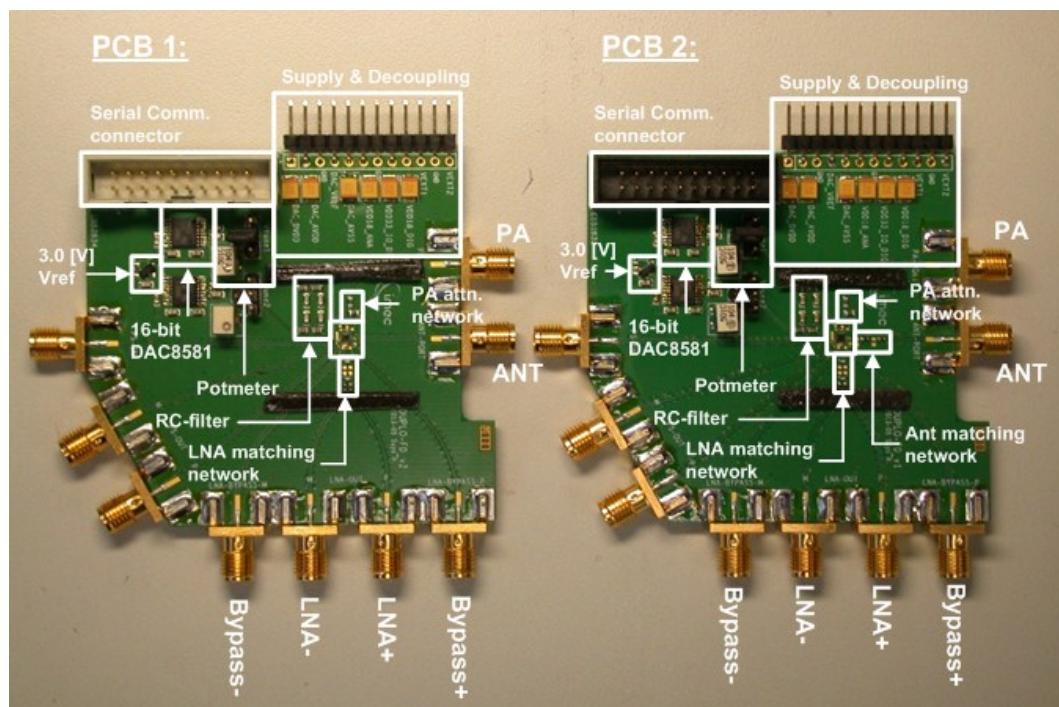


Figure 5.3 - Test PCB-1 for antenna & Test PCB-2 for 50Ohm

5.2.1 PCB functionality

Except for the addition (or omission) of a matching network at the antenna port, both PCBs have the following functionality: a digital-to-analog converter (DAC) to control the tuneable resistance, a serial connection to program the shift registers controlling the capacitor bank, an off-chip DAC, a reference voltage for the DAC, a potentiometer to allow manual tuning of the control voltage that sets the resistive part of the balancing network, an RC-filter at the input of the tuneable resistance, a resistive matching network to match the 50Ω of the signal generator to the PA port of the duplexer, and a matching network to the LNA.

5.3 Experimental Measurements

The measurements begin with an isolation measurement with the PIFA antenna. This is followed with the isolation bandwidth measurement and then the characterization of the balancing region.

5.3.1 Isolation with PIFA Antenna

The initial measurements investigate the duplexer's capability to provide a balanced condition with the PIFA. The measurement setup is illustrated in Figure 5.4. The antenna is connected to the Ant port of the PCB, and a vector network analyser (VNA) is connected to the Tx and bypass ports using a hybrid coupler in order to measure the Tx-to-Rx isolation through the duplexer.

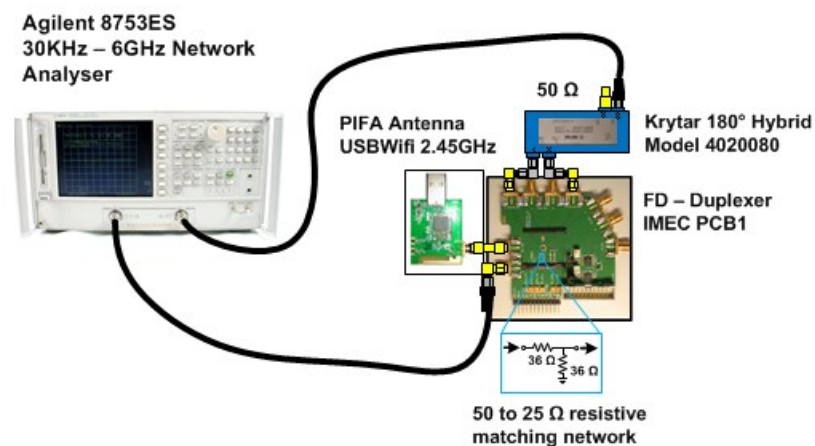


Figure 5.4 Isolation measurement setup

The isolation curves obtained are presented in Figure 5.5. The high peaks isolations at 2476 MHz were found using the potentiometer to tune the on-chip resistance and iteration with the capacitor banks. Such a deep peak could not be found easily at 2450 MHz, which indicates that the balancing region is located very close to the antenna impedance, but does not cover antenna impedance at 2.45 GHz.

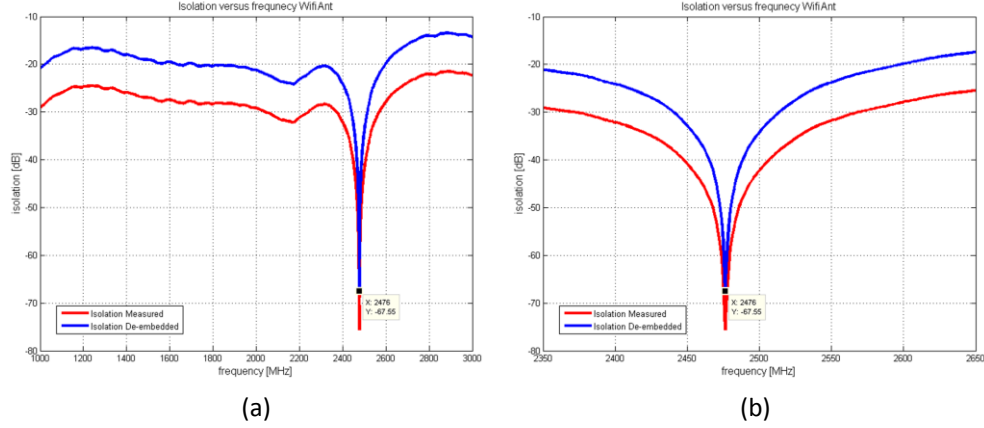


Figure 5.5 Measured Isolation PCB-1 (a) from 1 GHz to 3 GHz (b) Zoom in at 2.47 GHz

5.3.2 Isolation Bandwidth

To characterize the isolation bandwidth, the setup presented in Figure 5.6 was used. In this particular measurement, PCB-2 was used as it allows a comparison of the isolation characteristic with the antenna, and with a broadband $50\ \Omega$ load. PCB-2 is connected to either the antenna or the $50\ \Omega$ termination. The network vector analyser is connected to the PA port and the bypass ports of the PCB, and the setting of the balancing circuit is changed until high isolation is found. As the isolation characteristic has a global minimum, high isolation indicates that the balanced condition is obtained with that particular setting.

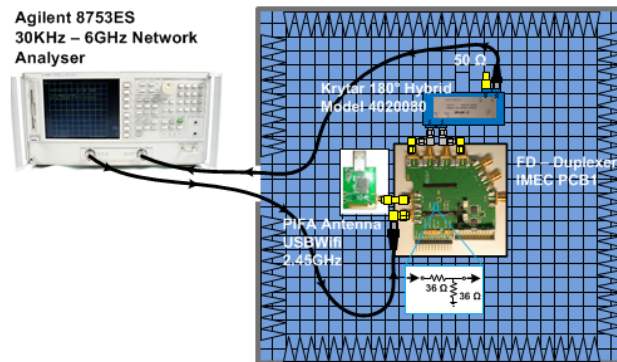


Figure 5.6 Isolation measurement setup

As the balancing circuit has 2^{24} settings, it takes a considerable amount of time to find the ideal setting for isolation by cycling through all possible settings in sequence. Therefore a search algorithm was devised that converges to the ideal tuning setting. The search grid and the isolation measurements taken as the algorithm converged are presented in Figure 5.7. The algorithm starts with an initial 25 setting grid that spans the entire tuning range. After these 25 points are measured, a new grid is calculated around the four points that gave to lowest average isolation. The search then continues until converges to the setting that provides the high isolation.

Four iterations are shown in Figure 5.7a. The first iteration spans the complete tuning space, and the following iterations cover ever-smaller sub-regions, illustrated in the figure by coloured squares (pink, green, yellow). Figure 5.7b shows the measured isolation at each setting, and how the algorithm converges to a setting that provides high isolation. The algorithm converged to 90 dB isolation in 6 iterations and took 150 measurements.

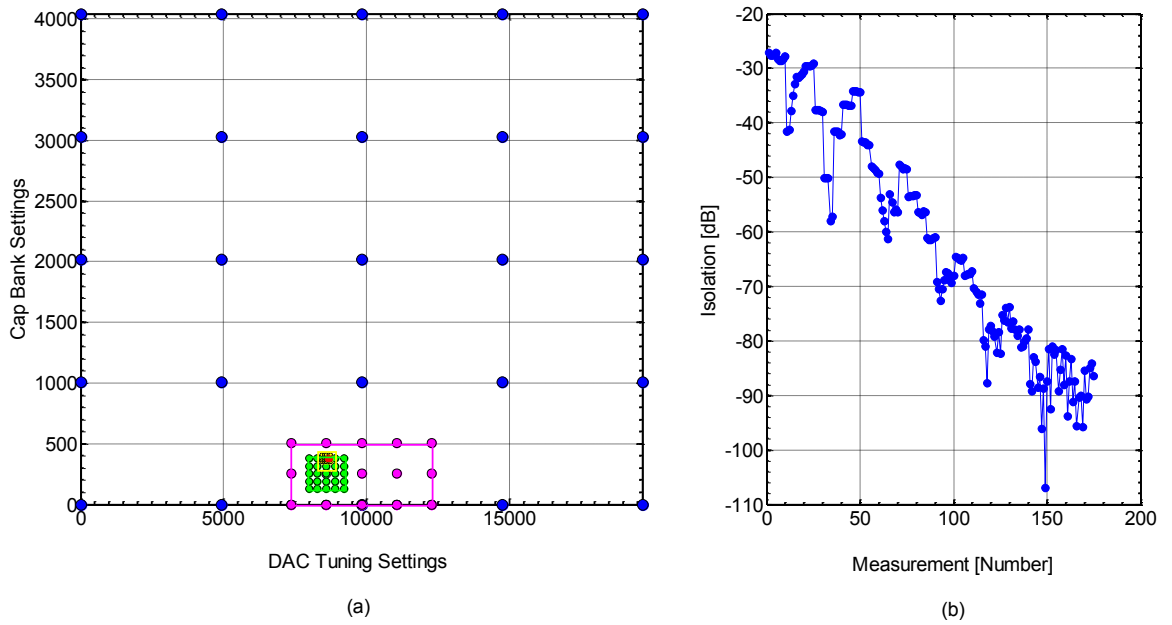


Figure 5.7 Convergence of the tuning algorithm

The settings that provide a balanced condition with a $50\ \Omega$ termination and the antenna are given in Figure 5.8, along with their corresponding isolation curve. The results show a high peak isolation for both, but the isolation bandwidth is significantly lower with the antenna lower than the bandwidth obtained using the $50\ \Omega$ termination.

The difference in isolation bandwidth is explained by the fact that both the balancing circuit and the broadband $50\ \Omega$ have consistent impedance values across frequency with

very little change, while the antenna impedance differs significantly with frequency. Therefore the absolute difference between the balancing circuit and a $50\ \Omega$ reference changes less across frequency compared to the absolute difference between antenna impedance and the balancing circuit across frequency.

The measured isolation bandwidth plotted on both linear and log scales for the antenna and the broadband $50\ \Omega$ against measured isolation are shown in Figure 5.9. From this graph it can be seen that the antenna is only able to provide 45 dB isolation for the desired 10 MHz isolation bandwidth, while the broadband $50\ \Omega$ load, provides 65 dB isolation for the same bandwidth.

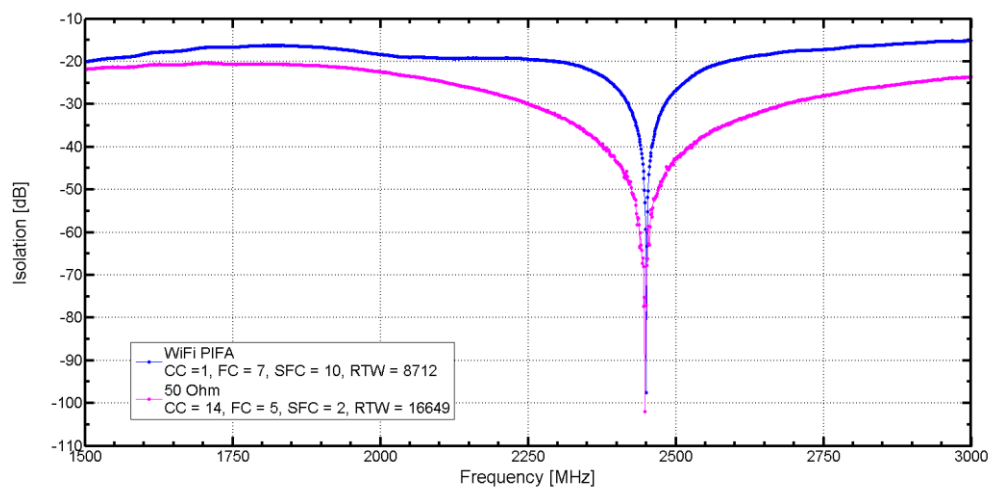


Figure 5.8 Measured isolation for the antenna and 50Ω load across frequency

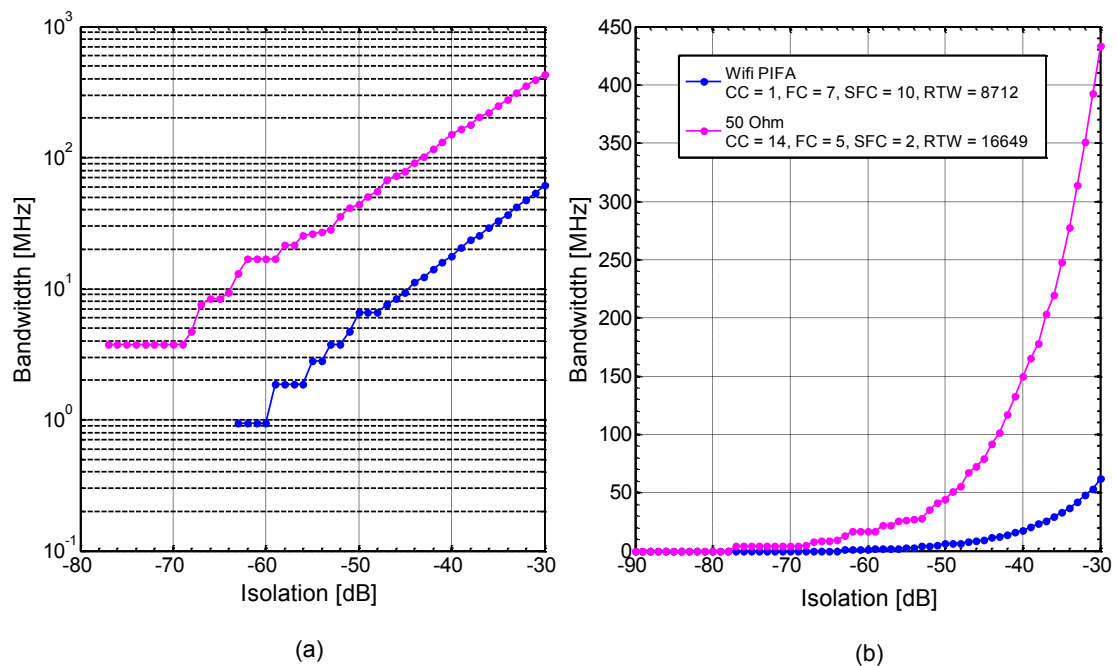


Figure 5.9 Isolation bandwidth comparison (a) log scale (b) linear scale

5.3.3 Characterization of the balancing region

The test setup used to verify if the balancing region is in the desired location is shown in Figure 5.10. It consists of a VNA, PCB-1 (no 50 Ω match), a Maury impedance tuner, and a Krytar 180° hybrid coupler.

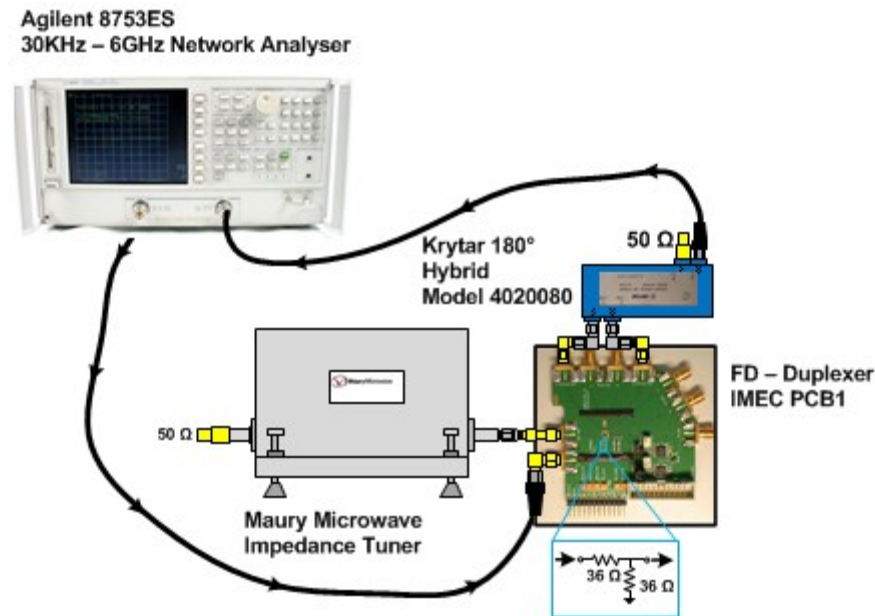


Figure 5.10 Balancing circuit characterization setup

During the measurement, the DUT is given a specific setting. The impedance presented by the tuner at the ANT port of the PCB is changed until high Tx-to-Rx isolation is found with the VNA. High isolation is obtained if a balanced condition is achieved. The isolation indicates that the impedance presented by impedance tuner combined with the intermediate interconnect equals the impedance provided by the balancing circuit at the given setting.

To obtain the impedance corresponding to a given setting of the balancing circuit, again a search algorithm was devised. The operation of this algorithm is illustrated in the Figure 5.11. The figure shows the data for the first four iterations of the algorithm plotted on the Smith chart (1-yellow 2-green 3-pink 4-blue). The algorithm uses two approaches depending on the measured isolation. During the first two iterations presented in the Figure 5.11, the program uses the first approach and sets the tuner to a grid of 25 equally spaced impedance points (yellow). At each point the VNA measures isolation provided with these impedances. Then it calculates the average isolation for all

16 squares (made from those 25 points) in the grid. The algorithm then defines a new 25 point grid on the square with highest average and its adjacent squares (green). If during one of these iterations an higher isolation is measured than a chosen threshold, the algorithm uses a fitted curve obtained through characterization of the duplexer's isolation pattern (discussed in the next section) to predict the absolute difference to the ideal tuner impedance. This can be seen in the figure as the search pattern changes to a circular shape around the impedance that provided the highest isolation (pink and blue). By using the isolation characteristic, the algorithm quickly converges to the ideal impedance and provides high isolation. The measured isolation at each impedance provided by the tuner is presented in Figure 5.12a which shows that after 6 iterations - 80 dB isolation is found (125 measurements). Figure 5.12b shows the impedance settings of the tuner as it converged toward the ideal value.

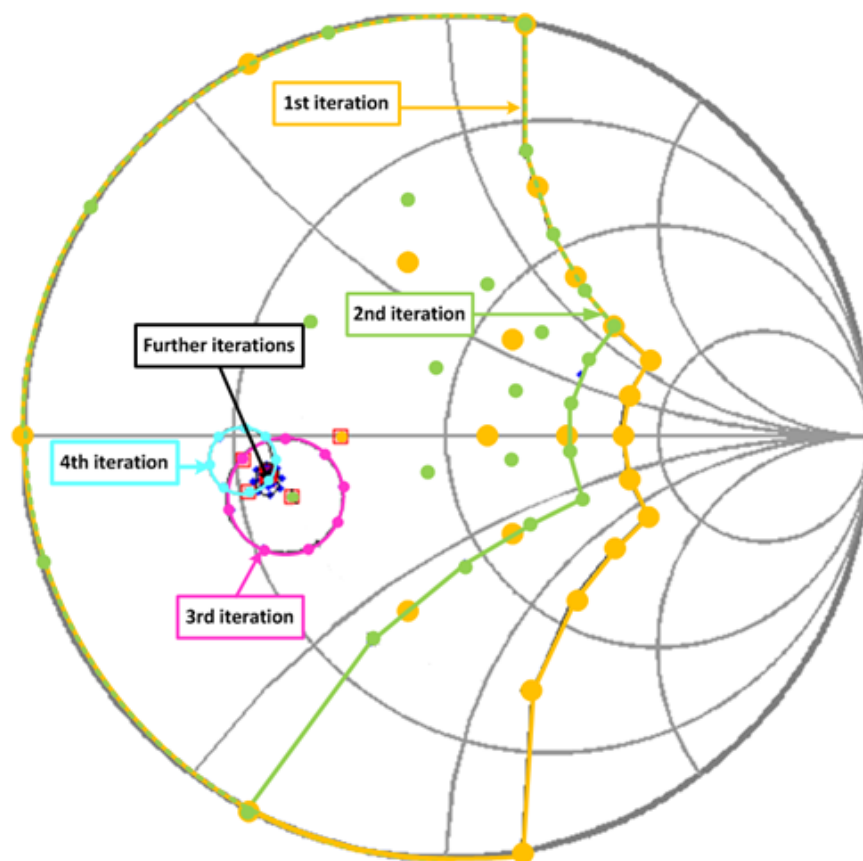


Figure 5.11 - Search iterations in the Smith chart

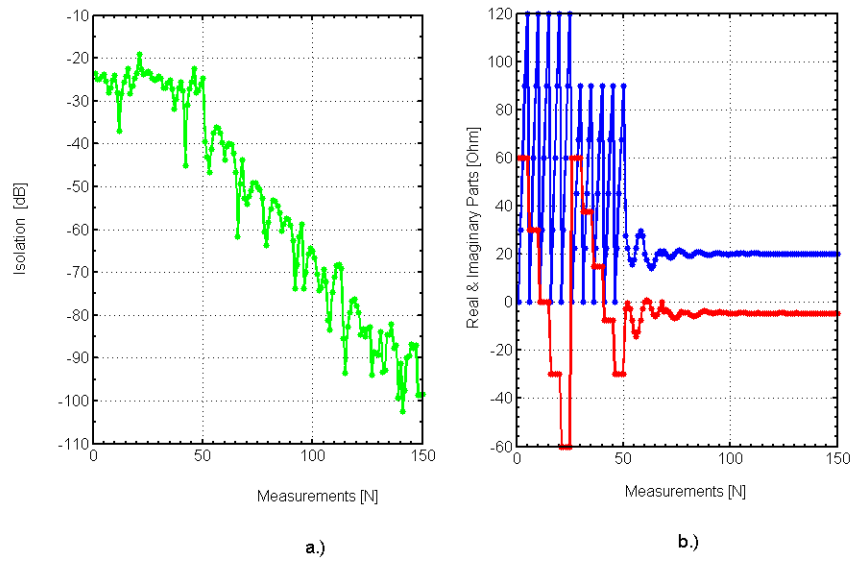


Figure 5.12 Convergence to the impedance provided by the balancing circuit
(a.) Isolation versus measurements numbers (N) (b.) Convergence to desired impedance value

Using the previously described setup and algorithm the balancing region illustrated in Figure 5.13 was obtained. For the measurement, 45 settings of the balancing circuit were selected that are evenly space across its complete tuning range. Each point in the figure corresponds to a tuner impedance to which the algorithm converged.

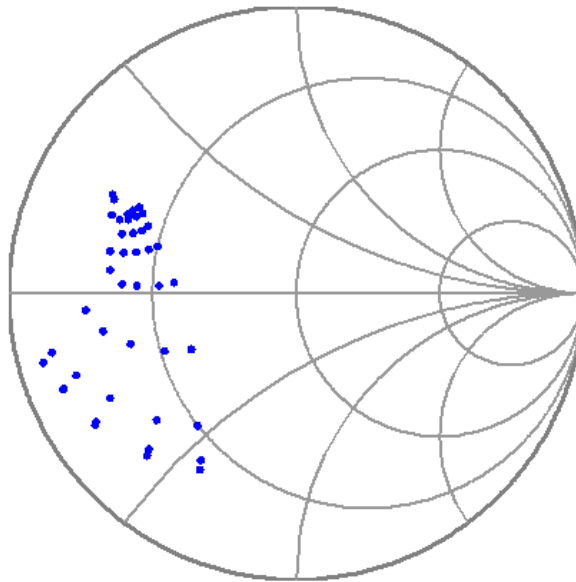


Figure 5.13 Measured impedances at various settings of the balancing circuit

The impedance values provide by the impedance tuner are, however, located at the connector interface of the PCB. To obtain the actual impedance presented by the balancing circuit at each particular setting, the measured impedances have to be

modified to account for the impedance change caused by the intermediate interconnect between the duplexer and the tuner. This problem is illustrated in Figure 5.14. The interconnect is modelled by a π -network consisting of the IC pad capacitance, a bondwire, the PCB pad capacitance, followed by a transmission line.

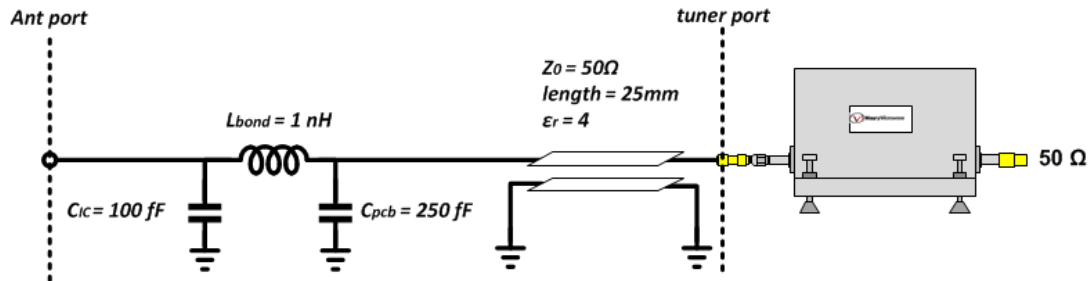


Figure 5.14 Tuner impedance transformation

The parameters of the π -network are estimations, while the transmission line was taken to be twice as long as measured (using a Caliper) to account for the permittivity of the PCB ($\epsilon_r \approx 4$). The result of the impedance added between Ant and IC bondpad to the measured data at the Ant port is presented in Figure 5.15. Although not an exact fit, it shows that the balancing circuit is near its intended impedance, which is consistent with previous measurements that indicated that the antenna could be balanced at the frequency of operation.

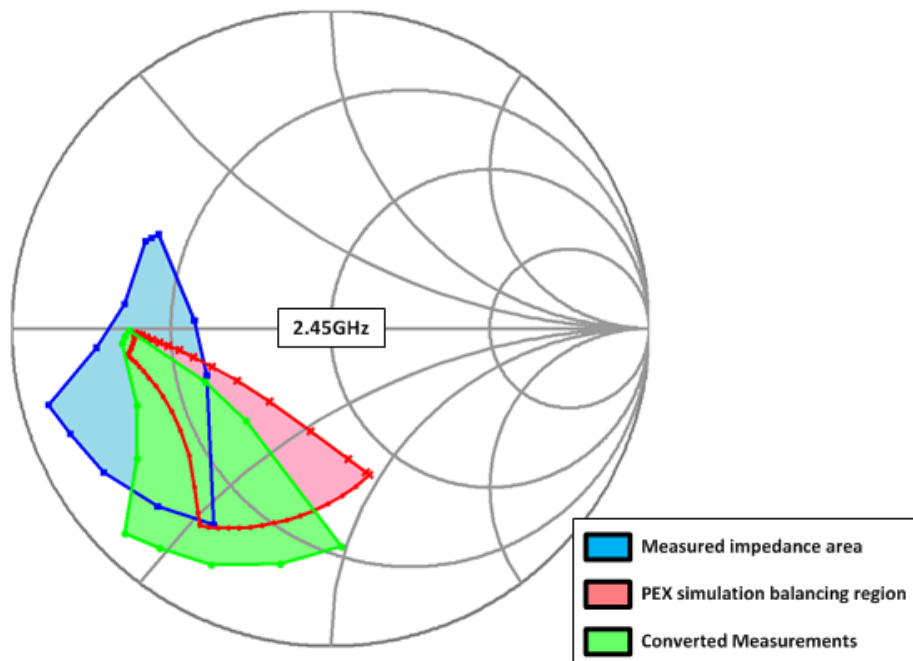


Figure 5.15 Transformed tuner impedances

5.3.4 Isolation versus imbalance

To see the relationship between imbalance and isolation, the tuner was used to provide impedances with an equal absolute difference from a known impedance corresponding a chosen tuning setting (point $21.81 - j10.64 \Omega$ which corresponds to setting $CC = 0$, $FC = 0$, $SFC = 0$, $RTW = 7500$ of the balancing circuit). While drawing these circles of impedance states around the know impedance, the Tx-to-Rx isolation was measured to determine the relationship between imbalance and isolation. The points around the selected impedance are illustrated in Figure 5.16 Measurement points around $Z_{bal} = 21.81 - j10.64$ and measured isolation for each point is given in Figure 5.17.

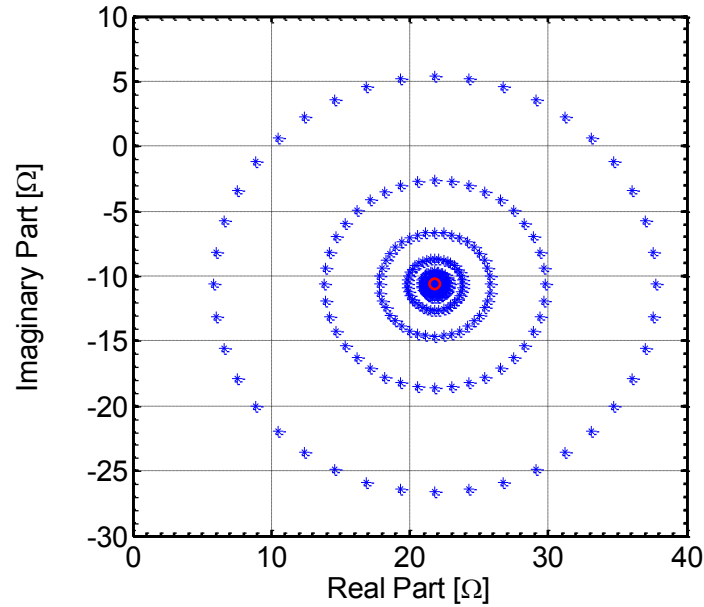


Figure 5.16 Measurement points around $Z_{bal} = 21.81 - j10.64$

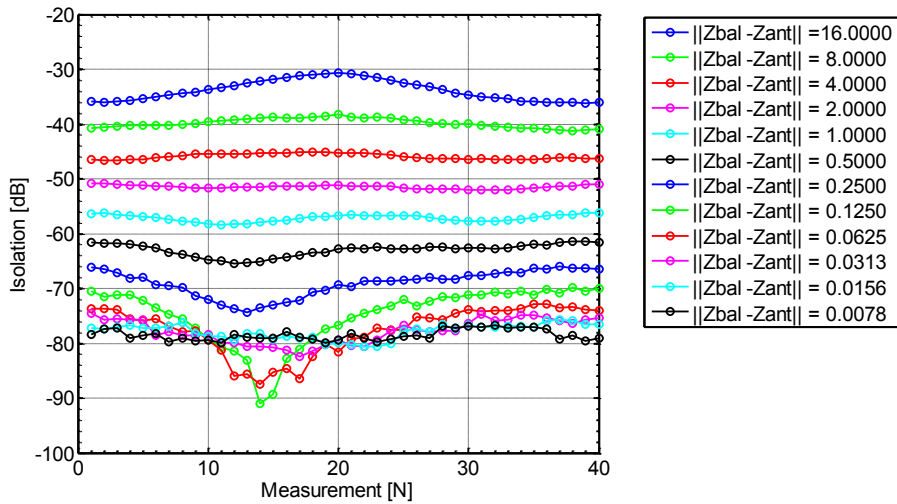


Figure 5.17 Isolation measurement with given absolute difference

Taking the average of the measured isolation for each circle, resulted in Figure 5.18. The measurements clearly show a 6 dB increase in isolation, each time the absolute difference is halved. Curve fitting the data resulted in the following relation:

$$ISO_{Tx} = 8.3712 \ln|Z_{Ant} - Z_{bal}| + 57.175 [dB] \quad (5.1)$$

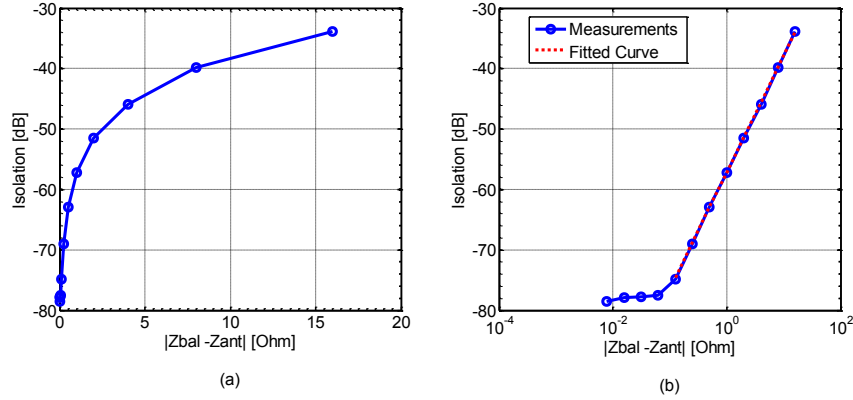


Figure 5.18 Isolation versus imbalance (a) linear scale (b) log scale

This equation was used in the search algorithm described in the previous section to estimate the impedance offset from the ideal impedance. This equation allowed the algorithm to converge in significantly faster. This curve only worked for the bypass ports of the PCB. When measuring isolation from at LNA output a new fit is required.

5.3.5 Common-mode Isolation

The common-mode isolation was measured using the network analyser. The results of this measurement are presented in Figure 5.19. Although the graph shows the common-mode isolation only up to 2.2 GHz the isolation at 2.45 GHz is expected to be similar. The results agree with simulations although a 2 dB difference in CM Tx isolation can be observed depending on the tuning setting of the balancing network.

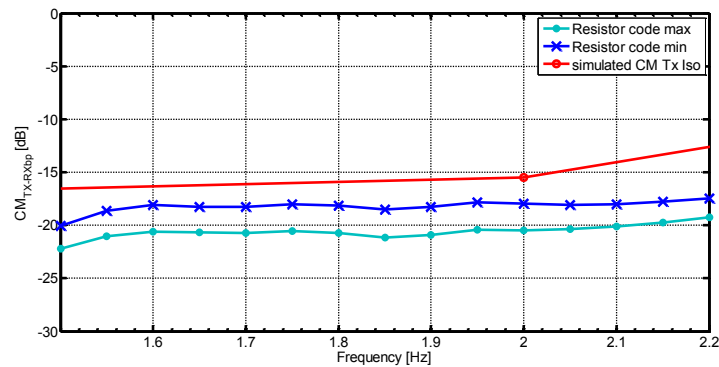


Figure 5.19 Common-mode isolation from 1.5GHz to 2.2GHz

5.3.6 Gain

The measured gain is given in Figure 5.20, which is lower than the post-layout simulation given by the red curve. Here just as in the post-layout simulations, the gain is shifted to lower frequency, indicating that the capacitance values used to resonate the transformer are too high. As seen in the CM isolation measurement, there is a code dependency in the gain curve, where the highest gain is observed close to the balanced condition. It should be noted that the simulated gain curve was taken in a more ideal balanced condition.

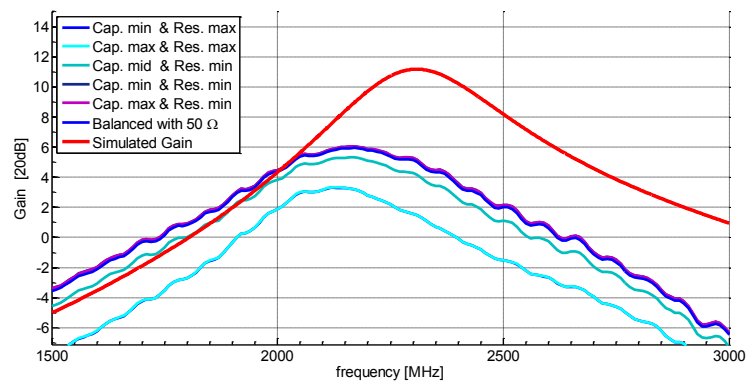


Figure 5.20 Cascaded Gain

5.3.7 Noise Figure

The noise figure was measured using the measurement setup is presented in Figure 5.21. The setup consists of a spectrum analyser, a noise source, PCB-2, a hybrid coupler, and a RF amplifier. The parasitic effects of the cables, hybrid coupler and amplifier were de-embedded from the measurement is shown in Figure 5.22

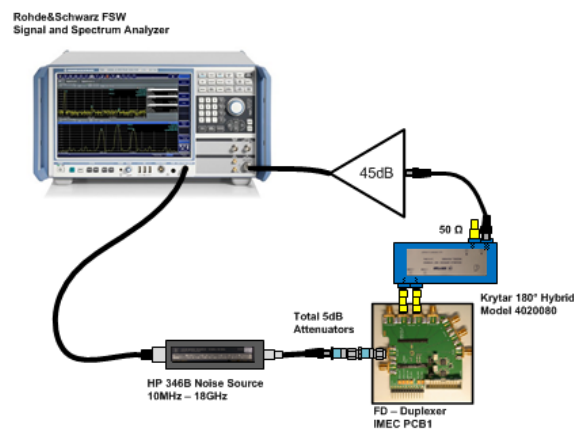


Figure 5.21 Noise figure measurement setup

The data shows an NF between 7 dB and 8dB depending on the setting of the balancing circuit. Here a lower resistance at the balancing circuit results in a lower NF. The measured NF is lower than found in the simulations (9 dB). The discrepancy found between measurements and simulations is that the simulations were done with a 50 Ω and 52 Ω at the Ant and Bal ports, respectively. However, during the measurements the 50 Ω impedance of the noise source is changed by a matching network so that balancing circuit can provide the balanced condition. Therefore the duplexer effectively sees two lower impedance terminations at the Ant and Bal ports, and therefore a lower NF is found in measurements.

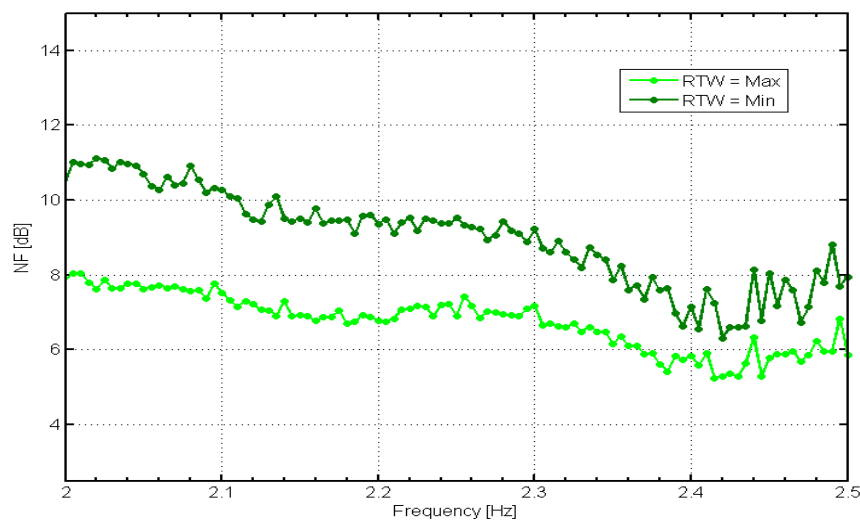


Figure 5.22 Measured noise figure

5.3.8 Linearity

The setup used to measure the linearity of the duplexer is given in Figure 5.23. Due to the passive nature of the duplexer, a significant input power is required to produce measureable third-order intermodulation distortion (IM3) above the measurement noise floor. The IM3 products produced by the signal generators and signal analysers dominated setup linearity. To reduce the IM3 generated by the signal generators, circulators were added to prevent reflection back into the generators and a 45dB amplifier was added so that the output power of the generators could be reduced, allowing them to function more linearly. This amplifier also produced significant IM3 products, so band-pass filters were required to filter these components off. In this way, a

cleaner two-tone was available for the DUT. A second pair of band pass filters was used to separate the IM3 products produced by the DUT from the main tones. This was necessary to prevent the IM1 power from swamping the desired IM3s. The setup was tested and the results are shown in Figure 5.24. As can be seen, the setup had an IIP3 of around 40dBm.

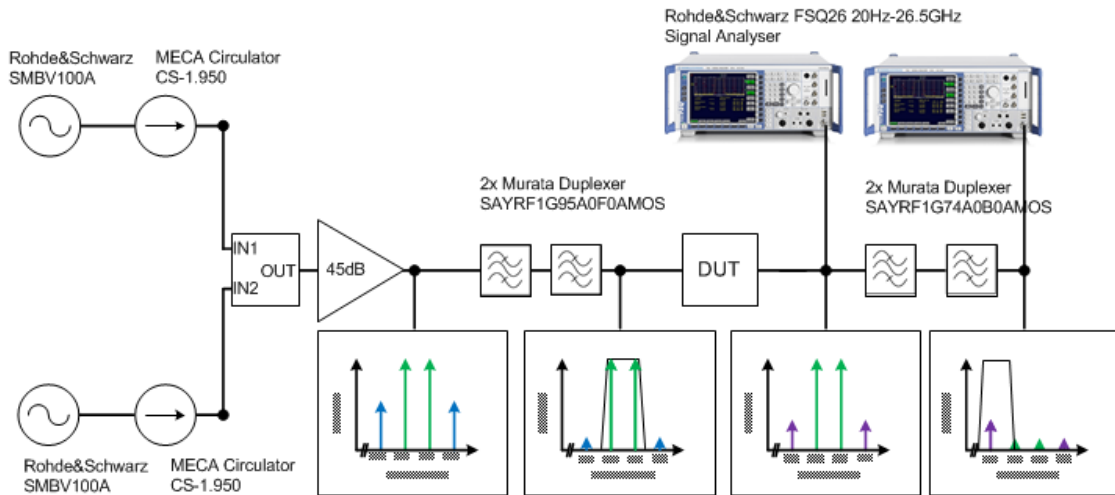


Figure 5.23 Measurement setup for the third-order intercept point

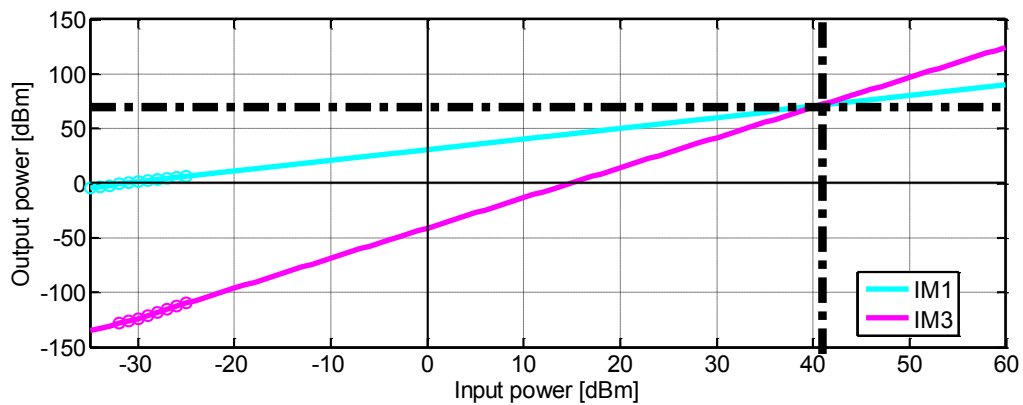


Figure 5.24 Third-order intercept point of the measurement setup

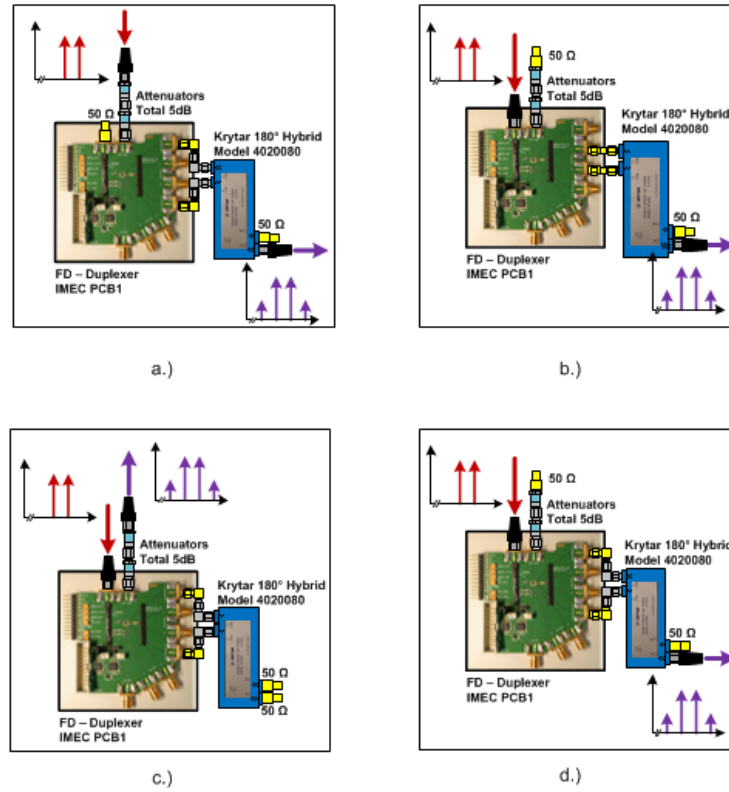


Figure 5.25 Measured DUT configurations

Figure 5.25 illustrates the four ways that the IIP3 of the DUT was measured. In the first measurement shown in Figure 5.25a, the two-tone signal was inserted in the Antenna port, and the fundamental and IM3 were measured at the bypass ports. The result of these measurements is illustrated Figure 5.26, where the blue curves represent the fundamental and the pink curves represent the IM3 products. The measurement was done at different setting of the balancing circuit. Extrapolating the fundamental and the IM3 products, the IIP3 was calculated. The result of these calculations is presented in Figure 5.27. It can be seen that the IIP3 lies between 20 and 30 dBm depending on the setting of the balancing circuit, where lower resistance in the balancing network corresponds with the lower linearity of 20 dBm. It should be noted that above input powers above -10dBm show unexpected behaviour at higher resistive settings, as the IIP3 at these setting no longer remain constant. This could be due to the fact than the part of the RF signal is able to travel to the gate of the NMOS used to provide the tunability of the tunable resistance of the balancing circuit.

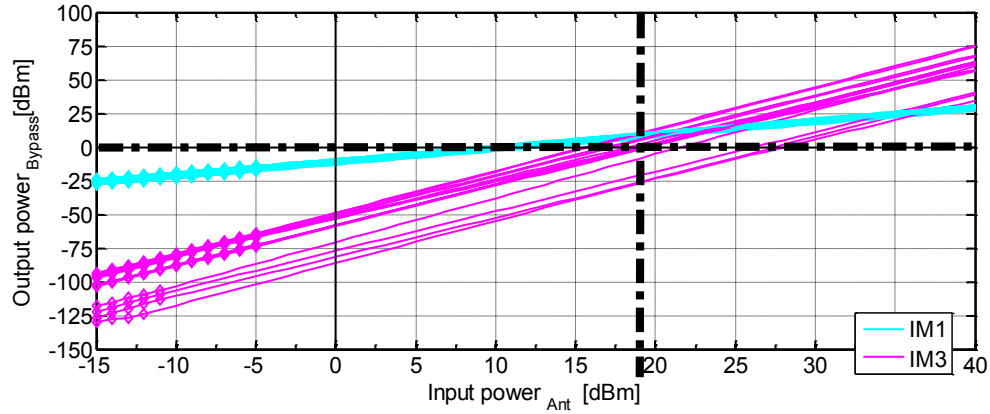


Figure 5.26 IM1 and IM3 measured from Antenna to Bypass ports

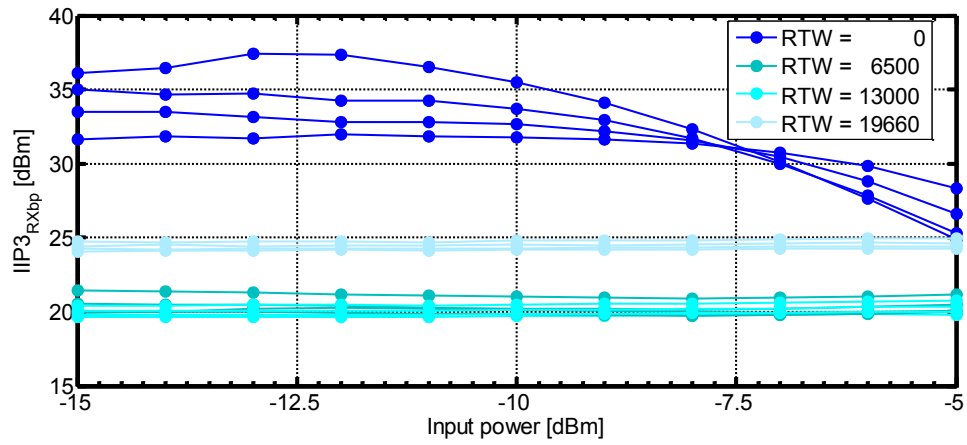


Figure 5.27 IIP3 measured from Antenna to Bypass ports

In the second IIP3 measurement, the two-tone signal is inserted in PA port and the fundamentals and IM3 products are measured at the output of the LNA (as depicted in Figure 5.25b). Again, multiple settings of the balancing circuit were used and the results are presented in Figure 5.28. The IIP3 corresponding to these measurements are plotted in Figure 5.29, showing an IIP3 between 0 dBm and 6 dBm. The low resistive setting of the balancing circuit correspond to the lower IIP3 values.

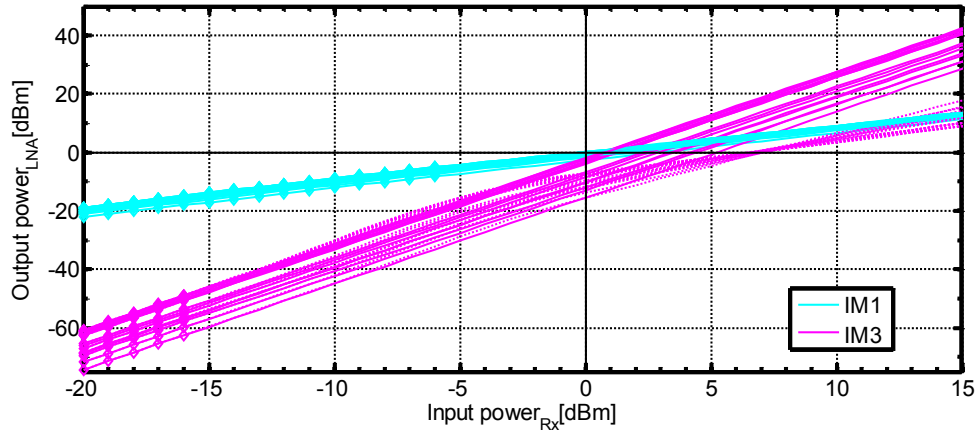


Figure 5.28 IM1 and IM3 measured from PA to LNA ports

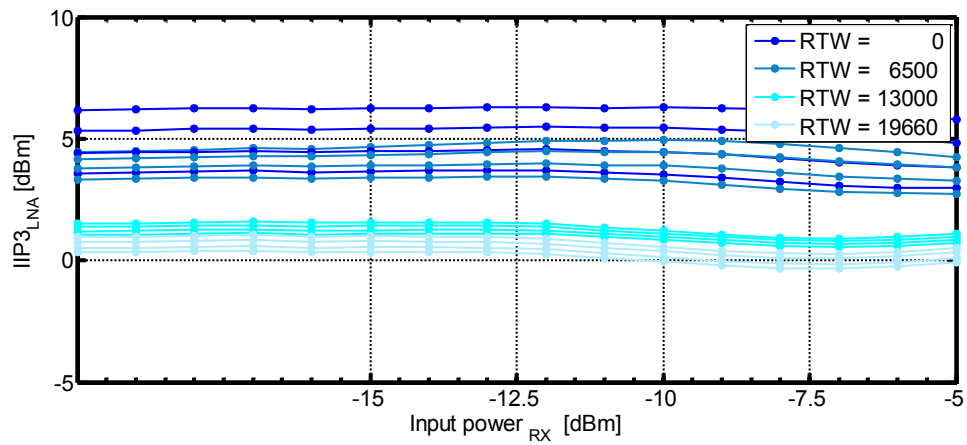


Figure 5.29 IIP3 measured from PA to LNA ports

The third IIP3 measurement test is shown in Figure 5.25c. Here the two-tone signal is inserted at the PA port and the fundamentals and the IM3 products are measured at antenna port. Multiple settings of the balancing circuit are used during the measurement. The IM1 and IM3 are presented in Figure 5.30, and the IIP3 is given in Figure 5.32. The measured IIP3 differs ranges from 36 dBm and 20 dBm, and the lower resistive values in the balancing circuit again correspond to the lower values intercept points. The results of this measurement also show that the IIP3 does not remain constant at higher input powers.

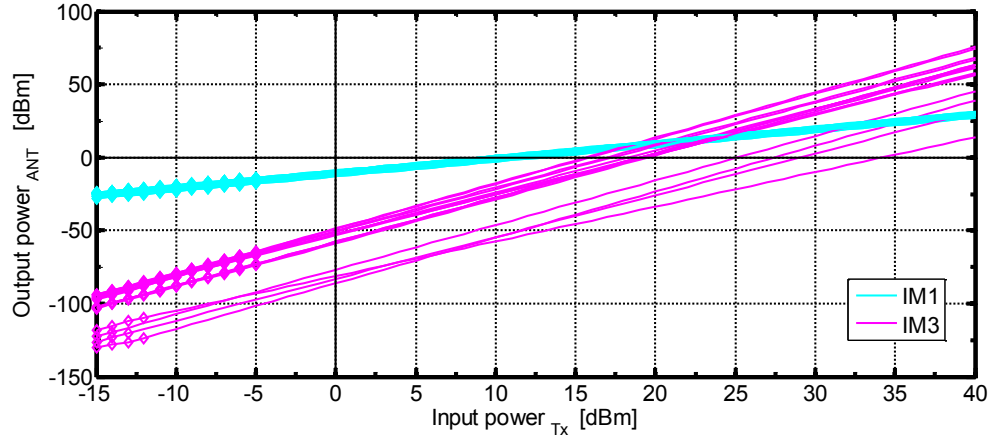


Figure 5.30 IM1 and IM3 measured from PA to Ant ports

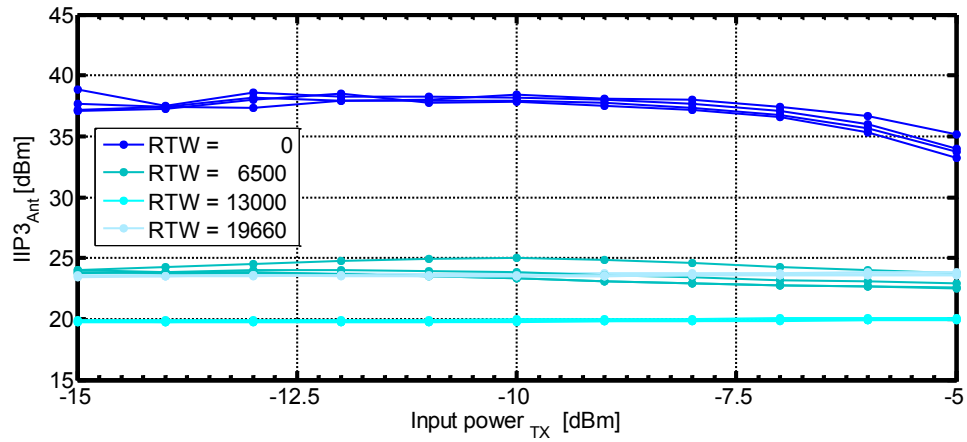


Figure 5.31 IIP3 measured from PA to Ant ports

For the final IIP3 measurement the two-tone signal is inserted at the PA port and the IM products are measured at the bypass ports as is depicted in Figure 5.25d. Again multiple settings are used this measurements and the results are given in Figure 5.32 and Figure 5.33. As can be seen from the data, measured IIP3s were between 37 dBm and 18 dBm, and the lower IIP3 values correspond to low resistance setting in the balancing network.

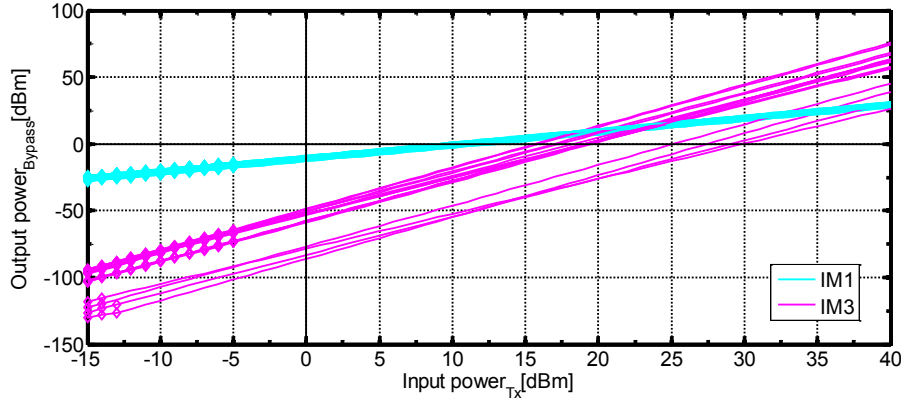


Figure 5.32 IM1 and IM3 measured from PA to Bypass ports

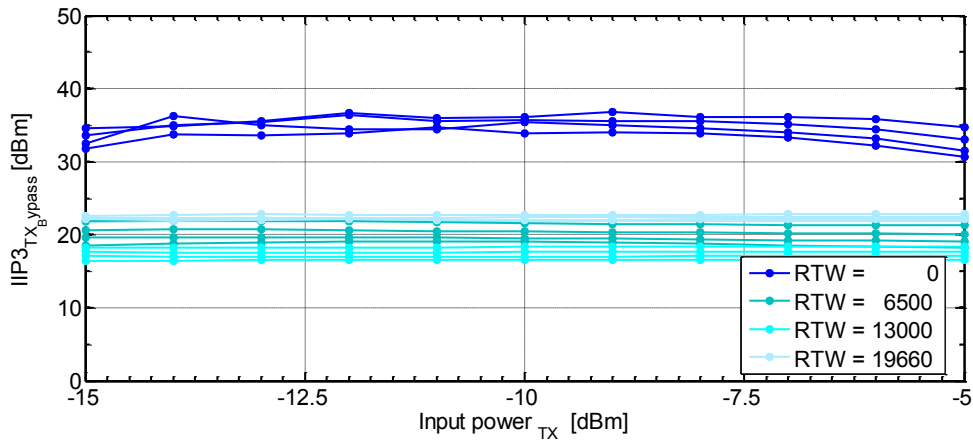


Figure 5.33 IIP3 measured from PA to Bypass ports

5.4 Measurement Summary

A summary of the duplexer performance is given in Table XI. The blue values are measured, while the red values obtained were obtained via post-layout simulations. The isolation characteristic of the duplexer is $\geq 70\text{dB}$ as desired, however, the bandwidth leaves something to be desired. Also the noise figure is too high as it leaves no noise budget for the following receiver stage. This was caused by inadequate understanding of the transformer behaviour and too much emphasis on an unbalanced desire to keeping the Tx insertion losses to a minimum during the design phase.

The prototype was not able to meet all the design goals, and shows less performance than previous integrated duplexers. This is caused by two aspects. The first is that the prototype design is characterized with a real antenna. The limited isolation and aggregated bandwidth are primarily caused by the frequency behaviour of the chosen antenna. All other duplexers in the table would suffer from similar narrowband performance if evaluated with a real antenna instead of $50\ \Omega$ terminations.

Table XI Duplexer performance

Specification	This work	Goals	[20]	[20]	[21]	[22]
Tx output power	-10 dBm	-10 dBm	24dBm	24dBm	24dBm	24dBm
Operating Frequency	2.47 GHz	2.45 GHz	1.95 GHz	1.95 GHz	1.9 GHz	1.95 GHz
1dB Compression Point	~ -10 dBm	-5 dBm	-	-	-	-
Cas. IIP3	0dBm	0 dBm	-	-	-	-
Differential isolation	70 dB	40-70 dB	> 50.0 dB	> 50.0 dB	> 55.0 dB	>70 dB
CM isolation	20 dB	30 dB	-	-	0dB	60dB
Tx insertion Loss	3.4 dB	3.5 dB	5.9dB	4.2dB	2.5dB	4.7dB
Rx insertion Loss	-11 dB	4.0 dB	2.9dB	4.2dB	-	-
Cascaded NF	8.0 dB	8.0 dB	6.1dB	7.4dB	5.0dB	6.7dB
Cascaded Gain	6.0dB	3.0 dB	23dB	24dB	27dB	17dB
Agg. Bandwidth	100 MHz	150 MHz	1 GHz	1 GHz	400 MHz	500 MHz
Iso. BW 60dB	1 MHz	10 MHz	5 MHz	5 MHz	250 MHz	190 MHz
Area	0.2mm ²	0.2mm ²	0.2 mm ²	0.2 mm ²	0.2 mm ²	0.6 mm ²

The second that constraint performance is the limited metal stack available in the 180 nm UMC technology. This made it difficult to realize a low loss transformer. The previous duplexer used significantly more advanced metal stacks [23] [25]. This prototype could however have performed better in terms of noise if a more balanced trade-off was made between the Tx and Rx insertion losses.

The low output power of the proposed FD application significantly relaxed linearity requirements as no high voltage precautions. The obtained IIP3 was 0 dBm so the -1dB compression point can be estimated at -10dBm. This is somewhat lower than the goal so any future design will have to take some measures to improve this number. CM Tx isolation was also somewhat lower than desired, but as there is little material to compare with it is difficult to say what could be achieved.

Although the balancing region in simulation was expected to be on top of the antenna impedance at 2,45GHz, this was not true in measurements as high isolation could only be found 25 MHz higher. However this could also be due to the PCB. If in a future design both are better characterized the design method used to place the balancing region on top of the measured antenna impedance could be validated as an exact means to design duplexer balancing circuits.

Chapter 6

Conclusion

This chapter starts with a summary. This is followed by contributions in this work and then by answers to the questions raised in the introduction. How does an integrated hybrid transformer provide isolation? How does this isolation relate to transceiver performance characteristics? And how does is this relation affected by process parameters? The last section suggests possible future work.

6.1 Summary

Chapter 1 Discusses wireless FD. This transmission scheme aims to improve spectral efficiency of wireless systems by allowing concurrent transmission and reception over a single carrier. The problem inhibiting FD is Tx-leakage. In conventional duplex schemes such a TDD and FDD, Tx-leakage is mitigated with filters or switches. Both techniques do not allow FD operation, so neither is applicable in FD transceivers. Therefore FD systems require other means to cancel their own Tx-interference. This can be done by an integrated hybrid transformer which provides directional isolation through balanced currents and voltages.

Chapter 2 provides theoretical background on the hybrid transformer operation and discusses its four unique properties: bi-conjugacy between alternate sets of ports, the ability to match all four ports, the ability to split power and to provide a 180° phase inversion in one of its transmission ratios. This is followed by a discussion on the isolation properties of the hybrid transformer when used as a duplexer.

Chapter 3 presents the design of the duplexer prototype in 180nm RFCMOS. It starts with the design goals and proceeds with the topology choice. After this, the designs of the transformer and the balancing circuit are presented.

Chapter 4 presents the layout of the prototype from top to bottom. This starts with the full die, and works its way down to the individual sub-circuits. At each level, layout considerations are discussed and the performance of the post-layout circuit is compared to schematic simulations in order to see how layout affects performance. The chapter ends with an evaluation of top level.

Chapter 5 presents the measurements results on the designed prototype. These showed high peak isolations of 80 dB and a 1 MHz isolation bandwidth for 60dB. The gain of the duplexer LNA cascade is 3dB and the NF 8dB. The measured IIP3 at the LNA output when a two-tone is inserted in the PA was measured to be 0 dBm and the duplexer also provided 20dB of CM-isolation. Measurements also show that the balancing network missed the targeted antenna impedance by 26 MHz, as the closest frequency where high isolation is provided with the PIFA antenna is 2476 MHz.

6.2 Contributions

This work documents the design and evaluation of an integrated electrical balance duplexer in 180nm RFCMOS. It shows that through proper characterization of the antenna impedance and intermediate interconnect, a duplexer and balancing circuit can be designed to provide a desired balanced condition and the resulting isolation. It is also shown through analysis and measurements, that with sufficient resolution in balancing circuit, the impedance provided by the antenna can be accurately replicated at the balance port of the transformer. This results in peak isolations as high as 80 dB. Although not achieved completely during this project, lessons have been learned that will enable development of a future duplexer to provide more favourable performance with respect to NF and isolation bandwidth. An attempt was made to properly document these findings so that future work on duplexer can benefit from the knowledge and experience gained during this study.

Characterization of future duplexers is made easier through the development of measurement setups and search algorithms that allow faster characterization of the balancing region and isolation characteristics. Even when used on a duplexer with a large number of settings (2^{24}), the high isolation setting can be found with less than 150 measurements. These experiments also showed that the isolation characteristics provided by a duplexer can be used to obtain a significant reduction in the number of iterations needed to locate the ideal tuning setting.

6.3 Conclusions

The goal of this work was to investigate how much isolation and isolation bandwidth can be obtained with a CMOS hybrid transformer and a commercial antenna. Measurements showed 80 dB peak isolation with an isolation bandwidth of less than 1

MHz. However to see how these two (and other) properties are related, three questions (as stated in the introduction) were used as guidelines. The first was to find out how an electrical balance duplexer provides isolation. This was partly answered with eq. (2.14), and to some degree confirmed through measurements which show that the isolation increases with 6 dB each time the absolute difference between the impedances on both sides of the autotransformer is halved. It can also be deduced from this result that isolation bandwidth increases if this absolute difference is kept small across frequency.

The second question was to see how the desired isolation trades-off with performance characteristics such as NF, linearity, Tx insertion loss and common-mode isolation. Although the prototype does not demonstrate an optimal trade-off between the different characteristics, it does provide insight in the relations between the different performance characteristics. In Chapter 3, it is explained that the isolation characteristics and linearity of the duplexer are primarily determined by the resolution, frequency behaviour and non-linearity of the balancing circuit, and that characteristics such as insertion losses, NF and CM-isolation are subject to transformer performance.

The answer to the third question is closely related to the second. This question asked how the trade-off between isolation and other desired performance characteristics is related to technology parameters. The two technology aspects that influence the performance of an integrated duplexer can be identified as the available metal stack and the devices available to implement the on-chip tuning network. The available metal stack determines which topology choices and trade-offs can be made in the transformer design, and therefore determines the insertion losses and NF obtainable for the duplexer. A more advanced metal stack, in the sense of thicker metals, higher conductivity metals, more metal layers, a higher resistivity substrate or inclusion of thicker dielectric layers between the windings and substrate would allow a transformer with lower energy losses, and thus lower duplexer insertion loss and NF and the a CM-isolation (provide more ideal ground connection). The performance of the balancing circuit depends on the resolution provided, and the parasitics that accompany this resolution. A more advanced technology node, for example, would improve balancing circuit performance as it provides smaller capacitor values and transistors that have a lower on-resistance and smaller capacitor parasitics. This allows a balancing circuit with finer resolution and less parasitic overhead.

6.4 Future Work

The peak isolation provided by the prototype was satisfactory, and the flaws in the prototype can be mitigated by accepting higher Tx insertion losses in order to obtain proper hybrid transformer operation. NF and insertion losses can be decreased further, by using a fabrication process with a more advanced metal stack. Two aspects that are not easily improved are the isolation bandwidth and balancing region placement.

The prototype showed that a balancing circuit implemented with a tuneable RC-circuit can provide a balance condition at a given frequency, but it is incapable of tracking the antenna impedance across a wide frequency range. This results in a narrow isolation bandwidth as the two impedances on either side of the transformer don't have similar frequency behaviour. Improvements to the isolation bandwidth can therefore, only be realized with a balancing circuit that behaves more like an antenna, or an antenna which behaves more like the balancing circuit, or by a co-design that does a little of both. Designing a balancing circuit that behaves more like an antenna requires a tuneable RLC-resonant circuit with a Q-factor similar to that of the antenna, which could be difficult in monolithic circuits. An antenna that behaves more like the balancing circuit is an antenna with low Q-factor, which is in line with the recent trend of developing more wide-band antennas. The combined approach would require RF circuit and antenna design expertise, in order to perform co-design.

The measured antenna impedances for this design were located in the lower half of the Smith chart. This allowed the balancing circuit to be implemented with a simple RC network. Not every antenna, however, displays this capacitive behaviour. This means that an antenna with a primarily inductive behaviour would require a different balancing circuit. Future work should, therefore, include the development of techniques that allow balance region placement to other locations in the Smith chart.

The measurements showed that through the use of simple search algorithms, the ideal setting to balance with the antenna could be found in 150 measurements. Future work could include the realization of a self-tuning duplexer. This requires isolation detection, an on-chip DAC, and digital hardware to implement a search algorithm.

Last, future work towards the realization of full-duplex receivers would be to implement an active self-interference stage to follow the duplexer. By developing the next SIC stage in the receiver, the realization of an integrated FD transceiver could become reality.

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