High Speed readout architecture for CMOS image sensor

A dual approach using adaptive reconfigurable Systems and low-power sar ADCS

Lee, J.

DOI
10.4233/uuid:5221e776-d2b3-472d-93d5-1d32efd7ea1e

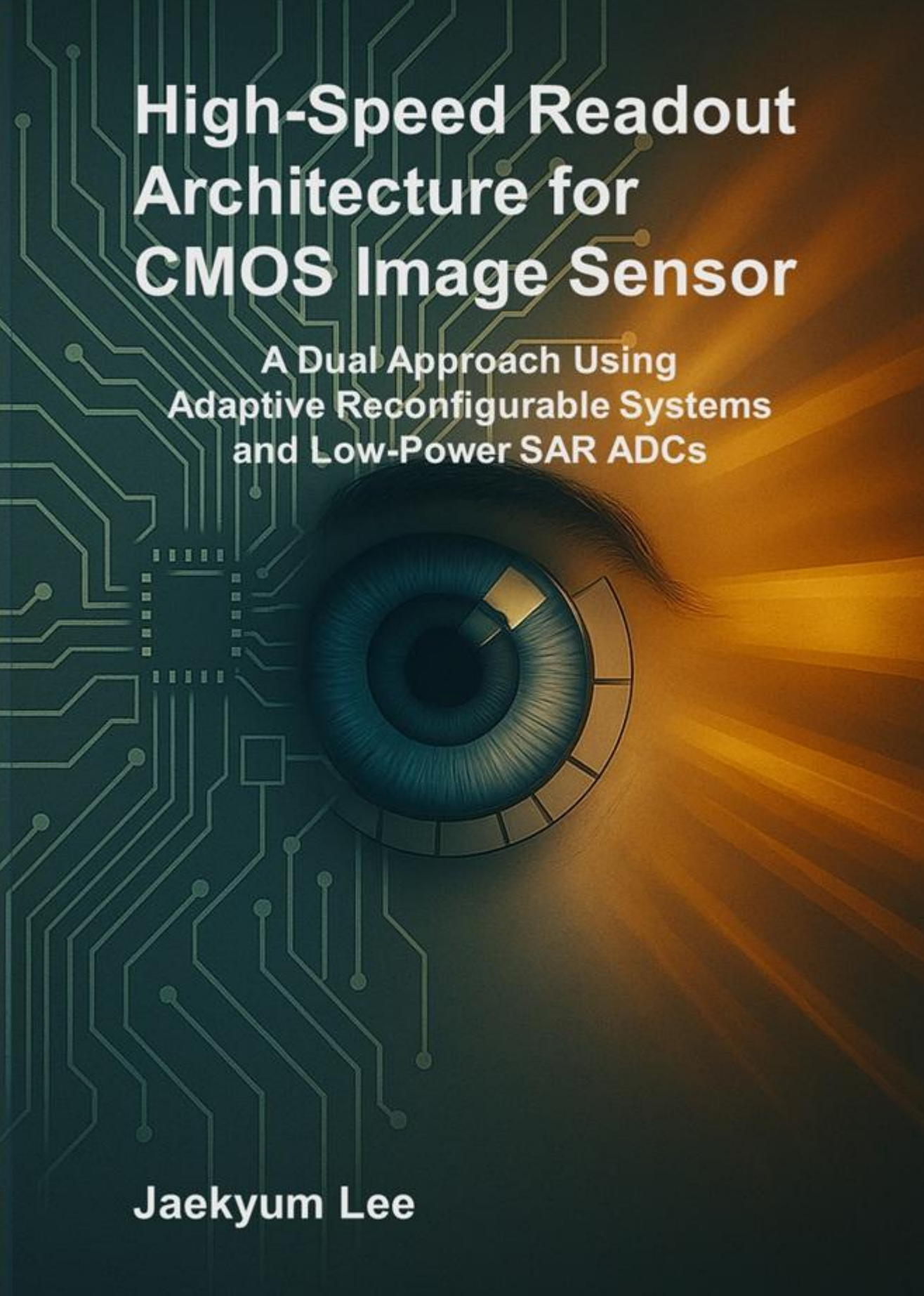
Publication date
2026

Document Version
Final published version

Citation (APA)
Lee, J. (2026). *High Speed readout architecture for CMOS image sensor: A dual approach using adaptive reconfigurable Systems and low-power sar ADCS* . [Dissertation (TU Delft), Delft University of Technology]. https://doi.org/10.4233/uuid:5221e776-d2b3-472d-93d5-1d32efd7ea1e

High-Speed Readout Architecture for CMOS Image Sensor

A Dual Approach Using Adaptive Reconfigurable Systems and Low-Power SAR ADCs



Jaekyum Lee

HIGH SPEED READOUT ARCHITECTURE FOR CMOS IMAGE SENSOR

A DUAL APPROACH USING ADAPTIVE RECONFIGURABLE SYSTEMS AND LOW-POWER SAR ADCS

HIGH SPEED READOUT ARCHITECTURE FOR CMOS IMAGE SENSOR

A DUAL APPROACH USING ADAPTIVE RECONFIGURABLE SYSTEMS AND LOW-POWER SAR ADCS

Dissertation

for the purpose of obtaining the degree of doctor
at Delft University of Technology,
by the authority of the Rector Magnificus, prof. dr. ir. T. H. J. J. van der Hagen,
chair of the Board for Doctorates,
to be defended publicly on
Thursday 8 January 2026 at 15:00 o'clock

by

Jaekyum LEE

Master of Science in Electrical Engineering,
KAIST (Korea Advanced Institute of Science and Technology), South Korea
born in Seoul, South Korea.

This dissertation has been approved by the promotors.

Composition of the doctoral committee:

Rector Magnificus,	Chairperson
prof. dr. ir. A. J. P. Theuwissen,	Delft University of Technology, promotor
prof. dr. P. J. French,	Delft University of Technology, promotor
Independent members:	
prof. dr. ir. F. P. Widdershoven,	Delft University of Technology
prof. dr. J. Lee,	Pohang University of Science and Technology, South Korea
prof. dr. ir. G. Meynants,	Katholieke Universiteit Leuven, Belgium
dr. ir. M. A. P. Pertijs,	Delft University of Technology
dr. P. Ramachandra Rao,	Delft University of Technology
prof. dr. ir. K. A. A. Makinwa,	Delft University of Technology, reserve member

Keywords: Image sensor, Machine vision, Region of interest, Readout IC

Printed by: U2pi BV, Den Haag, the Netherlands

Front & Back: Cover art generated using AI-assisted illustration tools, summarizing the core concept of this thesis.

ISBN 978-94-93437-59-3

An electronic version of this dissertation is available at
http://repository.tudelft.nl/.

The present is theirs;
the future, for which I really worked, is mine.

Nikola Tesla

CONTENTS

SUMMARY

This thesis presents a comprehensive study on enhancing the frame rate of CMOS image sensors through both circuit-level and system-level innovations. Motivated by the growing demands in machine vision and artificial intelligence applications such as ADAS and industrial automation, this work addresses the limitations of conventional high-speed image sensor designs, which typically require increased ADC sampling rates or a higher number of ADCs—often leading to trade-offs in area, power consumption, and image quality.

The first contribution of this research lies in the analog front-end design, particularly in optimizing the ADC architecture. A column-parallel SAR ADC is developed, with both conventional and advanced two-step structures implemented to reduce noise, improve linearity, and minimize layout area. These ADCs are designed to operate efficiently at 250kS/s while maintaining low temporal noise. Techniques such as analog correlated double sampling (CDS), comparator offset calibration, and FPN suppression using optical black (OB) pixels are applied to ensure image quality despite the high-speed operation. The overall noise model is theoretically analyzed and validated, showing that with proper bandwidth and CDS timing, temporal noise remains within acceptable limits without requiring high-frequency operation.

Beyond the circuit-level improvements, a major innovation is the implementation of an adaptive reconfigurable system that switches between full-frame and region-of-interest (ROI) modes. Recognizing that in many practical scenarios—such as tracking a moving object in a fixed background—only a small part of the image needs to be updated, the proposed system dynamically identifies and captures a small ROI (e.g., 10×10 pixels) around the object. By capturing multiple ROI images within a single full-frame cycle, the effective frame rate is dramatically improved without increasing ADC speed or interface bandwidth. The intelligent switch network, pixel array design, and address decoder architecture are all tailored to support seamless mode switching, enabling up to 750,000fps in effective frame rate while operating under fixed ADC sampling constraints.

The image data path, from pixel readout to ADC conversion and digital transmission, is carefully coordinated. In zoom-in mode, 300 ADCs sample and convert ROI data across three separate sets per horizontal line, managed by FPGA-controlled timing. Image data is reassembled and analyzed in real-time within the FPGA to update the ROI position based on intensity variation. The image analyzer performs high-speed comparison using a sliding 10×10 mask and updates ROI coordinates frame-by-frame. This feedback loop ensures accurate object tracking while minimizing redundant data processing.

Measurement results confirm that the proposed design successfully achieves high-speed performance and high image quality with improved energy efficiency. The background offset calibration achieves VFPN levels as low as 0.37LSB, and the system avoids the power and timing penalties typically associated with high-speed ADC operation and

high-throughput interfaces. The architecture demonstrates a scalable, application-specific approach to image sensor design, suitable for future intelligent sensing systems.

In summary, this thesis delivers a novel image sensor readout architecture that enhances frame rate without compromising image quality or power efficiency. It introduces a practical framework for high-speed operation through a dual approach: a compact, high-performance SAR ADC and a flexible reconfigurable system architecture. Together, these solutions form a robust platform for next-generation machine vision applications that demand both speed and intelligence.

1

INTRODUCTION

The rapid advancement of artificial intelligence and machine vision technologies has significantly increased the demand for high-performance image sensors. Key challenges include enhancing pixel resolution, readout speed, and image quality while maintaining low power consumption. This chapter introduces the motivation behind this research, outlines design considerations, and sets the direction of the proposed solution, which focuses on increasing frame rates through analog front-end speed optimization and reconfigurable system integration. The chapter concludes with a detailed thesis outline.

1

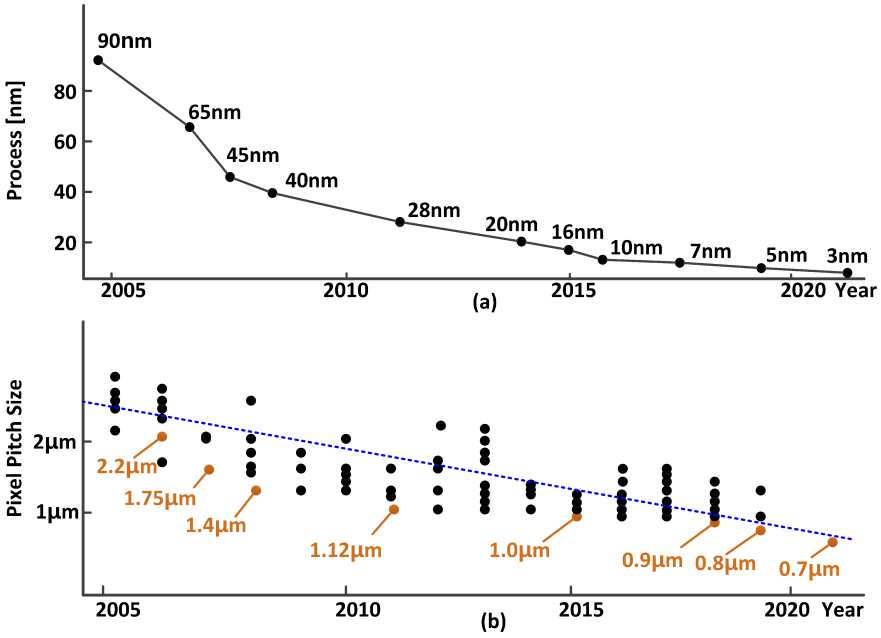


Figure 1.1: The development of (a) the semiconductor design process technology and (b) the pixel pitch size

1.1. THE RESEARCH BACKGROUND

A novel change has started in human life since the development of artificial intelligence. Artificial intelligence technology is used in image sensor applications, such as autonomous driving assistance systems (ADAS) and extreme ultraviolet (EUV) lithography machines. These applications completely changed how we work. The development of these machine vision applications has started after the research in various areas related to the image-sensor-achieved technological improvement. In particular, the following technological improvements have facilitated this change.

First, the semiconductor fabrication process has been improved following Moore's law [1]. Figure 1.1(a) shows the semiconductor technology development by year [2]. As shown in Figure 1.1(a), the 90nm process was commercialized about 20 years ago, and 3nm process is about to be commercialized in 2023. This advanced technology led to an increase in the circuit integration rate and smaller pixel size for image sensors. As a result, the resolution of the pixel array has increased. Figure 1.1(b) shows the pixel size designed for the smartphone and the digital still camera by year. In 2008, the earlier smartphone had a 1.4μm pixel pitch with a 5mega-pixel resolution, but recently 0.7μm pixel pitch size has been available, and the resolution already exceeds 50 mega-pixel. Recently Samsung and OmniVision announced through their publications that the pixel pitch size reached 0.61μm and 0.64μm, respectively [3], [4]. Furthermore, a paper presented at the 2023 International Image Sensor Workshop (IISW) reported a 0.56μm pixel pitch. In 2024, Samsung introduced a 0.5μm pixel image sensor [5].

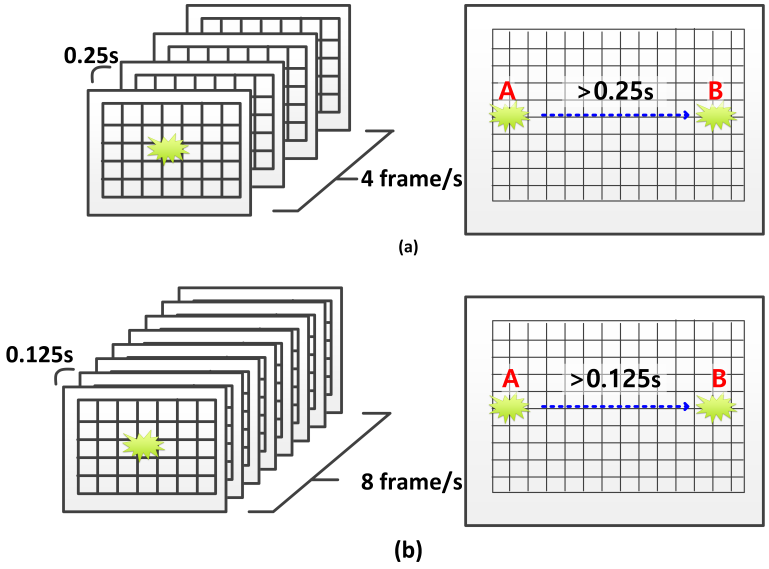


Figure 1.2: Example of the 2 image sensors having different frame rates

Second, the performance of the interface to transmit the data to the outside of the world has been improved. The improvement of the pixel resolution increased the amount of data to be processed inside the image sensor. In the case of early image sensors, the LVDS, developed in the 1990s, is used to transmit the data from the sensor to the display [6]. However, image sensors require interfaces with data rates reaching Gb/s per channel as pixel resolution increases. As a result, some companies, such as Samsung, used MIPI D-PHY, and others, such as SONY, developed their interface, SLVS-EC [7].

Third, the image sensor's performance also improved. In 2006, the structure introduced in [8] combined the correlated double sampling (CDS) and the digital double sampling (DDS) technique. Since this structure is simple and nicely improves noise performance, this structure has been commonly used in the industry. In addition to this improvement, the back-side illumination (BSI) technique with a vertical transfer gate (VTG) and the stacked structure had been developed. These improvements led to a better fill factor, and the device characteristics have been improved by separating the circuit and pixel fabrication process [9], [10], [11], [12], [13].

These technological advances have accelerated various applications. Along with the development of artificial intelligence, research to improve the performance of machine vision applications continued.

1.2. MOTIVATION

A machine vision system captures an image through the image sensor. Since the image sensor generates images in video mode, a high frame rate operation of the image sensor is required. Mainly there are several positive effects when the image sensor has a

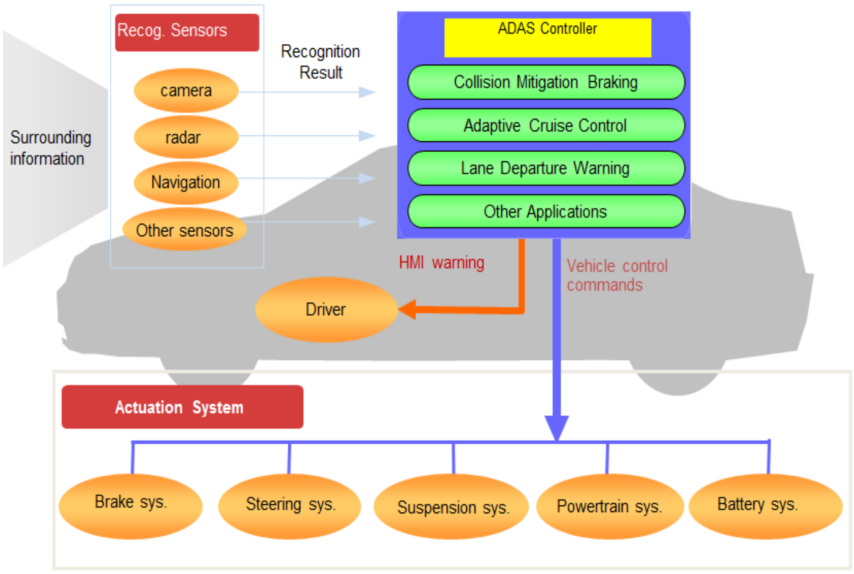


Figure 1.3: An example of the ADAS system from Hitachi, including a sensor interface

higher frame rate.

First, the movement of a fast-moving object can be detected as the frame rate increases. Figure 1.2 gives one example of the 2 image sensors having a frame rate of 4 frames/s and 8 frames/s, respectively. Since the time differences between sequentially generated 2 images are 0.25s and 0.125s, the maximum speed of the moving object that the image sensor detects is different. For example, the moving object is captured at point A in each case, and if the image sensor can detect the movement of this object, at least this moving object has to be detected at point B. From this point of view, the minimum time required to reach point B has to be 0.125s in the case of Figure 1.2(b). On the other hand, in the case of Figure 1.2(a), the required minimum time is 0.25s. The object speed detected at each frame rate is 2 times different. Therefore, a high frame rate image sensor can capture the movement of a relatively fast-moving object.

Second, a high frame rate operation improves the quality of the video. The image sensor generates the images periodically in video mode, and sequentially generated images show all possible transitions in the captured image in chronological order. The images arranged in chronological order have continuity. However, if the frame rate is low, the possible change between the image increases and the continuity of the images gets weaker because the time between each image is longer. Therefore, a high frame rate operation fortifies the image quality and the continuity of the images taken by the image sensor working in video mode.

Third, the efficiency of the system is improved. In a machine vision system, the system captures the data through the image sensor, performs data analysis and delivers the command after analysis. Figure 1.3 shows an example of a machine vision system used

Figure 1.4: The image taken at the tunnel (a) with and (b) without HDR mode

in an automobile [14]. In this system, the image sensor transmits the image to the controller called MCU, and the MCU makes an order for the driving. Since driving requires fast decisions at the right time, the system requires fast data processing to reduce the latency of this system. Since the image sensor contributes part of the latency and manages the accuracy of the data, developing a high image sensor frame rate is one of the critical factors in this system.

The positive effects mentioned above show the reason for improving the frame rate of the image sensor. Since high frame rate image sensors enable the system to get high-quality video images within a short time and with better efficiency, research in this area is strongly required.

1.3. DESIGN CONSIDERATION

Increasing the frame rate of an image sensor can be achieved by improving the performance of the analog-to-digital converter (ADC) designed within the sensor or by increasing the number of ADCs. However, high frame rate operation not only affects the image quality of the sensor but also influences the operational behavior of the system that controls the sensor. Therefore, the factors discussed below are essential considerations for increasing the frame rate of an image sensor.

First, it is essential to consider the characteristics of the data required by the system. In various conditions, such as location, illumination, and object behavior, the image sensor acquires data with different characteristics depending on its application. In the case of the advanced driver assistance system (ADAS), the image sensor aims to provide accurate information to the system. For example, when a car is leaving a tunnel, the contrast of light becomes extremely high, as shown in Figure 1.4 [15]. In this condition, the ADAS system utilizes an image sensor with high dynamic range, ensuring accurate information delivery even during leaving the tunnel. Consequently, research has been conducted on relevant characteristics [16], [17], [18]. On the other hand, the dynamic vision sensor (DVS) focuses on fast scanning of the surrounding environment. Particularly, when tracking moving objects, the DVS pixel array can quickly perceive the position of the moving object by receiving 1-bit data from each pixel, even if the object's motion is rapid. Moreover, since DVS generates 1-bit data, it does not require an ADC, and the sys-

tem is specialized for such operations. Instead, extensive research has been conducted on algorithms related to analyzing the acquired data to efficiently identify rapidly changing positions [19].

Second, the performance related to the image quality, such as temporal noise and fixed pattern noise (FPN), must be considered. If the ADC sampling rate increases to enhance the frame rate, the bandwidth of each readout channel inevitably increases. A larger bandwidth directly leads to worse temporal noise performance. On the other hand, if the number of ADC increases in limited space to enhance the frame rate, the FPN performance inevitably degrades. Especially in some of the research, the SAR ADC or Sigma-delta ADC has been designed to improve the sampling rate instead of a single-slope ADC. In this case, though the sampling rate improved due to the efficient algorithm, temporal noise and FPN performance degraded together due to the area occupied by the SAR ADC [20], [21], [22]. Therefore, a sensor structure review and the analysis of the noise performance are mandatory.

Third, the data managing speed at each block on the data path must be considered. Since there are many blocks on the data path, such as the pixel array, the signal processing block and the interface, these blocks must have the same data rate. For example, if 1000 ADCs work at 100kS/s, the pixel array must have a 1GHz speed. In addition, the same number of data also must be sent to the system at the same speed. The interface speed has to be 1 Gb/s. Since each communication does not have the same number of channels, the data processing speed must be managed.

As shown above, many factors must be considered to implement a high frame rate image sensor. Therefore, this consideration must be the first step in designing an image sensor.

1.4. RESEARCH DIRECTION

In this project, the solution to enhance the frame rate of an image sensor has been studied. To increase the frame rate of an image sensor efficiently, this research has been performed in the following two research directions.

First, this work enhances the frame rate by improving the pixel rate. As mentioned above, increasing the number of ADCs inside the image sensor and the ADC sampling rate are direct solutions. In particular, some of the research [23], [24] proved that increasing the number of ADCs can have a higher pixel rate with a lower ADC sampling rate. Another research [25] proved that improving the ADC performance can enhance the pixel rate. In this work, a SAR ADC has been designed. The SAR ADC is an appropriate solution to improve the frame rate of the image sensor due to its simple algorithm. The SAR ADC has the best figure-of-merit (FOM) in the range from 100kS/s to 10MS/s [26]. In addition, the SAR ADC requires a slow clock which can improve the system power efficiency. However, this design still has the issues mentioned above. Therefore, the SAR ADC has been designed in a column-parallel structure to suppress the bandwidth. In the meantime, an FPN compensation technique has been suggested to improve the FPN performance.

Second, an application dedicated image sensor can contribute to increasing the frame rate. In order to increase the frame rate by increasing the pixel rate, the image sensor requires an assumption of infinite data transmission speed. However, in the actual de-

sign, a physical speed limitation from the interface, such as camera link, MIPI D-PHY and SLVS-EC, transmitting data is obvious. In these conditions, reducing the amount of data by selecting valuable data within the whole image data is inevitable to increase the frame rate. Therefore, selecting valid data within the full image data is implemented by designing a reconfigurable system in this thesis. In this project, the image sensor control system sets a 10x10 pixels window, called a region of interest (ROI), around the object. Since the number of image data within the ROI region is only 100 pixels, an entire image can be generated by reading out only data located in the ROI region, and the frame rate can be enhanced without increasing the ADC sampling rate. In particular, the ROI mode works together with the normal mode because the ROI region can be set after analyzing full image data.

Therefore, to implement the high frame rate operation, implementing a reconfigurable system, which changes the image sensor operation mode between ROI mode and the normal mode periodically, is inevitable.

1.5. THESIS OUTLINE

The organization of this thesis is as follows.

Chapter 2 presents the design of some basic circuit blocks, such as the row decoder, reference generator and LVDS interface. In particular, 2 image sensors have been designed in this thesis, and these 2 image sensors share these basic circuit blocks. Therefore, a block diagram overview and the timing diagram of these basic blocks are provided in this chapter.

Chapter 3 gives the readout algorithm and the noise analysis of the analog front end. As mentioned above, a column-parallel SAR ADC has been designed based on a 2-step data conversion algorithm. Therefore, a noise analysis and a FPN calibration algorithm are suggested.

Chapter 4 presents the practical design of a column-parallel SAR ADC. Based on the theoretical analysis in the previous chapter, the SAR ADC structure and the timing will be discussed. In particular, the circuit design for a FPN calibration and layout method to improve the capacitor DAC linearity are depicted.

Chapter 5 discusses the analysis of the physical speed limitation when implementing a high-frame image sensor by increasing the pixel rate. In addition, the detailed algorithm to select valid data after capturing an entire image is described, and the system design to support a reconfigurable system is explained.

Chapter 6 presents a practical design to implement the reconfigurable system. In particular, the intelligent switch box is additionally designed, and this switch box appropriately distributes the data to the proper ADC. The sensor control timing and operation mode switching method will be discussed in detail.

Chapter 7 shows the measurement result in this system. Since a FPGA is used in the measurement, the PCB design, including the FPGA, is shown in this chapter. In the end, the measurement result will be discussed. Based on the measurement result, a performance comparison is suggested.

Finally, chapter 8 discussed the conclusion of this project and the future work.

1

REFERENCES

[1] R. Schaller, "Moore's law: Past, present and future," *IEEE Spectrum*, vol. 34, no. 6, pp. 52–59, Jun. 1997. DOI: 10.1109/6.591665.

[2] TSMC, *Comprehensive portfolio of foundry process technologies dedicated to tsmc logic technology*, Accessed 1st July, 2023, 2023. [Online]. Available: https://www.tsmc.com/english/dedicatedFoundry/technology/logic.

[3] M. Uchiyama et al., "A 40/22nm 200mp stacked cmos image sensor with 0.61um pixel," in *2021 International Image Sensor Workshop (IISW)*, Online, 2021, pp. 5–8.

[4] D. Im et al., "0.64μm-pitch cmos image sensor with low leakage current of vertical transfer gate," in *2021 International Image Sensor Workshop (IISW)*, Online, 2021, pp. 9–12.

[5] D. Kim, "Development of 0.5 μm pixel 3-wafers stacked cmos image sensor with through silicon deep contact and in-pixel cu-cu bonding process," in *2024 IEEE Electronic Components and Technology Conference (ECTC)*, Denver, CO, USA, 2024, pp. 394–397. DOI: 10.1109/ECTC51529.2024.00070.

[6] T. Cools et al., "An sxga cmos image sensor with 8 gbps lvds serial link," in *2007 International Image Sensor Workshop (IISW)*, Ogunquit, ME, USA, 2007, pp. 45–48.

[7] T. Toyama et al., "A 17.7mpixel 120fps cmos image sensor with 34.8gb/s readout," in *2011 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2011, pp. 420–422. DOI: 10.1109/ISSCC.2011.5746379.

[8] Y. Nitta et al., "High-speed digital double sampling with analog cds on column parallel adc architecture for low-noise active pixel sensor," in *2006 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2006, pp. 2024–2031. DOI: 10.1109/ISSCC.2006.1696261.

[9] Y. Lim et al., "A 1.1e- temporal noise 1/3.2-inch 8mpixel cmos image sensor using pseudo-multiple sampling," in *2010 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2010, pp. 396–397. DOI: 10.1109/ISSCC.2010.5433971.

[10] H. Wakabayashi et al., "A 1/2.3-inch 10.3mpixel 50frame/s back-illuminated cmos image sensor," in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2010, pp. 410–411. DOI: 10.1109/ISSCC.2010.5433963.

[11] S. Sukegawa et al., "A 1/4-inch 8mpixel back-illuminated stacked cmos image sensor," in *2013 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2013, pp. 484–485. DOI: 10.1109/ISSCC.2013.6487825.

[12] T. Haruta et al., "4.6 a 1/2.3inch 20mpixel 3-layer stacked cmos image sensor with dram," in *2017 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2017, pp. 76–77. DOI: 10.1109/ISSCC.2017.7870268.

[13] Y. Kim et al., "A 1/2.8-inch 24mpixel cmos image sensor with 0.9μm unit pixels separated by full-depth deep-trench isolation," in *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2018, pp. 84–86. DOI: 10.1109/ISSCC.2018.8310195.

[14] Hitachi, *Advanced driver assistance system*, Accessed 1st July, 2023, 2016. [Online]. Available: https://www.hitachi-automotive.us/Products/oem/DCS/ADAS/index.htm.

[15] Samsung, *Automotive image sensor products*, Accessed 1st July, 2023, 2021. [Online]. Available: https://semiconductor.samsung.com/image-sensor/automotive-image-sensor.

[16] T. Kim, "Wide dynamic range technologies: For mobile imaging sensor systems," *IEEE Consumer Electronics Magazine*, vol. 3, no. 2, pp. 30–35, 2014. DOI: 10.1109/MCE.2014.2298072.

[17] M. Innocent et al., "Automotive 8.3 mp cmos image sensor with 150 db dynamic range and light flicker mitigation," in *2021 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2021, pp. 30.2.1–30.2.4. DOI: 10.1109/IEDM19574.2021.9720683.

[18] M. Mase et al., "A wide dynamic range cmos image sensor with multiple exposure-time signal outputs and 12-bit column-parallel cyclic a/d converters," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, pp. 2787–2795, 2005. DOI: 10.1109/JSSC.2005.858477.

[19] H. Leow et al., "Machine vision using combined frame-based and event-based vision sensor," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, Portugal, 2015, pp. 706–709. DOI: 10.1109/ISCAS.2015.7168731.

[20] R. Funatsu et al., "6.2 133mpixel 60fps cmos image sensor with 32-column shared high-speed column-parallel sar adcs," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2015, pp. 1–3. DOI: 10.1109/ISSCC.2015.7062951.

[21] D. Chen et al., "A 64 fj/step 9-bit sar adc array with forward error correction and mixed-signal cds for cmos image sensors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 11, pp. 3085–3093, 2014. DOI: 10.1109/TCSI.2014.2334852.

[22] S. Hwang et al., "A 2.7-m pixels 64-mw cmos image sensor with multicolumn-parallel noise-shaping sar adcs," *IEEE Transactions on Electron Devices*, vol. 65, no. 3, pp. 1119–1126, 2018. DOI: 10.1109/TED.2018.2795005.

[23] T. Watabe et al., "A 33mpixel 120fps cmos image sensor using 12b column-parallel pipelined cyclic adcs," in *2012 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2012, pp. 388–390. DOI: 10.1109/ISSCC.2012.6177047.

[24] M. Sakakibara et al., "A back-illuminated global-shutter cmos image sensor with pixel-parallel 14b subthreshold adc," in *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2018, pp. 80–82. DOI: 10.1109/ISSCC.2018.8310193.

[25] T. Yasue et al., "A 33mpixel cmos imager with multi-functional 3-stage pipeline adc for 480fps high-speed mode and 120fps low-noise mode," in *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2018, pp. 90–92. DOI: 10.1109/ISSCC.2018.8310198.

[26] P. Harpe, "Low-power sar adcs: Basic techniques and trends," *IEEE Open Journal of the Solid-State Circuits Society*, vol. 2, pp. 73–81, 2022. DOI: 10.1109/OJSSCS.2022.3211482.

2

THE BASIC IMAGE SENSOR DESIGN AND ITS TIMING

The image sensor requires multidisciplinary research and knowledge from various fields. In particular, the image sensor consists of various blocks, such as a row decoder, reference generator, interface, pixel array, and ADC. For this reason, it is tough to explain the image sensor operation based on the data conversion procedure due to the complicated system of the image sensor. In addition, controlling all of these blocks is very complicated. For this reason, in the industrial area, many companies have improved the system based on the system developed by Nokia [1]. This system supports several functions, such as controlling pixels in the appropriate address, generating reference current and voltage, transmitting data through the interface, and distributing appropriate clocks to each block. This work also has a similar system design to [1].

In this project, 2 image sensors have been designed and, based on the measurement result, research has been performed. In particular, the essential functions mentioned above are shared in both designs. Therefore, a detailed hardware implementation, including the timing of each signal behavior, is described in this chapter.

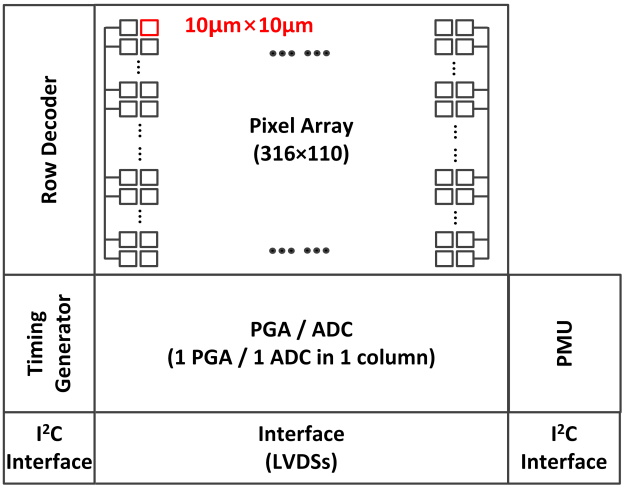


Figure 2.1: Block diagram of the image sensor architecture

2.1. IMAGE SENSOR ARCHITECTURE OVERVIEW

2.1.1. BLOCK DIAGRAM OVERVIEW

Figure 2.1 shows the block diagram of the image sensor architecture designed in this work. This sensor has a 5mm × 5mm size, including 144 I/O pads. Considering the chip size and the other circuit design area, this project uses a 316×110 pixel array, and each pixel has a 10μm pitch size. This pixel array is controlled by the row decoder located at the left side of the pixel array. Since this sensor employs a column-parallel structure, the analog front end consists of 316 ADCs and 316 programmable gain amplifiers (PGAs). Moreover, LVDSs are used as an interface to the outside world. In this project, 12 channels are designed. The timing generator mainly controls the various circuit blocks inside the image sensor, and this block also supports distributing the clock to each block.

In this project, a 300×90 pixel array is used as an effective pixel out of a 316×110 pixel array. Considering the mismatch of the pixel, the top 10 lines and bottom 10 lines are used as dummy pixels, and the left 8 columns and right 8 columns are also used as dummy pixels. The row decoder controls the pixels located at the address after decoding the vertical domain address (VDA). This VDA is a 7-bit digital code, and the row decoder requires 2 VDAs, which define the address for the read and the shutter operation. The pixel requires various reference voltages, which define the scale of signals that control each component within the pixel, such as the reset gate and sampling switch. These reference voltages are provided from the outside of the chip. In the analog front-end part, 316 ADCs are used to convert the analog output from the pixel, and the maximum ADC sampling rate is up to 250kS/s. In addition, this sensor can control the analog gain by controlling the PGA, which provides an analog gain of up to ×8. The reference generator provides the reference voltage to support the ADC and PGA operation. This reference generator creates the reference voltages using a BGR (Bandgap Reference). As mentioned above, this sensor uses an LVDS interface to transmit the data to the FPGA.

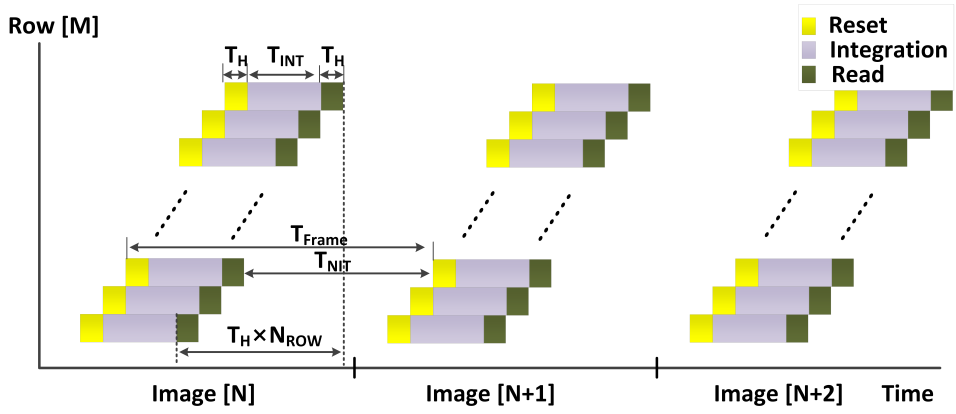


Figure 2.2: Pixel readout order

Since the 180nm process cannot support a high-speed operation, the maximum data rate is about 120Mb/s per channel.

2.1.2. PIXEL READOUT SEQUENCE AND TIMING

In this work, the image sensor is working in a rolling shutter mode [2]. Though the rolling shutter mode is relatively vulnerable to the motion artifact, the sensor can efficiently read the pixel with efficient timing compared to the global shutter mode [3]. Figure 2.2 shows the timing diagram of the pixel readout. In Figure 2.2, T_{H} refers to a single horizontal line time, the same as the time required to convert the 1-pixel output in this work. T_{NIT} and T_{NIT} give the charge integration time or the time between the read and the shutter, respectively. T_{FRAME} is the time for generating a single image, and the T_{FRAME} is calculated by the formula below.

$$T_{\mathrm{FRAME}} = T_{\mathrm{H}} + T_{\mathrm{INT}} + T_{\mathrm{NIT}} \tag{2.1}$$

In the rolling shutter mode, the image sensor reads each pixel line sequentially, and this image sensor reads 90 lines out of the 110 lines due to the dummy pixel lines at the top and bottom. The Verilog code in this work controls the address for selecting pixels.

As mentioned in section 2.1.1, 2 image sensors have been designed for this project. Both designs have slightly different ADC structures. However, sampling and data conversion timing are the same in each design since the same pixel structure has been used in both versions. Figure 2.3(a) and (b) show the PGA and ADC block diagrams of the first and second designs, respectively. In the first design, a PGA and 10-bit SAR ADC are designed. In the second version, a 2-step SAR ADC has been designed using a 6-bit ADC and the PGA.

Figure 2.3(c) gives the timing diagram of controlling the ADC within a single horizontal line time. When the horizontal line time starts after VDA is transmitted, the pixel outputs the reset level, $V_{\mathrm{PIX\_RST}}$ and the ADC starts sampling. Therefore, the PGA sam-

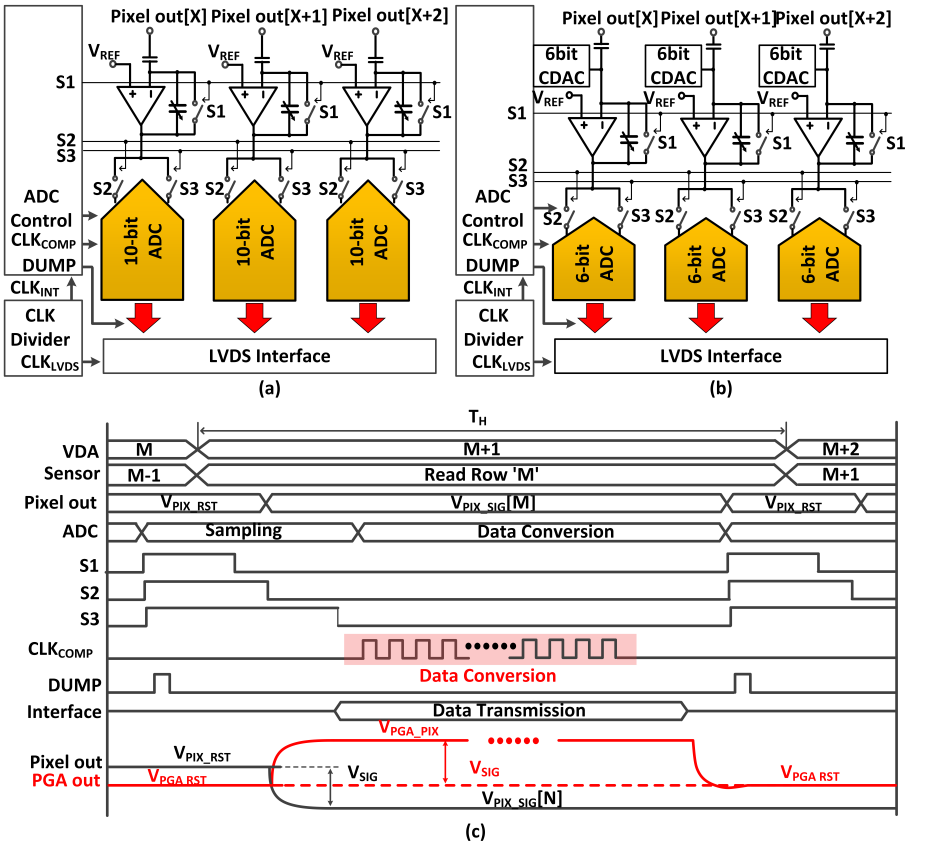


Figure 2.3: ADC and PGA block diagram of (a) 1st design and (b) 2nd design, and (c) timing diagram within 1 horizontal line time

ples the pixel output, $V_{\text{PIX\_RST}}$, and resets itself by simultaneously turning on the switch S1. In addition, The ADC starts sampling the output of the PGA, $V_{\text{PGA\_RST}}$, by turning on S2 and S3. When the reset level sampling is completed, switch S1 and S2 are sequentially turned off, and the pixel output its integrated signal, $V_{\text{PIX\_SIG}}$. After sampling the integrated signal, $V_{\text{PIX\_SIG}}$, the ADC turns off the switch S3 and starts 10-bit data conversion. In the meantime, the clock to control the comparator is applied to support data conversion. After data conversion, the ADC generates the final digital code in each column. This final digital code is transmitted to the interface at the rising edge of DUMP.

2.2. ROW ACCESS THROUGH ROW DECODER

2.2.1. PIXEL STRUCTURE AND PIXEL CONTROL TIMING

Figure 2.4 shows a circuit diagram of the pixel array and a single pixel included in a pixel array. As seen in Figure 2.4, the pixel array is composed of multiple pixels. Par-

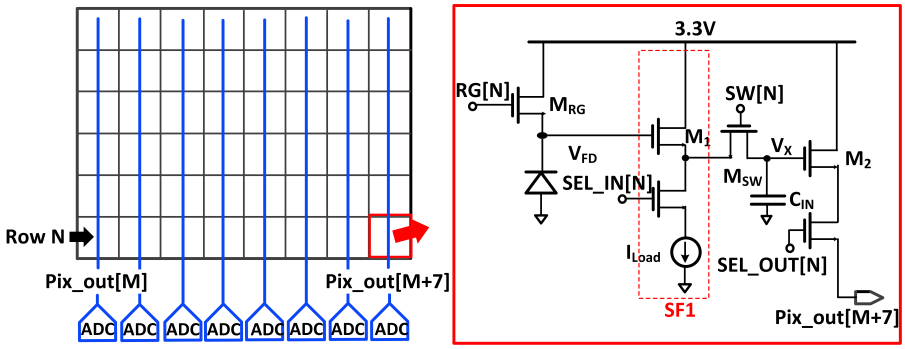


Figure 2.4: A circuit diagram of pixel array (left) and a single pixel included in a pixel array (right)

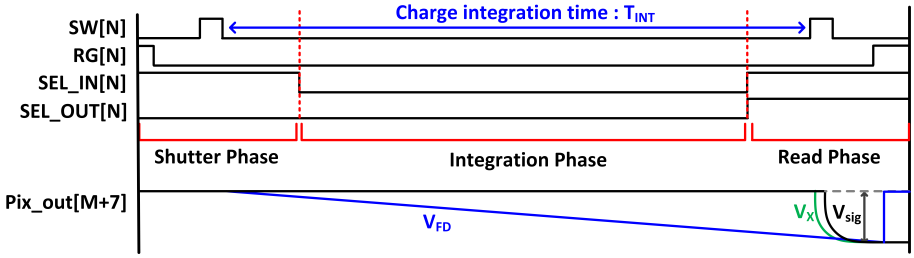


Figure 2.5: Timing diagram example for controlling a single pixel

ticularly, when the image sensor operates in normal mode, the output of each pixel in each column is connected to one output line, and these output lines are connected to the inputs of ADCs, with one ADC placed per column. In addition, each individual pixel contained in the pixel array has a circuit diagram shown in the figure. Figure 2.4 illustrates that the sensor generates signals using a 3T-type pixel, which is designed with 3 transistors and 1 photodiode. The 3T-type pixel offers a speed advantage over the 4T-type pixel, which is designed with 4 transistors and 1 photodiode. However, the 3T-type pixel exhibits worse temporal noise performance when compared to the 4T-type pixel. In order to keep the advantage of the 3T-type pixel with better temporal noise performance, the sampling network and additional buffer, SF1, are included in the pixel structure, as shown in Figure 2.4.

Figure 2.5 shows the timing diagram of controlling pixel described in figure 2.4. As described in Figure 2.5, the pixel control procedure consists of three phases: shutter, charge integration, and read. First, in the shutter phase, the row decoder turns on the reset gate, M_{RG}, to reset the pixel before the photodiode starts integrating the charge. After the pixel reset, the row decoder turns off the reset gate, M_{RG}, by controlling the signal RG[N], and then samples the reset level of the pixel on the sampling capacitor C_{IN} by turning on the switch M_{SW}. The capacitor C_{IN} preserves the sampled reset level until the read phase. In the meantime, the photodiode starts integrating the charge generated by the incoming light. The holding time of the sampled reset level is equal to the integra-

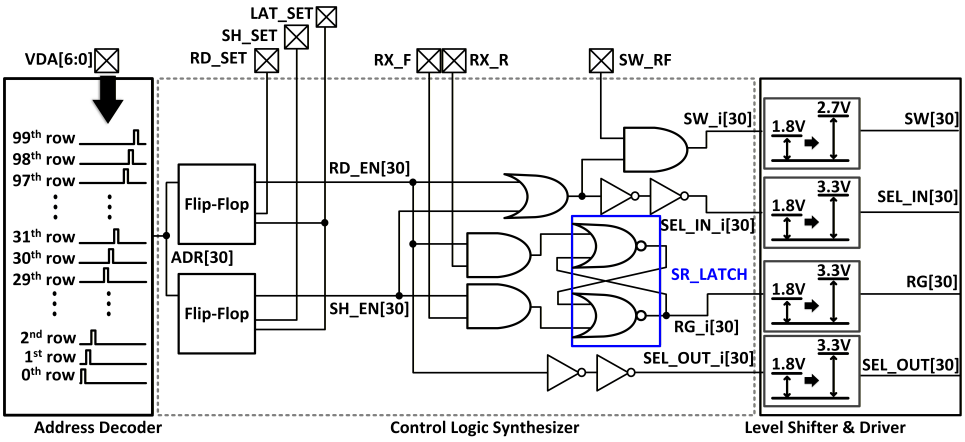


Figure 2.6: A block diagram overview of the row decoder, including a detailed logic synthesizer example of the 30-th row

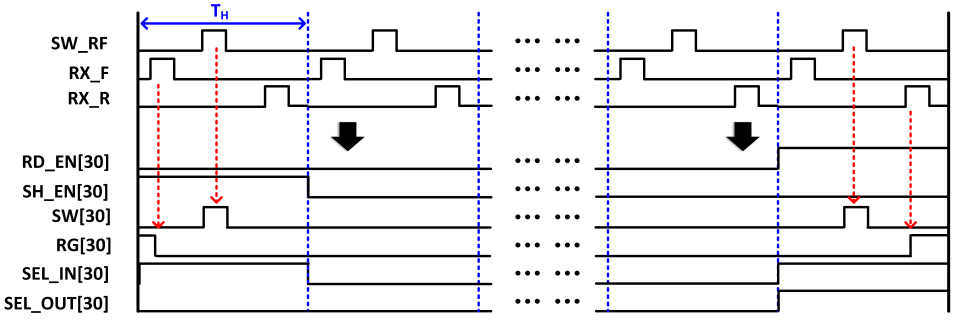


Figure 2.7: The timing diagram of the logic synthesizer

tion time, T_{INT}. In the read phase, the reset level preserved on C_{IN} is output to the PGA first through the output of the source follower, V_{PIX_OUT}. Next, the integrated signal is sampled on the C_{IN}, and this sampled integrated signal is also output to the PGA after reset level sampling. In the shutter and the read phase, since the signals from the photodiodes are output through an internal source follower (SF1), as shown in Figure 2.4, the current sources must be activated. Therefore, only the current sources of the two rows in the shutter and the read phase work at every horizontal line time to reduce power consumption.

2.2.2. ROW DECODER OVERVIEW AND SIGNAL SYNTHESIS

The Row Driver and Decoder (RDV) block generates pixel-control signals and delivers them to the pixel row designated by the vertical domain address (VDA). Once the 7-bit VDA code is received from the timing generator, the RDV activates the corresponding

row and drives it through the appropriate control pulses for the shutter or read operation.

Figure 2.6 shows the overall architecture of the RDV. As illustrated in Figure 2.6, the RDV consists of three functional sub-blocks: the address decoder, the control logic synthesizer, and the level shifter and driver, each responsible for generating and distributing pixel-control signals to the corresponding row. The address decoder receives the 7-bit VDA code from the timing generator and interprets it to select a single pixel row. It asserts one of its outputs to logic high (ADR[N]), corresponding to the row specified by the VDA. For example, when the 7-bit VDA code "0011110" is transmitted, the address decoder activates ADR[30], which represents Row 30. This activation signal is then forwarded to the control logic synthesizer.

The control logic synthesizer forms the core of the RDV, where the actual pixel-control signals are generated. The synthesizer receives the activation signal ADR from the address decoder and processes it through two flip-flops, each dedicated to the shutter and read operations, respectively. As shown in Figure 2.6, the flip-flops are controlled by three global timing signals from the timing generator: SH_SET, RD_SET, and LAT_SET. The signals SH_SET and RD_SET capture the activation signal ADR for the shutter and read operations, respectively, while LAT_SET triggers the flip-flops at the beginning of each horizontal line time to generate SH_EN and RD_EN. These enable signals remain high during one line period and activate the corresponding row for the shutter or read operation. All three timing signals (SH_SET, RD_SET, and LAT_SET) are globally distributed to every row within the RDV.

Once the enable signal (SH_EN or RD_EN) is asserted, the RDV synthesizes the pixel-control signals according to the timing diagram shown in Figure 2.7. The synthesizer combines the periodic control clocks RX_R, RX_F, and SW_RF, also supplied by the timing generator, with the enable signals to generate the pixel-driving waveforms. During the shutter operation, the SH_EN signal activates the pixel row, and SW_RF is directly forwarded to control the sampling switch, while RX_F controls the SR-latch to generate the reset-gate (RG) signal. In this timing, RX_R is ignored. Conversely, during the read operation, the RD_EN signal activates the corresponding row, SW_RF is again forwarded directly, and RX_R drives the SR-latch to produce RG, while RX_F is ignored. This selective combination of timing signals ensures proper sequencing between the shutter and read phases.

Figure 2.7 illustrates the resulting waveforms for Row 30, showing how the pixel is reset and integrates during the shutter phase and subsequently read out during the read phase. This architecture allows each selected row to autonomously generate its own control waveforms using the shared global timing references, ensuring both precise timing alignment and efficient hardware implementation.

The level shifter and driver stage finally convert these synthesized 1.8 V digital logic signals to higher voltage levels (2.7 V / 3.3 V) required by the pixel array. This stage provides sufficient voltage swing to fully drive the pixel transistors and isolates the analog and digital power domains. The driver also enhances power efficiency and minimizes noise coupling through the shared bias lines, ensuring stable operation of the pixel array during high-speed readout.

2.2.3. VDA CONTROL AND TIMING

To ensure that only the intended pixel row receives the control signals generated by the RDV, it is essential to correctly activate the RD_EN and SH_EN signals. This activation is managed by a flip-flop circuit, which determines when and how each row is enabled during the shutter and read phases. Proper control of this flip-flop guarantees both timing synchronization and accurate row selection, which are critical for avoiding image distortion or unintended pixel activation.

The use of a flip-flop offers two main advantages. First, it ensures a fixed trigger timing independent of the propagation delay of the vertical address (VDA) bits. Without this synchronization, slight delay mismatches among the VDA lines could momentarily activate unintended rows. By latching the decoded address through the flip-flop, the RDV prevents these transient activations and maintains precise pixel-level control. Second, because the system operates in a time-multiplexed manner, the same VDA bus is reused for both the shutter and read operations. Whether the captured address is used for the shutter or the read phase is decided by distinct global set signals (SH_SET or RD_SET), while the line-start strobe LAT_SET synchronizes the update. Consequently, even though the two flip-flops per row receive the same ADR[N] and share LAT_SET, their different set inputs make SH_EN[N] and RD_EN[N] assert in different line periods (cf. Fig. 2.7).

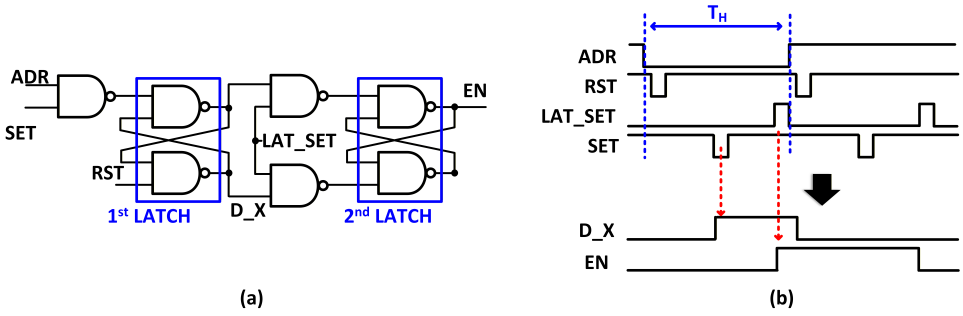


Figure 2.8: (a) Flip-flop circuit diagram with two cascaded NAND-latch stages controlled by SET, RST, and LAT_SET; (b) corresponding timing. The first latch captures ADR when SET (SH_SET or RD_SET) is high, after being reset by RST at the start of each line. The second latch outputs EN (SH_EN or RD_EN) on the rising edge of LAT_SET. While LAT_SET=0, both NAND outputs of the second latch are held at logic 1, so no race occurs and timing is deterministic.

Figure 2.8 details the internal flip-flop and its timing. The first latch temporarily stores the activation data (ADR) when SET is asserted. Here, SET corresponds to either SH_SET or RD_SET, depending on the intended operation. Before capturing the new VDA, the RST signal resets the first latch at the beginning of each horizontal line time, ensuring that any residual activation from the previous line is cleared (see Fig. 2.9). The second latch is gated by LAT_SET; when LAT_SET rises at the next line start, the stored data D_X is transferred to EN. Because the second stage is disabled while LAT_SET=0 (both NAND outputs held high), and enabled only on its rising edge, there is no competition between the two NAND gates and no metastability on the falling edge—EN updates deterministi-

cally once per line.

In the actual implementation, two flip-flops are allocated to each row: one for the shutter phase and one for the read phase. As illustrated in Figure 2.6, the address-decoder output ADR is combined with the global control signals SH_SET, RD_SET, and LAT_SET to generate the corresponding SH_EN and RD_EN. During operation, each enable signal remains active for one horizontal line time, allowing the control-logic synthesizer in the RDV (Section 2.2.2) to generate the appropriate pixel-level control waveforms such as the reset-gate (RG) and sampling-switch (SW[N]) signals.

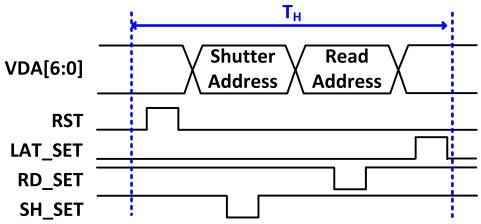


Figure 2.9: Timing diagram of the row-decoder control signals within one line period. RST resets the first latch exactly at the line start; SET (SH_SET or RD_SET) captures ADR; LAT_SET then propagates it to EN at the next line start.

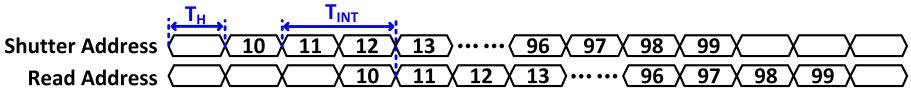


Figure 2.10: Example of VDA sequences for shutter and read within one frame. The time offset between the shutter-VDA capture and the read-VDA capture equals the integration time T_{INT}.

Figure 2.9 summarizes the signal relationship within a single line period. RST always triggers at the line start to initialize the first latch. Then SET (SH_SET or RD_SET) captures the active ADR into the first latch, and LAT_SET transfers it to the second stage at the beginning of the next line. Thus, SH_EN and RD_EN are asserted in different line slots even though both flip-flops share the same ADR and LAT_SET. During full-frame operation, the FPGA provides the shutter- and read-VDA sequences in ascending order on the same bus; the time difference between their captures equals T_{INT} (Fig. 2.10), ensuring uniform exposure and consistent readout timing across the frame.

2.3. REFERENCE GENERATOR USING BGR

2.3.1. GENERATING REFERENCE CURRENT AND VOLTAGE

Figure 2.11 shows the block diagram of the reference generator. In this work, the BGR, which has a well-known structure, is used to generate the reference current and voltage. As described in Figure 2.11, the BGR generates 1V output, V_{BGR}, which is transmitted to the regulator. Due to the negative feedback loop, the potential at the positive input of the amplifier, V_{LDO}, follows V_{BGR}. As a result, the regulator generates the current flowing at the load resistor R_{REF} is V_{BGR}/R_{REF}. Since the transistor M_P has the multiplication

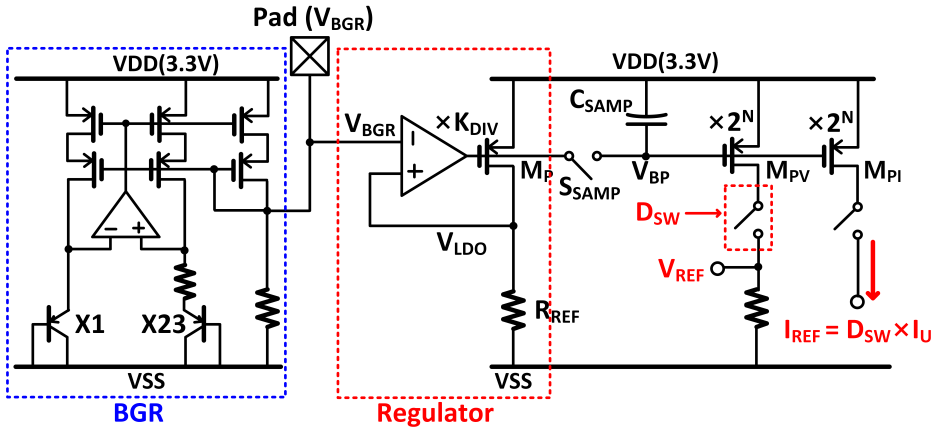


Figure 2.11: The circuit block diagram of the reference generator

number K_{DIV}, the unit current of the current source, I_{U}, is calculated as follows.

$$I_{\mathrm{U}} = \frac{V_{\mathrm{BGR}}}{R_{\mathrm{REF}} \times K_{\mathrm{DIV}}} \tag{2.2}$$

In addition, the number of the current sources turned on is managed by the N-bit digital code, D_{SW}. The generated output current I_{REF} is shown below.

$$I_{\mathrm{REF}} = I_{\mathrm{U}} \times D_{\mathrm{SW}} = \frac{V_{\mathrm{BGR}} \times D_{\mathrm{SW}}}{R_{\mathrm{REF}} \times K_{\mathrm{DIV}}} \tag{2.3}$$

In this work, R_{REF} and K_{DIV} are 10 kΩ and 40, respectively, and the I_{U} is 2.5μA. In order to improve the temporal noise, this reference generator samples the bias voltage, V_{BP}, at the sampling capacitor, C_{SAMP}. Considering the sampled temporal noise, the mathematical calculation of the power spectral noise density (PSD), $I_{\mathrm{PSD,REF}}$, at the output of the current source follows the formula below.

$$I^2_{\mathrm{PSD,REF}} \approx 4kT\gamma g_{m,\mathrm{PI}} \tag{2.4}$$

In particular, since the sampling capacitor is 10pF in this work, the temporal noise from the regulator and the BGR is negligible due to the limited bandwidth of the regulator.

In this work, the output of the BGR, V_{BGR}, is constantly monitored through a pad, which is connected to the outside world. Since the reference current is proportional to the V_{BGR}, the actual circuit operating condition can be estimated by comparing the output of the V_{BGR}.

2.3.2. PROVIDING REFERENCE CURRENT TO SF AND PGA

Figure 2.12 shows the circuit block diagram generating a reference voltage for the source follower. The reference current $I_{\mathrm{REF\_SF}}$ is generated by the method introduced

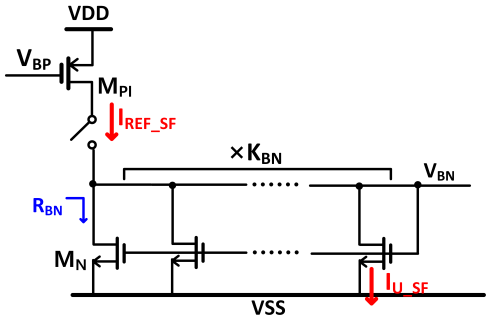


Figure 2.12: The circuit diagram generating reference voltage for the source follower

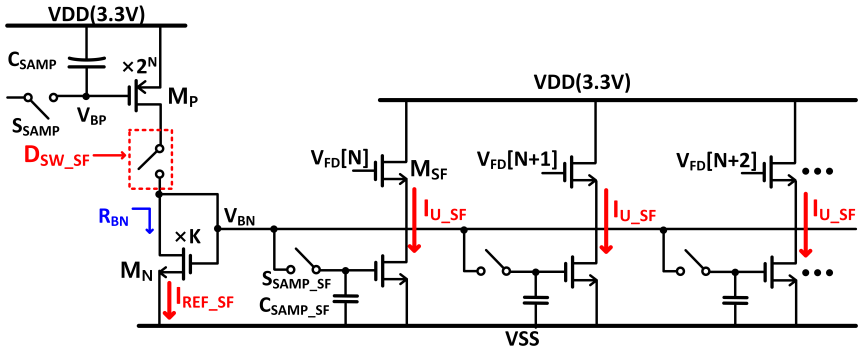


Figure 2.13: The bias sampling circuit organized within each column

in section 2.3.1. The reference current, $I_{\mathrm{REF\_SF}}$, is divided by the multiplication number K_{BN} in Figure 2.12. As a result, the reference voltage V_{BN} is generated, and this reference voltage is transmitted to the source follower located at the output of the pixel array. The unit current that is supposed to be generated at each source follower is calculated below.

$$I_{U_{\mathrm{SF}}} = \frac{I_{\mathrm{REF\_SF}}}{K_{\mathrm{BN}}} \tag{2.5}$$

In addition, the PSD included within the reference voltage, V_{BN}, follows the formula below.

$$\begin{aligned} V^2_{\mathrm{PSD,BN}} &= I^2_{\mathrm{REF\_SF}} \cdot R^2_{\mathrm{BN}} + 4kTR_{\mathrm{BN}} \\ &= 4kT\gamma g_{m,\mathrm{PI}} \left(\frac{1}{g_{m,\mathrm{N}}}\right)^2 + \frac{4kT}{g_{m,\mathrm{N}}} \\ &= 4kT\left(\frac{\gamma g_{m,\mathrm{PI}}}{g^2_{m,\mathrm{N}}} + \frac{1}{g_{m,\mathrm{N}}}\right) \end{aligned} \tag{2.6}$$

As shown in the equation, the output impedance, R_{BN}, at the node V_{BN} must be small

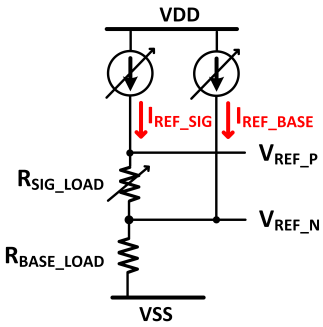


Figure 2.14: The example of the reference voltage generator using the variable resistors

enough to suppress the noise included in the reference voltage. In order to reduce the output impedance, R_{BN}, a larger current with a higher multiplication number K_{BN} is required. In this work, the maximum I_{REF_SF} is 1.28mA, and the reference current, I_{REF_SF}, is controlled by the register written by inter integrated circuit (I^2C) interface.

Though the PSD is relatively negligible compared to the PSD of ADC, the temporal noise from the reference circuit can degrade the horizontal temporal noise performance. Since the temporal noise on the bias voltage affects the current level of the whole source follower in the same direction simultaneously, the gain of the source follower can be different in each horizontal line readout time. The different gain source followers in each horizontal line time can make each line flicker randomly on the captured image even though the same input signal is applied.

In order to avoid this flickering, the bias sampling method [4] is applied. Figure 2.13 gives the bias sampling circuit to suppress the horizontal temporal noise. In each column, a sampling capacitor C_{SAMP_SF} is located. The bias voltage is sampled at the end of each horizontal line time. As a result, this bias sampling technique changes the horizontal temporal noise into temporal noise.

2.3.3. PROVIDING REFERENCE CURRENT TO SF AND PGA

The reference generator uses 2 reference currents, I_{REF_SIG} and I_{REF_BASE}, to generate the reference voltages. These 2 reference currents use 2 load resistors, R_{SIG_LOAD} and R_{BASE_LOAD}, to generate the reference voltages. Figure 2.14 shows the circuit diagram of the reference generator. The generated reference voltages, V_{REF_P} and V_{REF_N}, are calculated as follows.

$$\begin{aligned} V_{REF\_N} &= R_{BASE\_LOAD} \cdot (I_{REF\_SIG} + I_{REF\_BASE}) \\ V_{REF\_P} &= R_{SIG\_LOAD} \cdot I_{REF\_SIG} + V_{REF\_N} \end{aligned} \tag{2.7}$$

In particular, the difference between V_{REF_P} and V_{REF_N} is the same as the ADC saturation level of the image sensor. In addition, the reference current I_{REF_BASE} is controlled to manage the maximum reference voltage of V_{REF_P} below 1.8V because the ADC uses a 1.8V power supply.

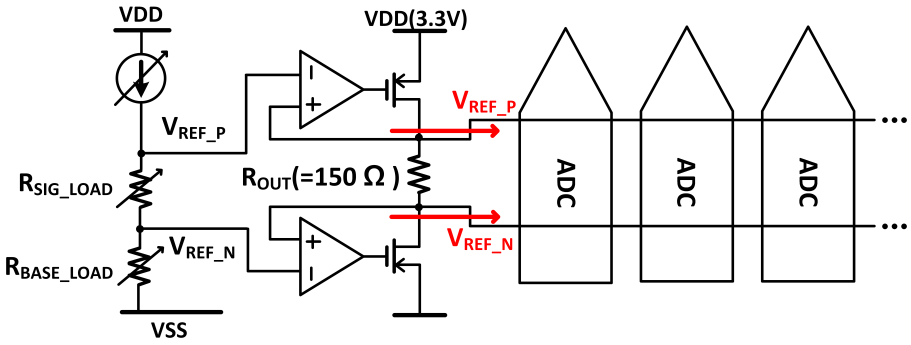


Figure 2.15: The circuit block diagram of the reference driver

In order to provide the reference voltage to the ADC array, the reference driver described in Figure 2.15 is used. Especially considering the SAR ADC operation in this work, the reference recovery has to be completed within a data decision cycle. In addition, the 6-bit SAR ADC spends 75% of the power in the first cycle, and this first cycle has to be used as a worst case in designing recovery time. In this work, 125ns is the shortest decision cycle. For this reason, the reference driver's load resistor, R_{OUT}, is set to 150Ω in the worst case.

2.4. CLOCK MANAGEMENT & INTERFACE CONTROL

2.4.1. CLOCK MANAGEMENT

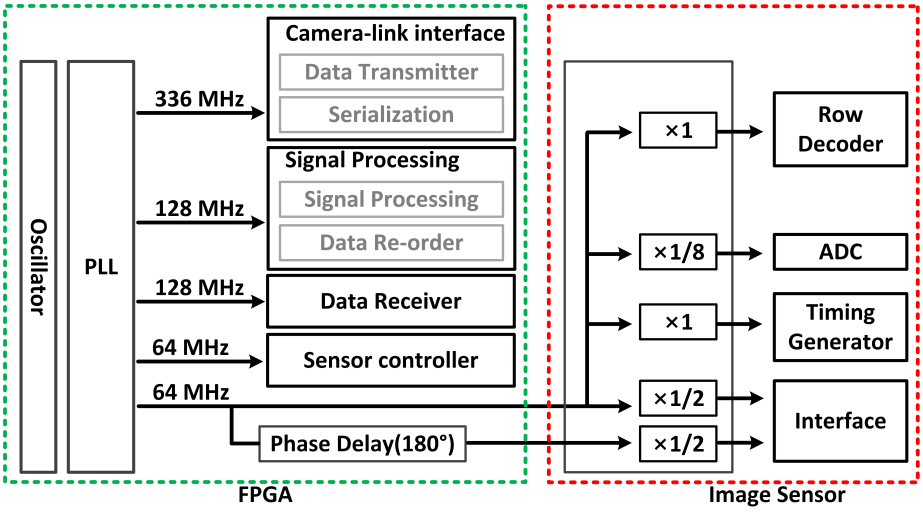


Figure 2.16: The block diagram of the clock tree

In this work, the FPGA XKCU035 from Xilinx has been used to control the sensor and handle the data output from the image sensor. Therefore, the sensor and the FPGA support various functions. Especially the clock for each block must have a different clock frequency because each operation requires a different data processing speed. Figure 2.16 shows the block diagram of the clock tree distributed to each block.

The main clock is generated from the oscillator embedded within the FPGA. The PLL inside the FPGA divides the frequency of the main clock to generate 3 clocks. These clocks have 336MHz, 128MHz and 64MHz frequencies, respectively. These clocks are transmitted to the Cameral-link interface, data receiver and the signal processing blocks, which use 336MHz and 128MHz clock, respectively. In addition, the distance between FPGA and the image sensor on the PCB board is relatively long. This long clock path can generate timing uncertainty. For this reason, to control the image sensor, the FPGA generates sensor control signals using a 64MHz clock, and some of the signals are generated inside the image sensor by receiving this 64MHz clock. In the image sensor, the clock divider generates 4 clocks for the row decoder, ADC, timing generator and interface, as depicted in Figure 2.16. Since the signals that require accurate control are generated inside the image sensor, the structure improves the uncertainty of the timing and the robustness of the image sensor operation.

2.4.2. THE SENSOR START-UP SEQUENCE

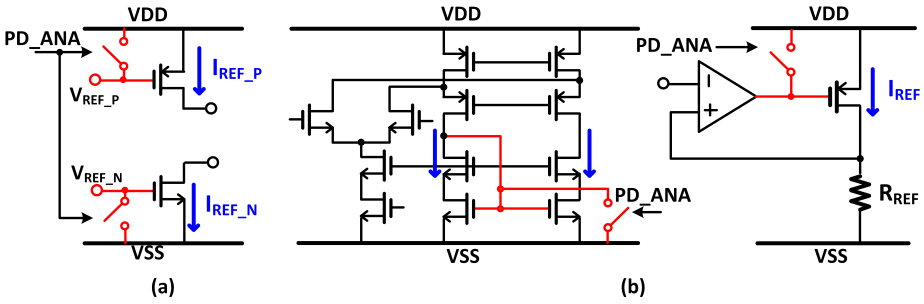


Figure 2.17: The example of reference block control in power down mode: (a) current sources, (b) the Amplifier and the regulator

When driving the sensor by applying power, an appropriate start-up sequence is required to guarantee the operation of the sensor. In particular, analog circuits, such as BGR or regulators, require a large amount of current if all circuits are simultaneously driven. For this reason, there is a risk that analog circuits, such as BGR and regulators, may malfunction.

This work uses 3 signals, such as PD_ANA, PD_DIG and INTIAL_SET, to control the image sensor's start-up sequence. First, PD_ANA is used to block the current path of the analog circuit in power-down mode. For instance, as described in Figure 2.17(a), the reference voltage of each current source is forced to ground or power, and the signal, PD_ANA, turns off the current sources. In the same way, the reference voltage of the amplifier is forced to ground and power to block the current path. In addition, if the

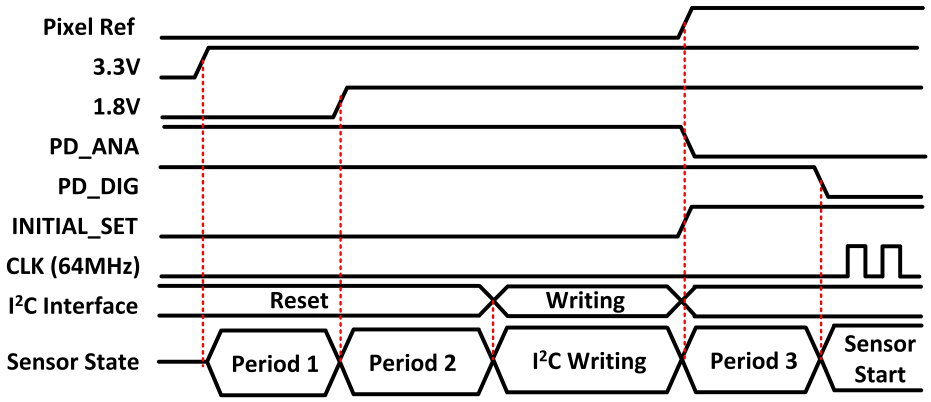


Figure 2.18: The timing diagram of the start-up sequence

amplifier is used in a regulator, the output of the amplifier is forced to power. The block diagram of Figure 2.17(b) shows the example. In this work, the BGR is the only block managed by the signal PD_ANA. Second, PD_DIG is used to reset the digital blocks, such as flip-flops and timing generators. Exceptionally, PD_DIG does not reset the I^2C register array when it is high. Third, INITIAL_SET triggers the analog circuit to start settling. Therefore, after the I^2C writing period, INITIAL_SET becomes high, and the analog circuits start settling. When INITAL_SET is low, the analog circuit blocks are automatically set to power-down mode.

Figure 2.18 shows the timing diagram of the start-up sequence. At the beginning of the start-up sequence, the PD_ANA and PD_DIG are set to high to put the sensor in power-down mode and reset the digital blocks. 3.3V power is first applied to the sensor in period 1. Then only the BGR starts settling, and the other analog circuit does not have a current path due to PD_ANA.

After the BGR settling, the 1.8V digital power is applied in period 2. In the meantime, the I^2C register blocks have to be reset. After the 1.8V power is applied, the FPGA starts writing code at the I^2C register array, and this code contains sensor operation mode and the register set-up for the reference circuit blocks. In period 3, the PD_ANA is set to ground to change the power-down mode to normal operation mode. In the meantime, the analog circuits start settling, and the pixel's reference voltage is applied. After period 3, PD_DIG is set to ground, and the FPGA transmits the 64MHz main clock to the image sensor. After all of the procedures, the sensor is ready for normal operation.

2.4.3. I^2C INTERFACE CONTROL

As mentioned in section 2.3, the reference circuit operating conditions are set by the register array. The I^2C interface writes the register array at the beginning of the sensor operation after 1.8V power is applied. Figure 2.19 shows the I^2C interface hardware block diagram and the timing diagram. Figure 2.19(a) depicts the shift register array organizes the I^2C interface. Especially the initial value of the register output at the FPGA, which is defined by the Verilog code, is the register value that has to be written at the register array

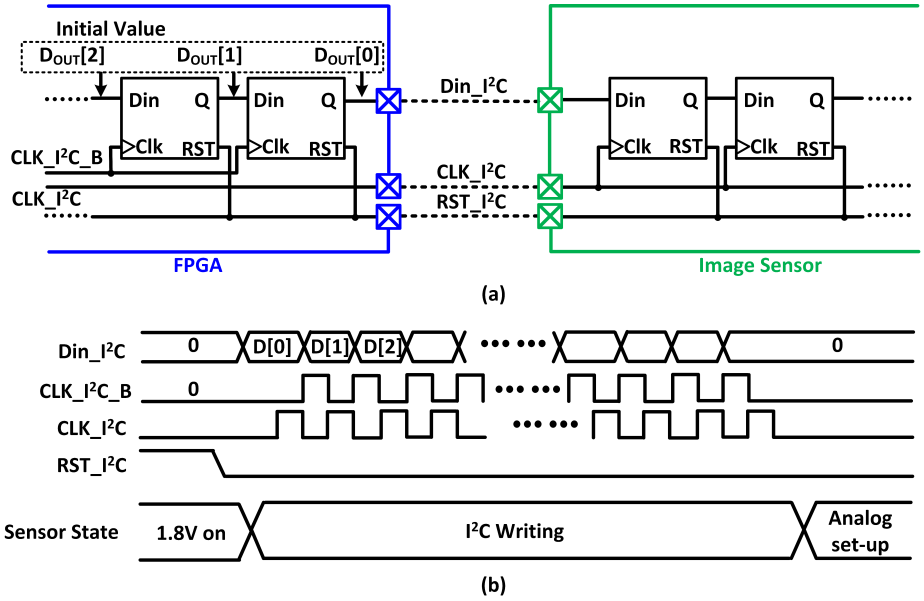


Figure 2.19: The I^{2}C interface (a) hardware block diagram and (b) timing

in the image sensor. The register array located in the image sensor receives this initial value and has the output directly connected to the switch controller of the reference circuits. As shown in Figure 2.1, the register array is located at the bottom right of the image sensor, and the register array handles 432 register values.

In order to control this I^{2}C interface, 4 signals are required, as described in Figure 2.19: `CLK_I2C_B`, `CLK_I2C`, `DIN_I2C` and `RST_I2C`. When the sensor starts applying power, the register array in FPGA and the image sensor are reset by using `RST_I2C`. After 1.8V power is applied, the register value is transmitted from the FPGA to the image sensor. The register array is controlled by the clock `CLK_I2C_B` and `CLK_I2C`, and these 2 clocks have a phase difference of 180 degrees. The register value is sequentially transmitted to the image sensor using `DIN_I2C`.

2.4.4. LVDS INTERFACE CONTROL

As described in Figure 2.3(c) of section 2.1.2, the data is transmitted to the FPGA through an LVDS interface after reading out pixel output using the ADC. Figure 2.20 shows the block diagram of the interface, including the serializer. As shown in Figure 2.20, the LVDS interface consists of 4 channels, each with 79 sets of the register. 12 flip-flops organize a single register set. Especially since the 180nm process is used to design this image sensor, 4 channel interface is a helpful structure to avoid speed limitation. Therefore, the clocks, CLK_CH1, CLK_CH2, CLK_CH3 and CLK_CH4, have 32MHz of maximum frequency, each with a 90-degree phase difference, as shown in Figure 2.22.

Figure 2.21 and figure 2.22 show the connection between the ADC and the register array and the timing diagram of the LVDS interface, including the register array control,

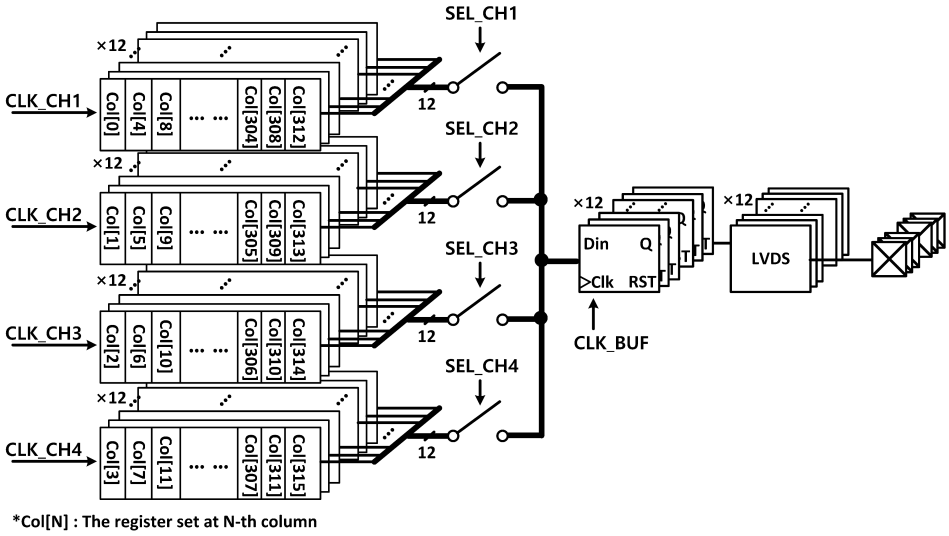


Figure 2.20: The block diagram of the LVDS interface, including the 4-channel register array and LVDS drivers

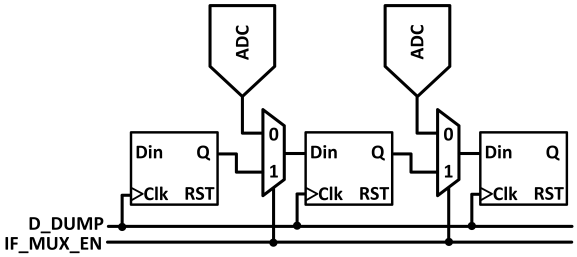


Figure 2.21: The connection between ADC and the register array using the 2 to 1 MUX

respectively. In Figure 2.21, the 2 to 1 MUX controls the input signal of each register. Therefore, when the IF_MUX_EN is low, 12-bit ADC outputs are connected to the register, and at the rising edge of the D_DUMP, the data is stored in the register. When IF_MUX_EN is high, the input of the register is connected to the output of the register from the previous column. The clocks, CLK_CH1, CLK_CH2, CLK_CH3 and CLK_CH4, are used to push the data to the right edge of the register array. Therefore, at the rising edge of the clocks, CLK_CH1, CLK_CH2, CLK_CH3 and CLK_CH4, each data stored at the register is transmitted to the register in the next column.

The output of the register at the right edge of each channel is the data transmitted through the LVDS. The 4 to 1 MUX supports serialization. The clocks, SEL_CH1, SEL_CH2, SEL_CH3 and SEL_CH4, open one of the switches out of 4. The output of each channel is transmitted to the flip-flop and stored in the flip-flop at the rising edge of clock CLK_BUF. When the flip-flop captures the output from the 4-channel register array, the LVDS immediately drives the data to the FPGA. Therefore, the maximum oper-

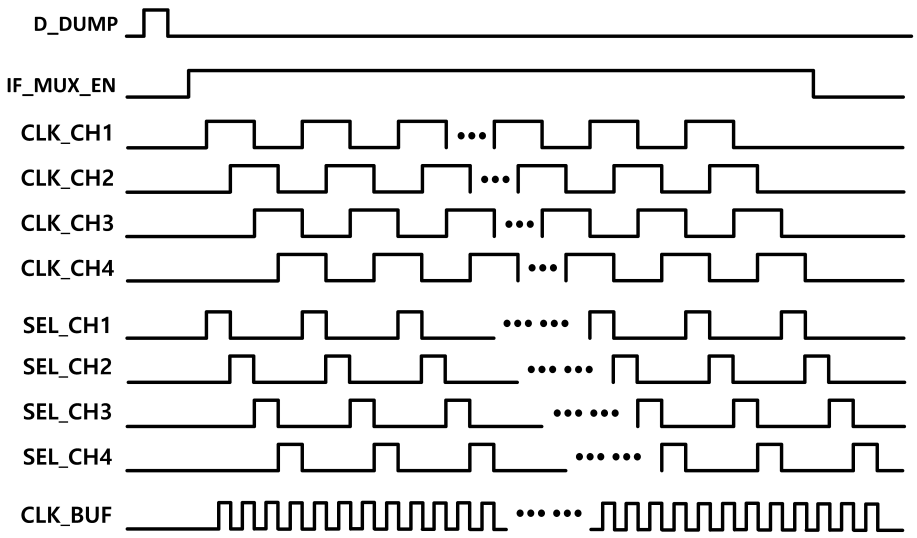


Figure 2.22: The timing diagram of the LVDS interface

ating speed of the clock, CLK_BUF, is 128MHz.

2.5. CONCLUSION

In this chapter, a brief explanation is provided regarding the common blocks shared in this project and the timing required to control these blocks. In order to operate the image sensors properly, a proper power-up sequence, as mentioned earlier, should be followed, sequentially supplying power to the components. In addition, an I^2C interface is employed to configure the operational mode of the image sensor, and data is written at appropriate timings. Information such as the reference voltage level, current level generated inside the image sensor, and digital signal processing settings are determined by the register setup using the I^2C interface. Furthermore, this chapter explains the signals used to control the row decoder and the delivery of VDA, containing information about the pixels for shutter operation and read operation. Moreover, it elaborates on how the digitally converted image data is transmitted to the FPGA with the timing diagram.

REFERENCES

[1] Nokia, *SMIA 1.0 Part 1: Functional Specification*, Available: http://www.smia-forum.org/ (accessed Nov. 12, 2007), Jun. 2004.

[2] C. Liang et al., "Analysis and compensation of rolling shutter effect," *IEEE Transactions on Image Processing*, vol. 17, no. 8, pp. 1323–1330, Aug. 2008. DOI: 10.1109/TIP.2008.925384.

[3] M. Wany et al., "Cmos image sensor with nmos-only global shutter and enhanced responsivity," *IEEE Transactions on Electron Devices*, vol. 50, no. 1, pp. 57–62, Jan. 2003. DOI: 10.1109/TED.2002.807253.

[4] T. Toyama et al., "Solid-state imaging device, method of driving the device, and camera system with varied timing of sampling period for sampling bias voltage during pixel readout," US Patent 8,687,100 B2, Apr. 2014.

3

Enhancing Readout Speed for Improving the Frame Rate of the Image Sensor: Theoretical Analysis

The main factors determining the frame rate of an image sensor include the pixel resolution, the image sensor's readout speed, and sensor architecture. Therefore, as mentioned earlier, maximizing the pixel rate is the practical solution to improve the frame rate, and much research has been conducted on improving the pixel rate. In addition, advancements in process technology have provided favorable conditions for improving the frame rate. For example, the performance of the ADC has significantly improved, and the circuit integration rate has improved, allowing for further improvements in the image sensor's performance.

In Chapter 3, the prototype of the SAR ADC and the optimized SAR ADC to improve the frame rate will be discussed.

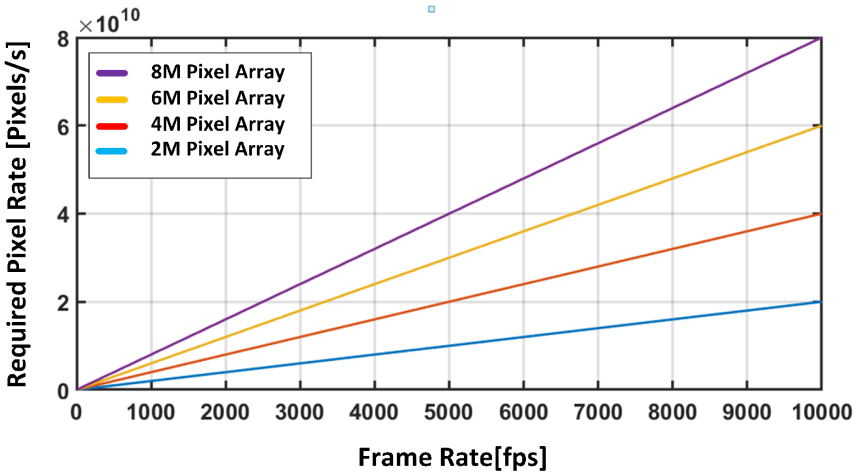


Figure 3.1: The required pixel rate depends on the frame rate

3.1. HIGH FRAME RATE OPERATION AND ADC

3.1.1. FRAME RATE AND ADC SAMPLING RATE

The frame rate refers to the number of images an image sensor can produce per unit of time, and it is calculated using the following formula.

$$F_{FR} \leq \frac{F_{ADC} \times N_{ADC}}{P_{ROW} \times P_{COL}} \approx \frac{F_{PIXEL}}{P_{ROW} \times P_{COL}} \tag{3.1}$$

In the given formula, F_{FR} represents the frame rate, F_{ADC} represents the ADC sampling rate, N_{ADC} represents the number of ADCs, and P_{ROW} and P_{COL} represent the number of rows and columns in the pixel array, respectively. As observed in the formula, three variables play a role in determining the frame rate: ADC sampling rate, the number of ADCs, and pixel resolution. Figure 3.1 employs this equation to illustrate the necessary pixel rate, F_{PIXEL}, within the image sensor to achieve different frame rates associated with different resolutions.

In Figure 3.1, the assumed aspect ratio of the pixel array's rows and columns is 16:9. As demonstrated in Figure 3.1, the required pixel rate varies based on the pixel array resolution when aiming to achieve the same frame rate. However, once the pixel array resolution is determined due to the system specification, the only option to attain a specific frame rate involves the pixel rate, F_{PIXEL}.

First, one of the effective methods to enhance the pixel rate is increasing the number of ADCs. In previous work, [1] and [2] have shown that situating ADCs on both sides of the pixel array leads to the pixel array reading out twice the speed compared to using one side only. Moreover, the stacked structure is used to increase the number of ADC in [3]. In [3], the pixel array is located on the top plate, and the ADCs are placed on the bottom. Since the number of the ADC is the same as the number of pixels in the top plate, the pixel rate is fast enough to achieve 660fps, though the ADC sampling rate is the same as the image sensor's frame rate. As demonstrated in [1], [2], [3], these approaches

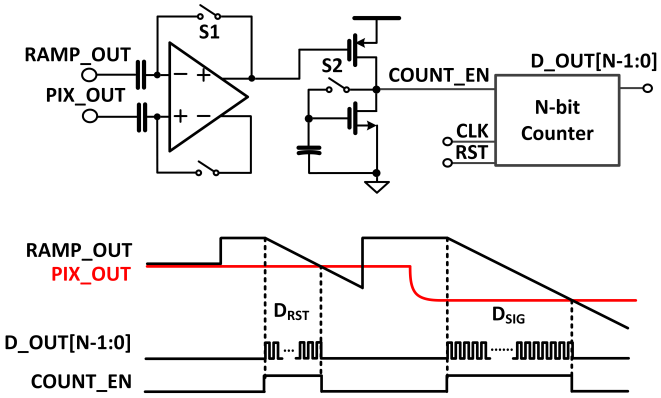


Figure 3.2: The general single-slope ADC circuit diagram and its operation timing

enhance the image sensor's pixel rate without improving the ADC sampling rate. As a result, the ADC can maintain a small signal bandwidth, and the temporal noise performances are not degraded. However, since many ADCs are designed within a small area, FPN performance degradation is inevitable. Consequently, when the number of ADCs is increased to improve the pixel rate, effective compensation techniques for FPN become indispensable due to the compact integration of multiple ADCs.

Second, enhancing the ADC's sampling rate improves the pixel rate. Different types of ADC have been used, especially to improve the inefficient algorithm of the single-slope ADC designed in previous image sensor research. For instance, [4] employs a cyclic ADC to minimize area and reduce the number of conversion steps. At the same time, [5] uses SAR ADC to improve the sampling rate significantly. Furthermore, [6] boosts the pixel rate using a pipeline technique. These methodologies require less increased design area, and less FPN performance degradation is expected. However, it is essential to note that increasing the ADC sampling rate requires higher signal bandwidth. Specifically, as discussed in [7], [8], the bandwidth directly influences temporal noise performance and leads to a decline in image quality.

As mentioned above, to enhance the image sensor's pixel rate, the 2 factors, such as the number of ADCs and the ADC sampling rate, have to be improved. However, these 2 factors accompany the FPN degradation and the increase of temporal noise. In this project, a column-parallel architecture is adopted to simultaneously address both factors, while considering the associated challenges in FPN and temporal noise performance.

3.1.2. SINGLE-SLOPE ADC IN HIGH-SPEED DATA CONVERSION

The analog front end of the image sensor has been designed using single-slope ADC for a long time, and the image sensor's performance has been optimized based on this structure. Especially when the single-slope ADC starts data conversion, the single-slope ADC sequentially compares the input signal with the reference voltage from the most positive to the most negative reference voltage level. Due to this simple data conversion

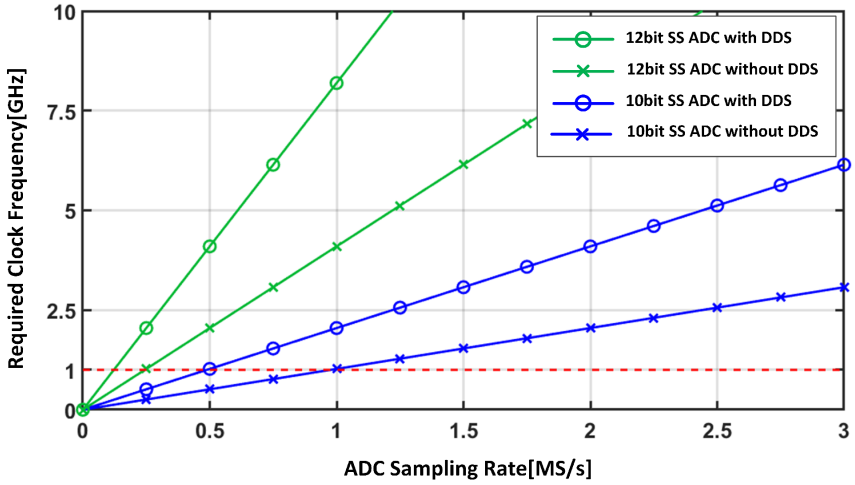


Figure 3.3: The required clock frequency depending on the sampling rate of the single-slope ADC

algorithm, the simple algorithm requires only a few numbers of the circuit blocks. In addition, to reduce the design area at each column of the image sensor, the reference voltage is provided from the current steering DAC (Digital to Analog Converter). A current steering DAC can simultaneously drive the reference voltage to all ADCs in the image sensor. For these reasons, a compact design is available when designing the single-slope ADC.

However, the single-slope ADC is inappropriate for implementing a high frame rate image sensor. First, the single-slope ADC has an inefficient data conversion algorithm. Figure 3.2 shows the general single-slope ADC circuit block diagram and its operation timing. As shown in Figure 3.2, the single-slope ADC receives reset levels at the input nodes `RAMP_OUT` and `PIX_OUT`, provided by the reference generator and pixel, respectively. The comparator is simultaneously reset by turning on both S1 and S2 switches. After reset, the single-slope ADC compares all reference voltage levels to identify the digital level. In the meantime, the N-bit counter counts the number until the reference voltage level is the same as the input signal level. The N-bit counter output signal is `D_OUT`[N-1:0], and the output of the comparator, `COUNT_EN`, is used as a counter-enabled signal. Therefore, the single-slope ADC must compare the signal with the reference for 2^N times for N-bit data conversion. The algorithm inevitably requires a high-frequency clock at least 2^N times faster than the ADC sampling rate. In addition, if the DDS (Digital Double Sampling) technique [9] is used in data conversion, the ADC converts the reset and signal levels sequentially, and the 2^{N+1} times faster clock is required. Figure 3.3 illustrates the required clock frequency depending on the ADC sampling rate. In Figure 3.3, when the ADC sampling rate is over 1MS/s, the required counter control clock frequency of 10-bit ADC exceeds 1GHz, and when DDS is applied as described in Figure 3.2, the required clock speed is 2GHz. The high-frequency clock becomes a burden when the image works at a high frame rate. The image sensor requires high-speed circuitry, consuming consid-

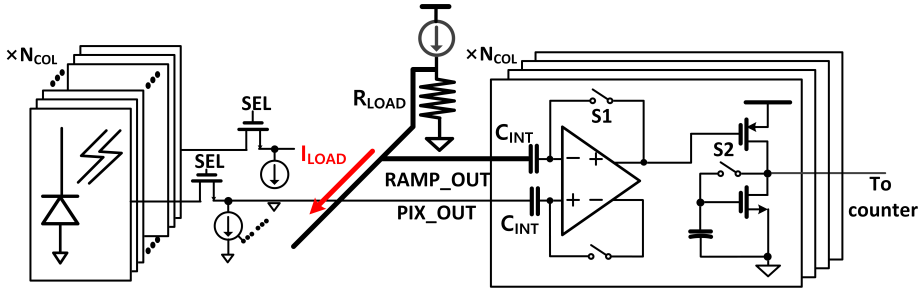


Figure 3.4: The circuit network, including the ADC array and the ramp generator

erable power due to the high-frequency system operation, and the clock path must be managed.

Second, the global reference encounters speed limitation in high-speed data conversion. The global reference is one of the reasons that single-slope ADC has an area-effective design. Figure 3.4 shows the circuit network between the comparator of the single-slope ADC and the reference driver. In this circuit network, the RC time constant, T_{RAMP}, is a critical factor that decides the reference driving speed. T_{RAMP} and the current required in the reference voltage generator, I_{LOAD}, are calculated as follows.

$$T_{\mathrm{RAMP}} = R_{\mathrm{LOAD}} \times N_{\mathrm{COL}} \times C_{\mathrm{INT}} \tag{3.2}$$

$$I_{\mathrm{LOAD}} = \frac{V_{\mathrm{SAT}}}{R_{\mathrm{LOAD}}} \tag{3.3}$$

In this formula, R_{LOAD} represents the output resistor of the reference generator, N_{COL} is the number of columns in the pixel array, C_{INT} is the capacitance of the sampling capacitor, and V_{SAT} is the image sensor's ADC saturation level. For this reason, when the image sensor's frame rate increases or the resolution increases, the output resistor value of R_{LOAD} must be reduced, and the reference generator has to increase the load current, I_{LOAD}. To reduce the time constant at the output of the reference generator, the buffer to transfer the reference voltage to the comparator is designed at each column [10]. Since the output of the reference generator is connected to the gate of the input transistor, designing buffer at each column can effectively reduce the time constant at the output of the reference generator. However, reference mismatch and the additional noise degradation are inevitable. When the resolution of the pixel increases, the time constant increases again though the buffer is designed in each column.

Third, maintaining the circuit performance uniformity within the ADC array is difficult in the high frame rate image sensor. In particular, the high frame rate image sensor inevitably consumes a lot of power. This results in an IR drop or IR rise on the power line from the center of the ADC array to both ends, as shown in Figure 3.5. Since the reference bias voltage is shared within the array, the circuit operating point is changed due to this potential variation. Figure 3.5 shows the IR rise on the ground power line. In Figure 3.5, K_{COL} represents the number of columns, and the current and the parasitic resistor at each column are denoted as I_{COL} and R_{COL}, respectively. As shown in Figure 3.5,

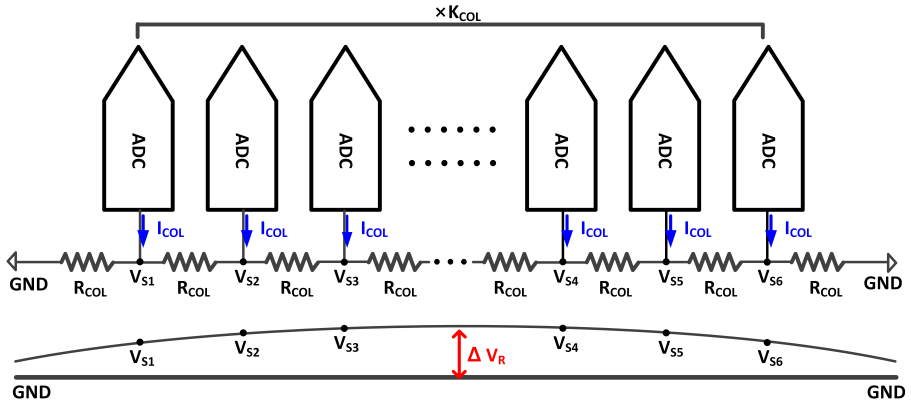


Figure 3.5: The IR rise effect one the power line (GND)

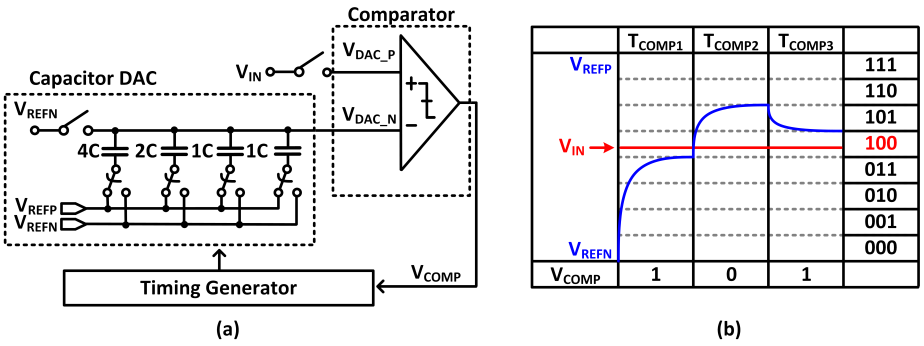


Figure 3.6: (a) The example of 3-bit SAR ADC block diagram and (b) its timing

the center of the array has the worst condition, and the calculated IR rise in the middle of the array, ΔV_R is as follows.

$$\Delta V_R = I_{COL} \cdot R_{COL} \sum_{X=1}^{K_{COL}/2} X = I_{COL} \cdot R_{COL} \cdot \left(\frac{K_{COL}^2}{8} + \frac{2K_{COL}}{8} \right) \tag{3.4}$$

For this reason, ΔV_R leads to the current mismatch. The mismatch gets worse if the resolution or the power consumption increases. This mismatch finally induces channel mismatch within the ADC array.

3.1.3. SAR ADC IN HIGH-SPEED DATA CONVERSION

The SAR (Successive Approximation Register) ADC is an optimal solution for realizing high frame-rate image sensors. Notably, the following explanation presents the 3 factors that the SAR ADC contributes to enhance the high frame rate of image sensors.

First, the SAR ADC employs efficient data conversion algorithms. Figure 3.6 illus-

trates a simplified 3-bit SAR ADC block diagram and its timing diagram. A SAR ADC consists of 3 main blocks: capacitor DAC, comparator, and timing generator. The capacitor DAC has 8-unit capacitors for the 3-bit data conversion. When the SAR ADC starts data conversion, the ADC samples the input signal at its positive input, V_{DAC_P}, and the negative reference voltage at its negative input, V_{DAC_N}. In the meantime, the bottom plate of the sampling capacitor should be connected to the negative reference, V_{REFN}. After sampling, the potential at the positive and negative pins are described in the following formula.

$$\begin{aligned} V_{DAC\_P} &= V_{IN} \\ V_{DAC\_N} &= \frac{N}{8} V_{REFP} + \frac{M}{8} V_{REFN} \end{aligned} \tag{3.5}$$

In this formula, the N and M are the number of unit capacitors whose bottom plates are connected to the positive reference, V_{REFP}, and the negative reference, V_{REFN}, respectively. The comparator compares the potential difference between each input node, V_{DAC_P} and V_{DAC_N}. If the potential difference of V_{DAC_P} and V_{DAC_N} satisfies the following statement, the comparator outputs '1'.

$$V_{DAC\_P} - V_{DAC\_N} = (V_{IN} - V_{REFN}) - \frac{N}{8} \cdot \Delta V_{REF} < 0 \tag{3.6}$$

In the formula above, ΔV_{REF} is the same as V_{REFP}-V_{REFN}. In addition, the SAR ADC applies the binary search algorithm. Therefore, the SAR ADC compares the input signal with the middle level between V_{REFP} and V_{REFN} at the first comparison time, T_{COMP1}, and the N and M are set to 4, respectively. Considering the data conversion algorithm, an N-bit SAR ADC requires N comparison cycles to complete the conversion. For instance, the 3-bit SAR ADC in Figure 3.6 performs 3 comparison cycles for data conversion. As described in Figure 3.6(b), if the input signal, V_{IN}, is larger than $0.5\times\Delta V_{REF}$, the SAR ADC set N and M as 6 and 2 in the second comparison time, T_{COMP2}, respectively. In the third comparison time, T_{COMP3}, the N and M are set to 5 and 3, following the same algorithms. For this reason, the clock necessary for data conversion is very slow compared to the single-slope ADC. For instance, to control SAR ADC operating at 250kS/s, the SAR ADC only requires 8MHz clocks. Furthermore, substantial research has been performed on low-power SAR ADCs, as mentioned in [11]. In particular, the figure-of-merit (FOM), an indicator of power efficiency, has significantly improved, reaching 1fJ/conv-step.

Second, each column in the imager has its own reference generator, which is implemented using a capacitor DAC. The single-slop ADC uses a global reference shared in the ADC located at each column, as shown in Figure 3.7(a). As mentioned previously in 3.1.2, this global reference has several problems. In particular, the ADC operation speed is limited due to the huge RC time constant at the output node of the reference generator. Though the RC time constant at the output node of the reference generator is reduced by using the input buffer for each column, the speed is limited for the same reason when pixel resolution increases. In addition, the RC time constant affects the linearity of the sensor by lowering the linearity of the reference voltage output generated from the reference generator. In particular, the INL (Integral Nonlinearity) performance of the ADC located in each column deteriorates. Although the INL does not directly affect image quality, it can be one of the roots of worse PRNU (Photo Response Nonuniformity).

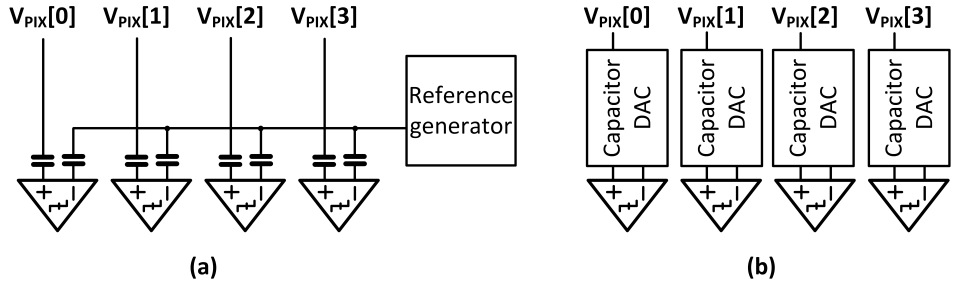


Figure 3.7: The block diagram of the circuit connection using (a) global reference and (b) individual reference

On the other hand, the SAR ADC cannot share the same reference voltage with the SAR ADCs in the other column due to its operation characteristics. Figure 3.7(b) shows an example of the reference generator providing reference voltage using the capacitor DAC located in each column. Since the reference generator is included in the column area, this capacitor DAC degrades the area efficiency compared to the single-slope ADC. However, as the frame rate of the image sensor increases, supplying reference voltages through individual reference generators becomes comparatively easier, offering a potential solution to the issue of speed limitations. Especially, although the output node of each capacitor DAC has a minimal RC time constant, each decision cycle in the SAR ADC is relatively long compared to that of the single-slope ADC. This relatively long cycle allows sufficient decision time even at low clock frequencies. For this reason, the SAR ADC can achieve high-speed operation without requiring a high-frequency clock, making it highly efficient. Furthermore, the research for digital error correction, such as [12] and [13], explained that the decision error at the MSB (Most Significant Bit) can be compensated. Therefore, MSB decision error can be compensated due to the large RC time constant when the SAR ADC controls the MSB capacitor. Since the RC time constant is small at the LSB (Least Significant Bit) decision, the SAR ADC can use a relatively accurate reference voltage compared to the single-slope ADC.

Third, with the advancement of process technology, the design area of SAR ADCs continues to shrink while their performance improves. As shown in Figure 3.6(a), the SAR ADC consists of three main blocks: the capacitor DAC, comparator, and timing generator. Among these, the capacitor DAC and timing generator typically occupy more than 70% of the total area and are therefore most affected by scaling in advanced process technologies. For example, a smaller feature size allows the timing generator to be implemented in a smaller area and to operate at a lower supply voltage, resulting in lower power consumption. Likewise, if the capacitor device is improved to offer higher capacitance density, the capacitor DAC can also be implemented with a smaller area compared to older technologies. As reported in [11], these improvements have significantly enhanced SAR ADC performance. The figure-of-merit (FOM), an indicator of power efficiency, has already reached values below 1 fJ/conversion-step. Furthermore, noise-shaping techniques have been applied to SAR ADCs to further extend their resolution toward higher-bit designs.

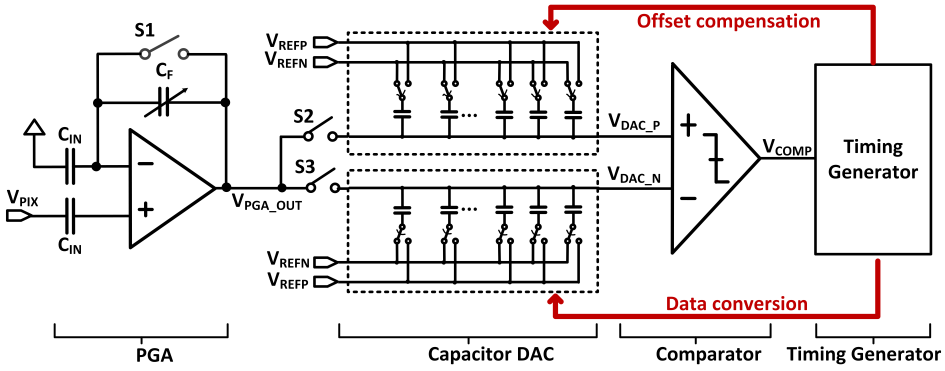


Figure 3.8: The block diagram of a single-channel readout chain using a conventional SAR ADC

These three factors show why the SAR ADC is better suited than the single-slope ADC for high frame rate image sensors. Therefore, it serves as an optimal solution for frame rate enhancement.

3.2. SAR ADC DESIGN IN CONVENTIONAL STRUCTURE

3.2.1. THE STRUCTURE AND THE TIMING OVERVIEW

Figure 3.8 illustrates the block diagram of a single-channel readout chain using a conventional SAR ADC. This single-channel readout chain is implemented in each column of the column-parallel structure. The readout chain comprises the PGA (Programmable Amplifier) and the SAR ADC. As mentioned in 3.1.3, the SAR ADC contains 2 capacitor DACs on the negative and positive side, a comparator, and a timing generator.

The PGA receives the pixel output via V_{PIX} from the pixel array and buffers the signal to the ADC through V_{PGA_OUT}. The switch S1 is used to reset the PGA at the beginning of the horizontal line time. The PGA especially switches the signal range from the 3.3V domain to the 1.8V domain. In addition, the PGA supports the analog gains up to ×8. Therefore, depending on the condition that the image sensor captures the image, such as low illumination conditions, the PGA amplifies the signal by applying the analog gain. The analog gain, A_{ANA}, supported by the PGA, is calculated as follows.

$$A_{ANA} = \frac{C_{IN}}{C_F} \tag{3.7}$$

The signal from the PGA is sampled at the capacitor DAC through the switch S2 and S3. Since the signal is sampled using the top plate sampling method, it is sampled at the top plate of the capacitor, and the reference voltages, V_{REFP} and V_{REFN}, are connected to the bottom plate of the capacitor. The capacitor DACs on the positive and negative sides consist of 1024-unit capacitors to support 10-bit data conversion, respectively. This SAR ADC is designed as a single-ended structure. As shown in Figure 3.8, the timing generator only controls the capacitor DAC on the negative side for the data conversion, and the capacitor DAC on the positive side is used to compensate for the comparator's offset.

When the ADC starts sampling, the reset level of the PGA is sampled on the positive side, and the signal corresponding to the integrated charge at the pixel is sampled on the opposite side. The output of the capacitor DAC is connected to the input of the comparator, and the comparator is designed with a pre-amplifier, which is relatively less sensitive to the kick-back noise during the comparison.

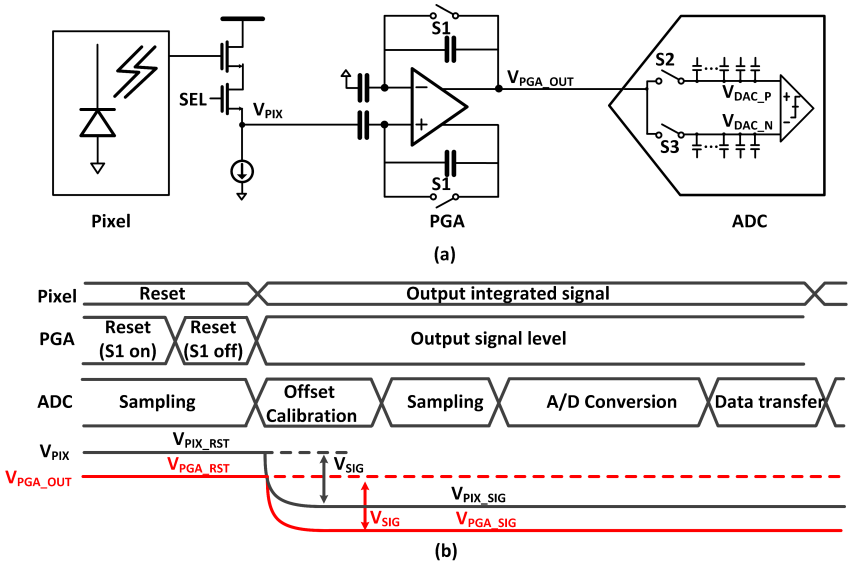


Figure 3.9: (a) The single channel readout chain within the column parallel structure, and (b) the timing diagram for one horizontal line time

As mentioned in Chapter 2, a column-parallel structure has been used to design the image sensors in this work. Each column within the column parallel architecture has the readout chain described in Figure 3.9(a). The readout chain contains the PGA and the ADC. In addition, the pixel provides the signal to the readout chain. The signal from the pixel is transferred to the PGA through the source follower, and the output of the source follower is connected to the positive input of the PGA. Figure 3.9(b) shows the timing diagram, including the status of each component, such as the pixel, the PGA, and the ADC. At the beginning of one horizontal line time, the PGA resets itself by turning on switch S1. In the meantime, the ADC samples the reset level, V_{PGA_RST}, from the PGA on the capacitor DAC by turning on S2 and S3. The PGA completes the reset operation after turning off S1, while the ADC finishes its sampling by turning off S2 and S3. After reset level sampling, the ADC performs the offset calibration for two cycles, and the pixel starts transmitting the integrated signal to the PGA. In the next phase, the ADC samples the integrated signal, V_{PGA_SIG}, from the PGA with S3 turned on. After the sampling is completed by turning off S3, the potential at V_{DAC_N} and V_{DAC_P} are the same as V_{PGA_SIG} and V_{PGA_RST}, respectively. The potential difference between V_{DAC_N} and V_{DAC_P} is V_{SIG}, which corresponds to the integrated charge inside the pixel. After sampling, the ADC converts the sampled signal into the 10-bit digital code. When the data conversion is

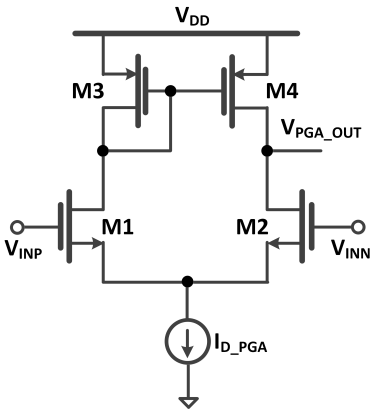


Figure 3.10: The circuit block diagram of the PGA

completed, the data is transferred to the final buffer.

3.2.2. PGA CIRCUIT DESIGN AND THE DETAIL CONTROL

As mentioned in 3.2.1, PGA buffers the signal and amplifies it by applying the analog gain. Figure 3.10 illustrates the circuit diagram of the PGA used in this work. The PGA is designed as a differential amplifier with a single-ended output. The PGA consists of 2 input nMOS transistors, 2 pMOS load transistors, and the current source. The load current at the current source is controlled from 20μA to 45μA in each column. The pixel output is connected to the bottom plate of the input capacitor, which is connected to the positive input transistor, M1. On the other hand, the bottom plate of the capacitor connected to the negative input transistor, M2, is set to the ground. For this reason, this structure doesn't require the additional reference voltage to set the common level. However, when the PGA is reset, the output $V_{\mathrm{PGA\_OUT}}$ is set to V_{DD}-V_{THP}, where V_{THP} is the threshold voltage of the pMOS transistors M4 and M3. Considering the signal range, the pixel output is connected to the positive input of the amplifier. Therefore, this structure has the same polarity of input and output signals. This circuit network connection explained above is shown in Figure 3.11(a).

Figure 3.11(b) illustrates the timing diagram of the PGA. When the switch S1 is turned on, and the pixel transfers the reset level, $V_{\mathrm{PIX\_RST}}$, through the node V_{PIX}, the PGA output is set to the reset level. The PGA reset level is the same as V_{DD}-V_{THP}, as mentioned above. When the PGA completes the reset operation, the switch S1 is turned off, and the output of the PGA is maintained at the same potential. If the pixel outputs the signal level corresponding to the integrated charge, the pixel output V_{PIX} becomes $V_{\mathrm{PIX\_RST}}$-V_{SIG}. The change, V_{SIG}, is proportional to the amount of the integrated charge inside the photodiode. The PGA also outputs the signal level after it receives the pixel outputs, $V_{\mathrm{PIX\_RST}}$-V_{SIG}. The output of the PGA becomes V_{DD}-V_{THP}-V_{SIG2}, and V_{SIG2} is proportional to V_{SIG}. Therefore, if the input capacitor C_{IN} is the same as the feedback capacitor C_{F}, V_{SIG2} is the same as V_{SIG}. In addition, if the feedback capacitor size is not the same as the input capacitor size due to the analog gain, V_{SIG2} is calculated as follows.

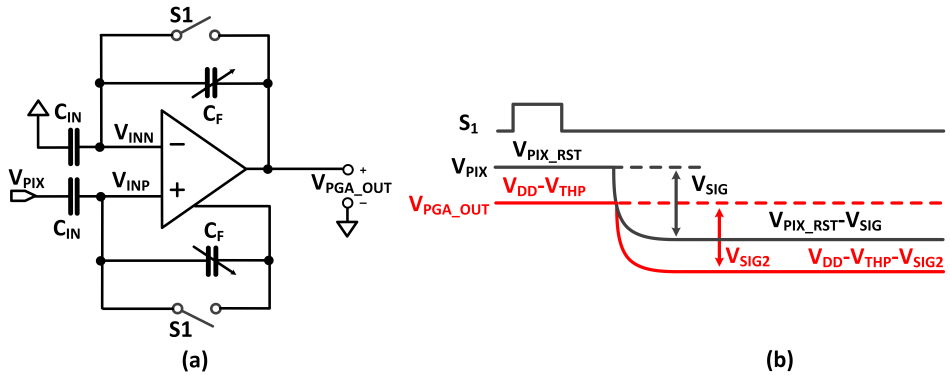


Figure 3.11: (a) The PGA network connection and (b) the timing diagram

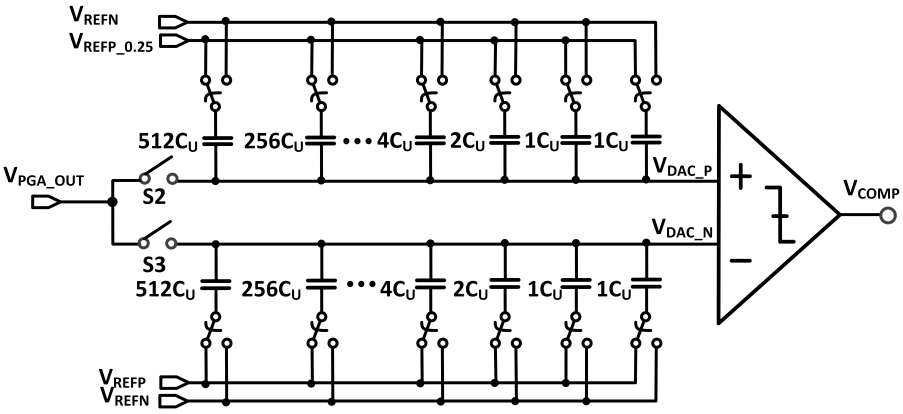


Figure 3.12: The circuit block diagram of the 10-bit SAR ADC

$$V_{\mathrm{SIG2}} = V_{\mathrm{SIG}} \times \frac{C_{\mathrm{IN}}}{C_{\mathrm{F}}} \tag{3.8}$$

3.2.3. SAR ADC DATA CONVERSION ALGORITHM

The capacitor DAC in the SAR ADC is designed as illustrated in Figure 3.12. The capacitor DAC in the positive and the negative input parts consists of 1024-unit capacitors, respectively, and the switches S2 and S3 are used to control the sampling. Since this SAR ADC only uses the negative part for the data conversion, the positive and the negative reference voltages, V_{REFP} and V_{REFN}, are provided to the capacitor DAC in the negative input part. The reference voltage is connected to the bottom plate of the capacitor through the switch network. On the other hand, the positive input part samples the reset level from the PGA, but the capacitor is not controlled during the data conversion. The capacitor DAC in the positive input part is controlled to compensate for the compara-

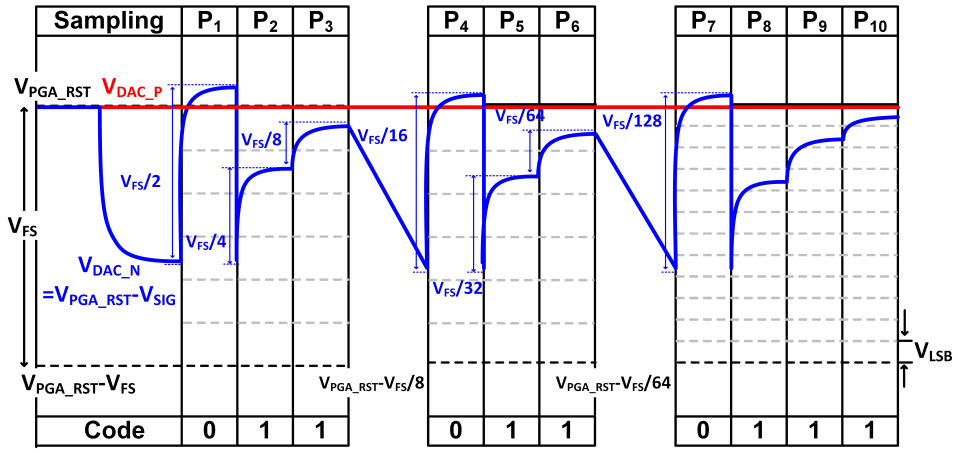


Figure 3.13: The example of the capacitor DAC output control during data conversion

tor's offset. Since the offset calibration requires 0.25LSB precision, the reference voltages provided to the capacitor DAC in the positive part are $V_{\mathrm{REFP\_0.25}}$ and V_{REFN}. The difference between $V_{\mathrm{REFP\_0.25}}$ and V_{REFN} is one-fourth of the signal range, and the relationship among those reference voltages is as follows.

$$\frac{1}{4} \times (V_{\mathrm{REFP}} - V_{\mathrm{REFN}}) = V_{\mathrm{REFP\_0.25}} - V_{\mathrm{REFN}} \tag{3.9}$$

In addition, the capacitor DAC continuously redistributes the charge after the unit capacitors are controlled. For this reason, the absolute value of the reference voltage does not affect the ADC performance. Still, the difference between the positive and the negative reference voltage is the same as the maximum size of the input signal. Therefore, the signal full-scale V_{FS} has the following relationship described in the following formula.

$$V_{\mathrm{FS}} = V_{\mathrm{REFP}} - V_{\mathrm{REFN}} \tag{3.10}$$

The SAR ADC uses this capacitor DAC and performs the data conversion in the following procedure. Figure 3.13 describes the data conversion procedure, including the capacitor DAC control and its output. As mentioned above, when the sampling is completed, the potential at the positive and the negative capacitor DAC's output is calculated as follows.

$$\begin{aligned} V_{\mathrm{DAC\_P}} &= V_{\mathrm{PGA\_RST}} \\ V_{\mathrm{DAC\_N}} &= V_{\mathrm{PGA\_RST}} - V_{\mathrm{SIG}} \end{aligned} \tag{3.11}$$

$V_{\mathrm{PGA\_RST}}$ and V_{SIG} are the reset level of the PGA and the signal corresponding to the integrated charge inside the pixel, respectively. If capacitor DAC in the negative input part is controlled the potential change at $V_{\mathrm{DAC\_N}}$ is as follows.

$$V_{DAC\_N} = V_{PGA\_RST} - V_{SIG} + \frac{N_P \cdot C_U}{C_{total}} \cdot (V_{REFP} - V_{REFN}) \tag{3.12}$$

In this formula, C_U and C_{TOTAL} refer to the capacitance of the unit capacitor and the total capacitor designed in the negative input part. The term N_P denotes the number of unit capacitors whose bottom plates are connected to the positive reference voltage V_{REFP}. Since the SAR ADC uses binary search algorithm, the SAR ADC compares the V_{SIG} with the middle level of the 2 reference voltages, V_{REFP} and V_{REFN}, at the first decision phase, P1.

$$V_{DAC\_N} = V_{PGA\_RST} - V_{SIG} + \frac{512 \cdot C_U}{1024 \cdot C_U} \cdot (V_{REFP} - V_{REFN}) \tag{3.13}$$

Therefore, the MSB capacitor, which is the same as 512-unit capacitors, is connected to the positive reference voltage, V_{REFP}. As shown in Figure 3.13, the signal level at P1 shows that the potential at the negative capacitor DAC output, V_{DAC_N}, is larger than the positive capacitor DAC output, V_{DAC_P}. The decision is '0'. As the decision is '0', the bottom plate of the MSB capacitor, which initially connects to V_{REFP}, switches back to the negative reference V_{REFN}. In the next phase, the ADC compares the signal V_{SIG} with $V_{FS}/4$. Therefore, the bottom plate of the 256-unit capacitors is connected to the positive reference voltage, V_{REFP}. In the same method, the potential at the negative capacitor DAC output, V_{DAC_N} is calculated as follows.

$$V_{DAC\_N} = V_{PGA\_RST} - V_{SIG} + \frac{256 \cdot C_U}{1024 \cdot C_U} \cdot (V_{REFP} - V_{REFN}) \tag{3.14}$$

In P2 phase, V_{DAC_N} is smaller than V_{DAC_P}, and the comparison result is '1'. In this case, the 256-unit capacitors maintain the connection with the positive reference voltage, V_{REFP}. In the same manner, the bottom plate of the 128-unit capacitors is connected to the positive reference voltage, and the potential of V_{DAC_N} is as follows.

$$V_{DAC\_N} = V_{PGA\_RST} - V_{SIG} + \frac{(256+128) \cdot C_U}{1024 \cdot C_U} \cdot (V_{REFP} - V_{REFN}) \tag{3.15}$$

Since the comparison result at P2 is '1', the total unit-capacitor connects its bottom plate with the positive reference voltage, V_{REFP}, is 384-unit capacitors. This operation is repeated during 10 cycles. After 10 cycles, the SAR ADC outputs the 10-bit digital code. In Figure 3.13, the final output is '0110110111' in binary code.

3.3. ADVANCED SAR ADC DATA CONVERSION ALGORITHM

3.3.1. THE STRUCTURE AND THE TIMING OVERVIEW OF THE TWO-STEP SAR ADC

Section 3.3 explains the two-step SAR ADC design. In particular, the two-step structure improves the linearity of the SAR ADC designed in section 3.2. As described in Section 3.2, the SAR ADC includes a capacitor DAC composed of 1024 unit capacitors. Due to the large number of unit capacitors, a corresponding number of control lines is required, which increases layout complexity. This spatial complexity often forces the unit capacitors to be designed smaller, resulting in degraded linearity performance.

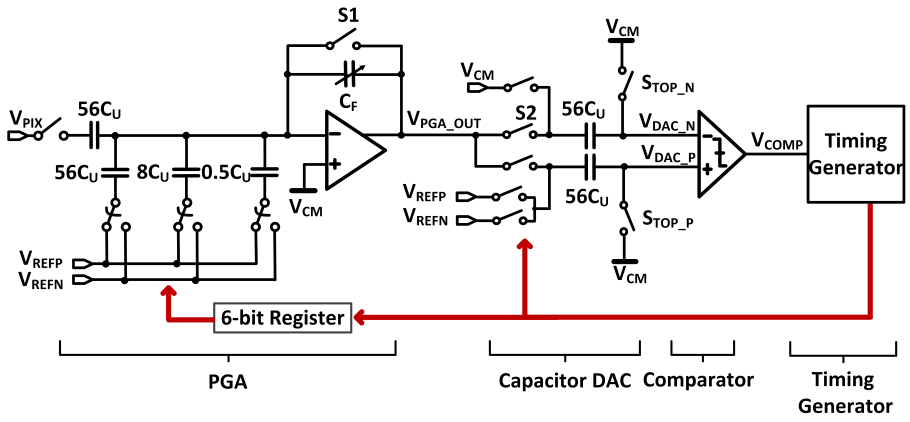


Figure 3.14: The block diagram of the readout chain designed with two-step SAR ADC

Figure 3.14 shows the readout chain containing a two-step SAR ADC designed in each column of the column-parallel structure. The readout chain consists of a 6-bit SAR ADC and a PGA. The SAR is designed in a single-ended structure with 56-unit capacitors on the positive and negative sides. Since the top-plate sampling generates the offset, the bottom-plate sampling technique is applied. As depicted in Figure 3.14, the PGA receives the pixel output at the negative input of the PGA, and outputs the signal to the ADC through its positive output. To control the reset level of the PGA output, the reference voltage V_{CM} is connected to the positive input of the PGA, and the V_{CM} is set to 0.8V. The PGA provides analog gain up to ×8. To support analog gain, the feedback capacitor, CF, is controlled from 7C to 56C. In addition, the PGA supports generating the residue after 6-cycles coarse analog to digital conversion. The residue enables the two-step data conversion of the ADC. For this reason, the 6-bit capacitor DAC is included in the PGA, and the capacitor DAC consists of the 56-unit capacitors. The 6-bit capacitor DAC is controlled by the 6-bit registers, which capture the coarse conversion result.

Figure 3.15 is a timing diagram of the pixel output readout timing within a single horizontal line time. When the horizontal line time starts after VDA (Vertical Domain Address) is transmitted, the pixel outputs the reset level, V_{PIX_RST}, via the pixel output node, V_{PIX}. The reset level, V_{PIX_RST}, is used to reset the PGA, and the PGA turns on the switch S1 to reset itself. The PGA output, V_{PGA_RST}, is sampled at the negative input of the ADC. The switches S2, S_{TOP_P}, and S_{TOP_N} are turned on to sample the reset level. When the PGA completes the reset operation, the switch S1 is turned off. The ADC turns off the switch S_{TOP_N} after the sampling reset level. When the sampling reset level is finished, the pixel starts transmitting V_{PIX_SIG}, corresponding to the integrated charge at the photodiode. The V_{PIX_SIG} is sampled at the PGA, and the PGA outputs the signal V_{PGA_SIG} to the ADC. When the ADC completes sampling the signal, V_{PGA_SIG}, the ADC turns off the S_{TOP_P} and S2 sequentially to support bottom plate sampling. The potential difference between the sampled signal on the positive and negative input of the ADC, V_{SIG}, is proportional to the integrated charge.

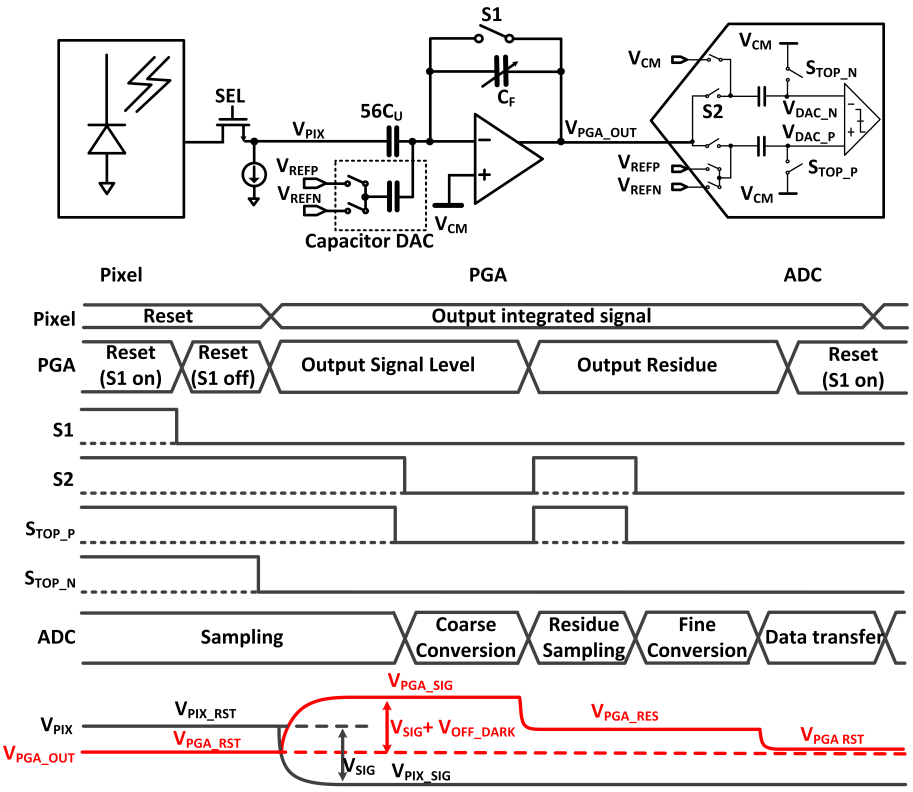


Figure 3.15: The readout chains of a single channel, including the pixel and the two-step SAR ADC, along with the timing diagram for one horizontal line time

After sampling the reset and signal levels, the ADC starts a 6-cycle coarse conversion. When the 6-cycle coarse conversion is completed, the PGA uses the coarse conversion result to generate the residue, V_{PGA_RES}, by controlling the capacitor DAC. The residue, V_{PGA_RES}, is sampled at the positive input of the ADC by turning on the switch S_{TOP_P} and S2. When the sampling is completed, the ADC starts a 6-cycle fine conversion. After the data conversion is finished, the 12-bit data conversion result is transmitted to the LVDS interface. The 12-bit conversion result generates an 11-bit digital code at the post-signal processing part.

3.3.2. PGA DESIGN AND ITS FUNCTIONALITY

As mentioned in section 3.3.1, the PGA provides the analog gain and regulates the signal range from the 3.3V domain to the 1.8V domain. In addition to the general PGA functions, the PGA generates residue after ADC coarse data conversion is completed. The PGA also generates the offset to control the image sensor's dark level and compensate for the reference mismatch between the coarse and fine conversion.

Figure 3.16 shows the PGA network connection depending on its operation and the

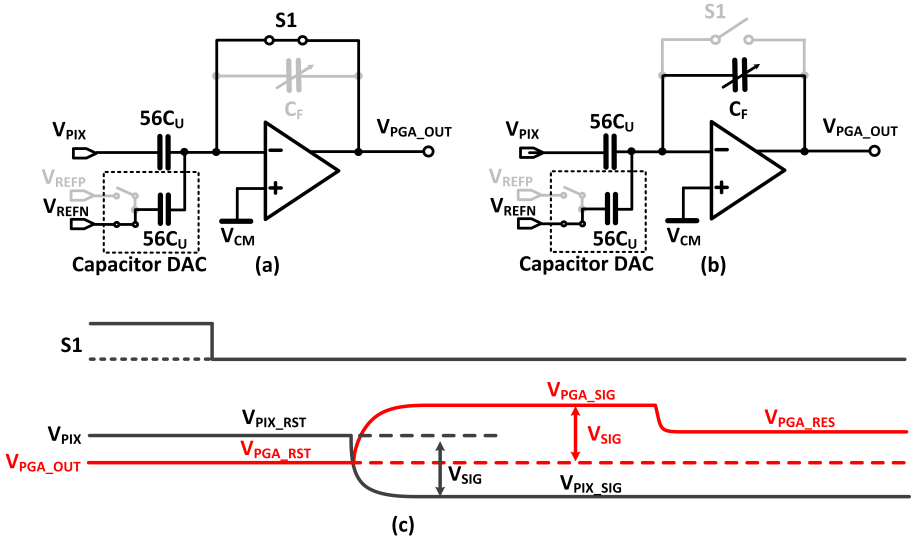


Figure 3.16: The PGA network connection during (a) reset phase, (b) after reset phase, and (c) the timing diagram for the PGA operation

timing. As described in Figure 3.16, the PGA receives the pixel output at the negative input of the PGA, and the positive output of the PGA is used to output the signal to the ADC. This type of PGA design has a different polarity between the input and output. Moreover, the positive input of the PGA is connected to the reference voltage, V_{CM}. The V_{CM} controls the reset level of the ADC, and to support the 0.8V signal output range, the V_{CM} is set to 0.8V.

As described in section 3.3.1, the PGA uses the pixel reset level, V_{PIX_RST}, to reset itself. When the PGA starts resetting itself, it turns on the switch S1, as shown in Figure 3.16(a). The input of the PGA is connected to the output of the PGA, V_{PGA_OUT}, and the V_{PGA_OUT} is equal to V_{CM} if the PGA is ideal. When the reset operation is completed, the PGA turns off the switch S1, as shown in Figure 3.16(b). However, since the pixel output is maintained as a reset level, V_{PIX_RST}, the PGA maintains its output as V_{PGA_RST}. After reset sampling, the pixel starts transmitting the signal level, V_{PIX_SIG}, to the PGA. Though the voltage level at the pixel output gets lower, the PGA output gets higher since the input and the output of the PGA have different signal polarity. The PGA amplifies the difference between V_{PIX_RST} and V_{PIX_SIG}. The difference between the V_{PGA_RST} and V_{PGA_SIG} is described as follows.

$$V_{PGA\_RST} - V_{PGA\_SIG} = A_{PGA} \times (V_{PIX\_RST} - V_{PIX\_SIG}) \tag{3.16}$$

The A_{PGA} is the gain of the PGA, which is the same as $56C/C_F$. As shown in Figure 3.16(c), If the gain of the PGA is equal to 1, the difference between the V_{PIX_RST} and V_{PIX_SIG} is equal to the difference between the V_{PGA_RST} and V_{PGA_SIG}. During each signal sampling, the bottom plate of the capacitor DAC is connected to the negative reference,

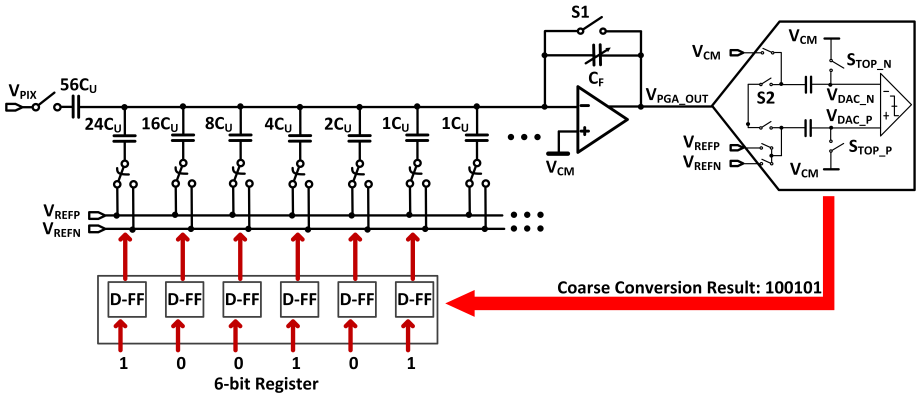


Figure 3.17: The capacitor DAC inside the PGA control network using 6-bit register

V_{REFN}.

As mentioned in section 3.3.1, residue generation is the key operation to implement the two-step SAR ADC. As depicted in Figure 3.14, the PGA generates the residue after the ADC completes a 6-cycle coarse conversion. The 6-bit conversion result is captured at the 6-bit register, and the output of the 6-bit register directly controls the capacitor DAC, as described in Figure 3.17. Figure 3.17 shows an example of generating residue. When the ADC completes the conversion, the MSB code controls the 24-unit capacitor, and the LSB code controls the 1-unit capacitor since the capacitor DAC designed in PGA is the same as the capacitor DAC used for data conversion inside the SAR ADC. The generated residue, V_{PGA_RES}, is calculated as follows.

$$V_{PGA\_RES} = V_{PGA\_SIG} - (V_{REFP} - V_{REFN}) \times \frac{N_P \cdot C_U}{56 \cdot C_U} \tag{3.17}$$

N_P denotes the number of unit capacitors whose bottom plates are connected to the positive reference voltage, and C_U represents the capacitance of a single unit capacitor. V_{REFP} and V_{REFN} are the positive and negative reference voltages. The generated residue, V_{PGA_RES}, is sampled on the positive input of the ADC before starting fine conversion.

The PGA generates the offset 2 times within a horizontal line time. In the timing diagram shown in Figure 3.15, when the ADC completes reset level sampling, the PGA generates the offset. Since the dark level is set to 256 in this work, the PGA controls the 8-unit capacitor to make the analog signal corresponding to 256 LSB. To implement this operation, the PGA has additional 8-unit capacitors, described in Figure 3.18(a), and the reference voltage connected to the bottom plate of the additional 8-unit capacitors is changed from V_{REFN} to V_{REFP}. The generated offset is calculated as follows.

$$\begin{aligned} V_{PGA\_SIG} &= V_{PGA\_RST} + V_{SIG} + (V_{REF\_P} - V_{REF\_N}) \times \frac{8C_U}{C_F} \\ &= V_{PGA\_RST} + V_{SIG} + V_{OFF\_DARK} \end{aligned} \tag{3.18}$$

In this formula, V_{SIG} is the difference between V_{PGA_SIG} and V_{PGA_RST} in Figure 3.15.

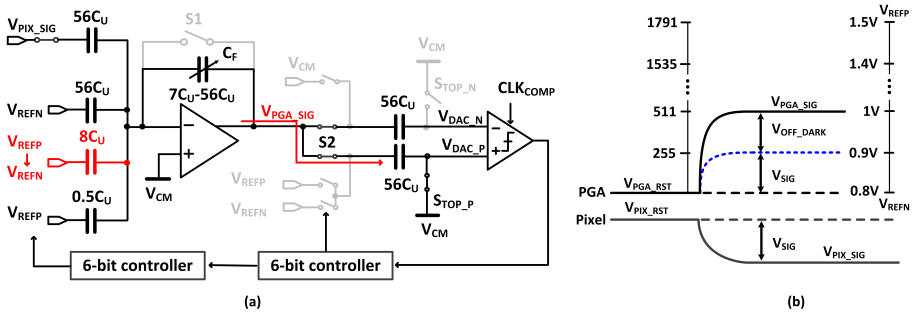


Figure 3.18: (a)The PGA control generating offset to control dark level corresponding to 256LSB, and (b) the PGA output with or without offset

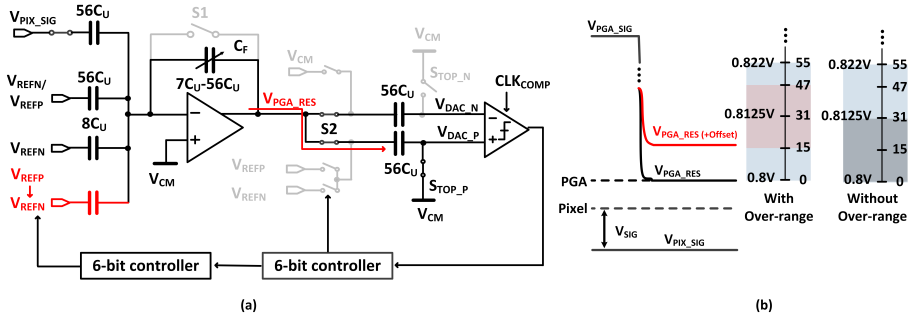


Figure 3.19: (a) The PGA control generating offset for compensation, and (b) the PGA output with or without offset during generating residue

The generated offset after controlling the 8-unit capacitor is $V_{\mathrm{OFF\_DARK}}$.

In addition, The PGA also generates the offset when the PGA generates the residue. The offset compensates for the wrong data conversion from the coarse data conversion. There are two main reasons for the wrong data conversion. First, the incomplete settling at the PGA output distorts the signal sampled at the ADC. Second, the reference mismatch between the coarse and fine conversion leads to wrong data conversion. Therefore, the first cycle at the fine conversion is used to correct the decision. Figure 3.19(a) shows that the additional 0.5-unit capacitor is controlled to generate the offset. The reference voltage connected to the bottom plate of the capacitor is changed from V_{REFP} to V_{REFN}. The residue, including the generated offset, is calculated as follows.

$$V_{\mathrm{PGA\_RES}} = V_{\mathrm{PGA\_SIG}} - (V_{\mathrm{REFP}} - V_{\mathrm{REFN}}) \times \frac{C_{\mathrm{P}}}{56C} + (V_{\mathrm{REFP}} - V_{\mathrm{REFN}}) \times \frac{0.5C_U}{56C_U} \tag{3.19}$$

The last term (V_{REFP}-V_{REFN})×0.5C/56C corresponds to the generated offset, and this offset level is the same as 8LSB. The rest of the formula is the same as the residue calculated above. Since the first cycle of the fine conversion is used as a redundancy, the decision range corresponds to 56LSB. As described in Figure 3.19(b), the additional de-

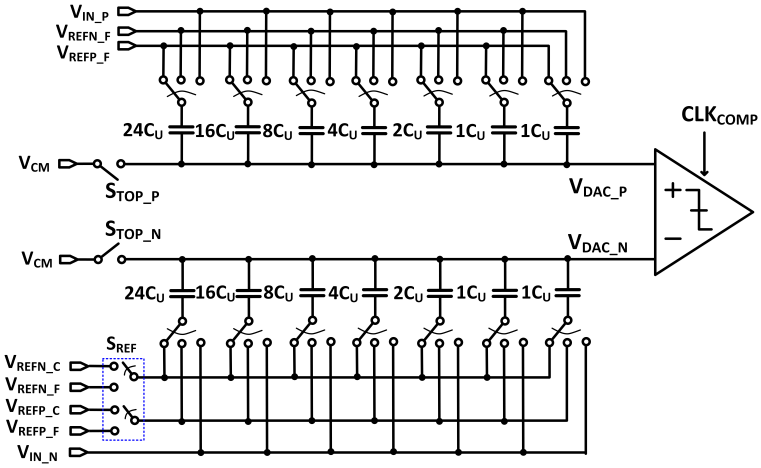


Figure 3.20: Circuit block diagram of the two-step SAR ADC

cision range of the SAR ADC is only +24LSB above the actual signal range if the offset is not generated. On the other hand, the additional decision range is +16LSB/-8LSB with 8LSB offset. The detailed operation is explained in the next section, 3.3.3, together with the data conversion algorithm.

3.3.3. TWO-STEP SAR ADC DATA CONVERSION ALGORITHM

Figure 3.20 shows the block diagram of a 6-bit SAR ADC used in a two-step ADC, consisting of a capacitor DAC, comparator, and control logic. As mentioned in section 3.3.1, the 6-bit DAC has 56-unit capacitors, and the 56-unit capacitors are included in positive and negative capacitor DACs, respectively. Since the total unit capacitor is 56 on each side, the MSB capacitor consists of 24-unit capacitors. The number of the unit capacitors in the remaining part is designed with a binary weighted number. The SAR ADC is designed in a single-ended structure. During the data conversion, the SAR ADC controls the capacitor DAC at the negative input part. As shown in the timing diagram in Figure 3.15, the reset level, V_{PGA_RST}, and the signal level, V_{PGA_SIG}, are sampled at the capacitor DAC in the positive input part and the capacitor DAC in the negative input part, respectively. The switches S_{TOP_N} and S_{TOP_P} on both positive and negative sides manage the connection between the switches and the reference voltage V_{CM}. The reference voltage and the input signal are sampled at the bottom plate of the capacitor DAC, and 3 switches control the connection. In addition, the ADC uses different reference voltages between coarse and fine conversion. The reference voltages, V_{REFP_C} and V_{REFN_C}, are the reference voltages for the coarse conversion, and the reference Voltages, V_{REFP_F} and V_{REFN_F} are used for the fine conversion. Depending on the data conversion phase, the switch S_{REF} selects the appropriate reference voltage.

Figure 3.21 illustrates the example of the two-step SAR ADC data conversion. In Figure 3.21, S_{ADC} refers to the practical signal range except for the dark level and the margin above the highest code. V_{LSB} is the analog signal range corresponding to 1LSB digital

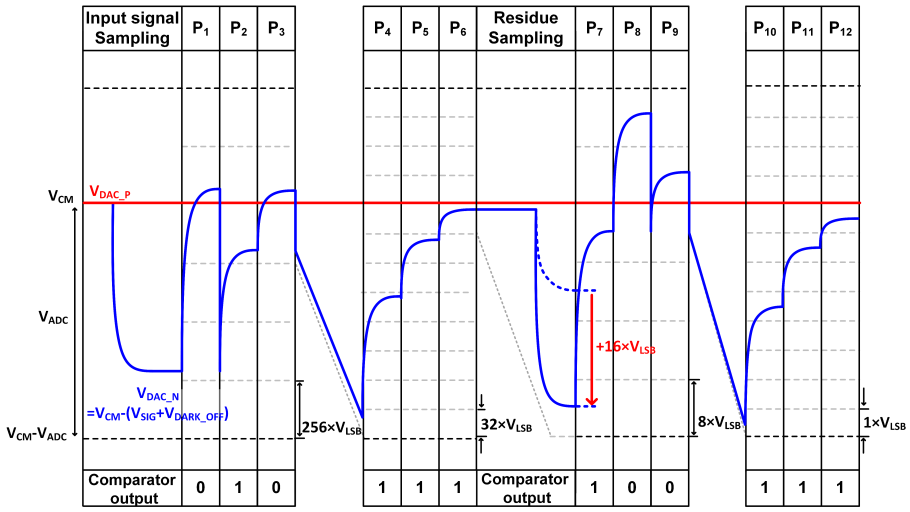


Figure 3.21: The example of the capacitor DAC output control of the two-step SAR ADC during the data conversion

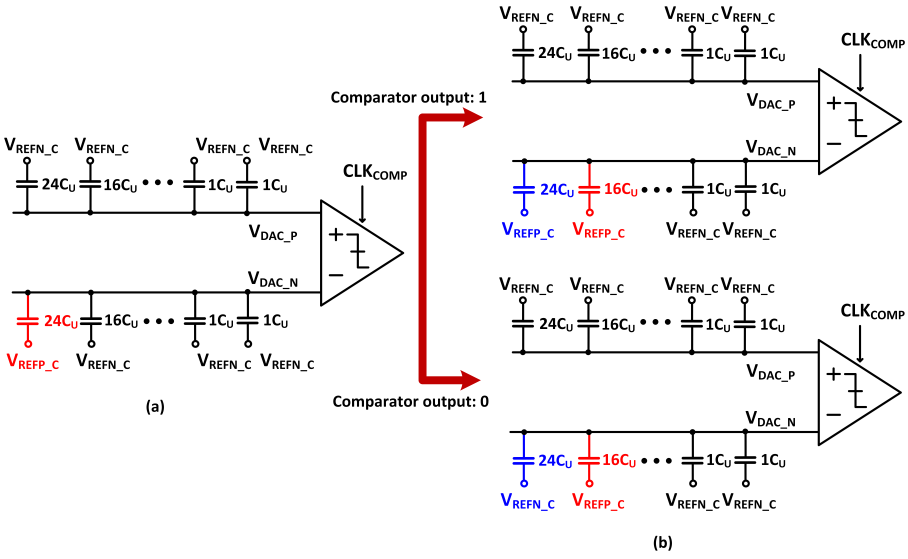


Figure 3.22: Capacitor DAC control (a) at the first cycle, and (b) at the second cycle

output. P1 to P12 represent the ADC data conversion cycle. The 6-bit SAR ADC starts a 6-cycle coarse conversion after completing input signal sampling. Figure 3.22(a) shows the capacitor DAC control at the first cycle of the data conversion. The bottom plate of the MSB capacitor is connected to the positive reference voltage, V_{REFP_C}. The calculated capacitor DAC output, V_{DAC_N}, is shown below.

$$V_{DAC\_N} = V_{CM} - (V_{PGA\_SIG} - V_{REFN\_C}) + \Delta V_{REF\_C} \times \frac{24C_U}{56C_U} \tag{3.20}$$

In the formula above, V_{PGA_SIG} is the signal sampled on the negative capacitor DAC and is the same signal described in Figure 3.15. V_{PGA_SIG} includes the dark level, V_{DARK_OFF}, mentioned in section 3.3.2. Therefore, V_{PGA_SIG}-V_{REFN_C} is equal to V_{SIG}+V_{DARK_OFF} in Figure 3.21. ΔV_{REF_C} is the reference voltage difference between V_{REFP_C} and V_{REFN_C}. Since the output of the capacitor DAC on the positive side is equal to V_{CM}, the potential difference is calculated below.

$$V_{DAC\_P} - V_{DAC\_N} = \left(V_{SIG} + V_{DARK\_OFF}\right) - \Delta V_{REF\_C} \times \frac{24C_U}{56C_U} \tag{3.21}$$

The comparator uses the potential difference between its positive and negative inputs, V_{DAC_P}-V_{DAC_N}. If the difference is below 0, the comparator outputs '0'. The ADC changes the connection between the MSB capacitor and the reference voltage. The negative reference voltage, V_{REFN_C}, is connected to the MSB capacitor. On the other hand, if the difference is above 0, the comparator outputs '1'. The ADC maintains the connection between the MSB capacitor and the positive reference voltage, V_{REFP_C}. In Figure 3.21, since the difference is below 0 at the first cycle, the output of the comparator is 0.

In Figure 3.21, when ADC starts the second cycle, P2, the ADC changes the connection between the second MSB capacitor and the reference voltage. The second MSB capacitor consists of 16-unit capacitors. Figure 3.22(b) shows the capacitor DAC control at the second cycle. As described in Figure 3.22(b), the connection between the MSB capacitor and the reference voltage is different, and the ADC connects the bottom plate of the second MSB capacitor with a positive reference voltage, V_{REFP_C}. The output of the negative capacitor DAC is calculated as follows.

$$V_{DAC\_N} = V_{CM} - (V_{PGA\_SIG} - V_{REFN\_C}) + D_1 \cdot \Delta V_{REF\_C} \cdot \frac{24C_U}{56C_U} + \Delta V_{REF\_C} \cdot \frac{16C_U}{56C_U} \tag{3.22}$$

In the formula, D_1 is the decision result from the first cycle. The difference of the capacitor DAC output on the positive and negative sides is calculated below.

$$V_{DAC\_P} - V_{DAC\_N} = \left(V_{SIG} + V_{DARK\_OFF}\right) - D_1 \cdot \Delta V_{REF\_C} \cdot \frac{24C_U}{56C_U} - \Delta V_{REF\_C} \cdot \frac{16C_U}{56C_U} \tag{3.23}$$

In the same way as the first comparison, if the difference, V_{DAC_P}-V_{DAC_N}, is below 0, the comparator outputs '0'. On the other hand, if the difference is above 0, the comparator outputs '1'. In Figure 3.21, the comparator outputs '1'. Following the same work principle, the ADC completes the 6-cycle coarse data conversion. The coarse conversion result is '010111'.

After coarse conversion, the PGA generates the residue, which is again sampled on the negative capacitor DAC again. Since the offset is generated to set up the +8LSB/-16LSB over-range, the offset corresponding to 16LSB is included in the residue. In the meantime, the ADC controls the switch, S_{REF}, to change the reference voltage used for fine conversion. As a result, the reference voltages, V_{REFP_F} and V_{REFN_F}, are used for the fine conversion. When the sampling is completed, the ADC starts a 6-cycle fine conversion. The conversion method is the same as the coarse conversion. Therefore, the fine conversion controls the MSB capacitor first. The capacitor DAC output at the negative capacitor DAC after connecting the positive reference voltage to the bottom plate of the MSB capacitor is calculated as follows.

$$V_{DAC\_N} = V_{CM} - (V_{PGA\_RES} - V_{REFN\_F}) + \Delta V_{REF\_F} \times \frac{24C_U}{56C_U} \tag{3.24}$$

The V_{PGA_RES} is the residue shown in Figure 3.15. The difference of the capacitor DAC output on the positive and negative sides is calculated below.

$$V_{DAC\_P} - V_{DAC\_N} = (V_{PGA\_RES} - V_{REFN\_F}) - \Delta V_{REF\_F} \times \frac{24C_U}{56C_U} \tag{3.25}$$

In the same way as the coarse conversion, the comparator outputs the code depending on the polarity of the difference, V_{DAC_P}-V_{DAC_N}. In Figure 3.21, the first cycle decision result is 1 because the difference is above 0. The result of the 6-cycle fine conversion is '100111'.

The 12-bit decision result is directly transmitted to the interface, and the final 11-bit digital code is generated at the FPGA. The calculation of the final output, D_{OUT}, is as follows.

$$D_{OUT} = \sum_{i=2}^{6} 2^{11-i} \cdot D_i + \sum_{i=8}^{12} 2^{12-i} \cdot D_i + 1.5 \times (2^9 \cdot D_1 + 2^4 \cdot D_7) - 16 \tag{3.26}$$

In this formula, D_i is the decision result at the i-th cycle. Since the offset is included in the residue, 16LSB is subtracted from the final code.

The two-step SAR ADC has the transfer curve of the red line in Figure 3.23 without distortion at coarse conversion. The minimum output code at fine conversion is 16 due to the offset, $16V_{LSB}$ in Figure 3.21. However, if the coarse decision is wrong, the generated residue deviates from the red area in Figure 3.23. Nevertheless, if the error is within the over-range marked in blue, it is possible to compensate for it during the fine conversion. For example, if the coarse conversion is wrong due to a lack of the PGA bandwidth, the digital output from the coarse conversion can be less than the ideal conversion result. In this case, the transfer curve deviates from the red curve, and this curve follows the transfer curve of case 1 in Figure 3.23. Though the coarse conversion result is lower than expected, accurate conversion is available because the actual input signal from the pixel is preserved. Therefore, the 1-bit redundancy covers this deviation and finally leads to the correct result. In addition, the over-range corresponds to 0.25LSB and 0.5LSB, respectively, in the case of coarse conversion. In the opposite case, the transfer curve follows the transfer curve of case 2 in Figure 3.23.

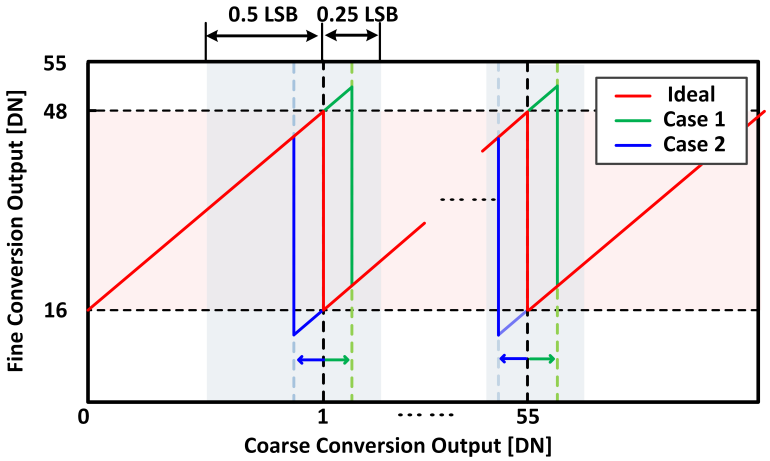


Figure 3.23: Transfer curve of the final conversion result of the two-step SAR ADC

3.4. CONCLUSION

This chapter discusses a theoretical SAR ADC data conversion algorithm and the SAR ADC design. As mentioned in section 3.3.1, the SAR ADC data conversion algorithm is straightforward because the SAR ADC uses the binary search algorithm. The required clock to control SAR ADC is relatively slow enough to implement a robust system. Therefore, the SAR ADC is one of the best options for implementing high-speed readout architecture. Especially the 2 types of SAR ADC design and the data conversion algorithm are explained in this chapter. Section 3.3.2 explains the conventional 10-bit SAR ADC design and its data conversion algorithm. In this design, the ADC offset calibration technique is applied as a background operation, and ADC performs the offset calibration between the pixel's reset level and signal level sampling time. Section 3.3.3 explains the two-step SAR ADC design and the data conversion algorithm. The PGA generates the residue after a 6-cycle coarse conversion in this design. Therefore, the readout architecture requires only 6-bit ADC. Instead, the PGA contains the 6-bit capacitor DAC. As a result, the number of unit capacitors designed in a two-step readout architecture is reduced compared to conventional 10-bit SAR ADC. In addition, the over-range set by the redundancy compensates for the wrong coarse conversion result. The wrong coarse conversion result originates from the incomplete input signal settling at the PGA or the reference mismatch between the coarse and fine conversion.

REFERENCES

[1] T. Haruta et al., "4.6 a 1/2.3inch 20mpixel 3-layer stacked cmos image sensor with dram," in *2017 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2017, pp. 76–77. DOI: 10.1109/ISSCC.2017.7870268.

[2] T. Yasue et al., "A 33mpixel cmos imager with multi-functional 3-stage pipeline adc for 480fps high-speed mode and 120fps low-noise mode," in *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2018, pp. 90–92. DOI: 10.1109/ISSCC.2018.8310198.

[3] M. Sakakibara et al., "A back-illuminated global-shutter cmos image sensor with pixel-parallel 14b subthreshold adc," in *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2018, pp. 80–82. DOI: 10.1109/ISSCC.2018.8310193.

[4] S. Lim et al., "A 240-frames/s 2.1-mpixel cmos image sensor with column-shared cyclic adcs," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2073–2083, Sep. 2011. DOI: 10.1109/JSSC.2011.2144010.

[5] R. Funatsu et al., "6.2 133mpixel 60fps cmos image sensor with 32-column shared high-speed column-parallel sar adcs," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2015, pp. 1–3. DOI: 10.1109/ISSCC.2015.7062951.

[6] T. Yasue et al., "A 1.7-in, 33-mpixel, 120-frames/s cmos image sensor with depletion-mode mos capacitor-based 14-b two-stage cyclic a/d converters," *IEEE Transactions on Electron Devices*, vol. 63, no. 1, pp. 153–161, Jan. 2016. DOI: 10.1109/TED.2015.2451700.

[7] J. Cheon et al., "Noise analysis and simulation method for a single-slope adc with cds in a cmos image sensor," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 10, pp. 2980–2987, 2008. DOI: 10.1109/TCSI.2008.923434.

[8] X. Ge et al., "A 0.5e^- rms temporal noise cmos image sensor with gm-cell-based pixel and period-controlled variable conversion gain," *IEEE Transactions on Electron Devices*, vol. 64, no. 12, pp. 5019–5026, 2017. DOI: 10.1109/TED.2017.2759787.

[9] Y. Nitta et al., "High-speed digital double sampling with analog cds on column parallel adc architecture for low-noise active pixel sensor," in *2006 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2006, pp. 2024–2031. DOI: 10.1109/ISSCC.2006.1696261.

[10] A. Suzuki et al., "6.1 a 1/1.7-inch 20mpixel back-illuminated stacked cmos image sensor for new imaging applications," in *2015 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2015, pp. 1–3. DOI: 10.1109/ISSCC.2015.7062950.

[11] P. Harpe, "Low-power sar adcs: Basic techniques and trends," *IEEE Open Journal of the Solid-State Circuits Society*, vol. 2, pp. 73–81, 2022. DOI: 10.1109/OJSSCS.2022.3211482.

[12] S. Cho et al., "A 550μw 10b 40ms/s sar adc with multistep addition-only digital error correction," in *2010 IEEE Custom Integrated Circuits Conference (CICC)*, San Jose, CA, USA, 2010, pp. 1–4. DOI: 10.1109/CICC.2010.5617408.

[13] C. Liu et al., "A 10b 100ms/s 1.13mw sar adc with binary-scaled error compensation," in *2010 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2010, pp. 386–387. DOI: 10.1109/ISSCC.2010.5433970.

4

Enhancing Readout Speed for Improving the Frame Rate of the Image Sensor: Image Quality

Maximizing the ADC performance leads to an improvement of the image sensor's frame rate. Particularly, the data conversion algorithm of SAR ADC used in this work is the appropriate solution to improve the frame rate due to its efficient data conversion algorithm. However, though the image sensor's frame rate is improved, several indicators, such as temporal noise, FPN (fixed pattern noise), should be managed to have good image quality. Especially a high-speed ADC inevitably has large noise bandwidth. The large bandwidth induces image quality degradation due to the temporal noise. In addition, the FPN degradation mainly induced by the dark current and offset within the data path can be an obstacle to maintaining the image quality.

In this chapter, a practical design to maintain the image quality is discussed. In particular, the ADC performance analysis based on measured indicators such as temporal noise and FPN, is discussed.

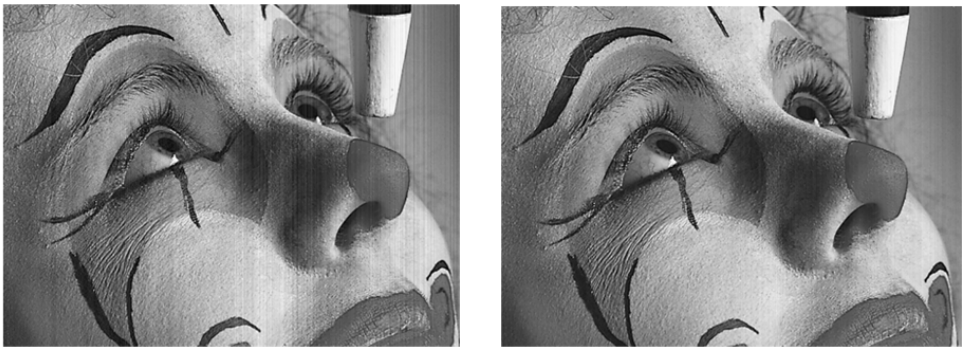


Figure 4.1: Impact of column fixed pattern noise (CFPN) reduction on image quality: (a) Image with 3% CFPN and (b) Image with 1% CFPN

4.1. IMAGE SENSOR SYSTEM SPECIFICATION

4.1.1. NOISE SPECIFICATION OF IMAGE SENSOR

To understand how to enhance the readout speed effectively, it is essential to first analyze the sources of noise that impact image quality. According to EMVA1288 standard [1], fixed pattern noise (FPN) and temporal noise are crucial factors that significantly impact image quality. The fundamental causes of these two factors and their impacts on image quality are as follows.

Fixed pattern noise (FPN), mainly caused by pixel-to-pixel offset variations, can appear as column-wise fixed pattern noise (CFPN) or row-wise fixed pattern noise (RFPN). It is measured as dark signal non-uniformity (DSNU) in the absence of light and as photo response non-uniformity (PRNU) under illumination. Both DSNU and PRNU are mainly influenced by pixel characteristics. The main contributors generating the FPN are electron-hole pair generation in the depletion region of reverse-biased p-n junctions, diffusion currents from minority carriers, and surface currents caused by lattice structure discontinuities [2]. In addition, the offset variations in each readout channel contribute to FPN. The column-parallel ADC layout often results in unavoidable offset variations due to the challenge of maintaining symmetry within strict layout constraints, requiring the use of correlated double sampling (CDS) [3], [4], [5] or digital double sampling (DDS) to mitigate FPN [6]. Digital column switching (DCS) can also convert FPN into temporal noise [7].

Since the FPN is inevitable due to the physical area limitation, establishing realistic design targets becomes essential for managing the image quality. For example, one study [7] demonstrates the impact of improving FPN performance from 3% to 1%. As shown in Figure 4.1, the image with 1% FPN in Figure 4.1(b) is almost free of visible FPN compared to the 3% FPN image in Figure 4.1(a). Furthermore, merely achieving low FPN does not ensure superior image quality; it is also vital to minimize peak FPN values.

In addition to FPN, temporal noise is another major factor that affects image quality, and it arises from different physical phenomena, including three primary types: thermal noise, shot noise, and 1/f noise. First, shot noise is the noise that exists in electronic de-

vices, which originates from the discrete nature of the electric charge. For instance, if the generated electrons from the incident light is N, the shot noise corresponding to N electrons is $\sqrt{N}$. Second, the 1/f noise, which is also called flicker noise, mainly originates from the electronic device's defect. The 1/f noise primarily consists of a low-frequency factor, and the 1/f noise can be eliminated by the CDS algorithm [3]. The 1/f noise impacts the input transistor of the source follower or the input transistor of the PGA. Third, the thermal noise measured in the image sensor can be classified into reset noise and read noise. As mentioned in [8], [9], [10], reset noise is generated in the pixel, and the reset noise originates when the pixel samples the reset level at the FD node. In addition to the reset noise from the pixel, the readout circuit, such as ADC, contributes to the noise.

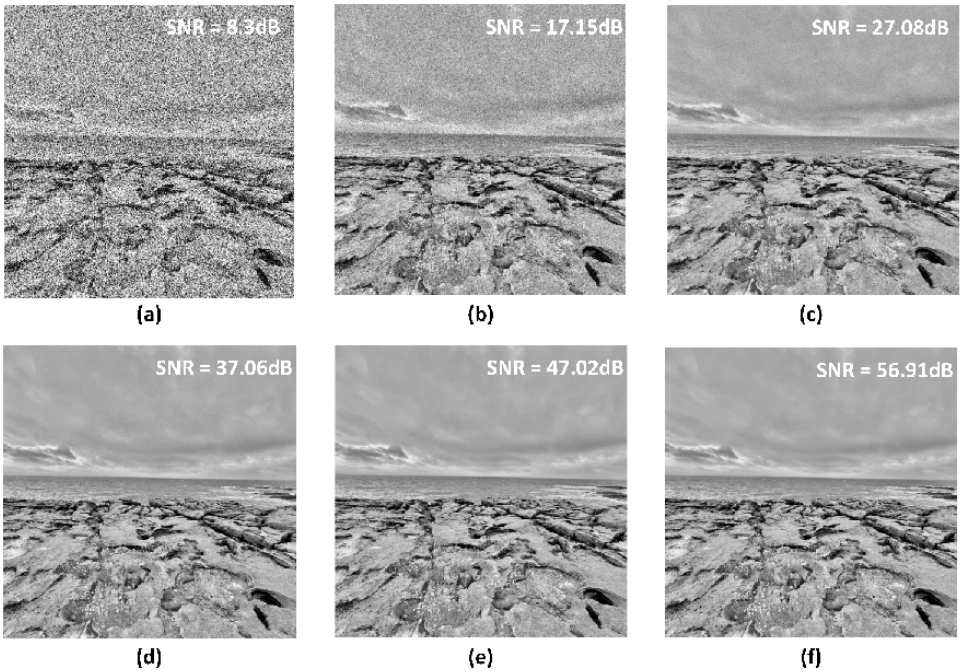


Figure 4.2: Temporal noise effects on image in different SNR condition

Temporal noise also affects image quality. Figure 4.2 illustrates the effect of temporal noise on the image [11]. The 6 images exhibit varying levels of temporal noise, each corresponding to a different signal-to-noise ratio (SNR). Specifically, the noise levels have been adjusted to match SNR values of 8.3dB, 17.15dB, 27.08dB, 37.06dB, 47.02dB, and 56.91dB, demonstrating the impact of increasing noise as SNR decreases. These SNR levels were synthetically generated by injecting Gaussian noise into a clean reference image using floating-point precision. The resulting images were then scaled and quantized to 8-bit for visualization. Although the theoretical SNR limit for 8-bit quantization is approximately 48dB, the inclusion of higher SNR values in the simulation allows for a clearer visual comparison across a wider dynamic range. As the SNR decreases, the

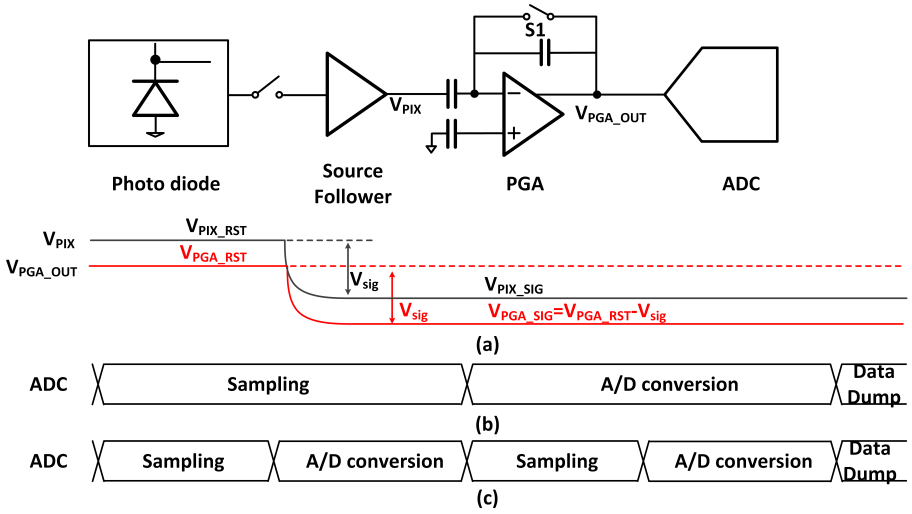


Figure 4.3: (a) Image sensor readout structure in a single channel, (b) timing diagram for applying CDS to remove pixel reset level variation and (c) DDS timing diagram for reducing pixel and readout circuit offset variations

shape of the vegetation in the lower central region of the image becomes indistinct. Furthermore, noticeable noise artifacts become visible in the cloud structures when the SNR falls below 37dB. Therefore, the appropriate temporal noise target is essential, depending on the sensor operation condition.

4.1.2. PIXEL READOUT WITH CDS ALGORITHM

Given the limited space for circuit integration within sensors, addressing noise reduction solely through hardware design is impractical. Thus, the correlated double sampling (CDS) algorithm emerges as a pivotal technique for enhancing image quality. The CDS algorithm utilizes the pixel's reset level as a reference; the pixel output, which corresponds to the integrated charge, is derived from the difference between the reset and signal levels.

The CDS algorithm has been applied in 2 different ways in previous research. First, the CDS algorithm is used only in the analog domain to remove the reset level variation at the pixel output [5], [12], [13]. Figure 4.3(a) shows the image sensor readout structure in a single channel, and the PGA and pixel output are described together. As shown in the timing, the pixel outputs the reset level and signal level to apply the CDS algorithm. The PGA regulates the signal level suitable for the ADC. Figure 4.3(b) shows the timing diagram that involves applying CDS algorithms to remove the pixel output's reset level variation. As described in the timing diagram in Figure 4.3(b), the ADC samples the reset level and signal level. After sampling, the ADC converts the difference of the sampled data into digital code. Therefore, the CDS technique minimizes the pixel's offset variation. However, this CDS algorithm doesn't remove the offset from the ADC.

While analog CDS effectively reduces reset level variations at the pixel output, digital

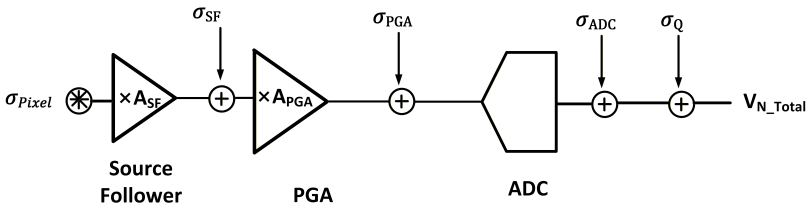


Figure 4.4: Simplified noise model of the image sensor readout circuit

double sampling (DDS) reduces the offset variation including the offset from the readout circuit in digital domain [6], [14], [15]. As shown in Figure 4.3(c), the ADC performs data conversion 2 times after sampling reset level and signal levels. Since each conversion contains the same offset from the pixel and readout circuit, the DDS technique can efficiently remove the offset variation, and the FPN performance is relatively better than the CDS applied only in the analog domain. However, since this algorithm performs digital domain CDS, the ADC must convert data conversion 2 times. This double data conversion takes more time and consumes twice the power of analog domain CDS. Moreover, the longer CDS interval worsens temporal noise performance in the low-frequency domain.

For this project, we opted for analog CDS to minimize processing time and reduce power consumption compared to DDS. We will manage offsets from the readout circuit using additional techniques to reduce FPN. Understanding these noise sources is essential for designing an effective readout circuit that maximizes frame rate while maintaining high image quality, as discussed in subsequent sections.

4.2. READOUT CIRCUIT FOR TEMPORAL NOISE IMPROVEMENT

4.2.1. THEORETICAL ANALYSIS WITH NOISE MODEL

To systematically evaluate temporal noise throughout the entire readout path, this work introduces a comprehensive five-source noise model specifically formulated for image sensor readout circuits. Unlike conventional analyses that focus only on pixel or ADC noise, the proposed model comprehensively integrates all dominant RMS noise contributors from the photodiode to the ADC output, enabling a unified understanding of temporal-noise propagation. The five primary root-mean-square (RMS) noise sources are defined as follows:

- **Photodiode RMS noise** (σ_{pixel}) — Arises from the intrinsic properties of the photodiode.
- **Source-follower RMS noise** (σ_{SF}) — Caused by thermal noise within the source-follower transistor.
- **PGA RMS noise** (σ_{PGA}) — Originates from the PGA, depending on its gain configuration.
- **ADC RMS noise** (σ_{ADC}) — Results primarily from comparator noise.

- **Quantization RMS noise** (σ_Q) — Caused by the finite resolution of the ADC.

Figure 4.4 illustrates the proposed noise model of the image-sensor readout chain, where A_{SF} and A_{PGA} denote the gains of the source follower and PGA, respectively (with $A_{\text{SF}} = 1$). The total output-referred noise is expressed as

$$\sigma_{\text{Total}} = \sqrt{A_{\text{PGA}}^2\left(\sigma_{pixel}^2 + \sigma_{SF}^2\right) + \sigma_{PGA}^2 + \sigma_{ADC}^2 + \sigma_Q^2}. \tag{4.1}$$

In this work, the SAR-ADC-based readout structure is analyzed using this model, where each noise term is defined according to the circuit topology and pixel type employed in the chain.

First, the RMS noise from the PGA (σ_{PGA}) becomes negligible when the analog-gain stage is bypassed [16]. When active, its internal noise is suppressed by the feedback loop gain L in the total noise calculation.

Second, the thermal noise from the pixel depends on the pixel architecture. In an ideal 4T pixel, the thermal reset noise associated with the floating diffusion (FD) node can be theoretically eliminated by correlated double sampling (CDS) because the reset and signal levels are sampled from the same node and are thus fully correlated. In practice, however, residual noise remains due to non-ideal switch resistance and source-follower noise. In contrast, in a 3T-type pixel, the FD node is completely reset between the two samples, leading to uncorrelated levels that CDS cannot cancel.

Third, the quantization noise depends on ADC resolution and is expressed as

$$\sigma_Q = \frac{\Delta V_{\text{1LSB}}}{\sqrt{12}}, \tag{4.2}$$

where ΔV_{1LSB} is the analog step corresponding to one LSB. As the ADC resolution increases, ΔV_{1LSB} decreases, thereby reducing σ_Q.

In this project, the noise sources of the modified 3T-type pixel (Section 2.2.1) are modeled as the combined contributions of the photodiode and the first source follower. Because the pixel operation sequence follows that of a 4T pixel, the kT/C reset noise from the photodiode is negligible. The dominant temporal noise therefore originates from the sampling network and the two source followers. The following subsections analyze these mechanisms in detail.

4.2.2. TEMPORAL NOISE FROM THE MODIFIED 3T-TYPE PIXEL

From Figure 4.4 and the total noise in Equation (4.1), the photodiode and its source followers contribute nearly half of the total readout noise power. Since the thermal noise sampled at the FD node during the reset and signal phases is cancelled by correlated double sampling (CDS), its contribution can be neglected. This section focuses on the temporal-noise behavior of the modified 3T-type pixel, where the main contributors are the two source followers and the sampling network.

Figure 4.5 illustrates the switch timing and control scheme of the modified 3T-type pixel. During the reset phase (T_1), the FD node is driven to V_R by turning on M_{RG}, as shown in Figure 4.5(a). At this moment, the thermal noise generated by the reset transistor is sampled onto the FD node, producing an instantaneous thermal-noise component

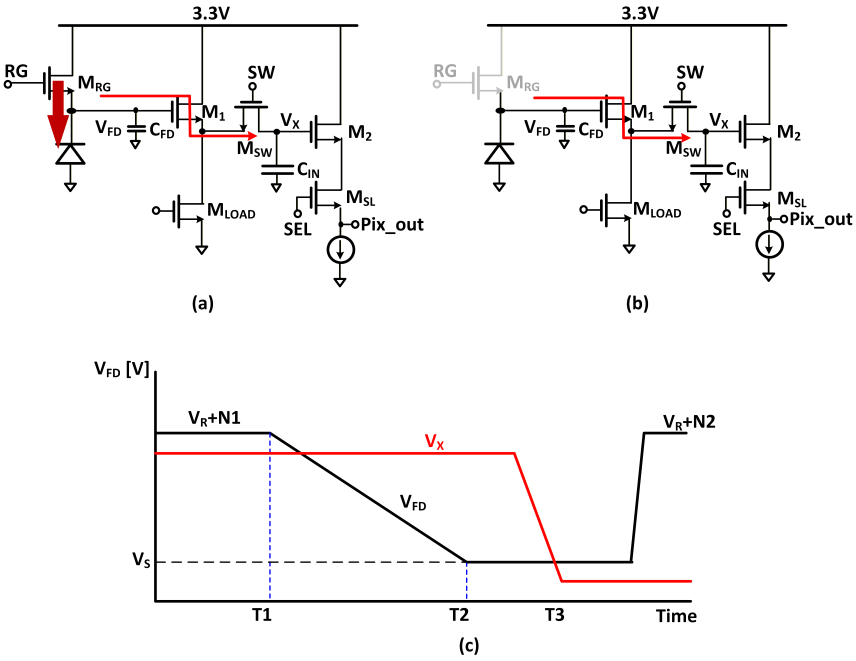


Figure 4.5: (a) Switch control during the reset period T_1, (b) switch control after sampling to preserve the reset level and its thermal noise, and (c) timing diagram showing reset and signal-level sampling

N_1:

$$V_{\mathrm{FD}}(T_1) = V_R + N_1. \tag{4.3}$$

Immediately afterward, the sampling switch M_{SW} stores this potential onto C_{IN}. After preserving the reset level, the photodiode begins integrating charge. When the ADC completes the conversion of the reset level, a second sampling occurs at time T_2 (Figure 4.5(c)), yielding

$$V_{\mathrm{FD}}(T_2) = V_R - \frac{N_e Q_e}{C_{\mathrm{FD}}} + N_1, \tag{4.4}$$

where C_{FD} is the FD-node capacitance, N_e is the number of integrated electrons, and Q_e is the elementary charge. The CDS output, i.e., the difference between these two samples, is

$$V_{\mathrm{FD}}(T_1) - V_{\mathrm{FD}}(T_2) = \frac{N_e Q_e}{C_{\mathrm{FD}}}. \tag{4.5}$$

Because the FD node is not reset again between the two samples, the same noise component N_1 appears in both and is therefore fully cancelled by CDS. The remaining output-referred noise thus arises primarily from the two source followers and the sampling network.

Figure 4.6 presents a simplified circuit of a single source follower driving a capacitive load, which is analyzed to establish the fundamental thermal-noise expression. In this

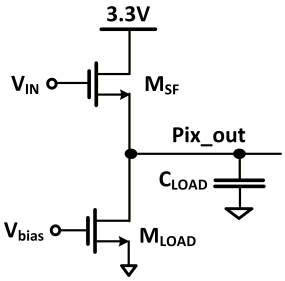


Figure 4.6: Single source follower driving the sampling/load capacitor C_{LOAD}. The output node `Pix_out` is loaded by C_{LOAD}, while M_{LOAD} provides the bias current

work, this model is re-applied to the two source followers in the modified 3T-type pixel to quantitatively evaluate their combined temporal-noise contribution in the complete readout path.

Based on this analytical foundation and following the formulation in Section 7.4.3 of [17], the output-referred power spectral density (PSD) of a single source follower (excluding flicker noise) is

$$S_{v,\mathrm{SF}}(f) = 4kT\gamma\left(\frac{1}{g_{m,\mathrm{SF}}}\right)\left(1+\frac{g_{m,\mathrm{LOAD}}}{g_{m,\mathrm{SF}}}\right), \tag{4.6}$$

where γ is the channel excess-noise factor (typically $\approx 2/3$), $g_{m,\mathrm{SF}}$ and $g_{m,\mathrm{LOAD}}$ denote the transconductances of the transistor M_{SF} and its load transistor M_{LOAD}, respectively, k is the Boltzmann constant, and T is the absolute temperature.

Since the source follower together with the load capacitance C_{LOAD} forms a first-order low-pass network, its frequency response can be expressed as

$$H(f) = \frac{1}{1+j2\pi f\, C_{\mathrm{LOAD}}/g_{m,\mathrm{SF}}}. \tag{4.7}$$

Here, C_{LOAD} is the total load capacitance at the output node, which dominantly determines the output pole of the source-follower stage. This low-pass behavior shapes the output noise spectrum and determines the effective noise bandwidth.

The total output-noise power is obtained by integrating the PSD over all frequencies:

$$\sigma^2_{\mathrm{SF}} = \int_0^\infty S_{v,\mathrm{SF}}(f)\,|H(f)|^2\,df = \frac{kT}{C_{\mathrm{LOAD}}}\gamma\left(1+\frac{g_{m,\mathrm{LOAD}}}{g_{m,\mathrm{SF}}}\right), \tag{4.8}$$

where σ_{SF} denotes the RMS output-referred noise voltage of the source follower.

In this design, the ratio $g_{m,\mathrm{SF}} \approx 2g_{m,\mathrm{LOAD}}$ is used, yielding

$$\sigma^2_{\mathrm{SF}} = 1.5\gamma\frac{kT}{C_{\mathrm{LOAD}}} \approx \frac{kT}{C_{\mathrm{LOAD}}}. \tag{4.9}$$

Thus, the thermal noise approaches the fundamental kT/C limit and is inversely proportional to the load capacitance.

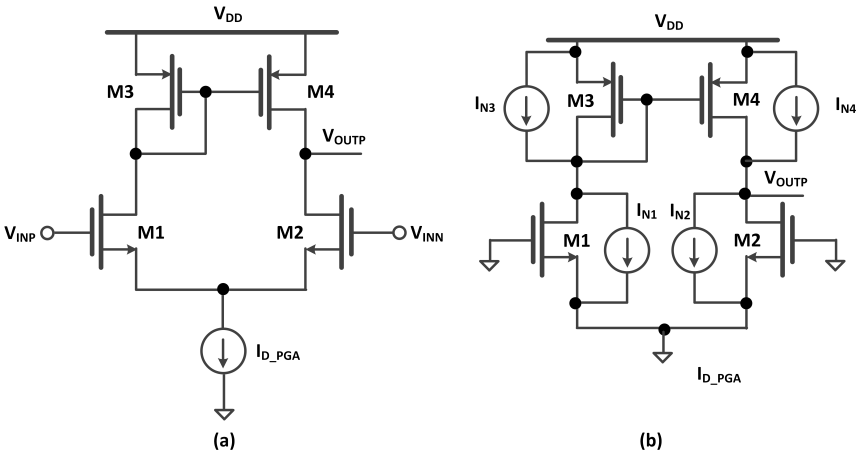


Figure 4.7: (a) Differential amplifier inside the PGA and (b) its dominant thermal-noise sources

Applying this to the modified structure shown in Figure 4.5, the first source follower in the pixel chain drives the sampling capacitor C_{IN} ($C_{\mathrm{LOAD}} = C_{\mathrm{IN}}$), while the second source follower, located at the readout buffer stage, drives the PGA input sampling capacitor ($C_{\mathrm{LOAD}} = C_{\mathrm{PGA}}$). Because the thermal-noise contributions from these two source followers are uncorrelated, their variances add in the total output-referred noise.

In this design, $C_{\mathrm{IN}} \approx 30\,\mathrm{fF}$—significantly larger than the FD-node capacitance of a conventional 3T-type pixel—so the sampled noise through the first source follower is much smaller than the kT/C_{FD} noise observed in a conventional 3T-type pixel, whereas the noise contributed by the second source follower remains comparable. Consequently, the modified 3T-type pixel achieves a substantially lower temporal-noise floor, confirming that the sampling network, rather than the FD node, dominates the in-band thermal noise.

4.2.3. THE TEMPORAL NOISE OF THE ADC SAMPLING NETWORK AND PGA

After being buffered by the column source follower, the pixel output is fed into the PGA stage, which provides the adjustable analog gain of the readout chain and defines the effective noise bandwidth seen by the ADC. The PGA is implemented as a differential amplifier (Figure 4.7), where its dominant thermal-noise sources are transistors M1–M4, while the tail-current source contribution is negligible.

From the noise model in Figure 4.7 (b), the intrinsic current-noise power spectral density (PSD) of the PGA is expressed as

$$S_{i,\mathrm{PGA}}(f) = 4kT\gamma \sum_{i=1}^{4} g_{m,i}, \tag{4.10}$$

where $g_{m,i}$ denotes the transconductance of each transistor M_i (i = 1–4).

The feedback model for the closed-loop PGA is illustrated in Figure 4.8. Under the

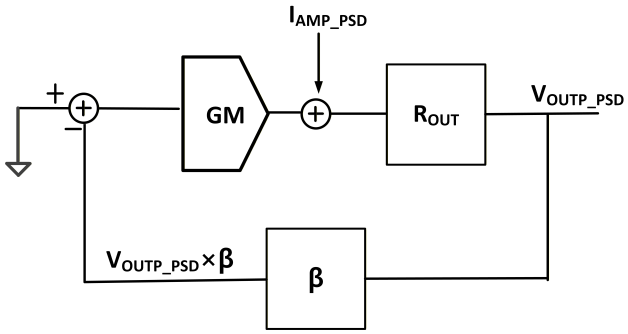


Figure 4.8: Feedback model for closed-loop PGA noise transfer

feedback network, the loop gain $L(f)$ is given by

$$L(f) = \beta GM R_{\mathrm{OUT}}(f), \tag{4.11}$$

where β is the feedback factor, GM is the effective transconductance of the input differential pair (approximately equal to g_{m1}), and R_{OUT} is the small-signal output impedance of the amplifier stage.

The corresponding output-referred voltage-noise PSD from the PGA is

$$S_{v,\mathrm{PGA}}(f) = 4kT\gamma \frac{R_{\mathrm{OUT}}^2}{(1+\beta GM R_{\mathrm{OUT}})^2} \sum_{i=1}^{4} g_{m,i}, \tag{4.12}$$

where R_{OUT} is the open-loop output impedance of the amplifier. As shown in Equation (4.12), the output noise is strongly suppressed by the loop gain $1+\beta GMR_{\mathrm{OUT}}$. In unity-gain operation ($A_{\mathrm{CL}} \approx 1$) with $A_{\mathrm{OL}} = GMR_{\mathrm{OUT}} \sim 100$, this term is reduced by approximately 40 dB, making the PGA's own noise contribution negligible.

PGA bandwidth as the effective noise low-pass filter. The source follower in the pixel generally has a wider bandwidth than the PGA; hence, its noise is low-pass-filtered by the PGA. With ADC sampling capacitor C_{SAMP} at the PGA output, the closed-loop bandwidth is approximated by

$$f_{\mathrm{PGA\_GB}} = \frac{GM}{2\pi C_{\mathrm{SAMP}}}, \tag{4.13}$$

and the corresponding magnitude response is

$$H_{\mathrm{PGA}}(f) = \frac{1}{1+j2\pi f C_{\mathrm{SAMP}}/GM}, \qquad |H_{\mathrm{PGA}}(f)|^2 = \frac{1}{1+(2\pi f C_{\mathrm{SAMP}}/GM)^2}. \tag{4.14}$$

As shown in Figure 4.9, the ADC sampling capacitor defines the effective noise bandwidth at the PGA output. Because $S_{v,\mathrm{PGA}}(f)$ in Equation (4.12) is divided by the loop gain, the dominant noise at the ADC input is the source-follower thermal noise integrated over the PGA bandwidth in (4.13).

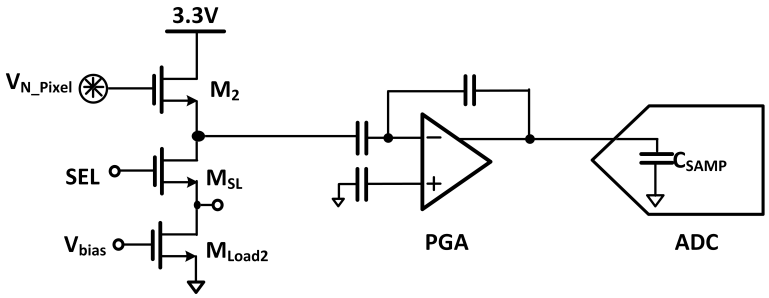


Figure 4.9: ADC sampling network and PGA interface used in temporal-noise analysis

During A/D conversion, additional noise components arise from the ADC itself—primarily comparator noise and quantization noise. In this design, the ADC performs a single differential conversion in which the reset and signal levels are applied to the positive and negative inputs, respectively. These noise sources originate within the conversion process, remain unaffected by the correlated-double-sampling (CDS) operation, and are statistically independent of the analog front-end noise. Their magnitudes are set by design parameters (e.g., comparator input-referred noise and ADC resolution) and are treated as fixed constants in the overall noise budget and dynamic-range estimation.

Design point. The source follower and PGA bias currents are $2\,\mu$A and $6\,\mu$A, respectively. With these values, the closed-loop transconductance and sampling capacitor yield a bandwidth of $f_{\mathrm{PGA\_GB}} \approx 2.86\,\mathrm{MHz}$, corresponding to a time constant of about 55 ns. This time constant ensures that the sampled signal settles within approximately $\frac{1}{4}$ LSB accuracy during the $\sim 500\,\mathrm{ns}$ ADC sampling window, providing adequate settling margin for accurate charge transfer.

Thus, (i) the PGA noise remains negligible, and (ii) the bandwidth properly limits the integrated source-follower noise while maintaining analog-gain programmability. With $\tau \approx 55\,\mathrm{ns}$, the residue settles by $e^{-500/55} \approx 1.13 \times 10^{-4}$ ($\approx 0.011\%$), comfortably below the 10-bit (0.098%) accuracy target.

4.2.4. TEMPORAL NOISE INCLUDING THE CDS OPERATION

Correlated double sampling (CDS) is a key technique for reducing temporal noise, particularly effective in suppressing low-frequency ($1/f$) components. In this design, CDS is implemented by sequentially sampling the reset and signal levels at the ADC input, as illustrated in Figure 3.15, and computing their difference within a single A/D conversion.

CDS acts on the noise appearing at the outputs of the source followers and the PGA. However, the PGA's output-referred noise is strongly attenuated by its large loop gain (Section 4.2.3) and can be neglected. Therefore, CDS mainly affects the noise from the two source followers shown in Figure 4.5.

Due to the sensor operation sequence, the two CDS intervals differ. The first source

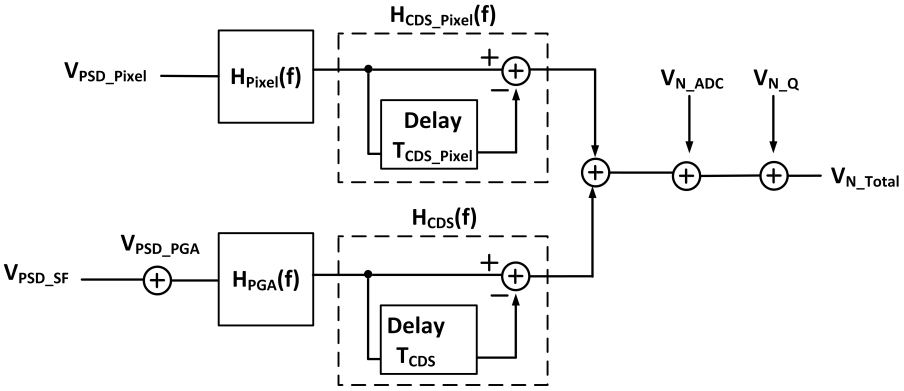


Figure 4.10: System block diagram incorporating the CDS algorithm into the temporal-noise analysis

follower inside the pixel is sampled across the charge-integration period, while the second source follower in the column buffer (preceding the PGA) is sampled across the ADC reset–signal interval, typically a few hundred nanoseconds. Considering these distinct intervals, the readout noise propagation under CDS is modeled by the system block diagram in Figure 4.10.

CDS transfer function. CDS samples the same node at two instants separated by a fixed interval T_{CDS} and computes their difference, using the first sample as a reference to extract the relative change of the signal while canceling correlated noise. Following the analytical formulations presented in [18], [19], the CDS transfer function in the frequency domain is expressed as

$$H_{\mathrm{CDS}}(f) = 1 - e^{-j2\pi f T_{\mathrm{CDS}}}, \tag{4.15}$$

and its magnitude response is

$$|H_{\mathrm{CDS}}(f)|^2 = 4\sin^2(\pi f T_{\mathrm{CDS}}) = 2(1-\cos(2\pi f T_{\mathrm{CDS}})). \tag{4.16}$$

Thus, the CDS acts as a discrete-time high-pass filter that strongly suppresses low-frequency components such as flicker noise and offset, while allowing thermal noise within the signal band to pass almost unchanged. When this high-pass characteristic is combined with the first-order low-pass response of the PGA described in (4.13), the overall noise-transfer function can be expressed as

$$H_{\mathrm{TF}}(f) = H_{\mathrm{CDS}}(f)H_{\mathrm{PGA}}(f) = \frac{1 - e^{-j2\pi f T_{\mathrm{CDS}}}}{1 + j2\pi f C_{\mathrm{SAMP}}/G_M}. \tag{4.17}$$

Figure 4.11 shows the frequency responses of the CDS high-pass filter, the PGA low-pass filter, and their combined transfer function. The CDS operation attenuates low-frequency correlated and $1/f$ noise components, while the PGA limits high-frequency thermal noise through its finite bandwidth. In practice, the bandwidth of the source follower is designed slightly higher than that of the PGA, so the overall noise bandwidth

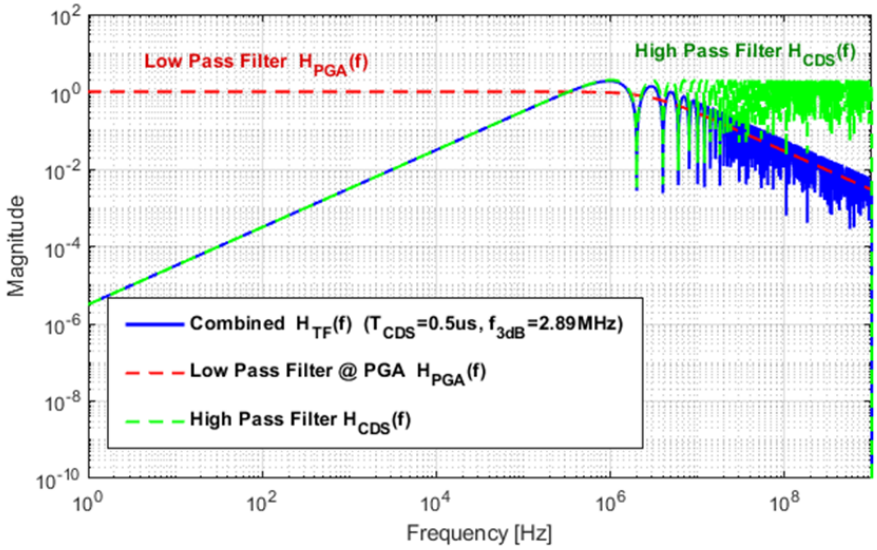


Figure 4.11: Frequency responses of the CDS,PGA, and their combined function

is effectively limited by the PGA response. As a result, the combined response exhibits a band-pass characteristic that defines the effective temporal-noise bandwidth of the readout chain. The relationship between the CDS interval and the PGA bandwidth determines the overall integrated noise power and thus the temporal-noise floor of the system.

Source-follower noise with CDS and LPF shaping. The correlated-double-sampling (CDS) transfer function derived in Section 4.2.2 is now applied to the single source-follower model discussed earlier in Figure 4.6. Using the previously defined overall transfer function $H_{\mathrm{TF}}(f)$, it is applied to the source follower and denoted as $H_{\mathrm{TF,SF}}(f)$. The total output-referred noise of each source follower is then evaluated by integrating its voltage-noise power spectral densities (PSDs) as

$$\sigma^2_{\mathrm{SF,CDS}} = \int_0^\infty \left[S_{v,\mathrm{th}}(f) + S_{v,1/f}(f)\right] |H_{\mathrm{TF,SF}}(f)|^2 \, df. \tag{4.18}$$

where $S_{v,\mathrm{th}}(f)$ and $S_{v,1/f}(f)$ represent the thermal and flicker-noise PSDs of the source follower, respectively.

Since the thermal and flicker noise components originate from distinct physical mechanisms, they are statistically uncorrelated and can therefore be treated separately:

$$\sigma^2_{\mathrm{SF,CDS}} = S_{v,\mathrm{th}} \int_0^\infty |H_{\mathrm{TF,SF}}(f)|^2 \, df + \frac{K_f}{C_{\mathrm{ox}}^2 W L} \int_0^\infty \frac{|H_{\mathrm{TF,SF}}(f)|^2}{f} \, df. \tag{4.19}$$

Here (revisiting Equation (4.6)),

$$S_{v,\mathrm{th}} = 4kT\gamma \left(\frac{1}{g_{m,\mathrm{SF}}}\right)\left(1 + \frac{g_{m,\mathrm{LOAD}}}{g_{m,\mathrm{SF}}}\right), \tag{4.20}$$

where $g_{m,\mathrm{SF}}$ and $g_{m,\mathrm{LOAD}}$ are the transconductances of the source-follower and its load transistor in Figure 4.6, respectively.

The flicker-noise power spectral density is modeled according to Section 7.2.2 of [17] as

$$S_{v,1/f}(f) = \frac{K_f}{C_{\mathrm{ox}}^2 W L f}, \tag{4.21}$$

where K_f is the flicker-noise coefficient of the MOS transistor, C_{ox} is the gate-oxide capacitance per unit area, and W and L are the device width and length.

Substituting the combined transfer function into (4.19), the thermal-noise contribution becomes

$$\sigma_{\mathrm{th,CDS}}^2 = S_{v,\mathrm{th}} \int_0^\infty \frac{2\big(1-\cos(2\pi f T_{\mathrm{CDS}})\big)}{1+(2\pi f\tau)^2}\, df, \qquad \tau = \frac{C_{\mathrm{SAMP}}}{G_M}, \tag{4.22}$$

where T_{CDS} is the CDS interval, C_{SAMP} is the sampling capacitor, and G_M is the effective transconductance of the PGA stage.

Evaluating this integral yields a closed-form expression:

$$\sigma_{\mathrm{th,CDS}}^2 = S_{v,\mathrm{th}} \cdot \frac{1}{2\tau}\big(1-e^{-T_{\mathrm{CDS}}/\tau}\big) = S_{v,\mathrm{th}} \cdot \frac{G_M}{2C_{\mathrm{SAMP}}}\Big(1-e^{-T_{\mathrm{CDS}} G_M / C_{\mathrm{SAMP}}}\Big). \tag{4.23}$$

The flicker-noise component is similarly obtained as

$$\sigma_{1/f,\mathrm{CDS}}^2 = \frac{K_f}{C_{\mathrm{ox}}^2 W L} \int_0^\infty \frac{2\big(1-\cos(2\pi f T_{\mathrm{CDS}})\big)}{f\,[1+(2\pi f\tau)^2]}\, df, \tag{4.24}$$

which can be approximated by a logarithmic dependence between the CDS interval T_{CDS} and the LPF time constant τ:

$$\sigma_{1/f,\mathrm{CDS}}^2 \approx \frac{K_f}{C_{\mathrm{ox}}^2 W L} \cdot \frac{1}{2} \ln\Big(1+\alpha\,\frac{T_{\mathrm{CDS}}}{\tau}\Big), \qquad \alpha \approx 1, \tag{4.25}$$

where α is an empirical constant of order unity that accounts for the finite low- and high-frequency bounds of the $1/f$ spectrum.

Finally, the total output-referred noise of the source follower including both thermal and flicker terms is

$$\boxed{\sigma_{\mathrm{SF,CDS}}^2 = S_{v,\mathrm{th}} \cdot \frac{1}{2\tau}\big(1-e^{-T_{\mathrm{CDS}}/\tau}\big) + \frac{K_f}{C_{\mathrm{ox}}^2 W L} \cdot \frac{1}{2} \ln\Big(1+\alpha\,\frac{T_{\mathrm{CDS}}}{\tau}\Big)} \tag{4.26}$$

The total output-referred noise in equation 4.26 can be further simplified depending on the relation between the CDS interval T_{CDS} and the system time constant τ.

Depending on the time constant τ, two limiting cases can be identified:

$$\text{If } T_{\mathrm{CDS}} \ll \tau: \quad \sigma_{\mathrm{th}}^2 \approx S_{v,\mathrm{th}} \frac{T_{\mathrm{CDS}}}{2\tau^2}, \quad \sigma_{1/f}^2 \approx \frac{K_f}{C_{\mathrm{ox}}^2 W L} \cdot \frac{\alpha}{2} \frac{T_{\mathrm{CDS}}}{\tau}.$$

$$\text{If } T_{\mathrm{CDS}} \gg \tau: \quad \sigma_{\mathrm{th}}^2 \approx S_{v,\mathrm{th}} \frac{1}{2\tau}, \quad \sigma_{1/f}^2 \approx \frac{K_f}{C_{\mathrm{ox}}^2 W L} \cdot \frac{1}{2} \ln\Big(\alpha\,\frac{T_{\mathrm{CDS}}}{\tau}\Big).$$

Table 4.1: Estimated RMS noise contributions of individual components (μV_{RMS}, differential)

Noise Source	Thermal	$1/f$	Total
Photodiode	~0	~0	~0
SF1 (Pixel)	142	470	491
SF2 (Column)	77.6	56.3	95.9
PGA	$\ll$30	–	$\ll$30
ADC Comparator	–	–	135
Quantization	–	–	**169**
System Total			**545**

In practical implementation, T_{CDS} is typically set to at least 9–10 times the sampling-network time constant to guarantee full settling for 10–12 bit accuracy. Under this condition ($T_{CDS} \gg \tau$), the thermal-noise component reaches its steady-state limit and the two sampled signals become uncorrelated, so CDS cannot further suppress thermal noise. In contrast, flicker noise remains dependent on T_{CDS}; a shorter interval raises the high-pass corner of the CDS filter, effectively reducing low-frequency $1/f$ noise. Thus, T_{CDS} is minimized within the settling constraint to balance conversion accuracy and low-frequency noise suppression.

4

NOISE ESTIMATION

Based on the analytical model derived in Section 4.2, the total temporal noise of the readout chain was estimated using the following expression:

$$\sigma_{\text{Total}} = \sqrt{\sigma_{\text{SF1}}^2 + \sigma_{\text{SF2}}^2 + \sigma_{\text{ADC+PGA}}^2 + \sigma_Q^2}.$$

Each term represents the RMS noise contribution from the two source followers in Figure 4.5 (σ_{SF1}, σ_{SF2}), the ADC–PGA path ($\sigma_{\text{ADC+PGA}}$), and the quantization noise (σ_Q). The individual noise components were calculated using the CDS–LPF model, with process parameters of $C_{ox} = 5$ fF/μm^2 and a flicker-noise constant of $K_f = 9 \times 10^{-26}$. This K_f value was chosen so that the predicted total noise matches the measured result of 0.50–0.56 mV_{RMS}.

The estimated results are summarized in Table 4.1. The first source follower located inside the pixel (SF1) dominates the total temporal noise due to its long CDS interval, which amplifies the low-frequency $1/f$ component, while the column source follower (SF2) contributes less because of its shorter sampling interval. The PGA noise is negligible owing to strong feedback suppression. The comparator noise (obtained from post-layout simulation) and the quantization noise were added as uncorrelated terms. It should be noted that the simulated comparator noise may appear slightly smaller than the actual value because transient simulations typically limit the minimum frequency range (f_{min}), which can underestimate the low-frequency noise contribution.

Overall, the predicted total temporal noise of approximately 0.54 mV_{RMS} agrees well with the measured data, confirming that the analytical model in Section 4.2 accurately represents the dominant noise mechanisms in the proposed readout chain. This model also forms the foundation for the fixed-pattern noise analysis and other theoretical discussions in the following chapters, and is experimentally validated by the measurement

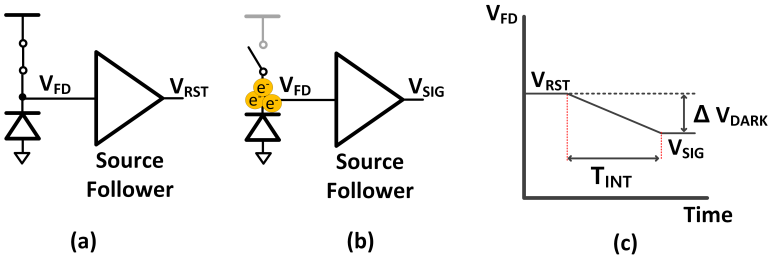


Figure 4.12: (a) Pixel and source follower circuit block diagram before charge integration, (b) pixel and source follower circuit block diagram after charge integration and (c) potential change at the FD node during integration and dark current error

results presented in Chapter 7. Having established the temporal-noise characteristics, the next section discusses fixed-pattern noise (FPN), emphasizing the spatial variations across the pixel array.

4.3. FPN COMPENSATION TECHNIQUES

4.3.1. FPN ORIGINS AND KEY CALIBRATION FACTORS

While minimizing the temporal noise is crucial for maintaining image quality, improving the VFPN performance is also significant. FPN arises from two primary sources: variations within the pixel array and inconsistencies in the readout circuitry.

First, the FPN originating from the pixel is mainly affected by the dark current, as mentioned in [1]. Figures 4.12(a) and (b) show the circuit block diagram of the pixel and source follower before the charge integration time and after the charge integration time. The potential change of the FD node, V_{FD}, is described in Figure 4.12(c). If the operation is performed under dark conditions, the potential at the FD node in both cases shown in Figure 4.12(a) and (b) should be the same. However, if there is a dark current, I_{DARK}, during the charge integration time T_{INT}, the sensor handles the output as if the charge is integrated under the illuminations. The error generated by the dark current, ΔV_{DARK}, is calculated as follows.

$$\Delta V_{DARK} = \frac{I_{DARK} \cdot T_{INT}}{C_{FD}} \tag{4.27}$$

Where CFD is the capacitance at the FD node, each pixel output varies when implemented in silicon, resulting in a different ΔV_{DARK} for each pixel. The variation of the ΔV_{DARK} becomes the FPN.

In addition to pixel variations, errors in the readout circuit also contribute significantly to FPN. The FPN within the readout circuit is generated when the image sensor reads the pixel without applying the DDS technique. Since the image sensor reads the pixel 2 times and subtracts the reset level and signal level with the DDS technique, as illustrated in [6], the subtraction cancels the readout circuit errors. Figure 4.13 depicts the circuit block diagram during the sampling period. As described in Figure 4.13, the pixel output corresponding to the reset level, V_{RST}, and signal level, V_{SIG}, are sequentially

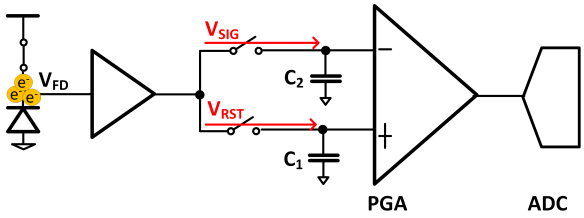


Figure 4.13: Circuit block diagram during pixel reset and signal level sampling in the readout circuit

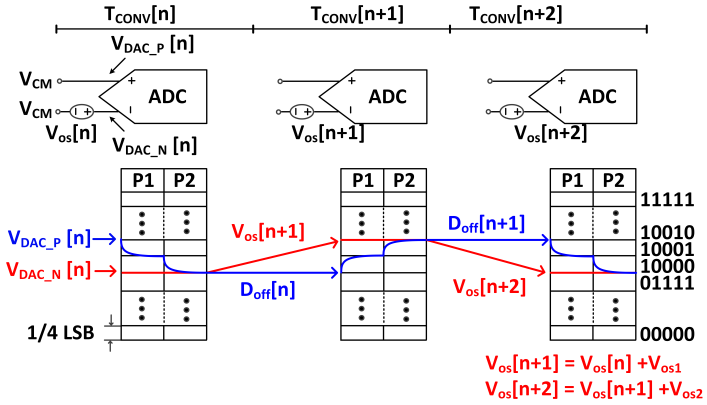


Figure 4.14: Offset calibration using memory to enable rapid offset correction

sampled at capacitors C_1 and C_2. After sampling, the PGA generates subtracted signals from the sampled signals, such as V_{RST} and V_{SIG}. During this operation, the reset level variation is compensated in the analog domain. The ADC only handles the difference between V_{RST} and V_{SIG}. For this reason, the ADC converts the input signal only once. If there is an error within the ADC or PGA, the error cannot be compensated.

For these reasons, since the DDS technique is not applied in this project, the FPN originating from the pixel and the readout circuit should be compensated. The solutions are discussed in the following section.

4.3.2. BACKGROUND COMPARATOR OFFSET CALIBRATION

THE CONCEPT OF THE OFFSET CALIBRATION

As mentioned in section 4.1, managing FPN is essential for maintaining high image quality. Since the image sensor is designed for a high frame rate operation, the DDS technique is not used, making it necessary to compensate for FPN from both the pixel and the readout circuit, as discussed in section 4.3.1. However, as the charge integration time needs to be short to support the high-frame-rate image sensor operation, FPN from the readout circuit becomes more prominent. At the same time, the FPN from the pixel is less significant. Additionally, the offset can vary slightly with each data conversion due to the continuously changing working conditions around the ADC. To address these

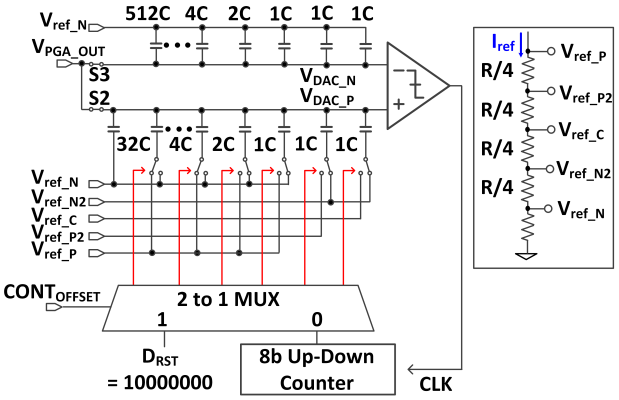


Figure 4.15: Capacitor DAC control with an 8-bit up-down counter for offset calibration

issues, background offset calibration is implemented in this design.

The background offset calibration uses memory, enabling rapid offset correction within two decision cycles. This fast calibration is necessary to support high-speed data conversion while maintaining a short CDS interval, effectively removing low-frequency temporal noise. Figure 4.14 illustrates how memory facilitates this fast offset calibration.

In this system, we assume that the offset, V_{OFF}, exists at the top plate of the negative capacitor DAC, V_{DAC_N}, and slightly varies at each conversion phase. Once the offset calibration begins, the ADC samples reset level, V_{CM}, at its positive and negative inputs. In n-th horizontal line time, $T_{CONV}[n]$, the potential level $V_{DAC\_N}[n]$ including offset at time $T_{CONV}[n]$ is given by:

$$V_{DAC\_N} = V_{CM} + V_{OFF}[n] \tag{4.28}$$

$V_{OFF}[n]$ is the offset during the period $V_{CONV}[n]$. Since the digital code controls the capacitor DAC, the compensation result, $D_{OFF}[n]$, is stored in a memory. When the stored compensation result is reused, the same amount of offset calibration is applied by controlling the capacitor DAC using $D_{OFF}[n]$. For this reason, in the following conversion at $T_{CONV}[n+1]$, the ADC only needs to compensate for the offset changes, V_{OS1}, which is the difference between $V_{OFF}[n+1]$ and $V_{OFF}[n]$. After offset calibration at $T_{CONV}[n+1]$, the offset calibration result should be accumulated and stored as a new offset calibration result, Doff[n+1], in the memory again. This process repeats in the subsequent conversion at $T_{CONV}[n+2]$, with each calibration requiring only two cycles per data conversion. This continuous accumulation of offset calibration data ensures precise compensation at each conversion phase.

THE IMPLEMENTATION OF THE OFFSET CALIBRATION

Setting an appropriate calibration step is crucial for implementing effective offset calibration and achieving the desired level of precision. This work sets the offset calibration step to 0.25LSB to ensure that the peak FPN remains below 0.5LSB. This 0.25LSB step

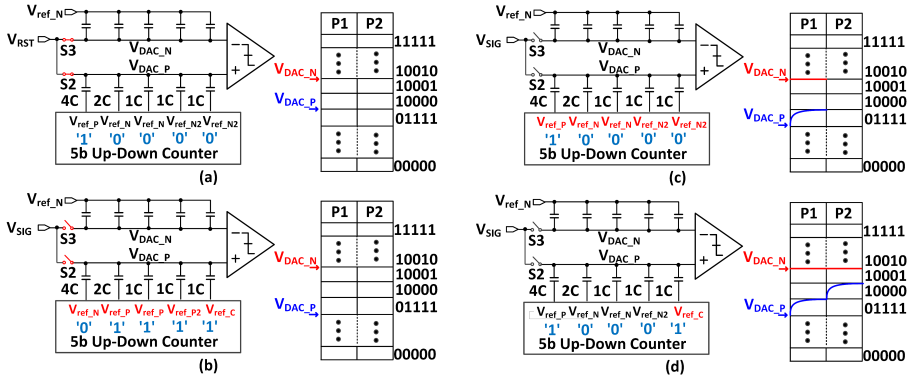


Figure 4.16: Offset-calibration sequence of the proposed ADC: (a) reset-level sampling, (b) signal-level sampling with DAC control, (c) first decision cycle of the calibration process, and (d) subsequent bit-decision and up–down counter update

allows for fine control over the compensation process, minimizing offset variations and preventing the FPN from exceeding the 0.5LSB.

This background offset calibration is designed using the ADC structure explained in Figure 3.7. Figure 4.15 shows an example of the capacitor DAC control accompanied by an 8-bit up-down counter for the offset calibration, and the offset cover range is ±32LSB. The offset calibration logic controls the capacitor DAC array of the positive input part. The reference voltages for 0.25LSB and 0.5LSB are generated from the resistor ladder shown in Figure 4.15. Therefore, two digits in the LSB part of the counter refer to 0.5LSB and 0.25LSB, respectively, and the unit capacitors controlled by these LSB parts use the reference voltage of V_{REFP2}, V_{REFN2} and V_{REFC}.

OFFSET CALIBRATION TIMING AND CONTROL

Figure 4.16 illustrates the example of the offset calibration procedure within a single horizontal line time. At the beginning, the ADC samples the reset level, and the bottom plate of all capacitors except for the 4C is connected to the negative reference, as shown in Figure 4.16(a). Once the reset sampling is complete, the switches S2 and S3 are turned off, disconnecting the reset level. Then, the bottom plate of the positive part of the capacitor DAC connects to the output of the up-down counter, as seen in Figure 4.16(b). The output of the positive capacitor DAC array, $V_{\mathrm{DAC\_P}}$, is given by:

$$V_{\mathrm{DAC\_P}} = V_{\mathrm{CM}} + (V_{\mathrm{MEM}} - V_{\mathrm{INIT}}) \cdot V_{1/4\mathrm{LSB}} \tag{4.29}$$

The $V_{1/4\mathrm{LSB}}$ represents the analog signal equivalent to 0.25LSB, while D_{INT} and D_{MEM} represent the counter's initial and memorized digital codes, respectively. Regarding the negative capacitor DAC output of $V_{\mathrm{CM}} + V_{\mathrm{OFF}}$ including the offset, the term (V_{MEM}-V_{INT})× $V_{1/4\mathrm{LSB}}$ estimates the offset V_{OFF}. The V_{MEM} is updated through the 2 decision cycles illustrated in Figure 4.16(c) and (d). In this procedure, the ADC compares the output of each capacitor DAC and controls the positive capacitor DAC array to estimate the offset. In each decision, the capacitor DAC is controlled by 0.25LSB. After 2 cycles of the offset

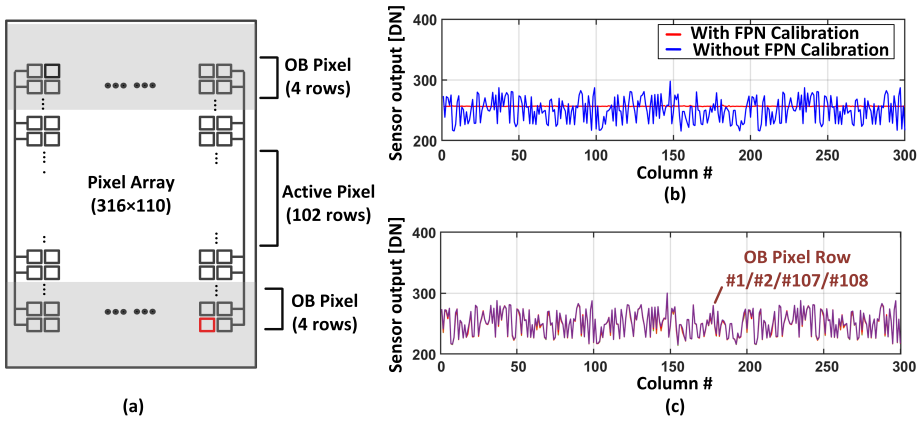


Figure 4.17: (a) Pixel array block diagram with optical black pixel for FPN calibration, (b) averaged output per column with and without FPN calibration and (c) averaged output of OB pixel for FPN calibration

calibration procedure, the up-down counter saves the digital outputs generated from the offset calibration until the next offset calibration. Since the counter memorizes the output until the next offset calibration, the offset can be re-estimated at the next calibration.

4.3.3. VFPN CALIBRATION UTILIZING OPTICALLY BLACK PIXEL

THE CONCEPTUAL EXPLANATION OF VFPN CALIBRATION USING OPTICALLY BLACK PIXEL

As explained in section 3.4, the advanced SAR ADC was designed to improve speed. However, the background offset calibration method in this design is not effective for three key reasons. First, it limits data conversion speed due to its 2-cycle offset calibration for each data conversion. Second, the offset calibration increases hardware complexity. The additional control lines required for the capacitor DAC make the layout more intricate. Due to the complicated area, the layout of the capacitor DAC is not good enough to guarantee linearity. Third, this offset calibration only compensates for the offset originating from the readout circuit. To further improve VFPN performance, it is also necessary to account for reset level variations from the pixel itself.

A solution has been implemented at the image sensor system level to address these issues. First, an optically black pixel array (OB pixel) is designed to enhance VFPN performance. The image sensor reads out the OB pixel to compensate for the FPN. Since the OB pixel outputs dark current information from each column, it allows for the compensation of FPN originating from both the pixel array and the readout circuit. Figure 4.17(a) shows the pixel array block diagram used in this design, with four lines of OB pixels positioned at the top and bottom of the array, specifically at vertical addresses 0 to 3 and 106 to 109. Due to design limitations of the design rule in the TowerJazz 180nm process technology, four OB pixel lines are the maximum allowable at each edge of the pixel array. Figure 4.17(b) depicts the average output per column with and without FPN calibration, while Figure 4.17(c) shows the average OB pixel output. As described in Figure 4.17(b) and (c), the averaged outputs from the OB pixel have a similar pattern to those from the

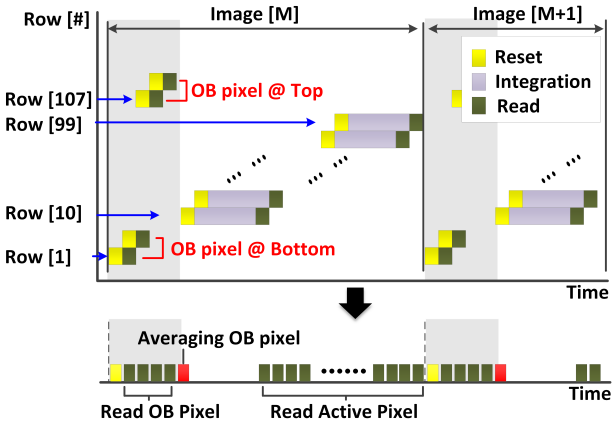


Figure 4.18: Timing diagram for FPN calibration using optical black pixel

active pixel array. Therefore, subtracting the OB pixel output from the active pixel output at each column effectively improves the VFPN performance.

Second, the offset calibration is performed before reading out the active pixel, which has real image data. Figure 4.18 shows the timing used in this FPN calibration. As described in Figure 4.18, the image sensor first reads the OB pixel at the top and bottom. Within the 4 lines at each part, only 2 lines are used to generate the averaged value at each column. Since the edge of the OB pixel at the top and bottom has light penetrating the pixel, the rest of the 2 lines at the top and bottom are not used. After reading the OB pixel, the image sensor reads the active pixel. The average OB pixel output is used to subtract the offset variation.

THE IMPLEMENTATION OF THE VFPN CALIBRATION WITH AN OPTICALLY BLACK PIXEL

The FPN correction algorithm requires a signal processing algorithm designed in an FPGA. Figure 4.19 describes the system block diagram of the FPN calibration algorithm. This algorithm consists of an FPN correction and an FPN estimation part. The calibration algorithm is implemented to process each column of data. As a result, since the pixel has 300 columns, 300 calibration algorithms are implemented to process each column output separately.

In the timing diagram in Figure 4.18, the system estimates the offset variation after reading out the OB pixel output. During reading out the OB pixel, the 11-bit input signal, $D_{IN}[n]$, is transmitted to the FPN estimation part inside the FPGA. Whenever the image reads the OB pixel, its input data, $D_{IN}[n]$, is accumulate and generates the 11-bit $D_{SUM}[n]$. Since the OB pixel's output cannot have higher code, the bit format of $D_{SUM}[n]$ is set to 11. After reading out 4 lines of OB pixels, the system generates the average output of the OB pixels, as shown in Figure 4.19. Since 4 data are accumulated, $D_{SUM}[n]$ is divided by 4, and for simple calculation, the last 2 bits of LSB are truncated. After truncation, two's complement is generated. The bit format should be 11. In addition, the expected dark level 256 is added. As a result, the final output $D_{FPN}[n]$ is the two's

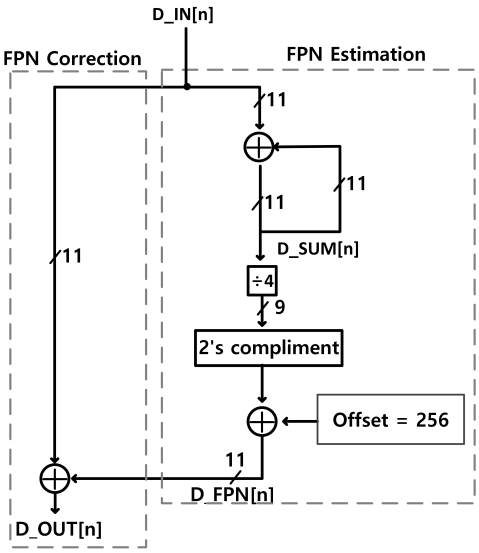


Figure 4.19: System block diagram of FPN calibration algorithm in FPGA

complement of the offset estimation.

When the signal processing is completed, the image sensor starts reading out active pixel array. During this procedure, the FPGA input signal DIN is directly sent to FPN correction part. The final output $D_{\mathrm{OUT}}[\mathrm{n}]$ is generated to be sent to the post processing part with the formula below.

$$D_{\mathrm{OUT}}[n] = D_{\mathrm{IN}}[n] + D_{\mathrm{FPN}}[n] \tag{4.30}$$

Figure 4.20 illustrates the captured image with and without FPN calibration to provide the impact on the image quality. These figures are taken after averaging 100 images to remove the temporal noise. To compare its impact clearly, the images are enhanced by a factor of 8. As shown in the figures, the FPN in Figure 4.20(a) is removed, and the result is shown in Figure 4.20(b). In the meantime, the VFPN performance improved from 19LSB to 0.37LSB.

4.4. CONCLUSION

Temporal noise and FPN must be carefully managed to enhance frame rates while maintaining image quality. This work utilized analog CDS to reduce temporal noise and implemented offset calibration to address FPN, achieving a balance between speed and quality.

Section 4.2 discusses the temporal noise analysis and circuit design direction for reducing temporal noise. In the simplified noise model, temporal noise originates from the photodiode, source follower, PGA, ADC and quantization noise. Since the 3T-type pixel is used in this work due to the speed, the 3T-type pixel structure is modified to improve the temporal noise performance. In particular, the sampling network inside the

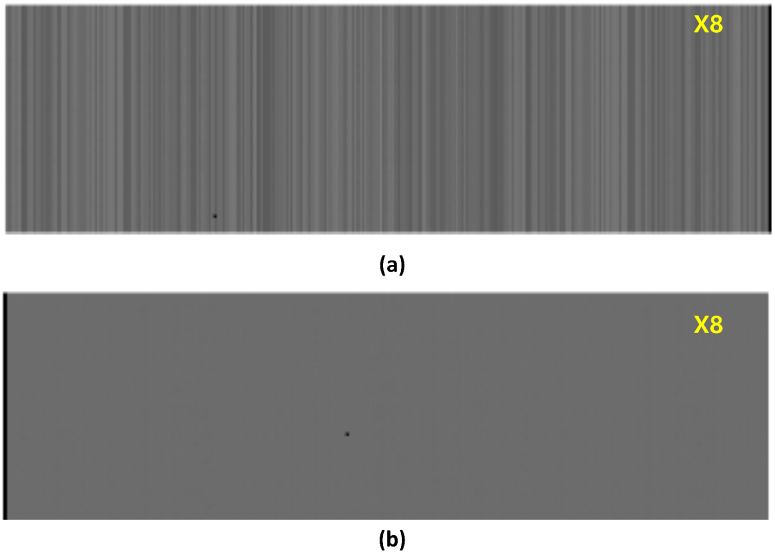


Figure 4.20: Captured image enhanced by a factor of 8: (a) without FPN calibration and (b) with FPN calibration

pixel architecture effectively suppresses the temporal noise from the 3T-type pixel. At the outside of the pixel, the ADC is the dominant factor contributing to the temporal noise, while the temporal noise from the PGA is divided by its loop gain. In addition, the CDS algorithm effectively removes the temporal noise from the low-frequency range. To optimize the temporal noise performance, the CDS interval must be shorter.

To compensate for the FPN, we first designed background offset calibration using a memory. This background offset calibration enables real-time offset compensation. However, as mentioned in section 4.3.3.1, the background offset calibration mainly has 3 issues. In particular, the background offset calibration requires additional time between the reset and signal level sampling times. The extra time limits the image sensor's frame rate enhancements and increases the CDS interval, degrading the temporal noise performance at the low-frequency range. In addition, the background offset calibration only removes the offset of the ADC, but the FPN originating from the pixel is not removed. As a result, the FPN calibration using the OB pixels has been implemented. As shown in 4.3.3.3, this calibration method has improved the FPN performance, and the measure FPN is an impressive 0.37LSB.

In summary, while enhancing the readout speed, crucial for improving frame rates, maintaining image quality requires careful temporal noise and FPN management through various calibration techniques.

References

[1] European Machine Vision Association, *EMVA Standard 1288: Standard for Characterization of Image Sensors and Cameras*, Online, Release 4.0. [Online]. Available: https://www.emva.org/wp-content/uploads/EMVA1288General_4.0Release.pdf [Accessed: 2025-05-01], Jun. 2021.

[2] J. Nakamura, *Image Sensors and Signal Processing for Digital Still Cameras*. CRC Press, 2005, pp. 67–77.

[3] R. Kansy, "Response of a correlated double sampling circuit to 1/f noise generated in ccd arrays," *IEEE Journal of Solid-State Circuits*, vol. 15, no. 3, pp. 373–375, Jun. 1980. DOI: 10.1109/JSSC.1980.1051404.

[4] H. Wey et al., "An improved correlated double sampling circuit for low noise charge coupled devices," *IEEE Transactions on Circuits and Systems*, vol. 37, no. 12, pp. 1559–1565, Dec. 1990. DOI: 10.1109/31.101279.

[5] T. Sugiki et al., "A 60 mw 10 b cmos image sensor with column-to-column fpn reduction," in *2000 IEEE ISSCC*, San Francisco, CA, USA, 2000, pp. 108–109. DOI: 10.1109/ISSCC.2000.839712.

[6] Y. Nitta et al., "High-speed digital double sampling with analog cds on column parallel adc architecture for low-noise active pixel sensor," in *2006 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2006, pp. 2024–2031. DOI: 10.1109/ISSCC.2006.1696261.

[7] M. Snoeij et al., "A cmos imager with column-level adc using dynamic column fixed-pattern noise reduction," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 3007–3015, Dec. 2006. DOI: 10.1109/JSSC.2006.884866.

[8] N. Teranishi, "Analysis of subthreshold current reset noise in image sensors," *Sensors*, vol. 16, no. 5, p. 663, May 2016. DOI: 10.3390/s16050663.

[9] J. Carnes et al., "Noise source in charge-coupled devices," *RCA Review*, vol. 33, pp. 327–343, 1972.

[10] D. Barbe, "Imaging devices using the charge-coupled concept," *IEEE Proceedings*, vol. 63, pp. 38–67, 1975.

[11] J. Lee, *Image used for noise analysis*, Personal collection, Ballyryan, Ireland, 2024.

[12] T. Watabe et al., "New signal readout method for ultrahigh-sensitivity cmos image sensor," *IEEE Transactions on Electron Devices*, vol. 50, no. 1, pp. 63–69, Jan. 2003. DOI: 10.1109/TED.2002.806472.

[13] X. Zhang et al., "14-bit fully differential sar adc with pga used in readout circuit of cmos image sensor," *Journal of Sensors*, vol. 2021, Article ID 6651642, 17, 2021. DOI: 10.1155/2021/6651642.

[14] S. Youn et al., "Design of low-noise cmos image sensor using a hybrid-correlated multiple sampling technique," *Sensors*, vol. 23, no. 23, p. 9551, 2023. DOI: 10.3390/s23239551.

[15] S. Lee et al., "Temporal noise suppression method using noise bandwidth limitation for pixel-level single-slope adc," in *2023 International Image Sensor Workshop (IISW)*, Crieff, Scotland, UK, 2023, p. 34.

[16] S. Hwang et al., "A 2.7-m pixels 64-mw cmos image sensor with multicolumn-parallel noise-shaping sar adcs," *IEEE Transactions on Electron Devices*, vol. 65, no. 3, pp. 1119–1126, 2018. DOI: 10.1109/TED.2018.2795005.

[17] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed. New York: McGraw-Hill, 2016.

[18] J. Cheon et al., "Noise analysis and simulation method for a single-slope adc with cds in a cmos image sensor," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 10, pp. 2980–2987, 2008. DOI: 10.1109/TCSI.2008.923434.

[19] X. Ge et al., "A 0.5e^- rms temporal noise cmos image sensor with gm-cell-based pixel and period-controlled variable conversion gain," *IEEE Transactions on Electron Devices*, vol. 64, no. 12, pp. 5019–5026, 2017. DOI: 10.1109/TED.2017.2759787.

5

Adaptive Reconfigurable Systems for Image Sensors: Adding Flexibility to Improve Speed

As highlighted in Chapter 1, machine vision applications demand high-frame-rate image sensors to optimize system efficiency. Significant advances have been made in improving image sensor frame rates, primarily by increasing readout speed or expanding the number of readout channels. However, these conventional methods often lead to side effects such as reduced pixel area, elevated thermal noise, and excessive power consumption. Moreover, the frame rate cannot be dramatically improved due to process technology limitations without significantly degrading image quality and overall system power efficiency.

This chapter presents a reconfigurable system to efficiently enhance frame rates while minimizing these drawbacks. It explores the motivation behind this approach, details the system's timing, and discusses the key advantages of employing a reconfigurable design to address the challenges associated with high-frame-rate image sensors.

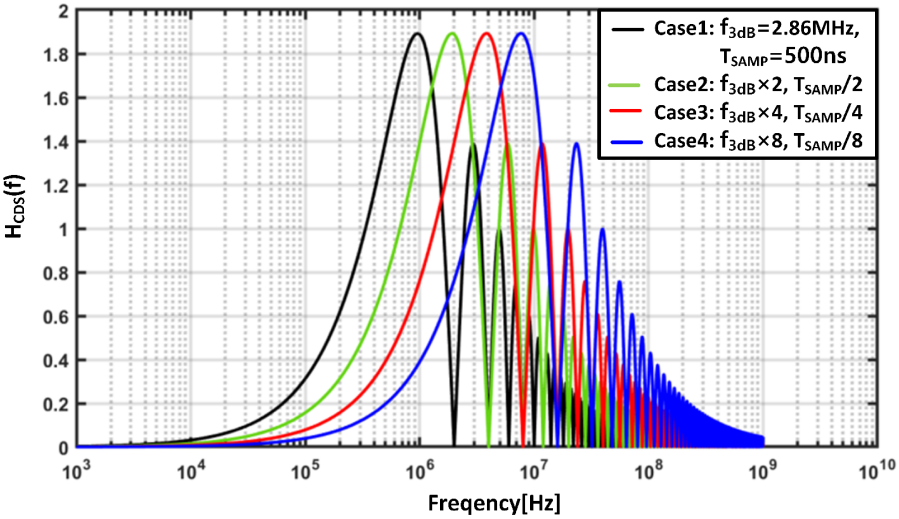


Figure 5.1: Frequency response of CDS transfer function by changing PGA bandwidth and sampling period

5.1. MOTIVATION OF THE RECONFIGURABLE SYSTEM

5.1.1. THE LIMITATIONS OF IMPROVING THE FRAME RATE

Much research has increased the pixel rate to improve the image sensor's frame rate. An increase in pixel rate requires increasing the pixel readout speed and the number of readout channels, as mentioned in section 3.1.1. However, this method is not always practical due to several technical issues.

First, enhancing pixel rate encounters physical limitations. As discussed in the previous chapter, integrating high-speed ADCs within the constrained area of an image sensor is challenging. For example, [1], [2] designed ADCs exceeding 10 MS/s, but each ADC is shared across 32 or 16 columns due to area constraints. While this approach supports high-speed operation, it does not substantially enhance the pixel rate, as the ADC must sequentially process multiple columns, creating a bottleneck that limits the effective per-pixel readout speed. As a result, despite the high ADC sampling rate, the overall frame rate gain is constrained. As pixel pitch shrinks to 0.56μm (Section 1.1), ADC design faces greater challenges due to denser interconnects, higher parasitic capacitance, and increased crosstalk, all of which degrade performance and efficiency.

Second, even if ADC sampling rate is improved, image quality still suffers due to large bandwidth. As the readout speed improved, the extended signal bandwidth made managing image quality difficult. As detailed in Chapter 4, temporal noise performance heavily depends on signal bandwidth. Increasing the readout speed broadens the signal bandwidth, heightening temporal noise levels and degrading image quality. Figure 5.1 shows the frequency response of the CDS transfer function, $H_{\mathrm{CDS}}(\mathrm{f})$. Since the area inside the CDS transfer function highly affects the temporal noise performance, comparing the area shows how the noise performance degrades. The examples are generated

by changing the signal bandwidth of the PGA and the ADC sampling period. For example, case 1 is the same specification designed in this work, and the PGA bandwidth, f_{3dB}, and the sampling period, T_{SAMP}, are 2.86MHz and 500ns. From case 2 to case 4, the bandwidth is doubled in each case, and the sampling period is divided by 2. As a result, the area inside the noise band is increasing. If the input signal of the ADC has PSD of 10-14 [V^2/Hz], the estimated temporal noises at the sampled signals are 42.35μV_{RMS}, 59.84μV_{RMS}, 84.47μV_{RMS} and 119.02μV_{RMS}, respectively.

Third, the data rate encounters the speed limitation. Typically, image sensors use high-speed serial interfaces such as LVDS, MIPI, or SLVS-EC to transmit pixel data. However, these interfaces also have bandwidth limitations. For example, the maximum data rate of LVDS is around 500Mb/s per channel in practical implementation. In the worst case, the image sensor must employ multiple LVDS channels to increase the data rate significantly, as implemented in [3], [4], [5], and the power consumption and complexity of routing signals across the chip also grow significantly. For example, if the image sensor operates at 1000fps with a 1M pixel array, the requested data rate should be more than 10Gb/s. Furthermore, transmitting data at such high speeds introduces additional power consumption due to the driving circuitry, leading to increased heat generation and inefficiency.

Therefore, while increasing the pixel rate has been a common approach, it faces critical technical limitations in ADC design, signal bandwidth management, and data transmission rates. A more efficient solution is required to achieve ultra-high-frame-rate image sensors without compromising image quality or energy efficiency.

5.1.2. THE EFFICIENCY OF THE IMAGE SENSOR OPERATION

Generally, an image sensor reads the entire pixel array to generate each image. This process is necessary when the sensor continuously captures different scenes by changing its angle or view. However, reading the entire pixel array becomes redundant and inefficient if the sensor observes a static scene where only the object's position within the frame changes.

Figure 5.2 illustrates an example of a machine vision application used in a factory, where the sensor monitors objects moving along a production line [6]. In [6], the background remains constant in every captured frame, and the only difference between each image should be the object's location and its condition. Consequently, continuously reading the entire pixel array wastes time and power, as most captured data remains unchanged

Figure 5.3 shows a scenario where the image sensor captures the same scene repeatedly as an object moves from point P_A to P_C via P_B. The area marked as A1 (gray) remains static and becomes irrelevant after the first frame, while area A2, which surrounds the moving object, becomes the region of interest (ROI). By focusing on the targeted readout of the ROI region, the sensor can avoid reading out the whole array, saving substantial time and energy. For example, consider an image sensor with a 1000×1000 pixel array. In conventional operation, the sensor reads out the entire array for every frame, and to achieve a frame rate of 1000 fps, the sensor would need to process each pixel within 1μs, resulting in a total of 1ms to read the entire array. However, if the ROI region is restricted to a 10×10 pixel area, the sensor only needs to read 100 pixels per frame. This dramat-

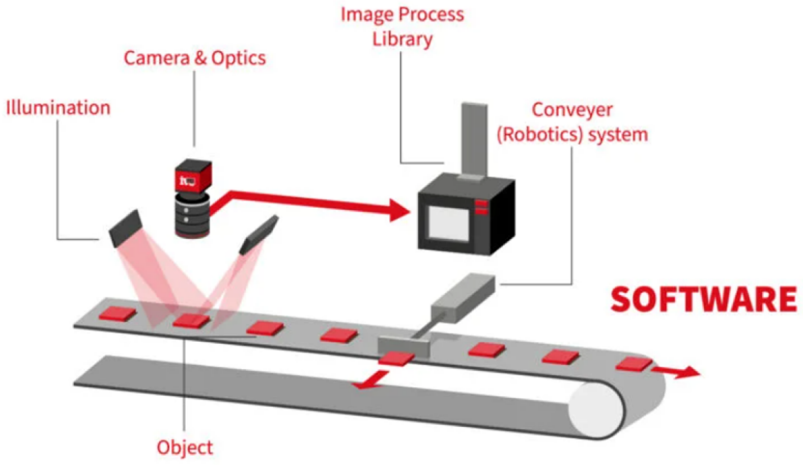


Figure 5.2: Machine vision example: monitoring objects on a production line

ically reduces the amount of data to be processed, allowing the sensor to achieve the same frame rate while spending far less time per pixel. This allocation allows more time for processing data from the ROI, lowering both workload and power consumption. In addition, since the amount of data to process is reduced, the required data rate is up to 1Mb/s instead of 10Gb/s. Figure 5.4 depicts the difference between both cases.

In conclusion, adopting an ROI-based readout approach allows the image sensor to focus on the most relevant areas of the scene, enhancing efficiency in terms of both speed and data processing. This method proves especially valuable in applications where the scene's background is static, and the object of interest is the primary focus, significantly reducing unnecessary data handling and power consumption.

5.1.3. PREVIOUS RESEARCH ON ROI-BASED IMAGE SENSOR

As discussed in section 5.1.2, designing image sensors for specific applications can significantly improve efficiency. Several studies have examined ROI-based image sensors tailored to particular tasks, revealing benefits in power savings and processing time [7], [8]. For instance, [8] implements a sun-tracking sensor with a simple algorithm to measure the angle between a satellite and the sun, achieving high energy efficiency by forgoing high image detail. In contrast, [7] employs an ROI-based approach to detect moving objects, reducing data processing requirements and extending available time per pixel, which improves image quality.

However, each study presents limitations. In [8], while low power consumption is achieved, the system faces difficulties in accurately detecting moving objects due to image data resolution after A/D conversion. Meanwhile, [7] encounters speed constraints with a single ADC structure using an off-chip 12-bit ADC. As frame rates increase, this

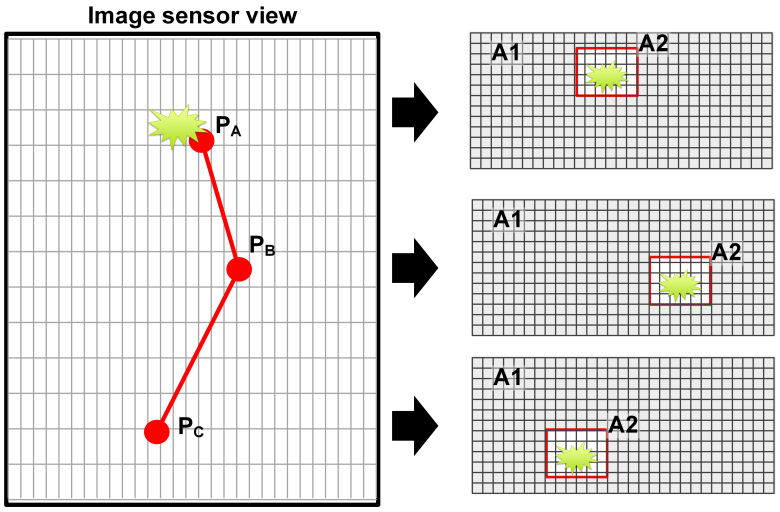


Figure 5.3: ROI-based readout approach for tracking moving objects in a fixed background

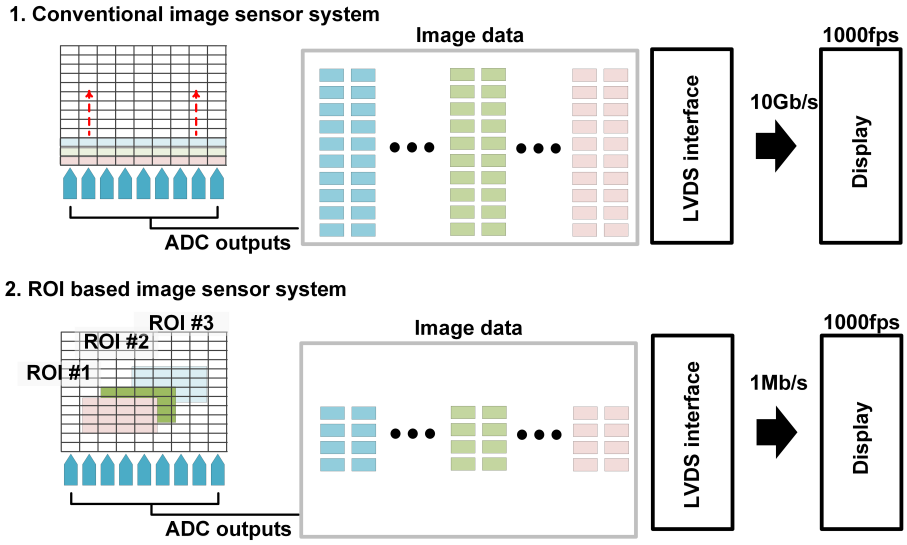


Figure 5.4: Comparison of data processing requirements for full-frame vs. ROI readout

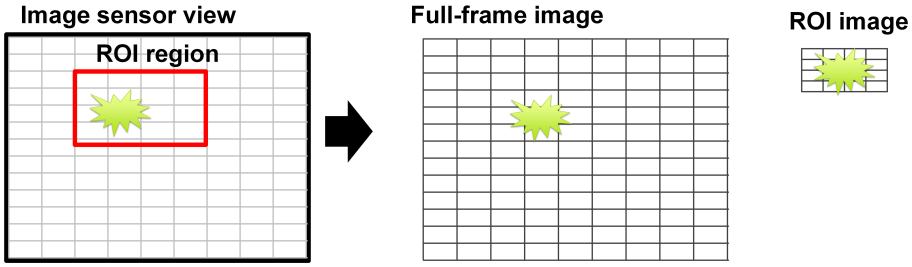


Figure 5.5: Full-frame and ROI mode Images for reconfigurable system

system requires improved ADC readout speed.

These studies underscore the potential for advancing application-specific sensor designs. Given the limitations of conventional methods for increasing frame rate, application-dedicated designs open pathways to enhanced performance. This work, therefore, proposes a reconfigurable system optimized to detect and track high-brightness, fast-moving objects at extremely high frame rates within a fixed viewpoint and angle.

To optimize the reconfigurable system, this design includes a switch network to facilitate seamless mode switching and efficiently route pixel data to the relevant ADCs. The column-parallel structure allows the switch network to read pixels within the ROI and process these outputs simultaneously. This system achieves an exceptionally high effective frame rate since the pixel data from the ROI region is processed within a single horizontal line time. The design and benefits of this approach are discussed further in sections 5.2 and 5.3.

5.2. THE RECONFIGURABLE IMAGE SENSOR

5.2.1. THE IMAGES PRODUCED BY THE RECONFIGURABLE SYSTEM AND TIMING

In this work, the image sensor is used under conditions where it continuously monitors a specific scene from a fixed angle, tracking a moving object emitting strong light. The object moves within the camera's field of view, and this predictable environment allows the sensor to operate in a reconfigurable system with two distinct modes: normal mode and zoom-in mode. The system switches between these modes to optimize speed and efficiency based on the size of the region being imaged. Figure 5.5 illustrates the images produced by these two modes.

In normal mode, the image sensor captures a full-frame image by reading out the entire pixel array, as shown in Figure 5.5(a). This full-frame image contains the background and the moving object, providing comprehensive scene information. A real-time image processing algorithm analyzes the image to detect the object's location. The image analysis procedure extracts the object's vertical and horizontal coordinates.

In zoom-in mode, only the pixel array within the ROI is read out, which focuses on tracking the object more efficiently, as illustrated in Figure 5.5(b). As mentioned above, this ROI region is set using the coordination extracted from the full-frame image in normal mode. Since fewer pixels are processed in zoom-in mode, the frame rate is signif-

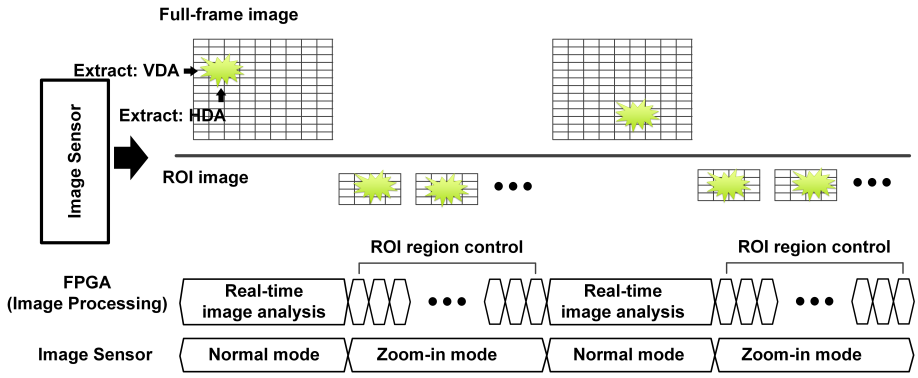


Figure 5.6: Timing diagram for switching between Full-frame and ROI modes

icantly increased, allowing the sensor to monitor the object's real-time movement with much faster updates. The zoom-in mode continues until the system recalibrates the object's position based on new full-frame data.

Figure 5.6 explains the timing between these two modes. The system usually begins by capturing a full-frame image to identify the object's location. Real-time image analysis occurs as the pixel data is being read out, and the coordinates of the object are calculated in the FPGA. These coordinates are then fed back to the sensor to set the ROI for zoom-in mode. Based on the object's movement speed, the system adjusts the number of frames generated in zoom-in mode. This adjustment further increases the effective frame rate. When the object's location requires recalibration, the sensor switches back to normal mode to update the ROI.

By alternating between these two modes, the reconfigurable system efficiently tracks the object while balancing power consumption and frame rate. This approach provides high-speed object tracking without continuously processing the entire pixel array, significantly reducing unnecessary data handling.

5.2.2. RECONFIGURABLE SYSTEM BLOCK DIAGRAM OVERVIEW

To support the 2 different image sensor operations mentioned in section 5.2.1, the reconfigurable system comprises 2 primary parts: the image sensor and the image processing unit. Figure 5.7 illustrates the system block diagram designed in this work.

The image sensor in Figure 5.7 has a similar architecture, explained in section 2.1.1. The image sensor has a 316×110 pixel array with a 10μm pixel pitch arranged in a column-parallel structure. Each column of the pixel array is connected to one of the 316 PGAs and the ADCs. The PGA supports analog gain up to 8, and the ADC performs data conversion using the 10.5-bit SAR ADC, as explained in 3.3.3. The digital data from the ADCs are transmitted to the image processing unit via a 12-channel LVDS interface, supporting a maximum data rate of 1.44Gb/s. Two additional components were designed specifically for the reconfigurable system: an intelligent switch box and a horizontal address decoder. The intelligent switch box distributes the pixel outputs to the appropriate ADCs based on whether the sensor operates in normal or zoom-in mode. Since the intelligent

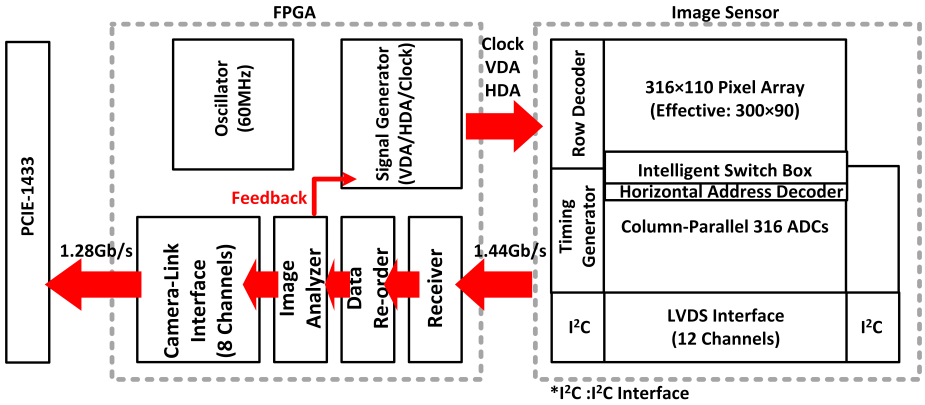


Figure 5.7: System block diagram of the reconfigurable image sensor design

5

switch box is the switch network, the horizontal address decoder controls the intelligent switch box based on the feedback from the image processing unit during the zoom-in mode.

The image processing unit manages the sensor control and processes the captured images. The image processing unit receives data from the sensor through the receiver block, which also applies FPN compensation using the method explained in section 4.3.3. The data are then reorganized in the data re-order block to reconstruct the image, which is passed to the image analyzer. This block identifies the moving object's location and coordinates. The signal generator creates feedback signals based on the object's location and sends them back to the sensor to configure the ROI region for zoom-in mode. In addition, the signal generator also generates basic sensor control signals, such as VDA (Vertical Domain Address). The camera interface transmits the processed images to the display using an 8-channel camera-link interface, capable of supporting data rates up to 1 Gb/s. The camera link protocol is used in communication.

As mentioned above, the reconfigurable system controls the image sensor and the image analyzer designed inside the FPGA. Therefore, communication between the FPGA and the image sensor is essential.

5.2.3. THE PIXEL READOUT TIMING AND PIXEL OUTPUT DISTRIBUTION AT NORMAL MODE AND ZOOM-IN MODE

Controlling the intelligent switch box in the reconfigurable system is essential, as it distributes pixel outputs from the pixel array to the appropriate ADCs depending on the image sensor's operating mode.

In normal mode, the image sensor reads the entire pixel array like a general image sensor. Since the sensor uses a column-parallel architecture, the ADC in each column reads pixel outputs from the same column. Figure 5.8 illustrates the intelligent switch box control during normal mode. As shown in Figure 5.8(a), one of the switches, S_{M1}, in each column is activated to connect the pixel output to the corresponding ADC in the

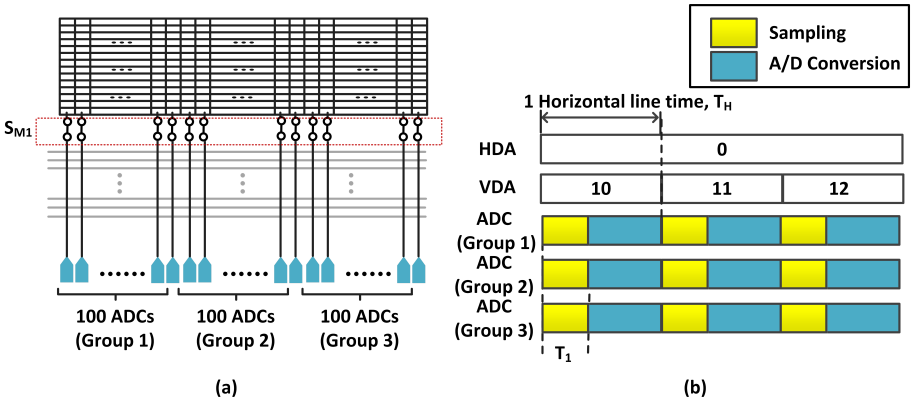


Figure 5.8: Intelligent switch box control in normal mode and (b) ADC timing

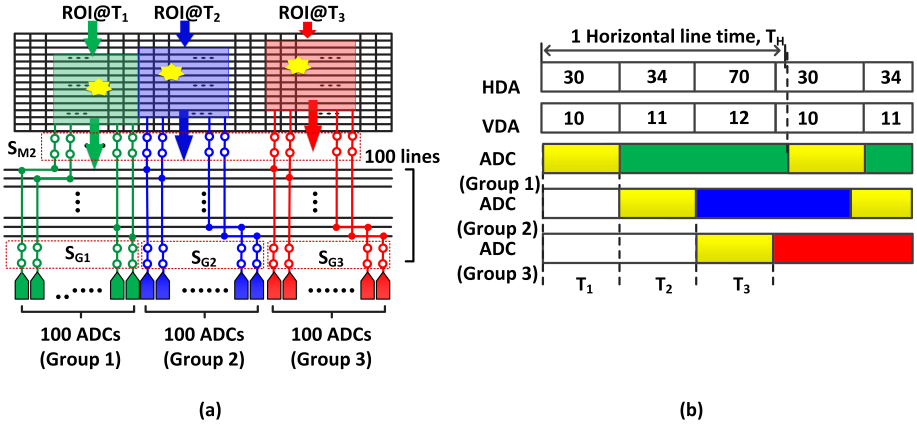


Figure 5.9: (a) Intelligent switch box control in zoom-in mode and ADC timing

same column, enabling sequential readout of the pixel array. The ADC control timing diagram in Figure 5.8(b) shows that all ADCs perform sampling simultaneously during the designated sampling period (T_1), followed by data conversion, ensuring synchronized readout and preventing timing mismatches that could degrade image uniformity. Additionally, the VDA is transmitted to select the corresponding row in the pixel array, while the HDA remains deactivated (set to 0).

In zoom-in mode, the intelligent switch box dynamically distributes the pixel outputs from the ROI region to the available ADCs. The image sensor generates the images from the ROI region within a single horizontal line time. Figure 5.9 shows the intelligent switch box's switch network control and timing. The image sensor turns on ten S_{M2} switches in the column within the ROI region, as depicted in Figure 5.9(a). Since the 10×10 ROI region outputs 100-pixel output signals, the switch network has 100 horizontal lines. These 100 horizontal lines are connected to the ADCs through the switch

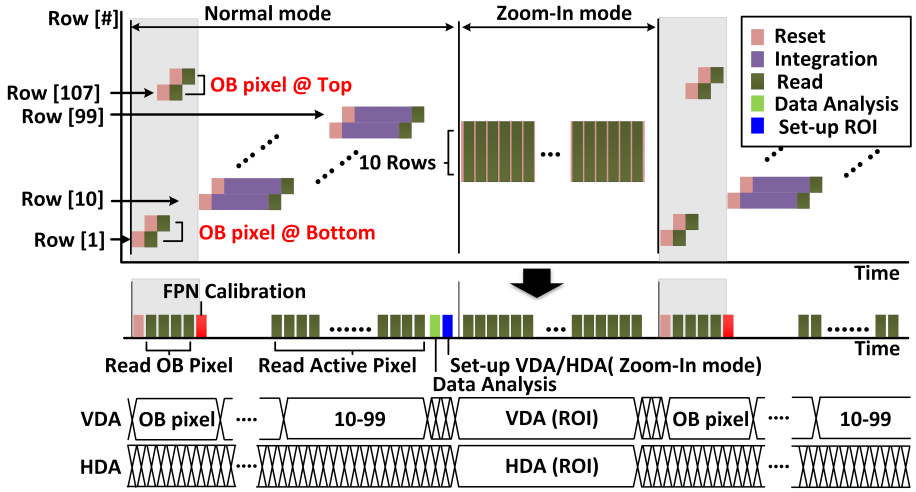


Figure 5.10: Timing diagram for seamless mode switching and ROI control

S_{G1}, S_{G2} and S_{G3}. For example, when the ROI region is set in the green region shown in Figure 5.9(a), the image sensor turns on 100 S_{G1} switches, connecting 100 horizontal lines with the input of the 100 ADCs. The first 100 ADCs sample the pixel output signals from the green area, described in the timing of Figure 5.9(b). Sequentially, in periods T_2 and T_3, 100 S_{G2} and S_{G3} switches allow the next 100 ADCs to sample pixel output signals in blue and red ROI regions following the timing in Figure 5.9(b). Additionally, the VDA and HDA correspond to the position of the ROI region extracted from full-frame image analysis, ensuring adaptive readout based on the identified region of interest.

Moreover, in zoom-in mode, pixel's 3 operations, such as reset, charge integration and read, must be completed within the sampling period. Though the charge integration time is relatively short, this operation enables the sensor to read the ROI region within a single horizontal line time. For this reason, to maximize the charge integration time, the ADC sampling time is about 1μs when the ADC is working at 250kS/s in this work. In addition, the image sensor tracks the moving object emitting intense light in this work, and a short charge integration time is not a problem. Furthermore, the ROI region can be set anywhere since the pixel operation is completed within the sampling period. This flexible ROI region control allows the ROI region to overlap during zoom-in mode.

5.2.4. RECONFIGURABLE SYSTEM CONTROL TIMING

The reconfigurable system operates based on the control timing shown in Figure 5.10, enabling a seamless switch between normal and zoom-in modes for efficient object tracking.

The image sensor initially begins in normal mode. During this mode, the HDA signal is not sent, and the row decoder follows the VDA to control the pixel readout as per the timing in Figure 5.10. To correct for FPN, the sensor first reads the OB pixels at the array's top and bottom. Only two lines of OB pixels out of 4 are read due to potential light

penetration issues affecting the edge pixels. To mitigate this, the integration time for the OB pixels is kept at a minimum, as illustrated in Figure 5.10.

Once the OB pixels are read, the sensor transitions to read the active pixel array. Simultaneously, the image analyzer in the processing unit performs real-time analysis to detect the object's location. When the active pixels are fully read, the object's location is determined, and the signal generator prepares the required VDA and HDA signals (refer to Figure 5.7) for controlling the Region of Interest (ROI) during zoom-in mode.

In zoom-in mode, the image sensor uses VDA and HDA signals to focus on the ROI. Since the 10×10 pixel array of the ROI is processed within a single horizontal line time, 100 ADCs are employed to generate an image. As described in the previous section, the system can generate multiple images during zoom-in mode based on the object's movement speed, allowing for the generation of 3N images within N horizontal line times. This dynamic adjustment enhances the system's frame rate without affecting image quality.

After the zoom-in mode, the system returns to normal mode to recalibrate the object's position. As before, OB pixels are reread to compensate for any FPN, ensuring consistent image quality throughout the operation.

5.3. THE IMPROVEMENT OF THE RECONFIGURABLE SYSTEM

5.3.1. FRAME RATE IMPROVEMENT AND LIMITATION

As introduced in section 3.1.1, the frame rate, F_{FR}, of an image sensor can be described by the following equation:

$$F_{FR} \leq \frac{F_{ADC} \cdot N_{ADC}}{P_{ROW} \cdot P_{COL}} \approx \frac{F_{PIXEL}}{P_{ROW} \cdot P_{COL}} \tag{5.1}$$

F_{FR} represents the frame rate, F_{ADC} represents the ADC sampling rate, N_{ADC} represents the number of ADCs, and P_{ROW} and P_{COL} represent the number of rows and columns in the pixel array, respectively. In addition, F_{PIXEL} stands for the pixel rate of the image sensor. In this work, the ADC sampling rate is 250kS/s, and the number of ADCs is 300. Given that the active pixel array resolution is 300×90, the maximum achievable frame rate in normal mode would be approximately 2,777fps.

However, in the reconfigurable system, the zoom-in mode allows further improvements in the effective frame rate. After reading the full frame, the image sensor updates the region of interest (ROI), dynamically tracking the object's location. Updating the ROI image has the same effect as generating a new full-frame image. As a result, if we assume that 3N images are generated during the N horizontal line time in zoom-in mode after generating 1 full frame image at normal mode, the effective frame rate, F_{FR_EFF}, is calculated as follows.

$$F_{FR\_EFF} \leq \frac{1+3N}{\frac{P_{ROW}}{F_{ADC}} + \frac{N}{F_{ADC}}} \tag{5.2}$$

In this formula, the numerator is the number of images taken during normal and zoom-in modes. The denominator is the time taking images during normal mode and zoom-in mode. Since the 3 ROI regions can be captured within a single horizontal line

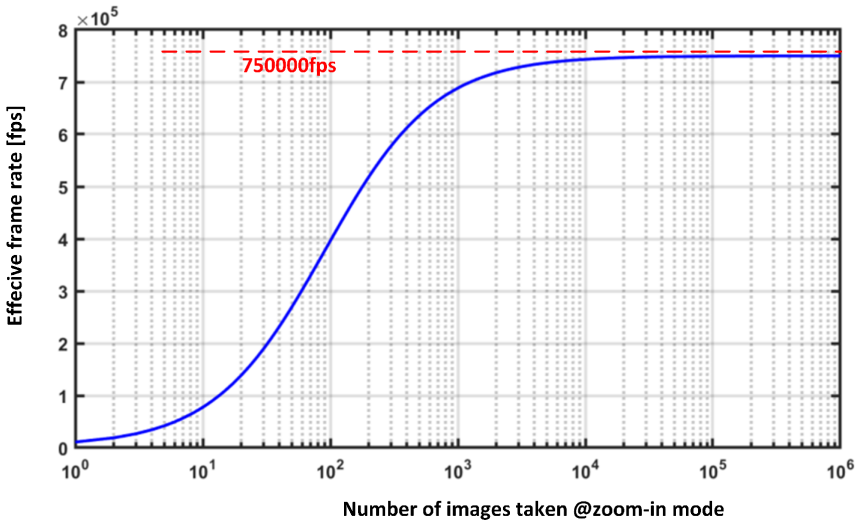


Figure 5.11: Achievable effective frame rate by changing the number of images captured in zoom-in mode

time in zoom-in mode, the number of images captured during N horizontal line time is set to 3N.

Figure 5.11 illustrates the effective frame rate, F_{FR_EFF}, by changing the number of images taken at zoom-in mode from 3 to 3,000,000. As described in Figure 5.11, the effective frame rate is saturated at around 750,000fps as the number of zoom-in mode images increases. If 30 images are captured in zoom-in mode, the effective frame rate, F_{FR_EFF}, would be 77,500fps.

However, there is a practical limitation to how much the variable N (the number of images captured in zoom-in mode) can be increased. The zoom-in mode captures only the pixels within the ROI, which may not be large enough to determine the object's movement. For this reason, if the system remains in zoom-in mode for too long, it risks losing the object's position within the scene. For instance, the ROI can effectively track the object in cases of minimal movement. Still, if the object temporarily moves out of the ROI, the system may lose its position.

In summary, the reconfigurable system significantly improves the effective frame rate, which can be dynamically adjusted based on the number of images captured during zoom-in mode. Although the frame rate in normal mode is not extremely high, the reconfigurable system allows for improved tracking of moving objects through an enhanced effective frame rate.

5.3.2. IMAGE QUALITY PRESERVATION THROUGH FIXED ADC SAMPLING RATE

The reconfigurable system design maintains a consistent ADC sampling rate across both normal and zoom-in modes, as shown in section 5.3.1. In the reconfigurable system, the effective frame rate is enhanced by increasing the number of images captured

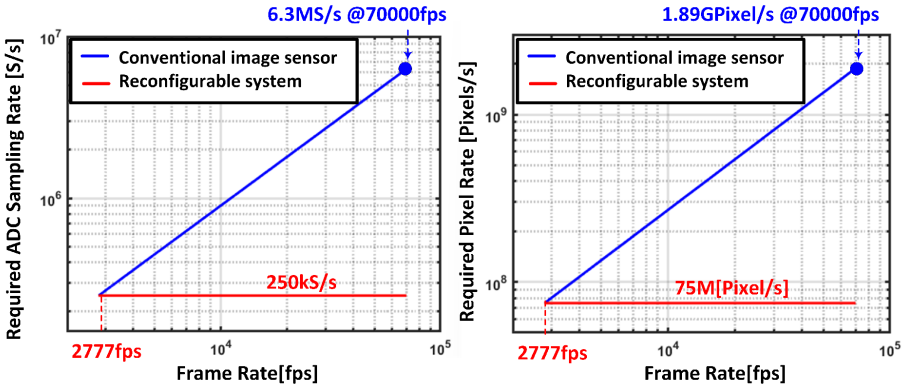


Figure 5.12: Required ADC sampling rate and pixel rate in conventional image sensor and reconfigurable system

during zoom-in mode while maintaining a constant ADC sampling rate.

Figure 5.12 illustrates the relationship between the required ADC sampling rate and pixel rate as a function of frame rate. The blue line represents a conventional image sensor, where the ADC sampling rate and pixel rate increase proportionally with the frame rate. The red line represents the reconfigurable system, showing how it maintains a constant ADC sampling rate of 250kS/s and a fixed pixel rate, even as the frame rate increases. As derived in section 5.3.1, the required ADC sampling rate, F_{ADC}, and pixel rate, F_{PIXEL}, are calculated as follows.

$$F_{\mathrm{ADC}} = \frac{P_{\mathrm{ROW}} \cdot P_{\mathrm{COL}} \cdot F_{\mathrm{FR}}}{N_{\mathrm{ADC}}} \tag{5.3}$$

$$F_{\mathrm{PIXEL}} = P_{\mathrm{ROW}} \cdot P_{\mathrm{COL}} \cdot F_{\mathrm{FR}} \tag{5.4}$$

In these equations, F_{FR} represents the frame rate, N_{ADC} is the number of ADCs, and P_{ROW} and P_{COL} are pixel array dimensions. For example, with a pixel array resolution of 300×90 and no zoom-in mode images captured (N=0), the frame rate is 2,777fps, corresponding to an ADC sampling rate of 250kS/s for both the conventional and reconfigurable systems. However, as the frame rate increases in a conventional sensor, the required ADC sampling rate scales proportionally, leading to higher pixel rates. In contrast, the reconfigurable system increases the frame rate by capturing multiple images in zoom-in mode while the ADC sampling rate and pixel rate remain fixed.

Maintaining a smaller signal bandwidth is crucial for preserving image quality. Increasing the frame rate in conventional systems leads to higher ADC sampling rates and signal bandwidth, which, as discussed in section 4.2, result in degraded temporal noise performance. However, the reconfigurable system keeps the signal bandwidth low and prevents introducing more high-frequency noise even when the frame rate is increased.

The increased bandwidth primarily contributes to temporal noise. As shown in Figure 5.1, increasing the sampling rate reduces low-frequency noise due to the shorter CDS interval. However, a larger bandwidth introduces more high-frequency noise, leading to

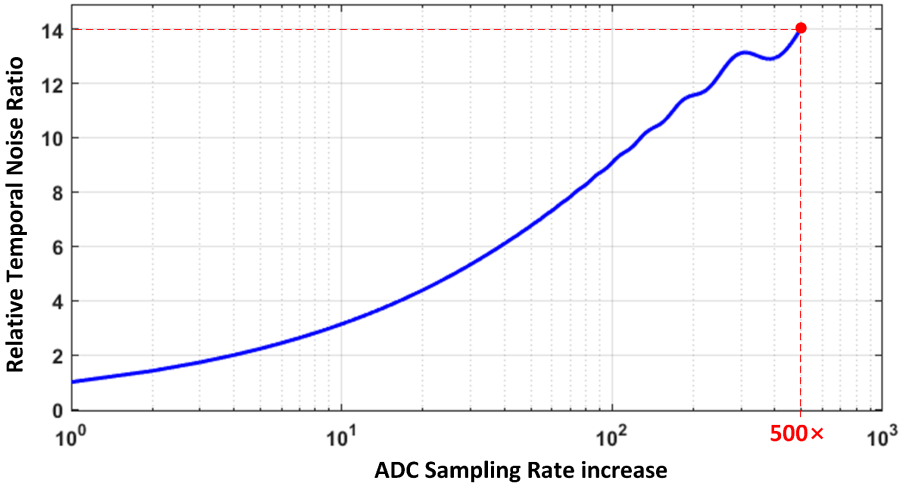


Figure 5.13: Temporal noise performance comparison by increasing the ADC sampling rate

an overall increase in temporal noise. Figure 5.13 illustrates the rise in temporal noise associated with higher ADC sampling rates. In this figure, the x-axis represents the relative difference in ADC sampling rate, normalized by the sampling rate at F_{FR} = 2,777fps, while the y-axis shows the ratio of estimated temporal noise to the original noise at F_{FR} = 2,777fps. The ADC sampling rate is increased up to 500×. Temporal noise is estimated by applying the same power spectral density (PSD) to the CDS transfer function, and the resulting noise is normalized to its original value at F_{FR} = 2,777fps. As shown in Figure 5.13, temporal noise increases as the ADC sampling rate rises. Specifically, when the ADC sampling rate is increased by 500, the estimated temporal noise increases approximately 14 times compared to its original value.

Therefore, the reconfigurable system is advantageous because it maintains the temporal noise as the frame rate increases. If the image sensor is required to operate at an extremely high frame rate, the efficiency of the reconfigurable system increases.

5.3.3. POWER CONSUMPTION REDUCTION

In conventional image sensors, increasing the frame rate generally requires a corresponding increase in the ADC sampling rate and interface output speed. However, the reconfigurable system eliminates the need for these increases, resulting in significant power savings.

In conventional systems, as the frame rate increases, the pixel rate must also rise proportionally to ensure that the sensor can process and transmit all pixel data in time. This requires a high-speed output interface to handle the increased data rate. For instance, with a pixel rate of 27Mpixel/s for 1,000fps at 300×90 active pixels, the output data rate must be at least 270Mb/s, assuming the interface data rate is approximately 10 times faster than the pixel rate. Therefore, for higher frame rates, the required data rate

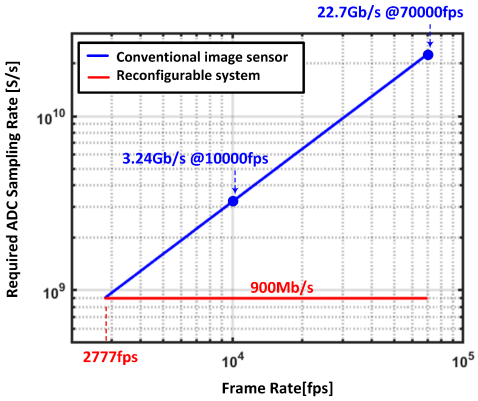


Figure 5.14: Required data rate at the output interface as frame rate increases in conventional image sensor and reconfigurable system

escalates.

Figure 5.14 illustrates this relationship. At a frame rate of 2,777fps, the required data rate in a conventional system is around 900Mb/s due to 12-bit of the ADC output format defined in section 3.3.3. If the frame rate increases to 10,000fps, the required output data rate rises to 3.24Gb/s. In this scenario, at least 27 LVDS channels would be needed to maintain the data rate regarding the single-channel LVDS interface, which supports around 120Mb/s. Since the design in this work employs 12 LVDS channels, an additional 15 channels would be required to handle the increased load. Given that each LVDS channel draws 3mA of current, the power consumption would increase by approximately 150mW.

In contrast, the reconfigurable system avoids these complications. Since the system can enhance the effective frame rate by capturing multiple images in zoom-in mode without increasing the ADC sampling rate, the output interface does not require any speed improvements. For instance, even at an effective frame rate of 10,000fps, the interface speed remains stable at 900Mb/s, with no additional LVDS channels required. Instead, an effective frame rate of 10,000fps can be easily realized by setting the number of images taken at zoom-in mode as 3.

Additionally, the power reduction in the ADC is significant. In conventional systems, the ADC power consumption increases proportionally with the sampling rate. Thus, if the frame rate increases tenfold, the ADC power consumption must also rise accordingly. However, in the reconfigurable system, because the ADC sampling rate remains unchanged, the system can achieve the same frame rate increase while saving up to 90% of the ADC power consumption.

In summary, the reconfigurable system offers multiple advantages regarding power efficiency. The interface data rate remains unchanged, reducing the need for additional LVDS channels and minimizing power consumption. Moreover, the consistent ADC sampling rate allows for substantial power savings, making the system significantly more energy-efficient than conventional high-frame-rate image sensors.

5.4. CONCLUSION

This chapter introduced a reconfigurable image sensor system designed to enhance frame rates efficiently without complex hardware modifications. Traditionally, improving frame rates required increasing the pixel rate, which leads to higher power consumption and more demanding hardware requirements. To overcome these limitations, application-specific designs are necessary.

This work implements the reconfigurable system, assuming the image sensor tracks a strongly illuminated moving object within a fixed scene. This setup allows the sensor to switch dynamically between two operational modes: normal mode and zoom-in mode. The essential advantage of this system is that it significantly improves the effective frame rate by capturing multiple images in zoom-in mode, all without increasing the ADC sampling rate. The number of images captured during zoom-in mode is crucial to this enhancement.

The reconfigurable system offers several benefits, including speed enhancement without the need for ADC improvements, preservation of image quality due to maintaining a small signal bandwidth, and substantial power savings. The system effectively mitigates the typical challenges associated with high-frame-rate image sensors by leveraging these advantages.

In summary, this reconfigurable system provides a flexible and efficient solution for boosting frame rates while minimizing power consumption and hardware complexity, making it ideal for real-time tracking applications.

REFERENCES

[1] T. Haruta et al., "4.6 a 1/2.3inch 20mpixel 3-layer stacked cmos image sensor with dram," in *2017 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2017, pp. 76–77. DOI: 10.1109/ISSCC.2017.7870268.

[2] T. Yasue et al., "A 33mpixel cmos imager with multi-functional 3-stage pipeline adc for 480fps high-speed mode and 120fps low-noise mode," in *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2018, pp. 90–92. DOI: 10.1109/ISSCC.2018.8310198.

[3] M. Sakakibara et al., "A back-illuminated global-shutter cmos image sensor with pixel-parallel 14b subthreshold adc," in *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2018, pp. 80–82. DOI: 10.1109/ISSCC.2018.8310193.

[4] S. Lim et al., "A 240-frames/s 2.1-mpixel cmos image sensor with column-shared cyclic adcs," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2073–2083, Sep. 2011. DOI: 10.1109/JSSC.2011.2144010.

[5] R. Funatsu et al., "6.2 133mpixel 60fps cmos image sensor with 32-column shared high-speed column-parallel sar adcs," in *2015 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2015, pp. 1–3. DOI: 10.1109/ISSCC.2015.7062951.

[6] J. Cheon et al., "Noise analysis and simulation method for a single-slope adc with cds in a cmos image sensor," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 10, pp. 2980–2987, Nov. 2008. DOI: 10.1109/TCSI.2008.923434.

[7] T. Yasue et al., "A 1.7-in, 33-mpixel, 120-frames/s cmos image sensor with depletion-mode mos capacitor-based 14-b two-stage cyclic a/d converters," *IEEE Transactions on Electron Devices*, vol. 63, no. 1, pp. 153–161, Jan. 2016. DOI: 10.1109/TED.2015.2451700.

[8] S. Hwang et al., "A 2.7-m pixels 64-mw cmos image sensor with multicolumn-parallel noise-shaping sar adcs," *IEEE Transactions on Electron Devices*, vol. 65, no. 3, pp. 1119–1126, Mar. 2018. DOI: 10.1109/TED.2018.2795005.

6

Adaptive Reconfigurable Systems for Image Sensors: Practical Design and Implementation

As discussed in Chapter 5, the reconfigurable system holds significant potential to efficiently enhance frame rates. Mode switching between normal and zoom-in modes using the ROI region enhances system efficiency. The system improves frame rates, reduces data processing needs, and lowers power consumption. Additionally, the image sensor maintains its sampling rate and signal bandwidth, preserving image quality. Implementing this system requires additional circuit blocks, efficient data distribution, and feedback mechanisms for precise ROI positioning based on image analysis, all synchronized with precise timing.

This chapter presents the hardware design, digital signal processing algorithms for data distribution and image analysis, and feedback mechanisms necessary for accurate ROI placement and tracking.

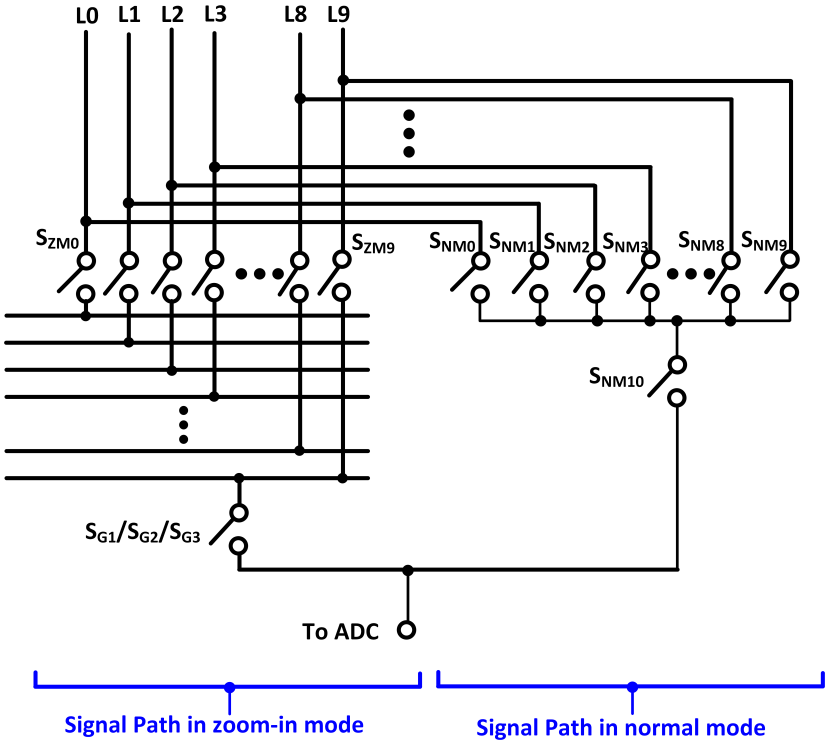


Figure 6.1: Layout of the intelligent switch network for column data routing

6.1. DATA DISTRIBUTION NETWORK CONTROL FOR RECONFIGURABLE SYSTEMS

The reconfigurable system relies on a robust and adaptive data distribution network to efficiently operate across normal and zoom-in modes. This network, encompassing the intelligent switch network, pixel array, and ADCs, ensures seamless data flow along the readout path. By dynamically managing data based on the current operational mode, the network enables the system to track moving objects while accurately maintaining efficiency. Crucially, this approach eliminates the need for an increase in AFE readout speed, thereby preserving power efficiency and system stability.

6.1.1. DATA DISTRIBUTION WITH INTELLIGENT SWITCH NETWORK

Figure 6.1 illustrates the design of the switch network connection within a column. Each column includes 10-pixel output lines, which are essential to support the 10×10 ROI readout in zoom-in mode. Since the ROI region spans 10 rows and 10 columns, each column must provide 10 parallel pixel outputs to enable simultaneous access to all pixels in the ROI. These output lines are also utilized in normal mode for line-by-line readout. The switch network dynamically controls which of these lines are active de-

pending on the operational mode, allowing flexible data routing without modifying the ADC structure. The switch network has a consistent design across all columns containing 22 switches. These switches include 10 switches for normal mode (S_{NM0} to S_{NM9}), an additional normal mode-specific switch (S_{NM10}), and 10 switches for zoom-in mode (S_{ZM0} to S_{ZM9}). Zoom-in mode is further supported by switches S_{G1}, S_{G2}, and S_{G3}, which route pixel data from 100 horizontal lines to the ADCs. These horizontal lines connect the pixel output lines from 10 adjacent columns, ensuring efficient data aggregation and distribution during zoom-in mode.

In normal mode, the pixel outputs are routed directly to the ADCs in the same column, allowing for a straightforward line-by-line readout of the entire pixel array. The pixel array outputs only one pixel at a time per column during each horizontal line period through the corresponding output line selected based on the pixel location. To support this operation, only one of the 10 switches (S_{NM0} to S_{NM9}), along with the dedicated switch S_{NM10}, is activated per column. Figures 6.2(a) and (b) show examples of switch network controls, while Figure 6.2(c) illustrates the associated timing in normal mode. For instance, as depicted in Figure 6.2(a), if the pixel output is transmitted through output line 0, L0, in period T_1, switches S_{NM0} and S_{NM10} are activated. In period T_2, the pixel output shifts to output line 1, L1, activating switches S_{NM4} and S_{NM10}. Turning on appropriate switches depending on the pixel location ensures the pixel output is connected directly to the corresponding ADC.

In zoom-in mode, the system uses the horizontal address decoder to activate specific switches within the selected column, dynamically routing pixel data from the defined ROI region to the corresponding ADCs. The ROI region is set based on the addresses transmitted to the image sensor. For instance, if the vertical domain address (VDA) is set to N, the ROI spans rows N to N+9, while the horizontal domain address (HDA) of M defines the columns M to M+9. This configuration leverages the 10 output lines from the pixel array, with all 10 S_{ZM} switches in the selected column activated simultaneously to route the data.

The horizontal lines aggregate pixel data from adjacent columns and distribute it to the ADCs. Depending on the timing, switches S_{G1}, S_{G2}, and S_{G3} are sequentially activated to route the data to the ADCs. Figures 6.3(a), (b), and (c) demonstrate the switch control, while Figure 6.3(d) illustrates the timing. At the start of zoom-in mode, S_{G1} switches transmit pixel data from the first ROI region to the first 100 ADCs. These 100 S_{G1} switches remain active during the ADC sampling period. Once the sampling is complete, S_{G2} switches route data from the next ROI region to the next 100 ADCs, as shown in Figure 6.3(b). Similarly, S_{G3} switches to manage the third batch of ROI pixel data, as depicted in Figure 6.3(c). After the third ADC sampling period ends, the first 100 ADCs finalize A/D conversion and are ready to sample the next pixel data set. This continuous operation ensures efficient processing of ROI data, as depicted in Figure 6.3(d), without interrupting the ADC's normal specifications.

The intelligent switch network seamlessly switches between normal and zoom-in modes, enabling efficient data distribution without requiring hardware modifications to the ADCs. This design allows precise pixel data handling and significantly improves the effective frame rate, as analyzed in Chapter 5.

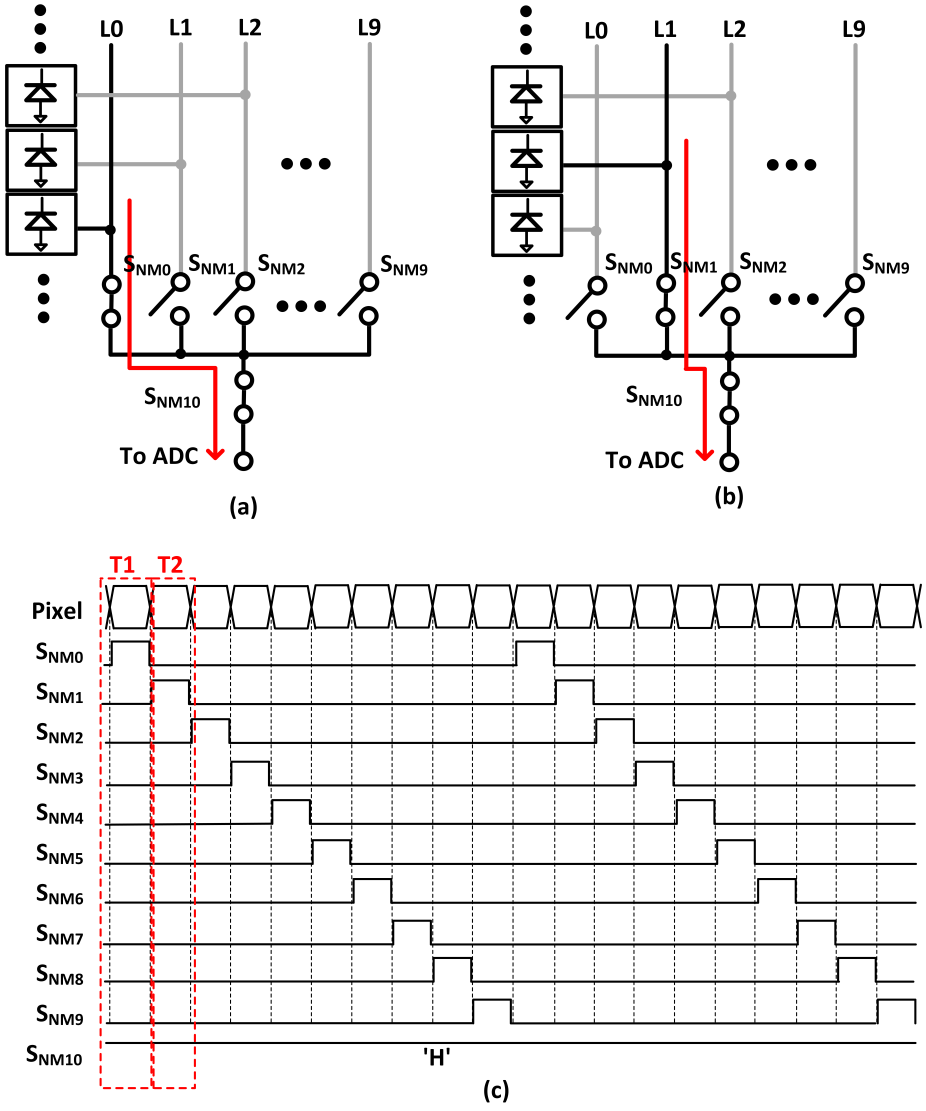


Figure 6.2: Switch network control example for (a) pixel output line L0 and (b) pixel output line L0 in normal mode and (c) timing diagram for switch activation in normal mode

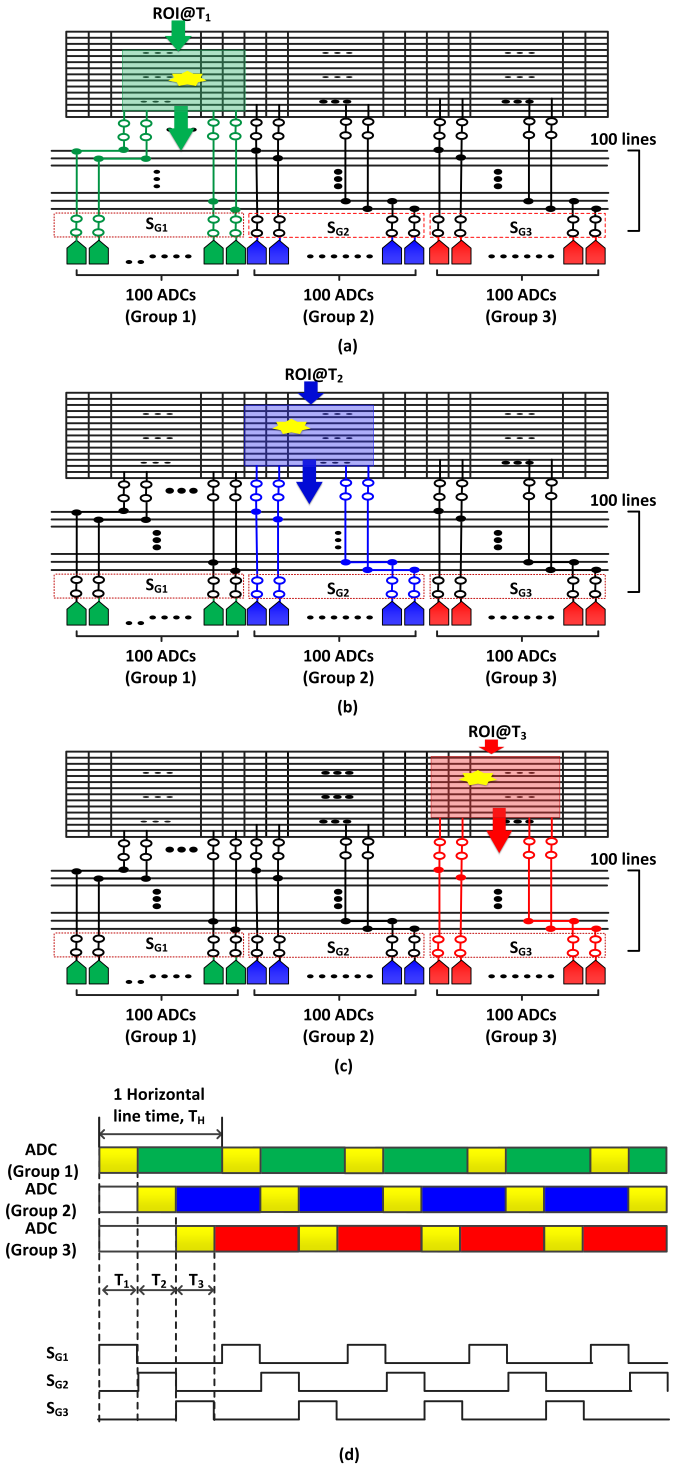


Figure 6.3: Switch control to connect the pixel output to the ADC in zoom-in mode using (a) SG1 switches, (b) SG2 switches and (c) SG3 switches and (c) associated timing diagram

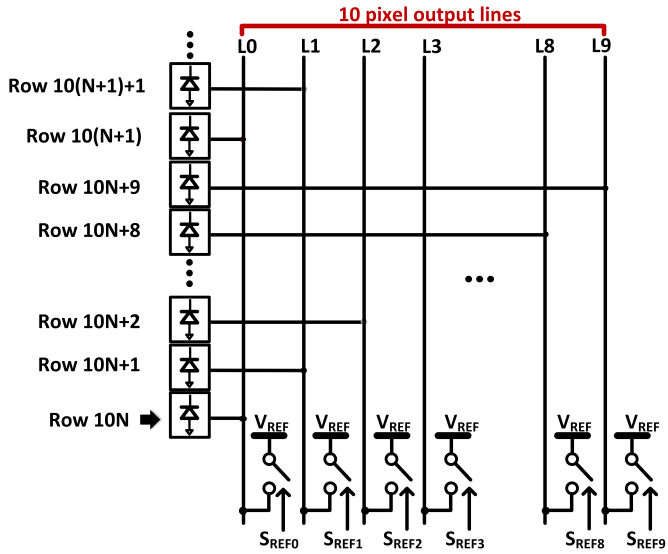


Figure 6.4: Pixel output connections and output line design within a column

6

6.1.2. PIXEL ARRAY DESIGN FOR RECONFIGURABLE SYSTEM

To implement the reconfigurable system, the pixel array must be specifically designed to support dual-mode operation. In particular, the pixel array requires 10 output lines per column to enable efficient readout of a 10×10 Region of Interest (ROI) window during zoom-in mode. These output lines also support line-by-line readout during normal mode without requiring separate routing networks.

Figure 6.4 illustrates a pixel output connection within a single column, where each output line is connected to one pixel every 10 rows during normal mode. In normal mode, the row decoder selects the appropriate row based on the vertical domain address (VDA), and only one-pixel output line per column is active at a time. To prevent floating output lines from generating fixed pattern noise (FPN) or temporal noise, the unused output lines are connected to the reference voltage, V_{REF}, via the 10 S_{REF} switches. The reference voltage is set to match the pixel output's reset level, ensuring rapid settling. Each of the 10 switches (S_{REF0} to S_{REF9}) is controlled by a dedicated VDA (112 to 121), transmitted alongside the VDA for pixel readout.

Figures 6.5(a) through 6.5(d) illustrate the pixel array control within a column, while Figure 6.5(e) provides the timing diagram. For example, when the image sensor receives a VDA of 10, the row decoder activates the pixels in the 10th row and transmits the pixel output to the ADC via the output line 0, L0. Simultaneously, the row decoder turns off switch S_{REF0} by receiving VDA 112, grounding the remaining output lines. Similarly, when VDA 11 is transmitted, output line 1, L1, is used, and switch S_{REF1} is deactivated via VDA 113. This cycle repeats as rows are selected, ensuring that unused output lines are grounded for optimal noise performance. When the row decoder processes higher VDAs, such as 20, output line 0, L0, is reused, and switch S_{REF0} is deactivated via VDA

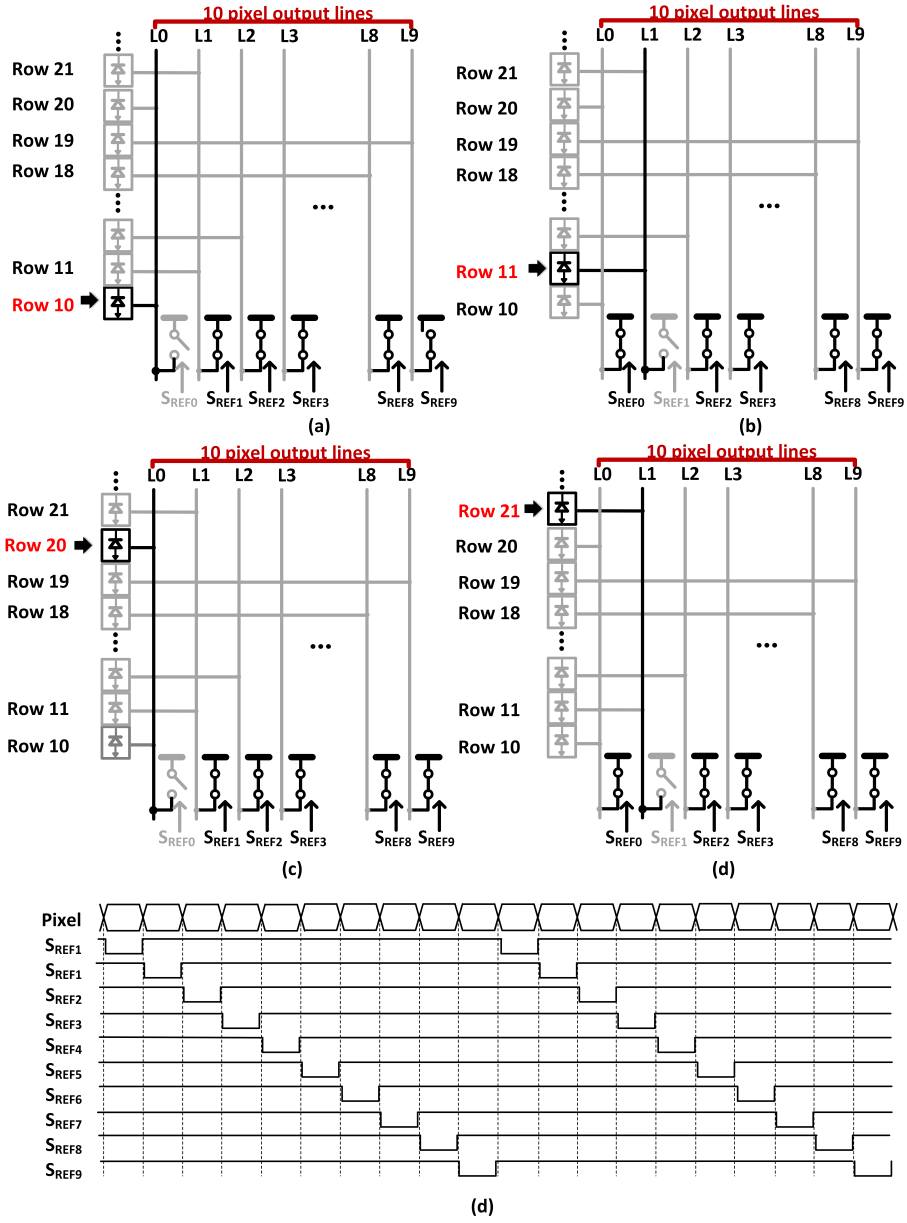


Figure 6.5: Pixel and switch control within a column when VDA is (a)10, (b)11, (c)20 and (d)21 and (d) the switch SREF control timing

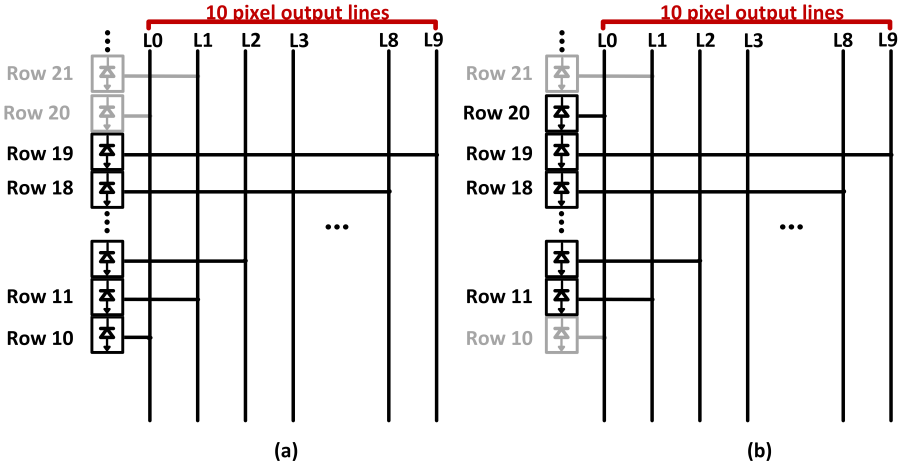


Figure 6.6: Pixel control in zoom mode with VDA of (a) 10 and (b) 11

112. The timing diagram in Figure 6.5(e) comprehensively illustrates the pixel output line selection and VDA configuration during normal mode operation.

The row decoder enables 10 pixels to output pixel data in zoom-in mode, and ten output lines are fully used. Since ten lines are fully used, the switches from S_{REF0} to S_{REF9} are deactivated during zoom-in mode. To activate 10 rows at the same time, the row decoder receives a VDA and activates the additional 9 rows above the selected rows. For example, with VDA of N, the row decoder enables the pixels located from the Nth row to N+9th row. Figures 6.6(a) and (b) show the pixel control example during zoom-in mode. For instance, if the row decoder receives a VDA of 10, the pixel outputs from the 10th to 19th row are sequentially transmitted to the ADC through the pixel output line 0, L0, to pixel output line 9, L9. During the operation, the pixel output at the pixel output line 0, L0, is from the pixel corresponding to the lowest address. However, if the image sensor receives a VDA of 11, the pixel output comes from the pixel from the 11th row to the 20th row. The pixel output at the pixel output line 0, L0, is from the pixel corresponding to the highest address.

In summary, the pixel array design ensures efficient dual-mode operation by enabling parallel readout during zoom-in mode and minimizing noise in normal mode through S_{REF} switches. These features are essential for the reconfigurable system's adaptability and performance.

6.1.3. ACCESSING ROW AND COLUMN IN RECONFIGURABLE SYSTEM

To enable the reconfigurable system, the image sensor must dynamically adjust the number of accessible rows and columns based on its mode. All ADCs operate synchronously during normal mode, while in zoom-in mode, ADC control is partially synchronized based on their array location, as detailed in Section 5.2. These functionalities are supported by the row decoder and horizontal address decoder, which use the VDA and HDA signals from the FPGA to activate the selected rows and columns. As illustrated in Fig-

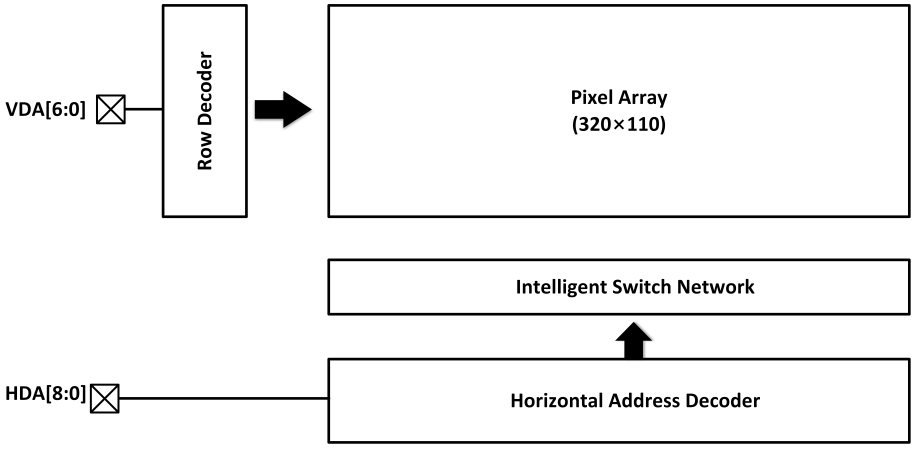


Figure 6.7: Pixel and switch network control using the row decoder and horizontal address decoder in reconfigurable system

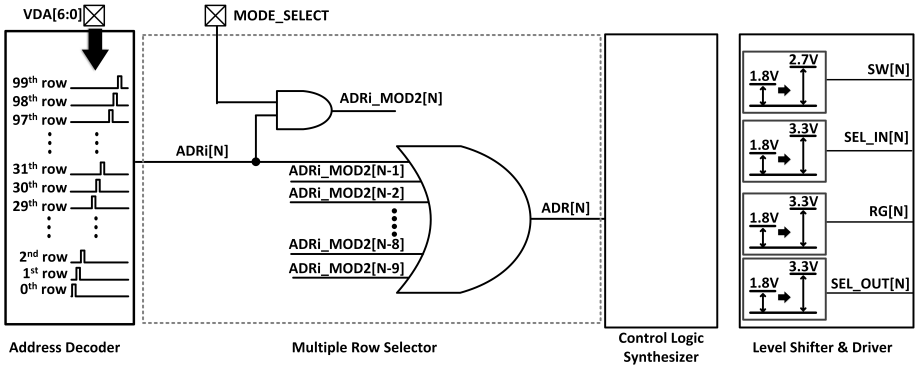


Figure 6.8: Multiple row selector design with AND and OR gate

ure 6.7, the row decoder controls the pixel, and the horizontal address decoder controls the intelligent switch network. The MODE_SELECT signal governs these operations according to the sensor's mode.

ENABLING ROI REGION USING VDA AND HDA

The image sensor accesses all pixels within a single row during normal mode and the 10×10 ROI region during zoom-in mode. To realize this operation, the row decoder and horizontal address decoder are equipped with a multiple row selector and multiple column selector, respectively. The horizontal address decoder, specifically active during zoom-in mode, selects columns to access the ROI.

As mentioned in section 2.2.2, the general row decoder consists of an address decoder and the control logic synthesizer. The multiple-row selector is designed between the address decoder and the control logic synthesizer. The address decoder generates

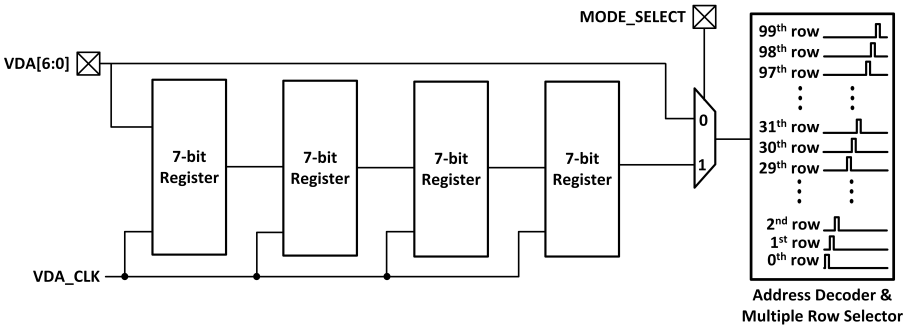


Figure 6.9: Register-based VDA capture mechanism for row synchronization

signals to activate the row specified by the VDA, while the multiple-row selector enables the simultaneous activation of multiple rows. Figure 6.8 describes the design of a multiple-row selector. Each row includes a 2-input AND gate and a 10-input OR gate. In normal mode (MODE_SELECT = 0), only the row corresponding to the VDA is activated, as the AND gates remain disabled. The AND gates are enabled in zoom-in mode (MODE_SELECT = 1), activating 10 rows simultaneously. In particular, the OR gate located in the Nth row receives the output of the AND gate, ADRi_MOD2, from the 9 rows from N-1 to N-9. For this reason, when VDA is N, rows N to N+9 are activated via the OR gates.

The horizontal address decoder mirrors the row decoder's design. With 320 columns, the HDA is a 9-bit code that enables specific column access, ensuring precise control during zoom-in mode. These enhancements allow accurate control of ROI regions, a critical feature for the reconfigurable system.

VDA AND HDA SYNCHRONIZATION

One critical challenge in the reconfigurable system is the synchronization of VDA and HDA signals, particularly due to transmission delays from the FPGA. Such delays can lead to incorrect row or column activation, especially in zoom-in mode, where precise timing is required. Normal mode uses the method described in Section 2.2.2, with the row decoder relying on multiple signals to activate the selected row. However, applying the same approach in zoom-in mode, where signal control must occur within a quarter of a horizontal line time, risks misalignment. To address this, the VDA and HDA signals are captured in registers before row and column access during zoom-in mode. The activation signals, such as RD_EN[N] and SH_EN[N], are then directly generated from the outputs of the multiple row and column selectors. This mechanism ensures precise timing by capturing signals ahead of row and column activation, mitigating the risk of misalignment during zoom-in mode. On the other hand, the row decoder operation maintains the same method explained in section 2.2.2 during normal mode.

Figure 6.9 illustrates the register-based VDA capture mechanism using a 2-to-1 MUX and a 7-bit register. In zoom-in mode (MODE_SELECT = 1), the VDA is stored in the register via a dedicated clock signal (VDA_CLK), which is activated four times within a single horizontal line period, as shown in Figure 6.11(b). During normal mode (MODE_SELECT

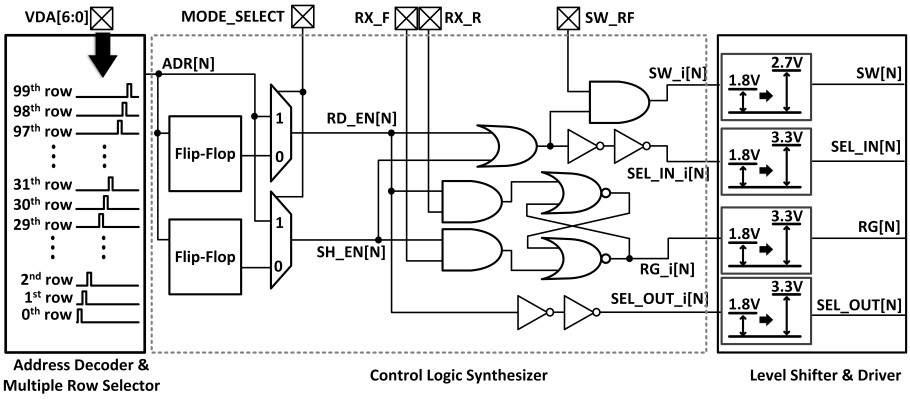


Figure 6.10: Logic synthesizer design using 2-to-1 MUX

= 0), the VDA is directly transmitted to the address decoder for single-row activation.

The generation of activation signals also adapts to the sensor's mode. During normal mode, the activation signals corresponding to the VDA are generated at the flip-flop in each row. As shown in Figure 6.10, RD_EN and SH_EN signals are derived from the multiple row selector outputs in zoom-in mode, bypassing the flip-flop-based generation used in normal mode. The 2-to-1 MUX is used to support this function. This ensures synchronized row and column activation even at reduced timing margins.

By addressing synchronization challenges, this design ensures reliable operation during zoom-in mode.

PIXEL AND ADC CONTROL DEPENDING ON THE MODE

As mentioned above, controlling the number of rows and columns accessible to the image sensor is essential. However, generating appropriate control signals to control the pixels and ADCs depending on the image sensor operation is also important.

Figures 6.11(a) and (b) illustrate the timing during the normal mode and zoom-in mode, respectively, and Figure 6.11(c) includes the pixel structure controlled by the signals from Figures 6.11(a) and (b). Pixel control signals, including SW_RF, RX_F, RX_R, and MODE_SELECT, are routed through the row decoder, as depicted in Figure 6.10. In normal mode, reset and read operations are performed separately, with the duration $T_{\text{INT\_NOR}}$ representing the pixel's charge integration time, as explained in Figure 6.11(a). In zoom-in mode, pixel control occurs within a condensed period equal to a quarter of the horizontal line time. Reset and read operations are performed within the same sampling period and are repeated three times per horizontal line time. To achieve this, SW is set to 1 during zoom-in mode. At the beginning of each sampling period in zoom-in mode, RX_R sets RG to 1, triggering the pixel reset signal. Once reset sampling at the ADC is complete, RG is switched to 0 by RX_F. The timing in Figure 6.11(b) shows that $T_{\text{INT\_ZM}}$, the charge integration time during zoom-in mode, is shorter than $T_{\text{INT\_NOR}}$ due to the need to complete operations within a quarter of the horizontal line time.

Like pixel control, ADC control varies based on the image sensor mode. In this design, ADC control logic comprises an ADC timing generator and an ADC signal gener-

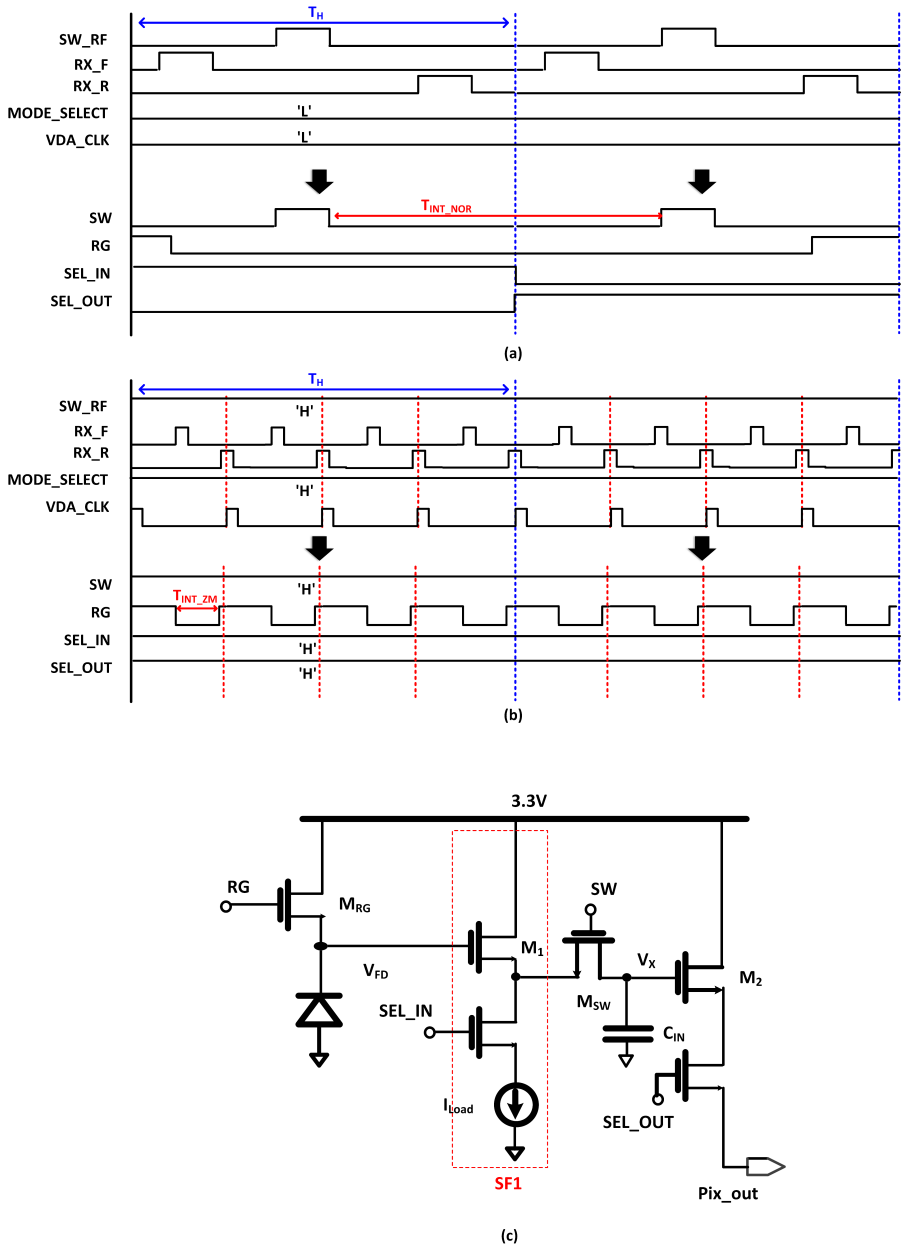


Figure 6.11: Timing diagram for control row decoder in (a) normal mode and zoom-in mode and (c) the pixel structure control by the signals in the timing

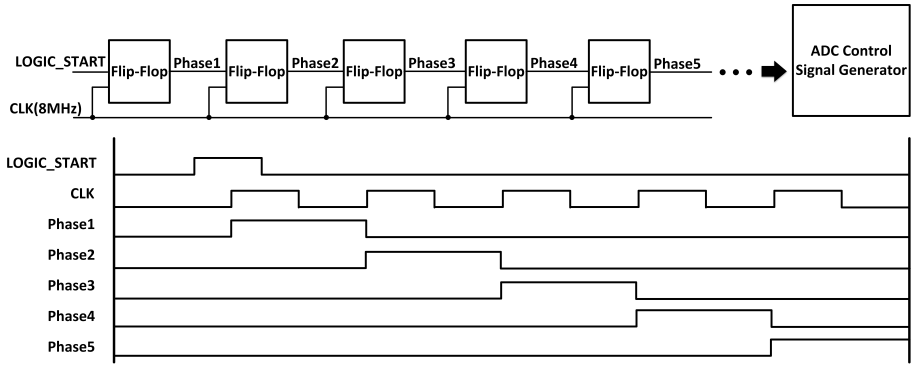


Figure 6.12: (a) Block diagram of ADC timing generation logic and (b) the associated timing

ator. Figure 6.12(a) illustrates the ADC timing generator utilizing flip-flops, while Figure 6.12(b) outlines the relevant timing. The FPGA transmits LOGIC_START to the ADC timing generator, controlled by an 8 MHz clock, as detailed in Section 2.4.1. The ADC timing generator uses 32 flip-flops, each outputting a signal set to 1 sequentially for one clock period. These outputs are sent to the ADC signal generator to produce the required ADC control signals. Once the LOGIC_START signal is transmitted to the ADC control logic, the ADC control signals are automatically generated.

Figure 6.13(a) illustrates the block diagram of the ADC control logic, including the ADC timing generator and ADC signal generator. Three identical ADC control logic blocks are employed to accommodate the three distinct ADC control timings required during zoom-in mode, each controlling 100 ADCs. The timing for both image sensor modes follows the sequence described in Figure 6.13(b). In normal mode, the ADC control signals LOGIC_START_1, LOGIC_START_2, and LOGIC_START_3 are activated simultaneously, allowing all ADCs to sample pixel outputs and perform data conversion synchronously, as shown in Figure 6.13(b). The three ADC control signals are sequentially transmitted in zoom-in mode with a quarter-horizontal-line-time interval. This staggered operation ensures efficient support for ROI mode by enabling ADCs to start their operation at different timings, aligned with the pixel outputs from the ROI.

6.1.4. CONSIDERATION OF COLUMN SCALABILITY AND TIMING CONSTRAINT

The proposed data distribution network is designed to support both column scalability and ROI region resolution scalability. In particular, the pixel structure, number of columns, and timing are all affected by changes in the total column count.

The switch network structure within a column is determined by the resolution of the ROI region, not by the total number of columns. As the number of rows in the ROI increases, the number of pixel output lines and corresponding switches per column increases accordingly. However, the switch network maintains a consistent structure regardless of this change. Figure 6.14(a) shows an example where the ROI region is 5×5. In this case, each column outputs 5 pixels, and the switch network includes 5 pixel output lines. The number of horizontal lines is also 25, matching the total number of pixels in

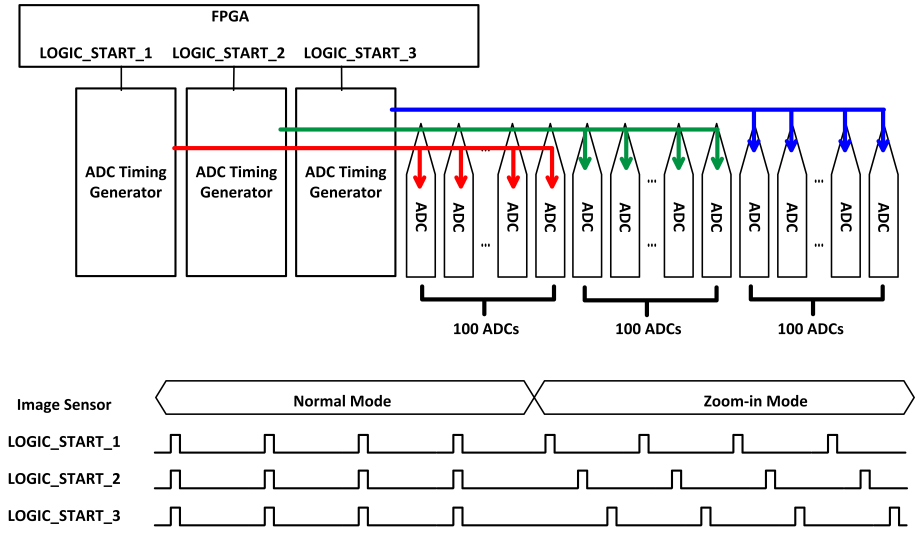


Figure 6.13: 3 identical ADC control logics to control 3 group of ADCs with the timing

6

the ROI. Figure 6.14(b) illustrates the case for a 20×20 ROI region. For this reason, each column outputs 20 pixels, and the switch network includes 20 pixel output lines. The number of horizontal lines becomes 400, equal to the number of pixels in the ROI.

The total number of columns in the pixel array is set as a multiple of the number of pixels in the ROI region. For example, if the ROI region is configured as $N_C \times N_R$ (columns × rows), the effective column count becomes $N_C \times N_R \times K$, where K is an integer. An additional 8 dummy columns are added on each side of the array to protect image integrity and edge uniformity.

In zoom-in mode, the ADC sampling time and the pixel charge integration time are affected by the number of column groups. As shown in Figure 6.15, if the effective column count is $N_C \times N_R \times K$, the ROI pixel data are divided into K groups, each assigned to one ADC sampling window. The total horizontal line time, T_H, is shared by the K groups, resulting in an ADC sampling time of T_H/K for each group.

For example, in Figure 6.3(d), the ROI is 10×10 and the effective column count is 300, corresponding to 3 groups. In this case, the condition $T_1 + T_2 + T_3 < TH$ must be satisfied. As the number of columns increases, the system forms additional column groups, each comprising 10 adjacent columns connected to a dedicated set of 100 horizontal lines. These groups are routed to separate ADC control paths using replicated S_{G1}, S_{G2}, and S_{G3} switching structures. For example, if the column count increases from 300 to 600, the number of ADC groups doubles from 3 to 6, requiring six sets of SG switches and associated control logic for parallel data routing. This modular replication ensures scalability without altering the fundamental column or ADC architecture.

Since the charge integration occurs during the ADC sampling period, shorter sampling windows result in reduced integration time. Therefore, as the number of columns increases, both ADC sampling time and pixel integration time decrease. To maintain

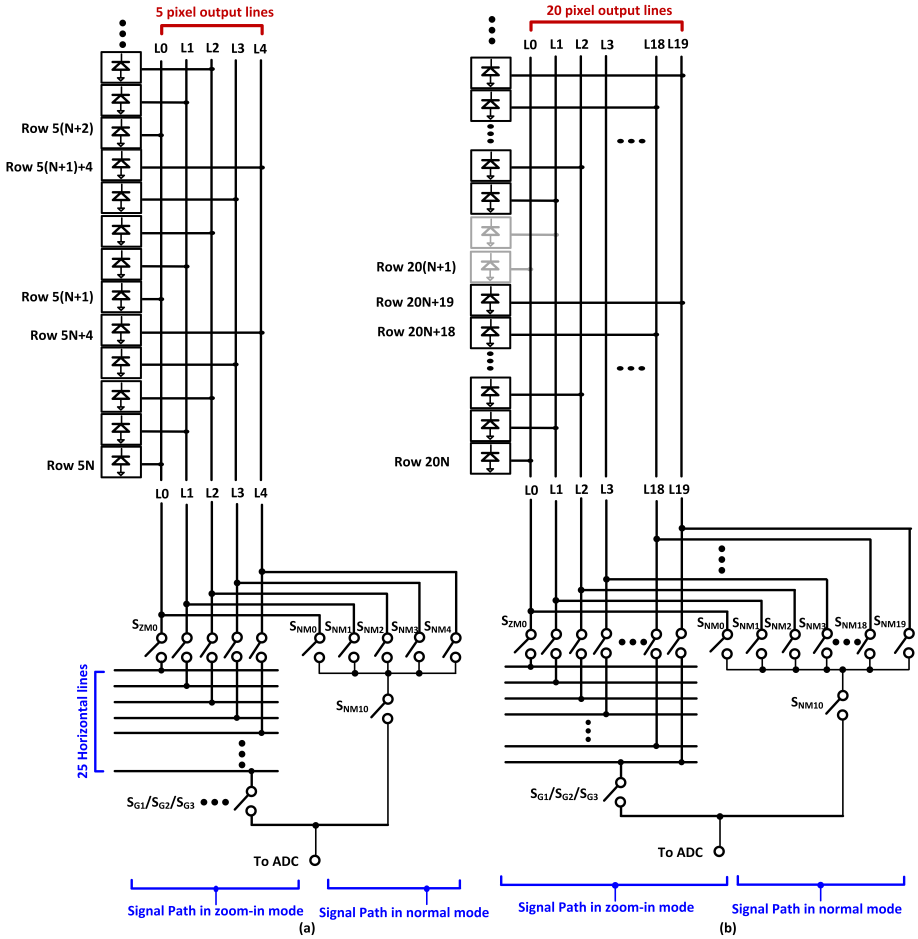


Figure 6.14: Switch network design in each column for different ROI resolutions: (a) 5×5 and (b) 20×20

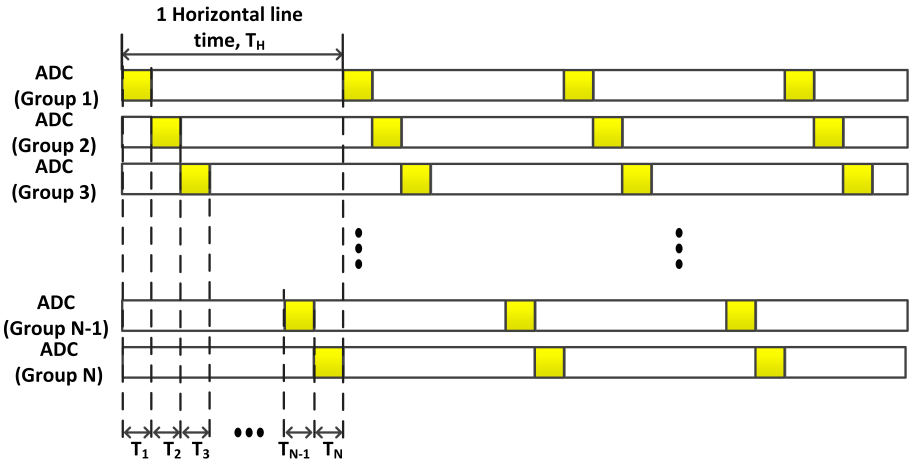


Figure 6.15: ADC sampling window allocation based on the number of column groups in zoom-in mode

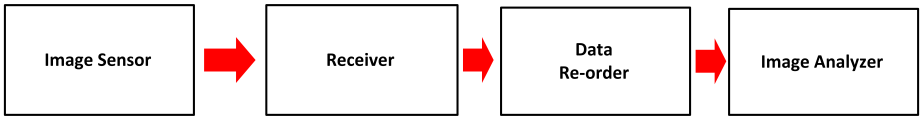


Figure 6.16: FPGA System block diagram for image data processing

image quality, the pixel sensitivity must improve accordingly. For stable performance across operating modes, the ADC sampling time in normal mode is kept constant, independent of zoom-in mode configurations.

6.2. IMAGE REARRANGEMENT PROCEDURE

As mentioned in Section 5.2.1, the captured image data from the image sensor is transmitted to the FPGA via the LVDS interface. Figure 6.16 illustrates a system block diagram of the FPGA's internal modules designed for efficient image analysis. The image data first passes through the re-order block, which is realigned to match the sensor's pixel arrangement, ensuring consistency for downstream processing. Once re-ordered, the data is sent to the image analyzer, which performs object detection.

Accurate transmission of image data from the sensor to the FPGA is crucial for effective image analysis. In addition, the image data rearrangement should reflect the pixel array's structure to ensure proper analysis. Since the order of received data can vary significantly due to operational modes and hardware configurations, implementing an efficient and adaptive data rearrangement process is essential.

6.2.1. STORING IMAGE DATA WITH 10 REGISTER ARRAY

The image data transmitted from the image sensor is stored in a register array for processing inside the FPGA. With 316 ADCs generating 316 image data per pixel line in

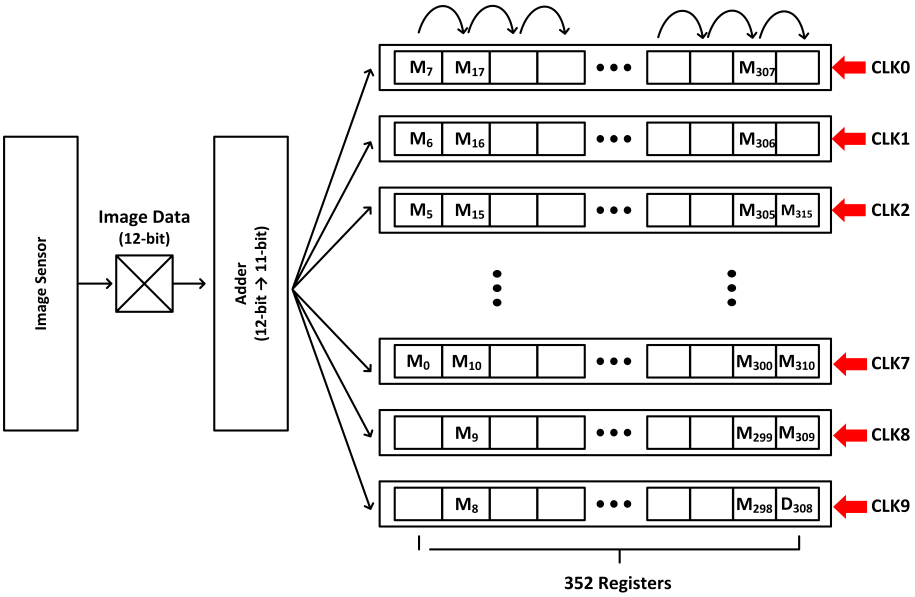


Figure 6.17: Receiver design with 10 register arrays

normal mode, each represented as a 12-bit digital code, the total data transmitted within a single pixel line is up to 3792 bits. For this reason, the FPGA requires at least 3476 registers, as the final bit format is 11 bits, as described in Section 3.3.3. These registers must operate at 128 MHz to synchronize with the 64 MHz clock controlling the image sensor.

However, maintaining a 128 MHz clock across all registers without data loss presents significant challenges. To overcome this challenge and maintain stable data transfer, the design employs 10 register arrays operating with phased clocks. This approach divides the data storage into 10 parallel paths, with each array containing 352 registers capable of storing up to 32 image data. The clock frequency for each array is reduced to 12.8 MHz, which is 10 times slower than the original 128 MHz clock. This design simplifies clock management while facilitating efficient data rearrangement in zoom-in mode, where data originates from the 10×10 ROI region.

Figure 6.17 illustrates the architecture of the receiver design, which integrates the 10 register arrays for stable and efficient data storage. Upon receiving the 12-bit image data in the FPGA, it passes through an adder to compute the final 11-bit output, as defined in Section 3.3.3. The formula for this computation is as follows:

$$D_{\text{OUT}} = \sum_{i=2}^{6} 2^{11-i} \cdot D_i + \sum_{i=8}^{12} 2^{12-i} \cdot D_i + 1.5 \cdot \left(2^9 \cdot D_1 + 2^4 \cdot D_7\right) \tag{6.1}$$

Here, D_1 is the MSB and D_{12} is the LSB of the 12-bit input image data. Figure 6.18 illustrates the phased clock operation that enables sequential data capture across the 10 register arrays. Each array functions as a shift register, moving the captured 11-bit data to

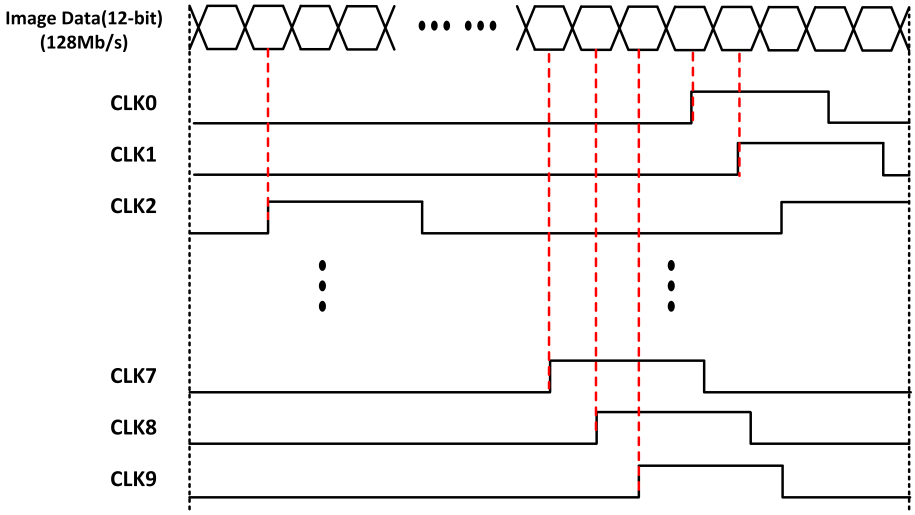


Figure 6.18: Clock control timing to capture the image data in receiver

the next register with every clock cycle. Following the timing diagram, the output, D_{OUT}, is captured by the 10 register arrays synchronized with 10-phase clocks (CLK0 to CLK9). For example, image data from the 316th column, M_{315}, is captured by CLK2 in the third register array, followed by image data from the 315th column, M_{314}, captured by CLK3 in the following register array. This process continues until all 316-image data is stored. As shown in Figure 6.17, the last image data from the 1st column of the pixel array, M_0, is stored in the eighth register array.

This design ensures stable data reception, enabling accurate downstream image analysis.

6.2.2. REARRANGING IMAGE DATA IN NORMAL MODE

The image data captured in the 10 register arrays should be rearranged to reflect the pixel arrangement of the image sensor, ensuring consistency for downstream analysis. This step is essential for formatting data in normal and zoom-in modes, enabling accurate and efficient object detection in the image analyzer.

Figure 6.19 illustrates the generation and transmission of image data from the ADC in normal mode. In normal mode, the ADC at each column generates image data by sampling the pixel output from the same column. After capturing the image data in the FPGA, the data is stored directly as shown in Figure 6.17, without requiring rearrangement.

The captured image data is then transmitted to the line memory, which consists of 3300 registers. Since the effective pixel array is a 300×90 array located in the middle of the entire pixel array, the data from the leftmost and rightmost 8 columns are excluded from active processing. The data transmission algorithm reverses the receiver's sequence for distributing captured data into the 10 register arrays. Figure 6.20 illustrates how rearranged data is transmitted to the line memory during normal mode operation. For ex-

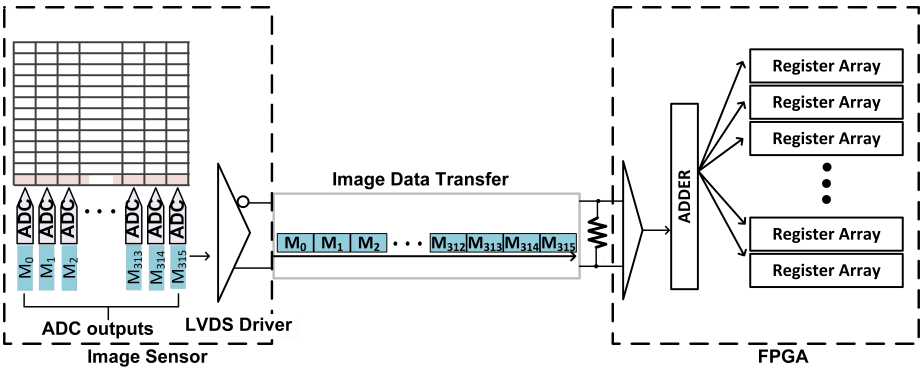


Figure 6.19: Data transmission and alignment in normal mode

ample, the effective image data's rightmost point, M_{307}, is stored in the last register of the line memory, while the leftmost point, M_8, is stored in the first register.

This process ensures that the captured image data in normal mode perfectly aligns with the pixel array, enabling seamless integration into subsequent image analysis.

6.2.3. REARRANGING IMAGE DATA IN ZOOM-IN MODE

In zoom-in mode, the location of the ROI region influences data rearrangement. The pixel design and the switch network connecting the pixel array to the ADCs play a critical role in determining the output data sequence. The VDA and HDA settings primarily govern this sequence, each capable of generating 10 distinct data arrangements.

DATA ORDER FROM THE IMAGE SENSOR

The image data order from the image sensor is highly dependent on the location of the ROI region. Understanding data order determined by VDA and HDA settings is essential for effective rearrangement algorithms. Observing the data order through specific examples provides valuable insights. Figures 6.21 and 6.22 illustrate the variations in data order for different VDA and HDA configurations with examples.

The VDA setting defines the order of 10 image data points within a single column. Figures 6.21(a), (b), and (c) provide examples of how the VDA affects the output sequence for a single column in the pixel array. For example:

- **When VDA = 10N:** The ROI region starts at row 10N. Pixel outputs from rows 10N to 10N+9 are transmitted to the ADCs. The output from the lowest row (10N) is sent to the leftmost ADC within a group of 10 adjacent ADCs, while the output from the highest row (10N+9) is sent to the rightmost ADC. Data from the rightmost ADC is transmitted to the FPGA first, and data from the leftmost ADC is transmitted last.
- **When VDA = 10N+1:** The data order shifts. Compared to Figure 6.21(a), the output from row 10N is replaced by that from row 10(N+1), as shown in Figure 6.21(b).
- **When VDA = 10N+9:** The output from row 10N+9 remains in the same position,

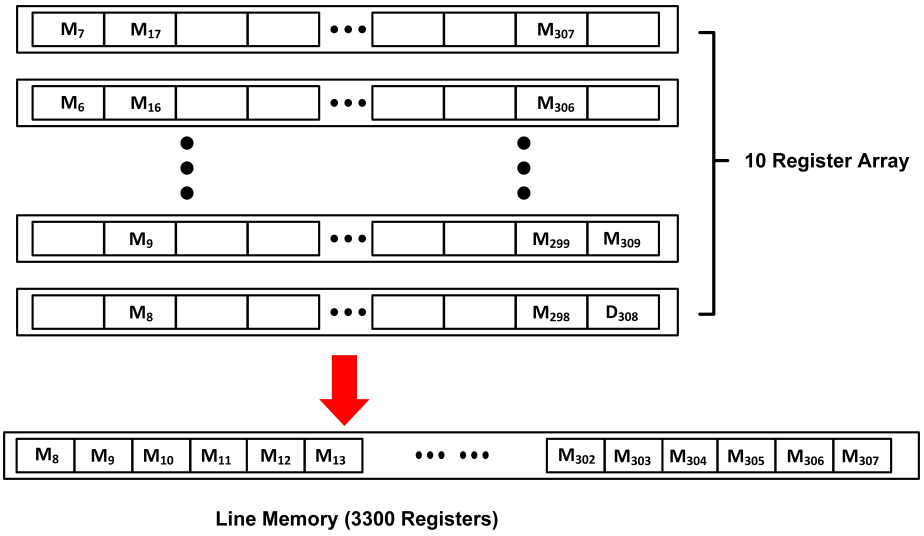


Figure 6.20: Transmitting from the 10 register array to line memory

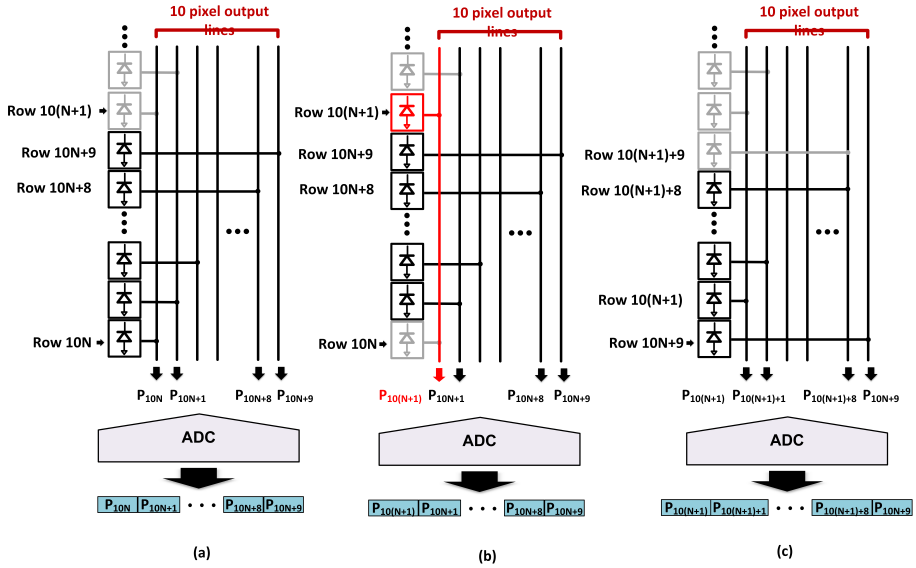


Figure 6.21: Data order example: (a) VDA = 10N, (b) VDA = 10N+1 and (c) VDA = 10N+9

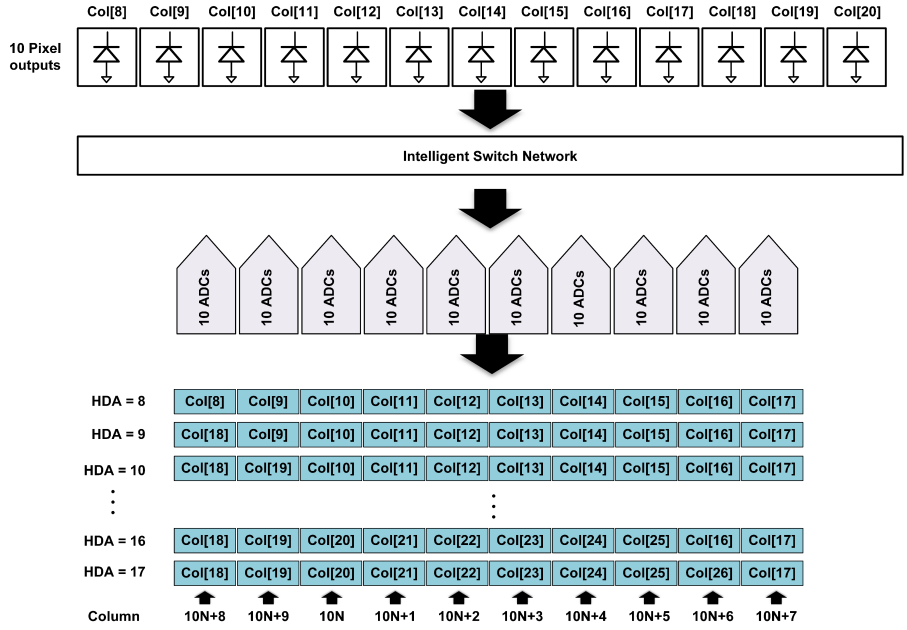


Figure 6.22: HDA impact on column output order in zoom-in mode

but outputs from all other rows are replaced by data from rows above 10N+9, as illustrated in Figure 6.21(c).

In addition, the HDA setting defines the output sequence across columns. Figure 6.22 demonstrates the impact of different HDA configurations on the output sequence. For instance:

- **When HDA = 10N+8:** The 10 image data outputs from column 10N+8 are transmitted last, while data outputs from column 10N+7 are transmitted first.
- **When HDA = 10N+9:** The data outputs from column 10N+8 are replaced by outputs from column $10(N+1)+8$, which are transmitted last.

These variations highlight the need for adaptive rearrangement algorithms to align image data with the pixel array for accurate downstream analysis.

DATA REARRANGEMENT IN ZOOM-IN MODE

Each register in zoom-in mode stores image data corresponding to a specific row and column, determined by the VDA and HDA settings. Figure 6.23 illustrates the arrangement of data before data rearrangement during zoom-in mode. Key principles of data storage include:

- Data from the same column is distributed across 10 register arrays.

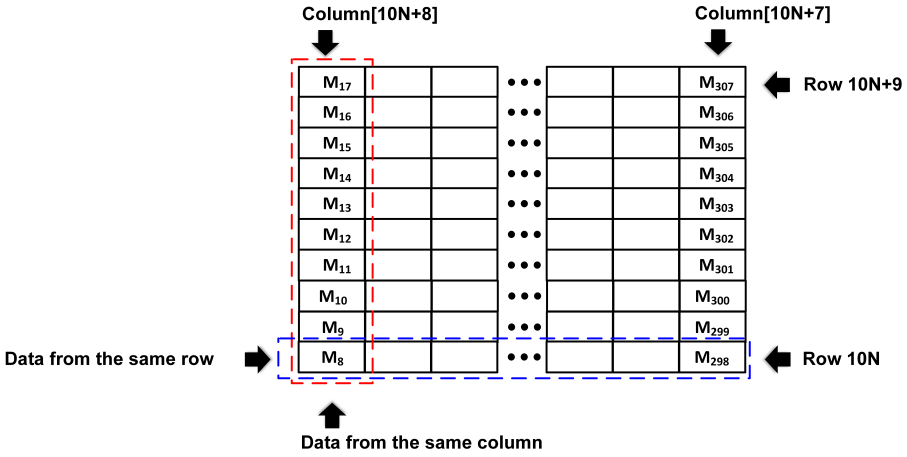


Figure 6.23: Data arrangement in zoom-in mode before data rearrangement

- Data from the same row is stored within the same register array.
- Data from row 10N is stored in the 10th register array, while data from row 10N+9 is stored in the 1st register array.
- Data from column 10N+8 is stored in the leftmost position, while data from column 10N+7 is stored in the rightmost position.

To align the data with the pixel array, the rearrangement process in zoom-in mode consists of two steps:

1. **VDA-Based Rearrangement:** Adjust the data order according to the VDA setting.
2. **HDA-Based Rearrangement:** Refine the data order based on the HDA setting.

For example, if the VDA is set to 21 and the HDA is 19, the initial data arrangement in the 10 register arrays corresponds to Figure 6.24(a). The rearrangement process proceeds as follows:

- **VDA-Based Rearrangement:** The data in the 10th register array is shifted to the 1st register array. Data from the 1st to 9th register arrays moves sequentially to the 2nd to 10th.
- **HDA-Based Rearrangement:** The data from the 1st column is shifted to the 10th column, while data from the 2nd to 10th columns shifts to the 1st to 9th columns.

This procedure is described in Figure 6.24(b), and (c) results from the data rearrangement. This process is repeated for the other nine VDA and HDA settings cases. However, when the VDA and HDA are set to 10N and 10N+8, respectively, no rearrangement is needed. Additionally, since three ROI images are transmitted simultaneously, the algorithm is applied independently to all three 10×10 ROI images.

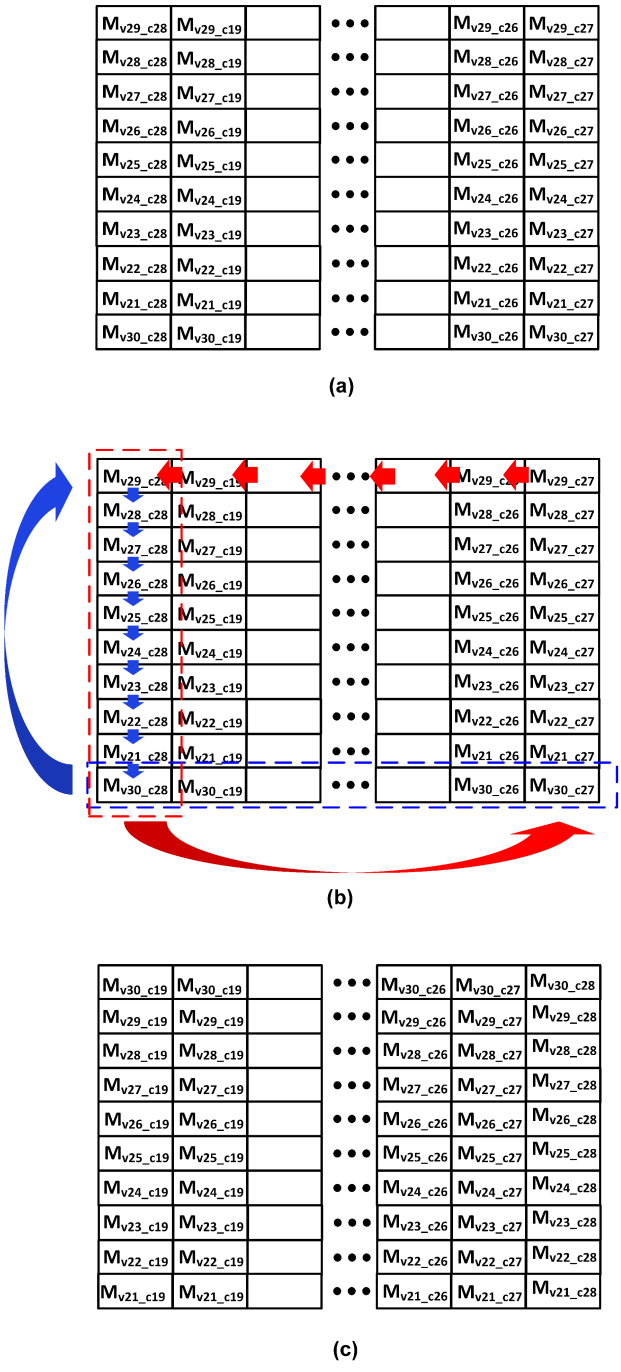


Figure 6.24: Data rearrangement procedure in zoom-in mode: (a) initial state, (b) the rearrangement operation and (c) rearrangement result

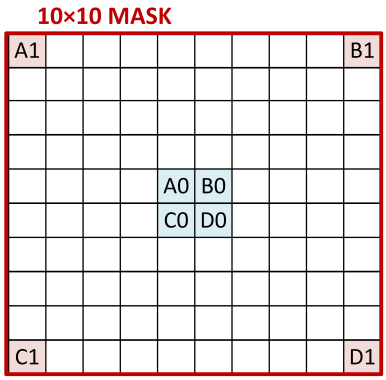


Figure 6.25: Mask design used for image analysis

After rearrangement, the processed image data is transferred to the line memory. The 10 rows of line memory capture the ROI data in the same format and arrangement as in the register arrays, ensuring compatibility for subsequent image analysis.

The dual-step rearrangement process ensures precise data alignment with the pixel array, facilitating efficient and accurate downstream image analysis.

6.3. IMAGE ANALYSIS ALGORITHM

Once the image data is reconstructed, it undergoes further processing to detect objects and extract relevant information. This process adapts based on the image sensor's operational mode.

6.3.1. IMAGE PROCESSING IN NORMAL MODE

Two key factors must be considered when performing image analysis: the type of algorithm employed and the amount of line memory required. This work utilizes 10-line memories and a sliding mask algorithm, a fundamental image analysis technique, to detect regions with significant intensity variations, particularly targeting brightly illuminated moving objects.

The algorithm uses a 10×10 mask that slides across the pixel array row by row. A comparison variable, M_{OUT}, is calculated for each position to evaluate intensity variations within the segment. A larger M_{OUT} value indicates higher intensity, helping identify areas with significant differences that may correspond to regions of interest, such as moving objects. After computing M_{OUT} across the entire image, the location with the largest M_{OUT} is selected as the ROI region, ensuring precise detection of the area of interest.

Figure 6.25 illustrates the 10×10 mask structure and the positions of variables A_0–D_1 used to compute M_{OUT} The algorithm computes M_{OUT} using the following formula:

$$M_{OUT} = (A_0 - A_1) + (B_0 - B_1) + (C_0 - C_1) + (D_0 - D_1) + C_{OFF} \tag{6.2}$$

Here, A_0, A_1, B_0, B_1, C_0, C_1, D_0 and D_1 represent the image data values within the mask window, as shown in Figure 6.25. Since M_{OUT} can result in a negative value, an

offset C_{OFF} is added to ensure all results are non-negative. In this work, C_{OFF} is set to 4096, as the most negative achievable M_{OUT} without the offset is -4096.

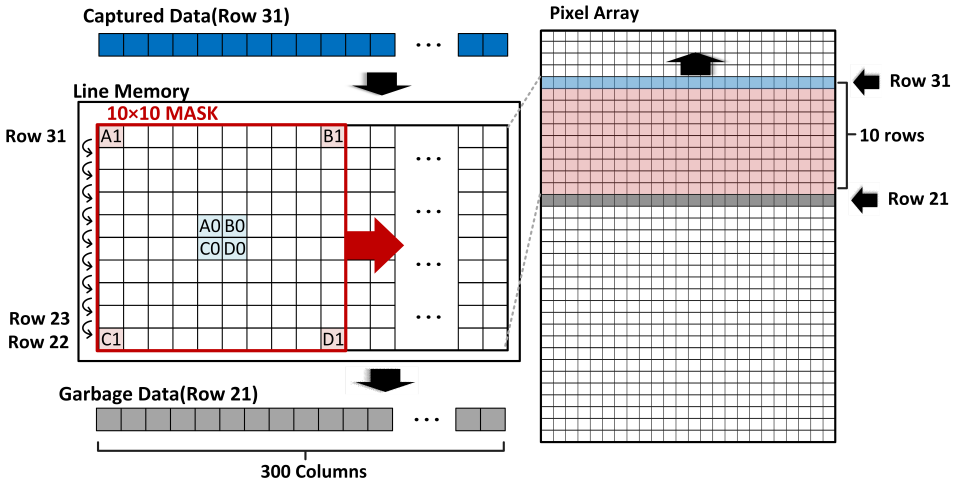


Figure 6.26: Line memory update to support real-time image analysis using sliding window technique when VDA is set to 31

As mentioned above, the image sensor dynamically updates 10-line memories to perform this algorithm. The memory stores the most recent ten rows of pixel data, updating with each new row readout. Figures 6.26 and 6.27 depict how the 10-line memories are dynamically updated during image processing. These figures illustrate the step-by-step process of updating the 10-line memories. For example, when the sensor reads the 31st row, rows 22 to 30 are stored. Upon reading the 32nd row, data shifts: rows 23 to 31 move to lines 2 to 10, the data from row 22 is discarded, and data from row 32 is stored in line 1.

Since the stored image data corresponds to a 300×10 pixel array, this process generates 290 M_{OUT} values per horizontal line, thus enabling real-time analysis without storing the entire image data. If image analysis is performed after storing the entire image, the time required to determine the ROI region would be significantly longer, and memory requirements would be much higher. Therefore, this dynamic approach ensures efficient and accurate detection of regions of interest.

6.3.2. DYNAMIC ROI CONTROL MECHANISMS

Accurately determining the location of the ROI region is critical for efficient operation in a reconfigurable system. This process requires seamless coordination across multiple functional blocks within the system. Managing operation timing and ensuring proper sequencing are essential to achieving optimal performance.

Figure 6.28 illustrates the timing diagram of the reconfigurable system during image processing in the FPGA, showing the sequence of data transfer, rearrangement, and parallel image analysis. The receiver operates with a 128MHz clock, with 512 cycles con-

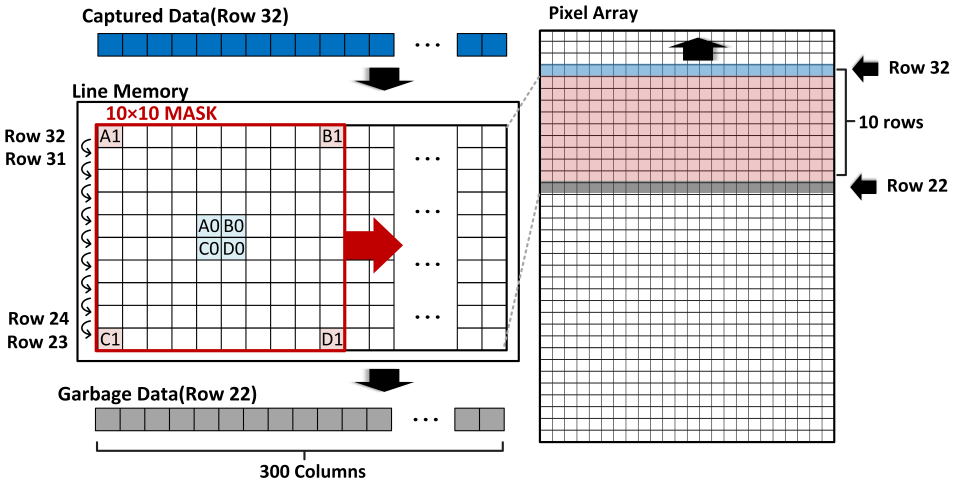


Figure 6.27: Line memory update to support real-time image analysis using sliding window technique when VDA is set to 32

6

stituting a single horizontal line time. During image data transfer from the sensor, 320 clock cycles are allocated to capture data into the FPGA, where the data is first stored in the register array described in Section 6.2.1. Following the data transfer, the data rearrangement process is performed in two steps: based on VDA and HDA. After rearrangement, the image data is moved to the line memory within the image analyzer, completing the sequence of the data transfer and data rearrangement operations within a single horizontal line time as part of the system's pipelined structure. The image analyzer applies a 10×10 mask to compute the comparison variable (M_{OUT}), which highlights regions of interest based on intensity variations, as described in Section 6.3.1. Using 290 masks simultaneously, the image analyzer generates 290 M_{OUT} values per horizontal line time. These values are then sorted in descending order to identify the top 12 highest-intensity regions within 290 clock cycles. The associated VDAs and HDAs of these top M_{OUT} values are then stored together. Image analysis and sorting operations are performed in parallel with data transfer and data rearrangement, as shown in Figure 6.27. The sorted information is incrementally updated with each processed line, ensuring continuous refinement until the entire pixel array is analyzed. After the readout of a single frame, the stored top 12 M_{OUT} values' VDAs and HDAs are used to define the ROI region for zoom-in mode operation. This efficient pipeline ensures real-time performance while maintaining the accuracy required for dynamic ROI selection, a critical feature of reconfigurable imaging systems.

6.4. CONCLUSION

This chapter presented the practical design and implementation of adaptive reconfigurable systems for image sensors, focusing on enhancing speed, flexibility, and accuracy. Key components of the reconfigurable system, including the data distribution net-

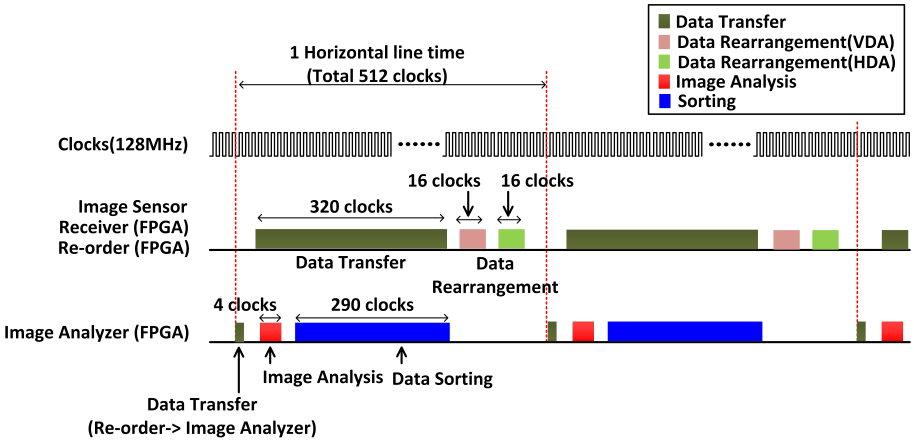


Figure 6.28: System control timing supporting image processing

work, pixel array design, and ADC control mechanisms, are thoroughly discussed. The intelligent switch network is highlighted as a critical element, enabling seamless mode switching between normal and zoom-in operations while maintaining power efficiency and preserving ADC specifications.

The chapter also detailed the data rearrangement procedure necessary to process ROI data, showcasing its role in aligning image data with the pixel array structure in normal and zoom-in modes. The design achieves efficient data handling within tight timing constraints by leveraging phased clocking and adaptive algorithms.

The image analysis algorithm is introduced, emphasizing real-time ROI detection using dynamic image processing techniques. The system efficiently processes image data, calculates comparison variables, and determines ROI regions through pipelined operations, ensuring high-speed performance with minimal data storage requirements.

Overall, this chapter demonstrated the proposed reconfigurable system's practicality and robustness, laying a solid foundation for the subsequent evaluation of its performance in Chapter 7.

7

MEASUREMENT RESULT AND DESIGN ANALYSIS

This chapter presents the experimental validation of the proposed image sensor system, focusing on two primary aspects: evaluating the analog front-end (AFE) performance in terms of fixed pattern noise (FPN) and temporal noise, and comparing frame rate and efficiency improvements enabled by the reconfigurable system. The maximum achievable frame rate is validated through comprehensive measurements. This is supported by the Analog Front-End (AFE) circuits designed to effectively manage image quality. An FPN compensation technique and detailed noise analysis to address temporal noise challenges have been rigorously verified, ensuring robust performance.

The reconfigurable system's operation is experimentally demonstrated, with an evaluation of the algorithm for identifying moving objects and the timing of mode switching—both critical to its functionality. Power consumption across various frame rates is also measured and compared with conventional image sensor operation, highlighting the system's energy efficiency.

This chapter details the measurement system's implementation, key metrics for readout circuits, and image quality. It assesses the reconfigurable system's ability to improve frame rate and operational efficiency dynamically.

7.1. SILICON PROTOTYPES AND MEASUREMENT SETUP

7.1.1. OVERVIEW OF THE FABRICATED PROTOTYPES AND READOUT ARCHITECTURES

Two prototype image sensor chips were fabricated using the TowerJazz 180 nm CMOS (1P4M) process. Both prototypes include the pixel array, readout driver (RDV), switch box (Swbox), ADC array, power management unit (PMU), and LVDS interface, following the system architecture introduced in Chapter 2.

The first chip employs a conventional column-parallel SAR ADC architecture with a discrete programmable-gain amplifier (PGA) preceding each ADC channel, as described in Section 3.2. This prototype primarily served as a functional reference to verify baseline timing and analog front-end operation. The second chip adopts the proposed 2-step SAR ADC architecture, in which the PGA functionality is merged into the ADC structure to realize a compact and low-noise residue amplification stage. Figure 7.1 shows die photographs of the two prototypes: (a) the first chip with discrete PGA and conventional SAR ADC, and (b) the second chip with an integrated 2-step SAR ADC. Both designs share the same pixel array layout and peripheral circuits, but the second chip incorporates improved control logic and expands the LVDS interface from 10 to 12 channels to support higher data throughput for high-frame-rate operation.

Each die measures 5 mm × 5 mm and contains 144 I/O pads for LVDS data, clock, and control signals. The chips operate from dual supply domains of 3.3 V for the analog and I/O circuits, and 1.8 V for the digital core and ADC blocks. Both dies were packaged in NTK CPGA-144 (ceramic pin grid array; 144 pins).

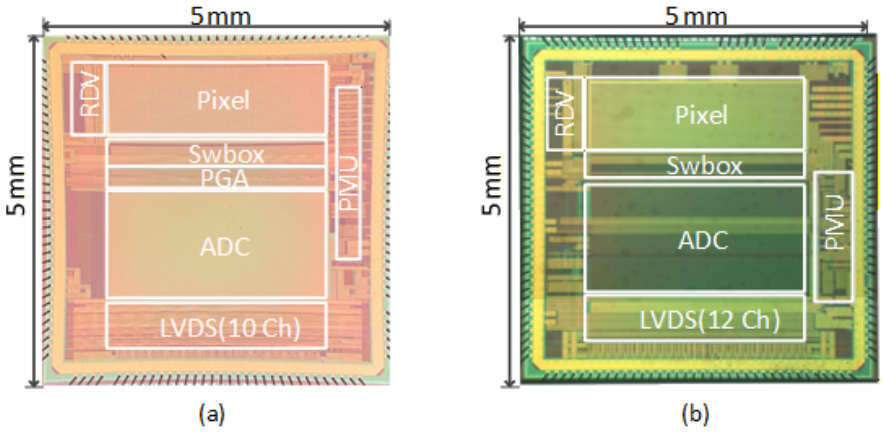


Figure 7.1: (a) First prototype with conventional SAR ADC and discrete PGA, and (b) second prototype with 2-step SAR ADC integrating the PGA.

7.1.2. OVERVIEW OF THE MEASUREMENT SYSTEM ARCHITECTURE

The measurement system in this work is built around an FPGA-based platform designed to control and evaluate the image sensor. Figure 7.2 illustrates the overall mea-

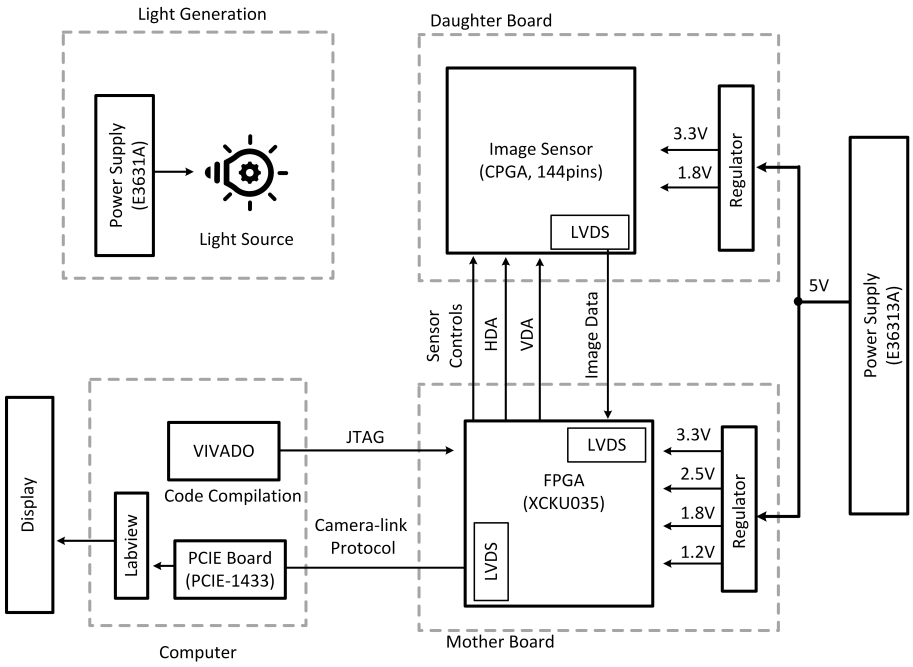


Figure 7.2: Overview of the FPGA-based measurement System

surement setup, highlighting the main components and data flow. The architecture consists of an FPGA, an image sensor, and associated PCB boards, with the FPGA mounted on the motherboard and the image sensor on the daughterboard.

The FPGA is configured using the JTAG (Joint Test Action Group) protocol, a reliable method for programming and debugging. VIVADO software compiles and writes the control code, enabling the FPGA to manage the image sensor's operations through VDA, HDA, and various control signals. The image sensor generates digital data, which is transmitted via an LVDS interface to the FPGA for processing. After processing, the data is transferred to a computer using the camera-link protocol, where a PCIe board captures it and the data is subsequently analyzed using LabVIEW and MATLAB software.

In this project, reproducible and accurate measurement characterization is achieved using a dark chamber, which ensures uniform alignment of the sensor, light source, and measurement equipment. First, a dark chamber isolates the setup from external light, providing a consistent testing environment for dark-condition evaluations and tests with a light source. In this setup, a light bulb provides controlled illumination, with its intensity regulated by a power supply to simulate varying lighting conditions. Figure 7.3 depicts the physical arrangement of the light source and PCB boards, highlighting their alignment for uniform illumination. The daughterboard is mounted perpendicularly to the motherboard, mimicking actual imaging system designs and ensuring realistic testing conditions. The light source is positioned 30 cm from the image sensor and aligned at the same height to provide uniform illumination across the sensor's surface. A stan-

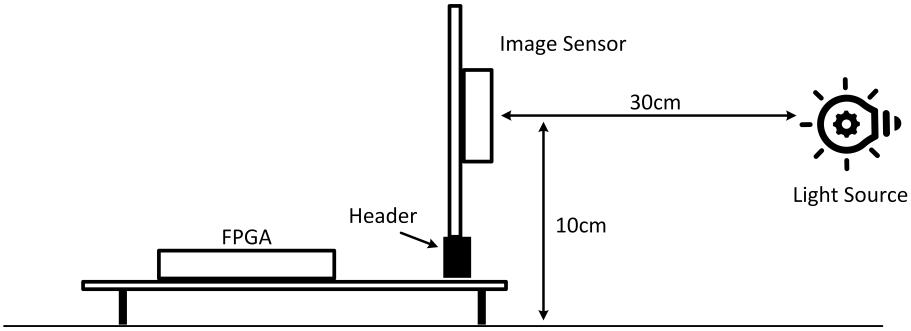


Figure 7.3: Physical arrangement of the light source and PCB boards

dard incandescent light bulb was used as the light source, providing sufficient visible light for all measurements.

As mentioned above, the testing environment facilitates precise evaluation of the image sensor's performance under controlled conditions, including noise analysis, linearity characterization, and ROI testing.

7.1.3. FPGA AND IMAGE SENSOR CONFIGURATION FOR MEASUREMENTS

The PCB architecture described in Section 7.1.2 consists of a motherboard and a daughterboard. This modular design enhances testability by independently verifying the motherboard and daughterboard components. Additionally, the FPGA resides on the motherboard, the measurement system's primary control and processing unit.

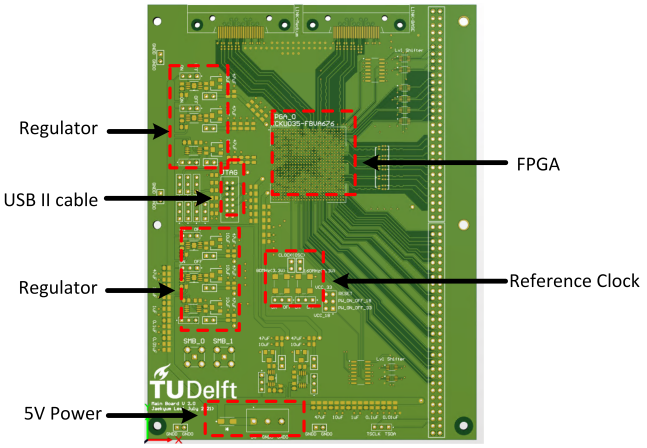


Figure 7.4: Layout of the motherboard

In this setup, the FPGA handles key tasks, including generating control signals for the image sensor and processing large amounts of image data. The design employs a total of 20 LVDS channels (12 for sensor-to-FPGA and 8 for FPGA-to-computer communication). The Xilinx XCKU035 FPGA is chosen for its high performance in meeting these demands.

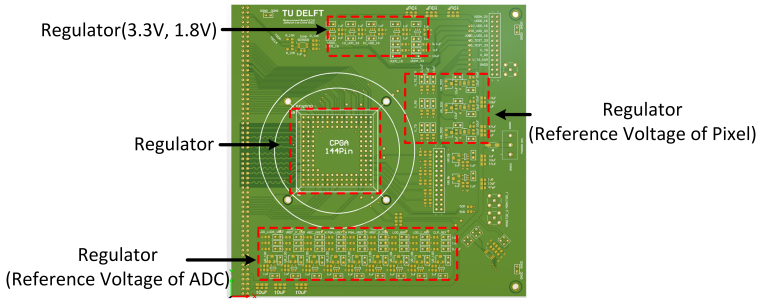


Figure 7.5: Layout of the daughterboard

Figure 7.4 illustrates the motherboard layout, highlighting the FPGA placement and its interfaces.

The FPGA is programmed via the JTAG protocol using a USB II cable for reliable configuration and debugging. Clock management is a key function of the FPGA; it employs an 80MHz reference clock multiplied and divided to generate the specific clock frequencies required by different system blocks, as detailed in Section 2.4.1. The 5V input to the motherboard is regulated to provide 3.3V, 1.8V, 1.2V, and 0.9V for the FPGA and its interfaces. For instance, the 3.3V supply supports LVTTL interfaces for most control signals, while the remaining signals are output via the 1.8V LVCMOS18 interface.

The daughterboard comprises the image sensor and regulators, providing appropriate reference voltages and power. Figure 7.5 shows the daughterboard design, detailing the image sensor and regulator configurations. The regulators on the daughterboard provide 3.3V and 1.8V power while generating critical reference voltages for the pixel array and ADC to maintain signal integrity and image quality. The regulators support the use of both internally and externally generated reference voltages. The FPGA controls these regulators following the startup sequence outlined in Section 2.4.2. The power and ground layers are designed to handle high current demands, mitigate IR drops, and ensure consistent power distribution across the PCB. Furthermore, external capacitors of up to 10μF can be placed at the reference voltage inputs to stabilize the image sensor's performance. This setup ensures robust performance and precise control by addressing the design and configuration requirements for the FPGA and the image sensor, forming the foundation for accurate and reliable measurements.

7.2. PERFORMANCE EVALUATION OF THE IMAGE SENSOR

Evaluating the image sensor's performance is essential to ensure it meets design specifications and achieves high frame rates. This section analyzes critical performance metrics, including frame rate limitations, FPN, temporal noise, and linearity. Measurements are conducted under dark and illuminated conditions to evaluate the sensor's behavior across various operational scenarios.

The frame time is set to 100 horizontal line times to optimize performance, with the maximum charge integration time matching the frame time. The 1LSB scale is also configured to 635μV since the image sensor achieves the optimal performance at 0.65V ADC

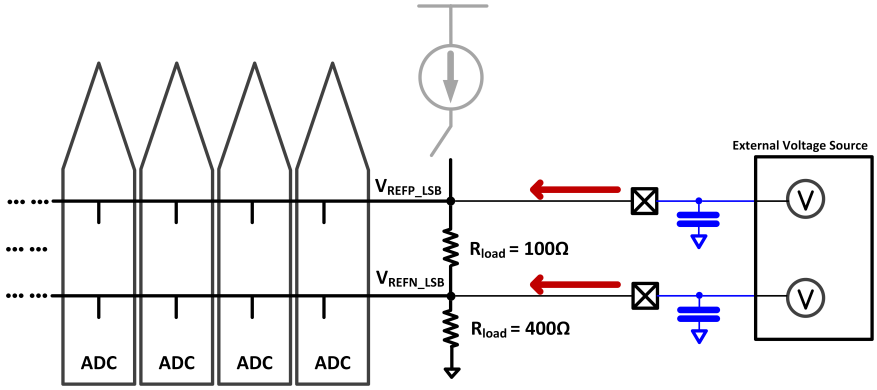


Figure 7.6: Reference voltage driver with circuit network for the ADC

saturation level. The image requires 3 reference voltages to control the ADCs: $V_{\text{REFP\_MSB}}$ for MSB conversion, $V_{\text{REFP\_LSB}}$ for LSB conversion, and V_{REFN}, shared across both MSB and LSB conversions. The measurement setup requires $V_{\text{REFP\_MSB}}$ and $V_{\text{REFP\_LSB}}$ to be set as 1.763V and 0.83V, respectively, along with a V_{REFN} of 0.8 V. The 1.763V and 0.8 V reference voltages are supplied internally by the reference driver explained in Section 2.3.3, while the 0.83V reference voltage is provided externally through the network illustrated in Figure 7.6. The external supply effectively addresses the current limitations of the internal LSB reference generator, enhancing bandwidth and ensuring stable operation of the 320 ADCs during LSB conversion.

7

7.2.1. ANALYSIS OF FRAME RATE LIMITATIONS

As discussed in Chapter 3, a SAR ADC is implemented to maximize the frame rate. The SAR ADC achieves a maximum sampling rate of 250kS/s, primarily constrained by the speed limitations of circuits designed with the 180nm process. Specifically, achieving a sampling rate higher than 250kS/s requires controlling the LVDS interface with clock frequencies exceeding 128MHz. However, operating each LVDS driver beyond 128Mb/s introduces errors such as missing codes. Consequently, 250kS/s represents the stable maximum sampling rate for the SAR ADC, ensuring reliable operation under these constraints.

Eight frame rate scenarios are tested to evaluate the image sensor's operation at different frame rates. Table 7.1 summarizes the clock and data rates required for each frame rate.

As shown in Table 7.1, the image sensor achieves a maximum frame rate of 2500fps with a horizontal line time (H-time) of 4μs. The ADC operates with an 8MHz clock at this rate, while the image sensor requires a 64MHz clock to achieve a 128Mb/s data rate per LVDS channel. The total data rate from 12 LVDS channels is 1.536Gb/s. Conversely, at the lowest frame rate of 156.3fps with an H-time of 64μs, the ADC requires a 0.5MHz clock, and the image sensor operates with a 4MHz clock, generating a total data rate of 96Mb/s across all channels.

Figure 7.7 presents the power consumption measured at each frame rate. Figure 7.7(a)

Frame rate [fps]	H-time [sec]	Image Sensor	ADC Clock [MHz]	LVDS (1 Channel)	Data rate (LVDS)
2500.0	4.00μs	64MHz	8MHz	128MHz	1.536Gb/s
1250.0	8.00μs	32MHz	4MHz	64MHz	768Mb/s
781.3	12.80μs	20MHz	2.5MHz	40MHz	480Mb/s
625.0	16.00μs	16MHz	2MHz	32MHz	384Mb/s
390.6	25.60μs	10MHz	1.25MHz	20MHz	240Mb/s
312.5	32.00μs	8MHz	1MHz	16MHz	192Mb/s
195.3	51.20μs	5MHz	0.625MHz	10MHz	120Mb/s
156.3	64.00μs	4MHz	0.5MHz	8MHz	96Mb/s

Table 7.1: Setup for different frame rates and corresponding clock and data rates

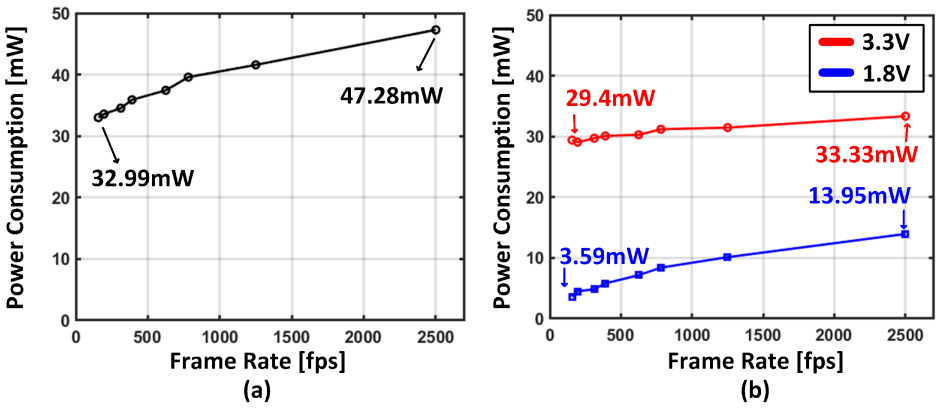


Figure 7.7: (a)Total power consumption across frame rates and (b)power contributions from 1.8V and 3.3V Supplies

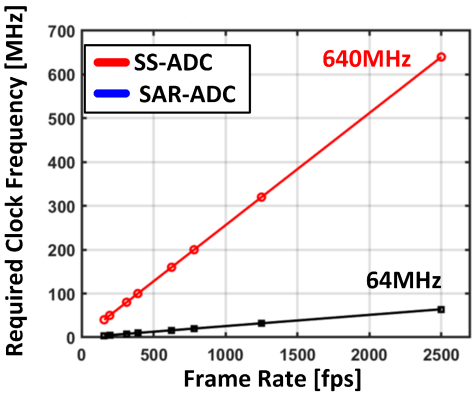


Figure 7.8: Required clock frequency comparison between single-slope ADC and SAR ADC

shows the total power consumption, while Figure 7.7(b) highlights the contributions from the 1.8V and 3.3V supplies. The 3.3V supply powers the reference generator, including the bandgap reference (BGR) and the source followers, while the 1.8V supply powers the 320 ADCs, the reference generator, and the digital circuitry. At 2500fps, the maximum power consumption is 44.6mW, with 32.5mW from the 3.3V supply and 12mW from the 1.8V supply. At 156.3fps, the total power consumption drops to 16.8mW. Notably, the 1.8V power consumption scales proportionally with the frame rate, while the 3.3V power increases discretely due to the incremental current setup of the source followers.

The SAR ADC provides significant advantages in clock speed compared to single-slope ADCs, as illustrated in Figure 7.8. A single-slope ADC achieving equivalent resolution (10.5-bits) would require 2560 clock cycles per horizontal line time, necessitating offset suppression using DDS techniques. Additionally, the current-steering DAC and counter in single-slope ADCs demand significantly higher clock speeds. For instance, to achieve a frame rate of 2500fps, a single-slope ADC would require a 640MHz clock, compared to the 64MHz clock needed for the SAR ADC. Similarly, at 156.3fps, a single-slope ADC would need an 80MHz clock, while the SAR ADC operates at just 8MHz. Figure 7.8 highlights these clock speed differences between the two ADC architectures.

7.2.2. FIXED PATTERN NOISE EVALUATION AND ANALYSIS

FPN is categorized into horizontal FPN (HFPN) and vertical FPN (VFPN), as discussed in Chapter 4. In this design, HFPN is relatively less significant due to the nature of the column-parallel readout architecture, while VFPN is mitigated using a compensation technique based on optical black pixels (Section 4.3.3.2). However, the two-step ADC is limited by its inability to achieve 0.25LSB precision using only 56-unit capacitors in the capacitive DAC, rendering the FPN calibration technique described in Section 4.3.3.1 inapplicable.

VFPN measurements are conducted under dark conditions using the dark chamber described in Section 7.1.1, effectively eliminating external light interference. To minimize temporal noise, 100 images are captured and averaged. VFPN is calculated as the

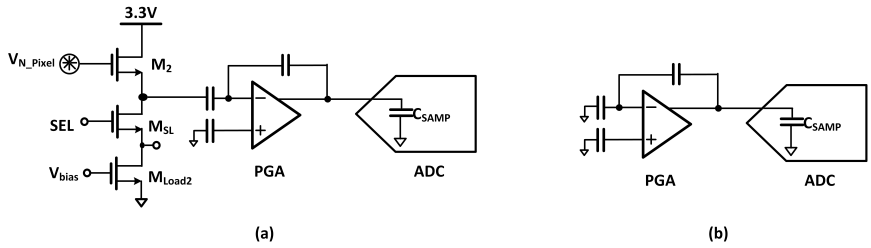


Figure 7.9: Measurement set up: (a) Pixel+PGA+ADC path, (b) PGA+ADC only

standard deviation of the column-wise averages in the resulting averaged image.

Measurement results indicate that the primary source of VFPN originates from the ADC. To isolate the error source, two measurement setups are employed: one capturing column-wise averaged outputs including the pixel array (Figure 7.9(a)) and the other excluding the pixel array's contributions (Figure 7.9(b)). Figure 7.10(a) illustrates the column-wise outputs without FPN calibration, clearly showing similar VFPN patterns for both measurement conditions. In contrast, Figure 7.10(b) presents the results after calibration, where VFPN is significantly reduced. Before calibration, the standard deviations for outputs, including and excluding the pixel array, are 17.8LSB and 16.8LSB, respectively. Moreover, the VFPN patterns between these 2 results are similar, confirming that the pixel array's contribution to VFPN is negligible. After FPN calibration, the standard deviations improve significantly to 0.34LSB and 0.24LSB, respectively.

The root cause of ADC-induced VFPN is the limited bandwidth of the ADC reference voltage distribution network, as illustrated in Figure 7.6. Each 6-bit ADC employs 56-unit capacitors in both the positive and negative branches of the capacitive DAC, with each unit capacitor sized at 14 fF. Across 320 ADCs, the total capacitive load reaches approximately 500 pF. Layout analysis further indicates that the resistance of the reference distribution path is in the range of 100–200 Ω, mainly due to the long and narrow metal routing from the reference buffer to each column. Consequently, the resulting RC time constant ($\tau = R \times C$) is approximately 100–200 Ω × 500 pF = 50–100 ns, which is longer than the 25 ns settling time required for the 250 kS/s ADC operation (4 µs horizontal period divided by 160 conversion steps). Incomplete settling of the reference voltage during the LSB conversion causes bit-dependent voltage errors across columns, manifesting as vertical fixed-pattern noise (VFPN) in the output image.

Figure 7.11 illustrates the reference voltage switching behavior during LSB conversion. During this phase, a notable voltage dip occurs after MSB DAC settling, and the reference voltage only fully recovers after the entire conversion process is complete. These fluctuations interfere with accurate bit decision and thus contribute significantly to VFPN.

Additional measurements corroborate this analysis. As shown in Figure 7.12 and summarized in Table 7.1, VFPN is approximately 0.34LSB at an H-time of 4μs, decreasing to 0.25LSB at an H-time of 8μs. As H-time increases, VFPN performance stabilizes due to adequate DAC settling time, reaching a minimum value of 0.14LSB at an H-time of 51.2μs.

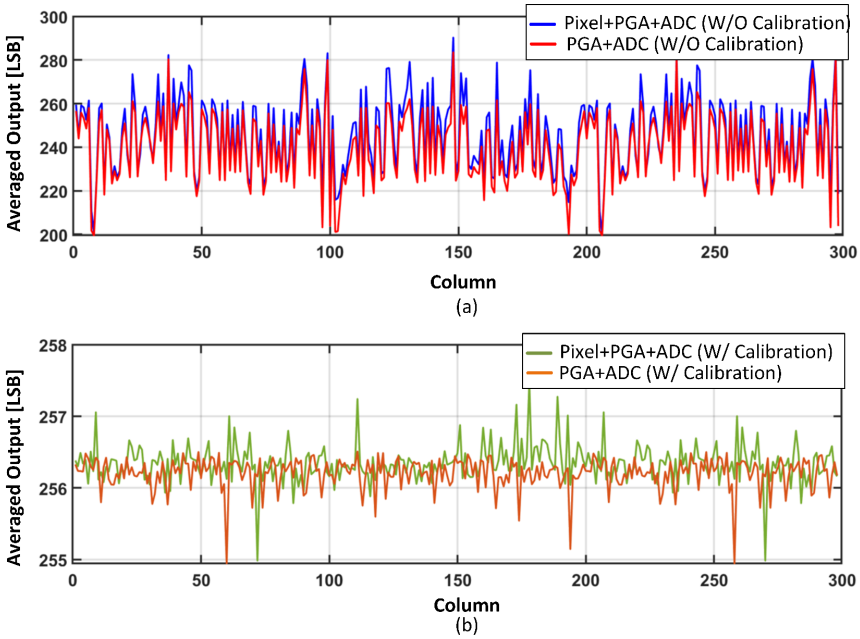


Figure 7.10: (a) Column-wise outputs without FPN calibration and (b) column-wise outputs with FPN calibration

7

7.2.3. TEMPORAL NOISE EVALUATION AND ANALYSIS

Temporal noise, a critical metric in image sensor performance, is measured under dark conditions using the same setup as FPN evaluations, as illustrated in Figure 7.9(a) and (b). Figure 7.9(a) includes all components on the data path, such as the pixel, source follower, PGA, and ADC, while Figure 7.9(b) isolates the PGA and ADC, excluding contributions from the pixel and source follower. 100 images are captured for each condition, and the standard deviation of intensity at each pixel is calculated. The temporal noise is defined as the median of these standard deviations across all pixels.

Figure 7.13 presents the measured temporal noise at various frame rates listed in Table 7.1. At the maximum frame rate of 2500fps, $\sigma_{\text{Total}} = 560\ \mu$V. For frame rates below 625fps, the temporal noise stabilizes at an $\sigma_{\text{Total}} = 380\ \mu$V. This noise reduction is attributed to the decreased bandwidth of the PGA and the extended ADC integration time per cycle at lower frame rates.

To understand the contribution of individual components, temporal noise is analyzed using the noise model described in Section 4.2. The PGA's load current is systematically varied, directly influencing its bandwidth and transconductance. A horizontal line time (H-time) of 16μs is maintained for all tests to ensure consistency. The PGA load current is incrementally adjusted from 2.5μA to 10μA in steps of 1.25μA, while the source follower load current is fixed at 16μA. This high current in the source follower provides sufficient bandwidth to minimize its noise contribution, isolating the effects of the PGA.

The temporal noise, as influenced by the PGA's bandwidth, originates from both the

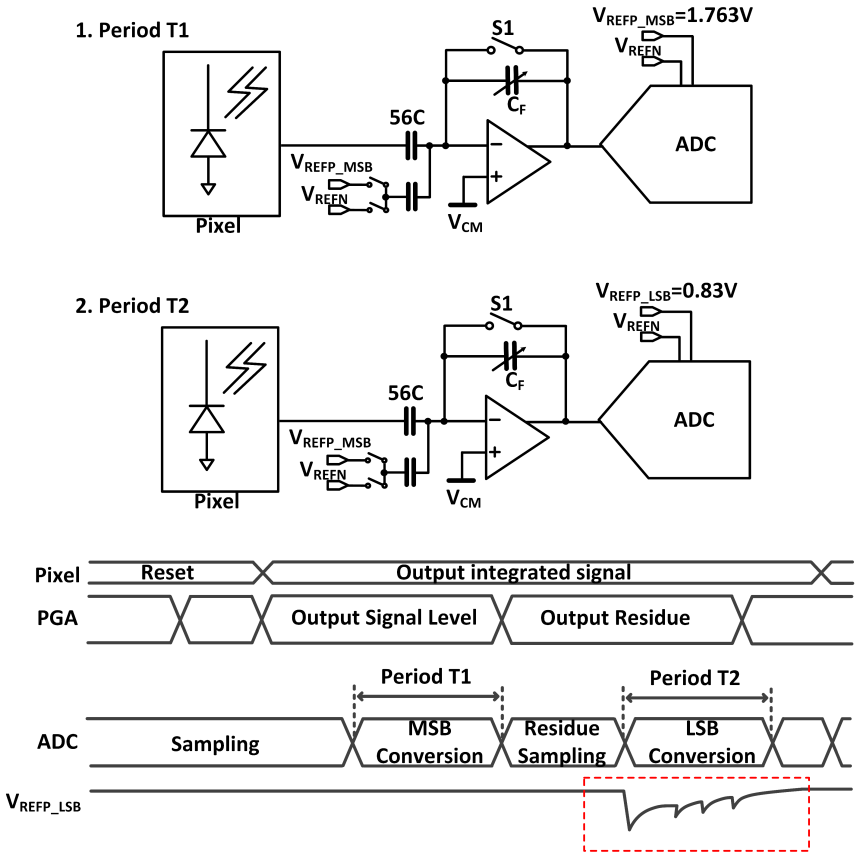


Figure 7.11: Reference switching timing and reference connection at each case

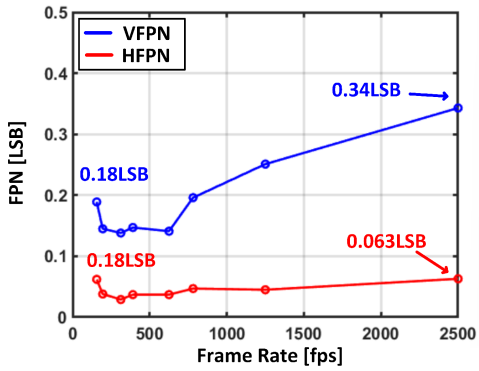


Figure 7.12: Measured VFPN and HFPN across the frame rate

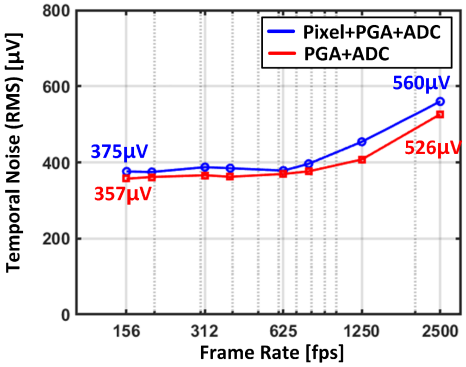


Figure 7.13: Measured temporal noise across different frame rates

PGA and the source follower and can be expressed as:

$$\sigma^2_{\text{MEA}} = \sigma^2_{\text{STATIC}} + \int_0^{f_{\text{PGA}}} S_{v,\text{VAR}}(f)\, df \approx \sigma^2_{\text{STATIC}} + S_{v,\text{VAR}}(0)\, f_{\text{PGA}} \tag{7.1}$$

Here, σ_{MEA} represents the RMS temporal noise measured, f_{PGA} is the PGA's bandwidth, σ_{STATIC} represents noise components unaffected by PGA bandwidth (including noise from pixels, ADC, and quantization), and $S_{v,\text{VAR}}(f)$ denotes the power spectral density of noise from the source follower and PGA. Using this equation, the measured temporal noise for PGA currents of 2.5μA and 10μA are:

$$(372.3\ \mu\text{V})^2 = \sigma^2_{\text{STATIC}} + \sigma^2_{\text{VAR}} \tag{7.2}$$

$$(420.3\ \mu\text{V})^2 = \sigma^2_{\text{STATIC}} + k\,\sigma^2_{\text{VAR}} \tag{7.3}$$

Here, $\sigma^2_{\text{VAR}} = \int_0^{f_{\text{PGA}}} S_{v,\text{VAR}}(f)\, df \approx S_{v,\text{VAR}}(0)\, f_{\text{PGA}}$, and $k = 2$ reflects the doubling of the PGA bandwidth when its load current increases by a factor of four, since the transconductance of the amplifier is proportional to the square root of its bias current ($f_{\text{PGA}} \propto \sqrt{I_{\text{bias}}}$). Solving these equations yields $\sigma_{\text{SF+PGA}} = 195.2\ \mu$V contributed by the source follower and PGA.

Using the same approach, noise contributions from the ADC and PGA are estimated for the setup shown in Figure 7.9(b). $\sigma_{\text{PGA}} = 178.7\ \mu$V. Considering $\sigma_Q = 155\ \mu$V, $\sigma_{\text{ADC}} = 252.5\ \mu$V. These component-specific noise contributions are summarized in Figure 7.14(b).

Figure 7.14(b) highlights the ADC as the dominant noise source, followed by the source follower and pixel. These results indicate that effective noise reduction strategies should prioritize improvements in ADC design and bandwidth optimization for both the source follower and PGA. By addressing these areas, the temporal noise performance of the image sensor can be significantly enhanced.

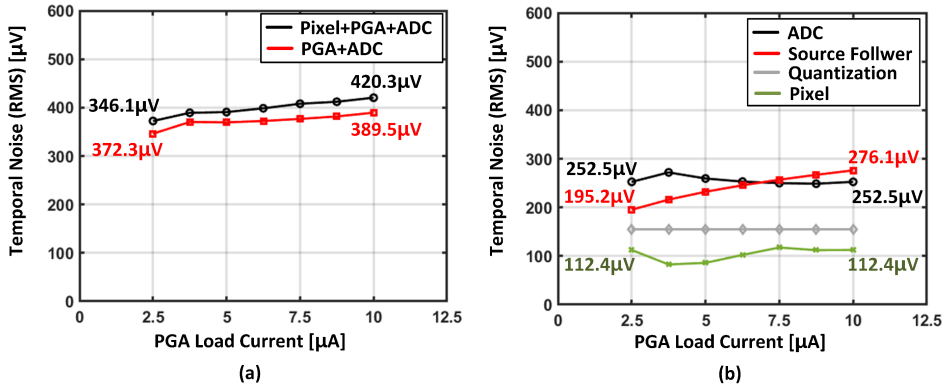


Figure 7.14: Temporal noise across different PGA current: (a) including and excluding pixel, and (b) noise factor contributions

7.2.4. LINEARITY CHARACTERIZATION USING PTC CURVE

The linearity characterization is performed using the light source described in Section 7.1.1. Measurements are taken by varying the exposure time to control the light reaching the sensor while maintaining constant light intensity. As with the VFPN measurement, 100 images are captured and averaged to generate a single output image. The averaged output value from a 50×50 pixel region at the sensor's center is used for characterization.

The light intensity is defined as the condition where the pixel output, including offset, reaches code 512 after ADC conversion with an exposure time of 32.768ms. To achieve this level, the supply voltage applied to the light bulb is set to 3.9V, corresponding to an estimated illumination of 0.2lux. The horizontal line time is configured to 8μs.

This configuration is chosen so that each ADC output code increment corresponds to a time difference of 8 horizontal line periods, providing a DNL measurement resolution of 0.125LSB. Code 512, positioned near the midpoint of the ADC range, is selected as the reference level because it provides sufficient signal amplitude, making the measurements more robust against minor inaccuracies in light intensity. In contrast, using lower code values would make the results more sensitive to variations in light source conditions, potentially compromising measurement consistency.

Figure 7.15 presents the differential nonlinearity (DNL), integral nonlinearity (INL), and transfer curves of the readout chain designed for this sensor. As shown in Figure 7.15(b) and (c), the measured DNL is +0.36/−0.28LSB, while the INL is +0/−12.46LSB. These results indicate that the DNL performance is satisfactory, whereas the INL performance is suboptimal. Figure 7.15(a) presents the measured Photon Transfer Curve (PTC) compared with the ideal response. The measured PTC curve inherently reflects the effects of INL, as it is derived from the actual ADC output behavior. While the deviation is about 1.02% at mid-code, it increases to 1.91% and 3.22% as the output approaches the maximum code.

The nonlinearity originates from variations in the current consumed within the pixel, fluctuating by up to 2.5% depending on the output signal level. Figure 7.16(a) and (b) illustrate the circuit block diagrams inside the pixel and signals at the first source fol-

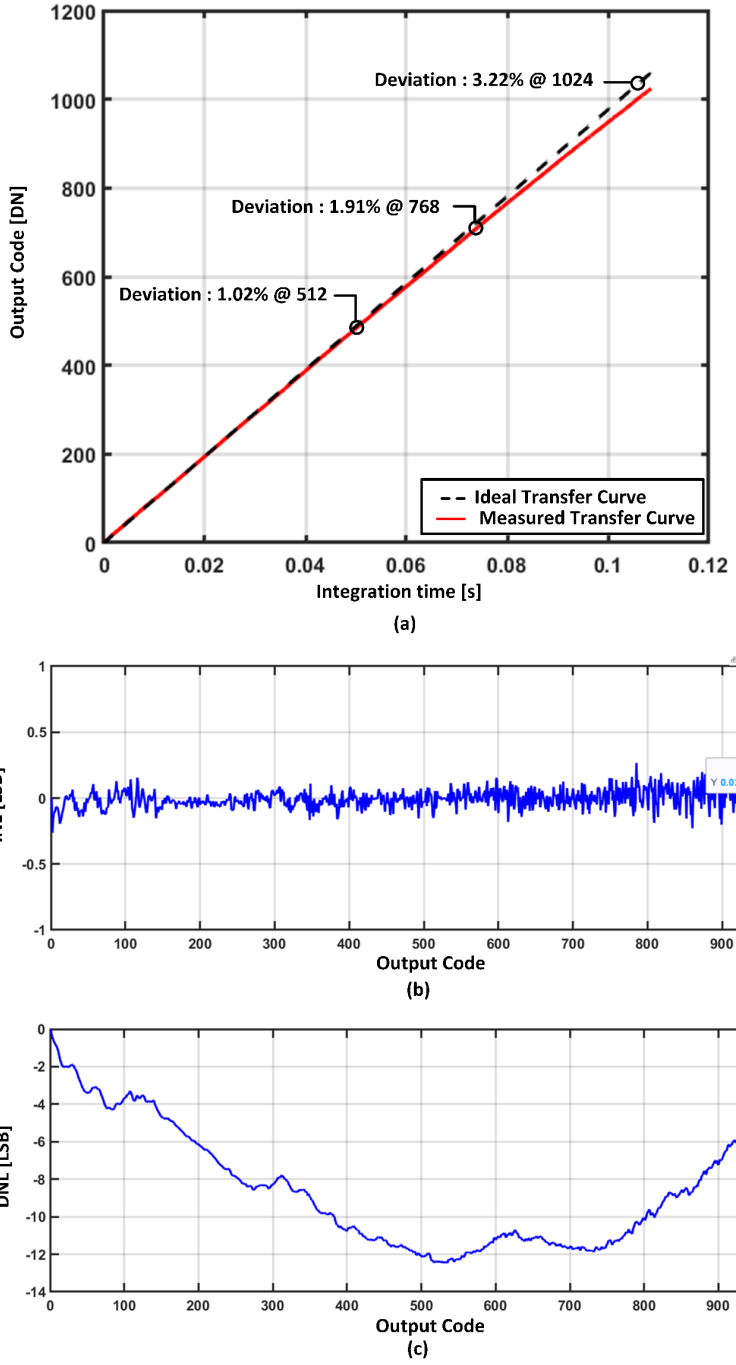


Figure 7.15: (a) Measured and ideal PTC curve, (b) DNL performance and (c) INL performance

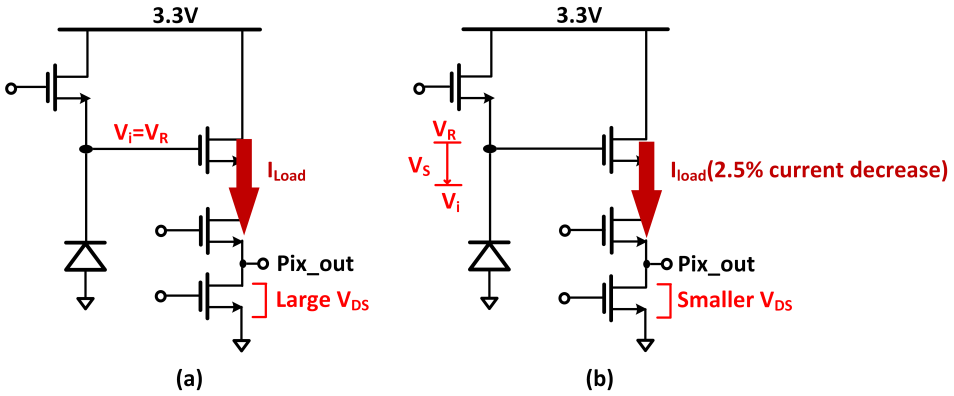


Figure 7.16: (a) Current inside the pixel at reset state and (b) Current during read state

lower during the reset and read periods, respectively. During the reset period, the input signal to the first source follower, Vi, equals the reset level V_R, which is transmitted to the sampling capacitor V_S via the source follower . Since the reset level represents the pixel's most positive output, the drain-source voltage across the current source is relatively large, producing a correspondingly large current. In the read period, the input signal is expressed as:

$$V_i = V_R - V_S \tag{7.4}$$

Here, V_S corresponds to the signal proportional to the integrated charge. As V_S increases, the source follower's output decreases, reducing the drain-source voltage across the current source and consequently decreasing the current. This variation arises from the limited output impedance of the single-transistor current source. Due to pixel area constraints, improving the current source's output impedance is challenging, resulting in these nonlinear effects.

These findings suggest that the source follower's nonlinearity significantly impacts the linearity of the readout chain, particularly at higher signal levels. Improving the output impedance of the current source or optimizing the pixel design could substantially enhance linearity performance and overall sensor reliability.

7.2.5. PERFORMANCE COMPARISON

As discussed in Section 7.2, the image sensor developed in this work achieves robust noise performance, including VFPN and temporal noise, while maintaining an impressive frame rate of 2500fps.

Table 7.2 presents a performance comparison among image sensors employing SAR ADC architectures, focusing on both noise characteristics and frame rate performance. Notably, the pixel rate per column is introduced as an additional metric for a fairer comparison among architectures with different column-to-ADC ratios. Although ADC sampling rate is often regarded as a dominant performance indicator, it can be misleading

Year	2023	2018	2012	2015	2015	2012	2013
Ref	This work	[1]	[2]	[3]	[4]	[5]	[6]
Technology	180nm P4M	90nm 1P5M	180nm 1P6M	180nm P4M	180nm P4M	130nm 2P4M	130nm 2P4M
Pixel Array	316×110	1920×1440	920×256	256×128	15488×877	1600×1200	1720×832
Pixel Type	3T	4T	4T	4T	4T	3T	3T
Frame Rate	2500fps	50fps	9fps	90fps	60fps	150fps	17fps
Column-to-ADC Ratio	1:1	16:1	4:1	1:1	32:1	2:1	1720:1
ADC Type	SAR	SAR	SAR	N5-SAR	Cyclic	SAR	Pipeline SAR
ADC Resolution	10	10	9	12	12	10	12
ADC Sampling Rate	0.25MS/s	12MS/s	0.033MS/s	0.12MS/s	17.95MS/s	0.58MS/s	26.7MS/s
Pixel Rate per Column	0.25Mpixels/s	0.75Mpixels/s	8.25Mpixels/s	30Mpixels/s	1.5Mpixels/s	0.29Mpixels/s	15.5Mpixels/s
Temporal Noise (RMS Value)	560μV (@1×)	273.6μV (@1×)	5300μV	527μV	614.4μV (@1×)	2.15LSB	187.5μV (@1×)
VFPN	0.034%	0.23%	0.50%	0.004%	0.049%	-	-
ADC Saturation Level	0.65V	0.7V	0.26V	0.684V	0.8V	-	0.358V
Dynamic Range	61.2dB	66.5dB	73dB	68.1dB	62.3dB	52dB	65.6dB
DNL	+0.36/-0.28LSB	+0.77/-0.54LSB	+1.21/-2.15LSB	+1.37/-1.69LSB	+6/-1LSB	-	-
INL	+0.15/-12.46LSB	+0.81/-0.54LSB	+4.5/-4.15LSB	+3.55/-1.42LSB	-	-	-

Table 7.2: Performance comparison of image sensors using SAR ADCs

without considering system-level parameters such as pixel resolution and column-to-ADC ratios. The pixel rate per column more accurately reflects the actual throughput of each column, providing a balanced view of readout efficiency.

This work achieves a frame rate of 2500fps using 180nm process technology while maintaining superior VFPN and temporal noise characteristics compared to other image sensors employing SAR ADCs. For example, [1] utilizes a 90nm process and achieves an ADC sampling rate of 12MS/s—48 times faster than the 250kS/s used in this work. However, since [1] shares one ADC across 16 columns, the actual pixel rate per column is only about three times higher. Moreover, its VFPN is 0.23%, significantly worse than the 0.034% achieved in this work.

Notably, [3] and [5] demonstrate excellent VFPN performance due to the use of digital double sampling (DDS) techniques. However, [3] exhibits an extremely low pixel rate per column, approximately 30kPixel/s, which limits its suitability for high-speed applications. In addition, although [5] achieves a twofold improvement in pixel rate per column, it benefits from 130nm process technology, which inherently offers more favorable conditions for designing high-speed SAR ADCs than the 180nm process used in this work.

The temporal noise performance achieved here is also competitive. Despite using 3T pixels—which typically yield worse noise characteristics than 4T designs—this sensor outperforms most prior works, except [1] and [3], which utilize noise-shaping techniques to suppress temporal noise. Furthermore, many sensors in Table 7.2 do not use a fully column-parallel ADC structure, resulting in higher bandwidth requirements for each readout path. The sensor architecture issue regarding the number of ADC leads to degraded temporal noise performance, underscoring the advantages of the proposed column-parallel design.

Table 7.3 compares the performance of this work with image sensors that achieve incredibly high frame rates by enhancing the pixel rate per column. In particular, [7] and [8] demonstrate higher column-level throughput than this design. For instance, [7] employs a single-slope ADC architecture in a 90nm process, where the global DAC operates at 1.3GS/s to generate the ramp signal, achieving a frame rate of 480fps. Similarly, [8] uses two ADCs per column to read two rows simultaneously and a 70-channel LVDS interface to address data bandwidth limitations, enabling a frame rate of 1000fps. Both

Year	2023	2016	2013	2018	2015
Ref	This work	[7]	[8]	[9]	[10]
Technology	180nm 1P4M	90nm 1P5M 65nm 1P9M	180nm	90nm 1P4M 65nm 1P7M	90nm 1P5M 65nm 1P5M
Pixel Array	316×110	4624×2296	2240×2240	1632×896	7936×4412
Pixel Type	3T	5T	4T	4T	4T
Frame Rate	2500fps	480fps	1000fps	660fps	120fps
Column-to-ADC Ratio	1:1	1:1	1:2	1:1632	1:1
ADC Type	SAR	Single-Slope	Sigma-Delta	Single-Slope	Cyclic
ADC Resolution	10	14	14	14	14
ADC Sampling Rate	0.25MS/s	1.1MS/s	1.115MS/s	0.665MS/s	0.26MS/s
Pixel Rate per Column	0.25Mpixels/s	1.1Mpixels/s	2.22Mpixels/s	1.07Mpixels/s	0.26Mpixels/s
Temporal Noise (RMS Value)	$12e^-$	$3.3e^-$	$5e^-$	$5.15e^-$	$5.2e^-$
VFPN	0.034%	0.05LSB	-	-	-
ADC Saturation Level	0.65V	0.922V	-	-	0.93V
Dynamic Range	61.2dB	76.34dB	72dB	70.2dB	69dB
DNL	+0.36/-0.28LSB	-	-	-	+0.95LSB/-0.85LSB
INL	+0.15/-12.46LSB	0.18%	-	-	+2.57/-28.27LSB

Table 7.3: Performance comparison of high-speed image sensors

sensors also achieve superior temporal noise performance, mainly due to using single-slope and sigma-delta ADCs, which inherently offer narrower noise bandwidths than SAR ADCs.

In addition, [9] adopts a pixel-parallel ADC architecture, assigning one ADC to every pixel. This configuration maximizes the pixel rate per column and significantly enhances noise performance by minimizing bandwidth requirements at the readout stage. While this approach offers outstanding bandwidth and noise performance, it requires significantly large area, limiting scalability in high-resolution sensors.

Although the designs in Table 7.3 surpass this work in specific metrics such as temporal noise or resolution, the architecture presented here exhibits strong potential for further improvement due to its simplicity, scalability, and efficiency. First, the current system operates with a modest 64MHz clock—20 times slower than the 1.3GHz clock used in [7]—highlighting the headroom available for scaling ADC speed using advanced process technologies such as 65nm. Second, expanding the number of LVDS channels could help mitigate output bottlenecks and enable higher frame rates. Lastly, adopting 4T pixels instead of 3T pixels could dramatically reduce temporal noise, which is currently dominated (30%) by pixel and source follower noise. A 4T pixel structure would isolate the floating diffusion node and allow correlated double sampling to suppress pixel-level noise more effectively.

Overall, the comparisons in Tables 7.2 and 7.3 underscore the scalability of the proposed SAR ADC-based architecture. While further optimization is possible in areas such as frame rate, VFPN and temporal noise, this work demonstrates a well-balanced trade-off between frame rate, noise performance, and power efficiency, providing a compelling foundation for scalable, high-performance image sensor design in future applications, such as machine vision and high-speed industrial inspection.

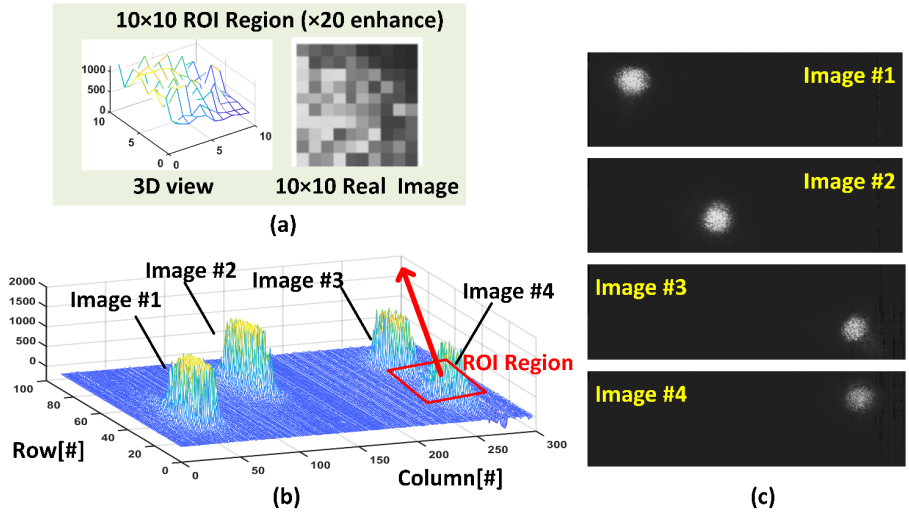


Figure 7.17: (a) Image captured from ROI region near moving object, (b) 3D view of captured Images in normal mode and (c) objects captured at different locations

7.3. EVALUATION OF RECONFIGURABLE SYSTEM

7.3.1. ZOOM-IN MODE CONTROL

To evaluate the performance of the reconfigurable system, a laser with a wavelength of approximately 400nm is used to create a moving object within the dark chamber described in Section 7.1.1. The laser with a short wavelength provides sufficient intensity, even under the short exposure times required for the image sensor's zoom-in mode operation. Following the experimental setup outlined in Chapter 5, the moving object is captured within a consistent background to ensure controlled testing conditions. The laser-generated moving object is tracked using the image sensor, with the reconfigurable system dynamically optimizing the tracking process. The sensor's horizontal line time is set to 64μs for this evaluation.

Figure 7.17 presents the tracking results of the moving object using the reconfigurable system. Figure 7.17(c) shows four captured images at distinct object locations in normal mode, which are merged into a 3D view, as illustrated in Figure 7.17(b). Even after merging these four images, the background remains entirely dark, with changes in the image confined solely to the moving object. This consistency confirms that only the object's information requires updating, validating the reconfigurable system's effectiveness in isolating and tracking moving objects, as discussed in Chapter 5.

Figure 7.17(a) depicts the image captured from the ROI region near the object in image #4. Due to the short exposure time during zoom-in mode, the brightness of the 10×10 image is enhanced by a factor of 20 through post-processing. The ROI region is determined using the algorithm detailed in Section 6.3.1. Figure 7.18(a) and 7.18(b) illustrate the real-time image analysis results, which dynamically adjust the VDA and HDA during image reading. These graphs represent the real-time image analysis results correspond-

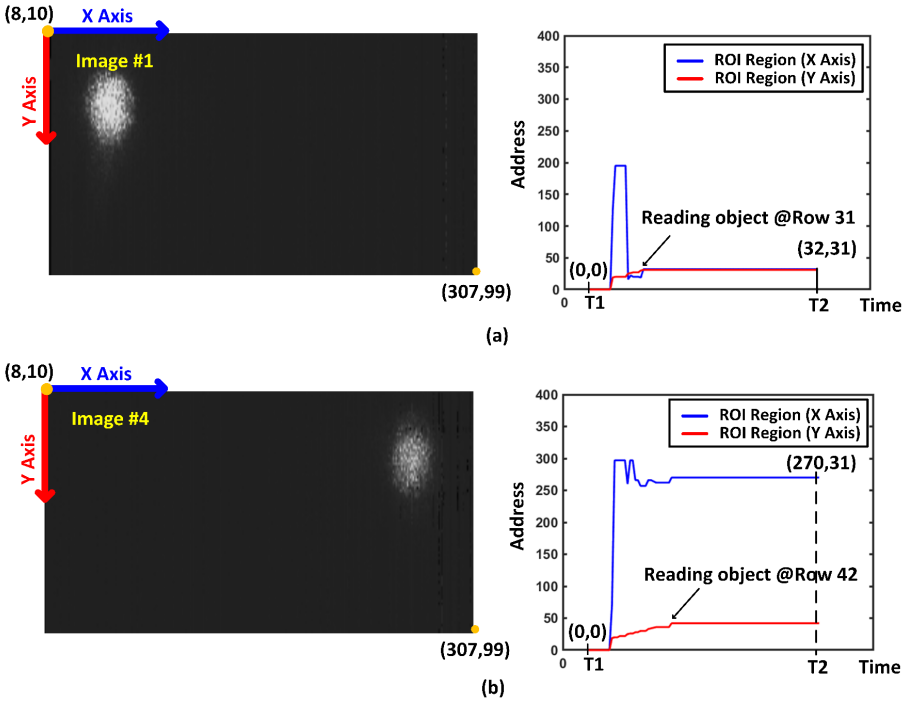


Figure 7.18: VDA and HDA changes during real time image analysis for (a) image #1 and (b) image #4

ing to images #1 and #4 in Figure 7.17(c). The horizontal axis corresponds to the time domain, while the vertical axis represents the VDA and HDA addresses.

Figures 7.18(a) and (b) show that the image sensor starts reading the pixel array at T1 and finishes at T2, processing pixels from row 10 to row 99. At T1, both cases initialize the VDA and HDA to (0,0). Once the sensor reads the rows containing the object, the VDA and HDA adjust to the correct location. After completing the readout process at T2, the VDA and HDA are used to send feedback information to the image sensor. This feedback sets the ROI region during zoom-in mode. In Figure 7.18(a), the final VDA and HDA feedback values are updated to [32, 31]. In contrast, in Figure 7.18(b), they are updated to [270, 42], ensuring accurate alignment of the ROI region with the object's location.

These measurement results demonstrate that the real-time image analysis is working correctly. The feedback information is sent to the image sensor on time, and the ROI region is properly set near the object.

7.3.2. IMAGE QUALITY ANALYSIS AND CHALLENGES IN THE ROI REGION

The image quality in the ROI region during zoom-in mode is evaluated, focusing on FPN and temporal noise performance. Measurements are conducted using the same methods outlined in Sections 7.2.2 and 7.2.3, enabling a direct comparison with the image quality achieved in normal mode.

In normal mode, the image quality metrics in the ROI region align with the results

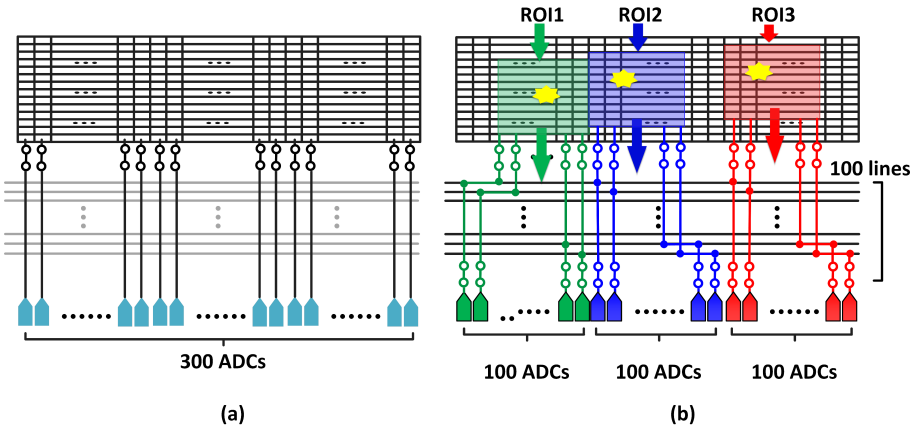


Figure 7.19: (a) Pixel and ADC connection in normal mode for proper FPN calibration and (b) pixel and ADC connection during zoom-in mode

presented in Section 7.2. VFPN and HFPN are measured at 0.34LSB and 0.24LSB, respectively, while the temporal noise achieves an RMS value of 560μV. However, in zoom-in mode, noticeable image quality degradation occurs. The VFPN and HFPN increase significantly to 7.8LSB and 7.6LSB, respectively, while the RMS value of the temporal noise rises to approximately 19mV. Several factors contribute to this image quality degradation.

First, signal crosstalk inside the pixel array and intelligent switch box worsens the noise performance. As discussed in Section 6.1, the 10-pixel output lines within the pixel array and the 100 horizontal lines connecting the ADC to the pixels in the intelligent switch box introduce mutual interference. This interference worsens both temporal noise and FPN, leading to degraded performance in the zoom-in mode.

Second, the FPN calibration using optical black (OB) pixels becomes less effective during zoom-in mode operation. Figure 7.19(a) illustrates the scenario where the FPN calibration operates effectively in normal mode. As described in Section 4.3.3.2, FPN originates from errors in both the pixel and the ADC. Effective calibration requires the ADC to read pixels located strictly within the same column, as shown in Figure 7.19(a). However, in zoom-in mode, the reconfigurable system allows the ADC to read pixels from different columns, as illustrated in Figure 7.19(b). Since the ROI region can dynamically span any row and column, the pixel-ADC combination changes, causing the FPN calibration process to fail in correcting pixel errors. As a result, while errors originating from the ADC can still be partially calibrated, the residual pixel errors remain uncorrected, leading to increased VFPN and HFPN.

In summary, image quality degradation in zoom-in mode is primarily caused by crosstalk between pixel output lines and ineffective FPN calibration due to dynamic pixel-ADC combinations.

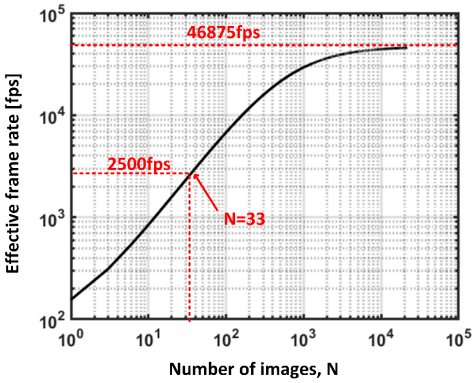


Figure 7.20: Effective frame rate calculation

7.3.3. FRAME RATE LIMITATIONS IN THE RECONFIGURABLE SYSTEM

As previously discussed, the horizontal line time is set to 64μs, resulting in a frame rate of 156fps during normal mode operation. The reconfigurable system supports zoom-in mode and normal mode, and the effective frame rate depends on the number of images generated from zoom-in mode. The effective frame rate, $F_{\text{FR\_EFF}}$, is calculated using the following equation:

$$F_{\text{FR\_EFF}} \leq \frac{1+3N}{\frac{P_{\text{ROW}}}{F_{\text{ADC}}} + \frac{N}{F_{\text{ADC}}}} \tag{7.5}$$

Here, P_{ROW} denotes the number of pixel rows in one full-frame read, F_{ADC} is the per-column ADC conversion rate (samples/s), and N is the number of ROI images generated during zoom-in mode between two normal frames. Figure 7.20 illustrates the effective frame rate computed from this equation: the horizontal axis is N and the vertical axis is $F_{\text{FR\_EFF}}$. When $N = 0$ (normal mode only), the effective frame rate is about 156 fps. As N increases, $F_{\text{FR\_EFF}}$ increases monotonically (e.g., ≈2 500 fps at $N = 33$). In the theoretical limit $N \to \infty$, the denominator is dominated by N/F_{ADC}, and thus $F_{\text{FR\_EFF}} \to 3F_{\text{ADC}}$; with our setup ($F_{\text{ADC}}$ = 15.625 kS/s), this converges to 3 × 15,625 = 46,875 fps (≈ 46.9 kfps). There are no circuit-level constraints that prevent handling additional ROI images under this operating condition.

The reconfigurable system enables dynamic adjustments to the number of images generated in zoom-in mode, offering precise control over the effective frame rate while maintaining operational stability.

In addition to the effective frame rate analysis, Figure 7.21 illustrates the measured power consumption at various frame rates, as detailed in Table 7.1. At an effective frame rate of 156fps, the power consumption is approximately 33mW and remains constant as the effective frame rate increases, reaching 2500fps while consuming the same 33mW. This consistency occurs because the ADC sampling rate does not change, even as the number of images (N) generated in zoom-in mode increases.

The 1.8V power rail, primarily consumed by the ADC, draws approximately 3.6mW at

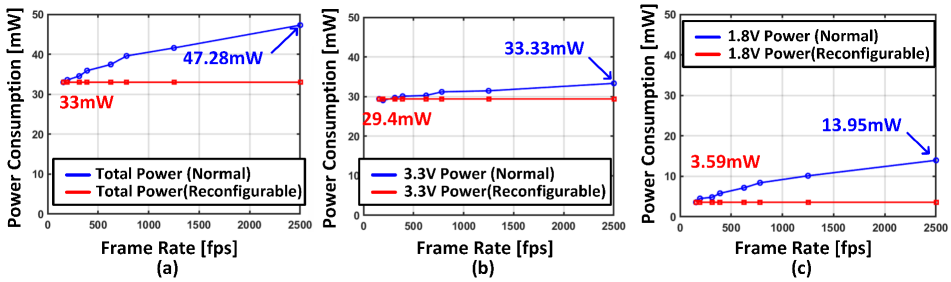


Figure 7.21: Power consumption comparison at different frame rates

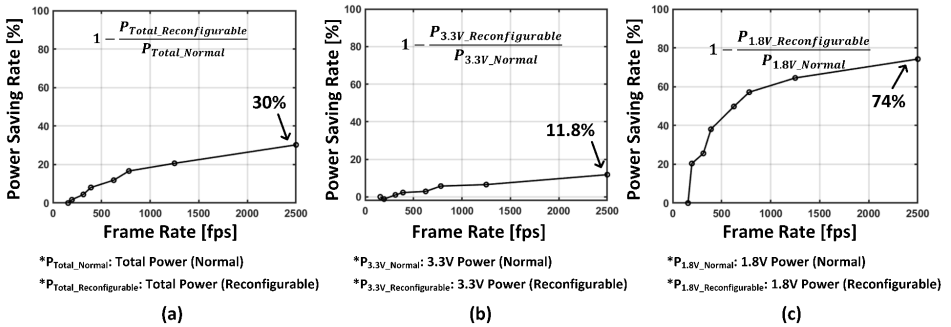


Figure 7.22: Power consumption savings compared to normal mode operation

156fps and remains unchanged at 2500fps. Compared to normal mode operation, where the 1.8V power consumption is approximately 13.95mW, the reconfigurable system operation achieves substantial power savings. Similarly, the 3.3V power rail consumes about 4mW less power than in conventional operation at 2500fps. Unlike normal mode operation, the horizontal line time does not decrease as the effective frame rate increases, resulting in consistent ADC operation across frame rates.

Figure 7.22 quantifies the power savings achieved at various frame rates. At 156fps, the power consumption of the reconfigurable system operation matches normal mode operation due to the minimal number of images generated from zoom-in mode. As the number of images generated from zoom-in mode increases, the effective frame rate rises, leading to considerable power savings. At 2500fps, the total power consumption decreases by approximately 30% compared to normal mode operation. Notably, the ADC operation achieves a significant reduction, with the 1.8V power rail showing savings of roughly 74%.

In summary, the reconfigurable system dynamically controls the effective frame rate through zoom-in mode by adjusting the number of generated images. This functionality not only enables a substantial increase in effective frame rate but also demonstrates remarkable power efficiency, particularly in ADC-related operations. These findings em-

phasize the versatility and energy-efficient performance of the reconfigurable system in high-speed imaging applications.

7.4. SUMMARY

This chapter presents the measurement results and design analysis of the proposed image sensor system. It focuses on enhancing the frame rate by increasing readout speed and implementing a reconfigurable system. A detailed measurement setup is described to ensure a uniform and accurate evaluation, implemented using an FPGA-based platform under controlled conditions.

The image sensor confirms that the horizontal line time can be set to 4μs, supporting a maximum ADC operation rate of 250kS/s. While the readout speed increases, image quality is maintained, with VFPN measured at approximately 0.34LSB and σ_{Total} = 560 μV (@×1). Design analysis based on these measurements is discussed in detail.

In the reconfigurable system, it is verified that the effective frame rate can increase by generating additional images from the zoom-in mode. The image analysis algorithm efficiently identifies and tracks the object in real time. However, challenges such as signal crosstalk and limitations in FPN calibration during zoom-in mode are noted as areas for improvement.

Significant power savings are achieved during zoom-in mode operation. At an effective frame rate of 2500fps, the 1.8V power rail, primarily consumed by the ADC, reduces power consumption by approximately 74%. In contrast, the 3.3V power rail achieves savings of around 4mW compared to normal mode operation. The consistent horizontal line time during zoom-in mode ensures stable ADC operation across frame rates.

Finally, comparing image sensors utilizing SAR ADCs highlights that this design achieves better overall performance. While frame rate enhancement is constrained by process technology, the reconfigurable system demonstrates that the image sensor can still achieve significant improvements through system-level enhancements. The reconfigurable system showcases its potential for enabling high-speed, energy-efficient image processing while identifying opportunities for further optimization, such as minimizing crosstalk and refining calibration algorithms.

REFERENCES

[1] S. Hwang et al., "A 2.7-m pixels 64-mw cmos image sensor with multicolumn-parallel noise-shaping sar adcs," *IEEE Transactions on Electron Devices*, vol. 65, no. 3, pp. 1119–1126, 2018. DOI: 10.1109/TED.2018.2795005.

[2] D. Chen et al., "A 64 fj/step 9-bit sar adc array with forward error correction and mixed-signal cds for cmos image sensors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 11, pp. 3085–3093, 2014. DOI: 10.1109/TCSI.2014.2334852.

[3] M. Kim et al., "An area-efficient and low-power 12-b sar/single-slope adc without calibration method for cmos image sensors," *IEEE Transactions on Electron Devices*, vol. 63, no. 9, pp. 3599–3604, Sep. 2016. DOI: 10.1109/TED.2016.2587721.

[4] R. Funatsu et al., "6.2 133mpixel 60fps cmos image sensor with 32-column shared high-speed column-parallel sar adcs," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2015, pp. 1–3. DOI: 10.1109/ISSCC.2015.7062951.

[5] M. Shin et al., "A 1.92-megapixel cmos image sensor with column-parallel low-power and area-efficient sa-adcs," *IEEE Transactions on Electron Devices*, vol. 59, no. 6, pp. 1693–1700, Jun. 2012. DOI: 10.1109/TED.2012.2190936.

[6] J. Deguchi et al., "A 187.5μvrms-read-noise 51mw 1.4mpixel cmos image sensor with pmoscap column cds and 10b self-differential offset-cancelled pipeline sar-adc," in *2013 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2013, pp. 494–495. DOI: 10.1109/ISSCC.2013.6487830.

[7] Y. Oike et al., "An 8.3m-pixel 480fps global-shutter cmos image sensor with gain-adaptive column adcs and 2-on-1 stacked device structure," in *2016 IEEE Symposium on VLSI Circuits*, Honolulu, HI, USA, 2016, pp. 1–2. DOI: 10.1109/VLSIC.2016.7573543.

[8] J. Cremers et al., "A 5 megapixel, 1000fps cmos image sensor with high dynamic range and 14-bit a/d converters," in *2013 International Image Sensor Workshop (IISW)*, Snowbird, UT, USA, 2013, pp. 309–312.

[9] M. Sakakibara et al., "A back-illuminated global-shutter cmos image sensor with pixel-parallel 14b subthreshold adc," in *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, USA, 2018, pp. 80–82. DOI: 10.1109/ISSCC.2018.8310193.

[10] T. Yasue et al., "A 14-bit, 33-mpixel, 120-fps image sensor with dmos capacitors in 90-nm/65-nm cmos," in *2015 International Image Sensor Workshop (IISW)*, Vaals, Netherlands, 2015, pp. 174–177.

8

Conclusion and Future Work

This thesis enhances the image sensor frame rate through two complementary strategies. The first improves the analog front-end (AFE) performance—particularly the SAR ADC—to increase pixel rate, thereby boosting the frame rate while achieving a better noise performance and a high linearity. In addition, a detailed analysis of the readout circuits' noise characteristics, including fixed-pattern and temporal noise, has been conducted. The second strategy introduces a reconfigurable system that dynamically switches the sensor operation from normal to zoom-in mode based on regions of interest (ROI). This system-level approach significantly improves the effective frame rate by reducing the data load and energy consumption without increasing the ADC speed. Together, these methods address the limitations of conventional image sensors and demonstrate a scalable, application-oriented framework for high-speed, energy-efficient imaging.

This chapter summarizes the main contributions in Section 8.1 and outlines potential directions for future improvement in Section 8.2.

8.1. CONCLUSION

This work advances the performance of image sensors by focusing on two complementary approaches: enhancing the readout speed and optimizing the system operation for application-specific use cases. A critical priority is maintaining robust image quality, even as the frame rate increases. By developing a column-parallel SAR ADC and implementing a reconfigurable system, this work effectively addresses these challenges, providing a foundation for high-speed, energy-efficient imaging systems.

8.1.1. FRAME RATE LIMITATION

This thesis presents significant advancements in improving the frame rate of image sensors through circuit- and system-level innovations. A column-parallel SAR ADC structure was employed at the circuit level to enhance the readout speed while optimizing the signal bandwidth and the power consumption. The two-step SAR ADC, comprising a 6-bit core and a residue-generating PGA, enables a compact layout within the narrow pixel column pitch. This design improves the capacitor DAC linearity by reducing the control line complexity. As a result, the image sensor achieves the excellent DNL performance of $+0.36/-0.28$LSB and supports a sampling rate of 250kS/s, even in a 180nm CMOS technology.

Nevertheless, as discussed in Section 7.2.1, the readout architecture faces limitations due to the speed constraints of the data interface, primarily dictated by the 180nm process technology. For example, with a horizontal line time of 4μs, the required data rate at the 12-channel LVDS interface is 1.536Gb/s. If the horizontal line time decreases further, the data rate will exceed 1.536Gb/s, which the 180nm technology cannot support. Consequently, the horizontal line time cannot be reduced below 4μs, limiting the readout speed compared to other high-speed image sensors, as shown in Table 7.3. Furthermore, as the pixel resolution increases, the demands on pixel readout speed and interface data rate will rise, necessitating further advancements.

To address these limitations, this thesis proposes a reconfigurable system optimized for application-specific efficiency. The system operates in two modes:

1. **Normal Mode:** Reads the entire pixel array for standard imaging tasks.
2. **Zoom-In Mode:** Focuses exclusively on a 10×10 window surrounding the moving object, reducing the data burden and improving efficiency.

Transitioning between modes is achieved through real-time image analysis in the FPGA, which determines the ROI coordinates (VDA and HDA). During the zoom-in operation, the image sensor can read three or more ROI images per horizontal line time, leveraging a switch network and 10-pixel output lines per column for efficient data transfer.

This reconfigurable approach delivers an effective frame rate of 46,875fps, offering three distinct advantages:

- **Data volume reduction:** ROI readout minimizes unnecessary pixel data.
- **No need for ADC sampling rate improvement:** Effective frame rate improves without raising the sampling frequency.

- **Energy efficiency:** ADC power consumption drops by 74% when the effective frame rate increases 16-fold.

This research suggests the optimal frame rate strategy should align with application-specific requirements. For video applications with dynamic changes in every frame, enhancing readout circuit speed is appropriate, and the SAR ADC design offers significant potential for further improvement. Conversely, application-dedicated image sensors like the proposed reconfigurable system provide an efficient solution for specific tasks such as tracking moving objects. This work highlights how an image sensor can achieve high-speed, energy-efficient performance tailored to specific applications.

8.1.2. IMAGE QUALITY MANAGEMENT

This work's central objective is maintaining image quality while increasing the frame rate. Two primary noise sources—fixed-pattern noise (FPN) and temporal noise—have been addressed through a targeted circuit design and calibration strategies.

To mitigate FPN, two calibration methods were implemented:

1. **Background ADC offset calibration using memory:** Reduces only ADC-induced offsets through a background operation (Section 4.3.1.1). It effectively suppresses vertical FPN (VFPN) caused by the ADC mismatch.

2. **FPN calibration using optical black (OB) pixels:** Removes both pixel- and ADC-related offsets by averaging OB pixel data and subtracting it at the FPGA level before the active pixel readout (Section 4.3.1.2). It enables frame-by-frame correction without additional latency.

Both methods demonstrate strong performance, keeping the VFPN below 0.4LSB. In this work, OB pixel calibration is primarily used, since the two-step SAR ADC architecture cannot support the 0.25LSB precision required for memory-based calibration. However, in zoom-in mode, the dynamic pairing between pixels and ADCs—determined by the ROI—can limit the effectiveness of the OB pixel calibration. Enhancing the algorithm to address this mismatch is proposed as a direction for future research.

Regarding temporal noise, the proposed system performs well even with a 3T pixel architecture. The column-parallel SAR ADC helps reduce the signal bandwidth, achieving approximately 560μV RMS noise at a 4μs horizontal line time and below 450μV when the line time is doubled. As summarized in Table 7.2, this outperforms prior designs, including those with 4T pixels lacking noise-shaping.

Furthermore, the reconfigurable system maintains stable temporal noise levels even as the frame rate increases. Since the ADC sampling rate remains fixed, the signal bandwidth does not scale with speed, preventing noise degradation under high-speed conditions. This robustness demonstrates the effectiveness and scalability of the proposed design in both image quality and system performance.

8.2. FUTURE WORK

This section outlines future work in two key areas: improving readout circuits, and advancing system control, to overcome current limitations and extend the capabilities of image sensor systems.

8.2.1. READOUT CIRCUIT IMPROVEMENT

The readout circuit developed in this study presents significant potential for further performance enhancement, mainly through process technology scaling and area optimization.

First, adopting advanced process technologies is expected to improve speed and power efficiency. This work was implemented in a 180nm CMOS process with supply voltages of 3.3V and 1.8V. Migrating to finer technologies, such as 65nm or 40nm, and lowering supply voltages (e.g., to 2.8V or 1.2V), would enable a faster SAR ADC operation due to improved digital circuit performance while reducing overall power consumption. However, such scaling introduces challenges in the analog design—especially in components like the programmable gain amplifier (PGA). At lower supply voltages, it becomes difficult to maintain sufficient output swing due to headroom limitations. For example, a 1.2V supply can restrict the performance of single-ended amplifiers. To mitigate this, inverter-based amplifier topologies, as demonstrated in [1], can be employed to maintain ADC saturation levels and ensure robust pixel readout.

Second, area optimization is essential for enabling higher-resolution image sensors. In this work, the capacitor DAC is a major contributor to the total area, occupying nearly 60% of the 21,000μm^2 per-channel footprint. Approximately 3.2 pF of capacitance is used per channel, split between the PGA and ADC. Reducing capacitor size can substantially reduce area; however, this must be balanced against increased thermal noise as discussed in Chapter 4.

Noise-shaping techniques are recommended to address this trade-off [2], [3], [4]. These allow smaller sampling capacitors (CS) to be used while maintaining noise performance by spreading the quantization noise over frequency and applying oversampling. In particular, the sampled noise power $(N_{\text{SAMP}})^2$ is inversely proportional to the oversampling ratio (OSR), following the relation:

$$N_{\text{SAMP}}^2 = \frac{kT}{C_S \times \text{OSR}} \tag{8.1}$$

Here, k is Boltzmann's constant and T is the absolute temperature. Figure 8.1. The estimated RMS noise vs. sampling capacitance for various oversampling ratios. As illustrated, a sampling capacitor as small as 100fF, combined with more than 20 multiple sampling steps, can achieve RMS noise performance equivalent to that of a 1pF capacitor.

This approach offers a scalable design strategy for next-generation image sensors by achieving a compact layout and robust readout quality.

8.2.2. SYSTEM CONTROL ENHANCEMENT

The reconfigurable system developed in this work has demonstrated an effective region-based operation by switching between normal and zoom-in modes. To further enhance the system's adaptability and tracking performance, two areas of improvement are proposed: enabling ROI-compatible FPN calibration and implementing intelligent ROI control.

First, to enable FPN calibration within the ROI region, adopting a digital double-sampling (DDS) technique is recommended to enhance the mitigation of vertical fixed-

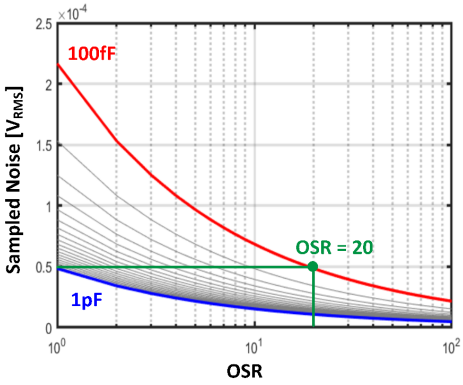


Figure 8.1: Noise reduction through oversampling with small sampling capacitors: comparison of RMS noise performance for CS = 1pF and CS = 100fF under multiple sampling steps

pattern noise (VFPN) [5]. Current FPN calibration methods are constrained by the requirement that the pixel and ADC reside in the same column, a condition often unmet during the zoom-in mode operation of the reconfigurable system. Consequently, calibration is restricted to VFPN originating solely from the ADC. By employing DDS, reset and signal levels can be sampled independently within a single horizontal line period, eliminating the dependency on pixel-ADC alignment. This enhancement is anticipated to significantly improve calibration precision, addressing the inherent architectural limitations of the reconfigurable system.

Second, leveraging advanced control algorithms offers an opportunity to further enhance system adaptability and performance. Machine learning techniques, such as predictive models, can anticipate object trajectories based on prior frames, reducing the computational overhead of real-time analysis while improving the accuracy of ROI adjustments. For example, predictive tracking algorithms could pre-emptively modify the ROI based on object motion patterns, ensuring seamless tracking even under erratic or high-speed movement. Additionally, implementing hierarchical control strategies, where multiple layers of analysis operate simultaneously—such as global scene evaluation paired with local detail tracking—can significantly enhance responsiveness and data handling efficiency. This layered approach would allow the system to dynamically allocate resources based on workload demands and operational conditions, making it highly adaptable across diverse use cases.

These improvements support the development of reconfigurable imaging architectures with enhanced adaptability, speed, and power efficiency for real-time, data-efficient machine vision applications.

8.3. SUMMARY

This chapter summarized the dual strategies—SAR ADC-based high-speed readout and ROI-enabled reconfigurable operation—and outlined future enhancements in circuit and system-level designs.

The proposed architecture demonstrated strong noise performance and robust ROI tracking, validated through measurements. These results confirm the effectiveness of combining circuit-level and system-level strategies for advanced image sensor design.

Future work focuses on two directions:

1. Enhancing readout circuit performance through process scaling and area-efficient design using noise-shaping techniques.

2. Improving system control by introducing ROI-compatible FPN calibration with DDS and adaptive ROI tracking using machine learning.

These directions will extend the flexibility, precision, and efficiency of future reconfigurable image sensor systems.

REFERENCES

[1] X. Tang et al., "An energy-efficient comparator with dynamic floating inverter amplifier," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 4, pp. 1011–1022, Apr. 2020. DOI: 10.1109/JSSC.2019.2960485.

[2] Y. Chae et al., "A 2.1 m pixels, 120 frame/s cmos image sensor with column-parallel delta-sigma adc architecture," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 236–247, Jan. 2011. DOI: 10.1109/JSSC.2010.2085910.

[3] N. Chen et al., "A low-noise cmos image sensor with digital correlated multiple sampling," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 1, pp. 84–94, Jan. 2018. DOI: 10.1109/TCSI.2017.2724855.

[4] M. Kim et al., "An area-efficient and low-power 12-b sar/single-slope adc without calibration method for cmos image sensors," *IEEE Transactions on Electron Devices*, vol. 63, no. 9, pp. 3599–3604, Sep. 2016. DOI: 10.1109/TED.2016.2587721.

[5] Y. Nitta et al., "High-speed digital double sampling with analog cds on column parallel adc architecture for low-noise active pixel sensor," in *2006 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2006, pp. 2024–2031. DOI: 10.1109/ISSCC.2006.1696261.

ACKNOWLEDGEMENTS

My Ph.D. journey has been, in many ways, a life of continuous challenge. When I decided to pursue a Ph.D. outside Korea, I believed that stepping beyond my familiar environment would allow me to explore more creative ideas and find joy in discovering and learning new things—even if I were doing similar work. However, starting a Ph.D. at the age of 32 raised concerns for many around me. Leaving behind a stable position at a reputable company, the decision felt like a risky gamble. And yet, as Albert Einstein is often quoted, "Insanity is doing the same thing over and over again and expecting different results." I believed that if I wanted a different life, I needed to choose a different path and take on new challenges. Fortunately, I had the opportunity to study at TU Delft, where I was able to learn deeply and work with joy and passion. This journey would not have been possible through my efforts alone. It was the support, guidance, and generosity of many people that allowed me to reach this point.

I would like to begin by expressing my sincere gratitude to my supervisor, **Prof. Albert Theuwissen**. Your guidance taught me how to plan, conduct, and evaluate research, which was instrumental in completing this Ph.D. successfully. Beyond the technical aspects, your respectful and composed way of dealing with people left a strong impression on me. Coming from a fast-paced and often sharp-tongued culture in Korea, your example helped me reflect, mature, and grow not only as a researcher but also as a person. I would also like to thank **Zu Yao Chang**, **Lukasz Pakula**, and **Ron van Puffelen**. Your support in setting up experiments and handling lab equipment was essential, especially during the times I was working alone and felt uncertain. Your help made my research process smoother and more manageable.

To my research group colleagues, thank you for making this journey fulfilling and enjoyable. **Accel Abarca**, you were like a big brother when I first joined the lab. You helped me adapt quickly to research and daily life, and I'm glad we've stayed in touch even after your graduation. **Amirhossein Jouyaeian**, **Arthur Campos de Oliveira**, **Roger Zamparette**, and **Jae-Sung Ahn**, your friendship, especially through football and casual conversations, helped me relax and feel at home in a foreign environment. In the early days, when I struggled with English, these moments were invaluable. **Eunchul Kang**, though our time together was short, your help during my early transition to TU Delft was significant, and I'm still grateful. **Tae-Hoon Kim**, although we had different supervisors, we shared many thoughts and supported each other during hard times. Your presence, especially during long evenings in the lab, was a real source of comfort. **Teruki Someya** and **Mojtaba Jahangiri**, our conversations and shared reflections have stayed with me. **Teruki**, I especially appreciated how we could understand each other despite our imperfect English, perhaps thanks to the similar grammar of our native languages. **Rao Padmakumar** and **Sandra K. R**, although we worked together only briefly, I appreciated your presence and hope we can collaborate again in the future.

To my Korean friends in the Netherlands, thank you for being my second family.

Juseong Lee, we started our Ph.D. paths together, and your presence—as a drinking mate and a friend through highs and lows—meant a lot. **Minjung Jeong**, **Hanjun Kim**, **Jeseung Moon**, and **Yeun Kim**, although we are now scattered in different countries, I miss the weekends of board games and the ski trips we looked forward to together. **Dongil Shin**, despite being younger, your maturity and your company during our many dinners and walks were always comforting. I look forward to the day we recall those times over a meal. **Jeongju Oh**, though our fields were different, our conversations and shared concerns meant a lot to me. I still think fondly of the times we rode bikes and talked freely. **Kijun Kim** and **Moonhyuk Choi**, we didn't spend a lot of time together, but our occasional meetups and chats were warm memories that I still cherish.

Finally, I offer my deepest thanks to my parents, who have always supported my choices. Although I often surprised you with my abrupt decisions, you never discouraged me—instead, you gave me the freedom and encouragement to pursue what I truly wanted. I wish I had invited you to visit more often during my time in the Netherlands, but I now look forward to spending more time together in the future. This Ph.D. title is not just mine—it belongs to you as well. I am profoundly grateful for your lifelong dedication.

These five years at TU Delft were filled with both expected and unexpected moments. What began with uncertainty and anxiety eventually led to confidence and gratitude. This journey was not only an academic achievement but also a meaningful period of personal growth. Though my Ph.D. has come to an end, my research will continue—and just as I received support from so many, I will strive to help others grow in their own paths.

CURRICULUM VITÆ

Jaekyum Lee received his Bachelor of Engineering (B.E.) degree in Electrical Engineering from Korea University in 2011. He then completed his Master of Science (M.S.) degree in Electrical Engineering at the Korea Advanced Institute of Science and Technology (KAIST) in 2013. His M.S. research, supervised by Professor Seung-Tak Ryu, focused on high-speed analog-to-digital conversion. His thesis, titled "10-bit 2-Channel Time-Interleaved SAR ADC with 2-Channel DC-DC Converters," explored mixed-signal circuit techniques for power-efficient, high-speed ADC design.

Following his graduate studies, he worked at Samsung Electronics from 2013 to 2017 as an Engineer in the Sensor Product Development Team. This marked the beginning of his involvement in CMOS image sensor development, where he gained hands-on experience in the design and characterization of sensor interface circuits, pixel readout chains, and system-level verification.

In 2018, he began his Ph.D. in Microelectronics at Delft University of Technology (TU Delft) in the Netherlands, under the supervision of Professor Albert Theuwissen. His doctoral research focused on high-speed image sensor readout architecture, with emphasis on the co-design of analog-to-digital conversion circuits and system-level data management to meet the demands of high frame rate and low power operation. Specifically, he proposed a dual-path approach to frame rate enhancement: first, by developing a compact, low-noise, and energy-efficient column-parallel SAR ADC architecture optimized for area-constrained image sensors; and second, by implementing an adaptive reconfigurable system that dynamically enables region-of-interest (ROI)-based readout to reduce unnecessary data transfer and processing overhead. The integration of circuit-level innovation with real-time reconfigurable control allowed for scalable performance improvements while maintaining image quality. His dissertation is titled "High-Speed Image Sensor Readout Architecture," and he is currently awaiting his doctoral defense.

After completing his Ph.D. contract, he joined the Microelectronics Circuits Centre Ireland (MCCI) at the Tyndall National Institute in Cork, Ireland, as a Senior Researcher in 2023. At MCCI, he continues his research on CMOS image sensors, with a focus on compact readout architecture and system integration, now targeting biomedical applications. His work involves the design of noise-shaping SAR ADCs with compact area for integration in ultra-small image sensors, particularly targeting a 1mm^2 sensor footprint. These architectures are optimized for high-efficiency imaging in resource-constrained environments, such as implantable and portable biomedical devices.

His research interests lie in CMOS image sensor readout architecture and system-level design, with particular emphasis on high-frame-rate and high-dynamic-range imaging. He is especially interested in enhancing readout speed through both circuit-level innovations—such as the design of energy-efficient SAR ADCs—and system-level approaches, including adaptive and reconfigurable sensor architectures. During his Ph.D., he published journal papers on high-speed readout circuit design and presented a work-

shop paper on reconfigurable system architecture for image sensors. His broader interests include temporal noise reduction, ROI-based imaging control, and integrated sensor systems for compact and application-specific platforms.

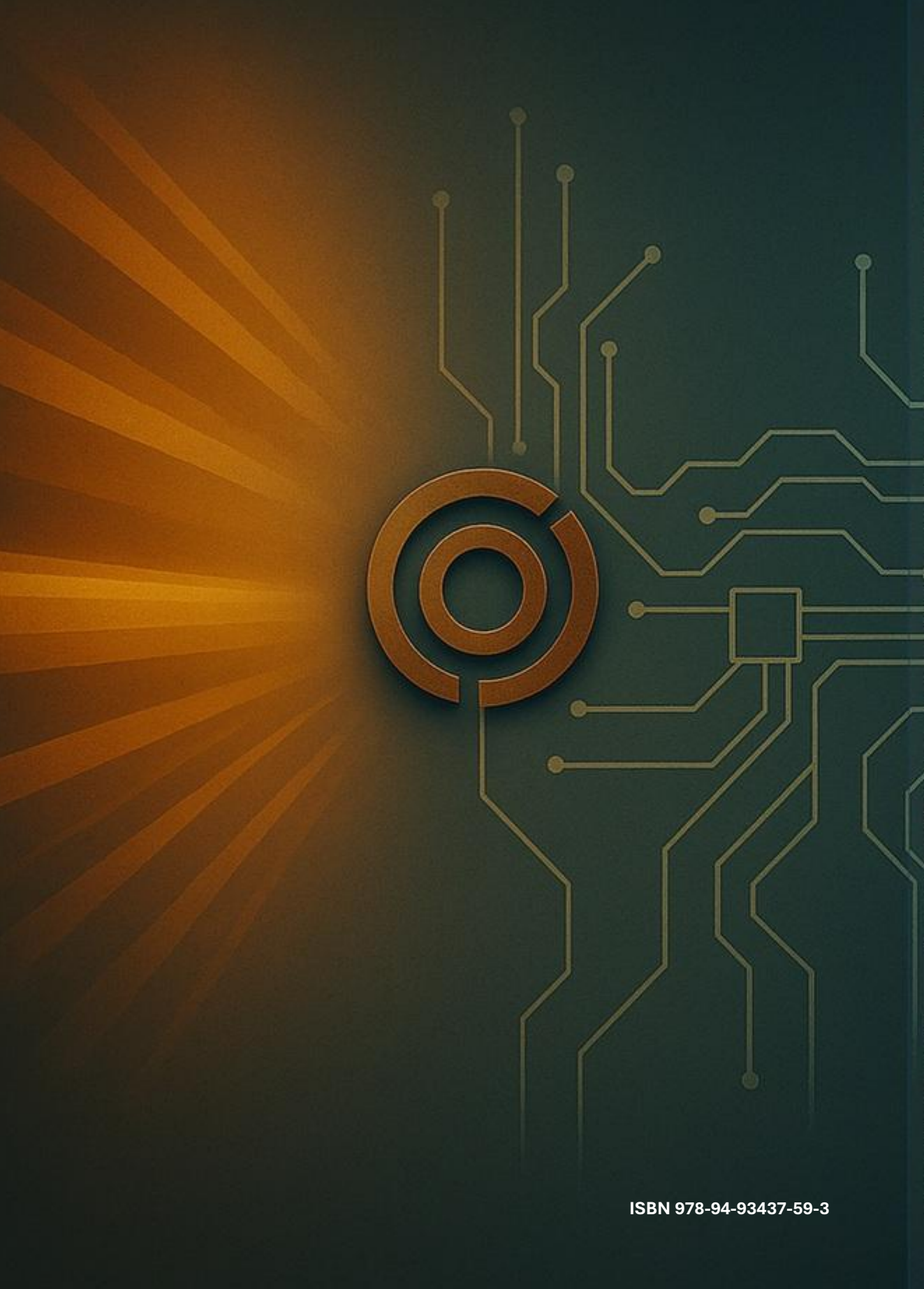
LIST OF PUBLICATIONS

4. **J. Lee**, A. Theuwissen, "A linearity improvement method for CIS column-parallel SAR ADC using two-step conversion," *ESSCIRC 2023*, Lisbon, Portugal, 2023.

3. **J. Lee**, A. Theuwissen, "A high-speed image sensor to track a moving object with a dual-mode reconfigurable system," *Scientific CMOS Image Sensors Workshop*, ESA-ESTEC, 22–23 November 2022.

2. **J. Lee**, A. Theuwissen, "An offset calibration technique for CIS column parallel SAR ADC using memory," *Electronic Imaging*, January 2022.

1. **J. Lee**, A. Theuwissen, "A 10b 1MS/s column parallel SAR ADC for high-speed CMOS image sensors with offset compensation technique using analog summation method," *Scientific CMOS Image Sensors Workshop*, Toulouse, 26–27 November 2019.



ISBN 978-94-93437-59-3