Dynamic Offset Compensated Amplifiers with Sub-pA Input Current and Low Distortion

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Dynamic Offset Compensated Amplifiers with Sub-pA Input Current and Low Distortion

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Dissertation

for the purpose of obtaining the degree of doctor
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chair of the Board for Doctorates
to be defended publicly on
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Voor mijn vader

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Chapter 1
Introduction

In an ideal world, CMOS amplifiers would have no offset, no input current and no drift or 1/*f* noise. In practice, they suffer from large offset (several millivolts), offset-drift (several μV/ºC), and high 1/*f* noise corners (several kilohertz). To tackle these non-idealities, dynamic offset compensation (DOC) techniques, such as chopping and auto-zeroing, are often used. These techniques rely on the fact that low-frequency errors can often be separated from the signal of interest. Auto-zeroing does this by performing the separation in the time domain, while chopping performs the separation in the frequency domain. Since both techniques are dynamic, i.e. continuously active, they also reduce offset-drift and 1/*f* noise. The following sections will introduce these techniques, their pros and cons and present an overview of the state of the art. It will be shown that while DOC amplifiers can achieve excellent offset, they also exhibit significant levels of input current (tens of pA) and distortion, limiting their use in applications such as high-impedance sensor readout, and high-linearity audio and instrumentation signal chains.

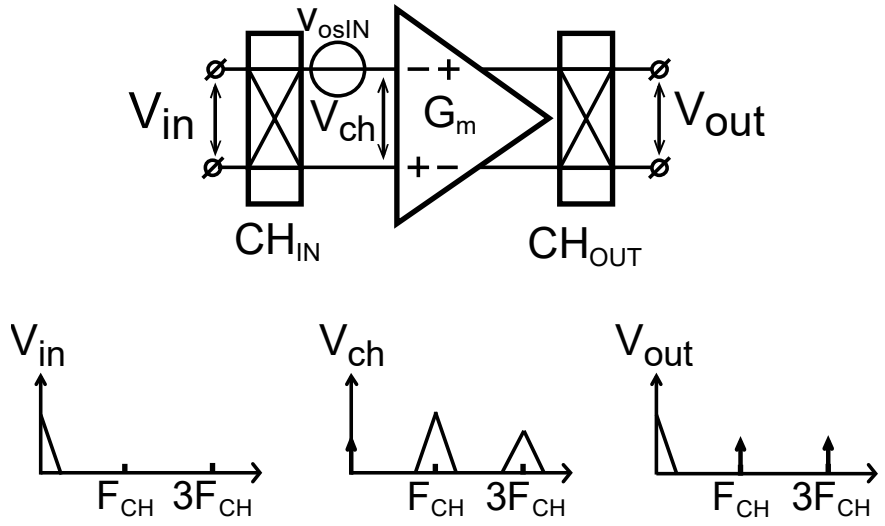

Fig. 1-1. A chopper amplifier and the different spectra for an input signal with a triangular spectrum.

1.1.1 Chopping

Chopping involves the use of polarity-reversing switches (choppers) to up-modulate low-frequency errors to a higher (chopping) frequency. An example of a chopper amplifier is shown in Fig. 1-1, where the input signal has a triangular spectrum near DC. The input signal (V_{in}) is first up-modulated by the input chopper (CH_{IN}) to the chopping frequency (F_{CH}) and its odd multiples, is then amplified, and finally, it is demodulated by the output chopper (CH_{OUT}) effectively leaving it at the baseband. In contrast, the offset (V_{osIN}) only passes through the output chopper, where it is up-modulated to F_{CH} and its odd multiples.

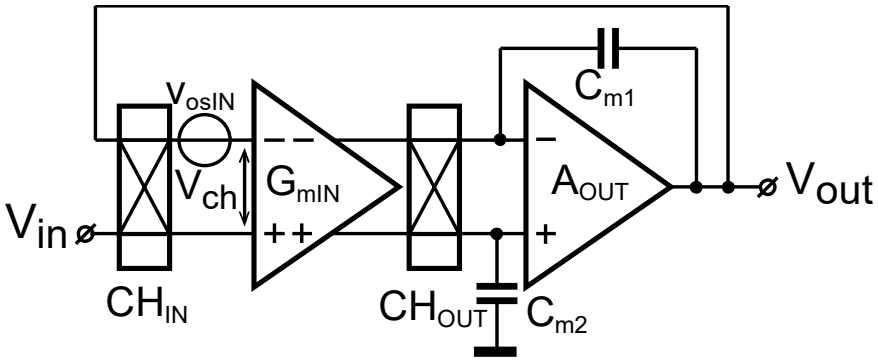

Fig. 1-2. A two-stage Miller compensated chopper amplifier.

A chopper amplifier can be used as the first stage of a two-stage Miller compensated amplifier, here configured as a buffer, as shown in Fig. 1-2. A major drawback of this amplifier is that the up-modulated offset will appear as output ripple. This will be somewhat filtered by the Miller capacitors (C_{m1} and C_{m2}), resulting in a triangular ripple voltage, which is superimposed on the desired output signal and may thus limit the amplifier's available output swing. Ripple can be further suppressed by placing a low-pass filter after the amplifier. However, to achieve sufficient ripple suppression, the filter's cut-off frequency needs to be much lower than the chopping frequency, which limits the available signal bandwidth. Moreover, the amplifier's available output swing will still be limited. Additional techniques are usually needed to limit the ripple, some of which will be described in the following sections.

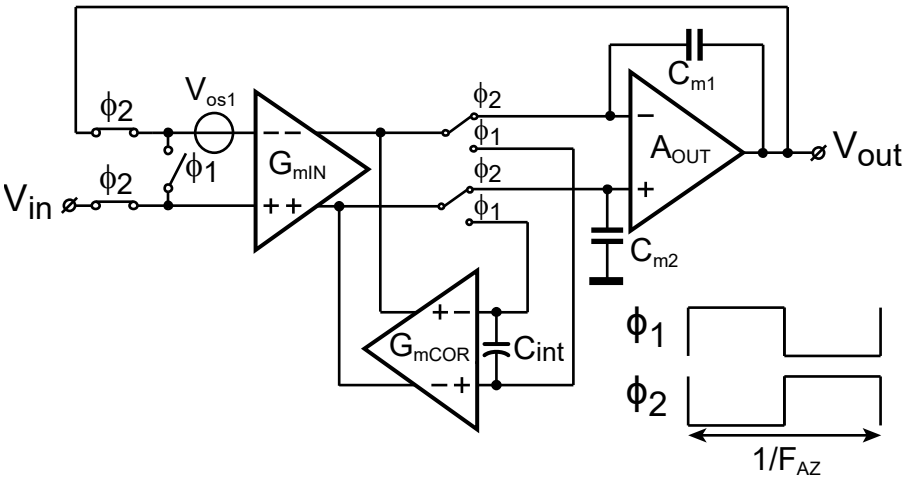

Fig. 1-3. An auto-zeroed two-stage amplifier in the amplification phase.

1.1.2 Auto-zeroing

Auto-zeroing involves periodically sampling the offset of an amplifier and then subtracting it from the input signal. An example of an auto-zeroed two-stage amplifier configured as a buffer is shown in Fig. 1-3. In a first phase (Φ_1), the offset of the input stage (V_{os1}) is detected by shorting its input. The resulting current from G_{mIN} is then integrated on C_{int} until the resulting voltage compensates for V_{os1} via the current generated by G_{mCOR}. In a second phase (Φ_2), the offset will still be canceled by the sampled voltage on C_{int}, while the amplifier is now connected to the input signal (V_{in}).

A major limitation of the amplifier shown in Fig. 1-3 is that it is not continuously available to process the input signal. To address this, two auto-zero amplifiers can be combined in a ping-pong fashion [1.1]. A second option is to use an auto-zero stabilized topology, in which an auto-zeroed amplifier corrects the offset of another, continuously available, main amplifier. This will be discussed in more detail in Section 1.4.1.

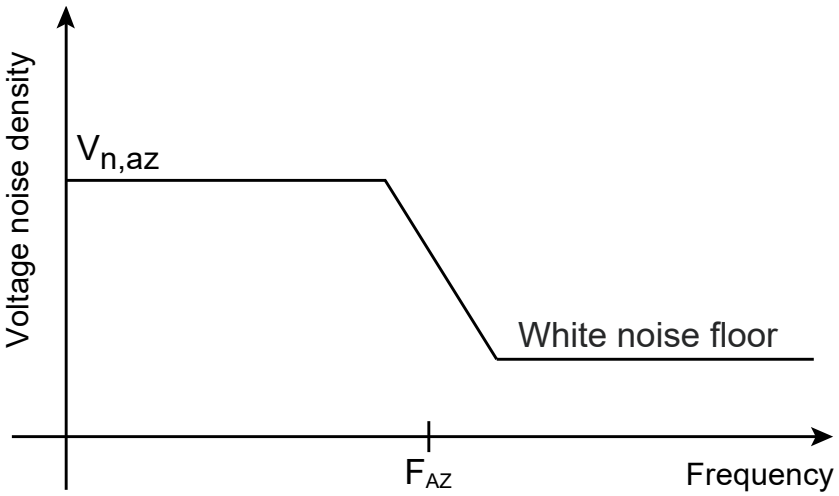

Fig. 1-4. Typical noise spectrum of an auto-zero amplifier.

Since it is a sampling technique, auto-zeroing also suffers from noise folding. This increases the noise below the auto-zeroing frequency (F_{AZ}), resulting in a noise bump around DC (Fig. 1-4). Even when noise folding is minimized by bandwidth limiting, the low-frequency noise of the input stage will always be sampled, which means that the noise floor will always be increased by at least a factor of $\sqrt{2}$. This effect will be further discussed in Chapter 3.

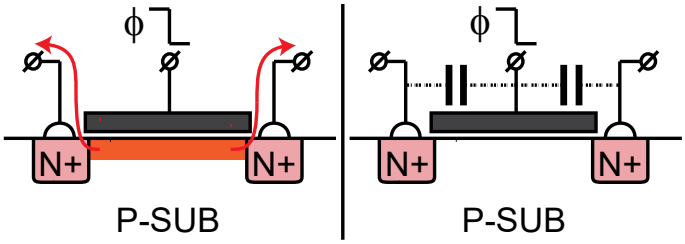

Fig. 1-5. Charge injection (Left) and clock feedthrough (Right) in a NMOS transistor.

1.2 Common drawbacks of DOC amplifiers

The performance of DOC amplifiers is often limited by the periodic activity of the MOS switches located at their inputs. To understand this better, this section will discuss the switching behavior of MOS transistors.

1.2.1 Charge injection and spikes

When a MOS switch transitions from "off" to "on", a channel is formed between its source and drain. As a result, the required channel charge (Q) is drawn from both terminals, with a total amount given by:

$$Q = WLC_{ox}(V_{GS}-V_{TH}). \quad (1\text{-}1)$$

In this equation, W and L are the width and length of the transistor, and C_{ox} is the gate capacitance per unit area, V_{GS} is the gate-source voltage, and V_{TH} is the threshold voltage. When the same switch transitions from "on" to "off", this channel charge is transferred back to these terminals and thus injected into the source and drain circuitry (Fig. 1-5 Left).

Besides this, there is also clock feedthrough, which occurs via the gate-drain and gate-source overlap capacitance of the transistor. This also causes charge transfer to the source and drain when the clock signal on the gate transitions (Fig. 1-5 Right). Commonly, the distinction between these two

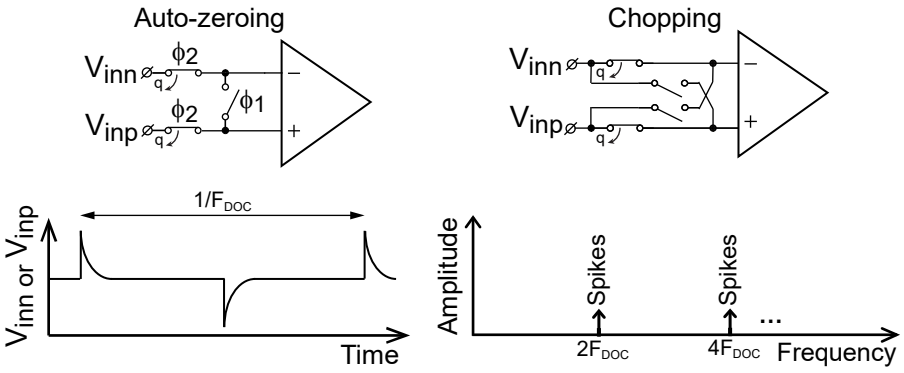

Fig. 1-6. Charge injection in auto-zero and chopper amplifiers and the resulting spikes in the time-domain (Left) and frequency-domain (Right)

effects is ignored, and both are referred to as "charge-injection". This convention will also be used in the rest of this thesis.

The charge injection of the MOS switches leads to short spikes in the input and output voltages of DOC amplifiers, whose amplitudes range from tens of μV to a few mV. These spikes typically settle exponentially, leading to the waveform shown in Fig. 1-6 (Left). They are also visible in the amplifier's output spectrum as tones at twice the chopping/auto-zeroing frequency (F_{DOC}) and its multiples (Fig. 1-6 (Right)).

The thermal noise density of a MOSFET switch is given by:

$$v_n = \sqrt{\frac{4kT}{\mu C_{ox}\frac{W}{L}(V_{GS}-V_{TH})}} \tag{1-2}$$

In this equation, μ is the mobility of the charge carriers, k is the Boltzmann constant, and T is the temperature. Comparing equations (1-1) and (1-2) shows that there is a tradeoff between spike amplitude and (thermal) noise. For lower noise, wider switches are required, which increases charge injection and, therefore, spike amplitude. Technology scaling reduces the required switch size for a certain noise level. This means that for the same noise specification, the charge injection is reduced by L^2, as shown in Appendix A.2.

In general-purpose operational amplifiers, spikes can be a significant drawback, especially since the phase relation of the DOC clock to the input signal is generally unknown. Even state-of-the-art DOC amplifiers suffer from

spikes to a greater or lesser degree, limiting their usefulness as general-purpose operational amplifiers.

1.2.2 Charge injection mismatch, input current and residual offset

The charge injection and absorption of a single switch will ideally cancel each other out after consecutive "on"-to-"off" and "off"-to-"on" transitions, leading to a net-zero input current. However, when several switches are involved, their charge injection mismatch can still lead to input current. This means that DOC amplifiers lose one of the main advantages of CMOS amplifiers, namely their low input current. Auto-zeroing requires half the number of input switches compared to chopping, leading to half the input current, assuming the same charge injection mismatch. Furthermore, the periodic shorting of the amplifier's input during auto-zeroing reduces the input current by an extra factor of two. This will be further discussed in Section 2.1.1.

The input current of a DOC amplifier will thus be proportional to the mismatch of the channel charge, which has a standard deviation of [1.2]:

$$\sigma_Q = C_{gate}\,\sigma_{VT} = C_{OX}A_{VT}\sqrt{WL} \tag{1-3}$$

In the above equation, A_{VT} is a proportionality factor, which decreases in modern technologies. Comparing equations (1-2) and (1-3) shows that there is also a trade-off between input current and noise. As discussed above, this improves with technology scaling. However, noise $\propto \sqrt{L/W}$ which means that for the same noise, W and L can be scaled together, e.g. by a factor of N. Since the input current $\propto \sqrt{WL}$, this means that the input current will be reduced by a factor N.

In a differential amplifier, charge injection mismatch will be stored on the amplifier's input capacitance, giving rise to residual offset. Since this charge injection mismatch occurs at every clock transition, a low DOC frequency is desirable, which is ultimately limited by the need for it to be higher than 1/*f* corner frequency.

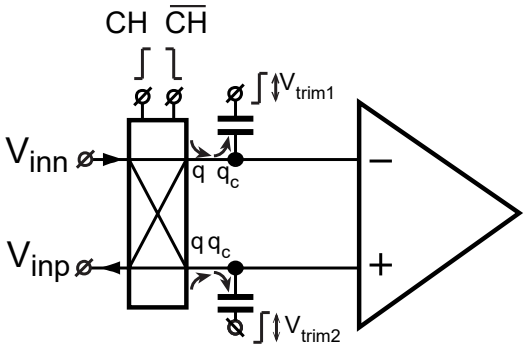

Fig. 1-7. Input current trimming.

1.3 Mitigating input current

In this section, ways of mitigating the input current of DOC amplifiers will be briefly discussed.

1.3.1 Minimum size switches

To minimize input current, both the size of the input switches and the DOC frequency should be minimized. The size of the switch is limited by the noise specification and the technology used. Since the noise specification is usually fixed, it helps to use a scaled technologies and minimize channel lengths. However, care must be taken since other forms of leakage, such as drain/source and gate leakage, have also increased in modern technologies. The DOC frequency is ultimately limited by the 1/*f* corner, which also increases with technology scaling. So, large devices and resistor degeneration should be used in the input differential pair to minimize its 1/*f* corner.

1.3.2 Input current trimming

Input current can also be compensated by trimming [1.17]. In Fig. 1-7, the charge injection mismatch of a chopper is compensated by injecting a compensating charge via two MOM capacitors. The capacitors are connected to clock signals with trimmable amplitudes, which can then be adjusted to compensate for the charge injection mismatch of the chopper. However, due to the high chopping frequency (4.8 MHz), the residual input current is still quite high (150 pA). Furthermore, the charge injection mismatch of the MOS switches and the compensating charge supplied by the MOM capacitors do not track well over PVT.

1.3.3 State-of-the-art input current in chopper amplifiers

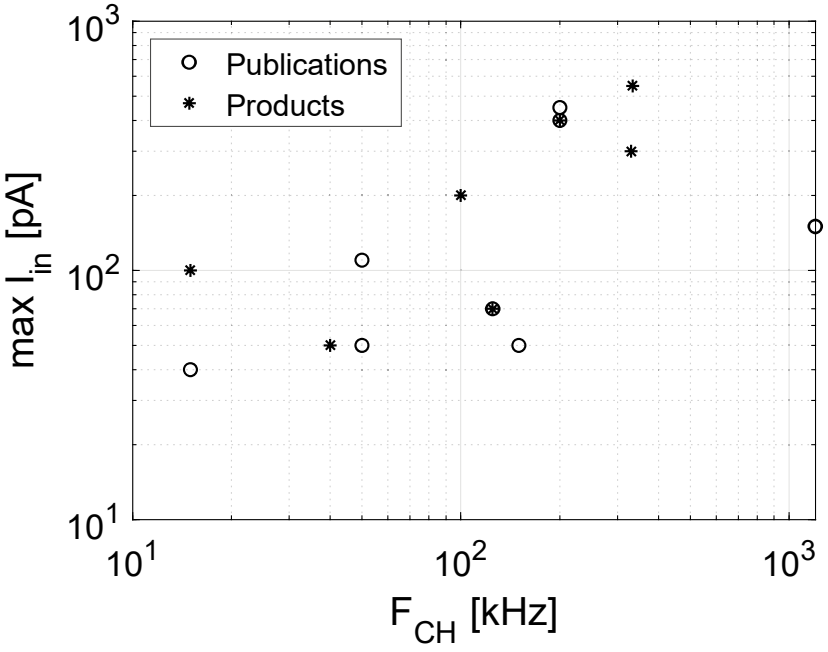

Fig. 1-8. Maximum input current vs chopping frequency for state-of-the-art chopper amplifiers.

Fig. 1-8 shows the maximum input current vs chopping frequency for state-of-the-art chopper amplifiers published before the start of this PhD in 2017; the underlying data can be found in Appendix A.1. A differentiation is made between products (stars) and publications (circles), since datasheets are typically based on data from more measured samples (thousands vs tens respectively). As discussed in section 1.3.1, chopper amplifiers with lower chopping frequencies should be able to achieve lower input current. However, this is only somewhat confirmed by Fig. 1-8. The expected trend is somewhat obscured by differences in technology, noise/distortion specifications and ESD leakage. It should also be noted that the amplifier with the highest chopping frequency (1200 kHz) uses trimming to lower its input current from 1.5 nA to 150 pA. State-of-the-art chopper amplifiers typically have maximum input currents in the range of several tens to hundreds of picoamps, with 40 pA being the lowest reported [1.8]. This can cause significant offset voltages in combination with high impedance signal sources (> tens of kΩ).

1.3.4 State-of-the-art offset in DOC amplifiers

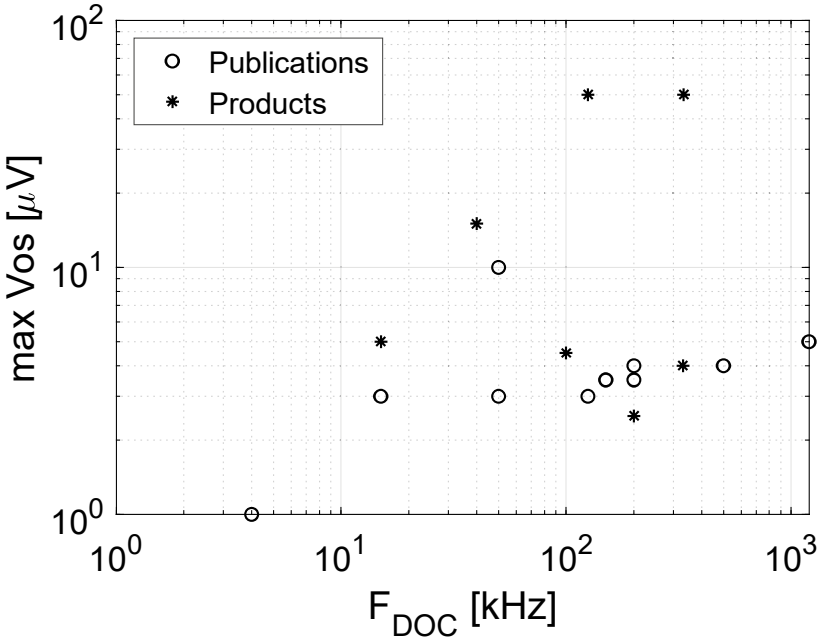

Fig. 1-9. Max offset voltage vs DOC frequency for state-of-the-art chopper amplifiers.

Similarly, Fig. 1-9 shows a plot of the maximum offset voltage vs the DOC frequency of state-of-the-art amplifiers published before 2017; the underlying data can be found in Appendix A.1. As discussed in the previous section, chopper amplifiers with lower chopping frequencies should achieve lower offset voltages. This is somewhat confirmed by Fig. 1-9, but is again somewhat obscured by the difference in technology and noise specifications. It shows that state-of-the-art chopper amplifiers with low chopping frequencies (<100kHz) can achieve offsets below 10μV. The lowest offset is achieved by a chopper-stabilized amplifier with the lowest chopping frequency (4kHz) [1.6].

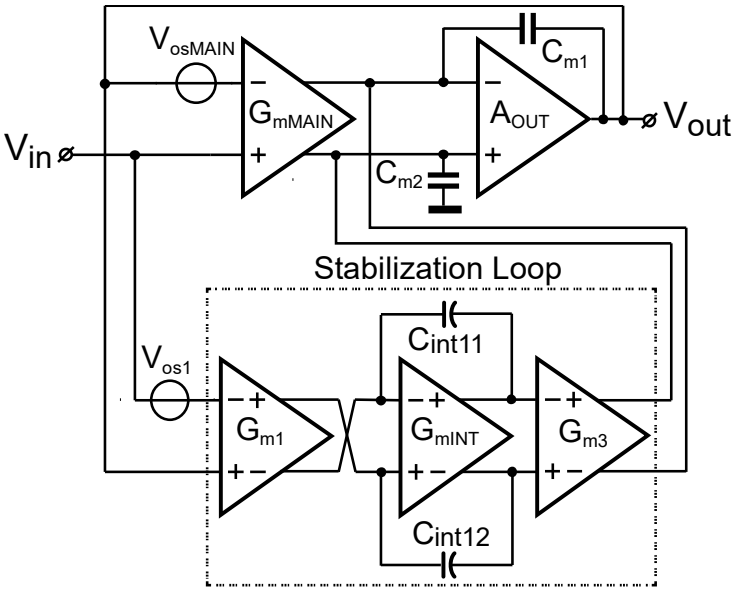

Fig. 1-10. An offset stabilized amplifier.

1.4 Mitigating chopper ripple

Ripple is a specific drawback of chopping. Numerous techniques have been proposed to mitigate it. In this section, some of the most important will be briefly discussed.

1.4.1 Offset-stabilized amplifiers

Offset-stabilized amplifiers [1.6] consist of a main amplifier whose offset is sensed and canceled by a low-offset stabilization loop. An example is shown in Fig. 1-10. The main amplifier consists of a two-stage amplifier with an offset V_{osMAIN}, which is then reduced by the stabilization loop. To minimize the overall offset, G_{m1} should be a low-offset amplifier, which is typically achieved with the help of chopping or auto-zeroing. Due to the feedback around the main amplifier, V_{osMAIN} is present at the input of G_{m1}. This is converted into a current and integrated on $C_{int11\text{-}12}$, which then drives G_{m3} to generate a current that compensates for the offset of G_{mMAIN}.

The advantage of offset-stabilization is that the main amplifier is always in the signal path, while the low-frequency path can be optimized to suffer less from the downsides of DOC techniques, such as ripple and spikes. The

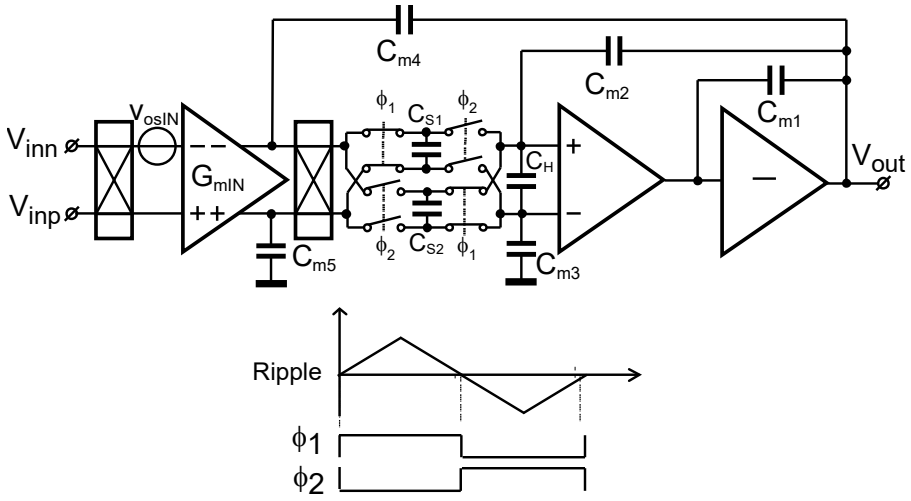

Fig. 1-11. A chopper amplifier with a switched-capacitor notch filter.

downside of this topology is that two low-noise input stages are required, which increases the overall area and power consumption.

1.4.2 Switched-capacitor notch filter

Noting that the upmodulated offset results in a triangular ripple at the output of an integrator or a Miller-compensated amplifier, its amplitude can be significantly reduced by sampling it at the zero crossings with a sample-and-hold circuit (Fig. 1-11) [1.7]. This can be achieved with the help of a two-stage switched-capacitor notch filter. Sampling capacitors C_{s1} and C_{s2} sample the ripple at the zero transitions at the end of Φ_1 and Φ_2 and transfer their charge to the hold capacitor C_H. The sinc function of the sample and hold causes a notch at the chopping frequency and its multiples. Although easy to implement, one downside of this technique is that the required capacitors can be quite large when low noise is required. Finally, the required current to charge the notch filter can result in more residual offset.

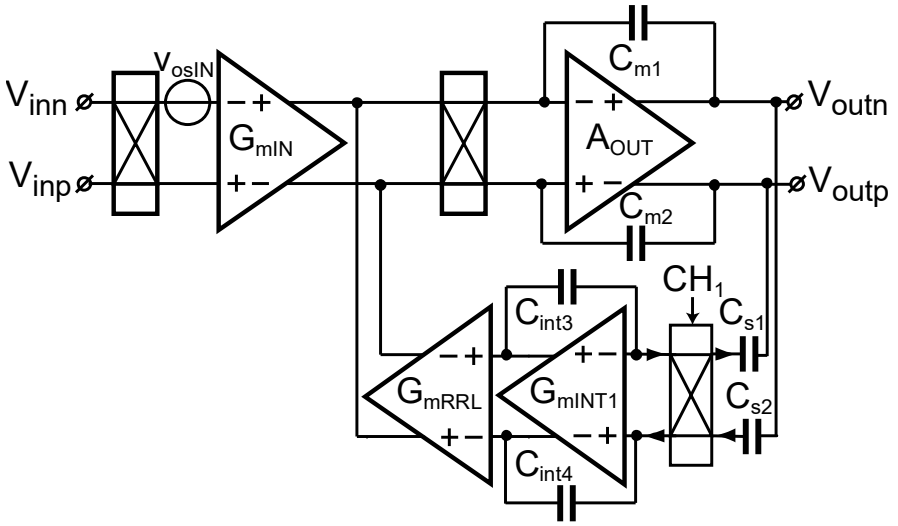

Fig. 1-12. A two-stage amplifier with ripple reduction loop.

1.4.3 Ripple reduction loops and auto correction feedback

A ripple reduction loop (RRL) [1.10] uses a feedback loop to sense ripple and then generate a compensating signal that minimizes the offset causing it. As shown in Fig. 1-12, capacitors (C_{s1} & C_{s2}) sense the ripple voltage and then convert it into a current that is then demodulated and integrated. Finally, an operational transconductance amplifier (OTA) is used to inject a correction current at a suitable point in the amplifier's input stage. However, input signals at the chopping frequency will also be suppressed the RRL, creating a notch in the amplifier's frequency response at the chopping frequency.

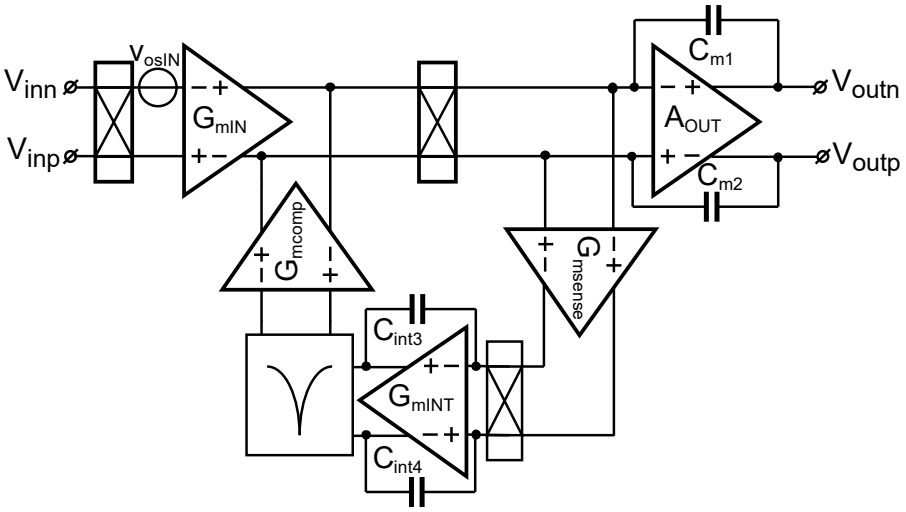

Fig. 1-13. A two-stage amplifier with auto correction feedback.

Auto correction feedback (AFCB) [1.11] uses a similar feedback loop to sense and suppress chopper ripple, as shown in Fig. 1-13. The main difference is that an OTA is used to sense the ripple at the virtual ground of the second stage. The sensed ripple current is then demodulated, integrated, and injected as a correction current. However, any DC signal at the amplifier input also reaches the input of the ACFB, which would normally suppress it. To prevent this, a notch filter is inserted after the integrator to filter out the upmodulated DC signal at the chopping frequency. ACFB also creates a notch in the amplifier's frequency response.

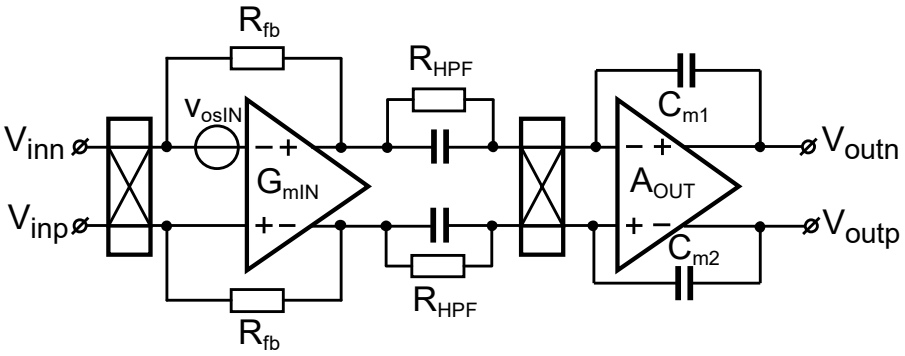

Fig. 1-14. A two-stage amplifier with a high-pass filter.

1.4.4 High-pass filtering

Another way to mitigate ripple is to filter out the offset of the input stage before it reaches the chopper [1.30] [1.31]. This can be achieved by inserting a high-pass filter (HPF) after the input stage before the output chopper, where it would otherwise create ripple (Fig. 1-14). A feedback resistor (R_{fb}) is placed across the input stage to limit the gain seen by the offset. One downside is that a low corner frequency is required to sufficiently suppress the ripple, which causes slow settling. Furthermore, R_{fb} must be large to preserve the gain of the input stage. The combination of a HPF and a chopper also creates a notch at the chopping frequency.

1.4.5 Ripple in chopper operational amplifiers

	Technique	Maximum ripple	F_{CH}
Kusuda [1.15]	ACFB	35µVrms	50kHz
ADA4051 [1.24]	ACFB	15µVrms	200kHz
Xu ISSCC2011[1.30]	RRL	2mVpp	500Hz
Fan ESSCIRC2012 [1.31]	RRL	0.5µVrms	25kHz
Fan JSSC2012 [1.14]	RRL	0.35µVrms	30kHz
Fan ISSCC2013 [1.20]	RRL	0.28µVrms	50kHz

Table 1-1 – Maximum ripple for state-of-the-art chopper amplifiers.

Unfortunately, the ripple amplitude is not often reported in datasheets and publications. Table 1-1 summarizes the reported maximum ripple of chopper amplifiers with an ACFB or RRL. The chopping frequency is also listed since it is easier to filter out high-frequency ripple. State-of-the-art chopper amplifiers with a ripple reduction loop can achieve a ripple below 1µVrms, which, in many applications, will be below the total integrated noise.

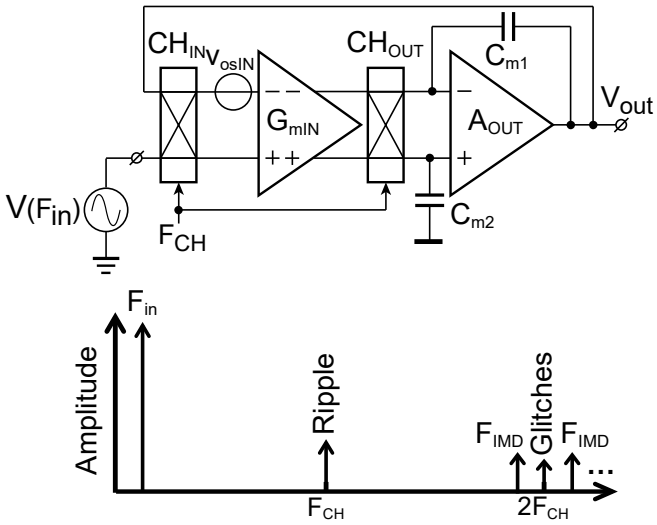

Fig. 1-15. Intermodulation distortion tones in chopper amplifiers.

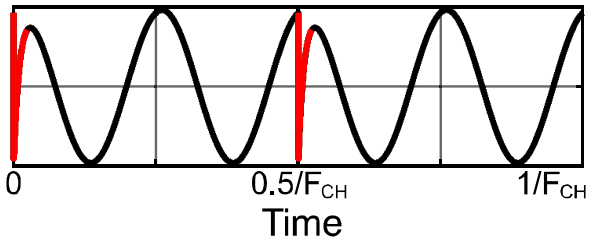

Fig. 1-16. Periodic pulse in the output of a chopper amplifier causing IMD.

1.5 Chopper drawback: intermodulation distortion

As shown in Fig. 1-15, intermodulation distortion [1.3]-[1.5] may occur in chopper amplifiers. An input signal at a fixed frequency (F_{in}) may intermodulate with the chopping frequency (F_{CH}) leading to tones at $F_{IMD} = |nF_{CH} \pm F_{in}|$, where n is even.

The basic cause of IMD can be understood by considering the output waveform that results when an amplifier with a finite bandwidth is chopped, as shown in Fig. 1-16. The output has large periodic pulses that are dependent on the input amplitude, causing tones in the output spectrum. These tones can be a significant form of distortion in chopper amplifiers. Auto-zero amplifiers

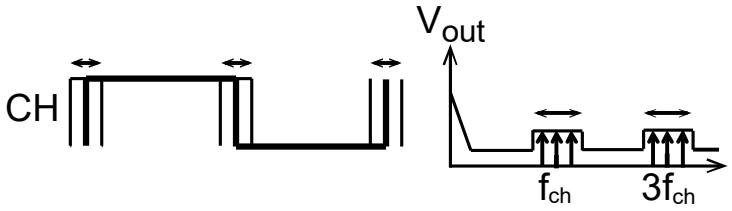

Fig. 1-17. Spectrum with spread-spectrum chopping.

also suffer from IMD mainly due to their inherent sample and hold action. In Chapter 2, the theory of IMD for both DOC techniques will be further developed.

1.6 Mitigating intermodulation distortion

In this section, techniques to mitigate intermodulation distortion will be described, and the performance of state-of-the-art amplifiers will be compared.

1.6.1 Spread-spectrum clocking

In prior art [1.12][1.13], spread-spectrum chopper clocks were used to lower the magnitude of DOC and IMD tones by dithering F_{DOC}. This turns DOC tones, IMD tones, and chopper ripple into noise-like signals, thus suppressing their amplitude (by ~10 to 20 dB) but at the expense of increasing the amplifier's noise floor (Fig. 1-17). However, since this approach does not actually solve the underlying problem, the tones will still be visible in the time domain [1.13].

1.6.2 State-of-the-art IMD in DOC amplifiers

	DOC technique	DOC frequency [kHz]	Spread spectrum	Input frequency [kHz]	IMD [dB]
AD8551 [1.3]	Auto-zero stabilized	4	No	0.5	-80
AD8571 [1.4]	Auto-zero stabilized	2 to 4	Yes	0.5	-90
Ivanonv [1.5]	Chopper stabilized with RRL	50 to 150	Yes	1	-103 (w/ Spread) -122.7 (w/o Spread)

Table 1-2 – IMD for state-of-the-art chopper amplifiers

Intermodulation distortion is not often reported for DOC amplifiers. In Table 1-2, the IMD of some state-of-the-art DOC amplifiers is shown. The input frequency is also listed since, as with most forms of distortion, it will be mitigated by the amplifier's loop gain, which typically decreases with frequency. Furthermore, the DOC frequency is also mentioned since, as will be discussed in Chapter 2, the IMD generally gets higher for input frequencies close to the DOC frequency. Using the spread spectrum technique, IMD tones can be reduced by 10 to 20 dB, depending on the spreading bandwidth. However, this is only effective at low input frequencies (~ 1kHz), where the distortion of amplifiers is generally good. Furthermore, the distortion is not really eliminated; it is merely spread out, and so it is still visible in the time domain. This makes DOC amplifiers unsuitable for applications that require high linearity (>90dB) at input frequencies above a few kHz.

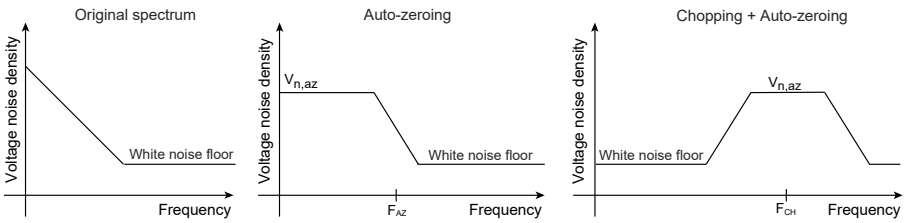

Fig. 1-18. Noise spectrum when combining chopping and auto-zeroing.

1.7 Auto-zeroing drawback: noise folding

A specific drawback of auto-zeroing is that it causes undersampled thermal noise to fold back to low frequencies [1.29]. As a result, the low-frequency noise density after auto-zeroing is typically larger than the original thermal noise density.

1.7.1 Combining chopping and auto-zeroing

Chopping and auto-zeroing can also be used together [1.8][1.9] to combine the advantages of both techniques. Auto-zeroing is then used to reduce the offset that would otherwise create chopper ripple. The whole auto-zeroed amplifier is then chopped to up-modulate the folded noise to the chopping frequency (Fig. 1-18). In [1.9], the auto-zero loop bandwidth is reduced to minimize the resulting noise bump. However, this comes at the expense of increased settling time.

1.8 Pros and cons of dynamic offset compensation techniques

	Auto-zeroing	Chopping
Spikes	-	-
Input current	-	--
Offset	++	++
Ripple	++	--
IMD	+/-	+/-
Noise	-	+

Table 1-3 – Pros and cons of auto-zeroing and chopping

State-of-the-art DOC amplifiers can achieve very low offsets (below 10μV). However, the charge injection mismatch of their input switches results in input currents of several tens to hundreds of picoamps. The input current of auto-zero amplifiers is theoretically four times lower than that of chopper amplifiers, as will be shown in Chapter 2, making them the preferred candidates for applications that require low input current. Furthermore, they do not suffer from ripple, making their outputs quieter. However, auto-zero amplifiers suffer from noise folding, which increases their low-frequency noise floor. One goal of this thesis is to design quiet auto-zero amplifiers with low input current and the lowest possible low-frequency noise.

Chopper amplifiers have the downside that they suffer from ripple. However, state-of-the-art chopper amplifiers have ripple voltages of around 1μVrms, which is below the total integrated noise in many applications. Chopper amplifiers also suffer from IMD, which limits their application in high linearity applications. Another goal of this thesis is to design low-distortion chopper amplifiers.

Achieving these two goals will result in amplifiers that invisibly use DOC techniques to approximate the performance of the ideal amplifier more closely, i.e. one with low-offset, low noise, and low distortion.

1.9 Organization of the thesis

The rest of the thesis is organized as follows. In Chapter 2, the theory of IMD, spikes and input current are discussed in more detail. Then in the following chapters, three designs that mitigate some of the drawbacks of DOC techniques are presented. In Chapter 3, a digitally-assisted auto-zero stabilized amplifier that achieves a combination of low offset, low noise, low input current, and no visible switching spikes is presented. In Chapter 4, the input

current is further lowered by trimming it. Chapter 5 presents a fill-in technique to minimize the effect of intermodulation distortion. Chapter 6 presents a relaxed version of this technique. Finally, the thesis ends with the conclusions and future work.

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Chapter 2
Input current and Intermodulation distortion in DOC amplifiers

2.1 Introduction

This thesis focuses on reducing the most critical remaining drawbacks of DOC techniques: input current and distortion. First, the input current of DOC amplifiers is discussed. Then, the theory of auto-zero-induced and chopper-induced intermodulation distortion is explained. Finally, the chapter ends with the analysis of the closed-loop IMD of a two-stage chopper amplifier and a chopper-stabilized amplifier.

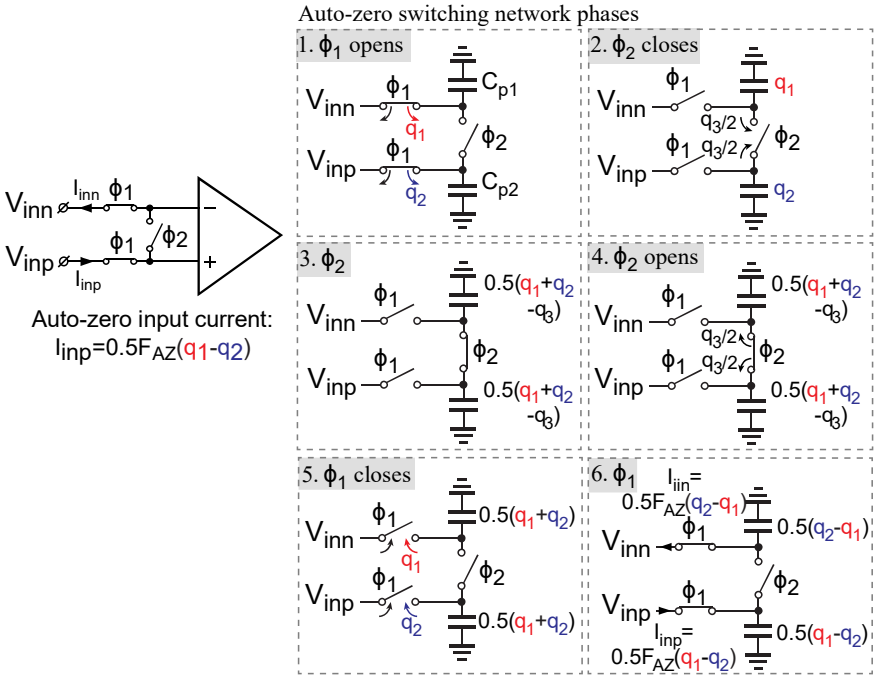

Fig. 2-1. Input current due to charge injection for an auto-zero amplifier.

2.1.1 Input current due to charge injection of auto-zero amplifiers

The input current of an auto-zero-amplifier can be determined by considering the non-overlapping switching sequences shown in Fig. 2-1. It is assumed that no differential input voltage is present, i.e. V_{inn}-V_{inp}=0, as would be the case in a high-gain feedback configuration. The switches introduce charge injection (CI) when they open and charge absorption (CA) when they close. The worst case is shown where all the CI/CA flows into/from the input/parasitic capacitors C_{p1} and C_{p2}. In reality, the input current will be lower since part of the charge will directly flow into/from V_{inn} and V_{inp} and cancel each other during consecutive opening and closing cycles. This split of CI/CA will depend on the source impedances and rise/fall time of the signals that control the switches. The input current is also accompanied by shot noise [2.1].

In the case of auto-zeroing, the CI of the opening ϕ_1 switches (q_1 and q_2) is stored on C_{p1} and C_{p2}. The ϕ_2 switch has symmetric impedances on both sides, so when it closes, its CA will equally split ($-q_3/2$) between the capacitors. The charge is shared during ϕ_2, resulting in $0.5(q_1+q_2-q_3)$ on each

capacitor. The CI of the opening ϕ_2 switch ($q_3/2$) will cancel $-q_3/2$, leaving $0.5(q_1+q_2)$ on each capacitor. When the ϕ_1 switches close again, their CA ($-q_1$ and $-q_2$) will be combined with the charge on C_{p1} and C_{p2}, leading to an average input current (I_{inp} and I_{inn}) of

$$I_{inp} = 0.5F_{AZ}(q_1-q_2) \quad (2\text{-}1)$$

$$I_{inn} = 0.5F_{AZ}(q_2-q_1). \quad (2\text{-}2)$$

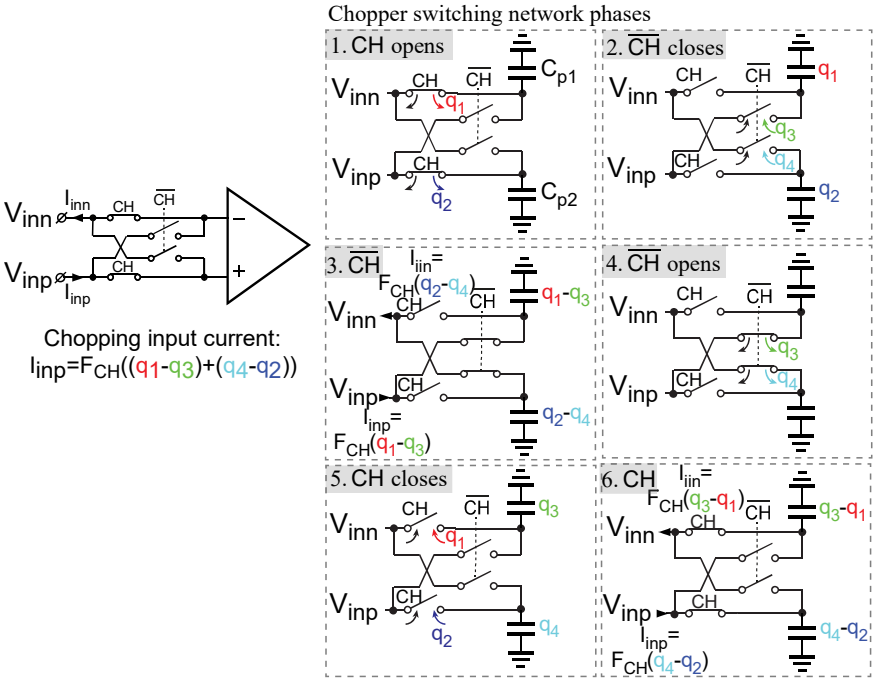

Fig. 2-2. Input current due to charge injection of a chopper amplifier.

2.1.2 Input current due to charge injection in chopper amplifiers

In the case of chopping (Fig. 2-2), the CI of the opening CH switches (q_1 and q_2) is stored on C_{p1} and C_{p2}. This is then combined with the CA of the closing $\overline{CH}$ switches ($-q_3$ and $-q_4$). This results in an I_{inn} of $f_{ch}(q_1-q_3)$ and I_{inp} of $f_{ch}(q_2-q_4)$ in $\overline{CH}$.

Similarly, the CI of the closing CH switches ($-q_1$ and $-q_2$) gets stored and combined with the CI of the opening $\overline{CH}$ switches (q_3 and q_4). This results in an I_{inn} of $f_{ch}(q_4-q_2)$ and I_{inp} of $f_{ch}(q_3-q_1)$.

After a complete chopping cycle, the result is a total average I_{inn} and I_{inp} can be expressed as:

$$I_{inn} = f_{ch}((q_1-q_3)+ (q_4-q_2) \quad (2\text{-}3)$$

$$I_{inp} = f_{ch}((q_3-q_1)+ (q_2-q_4). \quad (2\text{-}4)$$

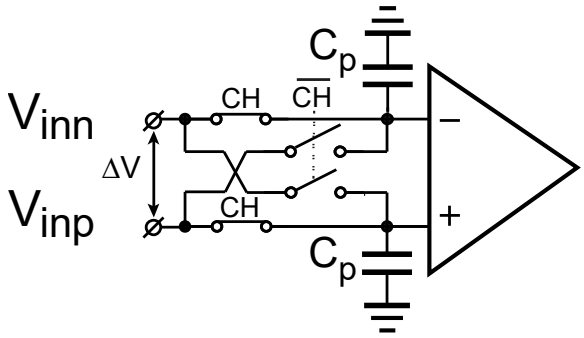

Fig. 2-3. Input current due to switched capacitor of a chopper amplifier.

Due to the chopping action, CI mismatch q_1-q_3 gets supplied by I_{inn} in $\overline{CH}$ and the opposite q_3-q_1 gets supplied by I_{inp} in CH, leading to incomplete cancellation.

2.1.3 Input current due to switched capacitor

Another source of input current is due to the switched capacitor resistor formed by the input switches and the input/parasitic capacitors (Fig. 2-3). When an input signal ΔV is present at the input, the parasitic capacitors C_p need to be charged every time the chopper transitions. This leads to an average input current of

$$I_{in} = 2\Delta V F_{CH} C_p. \qquad (2\text{-}5)$$

However, most chopper amplifiers are used in a feedback configuration, which minimizes the input swing. With sufficient DC gain, this is mostly an effect that becomes significant at higher input frequencies or in the case of instrumentation amplifiers. The same effect also occurs in auto-zero amplifiers.

2.1.4 Conclusion input current

Assuming the same CI/CA mismatch for all switches and $f_{ch}=f_{az}$, chopping generates four times more input current than auto-zeroing. This leads to the conclusion that when low input current is required, auto-zeroing is preferred over chopping.

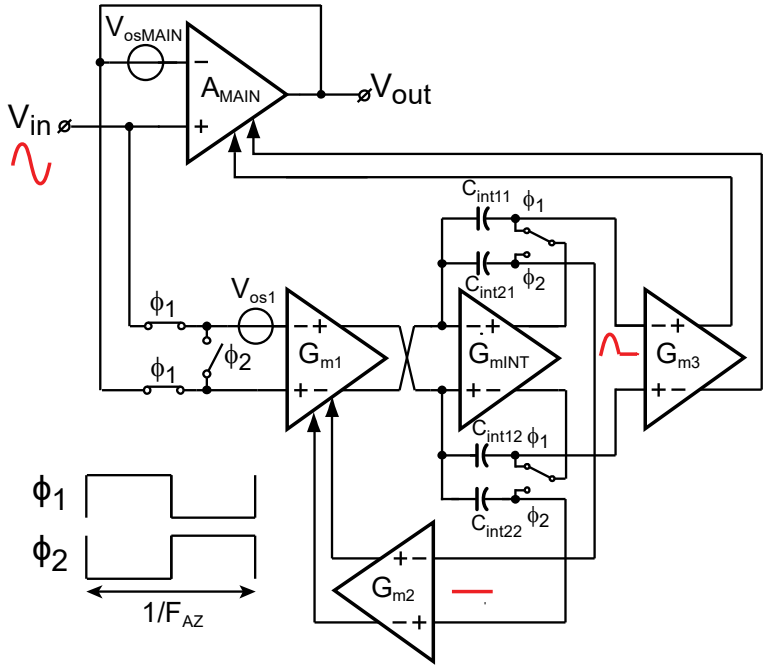

Fig. 2-4. Auto-zero stabilized amplifier with signal folding.

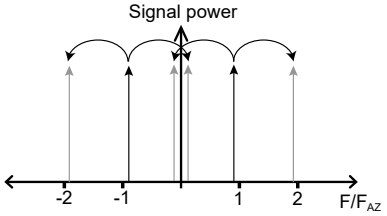

Fig. 2-5. Auto-zero stabilized amplifier with signal folding.

2.2 IMD in auto-zero amplifiers

In Fig. 2-4, an auto-zero stabilized amplifier based on an active integrator is shown. In phase ϕ_2, the offset of G_{m1} is auto-zeroed by shorting its input, integrating the resulting current on C_{int21} and C_{int22} and injecting a compensation current via G_{m2}. In phase ϕ_1, the offset of the main amplifier appears (due to the feedback around A_{MAIN}) at the input of G_{m1}, is integrated on C_{int11} and C_{int12} and compensated through G_{m3}. Since A_{main} has finite gain, a fraction of the input signal also appears at the input of G_{m1}. This will be

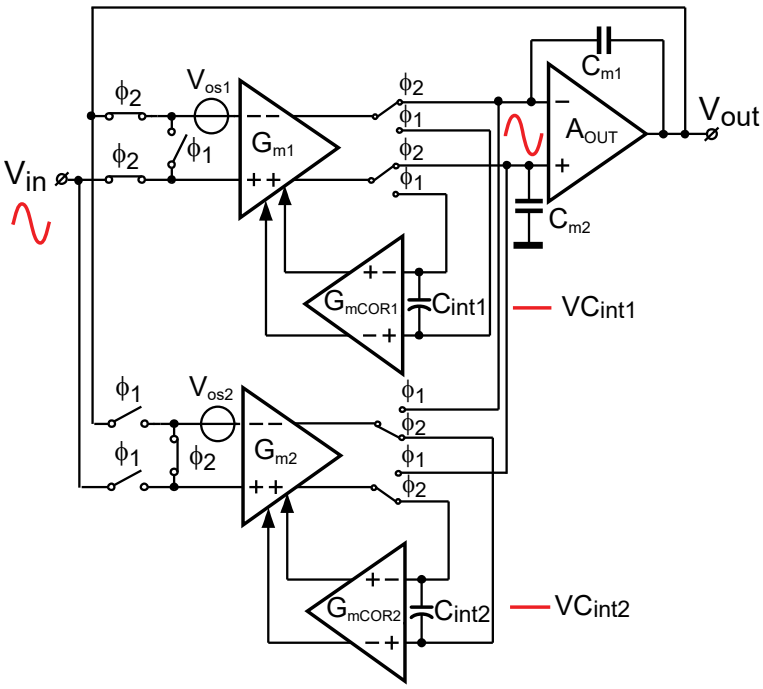

Fig. 2-6. Ping-pong auto-zero without signal folding.

integrated on C_{int11} and C_{int12} in phase ϕ_1 and gets held during ϕ_2. This sampling causes the input signal with frequencies above $F_{AZ}/2$ to foldback to baseband and cause IMD tones (Fig. 2-5).

In the ping-pong topology (Fig. 2-6), in phase ϕ_1, the offset of G_{m1} gets auto-zeroed by shorting the input and integrating the current on C_{int1}, while G_{m2} is available for the input signal. In phase ϕ_2, G_{m1} and G_{m2} switch roles, and G_{m2} gets auto-zeroed while G_{m1} is available to process the input signal. In this way, the signal does not get sampled on the auto-zeroing caps ($C_{int1,2}$), assuming ideal hold isolation. However, the settling process associated with the transitions between the two phases may still cause a small component of the input signal to get sampled on the hold capacitors, which, in turn, may cause IMD. This can be addressed by introducing a settling moment between the two phases [2.1].

In conclusion, direct signal folding in auto-zero amplifiers can be avoided by ensuring the signal is not sampled on the auto-zeroing capacitor(s).

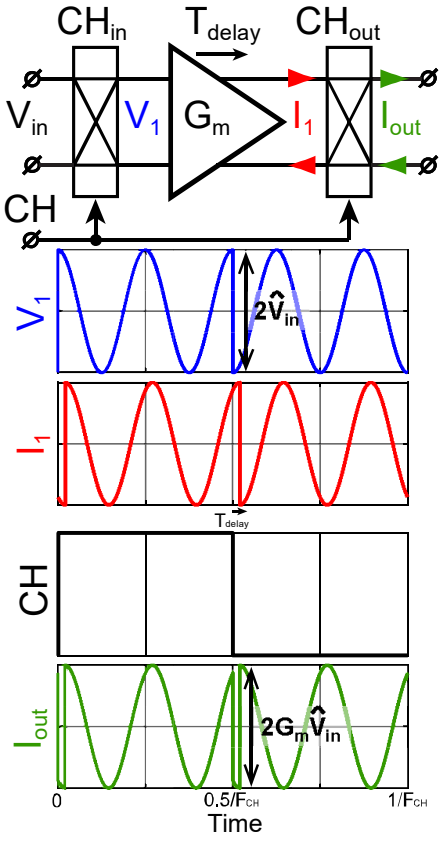

Fig. 2-7. Chopped OTA with a pure amplifier delay (T_{delay}) and the corresponding time-domain signals. The large pulses in the output current (I_{out}) result in chopper-induced IMD.

2.3 Chopper-induced IMD in open-loop

The cause of chopper-induced IMD can be understood by examining the signals in a chopped OTA in the presence of a sine-wave input signal V_{in} (Fig. 2-6). Due to the action of the input chopper (CH_{in}), the OTA's input V_1 will be an up-modulated version of V_{in}. Without loss of generality, the worst-case scenario is shown, in which the chopping transition coincides with the peak of

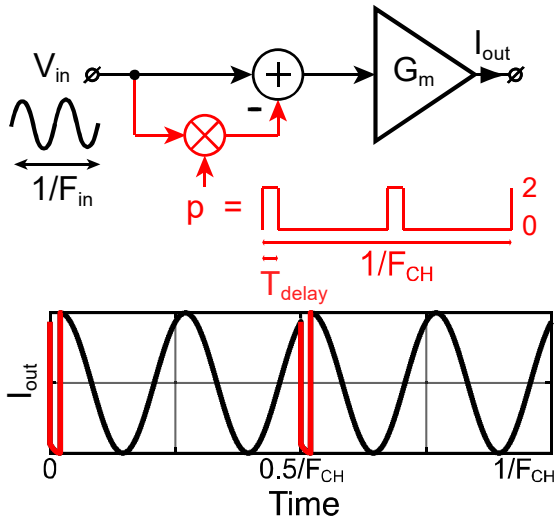

Fig. 2-8. Simplified model for a chopped OTA with a pure delay and the resulting waveform.

the input signal ($\hat{V}_{in}$). At this point, CH_{in} changes the polarity of the input signal, causing a $2\hat{V}_{in}$ step in V_1. This is converted into a current (I_1) by the OTA's transconductance G_m, and delayed by its finite bandwidth (here modeled as a pure delay T_{delay}). As a result, the edges of the chopping clock (CH) will no longer be aligned with the corresponding transitions in I_1. The demodulated current (I_{out}) produced by the output chopper (CH_{out}) will then contain large pulses around the chopping transitions. The amplitude of these pulses ($2G_m\hat{V}_{in}$) is equal to the instantaneous amplitude of the input signal and so can be a significant source of distortion. These pulses are the main cause of chopper-induced IMD.

In the frequency domain, the effect of these pulses can be better understood by considering the simplified model of the chopped OTA shown in Fig. 2-8. This consists of a delay-free OTA with an extra input path, shown in red, that models the IMD pulses. In this path, V_{in} is multiplied by a sequence

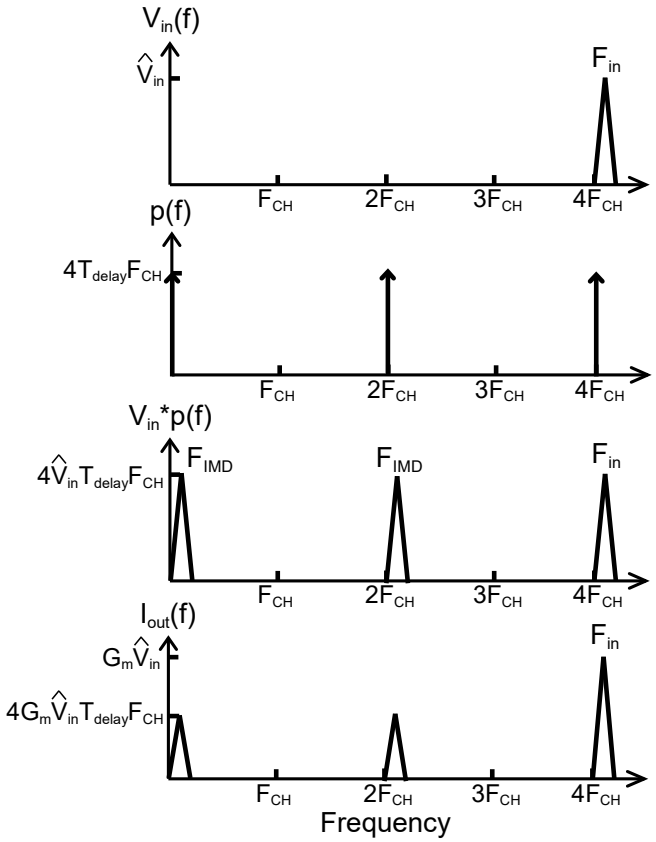

Fig. 2-9. The amplitude spectra of the different signals in the simplified model of a chopped OTA for a narrow-band triangular input spectrum.

of rectangular pulses (p) with an amplitude of 2, a width of T_{delay}, and a period of $0.5/F_{CH}$. The result (pV_{in}) is then subtracted from V_{in} to model the pulses generated at the chopping transitions.

In the frequency domain, it can be seen that the multiplication in the extra path will fold input signals near multiples of $2F_{CH}$ back to DC. The spectra of the various signals in Fig. 2-7 are shown in Fig. 2-9, where the input is assumed to have a narrow-band spectrum ($V_{in}(f)$) centered on $4F_{CH}$. At low frequencies, the spectrum of the rectangular pulses (p(f)) consists of impulses at multiples of $2F_{CH}$ with an amplitude of $4T_{delay}F_{CH}$ (see Appendix A.3). As a result, the convolution $V_{in}*p(f)$ consists of scaled and frequency-shifted versions of the input spectrum, which are subtracted from V_{in} and applied to

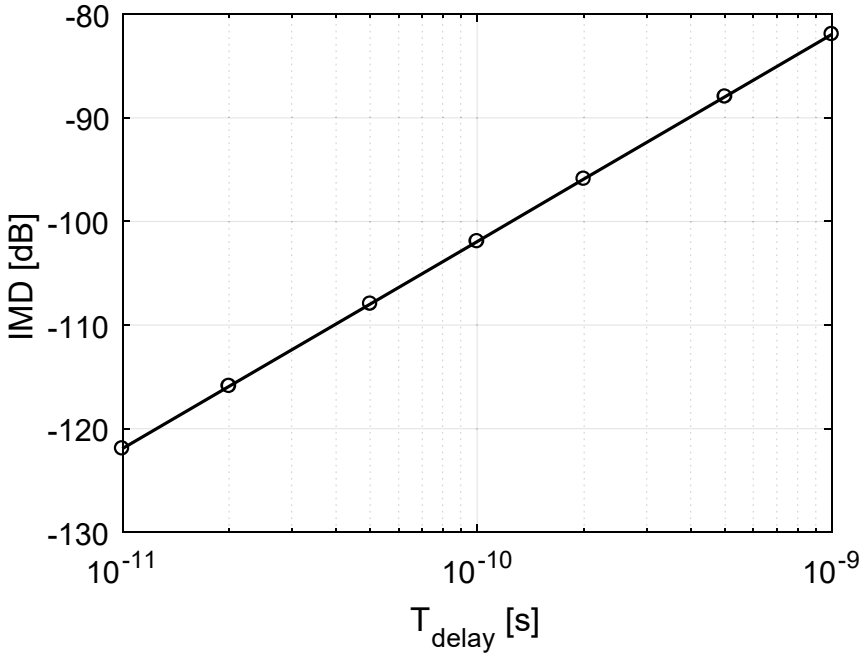

Fig. 2-10. The chopper-induced IMD tones vs the OTA delay for a fixed F_{CH} of 20 kHz.

the ideal OTA. The amplitude of the IMD tones in the resulting output current $I_{out}(f)$ in relation to the input tone are then given by:

$$\mathrm{IMD_{OL}} = 20\log\left(4T_{delay}F_{CH}\right). \tag{2-6}$$

For a fixed F_{CH} of 20 kHz, the IMD predicted by (2-6) is plotted in Fig. 2-10 for various values of T_{delay}. It can be seen that a delay of only 1 ns, results in a chopper-induced IMD of 82 dB. Decreasing the delay causes the amplitude of the IMD tones to roll-off at the rate of 20 dB/decade.

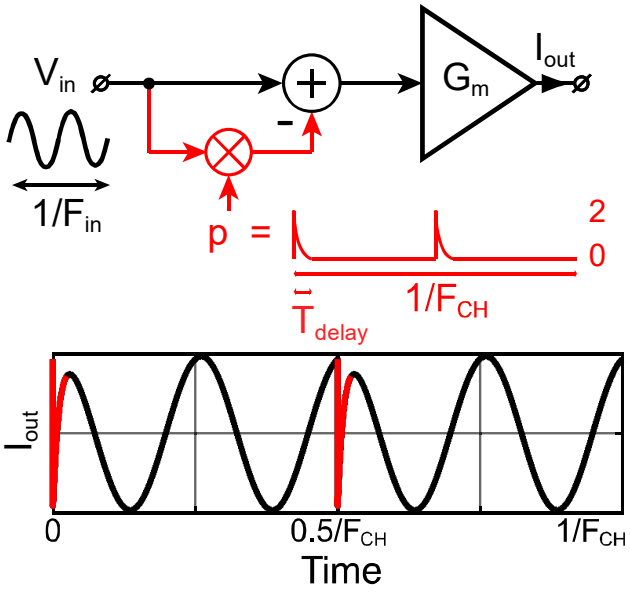

Fig. 2-11. Simplified model for a chopped OTA with limited bandwidth and the resulting waveform.

Rather than the rectangular pulses considered so far, finite OTA bandwidth will cause exponentially-settling pulses at the output of CH_{out}. This can be incorporated in the chopped OTA model (Fig. 2-8) by modifying the shape of the pulse sequence p(t), as shown in Fig. 2-11. Noting that $T_{delay} = 1/(2\pi BW)$, (2-6) can be rewritten in terms of amplifier bandwidth:

$$IMD_{OL} = 20\log\left(\frac{2F_{CH}}{\pi BW}\right). \qquad (2\text{-}7)$$

where BW is the bandwidth between the two choppers. This relation can also be shown directly by considering the Fourier transform of the pulse sequence shown in Fig. 2-11 (see Appendix A.4).

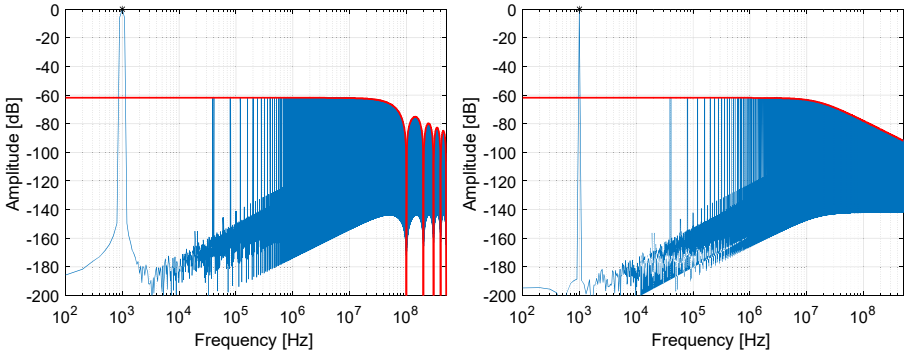

Fig. 2-12. IMD tones predicted by the delay model (Left) and the exponentially-settling model (Right) for equivalent T_{delay} of 10ns f_{ch}=20 kHz and f_{in}=1 kHz. In red the envelope predicted by the theory.

For low frequencies IMD tones, the open-loop IMD is predicted by equation (2-7) and there is no difference between the rectangular pulse model and the exponentially-settling pulse model. However, for higher-frequency IMD tones, a slight difference can be observed. This distinction is shown graphically in Fig. 2-12, showing the IMD tones predicted by the two different models for an equivalent T_{delay} of 10 ns, f_{ch}=20 kHz and f_{in}=1 kHz. In the first model (Left), the IMD tones are filtered by a sinc function at higher frequencies. In contrast, the latter (Right) is filtered by a low-pass filter (see Appendix A.4). This filtering effect only starts to play a role for IMD frequencies around the bandwidth of the amplifier. In red, the envelope of the IMD tones amplitude predicted by the theory is shown, confirming that there is a good agreement between the two.

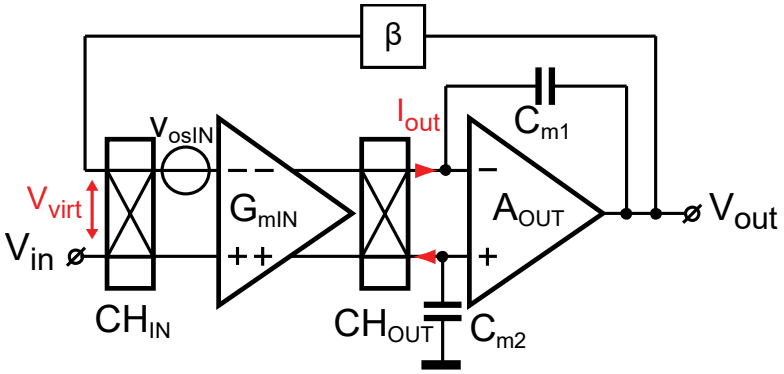

Fig. 2-13. Two stage chopper amplifier.

2.4 Intermodulation distortion in closed-loop

In the preceding analysis, the IMD was analyzed for the open-loop case. In this section, the IMD will be considered for the case with feedback. A simple two-stage amplifier, as well as a multi-path amplifier, is analyzed.

2.4.1 Two-stage chopper amplifier

The IMD in a two-stage chopper amplifier will be considered (Fig. 2-13). The voltage at the virtual ground of the chopped OTA is determined by the loop-gain (Aβ) and the amplitude of the input signal. This then leads to a voltage at the virtual ground of $V_{in}/A\beta$. As in the open-loop case, this then leads to IMD in the output current of the input OTA (G_{mIN}) given by:

$$I_{out,IMD} = \frac{G_{mIN} 2F_{CH} V_{in}}{\pi BWA\beta}. \tag{2-8}$$

Transferred back to the virtual ground, this results in a distortion of:

$$V_{virt,IMD} = \frac{2F_{CH} V_{in}}{\pi BWA\beta} \tag{2-9}$$

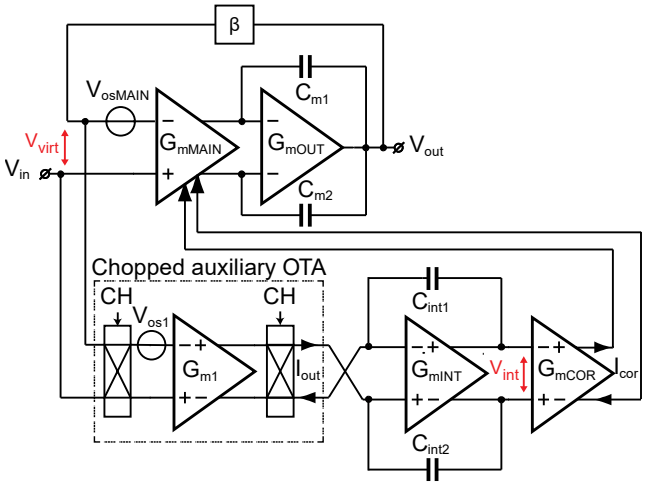

Fig. 2-14. Chopper stabilized amplifier

must be present. This distortion can only come from the output, so transferring it to the output (1/β) gives:

$$V_{out,IMD} = \frac{2F_{CH}V_{in}}{\pi BWA\beta^2}. \tag{2-10}$$

For Aβ >> 1, the signal at the output is given by V_{in}/β, so the ratio between the two gives:

$$IMD = \frac{2F_{CH}}{\pi BW}\frac{1}{A\beta} = IMD_{OL}\frac{1}{A\beta}. \tag{2-11}$$

This shows that, like other forms of distortion, feedback helps to reduce the open-loop IMD by a factor 1/Aβ.

2.4.2 Chopper-stabilized amplifier

A similar analysis can be done for the chopper-stabilized amplifier (Fig. 2-14). The current out of the G_{m1} contains the IMD (Equation (2-8)) and gets integrated into a voltage:

$$V_{int,IMD} = \frac{2F_{CH}V_{in}H_{loop}(f_{IMD})}{\pi BWA\beta} \tag{2-12}$$

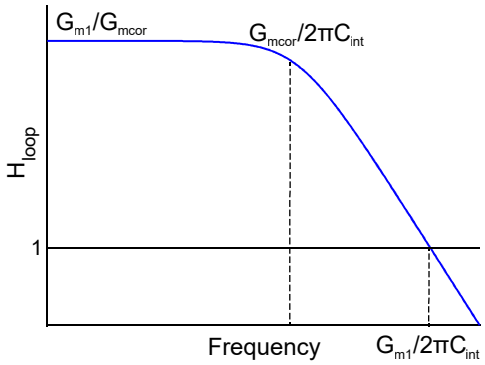

Fig. 2-15. Transfer function from the virtual ground to the output of the integrator.

where $H_{loop}(f_{IMD})$ is the transfer function from the virtual ground to the output of the integrator at the IMD frequency shown in Fig. 2-15.

This then gets converted to a current by G_{mCOR}, leading to:

$$I_{COR,IMD} = \frac{2F_{CH}V_{in}H_{loop}(f_{IMD})G_{mCOR}}{\pi BWA\beta}. \tag{2-13}$$

When this is referred to the virtual ground, though G_{mMAIN}, this leads to a distortion of:

$$V_{virt,IMD} = \frac{2F_{CH}V_{in}H_{loop}(f_{IMD})}{\alpha\pi BWA\beta} \tag{2-14}$$

where $\alpha=G_{mMAIN}/G_{mCOR}$. This distortion can only come from the output, so referring it to the output ($1/\beta$) leads to:

$$V_{out,IMD} = \frac{2F_{CH}V_{in}H_{loop}(f_{IMD})}{\alpha\pi BWA\beta^2}. \tag{2-15}$$

Looking at the ratio with the signal (V_{in}/β), the IMD becomes:

$$IMD = \frac{2F_{CH}}{\pi BW}\frac{1}{A\beta}\frac{H_{loop}(f_{IMD})}{\alpha} = IMD_{OL}\frac{1}{A\beta}\frac{H_{loop}(f_{IMD})}{\alpha}. \tag{2-16}$$

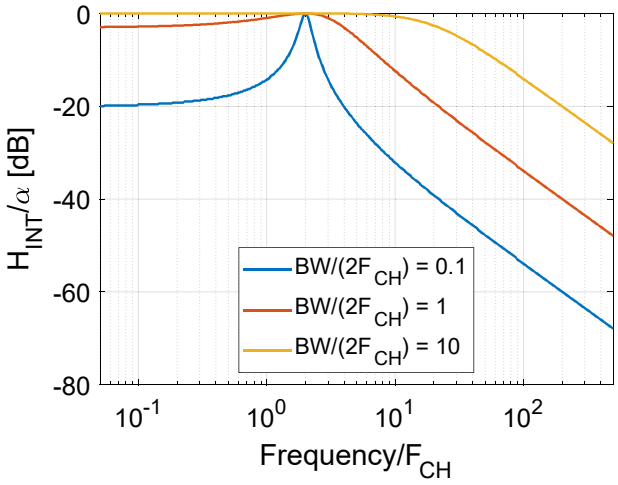

Fig. 2-16. H_{loop}/α as a function of Frequency/F_{CH} for three different BW/(2F_{CH}) ratios and n=2.

Compared to the two-stage amplifier, the additional term H_{loop}/α, represents the low pass filtering action of the stabilization loop. If we assume $G_{m1}=G_{mMAIN}$, which is often the case to achieve equal noise contribution, this function has a gain of one at low frequencies. To observe what this function does to the IMD tone amplitude for a certain F_{in}, it needs to be remapped according to $F_{IMD}=|nF_{DOC}\pm F_{in}|$. The shape of this remapped function depends on the ratio between nF_{DOC} and the bandwidth of H_{loop}/α (BW). This is graphically shown in Fig. 2-16, where the function is plotted for three different ratios of BW/(2F_{CH}) and a fixed IMD order n=2. In this case, the bandwidth given by BW = $g_{mCOR}/2\pi C_{int}$.

If BW >> nF_{DOC}, the remapped function looks similar to the original function. However, if BW << nF_{DOC}, peaking around nF_{DOC} occurs, where the function has a gain of 1. It should be noted that this peaking only occurs for $F_{IMDn}=|nF_{DOC}-F_{in}|$ and not for $F_{IMDp}=|nF_{DOC}+F_{in}|$. For low input frequencies, the IMD tones are filtered by an additional 20log(BW/(2F_{CH})) for the case of BW << nF_{DOC}. For the case of BW=2F_{CH}, this attenuation is 3 dB. At high frequencies, the original 20 dB/dec roll-off of H_{loop}/α is preserved for all the cases.

A chopper-stabilized amplifier can be made to be conditionally stable, with a two-pole roll-off for low frequencies and a single-pole roll-off for higher frequencies. Another option is to use hybrid-nested miller compensation with a 20dB/dec roll-off for the entire frequency range. The first

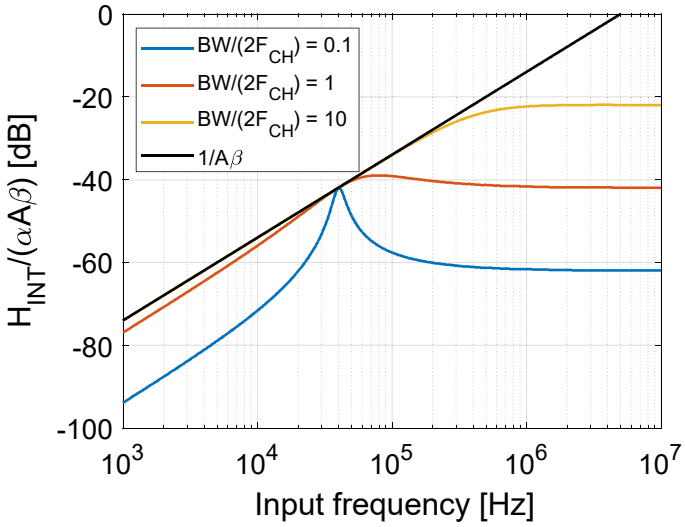

Fig. 2-17. $H_{loop}/(A\beta\alpha)$ as a function of input frequency for three different $BW/(2F_{CH})$ ratios and n=2.

option has a higher loop-gain at low frequencies, thereby improving the IMD. This is the case for all stabilized amplifiers presented in this thesis.

Overall, the open-loop IMD is shaped by the loop-gain and the filtering action of the loop, as shown in Fig. 2-17. This leads to an IMD vs input frequency that follows the loop-gain with either a 20dB/Dec or 40dB/Dec roll-off for low input frequencies, 20dB/Dec is depicted here. There is an additional suppression dependent on $BW/(nF_{CH})$. Based on the loop bandwidth, there is peaking around nF_{CH}, 40kHz in this case. Finally, there is a flat part where the -20 dB/Dec of the loop filter (H_{loop}/α) and the +20 dB/Dec of one over the loop gain ($1/A\beta$) cancel. The level of the IMD tones in the flat part can be calculated by considering the loop-gain at the BW of the stabilization loop ($A\beta(BW)$). At high frequencies above the second pole of the main amplifier, the open-loop IMD starts to roll-off, which is not shown in the figure.

In conclusion, it is advantageous for both low and high-frequency input frequencies to have a small stabilization loop bandwidth. However, the peaking at nF_{CH} always means that the IMD is limited to $IMD_{OL}/A\beta$.

2.5 Conclusion about intermodulation distortion

Both chopping and autozeroing can generate IMD tones, which appear in-band for $F_{IN}>F_{CH}$ and $F_{IN}>F_{AZ}/2$, respectively. Auto-zero amplifiers can only achieve decent IMD when the input signal is not sampled together with the offset, as is the case in the ping-pong topology. This only leaves the incomplete settling between the two phases as a possible source of IMD, which can be addressed with proper settling phases [2.2].

Chopping suffers from IMD due to limited bandwidth. For a two-stage amplifier, the closed-loop IMD improves by a factor of the loop-gain. For a stabilized amplifier, the integrator's filtering helps lower the high-frequency IMD tones. However, the low-frequency IMD tones are still limited to the open-loop IMD divided by the loop-gain. To improve the closed-loop IMD over the entire frequency range, increasing the loop-gain helps. However, this comes with a significant power increase. Ultimately, the best approach would be to improve the open-loop IMD. One way of achieving this will be presented in Chapter 6.

2.6 References

[2.1] J. Xu, Q. Fan, J. H. Huijsing, C. Van Hoof, R. F. Yazicioglu and K. A. A. Makinwa, "Measurement and Analysis of Current Noise in Chopper Amplifiers," in IEEE Journal of Solid-State Circuits, vol. 48, no. 7, pp. 1575-1584, July 2013.

[2.2] M. A. P. Pertijs and W. J. Kindt, "A 140 dB-CMRR Current-Feedback Instrumentation Amplifier Employing Ping-Pong Auto-Zeroing and Chopping," in IEEE J. of Solid-State Circuits, vol. 45, no. 10, pp. 2044-2056, Oct. 2010.

Chapter 3
A Digitally-assisted AZ Stabilized amplifier [1]

3.1 Introduction

This chapter presents an auto-zero stabilized voltage buffer that achieves a combination of low input current, low offset and low noise. It has an input current of 0.8 pA, state-of-the-art offset (0.4 μV) and a low-frequency noise density close to √2× its white noise density (14 nV/√Hz), which is the fundamental limit of an AZ amplifier [3.20].

The rest of the chapter is organized as follows. The chosen architecture and its design considerations are described in Section 3.2. Measurement results are shown and discussed in Section 3.3, and the chapter ends with conclusions.

[1] This chapter is based on: T. Rooijers, J. H. Huijsing and K. A. A. Makinwa, "An Auto-Zero-Stabilized Voltage Buffer With a Quiet Chopping Scheme and Constant Sub-pA Input Current," in IEEE Journal of Solid-State Circuits, vol. 57, no. 8, pp. 2438-2448, Aug. 2022.

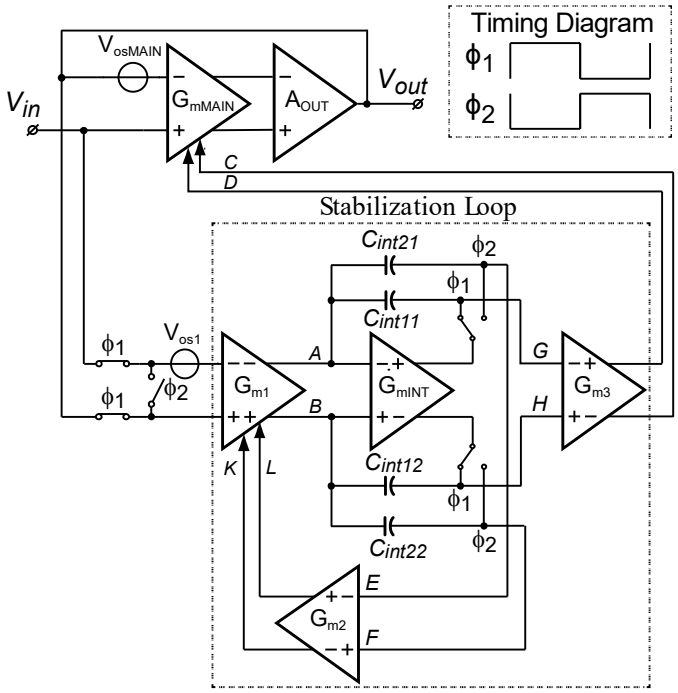

Fig. 3-1. Simplified block diagram of an auto-zero stabilized voltage buffer.

3.2 Amplifier architecture

A simplified schematic of the proposed auto-zero (AZ) stabilized buffer is shown in Fig. 3-1. It consists of a 3-stage buffer with a folded-cascode input stage (G_{mMAIN}), a folded-cascode intermediate stage with Class AB output stage (A_{OUT}), nested Miller compensation (30 pF and 7 pF, not shown) and Miller-zero compensation resistors (6 kΩ and 8 kΩ, not shown). The offset of the main amplifier (V_{osMAIN}) and 1/*f* noise are periodically canceled by an AZ stabilization loop consisting of an active integrator (G_{mINT}, $C_{int11-12}$ and $C_{int21-22}$) and two OTAs: G_{m1} and G_{m3}.

During phase ϕ_2, G_{m1} is auto-zeroed. Its input is shorted, and so its offset is converted by its transconductance (~230 µS) into an output current. This is integrated on capacitors $C_{int21-int22}$ (10 pF each), leading to a correction voltage across nodes E and F. G_{m2} then converts this into a correction current that cancels V_{os1}.

Due to negative feedback, the buffer's offset appears across its input terminals. During phase ϕ_1, this is sensed by G_{m1}. Its output current is then

integrated on capacitors $C_{int11\text{-}int12}$ (10 pF each), resulting in a correction voltage across nodes G and H, and a corresponding cancellation current generated by G_{m3}. To achieve sub-μV offset, while generating correction voltages of several hundred millivolts, each stabilization loop should have a high (>120 dB) gain. In this work, this is realized by multiplexing a single gain-boosted OTA (G_{mINT}) between the two loops, each with their own integration capacitors.

3.3 Noise Folding in Auto-Zero Amplifiers

The main drawback of auto-zeroing is that it causes under-sampled thermal noise to fold back to low frequencies [3.19]. As a result, the low-frequency (LF) noise density *after* auto-zeroing is typically larger than the original thermal noise density. The amount of noise folding is determined by the ratio of the bandwidth of the auto-zeroing loop (BW_{AZ}) and the auto-zeroing frequency (f_{AZ}). To achieve low input current, f_{AZ} should be as low as possible, i.e. somewhat higher than the $1/f$ corner frequencies of G_{m1} and G_{mMAIN}.

During the AZ phase ϕ_2, BW_{AZ} is given by [3.20],

$$BW_{AZ} = \frac{G_{m2}}{2\pi C_{int21\text{-}int22}} \tag{3-1}$$

where G_{m2} is the transconductance of G_{m2} and $C_{int21\text{-}int22}$ are the individual values of the corresponding integration capacitors. During phase ϕ_1, BW_{AZ} is determined by the transconductances of G_{mMAIN}, G_{m1} and G_{m3}. To equalize their noise contributions, the transconductances of G_{mMAIN} and G_{m1} are made the same, as are the transconductances of G_{m2} and G_{m3}. In this case, the bandwidth of the AZ loop can be expressed as:

$$BW_{AZ} = \frac{G_{m3}}{2\pi C_{int11\text{-}int12}} \tag{3-2}$$

where G_{m3} is the transconductance of G_{m3} and $C_{int11\text{-}int12}$ are the values of the corresponding integration capacitors.

Limiting the bandwidth of the stabilization loop, therefore, requires either large integration capacitors or small transconductances (G_{m2} and G_{m3}). The latter approach is the most attractive since it has the least impact on chip area. In a well-optimized design, the buffer's input-referred voltage noise density will then be determined by G_{mMAIN} (=G_{m1}), and so for a given integration capacitance, the low-frequency noise density due to folding will be inversely

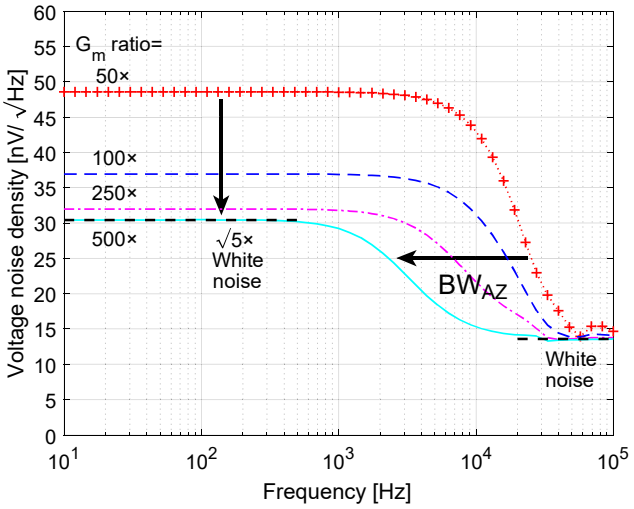

Fig. 3-2. Simulated voltage noise densities for a fixed f_{AZ} = 15kHz and different transconductance (G_m) ratios of G_{m1} & G_{mMAIN} and G_{m2} & G_{m3}, respectively (50×, 100×, 250× and 500×).

proportional to the G_m ratio $\alpha = G_{mMAIN}/G_{m3}$ (= G_{m1}/G_{m2}).

Fig. 3-2 shows the simulated input-referred voltage noise density of the buffer for a fixed G_{mMAIN} (=230 µS), integration capacitors (10 pF) and f_{AZ} =15 kHz but different gm ratios. As the gm ratio increases, the bandwidth BW_{AZ} decreases, the noise folding decreases, as does the voltage noise density at low frequencies. At large G_m ratios, however, the voltage noise density eventually stops decreasing and converges to a limit. As will be shown later, this limit is equal to $\sqrt{5}\times e_n$, where e_n is the voltage noise density associated with G_{mMAIN}. From Fig. 3-2, it can be seen that the gm ratio has to be at least 500× to reach this limit.

3.4 Digitally-Assisted Auto-Zero-Stabilized Loop

Using a gm ratio of 500× means that the combined offset of G_{mMAIN} and G_{m1} will be amplified by 500× at the output of the integrator. The maximum offset voltage that can be corrected by the stabilization loop is then limited to $V_{swing}/500$, where V_{swing} is the integrator's maximum output swing. In this work, $V_{swing} \sim \pm 0.6$ V, which corresponds to a maximum correctable

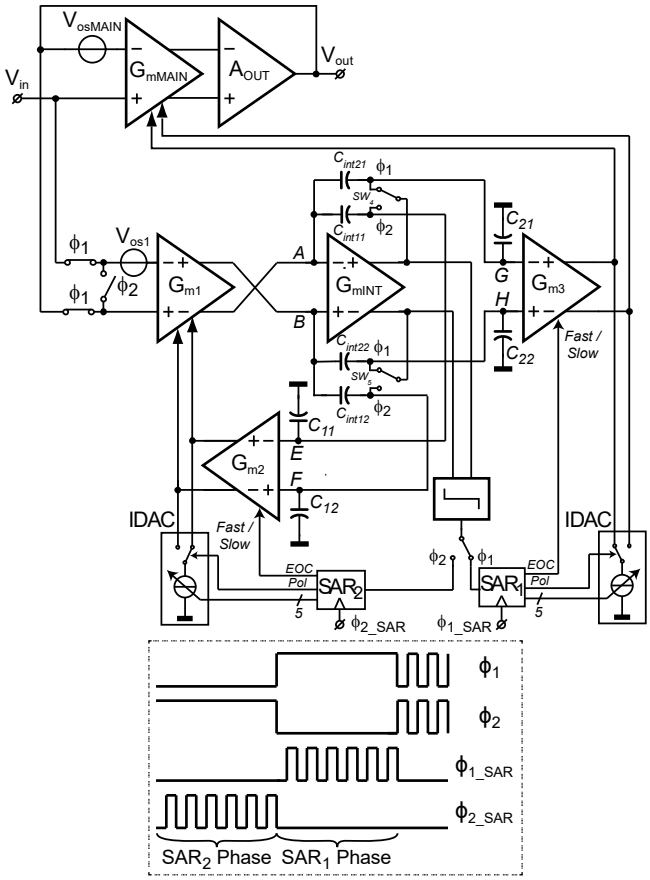

Fig. 3-3. Digitally-Assisted Auto-Zero-Stabilized Loop.

offset voltage of ±1.2 mV. From Monte-Carlo simulations, however, the expected offsets of G_{m1} and G_{mMAIN} are about 1.8 mV (6σ). On top of this, offset drifts of several hundreds of µVs may be expected over the intended operating temperature range (-40 to 85 °C) [3.11].

In prior work [3.20], an additional g_m stage driven by a voltage derived from an on-chip bandgap reference was used in order to trim the initial offset. In [3.21], a digitally-assisted calibration loop is used to lower the ripple of a chopper amplifier. In this work a similar approach is used, where the initial offset of both G_{mMAIN} and G_{m1} is trimmed at startup by a digital AZ loop, to handle worst-case offset and drift levels. As shown in Fig. 3-3, this consists of a comparator, a successive approximation register (SAR) and two current DACs (IDACs) in parallel with the outputs of G_{m2} and G_{m3}. At start-up, G_{m1}

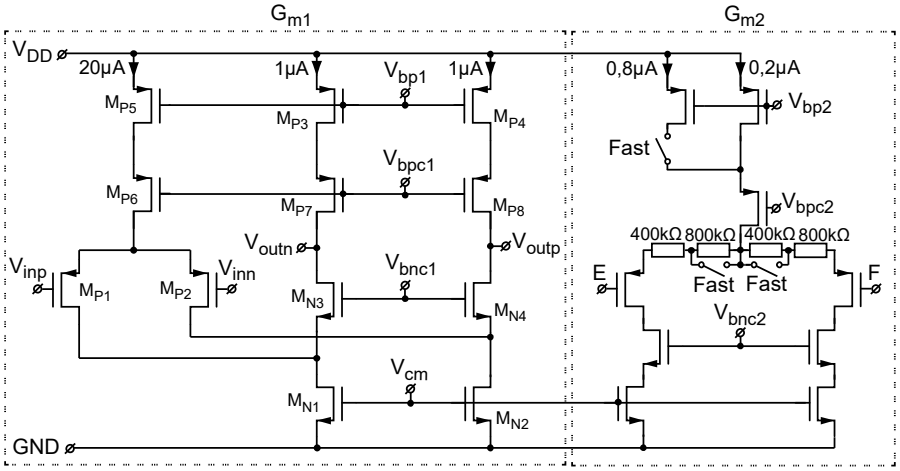

Fig. 3-4. Simplified schematic of G_{m1}/G_{mMAIN} and G_{m2}/G_{m3}

is first auto-zeroed by shorting its inputs and using a comparator to sample the integrator output and thus detect its offset polarity. This information is used to update the SAR, whose output drives the IDAC. Next, G_{mMAIN} is auto-zeroed in the same way by sensing its offset at the input of G_{m1} due to the feedback. As a result, the stabilization loop only has to cancel the offset drift and the residual offset corresponding to the LSB of the IDAC.

To ensure fast settling after each bit trial, the auto-zeroing bandwidth BW_{AZ} is temporarily increased. This is achieved by increasing the transconductances of G_{m2} and G_{m3} by ~4× during the operation of the digital AZ loop. This is implemented by switching both the bias current and the degeneration of G_{m2} and G_{m3} (Fig. 3-4). After the SAR bits are fixed, BW_{AZ} is decreased (via the end of conversion (EOC) bit) and the analog stabilization loop is enabled.

For robustness, the 5-bit IDAC is slightly over-designed, with the maximum current of 1 µA corresponding to an offset of 4.3 mV. Its MSB then corresponds to an offset of 2.5 mV, while its LSB corresponds to roughly 150 µV. A polarity bit is used to steer the DAC current to the appropriate output, and thus compensate for both positive and negative offsets.

Since the offsets of G_{m1} and G_{mMAIN} are amplified by the G_m ratio, the offset of the comparator can be quite relaxed. During startup, the G_m ratio is about 120, which means that the LSB of the IDAC corresponds to an integrator output of 18 mV. This is much greater than the simulated comparator offset

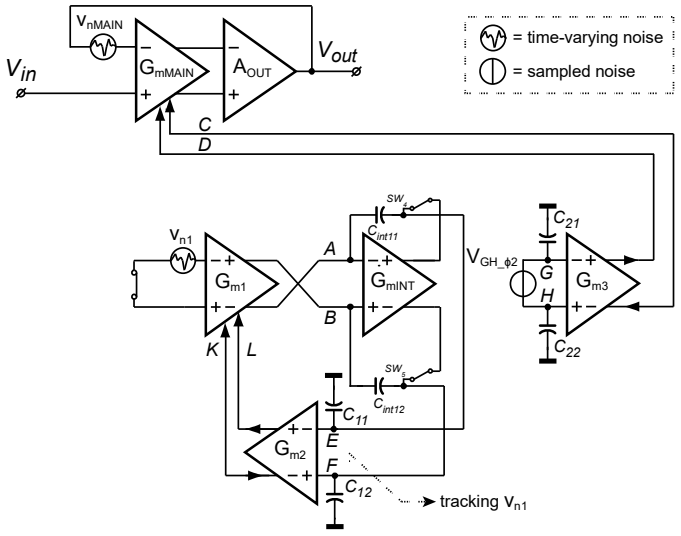

Fig. 3-5. Noise sources of the auto-zero stabilized voltage buffer in phase ϕ_2

(5 mV).

A further benefit of the digital AZ loop is that it reduces the amplitude of the switching spikes associated with the multiplexed operation of the integrator. It does this by reducing the integrator's output swing, which in turn, reduces the charge injection mismatch of its output switches. It also reduces the transient currents required to drive the integrator's load capacitors to the two different offset levels of G_{m1} and G_{mMAIN}. Due to the 500× G_m ratio, any spikes that still appear on nodes G and H will be attenuated by 500× when referred to the output.

3.5 Low-Frequency Noise Analysis

As shown in Fig. 3-2, even after minimizing BW_{AZ}, the LF noise density is still limited to about √5× the white noise level, which is higher than the √2× fundamental limit. To understand the reasons for this, in this section, the proposed amplifier's LF noise performance will be analyzed. At first, it will be assumed that all noise sources are uncorrelated. All noise sources refer to voltage noise densities, and capitalization will be used to denote sampled sources, while lowercases will be used for time-varying sources.

In phase ϕ_2 (Fig. 3-5), the input of G_{m1} is shorted and the voltage across nodes E and F tracks the (500× amplified) offset. It also tracks the noise of

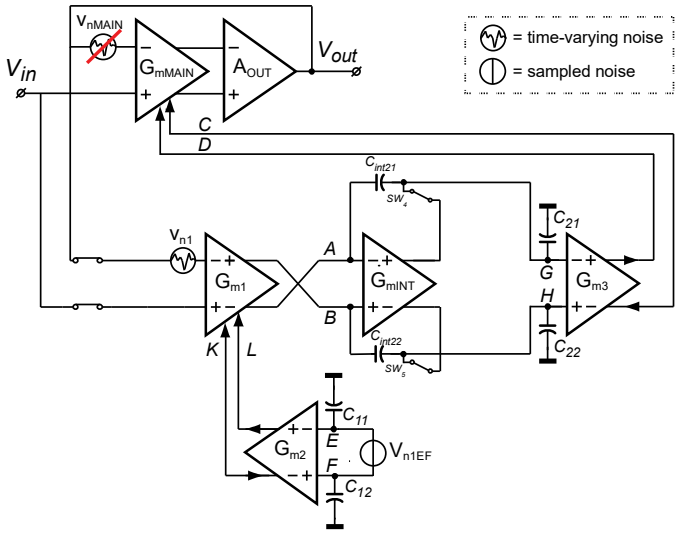

Fig. 3-6. Noise sources of the auto-zero stabilized voltage buffer in phase ϕ_1

G_{m1} (v_{n1}). At the end of phase ϕ_2, this noise will be sampled across E and F (V_{n1EF}) and held there during the following ϕ_1 phase.

In phase ϕ_1 (Fig. 3-6) the voltage across node G and H tracks and cancels the noise of G_{mMAIN} (v_{nMAIN}), in the same way as its offset. This is done by G_{m1}, whose offset is still being nulled by the voltage across E and F. This means that the voltage across G and H is the sum of the voltage needed to track the time-varying noise sources v_{nMAIN} and v_{n1}, and the sampled noise from E and F (V_{n1EF}), which are both amplified by α. As a result, the noise density across G and H during phase ϕ_1 can be expressed as:

$$v_{GH\_\phi1} = \alpha\sqrt{v_{nMAIN}^2+v_{n1}^2+V_{n1EF}^2}. \tag{3-3}$$

Assuming that the AZ stabilized loop has enough gain, it will completely cancel the LF noise of G_{mMAIN}, and so during ϕ_1 the buffer's output-referred noise density, referred to V_{out}, will be given by:

$$v_{out\_\phi1} = \sqrt{v_{n1}^2+V_{n1EF}^2}=\sqrt{2}e_n. \tag{3-4}$$

This shows that in phase ϕ_1 the buffer's LF output-referred noise density is fully determined by the noise of G_{m1}, which is also in good agreement with the results of Pnoise simulations.

In phase ϕ_2 (Fig. 3-5), the noise across G and H due to the contributions of v_{nMAIN}, v_{n1} and V_{n1EF} will be frozen. This leads to a total noise density across G and H during phase ϕ_2 of:

$$V_{GH\_\phi2} = \alpha\sqrt{V_{nMAINGH}^2+V_{n1GH}^2+V_{n1EF}^2} \tag{3-5}$$

, where $V_{nMAINGH}$ and V_{n1GH} are the sampled noise sources across G and H from v_{nmain} and $v_{n1,}$ respectively. Referred to the buffer's output, these contributions across G and H add to the noise v_{nMAIN}, and so the buffer's output-referred noise density in phase ϕ_2 is given by:

$$v_{out\_\phi2}=\sqrt{v_{nMAIN}^2+V_{nMAINGH}^2+V_{n1GH}^2+V_{n1EF}^2}=2e_n. \tag{3-6}$$

This result shows that in phase ϕ_2 the buffer's LF output-referred noise is equally determined by G_{m1} and G_{mMAIN}, which is also supported by the result of Pnoise simulations.

If phase ϕ_1 and ϕ_2 have a 50% duty-cycle, then the buffer's output noise over the two phases is the average of their respective noise contributions. The buffer's output noise is therefore determined by the average of (3-4) and (3-6) and is given by:

$$v_{out}=\sqrt{\frac{1}{2}\left(v_{out\_\phi1}^2+v_{out\_\phi2}^2\right)}. \tag{3-7}$$

Filling-in the earlier expressions for the output noise in phase ϕ_1 (3-4) and ϕ_2 (3-6) gives an output noise of:

$$v_{out}=\sqrt{\frac{1}{2}\left(v_{nMAIN}^2 + V_{nMAINGH}^2 + v_{n1}^2 + V_{n1GH}^2 + 2V_{n1EF}^2\right)}. \tag{3-8}$$

Removing the distinction between sampled and time-varying noise, this can be simplified to:

$$v_{out}=\sqrt{v_{nMAIN}^2 + 2v_{n1}^2}=\sqrt{3}e_n. \tag{3-9}$$

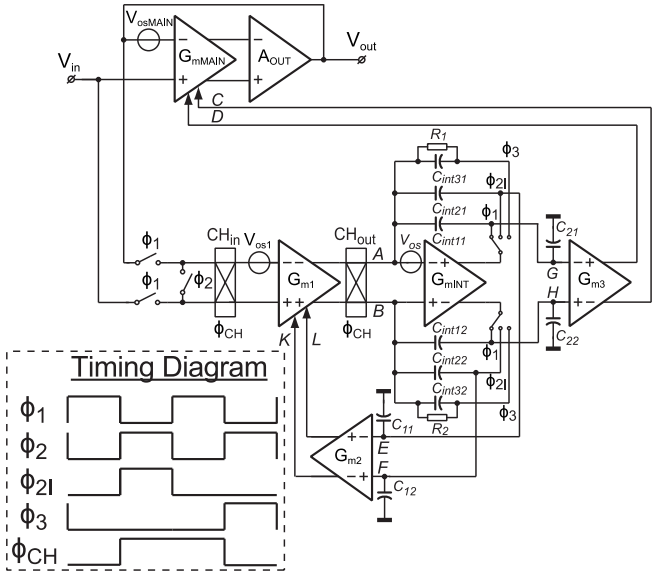

Fig. 3-7. Auto-zero-stabilized buffer with a chopped stabilization loop.

The final result in equation (3-9) shows that without correlation, the output noise will be $\sqrt{3}e_n$. However, V_{n1EF}, V_{n1GH} and $V_{nMAINGH}$ in equation (3-8) are sampled versions of v_{n1} and v_{nMAIN}, which leads to a partial correlation. Pnoise simulations show that these correlations increase the noise to $\sqrt{5}e_n$.
Based on this LF analysis, there are two possible ways to further reduce the total LF noise. One is to remove the dominant V_{n1EF} term in (3-8), the other is to extend phase ϕ_1 relative to phase ϕ_2, noting that the output noise in phase ϕ_1 (3-4) is much lower than phase ϕ_2 (3-6). These two approaches will be further explored in the following sections.

3.6 Chopped Stabilization Loop

To remove the V_{n1EF} term in (3-8), V_{n1EF} should not be allowed to propagate to G & H, and eventually to the output, in the same way during the two phases.

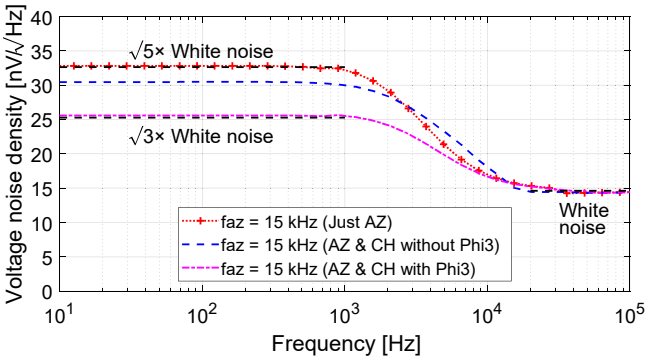

Fig. 3-8. Voltage noise density simulation for different configurations (AZ, AZ&CH without and with ϕ_3).

To achieve this, a chopper placed between nodes E & F and G & H (CH_{out} in Fig. 3-7) is used to periodically invert the polarity of the V_{n1EF} on its way to nodes G and H in phase ϕ_1. In this way, V_{n1EF} will reach the output with opposite polarities and thus cancel over one chopping period. In this case, the output noise would be given by:

$$v_{out}=\sqrt{\frac{1}{2}\left(v_{nMAIN}^2 + V_{nMAINGH}^2 + v_{n1}^2 + V_{n1GH}^2\right)} = \sqrt{2}e_n. \qquad (3\text{-}10)$$

Where the partial correlation still exists between V_{n1GH} and v_{n1} as well as $V_{nMAINGH}$ and v_{nMAIN}. Pnoise simulations show that for a 50% duty-cycle, the partial correlation limits the noise floor to about $\sqrt{3}e_n$. To preserve the correct loop polarity, a second Chopper CH_{in} is inserted at the input of G_{m1}. This chopper is switched in phase ϕ_2 when it is disconnected from the input by the AZ switches. This prevents its switching activity from generating transients, and thus introducing spikes in the amplifier's input current.

One issue is that the AZ loop is still active in between the two chopping phases. Therefore, V_{n1EF} will slowly change during chopping and so will not be perfectly canceled. The amount of change depends on the duration of the chopping period and hence on the AZ frequency f_{AZ}. Setting f_{AZ} = 15 kHz, which is enough to cancel the buffer's 1/*f* noise, only reduces the LF noise floor slightly (Fig. 3-8). To approach the $\sqrt{3}\times e_n$ limit, simulations show that f_{AZ} would have to be some 3× higher, resulting in significantly more input switching, and hence, more input current.

To preserve the noise across nodes E and F during a chopping period, extra capacitors $C_{int31\text{-}int32}$ (1 pF each) are used to implement a modified ϕ_2 phase, denoted by ϕ_3 (Fig. 3-7). During ϕ_3, the output of G_{mINT} is not connected to either AZ loop. Also, resistors $R_{1\text{-}2}$ (2 MΩ) limit the gain of G_{mINT}, preventing it from clipping due to the residual output current of G_{m1}. V_{n1EF} can then be fully chopped-out without changing f_{AZ} (Fig. 3-8). The chopping transitions are arranged to occur in phase ϕ_2, when the input chopper is disconnected from the input by the AZ switches. With these two measures, the AZ stabilization loop can be chopped, lowering the LF noise to $\sqrt{3}e_n$, without introducing extra spikes or input current.

Another issue is the integrator's own offset, which, via the chopper at its input, gives rise to a square-wave ripple voltage at the output of G_{m1}. This will be translated into a ripple voltage at the input of the buffer ripple voltage by dividing it by the transconductance and finite output impedance at f_{ch} of G_{m1}. With an expected integrator offset of about 2 mV, the output impedance of G_{m1} then needs to be quite high (>150 MΩ) to ensure that the resulting ripple is negligible (<100 nV). This requirement is met by implementing G_{m1} as a folded cascode OTA.

3.7 Duty-Cycling the AZ clock

With the V_{n1EF} term removed, the buffer's LF noise level can be further reduced by adjusting the ϕ_1:ϕ_2 duty-cycle. From the noise analysis, we can note that the output noise in phase ϕ_1 ($\sqrt{2}\times e_n$) is less than the noise in phase ϕ_2 ($2\times e_n$). The correlation will also be affected by the duty-cycle, and the more time the buffer spends in phase ϕ_1, the lower the noise gets. Since some settling time is required for ϕ_2, the resulting noise level in Pnoise simulations will then be somewhere between $\sqrt{3}\times e_n$ and $\sqrt{2}\times e_n$.

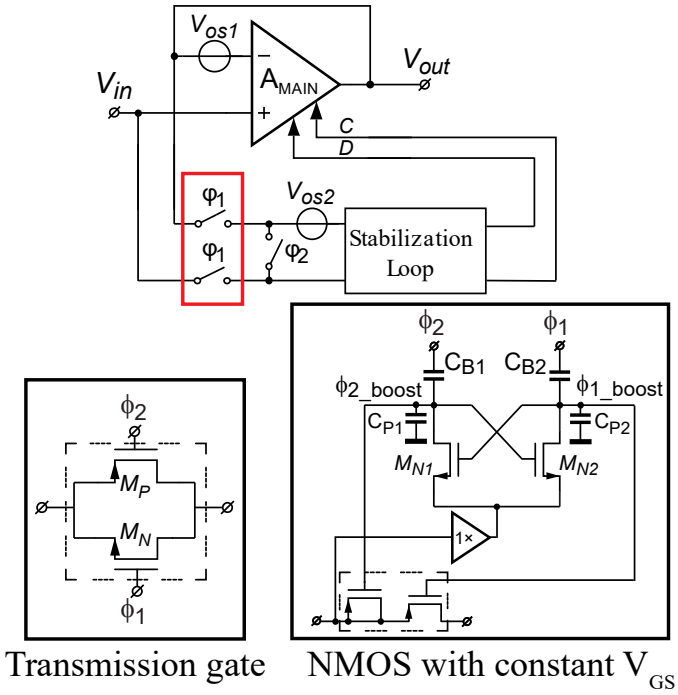

Fig. 3-9. Two implementations of the AZ switches. Transmission gates and NMOS switches with a constant Vgs drive.

3.8 Implementation of the AZ Switches

The input current of the AZ amplifier is determined by the charge injection mismatch of the two input switches driven by ϕ_1 (Fig. 3-9). Two implementations of the AZ switches were tested and compared: transmission gate switches [3.17] and NMOS switches with a constant V_{GS} drive [3.18]. The constant V_{GS} drive consists of two latching transistor M_{N1} and M_{N2} which pre-charges boosting capacitors C_{B1} and C_{B2} to the input voltage. A fraction of the clock signal is then boosted on top of this to get a V_{GS} driving the switches that is independent of the input voltage. The amplitude of the resulting clock signal $\Phi_{1,2\_boost}$ is determined by the ratio of the boosting capacitor ($C_{B1\text{-}B2}$) to the parasitic capacitance to ground ($C_{P1\text{-}P2}$). A simple buffer is used to make sure that the constant V_{GS} drive switching is not loading the input.

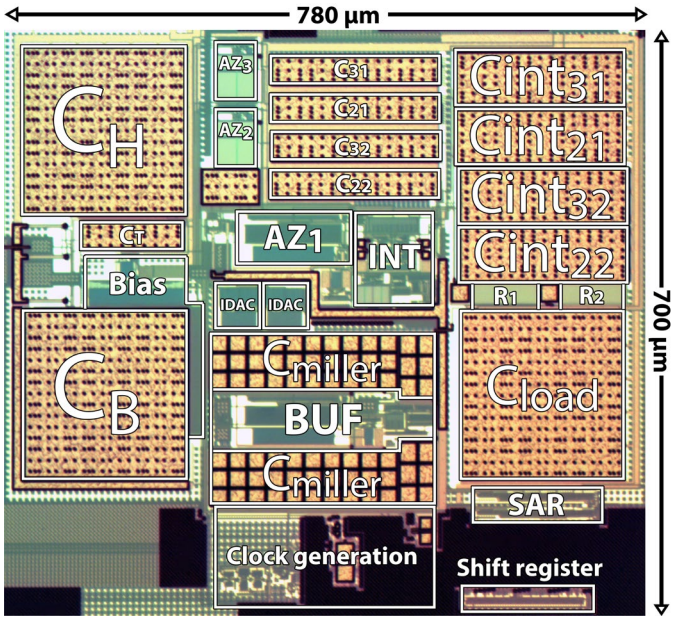

Fig. 3-10. Chip Micrograph of the Auto-Zero-Stabilized Voltage Buffer.

3.9 Measurement Results

The auto-zero-stabilized buffer was realized in a 0.18 µm CMOS technology (Fig. 3-10). It draws 210 µA from a 1.8 V supply and has an active area of 0.55 mm^2, 0.12 mm^2 of which is occupied by the low-leakage S&H circuit.

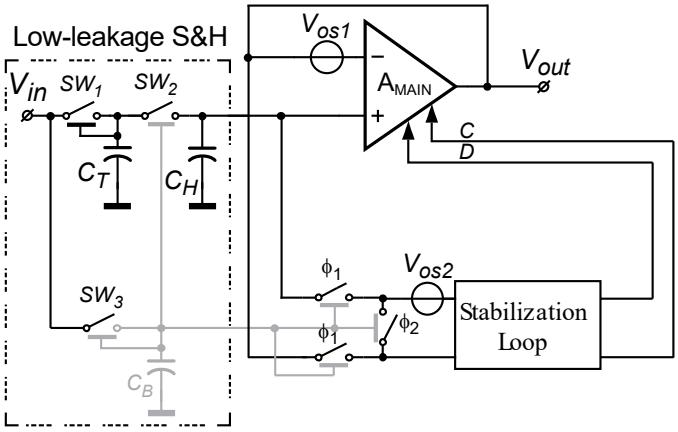

Fig. 3-11. Low-leakage S&H used to evaluate the input current.

3.10 Measuring the Input Current

To evaluate the extremely low input current of the buffer, a circuit similar to the sampled voltage reference is used (Fig. 3-11). An on-chip hold capacitor C_H (36 pF) is pre-charged to an input voltage through a low-leakage sampling network consisting of switches $SW_{1,2}$. The input is then disconnected and the voltage drift over time of the hold capacitor is observed to deduce the input current.

To minimize the leakage of the sampling switch, extra hold capacitors C_T (3 pF) and, via SW_3, C_B (36 pF) ensure that thechannel and body-diodes of SW_2 are operated at zero reverse bias. The same technique is applied to G_{m1}'s input switches $SW_{4\text{-}6}$, as the body diode leakage of these switches would cause the hold capacitor to discharge. All capacitors are implemented with custom MOM capacitors to minimize their leakage.

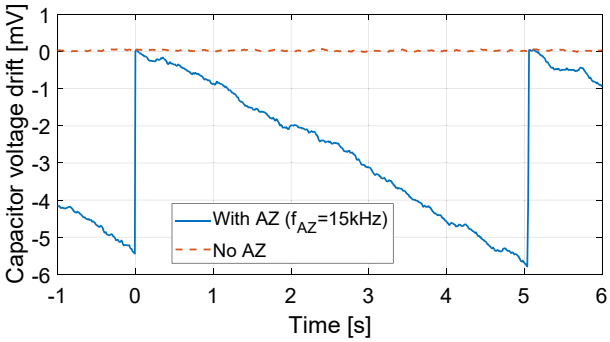

Fig. 3-12. The capacitor voltage drift with and without AZ & CH.

The voltage drift across C_H is shown for a typical sample with a 1 V input (Fig. 3-12). With AZ off, there is negligible leakage, illustrating the effectiveness of the low-leakage techniques.

The voltage drift across CH is an accurate measure of the buffer's input current. In a general-purpose buffer, another challenge, when interfacing off-chip sensors, is the leakage of the ESD devices, which is usually >1pA. To suppress this leakage, special bootstrapped ESD structures can be used [3.22]. These protection devices are outside the scope of this work. Instead, this paper focuses on showing that the input current of an AZ amplifier can be reduced to the sub-pA level.

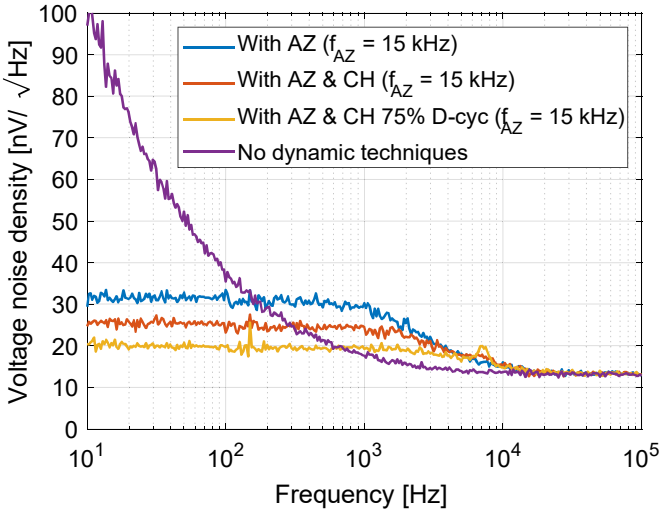

Fig. 3-13. Measured voltage noise density vs frequency for different scenarios.

3.11 Voltage Noise Density

With all dynamic techniques turned off, at low-frequencies, the 1/*f* noise can be seen with a corner frequency of about 700 Hz (Fig. 3-13). At higher frequencies, the white noise level can be seen with a level of 14 nV/√Hz. With auto-zeroing only, a low-frequency noise density of 31 nV/√Hz is achieved, which equals the earlier discussed √5× white noise. When chopping with the extra Φ_3 phase enabled, the low-frequency noise drops to 25 nV/√Hz, which equals the √3× white noise. Finally, when a 75% duty-cycle is used, a low-frequency noise of 20 nV/√Hz is achieved, which is very close to the √2× noise limit. This reduction from √5× to √2× noise corresponds to a 2.5× power saving in the input stages. All the noise reduction techniques lead to a competitive NEF of 7.3, due to the low increase in noise floor over a small bandwidth, which leads to an NEF that even outperforms even many chopper amplifiers. No tones at f_{AZ} or f_{CH} can be seen, demonstrating that the use of auto-zeroing and chopping does not add spikes and a quiet output is achieved.

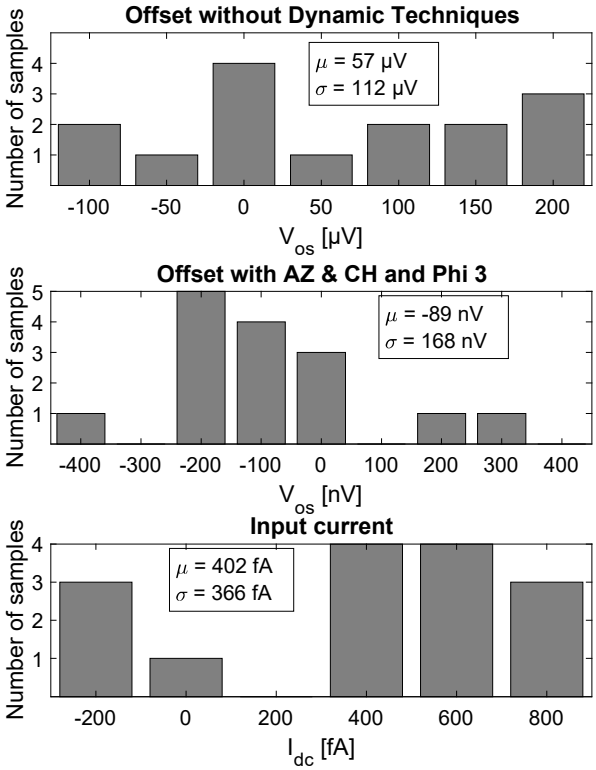

Fig. 3-14. Histograms (15 samples) of the measured offset (without and with AZ) and input current with AZ&CH and ϕ_3 (f_{AZ} = 15 kHz, Vin = 1V).

3.12 Offset and Input current

To evaluate the offset and the input current of the buffer measurements were done on 15 samples (Fig. 3-14). Without any dynamic techniques, the offset is below 200 μV. When all the dynamic techniques are switched on the offset is reduced to a maximum value of 0.4 μV. Finally, the input current

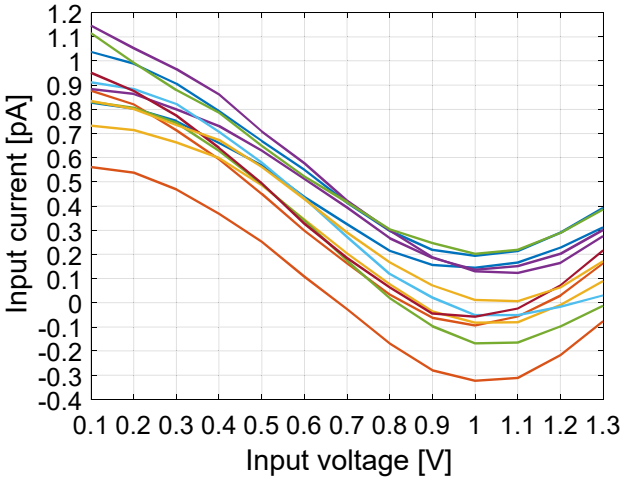

Fig. 3-15. Input current vs input voltage for transmission gate switches.

with all dynamic techniques and NMOS input switches with a constant V_{GS} drive has a maximum value of 0.8 pA. The 75% duty-cycle of AZ clock does not change the offset or input current performance. The low input current of this design can be attributed to several design choices. First, auto-zeroing is used instead of chopping, so that the input current only depends on the CI mismatch of one pair of switches. Making f_{AZ} low (15 kHz) also lowers the input current. The additional chopping is done during auto-zeroing phases, and so does not increase the input current. Finally, compared to most prior art [3.5]-[3.7], the use of finer technology (180nm) allows the use of smaller switches with less CI. In general, for a given minimum dimension L, CI scales with L^2, while CI mismatch scales with L [3.23].

For the two implementations of the AZ switches the input current vs input voltage was measured for up to 15 samples. The implementation with transmission gates shows a large variation of the input current vs input voltage changing up to 0.9 pA over the full range of the buffer (0.1 to 1.3 V) (Fig. 3-14).

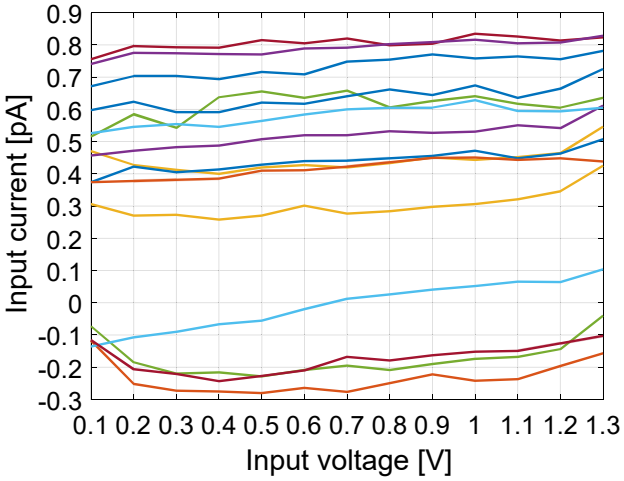

Fig. 3-16. Input current vs input voltage for NMOS with constant Vgs.

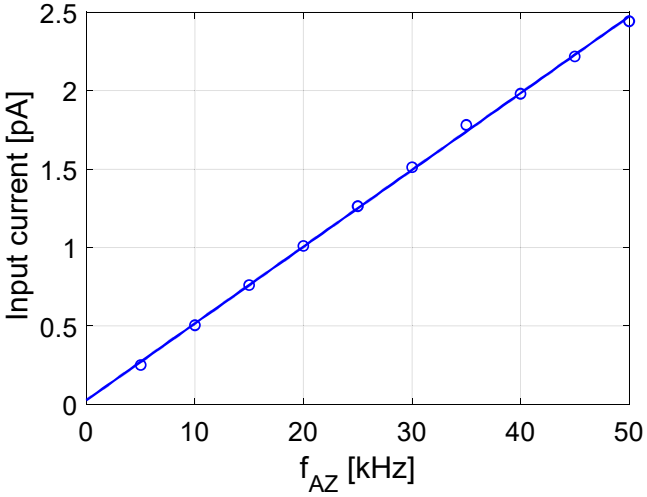

Fig. 3-17. Input current vs auto-zeroing frequency (f_{AZ}).

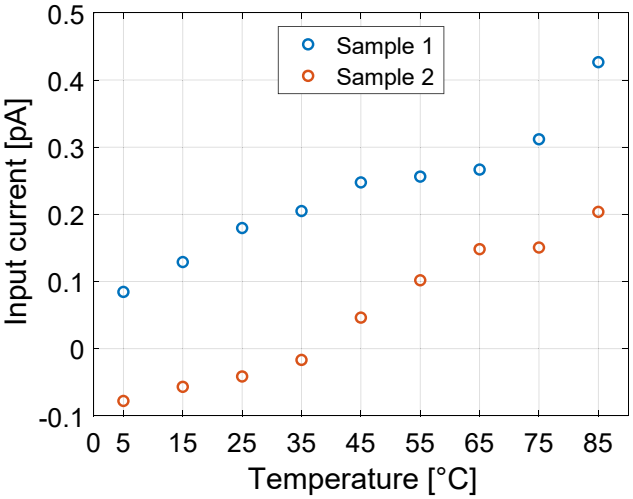

Fig. 3-18. Input current vs temperature for a fixed input voltage of 1V.

This change in input current can be attributed to the PMOS and NMOS being active for the different input voltages. For low input voltages, the charge injection of the NMOS is only contributing to the input current and for higher input voltages the PMOS is contributing. Around halfway the supply both switches will contribute which leads to a partial cancellation of the charge injection and therefore the lowest input current. The implementation of the NMOS switches with constant V_{GS} drive shows a much more constant input current over input voltage, where the worst-case sample changes around 0.2 pA (Fig. 3-16).

A measurement of the input current vs f_{AZ} shows a linear relationship (Fig. 3-17), that extrapolates to zero, which indicates that charge injection is the dominant source of input current.

The input current drift over temperature (from 5 °C to 85 °C) was characterized for two typical samples at a fixed input voltage of 1 V (Fig. 3-18). The input current drifts around 0.3 pA over 80 °C. This input current is still well below the expected ESD leakage. At higher temperatures a part of this drift can be attributed to the increased leakage of the S&H circuit.

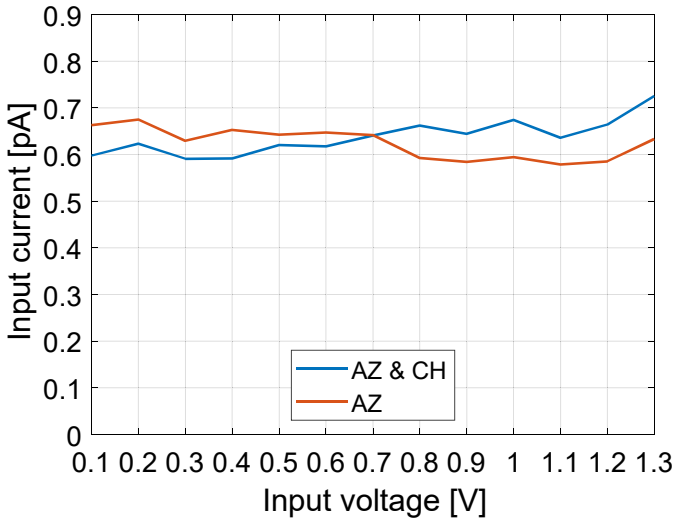

Fig. 3-19. Input current vs Input voltage for a typical sample in the case of AZ and AZ&CH.

The input current vs input voltage is also measured for the case of AZ and AZ & CH for a typical sample (Fig. 3-19). For both cases the input current is similar, showing that the chopping can be done without adding input current.

TABLE 3-I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART

	This work	Q. Fan [5]	Y. Kusuda [6]	A.T.K Tang [7]	M. A. P. Pertijs [20]	AD8551 [24]	S. Sakunia [25]
Dynamic technique(s)	**Auto-zeroing and Chopped Stabilization**	Chopping	Chopping	Chopping and Auto-zeroing	Chopping and Auto-zeroing	Auto-zeroing	Chopping and Auto-zeroing
Input current (Max)	**0.8 pA**	110 pA	72 pA	40 pA	-	50 pA	-
Offset (Max)	**0.4 µV**	1 µV	0.78 µV	3 µV	2.8 µV	5 µV	4 µV
Voltage noise (nV/√Hz)	**31 (AZ)** **25 (AZ&CH)** **20 (75% AZ&CH)**	10.5	5.9	20	38 (AZ) 27 (CH&AZ)	75	140 (AZ) 28 (CH&AZ)
GBW (MHz)	**1.45**	1.8	4	2.5	0.8	1	-
NEF	**7.3**	4.8	8.7	21.8	43.5	-	-
PSRR (dB)	**125**	120	142	-	138	130	128
Frequency (kHz)	**15 (f_{AZ}) / 7.5 (f_{CH})**	30	200	15 (f_{CH}) / 7.5 (f_{AZ})	28 (f_{AZ}) / 14 (f_{CH})	4	11 (f_{CH}) / 7.33 (f_{AZ})
Supply current	**210 µA**	143 µA	1.47 mA	800 µA	1.7 mA	750 µA	480 µA
Supply voltage	**1.8 V**	5 V	2.5 - 5.5 V	5 V	2.7 - 5.5 V	2.7 V	3.3 - 5.5 V
Technology	**0.18 µm**	0.7 µm	0.35 µm	0.6 µm	0.5 µm	-	0.5 µm
Die area (mm^2)	**1.4**	1.8	1.26	0.67	2.5	-	1.48

3.13 Comparison with the prior art.

In Table 3-I, the performance of the AZ Stabilized Voltage Buffer is summarized and compared with the state of the art. A 50× reduction in input current is achieved, while also achieving state-of-the-art offset (0.4 μV) and competitive LF voltage noise (20 nV/√Hz). The NEF of this AZ design is comparable with some CH amplifiers [6], due to the introduced LF noise reduction techniques.

3.14 Conclusions

An auto-zero-stabilized voltage buffer is presented that achieves a combination of low noise (20 nV/√Hz), low offset (0.4 μV max) and low input current (0.8 pA max). The elevated low-frequency noise density associated with auto-zeroing is minimized by using a combination of: a digitally-assisted AZ loop, chopping to remove correlation and an optimized duty-cycle for the AZ clock. This allows the buffer to reach a low-frequency noise density close to √2 times its white noise density (14 nV/√Hz), which is the fundamental limit of an AZ amplifier. This is the first design to demonstrate that dynamic offset correction techniques can be used to realize a buffer with both sub-pA input current and sub-μV offset.

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Chapter 4
An Auto-zero Stabilized Buffer with Trimmed Input Current[2]

4.1 Introduction

The design presented in Chapter 3 achieves state-of-the-art offset (< 1μV) and low-frequency noise performance (only √2× higher than the buffer's own thermal noise floor). However, the charge injection of its input switches gives rise to significant input current: up to 0.8pA. Since this current is relatively independent of input voltage, however, it can be effectively trimmed at a single input voltage.

This chapter presents the design and implementation of an input-current trimming scheme for auto-zero amplifiers. Since their input current is mainly due to charge injection, the scheme operates by trimming the clock swing, and hence the charge injection, of two dummy input switches. At room temperature, the trimming scheme reduces the maximum input current of an auto-zero stabilized voltage buffer from 1pA to 0.2pA (13 samples) over its full input voltage range (0 to 1.3V). This increases to 0.4pA over temperature (0 to 85°C), which is well below the leakage of typical ESD diodes, and is the lowest input current ever reported for an auto-zero amplifier.

The rest of the chapter is organized as follows. Details of the trimming scheme are described in Section 4.2. Measurement results are shown and discussed in Section 4.3, and the chapter ends with conclusions.

[2] This chapter is based on: T. Rooijers, J. H. Huijsing and K. A. A. Makinwa, "An Auto-Zero Stabilized Voltage Buffer with a Trimmed Input Current of 0.2pA," ESSCIRC 2019 - IEEE 45th European Solid State Circuits Conference (ESSCIRC), 2019, pp. 257-260.

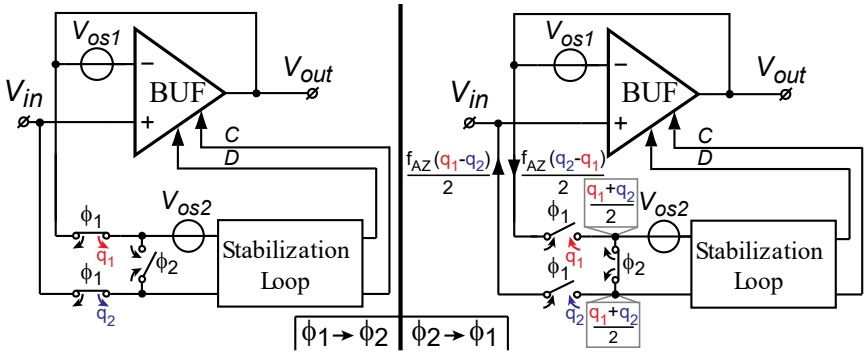

Fig. 4-1. Input current caused by charge injection mismatch of the AZ switches

4.2 Input current trimming scheme

The input network of the AZ stabilized buffer is shown in Fig. 4-1. The two main sources of offset are the offset of the buffer V_{os1}, and the offset of the stabilization loop V_{os2}. By appropriately configuring the three input switches, either V_{os1} can be sensed and auto-zeroed by the stabilization loop (phase Φ_1), or V_{os2} can be auto-zeroed by shorting the input of the stabilization loop (phase Φ_2). At the end of Φ_1, the Φ_1 switches turn off, while the Φ_2 switch turns on. As a result, most of the channel charge of the Φ_1 switches (q_1 and q_2) is absorbed by the Φ_2 switch. The charge injection mismatch of the Φ_1 switches, however, will divide equally between V_{in} and V_{out}, resulting in an input current $I = f_{AZ}(q_1-q_2)/2$.

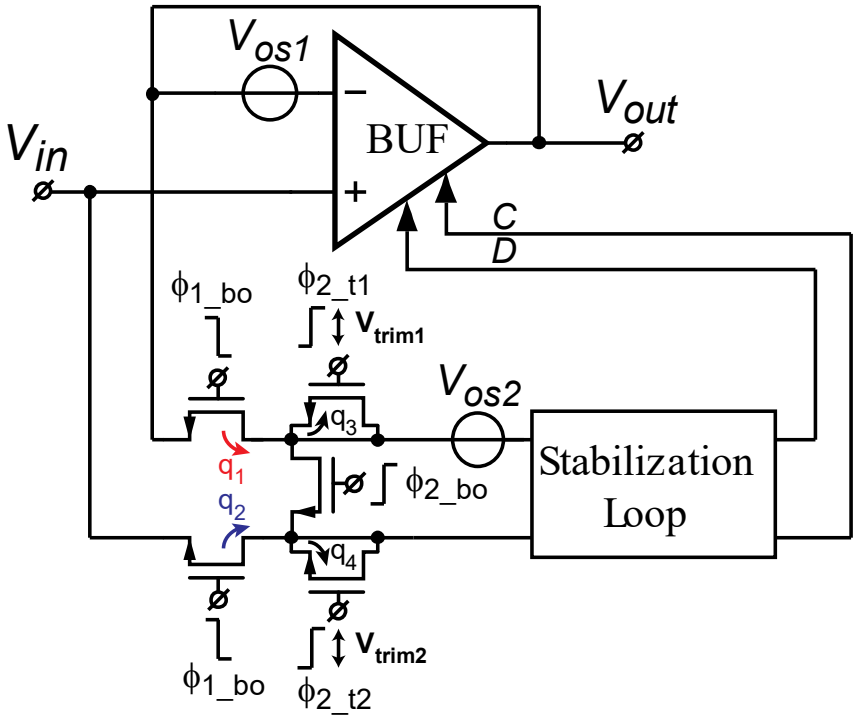

Fig. 4-2. Input current trimming using dummy switches with trimmed clock amplitudes.

In order to absorb this charge injection mismatch, dummy Φ_2 switches can be placed in series with the Φ_1 switches (Fig. 4-2). In this work, the charge these switches absorb (q_3 & q_4), and hence the input current, is made trimmable by including a circuit that adjusts the amplitude of the clock signals (V_{trim1} and V_{trim2}) applied to their gates.

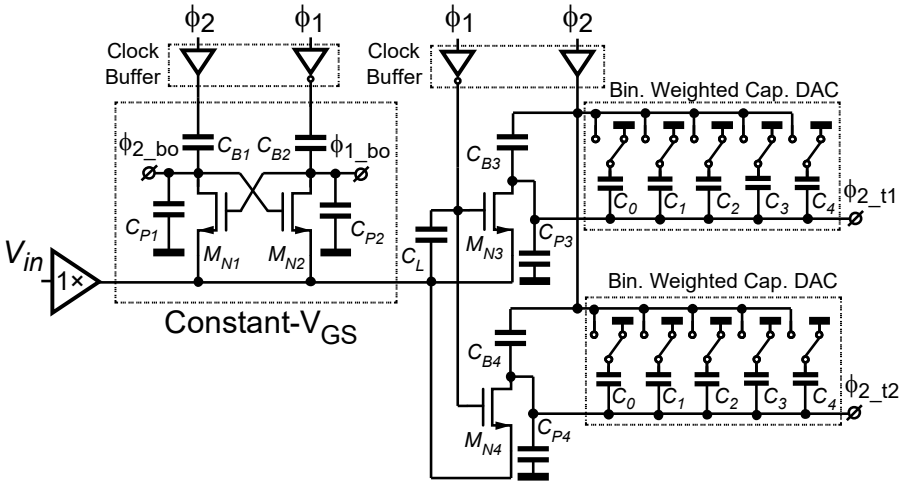

Fig. 4-3. Constant-V_{GS} drive with the trimming circuit for the clock amplitudes of the dummy switches

The main switches are driven by capacitively-coupled constant-V_{GS} drive circuits (Fig. 4-3), which effectively add a fraction of a 1.8V clock signal to a buffered version of V_{in}. The amplitude of the resulting clock signal $\Phi_{1,2\_bo}$ is determined by the ratio of the boosting capacitor ($C_{B1\text{-}B2}$) to the parasitic capacitance to ground ($C_{P1\text{-}P2}$). By adjusting this ratio via a capacitive DAC, a similar circuit can be used to adjust the amplitude of the clock signals $\Phi_{2\_t1,2}$ applied to the dummy switches. The DAC capacitors are always in parallel to either the boosting capacitor or the parasitic capacitor and thus are never floating.

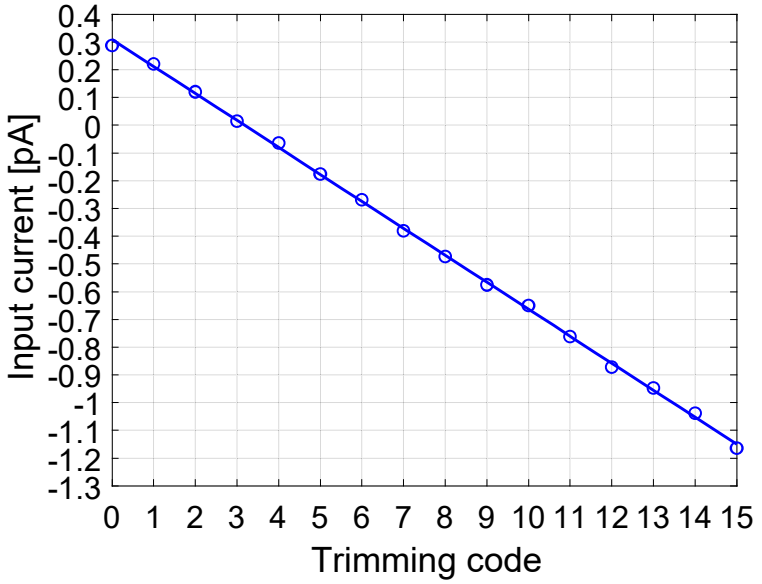

Fig. 4-4. Measured Input current vs Trimming code (4 bits) for a typical sample

The result is a very linear trimming characteristic, as can be seen from the measured input current vs trimming code (Fig. 4-4). From the work of chapter 3, the buffer's maximum input current is expected to be less than 1pA, and to vary by about 0.2pA over the buffer's input voltage range. A 4-bit binary weighted DAC with a 0.1pA LSB would then be sufficient to trim the input current. For near-minimum size dummy switches, this LSB corresponds to a 30mV change in clock amplitude, which can be achieved with a 40fF (minimum-size) LSB capacitor and a 1.1pF boosting capacitor. To ensure robustness to process spread, a 5-bit DAC was actually implemented.

To minimize power-supply spikes, the dummy switches are driven by Φ_1 and Φ_2 clock signals provided by a current-mode logic (CML) buffer. From Fig. 4, however, it can be seen that the trim DACs only load the CML buffer's Φ_2 output. To avoid generating asymmetric Φ_1 and Φ_2 clock signals, which would also cause current spikes in the buffered V_{in}, a dummy load capacitor (C_L) is also used on the Φ_1 side. Its value is roughly equal to the trim DAC capacitance at the mid-range DAC code.

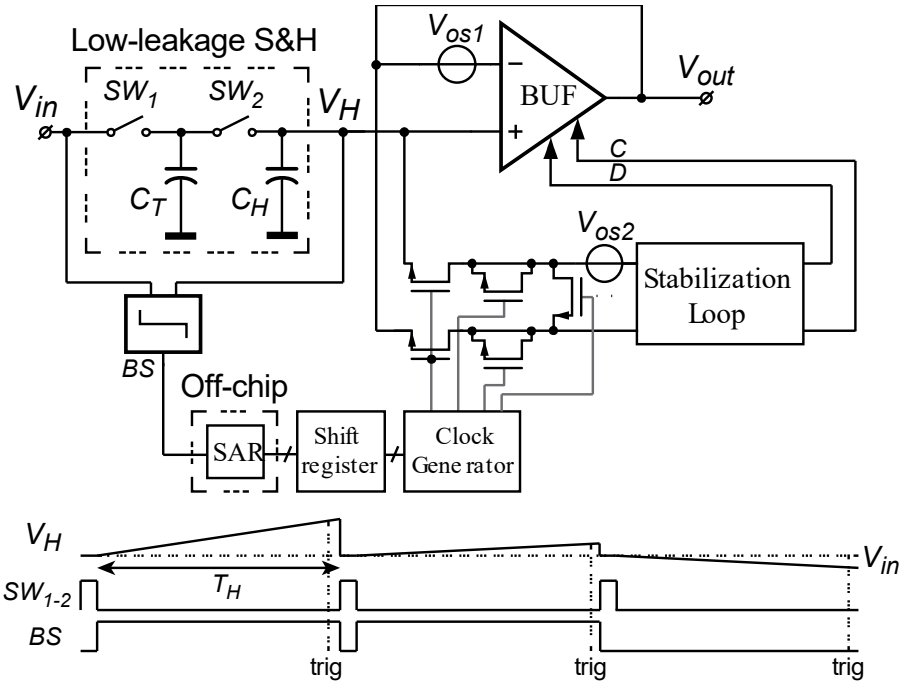

Fig. 4-5. Automatic input current trimming loop

As in [4,5], the input current can be measured by observing the voltage drift of an on-chip hold capacitor C_H (= 36pF) connected to a S&H circuit. The leakage of the S&H circuit is minimized by using additional hold capacitors to bootstrap the critical junctions of the sampling switches $SW_{1,2}$. One of these capacitors (C_T = 3pF) ensures that the channel of SW_2 is bootstrapped, minimizing its leakage. In this work, this drift is used as the sensing mechanism of an automated trimming scheme (Fig. 4-5).

Initially the voltage across C_H is reset by sampling the input voltage V_{in}. After a hold time T_H, a dynamic comparator senses the difference between V_{in} and the voltage on C_H. Its output (BS) then indicates the polarity of the input current. This is fed to off-chip SAR logic, which applies different trial codes to the trim DACs. To ensure that the voltage drift associated with the 0.1pA LSB current is significantly larger than the comparator's offset (< 5mV) and noise, the automatic trimming scheme employs a smaller hold capacitor (1pF) and a hold time (T_H) of 100ms.

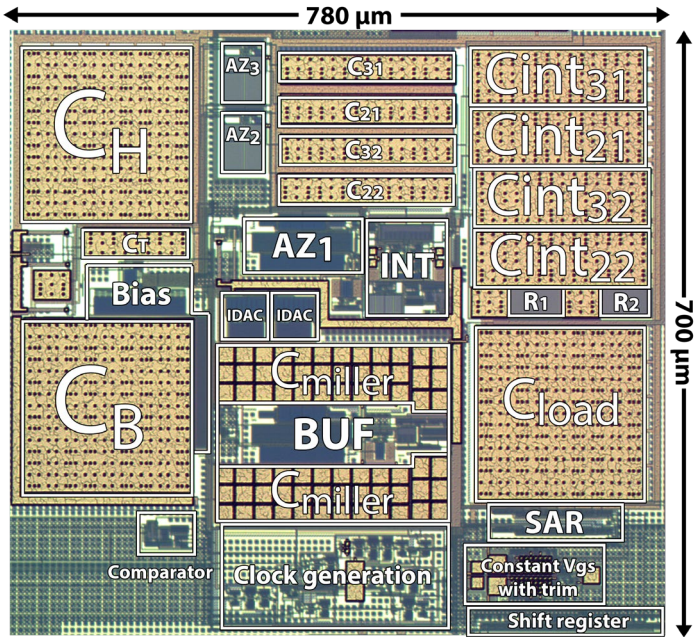

Fig. 4-6. Chip micrograph of the active area.

4.3 Measurement results

The proposed buffer is realized in a 0.18µm CMOS process (Fig. 4-6). It draws 210µA from a 1.8V supply, and has an active area of 0.55mm^2, 0.12mm^2 of which is occupied by the S&H circuit. Compared to the work of Chapter 3, the main change is the addition of the trim DACs, which occupy 0.012 mm^2, i.e. about 2% of the total active area.

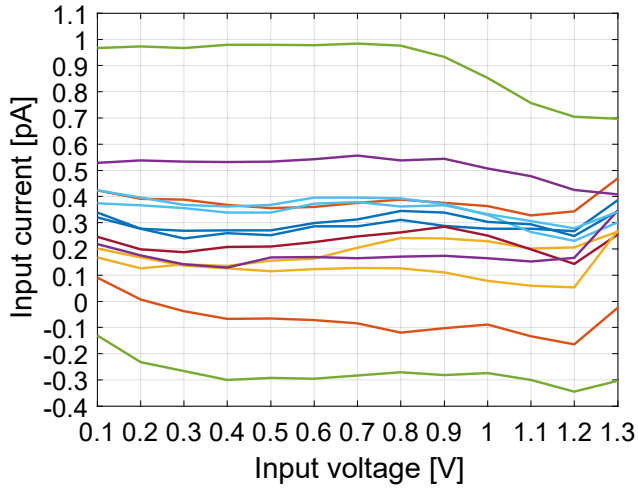

Fig. 4-7. Measured input current vs input voltage before trimming

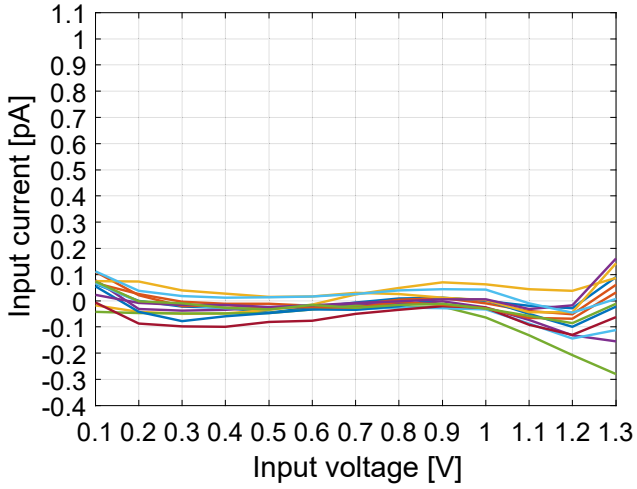

Fig. 4-8. Measured input current vs input voltage after a manual trim at 0.7V

The input current of 13 samples was measured over the buffer's full input voltage range (0 to 1.3V). Before trimming, the measured input current is limited to ±1pA (Fig. 4-7). Trimming the input current manually (Vin = 0.7V), reduces this to ±0.2pA (Fig. 4-8).

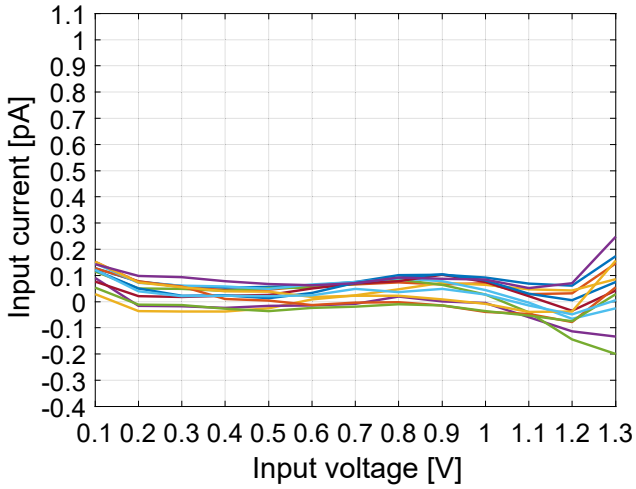

Fig. 4-9. Measured input current vs input voltage after automatic trimming at 0.7V

Good agreement can be seen between the manually and automatically trimmed samples (Fig. 4-9), proving the effectiveness of the automatic trimming scheme. This low input current was achieved while also keeping the same low low-frequency noise density (20 nV/√Hz) and offset (0.4 μV max) as in Chapter 3.

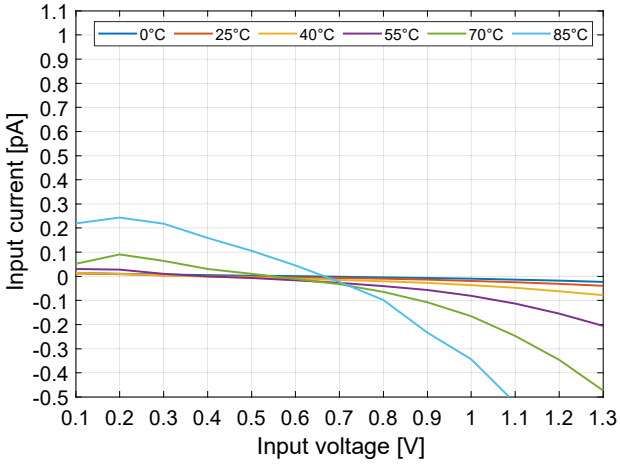

Fig. 4-11. Measured input current vs input voltage over temperature with auto-zeroing disabled.

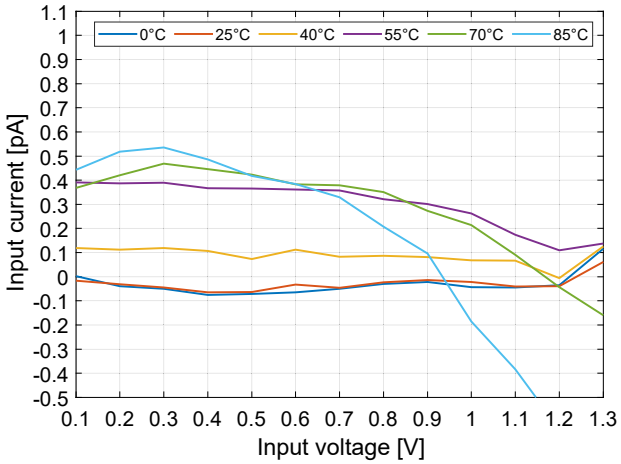

Fig. 4-10. Input current vs input voltage over temperatures with AZ enabled for a typical sample.

The input current of a typical sample was also measured over temperature (0 to 85°C). First, AZ was disabled and the input current vs input voltage was observed via the low-leakage S&H (Fig. 4-9). At higher temperatures, an apparent increase in the measured input current can be seen near the extremes of the buffer's input voltage range, probably because the passive bootstrapping of SW_2 does not perfectly suppress its parasitic junction

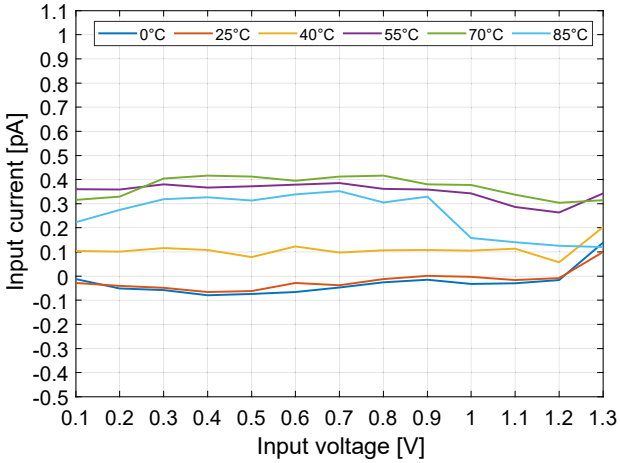

Fig. 4-12. Input current vs input voltage over temperatures for a typical sample with the S&H leakage subtracted.

leakage. With AZ enabled, a similar trend is observed (Fig. 4-10). To examine the behavior of the charge-injection related input current, the difference between the two measurements was also plotted (Fig. 4-12). It can be seen that the charge-injection related input current change is quite stable, only drifting by about 0.4pA over temperature. Simulations show that this drift is related to changes in the rise and fall time of the Φ_1 and Φ_2 clock signals, which, in turn, is related to the temperature-dependent bias current of the CML buffers.

In a general purpose application, the inputs of the buffer would be connected to pads, which would be protected by ESD diodes. To investigate the effect of these diodes, their leakage current was measured in a separate experiment. At room temperature, the variation in their leakage current with input voltage exceeds 0.5pA. Since diode leakage increases exponentially at higher temperatures, low-leakage (bootstrapped) ESD diodes will be needed to preserve the low input currents of the proposed amplifier [4.7].

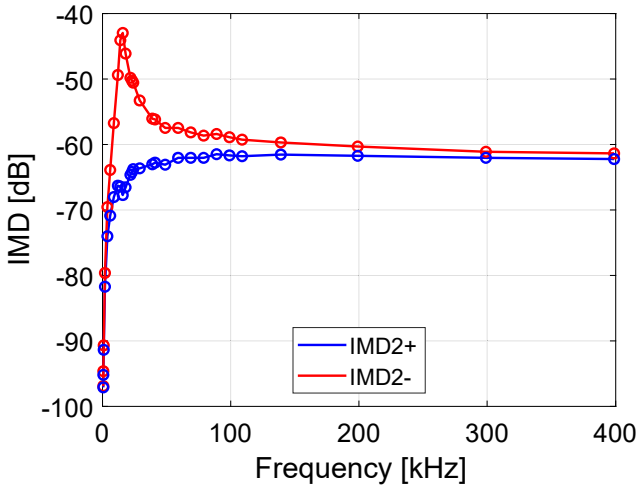

Fig. 4-13. Measured Intermodulation distortion with varying input frequency for a 100mV$_{rms}$ input signal and a typical sample.

Another switching artefact observed in auto-zero and chopper amplifiers, especially around their switching frequencies, is intermodulation distortion (IMD). The IMD of the buffer was measured by sweeping the frequency f_{in} of a 100mV$_{rms}$ input signal and observing the amplitude of the second order products ($f_{AZ} \pm f_{in}$ & $f_{in} - f_{AZ}$). The second order products above and below f_{in} were measured separately, denoted by IMD2+ and IMD2-, respectively, in Fig. 4-13. At low frequencies, the IMD2 is about 100dB, but it is only 44dB (IMD2-) around the AZ frequency (15kHz). For even higher frequencies a relatively constant IMD of around 60dB was measured.

4.4 Conclusions

An Auto-Zero Stabilized Voltage Buffer with a trimming scheme to minimize its input current is presented. To the authors' knowledge, this is the first time such a trimming scheme has been presented. The scheme operates by trimming the clock swing, and hence the charge injection, of two dummy input switches. Thanks to this scheme, the maximum input current can be lowered from 1pA to 0.2pA, which represents a 4× improvement on the work of Chapter 3, while only requiring 2% of the total area. Over temperature (0 to 85°C) the input current stays below 0.4pA, which is still well below the ESD leakage.

4.5 References

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[4.2] Q. Fan, et al., "Input characteristics of a chopped multi-path current feedback instrumentation amplifier," IEEE IWASI, pp. 61-66, 2011.

[4.3] A. T. K. Tang, "A 3μV-offset operational amplifier with 20 nV/√Hz input noise PSD at DC employing both chopping and autozeroing," ISSCC, pp. 386-387, Feb. 2001.

[4.4] T. Rooijers, et al., "A quiet digitally assisted auto-zero-stabilized voltage buffer with 0.6pA input current and 0.6μV offset," ISSCC, pp. 50-52, Feb. 2018.

[4.5] T. Rooijers, et al., "An Auto-Zero Stabilized Voltage Buffer with a Quiet Chopping Scheme and Constant Input Current," ISSCC, pp. 298-299, Feb. 2019.

[4.6] Y. Kusuda, "A 60 V Auto-Zero and Chopper Operational Amplifier With 800 kHz Interleaved Clocks and Input Bias Current Trimming," IEEE JSSC, vol. 50, no. 12, pp. 2804-2813, Dec. 2015.

[4.7] Linear Technology, "LTC6268/LTC6269datasheet",<https://www.analog.com/media/en/technical-documentation/data-sheets/662689f.pdf>

Chapter 5
A Fill-In Technique for Robust IMD Suppression in Chopper Amplifiers [3]

5.1 Introduction

As described in Chapter 2, chopper amplifiers exhibit intermodulation distortion (IMD) due to the interaction between the input signal and the chopper clock. This chopper-induced IMD is mainly due to amplifier delay, which causes large pulses at the output of the amplifier's output chopper. This chapter proposes the use of a so-called fill-in technique to eliminate these pulses, and thus the resulting IMD, by multiplexing the outputs of two identical amplifiers that are chopped in quadrature.

A prototype chopper stabilized amplifier was implemented in a 180-nm CMOS process. Measurements show that the fill-in technique suppresses chopper induced IMD by 28 dB, resulting in an IMD of −126 dB for input frequencies near $4F_{CH}$ (=80 kHz). It also improves the amplifier's two-tone IMD (with 79 and 80 kHz inputs) from −97 to −107 dB, which is the same as that obtained without chopping.

The rest of the chapter is organized as follows. The operation of the proposed fill-in technique and the resulting amplifier architecture are discussed in Section 5.2. Measurement results are shown and discussed in Section 4.3, and the chapter ends with the conclusions.

[3] This chapter is based on: T. Rooijers, S. Karmakar, Y. Kusuda, J. H. Huijsing and K. A. A. Makinwa, "A Fill-In Technique for Robust IMD Suppression in Chopper Amplifiers," in IEEE Journal of Solid-State Circuits, vol. 56, no. 12, pp. 3583-3592, Dec. 2021.

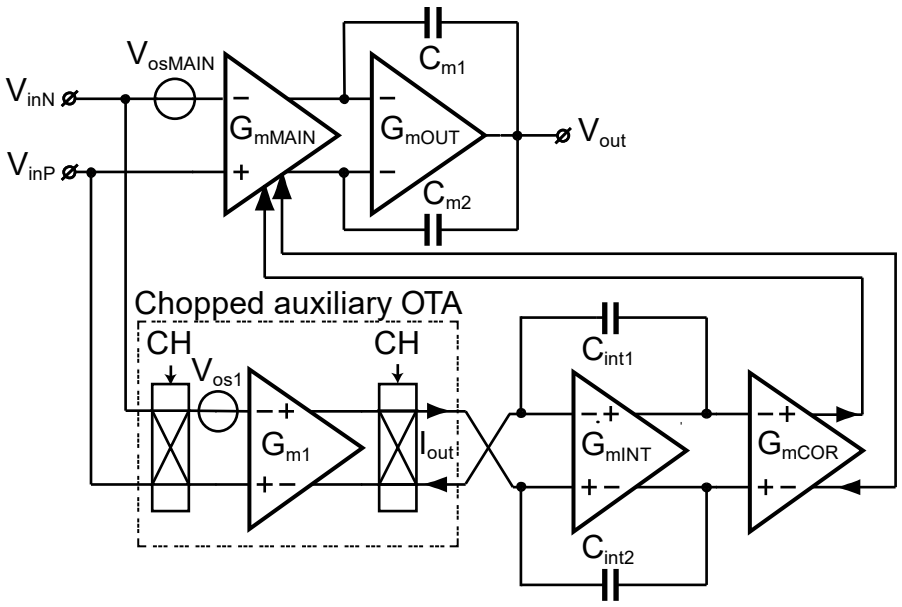

Fig. 5-1. Simplified block diagram of the chopper-stabilized amplifier.

5.2 The proposed amplifier topology with fill-in technique

A simplified block diagram of the proposed chopper-stabilized amplifier is shown in Fig. 5-1 . It consists of a two-stage main amplifier with a folded-cascode input stage (G_{mMAIN}) and a Class AB output stage (G_{mout}) with Miller compensation capacitors (C_{m1} and C_{m2}, 10 pF each) and Miller-zero compensation resistor (not shown, 5.4 kΩ). The offset and 1/*f* noise of the

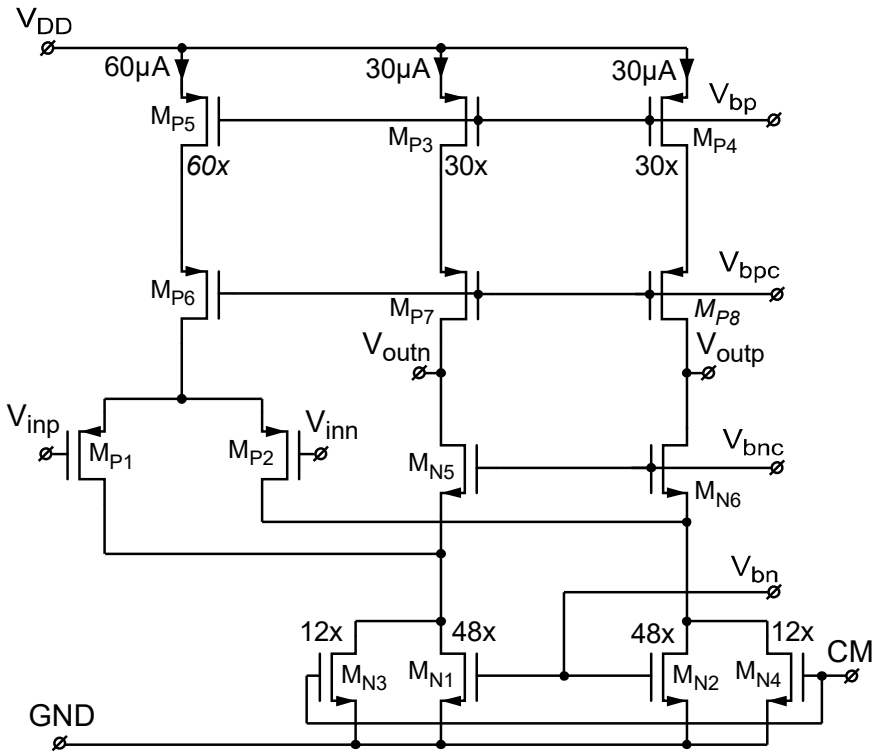

Fig. 5-2. Schematic of G_{m1} and G_{m2}

main amplifier (V_{osMAIN}) are suppressed by a three-stage auxiliary amplifier. To minimize its own offset (V_{os1}) and $1/f$ noise, the auxiliary amplifier employs a chopped OTA (G_{m1}, folded-cascode Fig. 5-2), followed by an integrator.

When used in a negative feedback configuration, the offset of the main amplifier (V_{osMAIN}) appears at the input of the chopped G_{m1}, whose output current is integrated (G_{mINT}) to generate, via G_{mCOR}, an offset-correcting signal for the main amplifier (G_{mMAIN}). Due to the amplifier's finite gain, the application of an AC input signal will give rise to a finite swing at the input of the chopped auxiliary OTA, whose finite bandwidth then causes chopper-induced IMD in its output current (I_{out}). The resulting tones will be somewhat suppressed by the active integrator. However, input frequencies close to $2F_{CH}$ (or $4F_{CH}$, $6F_{CH}$, etc.) will cause IMD tones near DC, and so will not be suppressed.

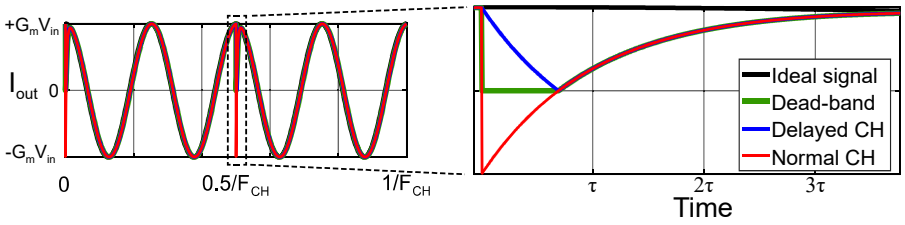

Fig. 5-3. Zoom-in of the pulse in I_{out} vs time for: ideal signal (no pulse), dead-band chopping, delayed output chopping and normal chopping.

To reduce the effect of near-DC IMD tones, the magnitude of the pulses in I_{out} should be reduced. One possibility would be to introduce a dead-band, as is sometimes done to mitigate the effect of chopping glitches [5.21]. In other words, make $I_{out} = 0$ for the duration of the pulses (Fig. 5-3). However, this will only reduce the amplitude of the pulses by about half: to G_mV_{in} from $2G_mV_{in}$. In the case of exponential settling, simulations show that the IMD reduction is limited to about 2 dB for the optimal dead-band, which ends at the zero-crossing of I_{out} (Fig. 9). Another solution would be to delay the clock of the output chopper to compensate for the OTA delay. However, simulations show that the IMD reduction is then limited to about 4 dB for the optimal delay, which again ends at the zero-crossing of I_{out} (Fig. 5-3). The limited effectiveness of these techniques can be attributed to their inability to compensate for the long settling tail of I_{out} after the zero-crossing.

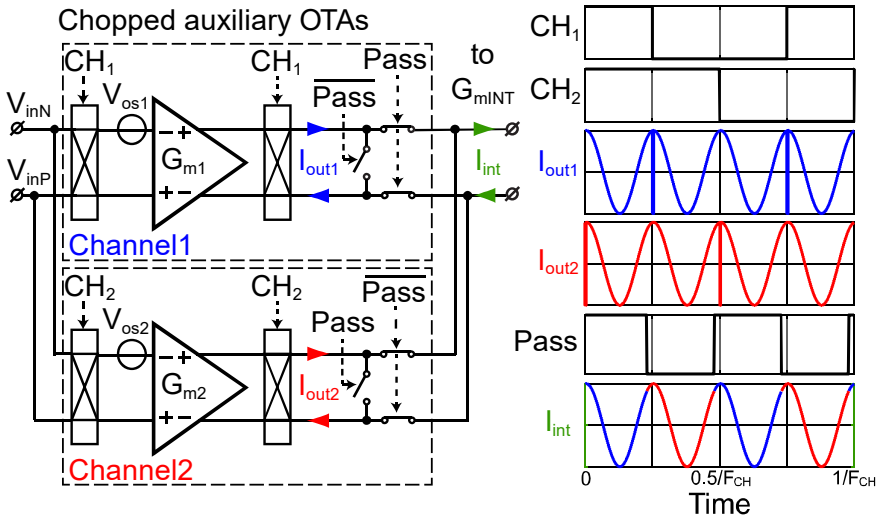

Fig. 5-4. Fill-in technique for the chopped auxiliary OTA.

The goal of the proposed fill-in technique is to suppress chopper-induced IMD by eliminating the pulses in I_{out}. As shown in Fig. 5-4, this can be done by using *two* identical auxiliary OTAs (G_{m1} & G_{m2}), which are chopped in quadrature (CH_1 & CH_2). Although the output current of each channel (I_{out1} & I_{out2}) will still contain pulses around the chopping transitions, these will only occur in one channel at a time. The OTAs' output currents ($I_{out1,2}$) are nominally identical, and so, by selecting the appropriate current slightly before each chopping transition, a combined output current can be generated that is free of pulses and, therefore, free of IMD. In other words, the pulses of one OTA are *filled in* by the output current of the other. The key insight is that the required switches can select the OTA's output currents much faster than the OTAs themselves can settle.

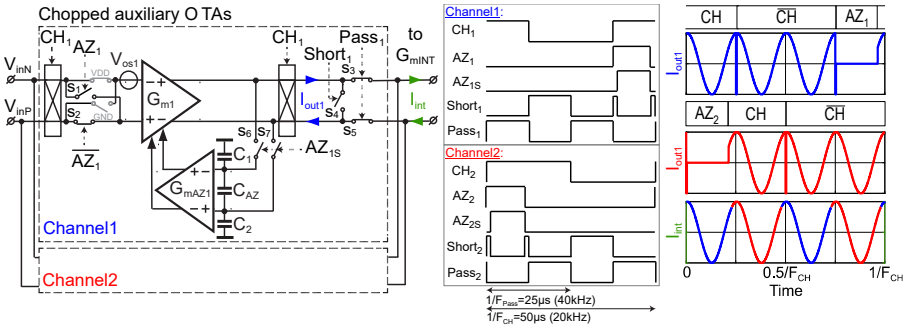

Fig. 5-5. Fill-in technique combined with auto-zeroing (Left), timing diagram (Middle) and the corresponding signals (Right).

However, the chopped offset of G_{m1} and G_{m2} (V_{os1} and V_{os2}) will still cause ripple. To suppress this, the proposed fill-in technique is combined with auto-zeroing (Fig. 5-5). An auto-zero (AZ) loop is added, which is used to AZ the OTA when it is not connected to G_{mINT}. To prevent input CM transients, which would cause additional IMD, the OTA inputs are shorted to one of the input pins during the AZ phase (via S_1). Dummy always-closed and always-open switches (in grey) ensure that the input network formed by the switch resistances and the parasitic capacitance is symmetric. During the AZ phase, C_{AZ} (25 pF) acts as a passive integrator whose output drives G_{mAZ1} (Telescopic) to cancel the OTA's offset. The resulting voltage is held by $C_{1,2}$ (1.8 pF each) during the amplification phase. To minimize noise folding, the noise BW during the AZ phase should be limited by minimizing G_{mAZ1}, but this increases the OTA's worst-case output swing. As a compromise, G_{mAZ1} is chosen to be ~50× smaller than G_{m1}.

At the start of the AZ phase, the output current of the OTA needs to transition from a level that depends on the input signal to a level that is nearly zero. To prevent these transients from reaching the AZ loop and thus causing additional IMD, shorting switch S_4 allows the OTA current to settle before it is connected via switches $S_{6\&7}$ to the virtual ground of G_{mINT}. [5.22]. $S_{6\&7}$ are controlled by the AZ_{1S} signal, which includes a dead-band that disconnects C_{AZ} during this settling time. The width of the dead-band is set to 100 ns, which guarantees OTA settling in the worst-case corner. Similarly, the AZ phase is ended roughly 100 ns before the next chopping phase, allowing $G_{m1,2}$ to settle before it is connected to G_{mINT}. To further minimize the voltage transient that occurs when the OTA is connected to G_{mINT}, the shorting switch (S_4) resistance is set to ~$1/G_{mINT}$ (6.8 kΩ). The remaining voltage transients are then mainly due to the charge-injection of the multiplexing switches (S_3 and S_5).

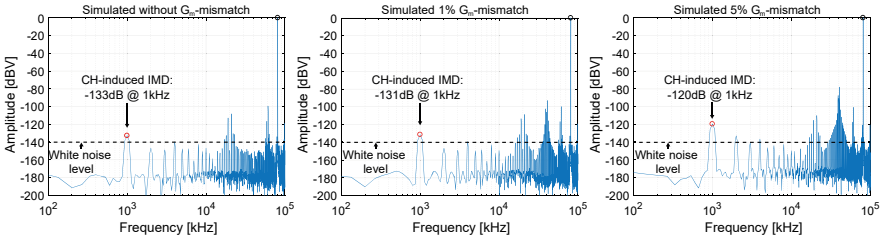

Fig. 5-6. Simulated amplitude spectrum without G_m-mismatch, 1% of mismatch and 5%.

The effectiveness of the fill-in technique is limited by the G_m matching of the two input OTAs, as any mismatch will cause additional transients in their composite output current. With a 1 V_{rms} 81 kHz input signal, the results of simulations with various degrees of intentional G_m mismatch are shown in Fig. 5-6. Without mismatch, the simulated chopper-induced IMD is -133 dB, increasing only slightly to -131 dB for 1% mismatch, which is readily achievable. Even with 5% mismatch, -120 dB IMD can still be achieved, showing that in practice, Gm mismatch is not an important limiting factor.

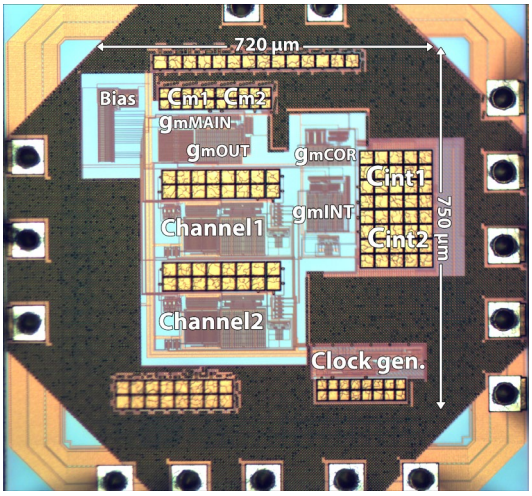

Fig. 5-7. Die micrograph.

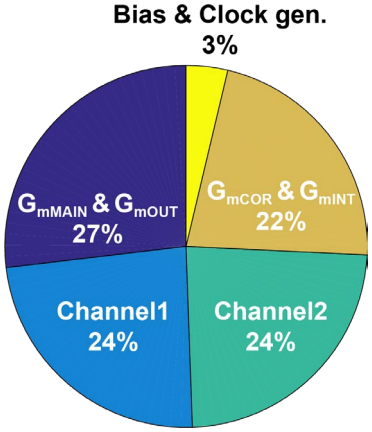

Fig. 5-8. Power breakdown of the most important blocks

5.3 Measurement Results

The prototype chopper-stabilized amplifier with fill-in technique was realized in a 0.18µm CMOS BCD process. The die micrograph is shown in Fig. 5-7, with the most important blocks highlighted. It occupies an active area of 0.54 mm^2 and draws 550 µA from a 5 V supply. The opamp has a 0 to 4.5 V input CM range, a 15.4 NEF and a 4.2 MHz GBW. A power breakdown is shown in Fig. 5-8. It is equally split between the main amplifier, Channel 1, Channel 2 and the rest of the stabilization loop. The first three all have low noise input stages and so dissipate significant power. Furthermore, at high input frequencies, the signal entering the stabilization loop increases due to

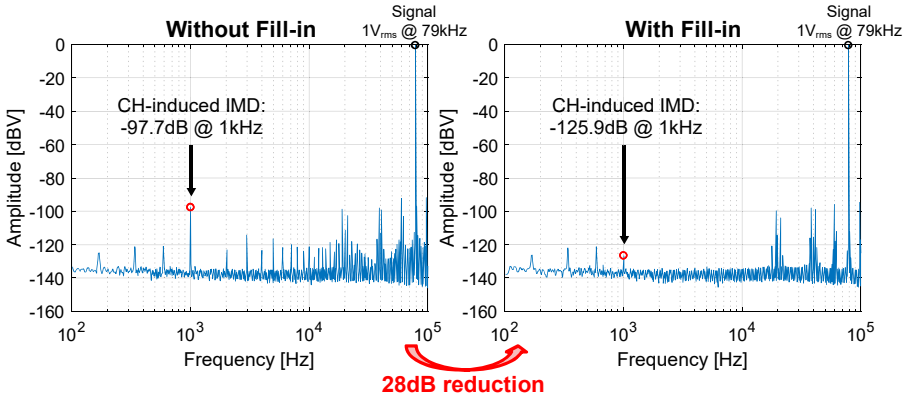

Fig. 5-9. Measured amplitude spectrum (10 averages) for a one-tone test of 79kHz $1V_{rms}$ for fill-in disabled and enabled

the roll-off of amplifier gain. To handle the resulting high current levels output by the input OTAs, the stabilization loop also dissipates significant power.

With the prototype amplifier configured as a buffer, a one-tone test was performed using an Audio Precision APx555 analyzer, which provides a 1 V_{rms} 79 kHz input tone at an input common-mode level of 2.2 V. To ensure that the IMD tones are well above the ~134 dB noise floor, an input tone near $4F_{CH}$ (79 kHz) was used rather than one near $2F_{CH}$ (39 kHz). The resulting output amplitude spectrum is shown in Fig. 5-9. The 79 kHz input tone, together with the chopping frequency of 20 kHz, leads to an IMD tone at 1 kHz ($4F_{CH}$-F_{in}). Without the fill-in technique, a large (-97.7 dB) IMD tone is present. With the fill-in technique enabled, this drops by 28 dB, to -125.9 dB. Some power-line interference is also visible below 1kHz. This is present even in the absence of the prototype chip and is thus caused by the measurement setup. Higher-order IMD tones (> 1 kHz) are also partly suppressed by the fill-in technique. Some residual ripple is also present at multiples of F_{CH}.

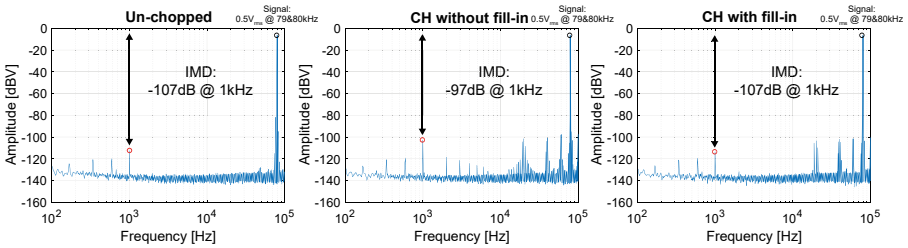

Fig. 5-10. Measured amplitude spectrum (10 averages) for a two-tone test of 79 and 80 kHz tone 0.5V_{rms} each, for the case of the un-chopped amplifier, chopped without fill-in and with fill-in.

A two-tone test was also performed using tones at 79 and 80 kHz, both with an amplitude of 0.5 V_{rms}. The resulting amplitude spectrum is shown in Fig. 5-10. As a baseline, the two-tone IMD was first measured with chopping disabled. Due to the amplifier's own non-linearity, an IMD tone of -107 dB can be seen at 1 kHz. When chopping is enabled, but without the fill-in technique, this tone increases to -97 dB, which is mainly due to chopper-induced IMD. With the fill-in technique enabled, the IMD drops back to -107 dB, demonstrating the effective suppression of chopper-induced IMD.

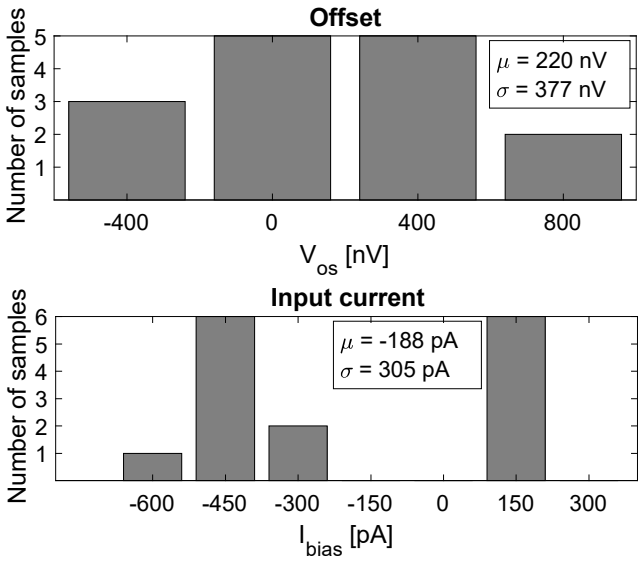

Fig. 5-12. Histogram of the offset voltage and input current for 15 Samples.

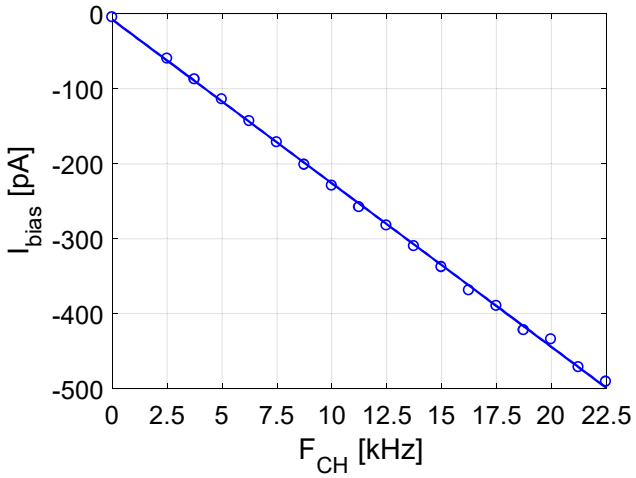

Fig. 5-11. Input current for different chopping frequencies.

With a 2.5 V input CM voltage and F_{CH} = 20 kHz, measurements on 15 samples show that the offset is less than 0.8 μV, while the input current is less than 600 pA (Fig. 5-12). The input current was measured by a Keithley 6514 electrometer, and guarding was used to minimize PCB leakage. The input current is a linear function of F_{CH} (Fig. 5-11), indicating that it is mainly due to the charge injection (mismatch) of the chopper and AZ switches.

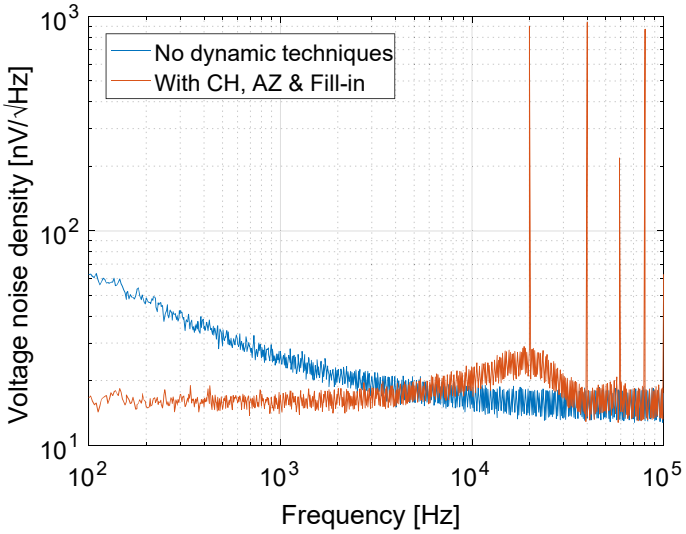

Fig. 5-13. Voltage noise density vs frequency for the case without any dynamic techniques and with CH, AZ and Fill-in.

The opamp's voltage noise density is shown in Fig. 5-13. With chopping disabled, its white-noise level is 16 nV√Hz and its $1/f$ corner frequency is ~6 kHz. With chopping, auto-zeroing and fill-in enabled, the $1/f$ corner frequency is less than a few Hertz. The noise folding associated with auto-zeroing each OTA at 20 kHz, causes a slight noise bump around this frequency. Some tones can also be seen at the chopping/auto-zeroing frequencies, which is due to PCB-mediated cross-talk between the 5V reference clock (80 kHz) and the prototype chip.

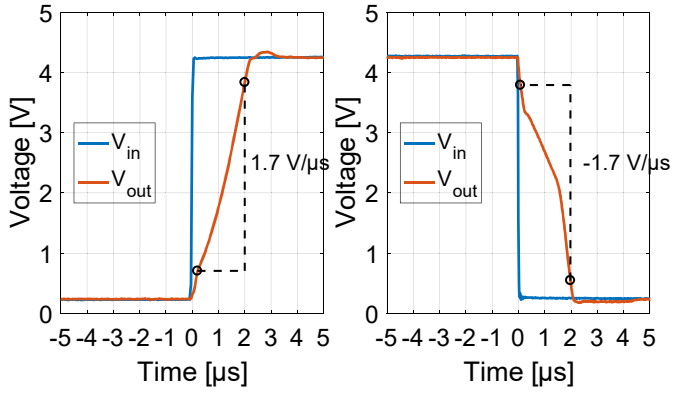

Fig. 5-15. Slew-rate measurement for a step-up and step-down

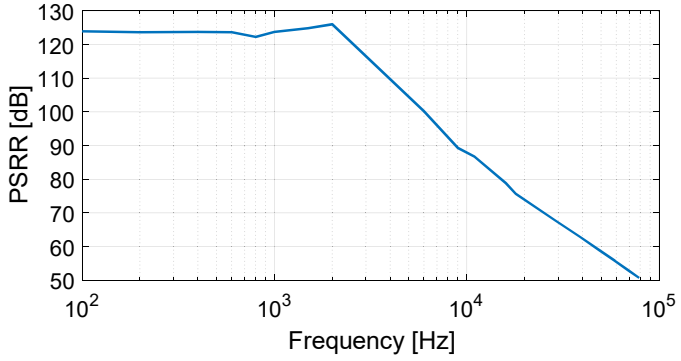

Fig. 5-14. Measured PSRR vs frequency.

To verify the amplifier's ability to handle rapidly changing signals, its slew rate was measured by applying a 4 V input step (Fig. 5-15). For both rising and falling steps, the speed at which the amplifier's output transitions from 10% to 90% of its final value corresponds to a slew-rate of 1.7 V/µs.

Fig. 5-14 shows the measured PSRR of the amplifier using a 1 V_{rms} disturbance added to the 5 V supply at different frequencies. At low frequencies, the PSRR is 124 dB, rolling off at higher frequencies.

TABLE 5-I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART

	This work	AD8551 [3.24]	AD8571 [5.18]	Ivanonv [5.19]	Rooijers [5.8]	
Dynamic technique(s)	**Chopper Stabilized with Auto-zeroing**	Auto-zero Stabilized	Auto-zero Stabilized	Chopper Stabilized with ripple-reduction	Auto-zero and Chopped Stabilization	
Chopper-induced IMD tone (dB @ f_{IMD})	**f_{in}=79 kHz -97.7 (No Fill-in) -125.9 (Fill-in) @ 1 kHz**	f_{in}=0.5 kHz -80 (Single)* - @ 4.5 kHz	f_{in}=0.5 kHz - -90 (Spread)* @ 4.5 kHz	f_{in}=1 kHz -103 (Single)** -122.7 (Spread)** @ 156 kHz	f_{in}=1 kHz -91 (Single) - @ 14 kHz	f_{in}=16 kHz -44 (Single) - @ 1 kHz
Offset (Max)	**0.8 µV*****	5 µV	5 µV	3.5 µV	0.6 µV***	
Input current (Max)	**600 pA*****	50 pA	50 pA	200 pA	1 pA (untrimmed)*** 0.2 pA (trimmed)***	
Voltage noise density (nV/√Hz)	**16**	42	51	6.5	20	
CH/AZ frequency (kHz)	**20**	4	2-4	50-150	15	
GBW (MHz)	**4.2**	1.5	1.5	10	1.45	
Slew rate (V/µs)	**1.7**	0.4	0.4	5	-	
PSRR (dB)	**124**	130	130	135	125	
Supply voltage	**5 V**	5 V	5 V	1.8 - 5.5 V	1.8 V	
Supply current	**0.55 mA**	0.85 mA	0.85 mA	1.65 mA	0.21 mA	
Technology	**0.18 µm**	-	-	0.6 µm	0.18 µm	
Die Area (mm^2)	**1.25**	-	-	1.626	1.4	

*V_{out}=1 V_{rms}@500 Hz (A=40 dB) [5.15] **V_{out}=1 V_{rms}@1 kHz (A=1)
***Maximum value of 15 sample

Table 5-I summarizes the performance of the amplifier and compares it to other DOC amplifiers using chopping, auto-zeroing or a combination of the two. The table reports the IMD of amplifiers that use both fixed DOC frequencies (Single) [5.8] [3.24] and spread-spectrum DOC frequencies (Spread) [5.18] [5.19]. For the latter, the IMD with a fixed DOC frequency is also reported (Single), where it should be noted that [3.24] and [5.18] describe the same amplifier. Although the reported IMD of the proposed amplifier is obtained from a single sample, the variation between five samples has been measured. Without the fill-in technique, the single-tone IMD varies between -97.2 and -98.2 dB. With the fill-in technique enabled, the IMD varies between -125 and -131 dB. The amplifier achieves the lowest IMD (125.9 dB) at a much higher input frequency (79 kHz), which is more difficult to achieve due to the roll-off of amplifier gain with frequency. Furthermore, at worst-case input frequencies ($f_{in} = nf_{AZ}$ with n = 1,3,5,.. or $f_{in} = nf_{CH}$ with n=2,4,6,..), which will cause near-DC IMD tones, an 81.9 dB improvement is obtained. For low input frequencies (< 1kHz) the IMD tones are below the -134 dB noise floor. Even though an additional low-noise input stage is required to implement the fill-in technique, the amplifier's total supply current (0.55 mA) is comparable with that of other designs. Each fill-in channel uses 24% of the power and 10% of the total active area.

5.4 Conclusion

In chopper amplifiers, finite amplifier delay gives rise to short pulses around the chopping transitions, which in turn give rise to significant amounts of chopper-induced intermodulation distortion (IMD). To address this problem, a novel fill-in technique is proposed, in which two identical amplifiers are chopped in quadrature such that a pulse-free output signal can be obtained by selecting the output of the appropriate amplifier. As a proof of concept, the fill-in technique was used in a chopper-stabilized amplifier, resulting in a 28 dB reduction of its chopper-induced IMD. This corresponds to less than -125 dB of chopper-induced IMD for a single-tone near $4F_{CH}$ (= 80 kHz), while the two-tone IMD (with 79 & 80 kHz tones) is less than -105 dB, mainly limited by the amplifier's own linearity. In addition, the amplifier achieves low offset (< 1μV) and low noise (16 nV√Hz), while its supply current (0.55 mA from a 5V supply) is comparable with that of other state-of-the-art precision amplifiers.

5.5 References

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Chapter 6
A Chopper-Stabilized Amplifier with a Relaxed Fill-in technique[4]

6.1 Introduction

The fill-in technique described in Chapter 5 robustly lowers the chopper-induced intermodulation distortion by 28 dB. However, the presented implementation suffers from a few drawbacks, caused by each OTA being used 50% of the time. First, both the OTA's offsets contribute equally to the chopper ripple and so both were reduced by auto-zeroing. However, the noise folding due to auto-zeroing then resulted in an up-modulated noise bump around F_{CH} in the amplifier's noise spectrum. Furthermore, the combination of chopping and auto-zeroing requires ten input switches, whose activity resulted in a relatively high maximum input current of 600pA. Finally, two power hungry OTAs are necessary which need to be on continuously. This chapter investigates a relaxed implementation of the fill-in technique to help mitigate these downsides. It uses a simpler architecture to achieve similar IMD performance (-125.7dB), a 25× lower input current (22.6pA) and a flat noise floor (12 nV/√Hz).

[4] This chapter is based on: T. Rooijers, J. H. Huijsing and K. A. A. Makinwa, "A Chopper-Stabilized Amplifier With a Relaxed Fill-In Technique and 22.6-pA Input Current," in IEEE Solid-State Circuits Letters, vol. 6, pp. 165-168, 2023.

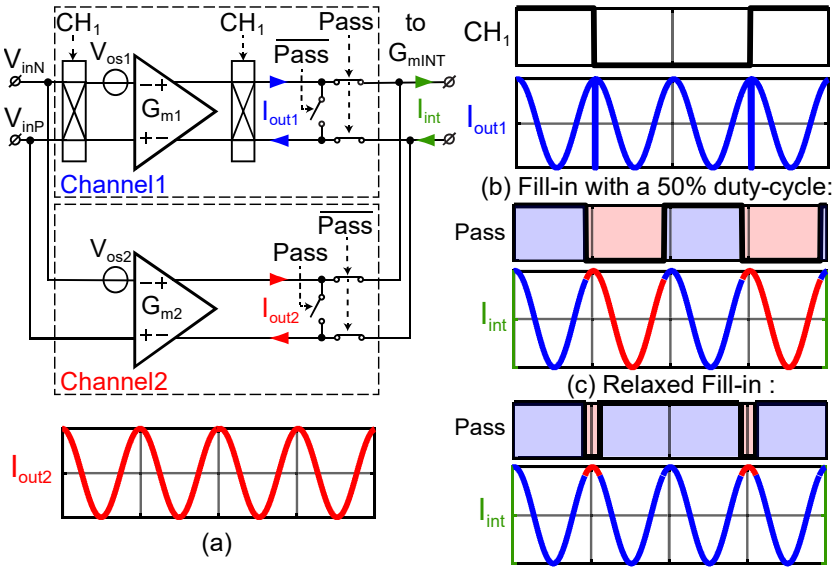

Fig. 6-1. Fill-in implementation with two OTAs and multiplexing switches (top left), the chopping signals and the resulting output current with spikes

6.2 Relaxed Fill-in

The implementation of the relaxed fill-in technique is shown in Fig. 6-1. The spikes in the output (I_{out1}) of a chopped main OTA (G_{m1}) are filled in by the output (I_{out2}) of a fill-in OTA (G_{m2}). As shown in Fig. 6-1c, I_{out2} is only used briefly, greatly relaxing the requirements on G_{m2} compared to the implementation in Chapter 5, Fig. 6-1b. The low duty-cycle suppresses the offset and $1/f$ noise of G_{m2}, which means that it does not need to be chopped. The $1/f$ noise and offset of G_{m1} can then be reduced by a ripple-reduction loop (RRL) without incurring a noise folding penalty. The lower limit of the duty cycle is set by the BW of G_{m1} (~16.5MHz). In this work, a duty-cycle of 0.4% was chosen to comfortably accommodate this over PVT.

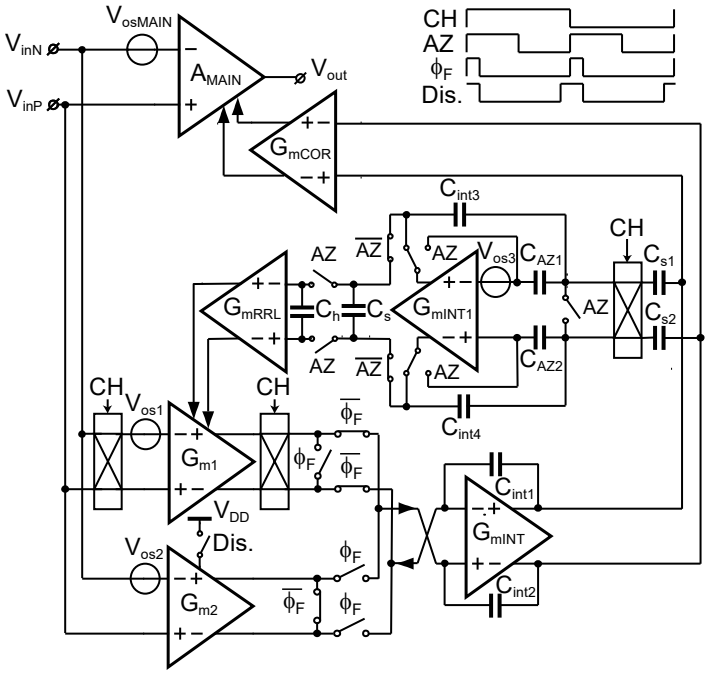

Fig. 6-2. Simplified block diagram of the proposed Chopper-Stabilized Operational Amplifier.

6.3 Implementation of the Chopper-Stabilized Amplifier with relaxed fill-in

The proposed chopper-stabilized amplifier is shown in Fig. 6-2. It consists of a main amplifier (A_{MAIN}), whose offset (and 1/*f* noise) appears between its input terminals when it is used in a negative feedback configuration, where it can be sensed and corrected by a chopped auxiliary amplifier. In this work, the offset of a two-stage main amplifier (folded-cascode 1st stage and Class AB 2nd stage) is suppressed by a three-stage auxiliary amplifier. To mitigate its own offset (V_{os1}), the auxiliary amplifier employs a chopped OTA (G_{m1}, folded-cascode), followed by an integrator (G_{mINT}, folded-cascode, $C_{int1,2}$ = 36pF), and a correction OTA (G_{mCOR}, telescopic). The fill-in OTA (G_{m2}) is a non-chopped replica of G_{m1}. Simulations show that its offset (< 1mV) has a negligible effect on the residual offset of the overall amplifier and causes only a small (< 3μV_{rms}) tone at $2F_{CH}$ (40kHz). Similarly, its 1/*f* noise also has a negligible effect, resulting in an overall 1/*f* noise corner of only 2Hz in simulation. All required clocks are generated from a single off-chip 80kHz clock by on-chip logic.

6.4 Low IMD Ripple reduction loop

The RRL consists of two capacitors $C_{s1,2}$ (3.6pF) that sense the ripple due to V_{os1} at the output of the integrator formed by G_{mINT} and $C_{int1,2}$. The resulting current is then demodulated and integrated by the RRL integrator formed by G_{mINT1} and $C_{int3,4}$ (9pF each). Its output is applied to G_{mRRL}, which cancels V_{os1} by injecting a correction current into G_{m1}. Since the amplitude of the ripple is limited by the offset of G_{mINT1}, this is auto-zeroed with the help of C_{AZ1} and C_{AZ2} (4pF each).

However, the RRL can also create chopper-induced IMD, since the signal transitions caused by its ripple-demodulating choppers are delayed by the RRL integrator before they reach the output choppers of G_{m1}. In this design, this extra source of IMD is suppressed in two ways. First, the contribution of the RRL to the output current of G_{m1} is minimized by using a large G_{m1}/G_{mRRL} ratio. However, this is limited to ~600× by the swing of G_{mINT1} and the expected magnitude of V_{os1}. In simulation, this limits the resulting IMD to -100dB. To lower this further, a sample-and-hold is used to freeze the input of G_{mRRL} just before each chopping transition. Further low-pass filtering is achieved by using a small sampling capacitor C_s (=0.5pF) to drive a larger hold capacitor C_H (=7.2pF). These measures ensure that the overall IMD is not limited by the RRL.

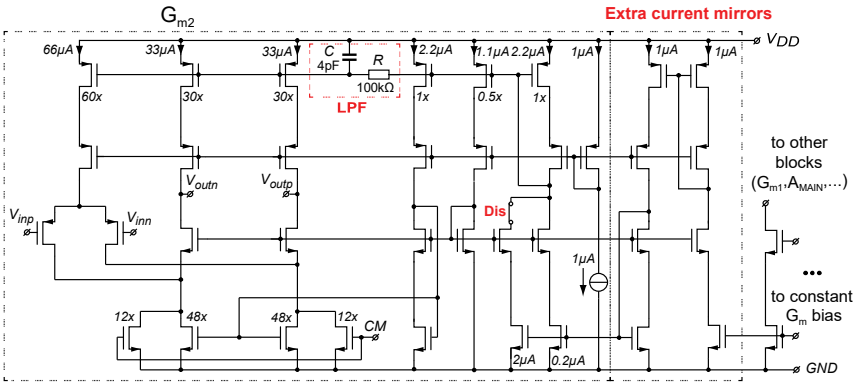

Fig. 6-3. Simplified implementation of G_{m2} with low-glitch duty-cycling measures.

6.5 Duty-cycled OTA

Since G_{m2} is only used briefly, it can be turned "off" most of the time. The implementation of Gm2 is shown in Fig. 6-3. To ensure that the process of turning it "on" and "off" does not itself cause input spikes and more distortion, three measures are taken. First, the OTA's main bias current is not completely turned off, but just reduced 11× by switching it from 2.2uA to 0.2uA to mitigate the change in the various biasing voltages. Second, a lowpass filter (R = 100kΩ and C = 4pF) at the gates of the switched bias current sources of G_{m2} is used to slow down the bias-current transitions. Third, the transitions in these bias sources are isolated from the main bias-current generator and other circuit blocks by an extra set of current mirrors.

Simulations show that these measures ensure that the resulting spikes are well below the noise floor, while incurring only a small power penalty. Switching the bias current of the fill-in OTA with a 20% duty-cycle (to allow sufficient settling) then results in a 76% power saving for G_{m2}.

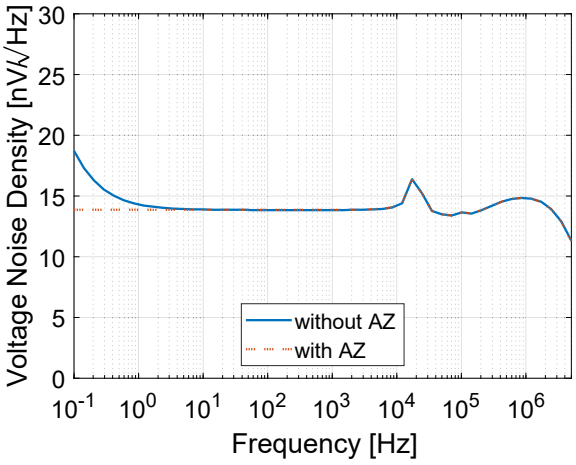

Fig. 6-4. Simulated voltage noise density vs frequency with and without AZ.

6.6 Auto-zeroing the fill-in OTA

The 1/*f* noise of the second (fill-in) OTA is significantly suppressed by the duty-cycle, but at low frequencies it is still significant. To investigate the noise performance, a simulation was done of the voltage noise density vs frequency (Fig. 6-4). At low frequencies <3Hz, the 1/*f* noise of the second OTA still makes a significant contribution to the overall noise.

A second issue is that, while the offset of second OTA does not have a significant contribution to the ripple, it will still show up every 100ns around the chopping transition. This means that the offset of the second OTA will contribute to the tone at $2F_{CH}$ and its multiples.

In order to mitigate this, dynamic offset compensation techniques will also have to be applied to the second OTA. However, since the white noise also gets suppressed by the duty-cycle, the white noise coming from the on-resistance of the switches is reduced. This allows the use of much smaller switches in the second OTA, minimizing its contribution to the overall input current.

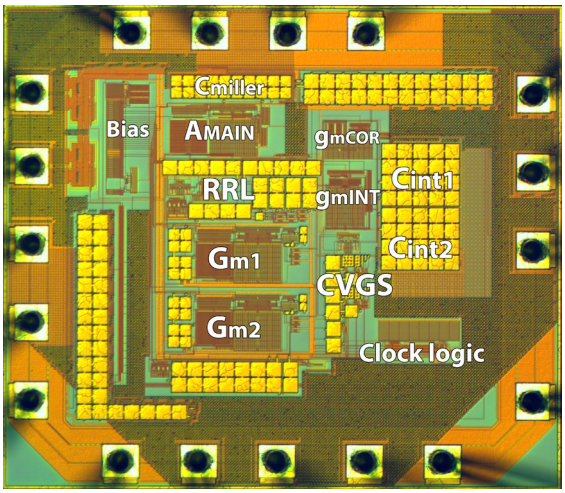

Fig. 6-5. Die micrograph

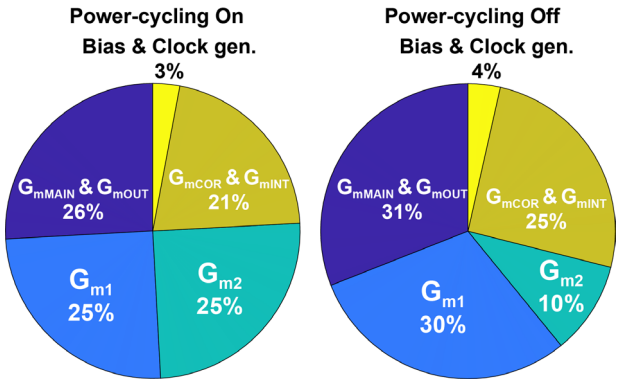

Fig. 6-6. Power breakdown

6.7 Measurement results

The opamp is realized in a 0.18µm CMOS BCD process and has an active area of 0.57mm^2. A die micrograph is shown in Fig. 6-5 with the most important blocks annotated. It draws 620µA from a 5V supply, which drops to 530µA when the fill-in OTA is duty-cycled, a 15% power saving. The power breakdown (Fig. 6-6) shows that the contribution of the fill-in OTA is then only 10%.

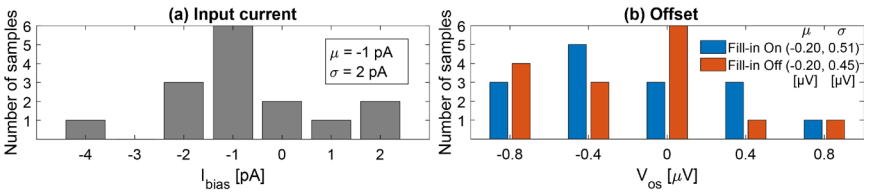

Fig. 6-7. Histogram of the input current (a) and offset (b) at 2.5V for 15 samples.

Measurements on 15 samples with a 2.5V input CM voltage and F_{CH} = 20kHz, show that the opamp's input current remains below 4pA (Fig. 6-7a) and that its offset does not exceed 0.8μV (Fig. 6-7b). Enabling and disabling fill-in only changes the offset slightly, confirming that not chopping the fill-in OTA does not significantly worsen the overall offset. The input current was measured using an Keithley 6514 electrometer. To minimize the leakage from the PCB, guarding and a PCB made of low leakage Roger material was used.

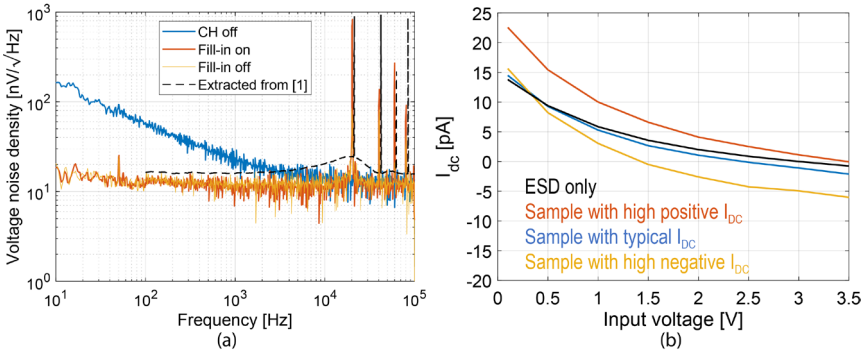

Fig. 6-8. Voltage noise density vs frequency (a) and input current vs input voltage (b).

The opamp's voltage noise density is shown in Fig. 6-8a without chopping, with chopping and with the fill-in OTA turned "on" and "off". The measured voltage noise density of the opamp in Chapter 5 is also shown. Without chopping, the opamp has a 1/*f* noise corner frequency of about 2kHz. With chopping, the use of an RRL eliminates the noise bump seen in the implementation of Chapter 5, resulting in a flat noise floor with a lower (12nV/√Hz) spectral density. The latter is mainly due to the higher biasing current used in the input stages of this design. The measured 1/*f* corner is below 10Hz and is not affected when the fill-in OTA is enabled. Furthermore, no extra tones are created when it is duty-cycled, confirming the effectiveness of the various spike mitigation measures. Some crosstalk from the external clock can be observed at 20, 60 and 80kHz.

Fig. 6-8b shows the input current vs input voltage characteristic of three samples: a typical sample, and two worst-case samples. All three draw more input current at low input voltages. Measurements of an un-connected pad show a similar trend, indicating that most of the input current at low input voltages is due to ESD diode leakage.

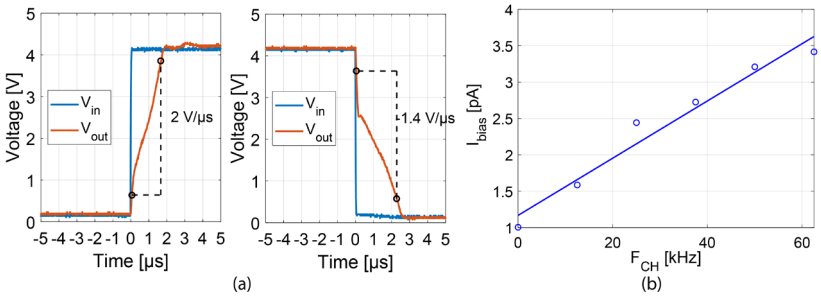

Fig. 6-9. Slew rate with a 4V input voltage step (0.2 to 4.2V) in a buffer configuration. Input current vs chopping frequency.

A step response measurement (Fig. 6-9a) shows that the opamp has a slew rate of 2V/µs (up) and 1.4V/µs (down), with no extra ringing due to the RRL. The input current at mid-supply is about 4pA, which, as predicted in Chapter 2, is roughly 4× larger than that of an AZ-stabilized amplifier realized in the same process. Measurements show that the input current at mid-supply increases linearly with F_{CH} (Fig. 6-9b), indicating that it is mainly due to the charge injection mismatch of the input chopper switches.

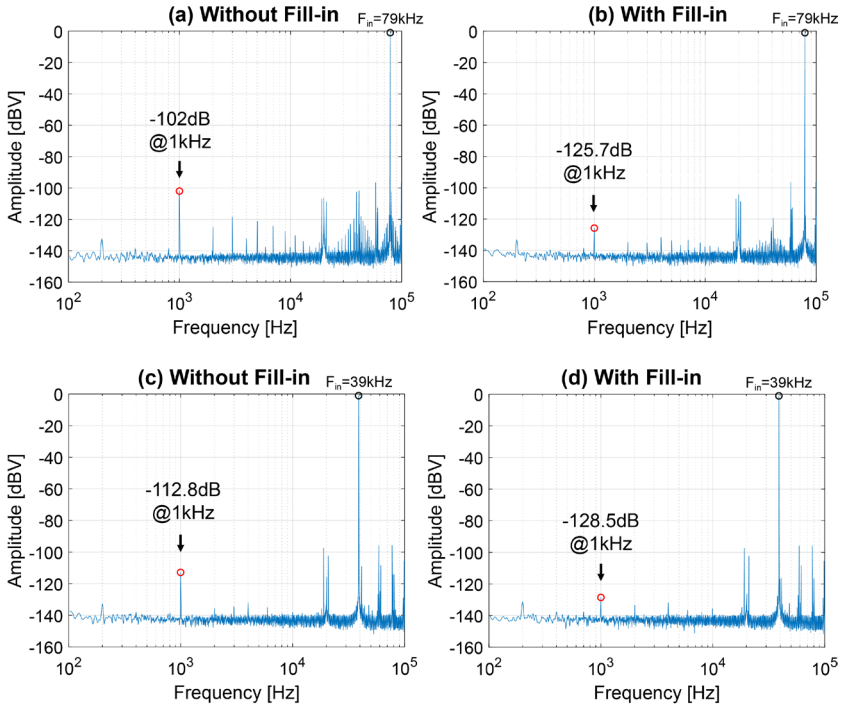

Fig. 6-10. Measured amplitude spectrum with a single 79kHz (a & b) or 39kHz (c & d) tone without (a & c) and with (b & d) the fill-in technique.

With the opamp configured as a buffer, a single $1V_{rms}$ 79kHz (~$4F_{CH}$) input tone results in the output amplitude spectrum shown in Fig. 6-10 (a & b). Without the fill-in technique (a), a large -102dB IMD tone is present at 1kHz ($4F_{CH}$-F_{in}). Enabling the fill-in technique reduces this by 24dB, to -125.7dB (b). Measurements on 5 samples show that the achieved IMD spreads between 123dB and 134.4dB, demonstrating good robustness. With a similar 39kHz tone (~$2F_{CH}$), the IMD tone is –112.8dB without fill-in and -128.5dB with fill-in, a 16dB improvement. At lower input frequencies (<5kHz), the IMD tones are below the -140dB noise floor.

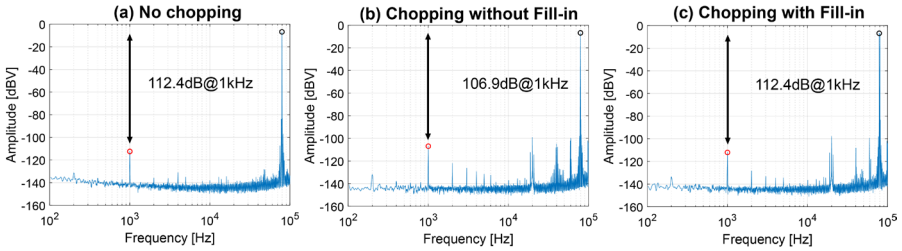

Fig. 6-11. Two-tone test all in a non-inverting buffer configuration for (a) no chopping, (b) chopping without fill-in and (c) chopping with fill-in.

When two input tones are applied (79 and 80kHz, $0.5V_{rms}$ each), the resulting amplitude spectrum is shown in Fig. 6-11. Without chopping, the IMD at 1kHz is –112.4dB, which increases to –106.9dB with chopping and with fill-in disabled. Enabling the fill-in technique restores the IMD to –112.4dB, demonstrating that it effectively suppresses chopper-induced IMD. Without fill-in, measurements show that the residual ripple amplitude at $2F_{CH}$ is around 0.7µVrms. With fill-in, this increases to 2.5µVrms for a worst-case sample with the largest fill-in OTA offset.

TABLE 6-I - PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE OF THE ART

	This work	Rooijers 2021 [6.1]	AD8551 [6.2]	AD8571 [6.3]	Ivanov [6.4]	Rooijers [6.5]
DOC technique(s)	**Chopping + RRL**	Chopping + AZ	AZ	AZ	Chopping + RRL	AZ + Chopping
DOC frequency (kHz)	**20**	20	4	2 to 4	50 to 150	15
Chopper-induced IMD tone (dB)	**f_{in}=79 kHz -102 (No Fill-in) -125.7 (Fill-in)**	f_{in}=79 kHz -97.7 (No Fill-in) -125.9 (Fill-in)	f_{in}=0.5 kHz -80 (Single) -	f_{in}=0.5 kHz - -90 (Spread)	f_{in}=1 kHz -103 (Single) -122.7 (Spread)	f_{in}=16 kHz -44 (Single) -
Offset (Max)	**0.8 µV**	0,8 µV	5 µV	5 µV	3.5 µV	0.6 µV
Input current (Max)	**22.6 pA**	**600 pA**	50 pA	50 pA	200 pA	1 pA (untrimmed) 0.2 pA (trimmed)
Voltage noise density (nV/√Hz)	**12**	**16**	42	51	6.5	20
Supply voltage	**5 V**	**5 V**	5 V	5 V	1.8 - 5.5 V	1.8 V
Supply current	**0.55 mA**	**0.55 mA**	0.85 mA	0.85 mA	1.65 mA	0.21 mA
Die Area (mm^2)	**1.25**	**1.25**	-	-	1.626	1.4

Table 6-I summarizes the opamp's performance and compares it to state-of-the art chopper and auto-zero amplifiers. It achieves similar IMD (-125.7dB @ 79kHz ~$4F_{CH}$) to [6.1], with a much simpler architecture. Among the chopper amplifiers, it achieves the lowest input current (22.6pA max), only beaten by an AZ amplifier [6.5], with a trimmed input current and much worse IMD (-44dB). Compared to [6.1], it achieves 25× less input current and a lower flat white noise level (12nV/√Hz) at similar supply current levels.

6.8 Conclusions

This work proposes a chopper-stabilized amplifier with a relaxed implementation of the fill-in technique. It achieves a similarly low level of intermodulation distortion as a previous implementation, -125.7dB with an input frequency of 79 kHz. However, it also achieves 25× less input current, with a maximum of 22.6pA. Finally, it achieves a flat lower noise floor of 12nV/√Hz, while consuming the same power (2.75mW).

6.9 References

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[6.4] V. Ivanov and M. Shaik, “A 10MHz-Bandwidth 4µs-Large-Signal-Settling 6.5nV/√Hz noise 2µV-Offset Chopper Operational Amplifier,” in *IEEE ISSCC Dig. Tech. Papers*, pp. 88-89, Feb. 2016.

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[6.6] T. Rooijers, J. H. Huijsing and K. A. A. Makinwa, "3.2 A Chopper-Stabilized Amplifier with a Relaxed Fill-In Technique and 22.6pA Input Current," in *IEEE ISSCC Dig. Tech. Papers*, pp. 2-4, Feb. 2023.

[6.7] T. Rooijers et al., “An Auto-Zero-Stabilized Voltage Buffer with a Quiet Chopping Scheme and Constant Sub-pA Input Current,” *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2438-2448, Aug.

Chapter 7
Conclusions

CMOS amplifiers suffer from offset (several millivolts), offset drift, and 1/*f* noise. To mitigate these drawbacks, dynamic offset compensation (DOC) techniques, such as auto-zeroing and chopping, are often used to achieve low offset (microvolt level), offset drift (<20 nV/ºC), and 1/*f* noise corners (several Hertz). However, these techniques also have their own drawbacks, such as increased input current and distortion. In this thesis, various ways of mitigating these drawbacks are described. The resulting DOC amplifiers improve significantly on the state of the art, especially in terms of their input current and linearity. This chapter summarizes the main findings, other applications and discusses some future directions of research.

7.1 Original contributions

The main findings of this thesis are as follows:

- In DOC amplifiers, the charge injection mismatch of the input switches causes input current. Auto-zeroing requires half the number of switches compared to chopping and has a charge-sharing phase, which lowers the maximum input current four times. This makes it the prime candidate for low-input current amplifiers (Chapter 2).

- Due to the sampling of the input signal in auto-zero stabilized amplifiers, they exhibit significant distortion. In contrast, ping-pong auto-zero amplifiers can achieve lower intermodulation distortion (Chapter 2).

- Chopper-induced intermodulation distortion is caused by limited bandwidth of the chopped OTA, causing large pulses in the demodulated output current (Chapter 2).

- The pulses that cause the chopper-induced IMD can be significantly reduced by multiplexing between at least two OTAs (Chapter 5).

- The requirements of the fill-in OTA can be significantly relaxed by lowering the amount of time it is in the signal path. This means that the fill-in OTA does not need to be chopped and it can be heavily power-cycled to save power. (Chapter 6).

- Chopper-stabilized amplifiers with a low loop bandwidth will show their maximum intermodulation distortion around input frequencies close to the even multiples of the chopper frequency (Chapter 2).

- AZ stabilized amplifiers operate in two phases: a first phase in which their offset is sampled and a second phase in which the offset of a main amplifier is canceled. Due to the correlation in the noise of these two phases, the overall low-frequency noise density is limited to $\sqrt{5}\times$ the white noise level. By chopping the sources of correlated noise, the low-frequency noise density can be reduced to $\sqrt{3}\times$ the white noise level without introducing extra input current. Finally, by spending more time in the second phase, it can be lowered even further, to $\sqrt{2}\times$ the white noise level (Chapter 3).

- An auto-zero-stabilized voltage buffer can achieve sub-pA input current together with a quiet output that has no visible tones in its noise spectrum (Chapter 3).

- The input current of DOC amplifiers is mainly due to the charge injection mismatch of their input switches. This error can be made constant over input voltage by using a constant Vgs drive, after which it can be reduced to sub-pA levels by trimming. The trimming process is automated by observing the voltage droop of sampled voltage with a comparator (Chapter 4).

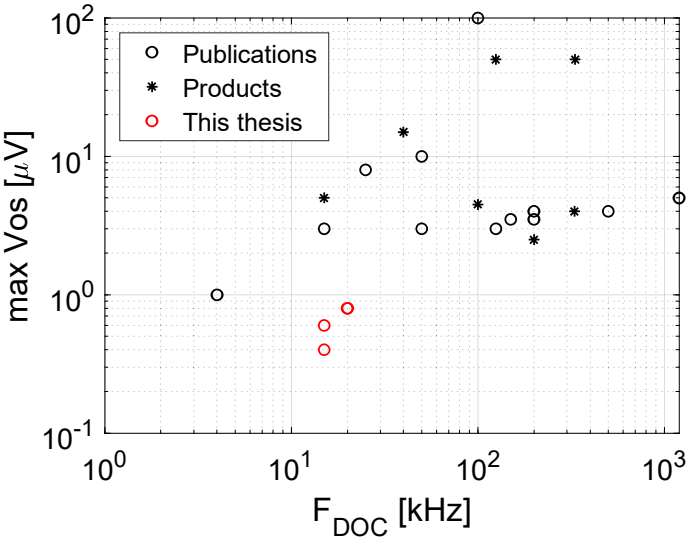

Fig. 7-1. Max offset voltage vs DOC frequency for state-of-the-art DOC amplifiers.

These findings have been confirmed by the measured performance of the DOC amplifiers presented in Chapters 3-6. As shown in Fig. 7-1, these amplifiers achieve state-of-the-art offset. In particular, the design presented in Chapter 3 achieves a max offset of 0.4μV, which is the lowest reported for a CMOS amplifier.

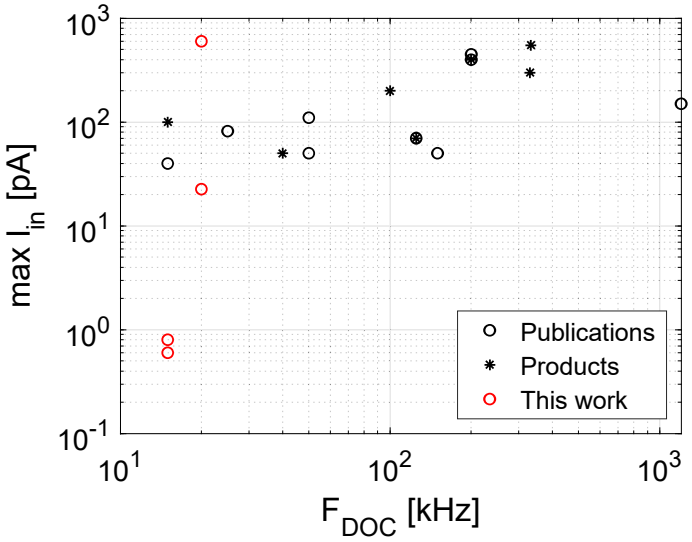

Fig. 7-2. Max input current vs DOC frequency for state-of-the-art DOC amplifiers.

The designs presented also achieve state-of-the-art input current, with the design in Chapter 4 achieving the best 0.2pA max after trimming and the design in Chapter 3 achieving 0.6pA max before trimming.

	DOC technique	DOC frequency [kHz]	Spread spectrum	Input frequency [kHz]	IMD [dB]
AD8551 [1.3]	Auto-zero stabilized	4	No	0.5	-80
AD8571 [1.4]	Auto-zero stabilized	2 to 4	Yes	0.5	-90
Ivanonv [1.5]	Chopper stabilized with RRL	50 to 150	Yes	1	-103 (w/ Spread) -122.7 (w/o Spread)
Chapter 4	Auto-zero stabilized	15	No	1 16	-91 -44
Chapter 5	Chopper stabilized with RRL	20	No	79	-97.7 (No Fill-in) -125.9 (Fill-in)
Chapter 6	Chopper stabilized with RRL	20	No	79	-102 (No Fill-in) -125.7 (Fill-in)

Table 7-1 – IMD for state-of-the-art chopper amplifiers

The AZ stabilized amplifiers presented in Chapter 4 operate in two phases: a first phase in which their offset is sampled and a second phase in which the offset of a main amplifier is canceled. During the second phase, a fraction of the input signal is sampled and then held in the subsequent phase, which causes significant intermodulation distortion. However, the chopper-stabilized amplifiers presented in Chapters 5 and 6 do not sample the input signal and, therefore, have better IMD. This is further improved by the use of the fill-in and relaxed fill-in techniques presented in Chapter 5 and 6, respectively. These amplifiers achieve state-of-the-art IMD with -125.9 dB at 79kHz.

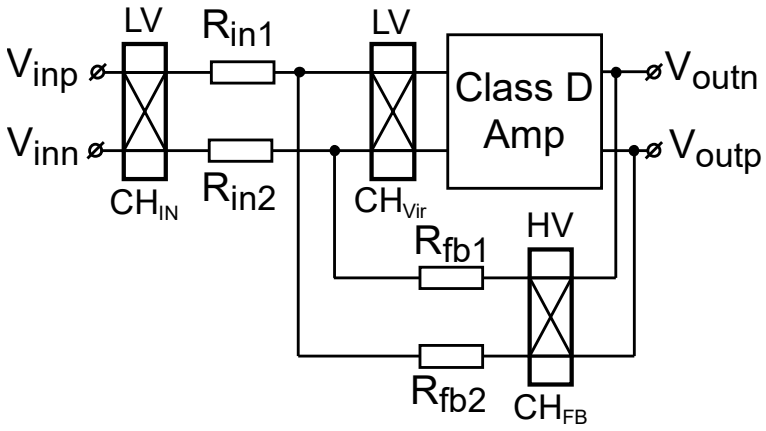

Fig. 7-3. Chopped Class-D Amplifier

7.2 Other applications

The insight that chopping a signal path with limited bandwidth or a non-zero delay causes output pulses, which, in turn, create distortion, can also be used in other applications. For example, in Class-D amplifiers, chopping minimizes the mismatch of feedback resistors, ensuring good PSRR (Fig. 7-3). However, the timing skew between the high voltage (HV) feedback choppers (CH_{FB}) and low voltage (LV) input choppers (CH_{IN}) causes pulses in the feedback current, which can be solved by multiplexing between two chopped feedback paths that are chopped in quadrature [7.1].

7.3 Future work

The DOC amplifiers presented in Chapters 3 and 4 significantly improve the input current (from tens of pA to hundreds of fA), quietness, and distortion performance of DOC amplifiers. However, there is still room for improvement. Several recommendations for future work are presented in the following sections.

7.3.1 Input current

The most straightforward way to lower the input current further is to reduce the required DOC frequency. However, this is ultimately limited by the $1/f$ corner frequency. While the $1/f$ corner frequency of the designs presented in Chapters 3 and 4 is relatively low due to the large transistor used in their input stages, the resulting corner frequency is around 10kHz. Further

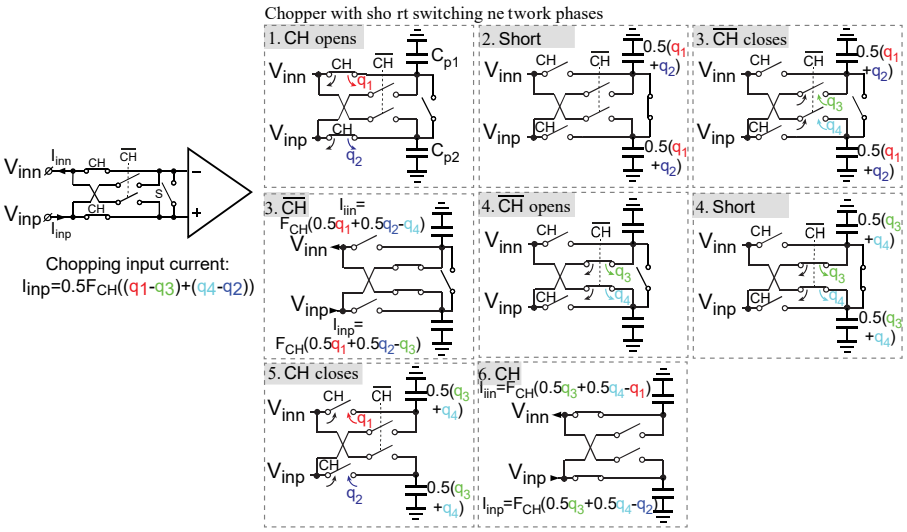

Fig. 7-4. Input current of chopper with short switches

optimization could be achieved by using source degeneration in the current sources of the input stages.

Another option would be to take advantage of technology scaling. The charge injection and charge injection mismatch benefit from smaller technologies. However, gate leakage and drain-source leakage will also increase, so an optimum could be investigated.

The analysis in Chapter 2 reveals that the maximum input current of chopper amplifiers is four times higher than that of AZ amplifiers. This difference could be reduced to a factor 2 by introducing a charge-sharing switch at the output of the chopper, as shown in Fig. 7-4. While this works well in theory and in simulation, it would be good to test it by fabricating a prototype that allows for the shorting to be turned on and off.

Finally, the input current of the DOC amplifiers presented in this work is lower than the leakage of typical ESD protection circuits. This means that in a general-purpose application, these designs are limited by the ESD leakage. Bootstrapped ESD diode structures have been successfully used in electrometer amplifiers [7.2]. These could also be applied to DOC amplifiers to achieve general-purpose low-input current DOC amplifiers.

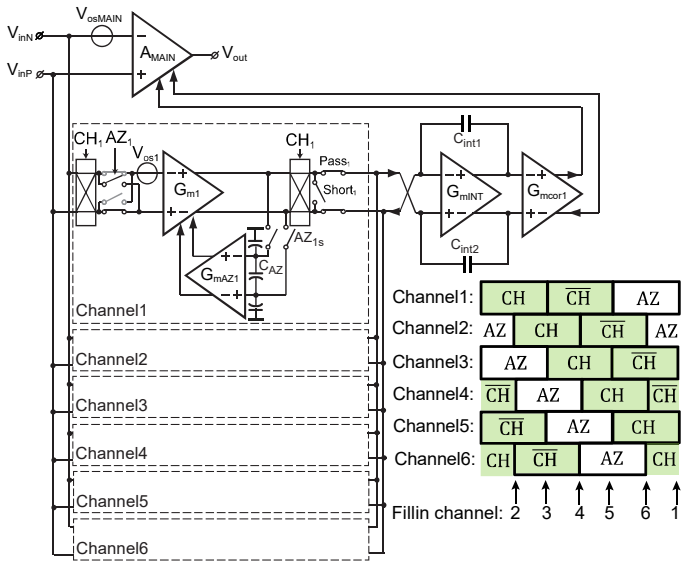

Fig. 7-5. Six-way interleaved chopper stabilized amplifier with fil-lin.

7.3.2 IMD

In the measured output spectra of chopper amplifiers, besides the expected even order IMD, odd order IMD is also observed. This odd-order IMD cannot be explained by the delay or bandwidth model presented in this thesis (Chapter 2). Simulations with mismatch in the chopper switches seem to indicate that this odd order IMD is caused by charge-injection mismatch spikes. Further research can be done to identify the exact cause and find potential solutions. If charge-injection mismatch spikes are the cause, trimming might be used to lower them.

To lower the overhead in power and area of the fill-in technique, the chopped OTA could be interleaved. In Fig. 7-5, an example is shown using six-way interleaving, where four OTAs are always in the signal path, one is auto-zeroing, and one is available for fill-in. This reduces the required transconductance per channel by a factor of four. In this way, the required current of the chopped input stages with fill-in is reduced from 2× to 1.5× at the cost of higher complexity.

The IMD achieved with the fill-in technique is limited by the matching of the transconductances. The required matching (about 5%) between the

transconductance for a level of 120dB is not very high and can be readily achieved by good layout. However, if even lower levels are required, the use of a gain error reduction loop [7.3] could be investigated to match the two transconductances automatically.

7.3.3 Quiet designs

The auto-zero amplifiers presented in this work did not show any spectral content at the auto-zeroing frequency. However, the spectrum of the presented chopper amplifiers does show spectral content at their chopping frequencies. By using the same techniques as the auto-zero amplifiers, the spikes in the chopper designs could be significantly lowered. The most important is proper shielding of all the capacitors, especially those connected to virtual grounds, and bringing the off-chip clock as a current to reduce the swing. Finally, using current mode logic can reduce the clock swing on-chip and the kicks on the supply, reducing the resulting spikes.

7.4 Concluding remarks

This thesis has discussed the development of DOC amplifiers with sub-pA input current and low distortion. This work has improved the input current by 120× while achieving a state-of-the-art offset of 0.4μV max. Furthermore, an AZ-stabilized amplifier has been developed without visible output spikes or tones in the noise spectrum. The cause of chopper-induced intermodulation has been investigated, and the resulting amplifiers with the fill-in technique lower the IMD by 28dB. However, there are still directions for further research. Chopper amplifiers still show higher input current, which could be potentially reduced by introducing a charge-sharing switch. Furthermore, their noise spectrums still show tones around the chopping frequency, which could be further lowered using the same design techniques as the quiet AZ design. Also, odd-order IMD is still visible in the spectrum and should be further investigated. Finally, the fill-in technique can also be applied in other areas where chopping (or dynamic element matching) is used and causes distortion, as has recently been done in Class-D amplifiers.

7.5 References

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Appendices

A.1 State-of-the-art input current and offset in chopper amplifiers

Papers

Reference	Iin [pA]	Vos [μV]	Fch [kHz]
Tang [1.8]	40	3	15
Kejariwal [1.14]	450	4	200
Burt [1.7]	70	3	125
Kusuda [1.11]	50	10	50
Fan [1.16]	110	3	50
Kusuda [1.17]	150	5	1200
Kusuda [1.18]	400	3.5	200
Ivanov [1.5]	50	3.5	150

Products

Reference	Iin [pA]	Vos [μV]	Fch [kHz]
AD8628 [1.19]	100	5	15
ADA4051[1.20]	50	15	40
ADA4523 [1.21]	300	4	330
ADA4528 [1.22]	400	2.5	200
LTC2057 [1.23]	200	4.5	100
OPA333 [1.24]	70	50	125
OPA378 [1.25]	550	50	333

A.2 Effect of technology scaling on charge injection

An important parameter for a MOS switch is the on-conductance (G_{on}), which is given by:

$$G_{on} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH}). \quad \text{(A-1)}$$

In this equation, μ is the mobility of the charge carriers. Comparing equations (1-1) and (A-1) shows that applications that require a large G_{on}, for example, to meet noise or distortion requirements, suffer from higher charge injection. Therefore, combining stringent noise or distortion specifications with low spikes and input current specifications is usually more difficult.

Technology scaling allows for the same G_{on} with a lower gate capacitance (WLC_{OX}). This means that modern processes suffer less from charge injection errors. An interesting metric to quantify this is the ratio of the on-conductance (G_{on}) and the channel charge Q:

$$\frac{G_{on}}{Q} = \frac{\mu}{L^2}. \quad \text{(A-2)}$$

This only depends on the mobility and the length of the transistor squared. The mobility of electrons and holes is fixed using a silicon substrate, while the minimum channel length is dependent on the technology. To maximize the conductance for a minimum amount of charge injection, a minimum length transistor in a modern technology is preferred.

A.3 Chopper-induced IMD with rectangular pulses

The sequence of rectangular pulses (p) can be described by the convolution:

$$p(t) = 2\mathrm{rect}\left(\frac{t}{T_{delay}}\right) * \sum_{n=-\infty}^{\infty} \delta\left(t - \frac{n}{2F_{CH}}\right) \tag{A-3}$$

where the rectangular function (rect) represents the short pulse caused by amplifier delay, and the impulse train represents its repetition rate (every $0.5/F_{CH}$). The Fourier transform of the first term is:

$$2T_{delay}\,\mathrm{sinc}(T_{delay}f) \tag{A-4}$$

and the Fourier transform of the second term is:

$$2F_{CH} \sum_{n=-\infty}^{\infty} \delta(f - n2F_{CH}). \tag{A-5}$$

The convolution in the time domain leads to a multiplication in the frequency domain, which results in:

$$p(f) = 4T_{delay}F_{CH}\mathrm{sinc}(T_{delay}f) \sum_{n=-\infty}^{\infty} \delta(f - n2F_{CH}). \tag{A-6}$$

The multiplication pV_{in} leads to the convolution:

$$\begin{gathered} p * V_{in}(f) = \\ 4T_{delay}F_{CH}\mathrm{sinc}(T_{delay}f) \sum_{n=-\infty}^{\infty} \delta(f - n2F_{CH}) * V_{in}(f) \\ = 4T_{delay}F_{CH}\mathrm{sinc}(T_{delay}f) \sum_{n=-\infty}^{\infty} V_{in}(f - n2F_{CH}). \end{gathered} \tag{A-7}$$

The frequency-shifted versions of the input spectrum leads to the IMD tones. pV_{in} is subtracted from V_{in} and multiplied by G_m, leading to an output current spectrum ($I_{out}(f)$) of:

$$I_{out}(f) = G_m V_{in} - \tag{A-8}$$

$$4T_{delay}F_{CH}\text{sinc}(T_{delay}f)G_m \sum_{n=-\infty}^{\infty} V_{in}(f - n2F_{CH}).$$

Looking at the ratio of the IMD tones to the input tone in dBs gives:

$$IMD_{OL} = 20\log\left(4T_{delay}F_{CH}\text{sinc}(T_{delay}f)\right). \quad \text{(A-9)}$$

The notches of sinc(T_{delay}f) occur at n/T_{delay} with n = 1,2,3,…. At low frequencies, the effect of the sinc function is negligible for a small T_{delay}. So, for IMD tones well below 1/T_{delay}:

$$IMD_{OL} = 20\log(4T_{delay}F_{CH}). \quad \text{(A-10)}$$

Using T_{delay} =1/(2πBW)

$$IMD_{OL} = 20\log\left(\frac{2F_{CH}}{\pi BW}\right). \quad \text{(A-11)}$$

A.4 Chopper-induced IMD with exponential settling

When exponential settling is considered, the rectangular pulses are replaced by exponentially settling pulses. The sequence of exponentially settling pulses can be described by:

$$p(t) = 2e^{-2\pi BWt}u(t) * \sum_{n=-\infty}^{\infty} \delta\left(t - \frac{n}{2F_{CH}}\right) \tag{A-12}$$

Where u(t) is the step function to describe single-sided exponential settling and BW is the amplifier's bandwidth. The Fourier transform of the first term is:

$$\frac{1}{\pi(BW + jf)} \tag{A-13}$$

Taking the amplitude, we end up with:

$$\frac{1}{\pi\sqrt{BW^2 + f^2}} \tag{A-14}$$

The rest is very similar to the analysis with the rectangular pulses. The convolution in the time domain leads to a multiplication in the frequency domain, which results in:

$$p(f) = \frac{2F_{CH}}{\pi\sqrt{BW^2 + f^2}} \sum_{n=-\infty}^{\infty} \delta(f - n2F_{CH}). \tag{A-15}$$

The multiplication pV_{in} leads to the convolution:

$$\begin{aligned} &p * V_{in}(f) = \\ &\frac{2F_{CH}}{\pi\sqrt{BW^2 + f^2}} \sum_{n=-\infty}^{\infty} \delta(f - n2F_{CH}) * V_{in}(f) \\ &= \frac{2F_{CH}}{\pi\sqrt{BW^2 + f^2}} \sum_{n=-\infty}^{\infty} V_{in}(f - n2F_{CH}). \end{aligned} \tag{A-16}$$

Leading to an output current spectrum ($I_{out}(f)$) of:

$$I_{out}(f) = G_m V_{in} -$$

$$\frac{2F_{CH}}{\pi\sqrt{BW^2+f^2}}G_m\sum_{n=-\infty}^{\infty}V_{in}(f-n2F_{CH}). \tag{A-17}$$

Looking at the ratio of the IMD tones to the input tone in dBs gives:

$$IMD = 20\log\left(\frac{2F_{CH}}{\pi\sqrt{BW^2+f^2}}\right). \tag{A-18}$$

This result differs slightly from the analysis with rectangular pulses. For high-frequency IMD tones, it shows a low pass filter characteristic with a cutoff frequency equal to the bandwidth and no notches from the sinc function. For the low-frequency IMD tones (f<<BW), this can be simplified to:

$$IMD = 20\log\left(\frac{2F_{CH}}{\pi BW}\right). \tag{A-19}$$

This is the same result as obtained by the rectangular pulses.

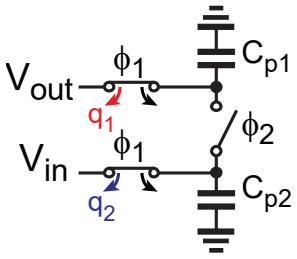

Fig. A1. Charge injection in typical AZ input switches.

A.5 Spikes

As mentioned in Chapter 1, DOC amplifiers suffer from spikes at their input and output. These spikes can be partly attributed to the charge injection of the input and output switching and partly to applying DOC with limited bandwidth [2.2]. The spikes due to the output switching and settling can be mitigated by making sure that they do not reach the amplifier output, while the spikes due to input switching are inevitable and can only be minimized.

A.5.1 Input switching spikes due to auto-zeroing

The charge injection of typical AZ input switches is shown in Fig. A1. The charge injection to the left side of the ϕ_1 switches (q_1 & q_2) directly leads to spikes at the output (V_{out}) and input (V_{in}). To avoid shorting the input, a non-overlapping switching scheme is preferred. However, in a non-overlapping scheme, the charge absorption of the ϕ_2 switches cannot compensate for this charge since the ϕ_1 switches disconnect them from input and output. For auto-zeroing, it is therefore advantageous to use either transmission gates or dummy switches to partly compensate the charge injection. However, as shown in chapter 3, the charge injection cancellation of transmission gates is input voltage dependent. Therefore, dummy switches are preferred.

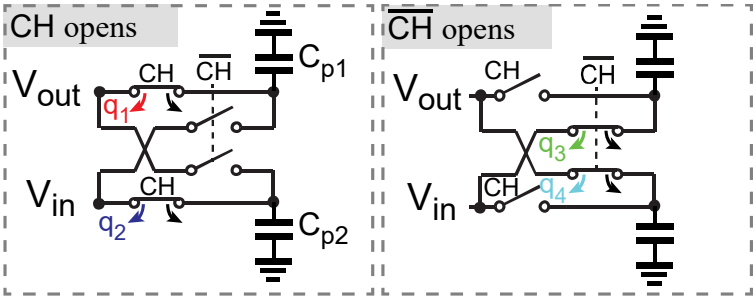

Fig. A2. Charge injection in an input chopper

A.5.2 Input switching spikes due to chopping

The charge injection of an input chopper is shown in Fig. A2. In choppers the charge injection of the CH switch (q_1) and $\overline{CH}$ switch can partly cancel. For proper suppression of the switching spikes, CH and $\overline{CH}$ need to switch synchronously. However, synchronous switching has the risk of overlap, so in practice only partial cancellation can be achieved.

A.5.3 Spikes due to output switching

Both chopping and auto-zeroing also generate spikes due to output switching. These are both due to the charge injection mismatch of the output switches and due to the limited bandwidth of the switched path. To minimize the effect of the spikes, the output can be briefly disconnected and shorted, to allow the spikes to settle.

A.5.4 Other sources of spikes

Other sources can also cause spikes. First, the required clock signal needs to be generated on-chip or brought on-chip. For an off-chip clock, the coupling from the bondwire can be the dominant source of spikes. To minimize this, a few things can be done. First, the clock can be brought in together with a complementary clock signal to try and cancel the effect of clock coupling, by balancing the injection from the clock and complementary clock. Second, the clock swing on the bondwire can be reduced. To minimize this, the clock can be brough in as a current. The AZ amplifier in Chapter 3 and 4 uses both current-input and complementary clocks, leading to no visible spikes. The CH amplifier in Chapter 5, does not use these techniques and shows significant spikes. The CH amplifier in Chapter 6, use a current-input clock but no complementary clocks, showing less spikes compared to the work in Chapter

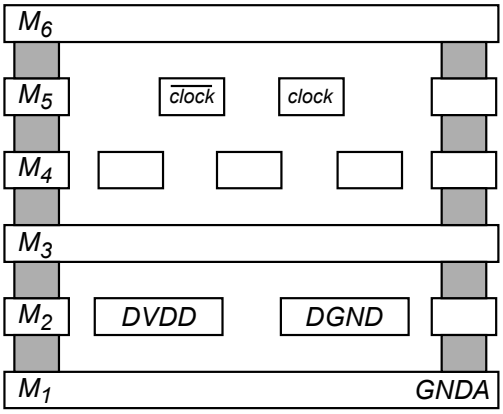

Fig. A3. Shielded coax for on-chip clock routing.

5. For an on-chip clock generator, coupling to sensitive analog nodes should be minimized. This coupling can either happen through capacitive coupling, substrate coupling or supply coupling.

To minimize capacitive coupling, especially the capacitors should be chosen well. MIM capacitors are often used, due to their high density. However, they are often implemented in the top metal layers, preventing shielding of the top plate of the capacitor. They can still be used if the top plate can be chosen as the ground. However, this is not always possible. Other good candidates are MOM capacitors, avoiding the top metal, and MOS capacitors.

To minimize substrate coupling, the dirty digital substrate should be isolated from the analog substrate. This can either be done by placing them in separate wells, if a deep n-well is available, or placing guard rings with substrate contacts around them.

To minimize supply coupling a few things can be done. The clock circuits can be driven as much as possible from an isolated supply. Finally, the last logic gate driving chopper and/or auto-zero switches is often driven by the analog supply. This prevents introducing the dirty digital supply directly in the analog domain. However, this also means that clock transients will be visible in the analog supply.

From the clock generator, the signals should be routed to the switches. This should be done in shielded on-chip coaxes. The clock and clock_bar signal should ideally be routed together in a symmetric fashion to compensate for any residual coupling. To preserve symmetry, the clock and clock_bar signals

might need to exchange places a few times on their way to the switches, to preserve symmetry.

Proper shielding of sensitive analog nodes is essential. Special care should be taken with capacitors used in analog circuitry and any virtual grounds. Ideally, capacitors should be shielded from all directions, i.e. top, bottom and sides. If MIM capacitors are used with top plates that cannot be shielded, the signal on the top plate should be the least sensitive signal. For example, in an integration capacitor, the top plate is preferably the output of the integrator and not the virtual ground. Care must be taken that the higher parasitic capacitance to ground by connecting the virtual ground to the bottom is not too big of a penalty, especially when this node is also shielded.

All these measures ensure that the spikes at the output are limited by the fundamental source, which is the charge injection and clock feedthrough of the input switches. This can lead to quiet DOC amplifiers, as presented in Chapter 3 and 4.

Summary

CMOS amplifiers suffer from high offset, offset drift, and 1/*f* noise. Dynamic offset compensated (DOC) techniques are often used to tackle these low-frequency errors. This thesis describes the theory, design, and implementation of amplifiers utilizing these techniques.

Chapter 1 is an introduction to this thesis. The DOC techniques, chopping, and autozeroing are introduced. Chopping separates the low-frequency errors from the signal in the frequency domain, while auto-zeroing separates them in the time domain. Next, the drawbacks of these techniques are introduced. Common to both techniques are spikes, input current, and residual offset due to charge injection and charge injection mismatch. Specific to auto-zeroing is noise folding, and specific to chopping is ripple and intermodulation distortion (IMD). The state-of-the-art techniques to mitigate these drawbacks are presented. While state-of-the-art DOC amplifiers can achieve very low offset (<10μV), they still have high input current (hundreds of pA) and clear visible tones in their spectrum. Due to the theoretical lower input current, auto-zero (AZ) amplifiers are the preferred candidate for developing low input current DOC amplifiers. Furthermore, they do not suffer from ripple, so they are also more suited for quiet amplifiers. However, AZ amplifiers still suffer from noise folding, while chopper amplifiers suffer from IMD, which should be addressed. This thesis aims to develop quiet AZ amplifiers with low input current and chopper amplifiers with low distortion.

In Chapter 2, the input current of auto-zeroing and chopping is analyzed. In theory, auto-zeroing can achieve a four times lower input current than chopping due to the lower number of switches and inherent charge sharing. The IMD in chopper amplifiers is caused by the delay resulting from the limited bandwidth of the chopped amplifier. In feedback amplifiers, loop gain helps to suppress IMD. In a chopper-stabilized amplifier, the stabilization loop filters the IMD, which can cause peaking around even multiples of the chopping frequency.

Chapter 3 describes an auto-zero stabilized voltage buffer that achieves low offset and low noise with sub-pA input current. A high-gain stabilization loop is used to cancel the buffer's offset periodically. The loop itself is periodically disconnected from the buffer and auto-zeroed, during which its bandwidth is reduced to reduce the associated noise folding. However, this also reduces its offset correction range, and so to avoid overloading, its initial

offset is digitally trimmed. To break up the correlation between the residual low-frequency noise of the auto-zero and stabilization phases, the loop is periodically chopped, significantly reducing the buffer's low-frequency noise. Finally, the duty-cycle of the two phases is optimized to bring the buffer's low-frequency noise density close to √2 times its white noise density (14 nV/√Hz), which is the fundamental limit of an AZ amplifier. The buffer also achieves a constant and low input current (0.8 pA) and a state-of-the-art offset (0.4 μV).

Chapter 4 presents an input-current trimming scheme for auto-zero amplifiers. Since their input current is mainly due to charge injection, the scheme operates by trimming the clock swing, and hence the charge injection, of two dummy input switches. At room temperature, the trimming scheme reduces the maximum input current of an auto-zero stabilized voltage buffer from 1pA to 0.2pA (13 samples) over its full input voltage range (0 to 1.3V). This increases to 0.4pA over temperature (0 to 85°C), which is well below the leakage of typical ESD diodes and is the lowest input current ever reported for an auto-zero amplifier.

Chapter 5 proposes using a so-called fill-in technique to eliminate the pulses caused by amplifier delay, and thus the resulting IMD, by multiplexing the outputs of two identical amplifiers that are chopped in quadrature. A prototype chopper-stabilized amplifier was implemented in a 180-nm CMOS process. Measurements show that the fill-in technique suppresses chopper-induced IMD by 28 dB, resulting in an IMD of −126 dB for input frequencies near four times the chopping frequency (=80 kHz). It also improves the amplifier's two-tone IMD (with 79 and 80 kHz inputs) from −97 to −107 dB, as obtained without chopping.

Chapter 6 presents a relaxed implementation of the fill-in technique in which the output of a fill-in OTA is only briefly used to avoid the spikes of a chopped main OTA. As a result, the fill-in OTA does not need to be chopped, so it can be duty-cycled to save power. Furthermore, the chopper ripple caused by the main OTA can now be suppressed by a single low-noise ripple-reduction loop rather than the two AZ loops required in a previous ping-pong implementation of the fill-in technique. Compared to the latter, the proposed amplifier achieves similar IMD performance (-125.7dB), a 25× lower input current (22.6pA), and a flat noise floor (12 nV/√Hz).

Chapter 7 presents the conclusions. The AZ amplifier presented in this thesis improves the state of the art in input current by 120× while also achieving a state-of-the-art offset of 0.4μV max. Furthermore, an AZ-

stabilized amplifier has been developed without visible output spikes or tones in the noise spectrum. The chopper amplifiers presented in this work achieve state-of-the-art IMD. Further work could still be done. Chopper amplifiers still show higher input current, which could theoretically be reduced by introducing a charge-sharing switch. Furthermore, their noise spectrums still show tones around the chopping frequency, which could be further lowered using the same design techniques as the quiet AZ design. Also, odd-order IMD is still visible in the spectrum and should be further investigated. Finally, the fill-in technique can also be applied in other areas where chopping (or dynamic element matching) causes distortion, as has recently been done in Class-D amplifiers.

Samenvatting

CMOS-versterkers hebben ongewenst hoge offset, offsetdrift en 1/*f*-ruis. Om deze laagfrequente fouten aan te pakken, worden vaak dynamische offsetcompensatie (DOC) technieken gebruikt. Dit proefschrift beschrijft de theorie, het ontwerp en de implementatie van versterkers die deze technieken gebruiken.

Hoofdstuk 1 is de inleiding van dit proefschrift. De dynamische offsetcompensatietechnieken: chopping en autozeroing worden geïntroduceerd. Chopping maakt onderscheid tussen de laagfrequente fouten en het signaal in het frequentiedomein, terwijl auto-zeroen ze onderscheid in het tijdsdomein. Vervolgens worden de nadelen van deze technieken geïntroduceerd. De gemeenschappelijke nadelen zijn uitgangspieken, ingangsstroom en resterende offset als gevolg van ladinginjectie en ongelijkheid in ladinginjectie. Specifiek voor autozeroing is het terugvouwen van ruis en voor chopping zijn uitgangsrimpel en intermodulatievervorming (IMD). De state of the art om deze nadelen te verminderen wordt gepresenteerd. Hoewel, state-of-the-art DOC-versterkers hele lage offset kunnen bereiken (<10µV), hebben ze nog steeds een hoge ingangsstroom (honderden pAs) en duidelijk zichtbare tonen in het spectrum. Door de theoretisch lagere ingangsstroom zijn auto-zero versterkers de voorkeurs kandidaat om lage ingangsstroom DOC-versterkers te ontwikkelen. Verder hebben ze geen last van uitgangsrimpel wat ze geschikter maakt voor stille versterkers. Echter hebben ze nog wel last van terugvouwende ruis en chopper versterkers van IMD. Het doel van dit proefschrift is om stille AZ-versterkers met lage ingangsstroom te ontwerpen en chopper versterkers met lage distorsie.

In Hoofdstuk 2 worden ingangsstroom en intermodulatievervorming geanalyseerd. In theorie kan auto-zeroing een vier keer lagere ingangsstroom bereiken dan chopping door het lagere aantal schakelaars en de inherente ladingsdeling. De IMD in chopperversterkers wordt veroorzaakt door de vertraging die optreed door de beperkte bandbreedte van de gechopte versterker. In feedbackversterkers helpt de lusversterking om IMD te onderdrukken. In een chopper gestabiliseerde versterker, filtert de stabilisatielus de IMD, wat kan zorgen voor pieken rond de even veelvouden van de chopper frequentie.

Hoofdstuk 3 beschrijft een auto-zero gestabiliseerde spanningsbuffer die een lage offset en lage ruis bereikt met sub-pA ingangsstroom. Een stabilisatielus met hoge versterking wordt gebruikt om de offset van de buffer periodiek te onderdrukken. De lus zelf wordt periodiek losgekoppeld van de buffer en geauto-zeroed, waarbij de bandbreedte wordt verminderd om de bijbehorende ruisvouwing te verminderen. Dit vermindert echter ook het offsetcorrectiebereik en om verzadiging te voorkomen, wordt de initiële offset digitaal getrimd. Om de correlatie tussen de resterende laagfrequente ruis van de auto-zero- en stabilisatiefasen te verbreken, wordt de lus periodiek gechopt, wat de laagfrequente ruis van de buffer aanzienlijk vermindert. Ten slotte is de duty-cycle van de twee fasen geoptimaliseerd om de laagfrequente ruisdichtheid van de buffer dicht bij $\sqrt{2}$ keer de witte ruisdichtheid (14 nV/$\sqrt{\text{Hz}}$) te brengen, wat de fundamentele limiet is van een AZ-versterker. De buffer bereikt ook een constante en lage ingangsstroom (0.8 pA), evenals een state-of-the-art offset (0.4 μV).

Hoofdstuk 4 presenteert een trimmethode voor de ingangsstroom van auto-zero-versterkers. Omdat hun ingangsstroom voornamelijk te wijten is aan ladinginjectie, werkt de methode door de klokzwaai, en dus de ladinginjectie, van twee dummy-ingangsschakelaars te trimmen. Bij kamertemperatuur verlaagt de trimmethode de maximale ingangsstroom van een auto-zero gestabiliseerde spanningsbuffer van 1 pA naar 0.2 pA (13 samples) over het volledige ingangsspanningsbereik (0 tot 1.3 V). Dit neemt toe tot 0.4 pA over temperatuur (0 tot 85 °C), wat ruim onder de lekstroom van typische ESD-diodes ligt en de laagste ingangsstroom is die ooit is gerapporteerd voor een auto-zero-versterker.

Hoofdstuk 5 stelt het gebruik van een zogenaamde fill-in-techniek voor om de pulsen veroorzaakt door de versterkervertraging, en dus de resulterende IMD, te elimineren door tussen de uitgangen van twee identieke versterkers te schakelen die in kwadratuur zijn gechopt. Een prototype chopper-gestabiliseerde versterker werd geïmplementeerd in een 180-nm CMOS-proces. Metingen tonen aan dat de fill-in-techniek chopper-geïnduceerde IMD met 28 dB onderdrukt, wat resulteert in een IMD van -126 dB voor ingangsfrequenties in de buurt van vier keer de chopperfrequentie (=80 kHz). Het verbetert ook de tweetoon IMD van de versterker (met 79 en 80 kHz ingangstonen) van -97 naar -107 dB, wat hetzelfde is als die verkregen zonder choppen.

In hoofdstuk 6 wordt een versoepelde implementatie van de fill-in techniek voorgesteld waarin de output van een fill-in OTA slechts kort wordt gebruikt om de spikes van een gechopte hoofd OTA te vermijden. Als gevolg

hiervan hoeft de fill-in OTA niet te worden gechopt, en kan deze dus periodiek worden uitgezet om energie te besparen. Bovendien kan de chopper rimpel veroorzaakt door de hoofd OTA nu worden onderdrukt door een enkele lage-ruis rimpelreductie lus, in plaats van de twee AZ-lussen die nodig waren in een eerdere pingpong implementatie van de fill-in techniek. Vergeleken met de laatste bereikt de voorgestelde versterker vergelijkbare IMD-prestaties (-125.7 dB), een 25× lagere ingangsstroom (22.6 pA) en een vlakke ruisvloer (12 nV/√Hz).

Hoofdstuk 7 presenteert de conclusies. De AZ-versterker gepresenteerd in dit proefschrift verbeterd de state of the art van ingangsstroom bij 120× terwijl het ook state of the art offset van 0.4μV max bereikt. Daarnaast is een AZ gestabiliseerde versterker ontwikkeld zonder zichtbare uitgangspieken of tonen in het ruisspectrum. De gepresenteerde chopper versterker bereikt state of the art IMD. Chopper versterkers hebben nog een hogere ingangsstroom, die potentieel gereduceerd kan worden door een lading delende schakelaar te introduceren. Verder laat het ruis spectrum nog steeds tonen zien rond de chopping frequentie, wat verder gereduceerd kan worden door dezelfde ontwerp technieken als de stille AZ-ontwerp. Verder is oneven IMD nog zichtbaar in het spectrum, wat verder onderzocht kan worden. Tenslotte, kan de fill-in techniek ook toegepast worden in andere gebieden waar chopping (of dynamic element matching) distorsie veroorzaak, zoals recent gedaan is in klasse D versterkers.

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This thesis marks the end of my PhD journey. When I started studying Electrical Engineering in 2009, I doubted if I could complete it. I truly never imagined that I would finish it with a PhD, albeit 15 years later. During this PhD journey, which started in 2017, I had the opportunity to work with and get support from many great people, to whom I want to address some words of appreciation.

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List of publications

Conference

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About the author

Thije Rooijers was born in Leiden, The Netherlands, in 1991. He received his B.Sc. and M.Sc. degrees in electrical engineering from Delft University of Technology, Delft, The Netherlands, in 2013 and 2016, respectively. In 2016, he worked as a researcher at Delft University of Technology, continuing his work on AZ amplifiers with a combination of low input current, low offset, and low noise. In 2017, he started pursuing a Ph.D. degree at Delft University of Technology, focusing on reducing the imperfections of dynamic offset compensated amplifiers. He is currently a senior analog and mixed-signal designer with Broadcom.

Mr. Rooijers was a recipient of the ADI Outstanding Student Designer Award in 2018, the ProRISC Best Oral Presentation Award in 2019, the ProRISC Best Poster Award in 2021, the silver price at the Huawei Student Design Contest 2021 and was one of the SSCS Predoctoral Achievement Award recipients in 2021-2022. He also serves as a Journal of Solid-State Circuits reviewer.