A Low-Voltage Low-Power Fully-Integratable Automatic Gain Control for Hearing Instruments

Wouter A. Serdijn, Albert C. van der Woerd, Jan Davidse, and Arthur H. M. van Roermund

Abstract— **A low-voltage low-power bipolar automatic gain control (AGC) for hearing instruments that works in the current domain and operates on a single 1.3-V battery is presented. In this AGC a large time constant (50 ms) is realized on-chip. The AGC consists of a gain cell, a comparator and a voltage follower. The active circuitry of the AGC has been integrated in the DIMES01 process and the total circuit demonstrates operation down to 1 V with only 4 μW power consumption. The compression range amounts to 38 dB. The AGC has a dynamic range (DR) of 62 dB at the output over a bandwidth of 10 kHz.**

I. Introduction

Apart from pitch, loudness and timbre, information in the world of sound is also characterized by more or less sudden temporary changes. For someone with hearing impairment these variations do not fit in his or her dynamic range and therefore there is either the lack of certain parts of the information or the pain limit is frequently exceeded. In this situation and *automatic gain control* (AGC) can offer certain improvement of the (speech) intelligibility.

An AGC is a circuit that automatically controls its gain in such a way that variations of the input signal result in smaller variations of the output signal. This control action is usually performed by means of a loop that contains a large time constant (e.g., several tens of milliseconds). In the past, this large time constant was realized by means of a large (external) capacitor [1], [2]. However, to reduce the size and production costs to a minimum, external components need to be avoided as much as possible. This also holds for the power supply; the use of more than one single zinc-air battery is precluded. This means that the AGC has to operate at "low-voltage level" (i.e., 1–1.3 V) and consume as little current as possible to ensure long battery life.

In practice two kinds of AGC's are found [3]: the input-controlled AGC-I and the output-controlled AGC-O. The AGC-I obtains its control signal from a signal in front of the volume control. In this way the control action will depend on the sound pressure level at the input of the hearing instrument. The control signal of the AGC-O is derived from the signal behind the volume control. The control action then depends on the sound pressure level that is offered to the ear.

Both AGC's differ from each other so far as that the control range of the AGC-I is always larger (for example, 60 dB) while for the AGC-O often 20 dB is enough. Also the compression ratio is different: e.g., between 1.5–10 for the AGC-I and infinite for the AGC-O.

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The authors are with the Department of Electrical Engineering, Delft University of Technology, 2628 CD Delft, the Netherlands.

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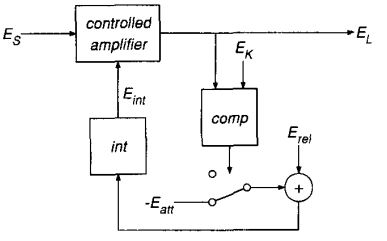

Fig. 1. Block diagram of an automatic gain control.

The circuit that is described here is an AGC-O with an infinite compression ratio. Section 2 presents a block diagram of an AGC that operates in the current domain, consisting of three sub-circuits: a *gain cell*, a *comparator*, and a *voltage follower*. Their design is presented in Section 3. In Section 4 the circuit diagram of the complete AGC is presented. As an example the active circuitry was integrated in the DIMES01 process. In Section 5 experimental results are given.

II. An AGC in the Current Domain

In Fig. 1 a typical AGC circuit is drawn. The output signal E_L is compared with a reference level E_K (the knee level) by a comparator that determines whether the integrating circuit—in practice often nothing more than an RC network—is charged (by $E_{\rm att}$—$E_{\rm rel}$) or discharged (by $E_{\rm rel}$). The output signal of the integrator $E_{\rm int}$ forms the control signal of the controlled amplifier. The operation is as follows: when $E_{\rm att}$ is larger than $E_{\rm rel}$ the output signal E_L is controlled towards the knee level E_K. Variations of the input signal therefore always result in smaller or equal variations of the output signal. The control action needs some time. This can be described by the expressions *attack time* and *release time*. The attack time is defined as the time needed for the AGC to respond to a sudden 25 dB increase of the input signal until the output signal is within 2 dB from its final value [4]. Vice versa, the release time is defined as the time needed to respond to a sudden 25 dB decrease of the input signal until the output signal is within 2 dB from its final value. The attack time and the release time must be < 5 ms and 50 ms, respectively.

Low-voltage low-power circuits preferably operate in the current domain [5]. This leads to the circuit diagram of Fig. 2. Apart from $E_{\rm int}$ all signals are now represented by currents. The output of the integrator is a voltage, as the

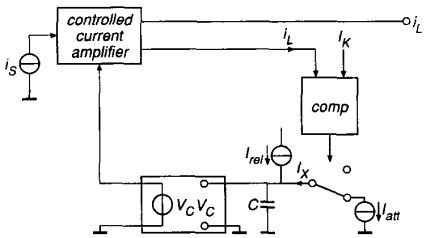

Fig. 2. Block diagram of an AGC operating in the current domain.

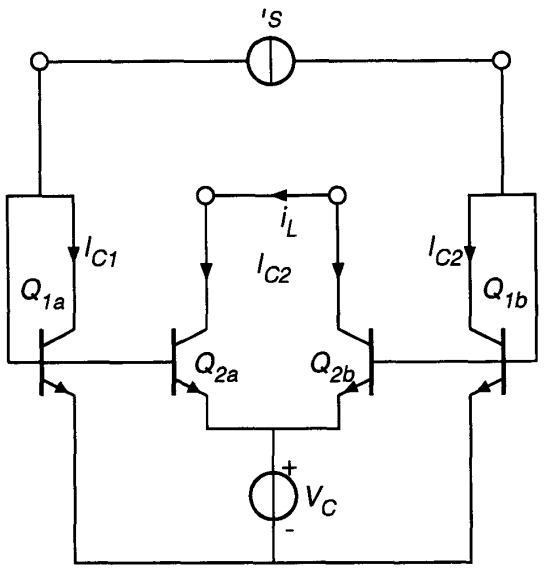

Fig. 3. A symmetrical current mirror, also known as a *Beta-Immune Type 'A' Cell.*

only integratable integrating element is a capacitance. The capacitance is followed by a voltage follower that generates a low-impedance version of V_C.

III. Design of the Subcircuits

So far the AGC has been designed at *system level.* We now take a closer look at the design of its components: the controlled amplifier, the comparator (including the switch and current source I_{att}) and the voltage follower.

A. Design of the Controlled Amplifier

A suitable controlled amplifier is the symmetrical version of a current mirror, also known as a *Beta-Immune Type 'A' Cell* [6, Chapter 2] (Fig. 3). This is a controlled current amplifier of which the gain equals the ratio of the (dc) collector currents I_{C2} and I_{C1}.

Another way of controlling the ratio of I_{C2} and I_{C1} is by means of controlling voltage V_C connected between the emitter of Q_1 and the emitter of Q_2. We now obtain a gain, G, that

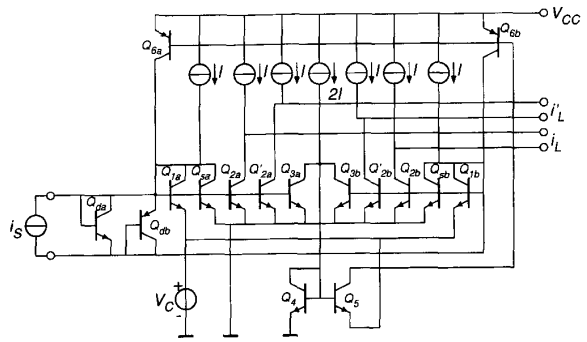

Fig. 4. A symmetrical current mirror as used in the controlled amplifier including its biasing circuitry.

is proportional to the anti-log of V_C, or

$$G = i_{C2}/i_{C1} = e^{V_C/V_T} \approx 335V_C \,\text{dB}, V_C \,\text{in V} \qquad (1)$$

in which V_T equals the thermal voltage kT/q, approximately 26 mV at 300 K.

This exponential relationship between the gain G and the control voltage V_C enables us to control the gain over a wide range and is also perceptibly the most comfortable. If V_C is made proportional to the absolute temperature, the gain is independent of the temperature as well.

A possible implementation of a voltage-controlled symmetrical current mirror is given in Fig. 4. Transistors Q_{1a} and Q_{1b} are the input transistors. Q_{2a} and Q_{2b} deliver the output current $i_L \cdot Q'_{2a}$ and Q'_{2b} are the output transistors for i'_L. The circuit also contains a *common-mode loop* [7]–[9] for biasing the transistors correctly ($Q_{3a}, Q_{3b}, Q_4, Q_5, Q_{6a}$, and Q_{6b}). The collector currents of both Q_{3a} and Q_{3b}, that equal the collector currents of both Q_{2a} and Q_{2b}, are added and compared with a current $2I$. The error signal controls via Q_4, Q_5, Q_{6a}, and Q_{6b} the collector currents of Q_{1a} and Q_{1b}. Because the gain in this loop, the *common-mode loop gain*, equals the current gain factor B_F of Q_{6a} and Q_{6b}, which is much larger than one, the error signal is nullified and the symmetrical current mirror is biased correctly. Q_{sa} and Q_{sb} limit the maximum gain of the amplifier to one. Q_{da} and Q_{db} shunt the input and prevent the amplifier from saturating.

B. Design of the Comparator

The comparator is the subcircuit that decides whether the output current i'_L of the controlled amplifier is larger or smaller than the reference level I_K. For this purpose we can again use a symmetrical current mirror, now acting as an amplifier with a saturated input-output relation. Its implementation is given in Fig. 5. $Q_{3a}, Q_{3b}, Q_4, Q_5, Q_{6a}, Q_{6b}$, and Q_{6c} form the common-mode biasing circuitry. In this case the *common-mode loop gain* is kept sufficiently low (i.e., equals 2) to prevent instability in the comparator. The output current I_X therefore switches between 0 and $\frac{2}{3}I$. The two diode-connected transistors Q_{da} and Q_{db} prevent the amplifier from saturating; the comparator switches faster.

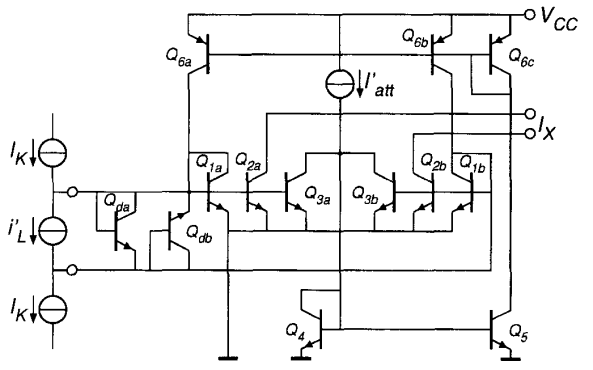

Fig. 5. A symmetrical current mirror used as a comparator. The common-mode loop gain equals two to prevent instability.

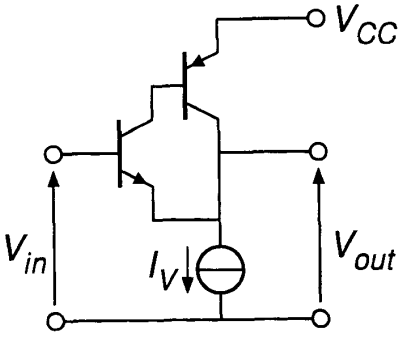

Fig. 6. A two-transistor voltage follower.

C. Design of the Voltage Follower

The voltage follower forms a buffer between the capacitance C and the controlled amplifier. A single Field-Effect transistor (JFET or MOST) would perform this task very well, but as such devices are not yet well specified for applications in low-voltage circuits, a sufficiently high input impedance should be created by means of negative feedback [10]. A two-transistor solution is given in Fig. 6. Although it might be confusing to see that the output voltage differs a base-emitter voltage from the input voltage, we have to consider that the voltage follower is part of a loop; the loop will control correctly.

IV. Overall Design

Now that all the different parts of the AGC have been designed at circuit level, all the subcircuits are linked together, and we take a closer look at the numerical values and the remaining bias circuitry.

When driving the filter as presented in [11] the maximum output current of the AGC circuit is chosen to be 25 nA (peak value). The reference current I_K (Fig. 2) therefore has been chosen to be equal to 25 nA. The current source I as depicted in Fig. 4 has been chosen well above 25 nA and equals 100 nA.

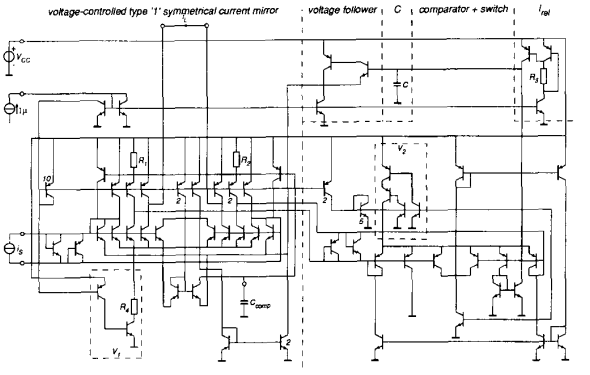

Fig. 7. The total automatic gain control. Instability may be counteracted by C_{comp}.

The values of I_{att} and I_{rel} can be derived from the attack time and the release time. Some calculation yields

$$I_{\text{att}} = \frac{5.2V_T C}{t_{\text{att}}} + I_{\text{rel}} \tag{2}$$

and

$$I_{\text{rel}} = \frac{2.6V_T C}{t_{\text{rel}}}. \tag{3}$$

For $I_{att'}$ (Fig. 5) it follows

$$I_{\text{att}'} = \frac{3}{2} I_{\text{att}} = \frac{7.8V_T C}{t_{\text{att}}} + \frac{3}{2} I_{\text{rel}}. \tag{4}$$

With $t_{\text{att}}, t_{\text{rel}}$ and C equal to 4 ms, 50 ms, and 400 pF, respectively, this results in 20 nA and 540 pA for $I_{\text{att}'}$ and I_{rel}.

The current source I_V (Fig. 6) supplies the collector current of the p-n-p transistor in the voltage follower and is chosen to be equal to 1 μA.

All these currents can be derived from a single current by means of current mirrors with multiple outputs and convenient scaling factors. The scaling factor can be obtained by choosing either a proper emitter area ratio or by means of resistors. The latter solution yields either a *Widlar mirror* or a *gm-compensated mirror* [6, Chapter 6].

The total circuit diagram of the AGC is depicted in Fig. 7. Two voltage sources (V_1 and V_2) have been added to prevent the current sources I_V and I_K from saturating. V_1 has been realized by means of a saturating n-p-n transistor and a resistor. V_2 contains two saturating p-n-p transistors in series. In this way their voltages are well above the saturation voltages of I_V and I_K.

In case of (common-mode) instability a capacitance C_{comp} can be added.

V. Experimental Results

The active circuitry of the circuit shown in Fig. 7 was integrated in the DIMES01 process (5 GHz, 2 μm), fabricated at the Delft Institute of Microelectronics and Submicron

TABLE I
MEASUREMENT RESULTS OF THE AGC

Parameter	Value	Unit
Compression range	38	dB
Attack time, $i_s = 1\mu$ A_p, 1 kHz	4.2	ms
Release time, $i_s = 10$ nA_p, 1 kHz	58	ms
Dynamic Range, $G = 1$, $B = 10$ kHz	62	dB
Bandwidth	> 100	kHz
Min. supply voltage	1	V
Supply current, $G = 1$	4	μA

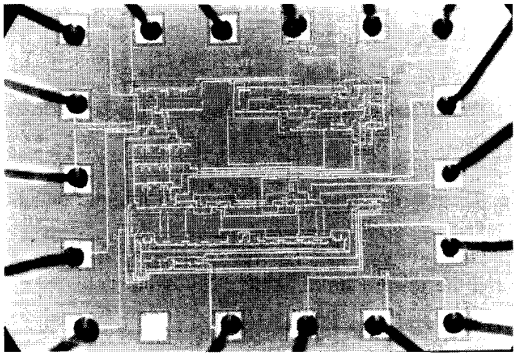

Fig. 8. Photograph of the integrated circuit.

Technology. Fig. 8 shows a microphotograph of the chip. Experiments proved the correct operation of the AGC. Table I gives the measurement results. No instability occurred. The relatively large value of the release time is caused by the base current of the first stage of the voltage follower. However, this did not pose a problem in our application.

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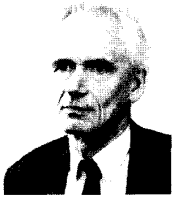
Wouter Serdijn was born in Zoetermeer, the Netherlands, in 1966. He started his study at the Faculty of Electrical Engineering at the Delft University of Technology in 1984, and received the "ingenieurs" (M.Sc.) degree in 1989.

Subsequently, he joined the Electronics Research Laboratory of the same university where he received the Ph.D. degree in 1994. His research includes developing a formal design theory for low-voltage low-power analog integrated circuits along with the development of circuits for hearing instruments.

Albert C. van der Woerd was born in 1937 in Leiden, the Netherlands. In 1977 he received the "ingenieurs" (M.Sc.) degree in electrical engineering from the Delft University of Technology, Delft, the Netherlands. He was awarded the Ph.D. degree in 1985.

From 1959 to 1966 he was engaged in research on and development of radar and TV circuits with several industry laboratories. In 1966 he joined the Electronics Research Laboratory of the Faculty of Electrical Engineering of the Delft University of Technology. During the first 11 years he carried out research on electronic musical instruments. The next 8 years his main research subject was on carrier domain devices. The last years he has been specialized in the field of low-voltage low-power analog circuits and systems. He teaches design methodology.



Jan Davidse received the M.Sc. degree in electrical engineering from Delft University of Technology in 1953 and subsequently the Ph.D. degree from Eindhoven University of Technology.

He was research scientist with Philips Research Laboratories and received a full professorship in electronics at the Delft University of Technology in 1964. From 1964 to the present, he has been head of the laboratory for Electronics at this university. His research interest is in analog electronics and in electronic pictorial techniques. He is the author of numerous papers and holds several patents in his field of interest. He is the author of ten books, among which is *Analog Electronic Circuit Design,* Englewood Cliffs, NJ: Prentice Hall, 1991.

Arthur H. M. van Roermund was born in Delft, The Netherlands in 1951. He received the M.S. degree in electrical engineering in 1975 from the Delft University of Technology and the Ph.D. degree in Applied Sciences from the K. U. Leuven, Belgium, in 1987.

From 1975 to 1992 he was with the Philips Research Laboratories in Eindhoven. First he joined the Consumer Electronics Group, where he has been involved with the design and integration of analog circuits and systems, especially switched-capacitor circuits. In 1987 he joined the Visual Communications Group where he has been engaged in video architectures and digital video signal processing. From 1987 to 1990 he was project leader of the Video Signal Processor project and from 1990 to 1992 of a Multi-Window Television project. Since 1992 he has been a full professor at the Electrical Engineering Department of the Delft University of Technology. He heads the Electronics Laboratory, which is part of DIMES: the Delft Institute of Micro Electronics and Submicron technology.