# A Single-Stage Dual-Output Regulating Voltage Doubler for Wireless Power Transfer

Lu, Tianqi; Makinwa, Kofi A.A.; Du, Sijun

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# A Single-Stage Dual-Output Regulating Voltage Doubler for Wireless Power Transfer

Tianqi Lu, *Graduate Student Member, IEEE*, Kofi A. A. Makinwa, *Fellow, IEEE*, and Sijun Du, *Senior Member, IEEE*

***Abstract*— A single-stage dual-output regulating voltage doubler (DOVD) is proposed for biomedical wireless power transfer (WPT) systems. Derived from the full-wave voltage doubler (VD) topology, it achieves ac-to-dc rectification and dual-output voltage regulation in a single stage by using only two power transistors. The DOVD's inherent voltage conversion ratio (VCR) of 2 enhances the overall voltage gain of a WPT system, thus extending the transfer range against varying link conditions. To eliminate cross-regulation between the two outputs and provide fast load-transient responses, a parallel pulse-frequency modulation (PPFM) controller is proposed. In addition, a digital-tuning adaptive delay compensation technique with fast error-variation responses is proposed to achieve soft-switching in the power stage. Implemented in a 180-nm Bipolar-CMOS-DMOS (BCD) technology and operating at 6.78 MHz, the proposed DOVD achieves dual regulated outputs at 1.8 and 3.3 V, a VCR of up to 1.875, and a power conversion efficiency (PCE) of up to 92.95% over an output power range of 2.6–90.5 mW. It also achieves instant load-transient responses and unnoticeable cross-regulation during 25× load transients at both outputs.**

***Index Terms*— Biomedical implantable devices, dual output, regulating rectifier, single-stage receiver (RX), voltage doubler (VD), wireless power transfer (WPT).**

## I. Introduction

WIRELESS power transfer (WPT) holds great promise as a solution for powering biomedical implantable devices, such as neural stimulators, retinal prostheses, and brain interfaces [1]. In biomedical WPT systems, the relative displacement between the transmitter (TX) coil and the receiver (RX) coil often leads to variations in the coupling condition. This variability impacts the voltage conversion ratio (VCR) across the link, resulting in voltage fluctuations at the RX side, as depicted in Fig. 1. These fluctuations pose a challenge for the RX circuit, which must consistently provide a regulated dc supply voltage to the functional blocks in the biomedical device. On the other hand, advanced biomedical devices typically require multiple independent supply voltages to power various functional blocks, including analog amplifiers, digital logic cells, memory, etc. Meeting this requirement adds another challenge to the RX circuit design.

A typical RX circuit consists of a rectifier followed by a dc–dc converter [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13]. The rectifier performs ac-to-dc conversion, and the dc–dc converter provides a regulated dc output. A straightforward approach is to combine a full-bridge rectifier (FBR) with a low-dropout regulator (LDO) [2], [3], [4]. However, the FBR has an inherent VCR of 1, and the LDO can only perform step-down voltage conversion. This necessitates a high power output from the TX side to compensate for varying link conditions. To enhance the VCR at the RX side, voltage doubler (VD) or voltage multiplier-based topologies have been proposed [5], [6], [8], [9]. Alternatively, the LDO can be replaced by switching-mode converters or charge pumps [11], [12], [13]. Such techniques improve RX performance under variable link conditions. However, the multistage structures and extra components they require inevitably cause cascaded power losses and increase system volume and cost.

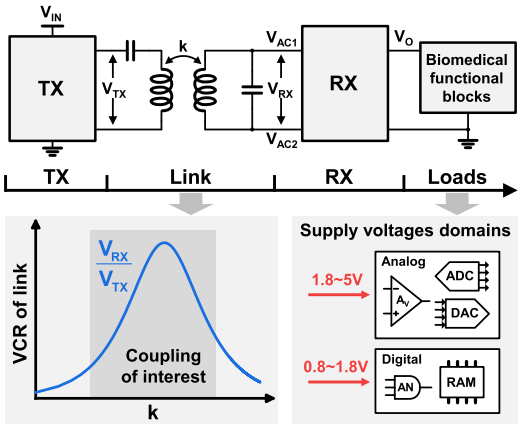


Fig. 1. Biomedical WPT system with varying link conditions and dual-output requirement.

To address the limitations of multistage structures, regulating rectifiers have been introduced, which simultaneously perform voltage rectification and regulation in a single power stage to avoid cascaded efficiency loss [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25]. As shown in Fig. 2(a), such rectifiers are similar to an FBR in which voltage regulation is realized by controlling the ON/OFF duty cycle of the power stage [16], [17], [18], [19], [23]. Though they improve power conversion efficiency (PCE) and power density by simplifying the power stage, they do not improve the VCR. Adding a voltage step-up stage can increase the output voltage, but this is at odds with the single-stage approach. In [22], a reconfigurable 1×/2× regulating rectifier is proposed, which combines an FBR and a VD in the power stage, as shown in Fig. 2(b). It regulates the output voltage by reconfiguring the power stage as either an FBR or a VD, thus enabling a VCR between 1 and 2 depending on the reconfiguration

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The authors are with the Department of Microelectronics, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: sijun.du@tudelft.nl).

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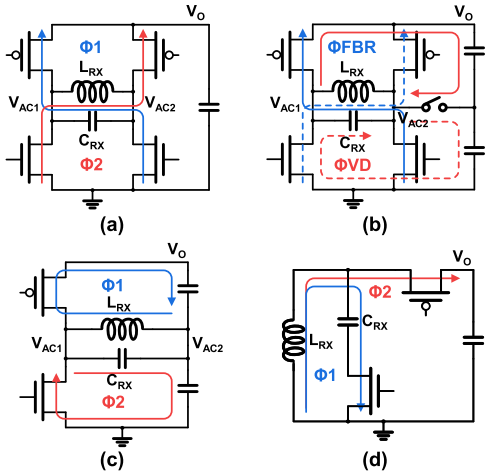



Fig. 2. Conventional single-stage single-output RX structures. (a) FBR-based regulating rectifier [19]. (b) 1×/2× regulating rectifier [22]. (c) VD-based regulating rectifier [25]. (d) RCM rectifier [27].

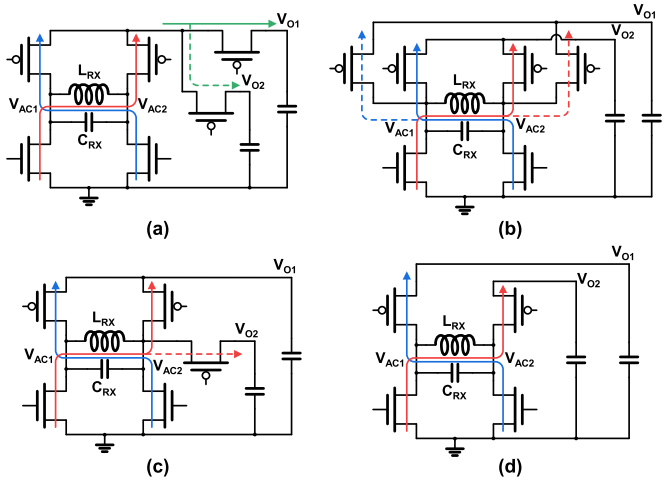



Fig. 3. Conventional single-stage dual-output RX structures. (a) FBR with output selection [31]. (b) FBR with two pairs of upper paths [21], [24]. (c) FBR with 1.5 pairs of upper paths [23]. (d) FBR with separated upper paths [17].

duty ratio. However, this technique complicates the power stage and requires further TX power tuning to maintain stable operation [26]. A regulating VD with a VCR of 2 is proposed in [25], as shown in Fig. 2(c), which improves the VCR and uses hysteresis-based output regulation to achieve stable ON/OFF operation. The VCR at the RX side can also be enhanced by a resonant current-mode (RCM) RX [27], as depicted in Fig. 2(d). It has two operating phases: an $LC$ resonance phase and a charging phase. By resonating for several consecutive periods, the RCM RX can accumulate the received ac energy, resulting in a primarily high VCR [28], [29]. Unfortunately, RCM topologies often struggle to achieve effective output regulation in a single stage without sacrificing PCE, due to the highly energetic $LC$ resonance phase. Moreover, charging frequencies are significantly lower than those of their VM counterparts.

To provide multiple regulated outputs at the RX side, multistage RX structures typically employ additional power stages. In [5] and [6], multiple parallel dc–dc converters are used after the rectification stage. Though adding more power stages eliminates cross-regulation between these regulated outputs, it requires even more power components. Lu et al. [30] present a dual-output two-stage RX where the second stage is a single-inductor dual-output (SIDO) dc–dc converter. This approach consolidates the multioutput function into a single power stage; however, it still employs a two-stage structure.

In single-stage RX structures, multiple outputs can be achieved by introducing additional power branches. As in a SIDO dc–dc converter, a dual-output regulating rectifier can be made by adding two output selection switches [31], as shown in Fig. 3(a). However, this method uses three power transistors in the conduction paths, resulting in high conduction losses. In [21], [24], and [16], the FBR is equipped with two pairs of upper paths, both of which are activated alternately, as illustrated in Fig. 3(b). The performance of this approach is only slightly worse than that of a single-output FBR. In [23], a dual-output FBR (DOFBR) with a single switch in the second upper path is presented [see Fig. 3(c)]. This design can be seen as a modified version of the topology in Fig. 3(b) and saves one power transistor by supporting the second output with half-wave operation. In Fig. 3(d), Lin et al. [17] introduce a DOFBR that separates the original pair of upper paths into two independent paths, each connected to one of the outputs. This is equivalent to driving the two outputs with two half-bridge rectifiers (HBRs). Compared to the topology in Fig. 3(b), it saves two power transistors but excludes the use of full-wave operation for each output. Although these four typologies all meet the multioutput requirement, they are all FBR-based, resulting in a limited VCR (<1). Additionally, they all require at least two power transistors in the conduction paths, contributing to high conduction losses.

In this article, a single-stage dual-output regulating VD (DOVD) is proposed, achieving ac-to-dc rectification and dual-output voltage regulation in a single stage with only two power transistors [32]. It has a theoretical VCR of 2 and uses only one power transistor in each output path, optimizing the PCE-VCR trade-off in a single-stage dual-output RX structure. With a dedicated parallel pulse-frequency modulation (PPFM) controller design, cross-regulation between the two outputs is eliminated, while fast load-transient responses can also be achieved. With the help of digital-tuning adaptive delay compensation, the DOVD achieves near-optimal soft-switching in the power stage. The remainder of this article is organized as follows. Section II introduces the proposed DOVD topology and its operations. Section III presents the system architecture and key circuit implementations. Section IV shows the measurement results. Section V provides discussions and Section VI concludes this article.

## II. Proposed Dual-Output Voltage Doubler

Fig. 4 illustrates the topology of the proposed single-stage DOVD. It consists of two power transistors, $M_P$ and $M_N$, and two stacked output capacitors, $C_{O1}$ and $C_{O2}$. Switch $S_{FW}$ will be activated in the freewheeling phase. Although the DOVD's power stage configuration is similar to that of a full-wave VD, both of its dc outputs are regulated, labeled as $V_{O1}$ and $V_{O2}$. $C_{O1}$ is charged via path 1, the upper path, while $C_{O2}$ is charged via path 2, the lower path. As a result, $V_{O1}$ can be supported by full-wave operation, while $V_{O2}$ is supported by half-wave

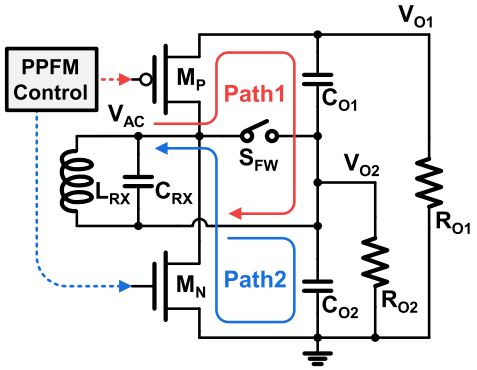



Fig. 4. Proposed single-stage DOVD.

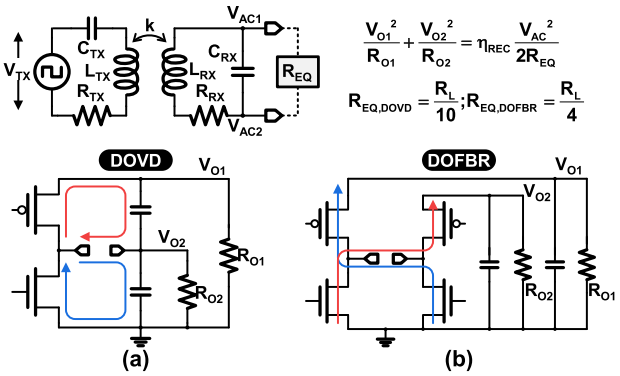



Fig. 5. WPT system model with (a) proposed DOVD and (b) DOFBR presented in [17].

operation. $R_{O1}$ and $R_{O2}$ mimic the load conditions of $V_{O1}$ and $V_{O2}$, respectively.

### A. System VCR Analysis

To compare the proposed DOVD with a conventional DOFBR, both are tested with identical inductive links (see Fig. 5). The DOFBR in [17] is chosen because it exhibits a VCR similar to other FBR-based topologies while naturally providing two outputs without a dedicated controller. In the steady state, the equivalent input resistances $R_{EQ}$ of the DOVD and the DOFBR can be determined by analyzing the power relationship at the RX side

$$\frac{V_{O1}^2}{R_{O1}}+\frac{V_{O2}^2}{R_{O2}}=\eta_{RX}\frac{V_{ac}^2}{2R_{EQ}} \tag{1}$$

where $\eta_{RX}$ is the PCE of the RX circuit, and $V_{ac}$ is the amplitude of the ac input voltage, $V_{AC1}-V_{AC2}$, which is assumed to be a sinusoidal waveform for simplicity. The power relationship in the DOVD can be further expressed as

$$\frac{V_{O1}^2}{R_{O1}}+\frac{V_{O2}^2}{R_{O2}}=\frac{\eta_{RX}}{2}\left(\frac{(V_{O1}-V_{O2})^2}{2R_{EQ}}+\frac{V_{O2}^2}{2R_{EQ}}\right). \tag{2}$$

As a result, $R_{EQ}$ can be expressed as

$$R_{EQ}=\eta_{RX}\frac{\left[(V_{O1}-V_{O2})^2+V_{O2}^2\right]R_{O1}R_{O2}}{4\left(R_{O2}V_{O1}^2+R_{O1}V_{O2}^2\right)}. \tag{3}$$

Assuming $\eta_{RX}=1$, $V_{O1}=2V_{O2}$, and $R_{O1}=R_{O2}=R_L$, $R_{EQ}$ of DOVD can be expressed as

$$R_{EQ,DOVD}=\frac{R_L}{10}. \tag{4}$$

The power relationship in the DOFBR is given by

$$\frac{V_{O1}^2}{R_{O1}}+\frac{V_{O2}^2}{R_{O2}}=\frac{\eta_{RX}}{2}\left(\frac{V_{O1}^2}{2R_{EQ}}+\frac{V_{O2}^2}{2R_{EQ}}\right). \tag{5}$$

Assuming $\eta_{RX}=1$, $V_{O1}=V_{O2}$, and $R_{O1}=R_{O2}=R_L$, $R_{EQ}$ of DOFBR can be expressed as

$$R_{EQ,DOFBR}=\frac{R_L}{4}. \tag{6}$$

The DOVD has a smaller $R_{EQ}$ than the DOFBR, reflecting its higher VCR. The VCR of a WPT system is defined as the ratio of its dc output, $V_{O1}$, and the amplitude of $V_{TX}$. Referred to [33] and [34], the system VCR, $VCR_{SYS}$, can be expressed as

$$VCR_{SYS}=\frac{knQ_1Q_2}{1+Q_2Q_L+k^2Q_1Q_2}\eta_{RX}VCR_{RXideal} \tag{7}$$

where $k$ is the coupling coefficient between $L_{TX}$ and $L_{RX}$; $n$ is the coil turns-ratio defined as $(L_{RX}/L_{TX})^{1/2}$; $VCR_{RXideal}$ is the ideal VCR of the RX circuit; $Q_1$ is the quality factor of the TX coil driving its coil resistance; $Q_2$ is the quality factor of the RX coil driving its coil resistance; and $Q_L$ is the quality factor of the RX coil driving the RX circuit ($R_{EQ}$). These three quality factors can be given by

$$Q_1=\frac{\omega L_{TX}}{R_{TX}};\quad Q_2=\frac{\omega L_{RX}}{R_{RX}};\quad Q_L=\frac{\omega L_{RX}}{R_{EQ}} \tag{8}$$

where $\omega$ is the angular frequency of the system excitation source $V_{TX}$, which is also the resonant frequency of the impedance matching network in the system

$$\omega=2\pi f=\frac{1}{\sqrt{L_{TX}C_{TX}}}=\frac{1}{\sqrt{L_{RX}C_{RX}}}. \tag{9}$$

Based on (7), $VCR_{SYS}$ will be affected by $k$ and $Q_L$. Fig. 6(a) shows the impact of $k$ on the system VCR under two normal load conditions: $R_L=200\ \Omega$ and $R_L=2\ k\Omega$. The value of $R_{EQ}$ can be calculated using (4) and (6). The $\eta_{RX}VCR_{RXideal}$ is idealized as 2 for DOVD and 1 for DOFBR. The inductive link in the model is defined as follows: $L_{TX}=1\ \mu H$, $Q_{TX}=140$, $L_{RX}=550$ nH, $Q_{RX}=80$, and $f=6.78$ MHz. In both $R_L=200\ \Omega$ and $R_L=2\ k\Omega$ cases, the DOVD exhibits obvious VCR enhancement in medium-to-strong coupling cases compared to the DOFBR, especially after the VCR-peak point. In weak coupling cases, both the DOVD and DOFBR demonstrate comparable system VCR. This occurs because the smaller $R_{EQ}$ of DOVD counteracts the benefit of its higher $VCR_{RXideal}$. To validate the modeled results, schematic-level simulations were conducted using Cadence Spectre, with identical inductive link conditions. In the simulation, the outputs of both the DOVD and DOFBR are unregulated, and since both topologies have separate power paths to their outputs, no additional controller is required. Fig. 6(b) displays the simulated results of the system VCR versus $k$ when $R_{O1}=R_{O2}=R_L=200\ \Omega$ or $R_{O1}=R_{O2}=R_L=2\ k\Omega$. Noticeably, the curves follow a similar trend to the modeled ones. Some minor differences appear at the VCR peak values and peak points, primarily due to the non-ideal $\eta_{RX}$ and model approximation errors.

The effect of $R_L$ on the system VCR is further examined, as illustrated in Fig. 6(c) and (d). The modeled and simulated results exhibit good consistency, with the proposed DOVD

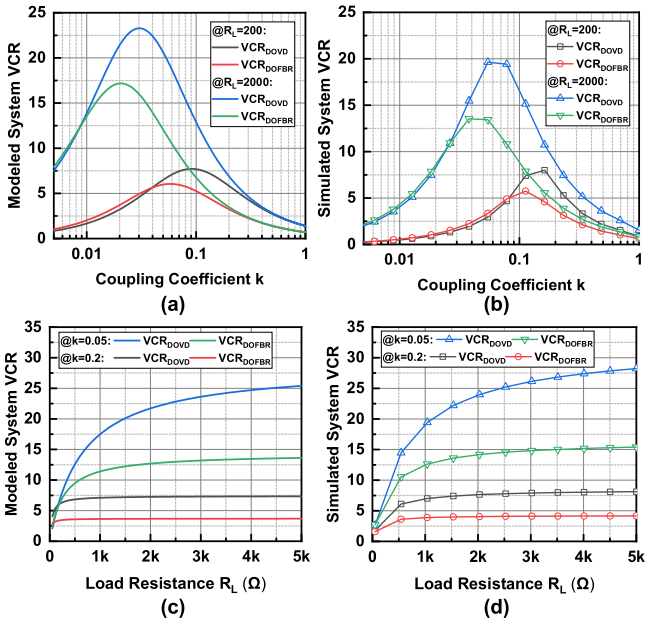



Fig. 6. System VCR analysis. (a) and (b) VCR versus $k$. (c) and (d) VCR versus $R_L$ ($R_{O1} = R_{O2} = R_L$).

showing explicit VCR enhancement compared to the DOFBR in most load scenarios. In cases of extremely heavy load, DOVD and DOFBR provide similar VCR values, which can be attributed to the smaller $R_{\mathrm{EQ}}$ of DOVD. In summary, compared to DOFBR, the proposed DOVD can achieve a higher system VCR under most conditions while maintaining it at a comparable level in other cases. Thus, the DOVD can help the WPT system adapt to varying coupling and loading conditions.

### B. Operational Principle

Given the natural division of the power stage into an upper path and a lower path, the proposed DOVD utilizes PPFM control with two independent hysteresis windows to regulate $V_{O1}$ and $V_{O2}$. A hysteresis window at a lower voltage level is applied to regulate $V_{O2}$. When $V_{O2}$ falls below the lower boundary of this hysteresis window, the DOVD charges $C_{O2}$ through the lower path. When $V_{O2}$ exceeds the upper boundary, the DOVD stops charging $C_{O2}$ by disabling the lower path. For regulating $V_{O1}$, a hysteresis window at a higher voltage level is employed. Since the upper path only charges $C_{O1}$ and $V_{O1}$ is the summed-up voltage across the two series-connected capacitors, $V_{O1}$ may surpass its upper boundary when the lower path charges $C_{O2}$. Hence, the effective hysteresis window of $V_{O1}$ can be slightly larger than that of $V_{O2}$. However, due to the higher $V_{O1}$ voltage, its larger hysteresis window does not translate into a larger percentage voltage ripple than $V_{O2}$, which will be validated in the measurement results.

To accommodate the dual-output regulation, a four-phase operation is employed by the proposed DOVD, as shown in Fig. 7 and explained below.

1) *Phase 1 ($\Phi_1$):* When both outputs require energy, the DOVD works in $\Phi_1$, the both-charging phase. In this phase, the DOVD works as a full-wave VD with $M_P$ and $M_N$ operating as active diodes. Thus, both $C_{O1}$ and $C_{O2}$ are charged in this phase.
2) *Phase 2 ($\Phi_2$):* When only $V_{O1}$ needs to level up, the DOVD switches to $\Phi_2$, the $C_{O1}$-charging phase. In this phase, $M_P$ functions as an active diode, while $M_N$ is disabled. Therefore, only $C_{O1}$ is charged through the DOVD.
3) *Phase 3 ($\Phi_3$):* When only $V_{O2}$ needs to level up, the DOVD switches to $\Phi_3$, the $C_{O2}$-charging phase. This phase follows an opposite pattern to phase 2, that is, $M_P$ is disabled and $M_N$ remains operational as an active diode. Hence, only $C_{O2}$ is charged through the DOVD.
4) *Phase 4 ($\Phi_4$):* When both outputs do not need to be charged, the DOVD enters $\Phi_4$, the freewheeling phase. In this phase, $S_{\mathrm{FW}}$ is turned on to short $L_{\mathrm{RX}}$, and both $M_P$ and $M_N$ are disabled. As a result, $C_{O1}$ and $C_{O2}$ are left being discharged by loads.

## III. System and Circuit Implementations

Fig. 8 illustrates the system diagram of the proposed DOVD, which is used as the RX circuit in a 6.78-MHz series-parallel resonant WPT system. The power stage comprises $M_P$, $M_N$, $C_{O1}$, and $C_{O2}$. In the upper power path, $M_P$ is controlled by $\mathrm{CMP}_P$, which compares $V_{\mathrm{ac}}$ with $V_{O1}$. To achieve zero-voltage switching (ZVS) in the power stage, a digital-tuning $\mathrm{ZVS}_P$ controller is implemented to compensate for the control loop delay from $\mathrm{CMP}_P$ to $M_P$. The gate driver $D_P$ can switch its operation between $V_{\mathrm{CMPP}}$ voltage buffer and $V_{\mathrm{MAX}}$ voltage follower, to accommodate the four-phase operation. The lower power path, including $M_N$, $D_N$, $\mathrm{CMP}_N$, and $\mathrm{ZVS}_N$ controller, is implemented in a similar way as the upper power path. The PPFM controller regulates the dual outputs by managing the four-phase operation. A local CLK signal, $\mathrm{CLK}_{\mathrm{RX}}$, is recovered from $V_{\mathrm{ac}}$ to synchronize the control signals with the power flow, achieving seamless phase transition.

### A. Parallel PFM Controller

Fig. 9 shows the circuit diagram of the PPFM controller. It consists of three parts: the $V_{O1}$ detector, the $V_{O2}$ detector, and the output stage including logic buffers and level shifters. In the $V_{O1}$ detector, $V_{O1}$ is compared with the upper threshold voltage $V_{\mathrm{REFH1}}$ by a latched comparator. The comparison event is synchronized by $\mathrm{CLK}_{\mathrm{RX}}$ with the moment that $V_{\mathrm{ac}}$ is approximately equal to $V_{O2}$. This ensures that no conduction path exists when the DOVD detects the voltage level of $V_{O1}$ and anticipates potential changes in its operational phase. In contrast, $V_{O1}$ is compared with the lower threshold voltage $V_{\mathrm{REFL1}}$ by a continuous-time comparator, considering that DOVD might be in the freewheeling phase ($\Phi_4$) without a valid $\mathrm{CLK}_{\mathrm{RX}}$ edge. Following the comparison stages, changes in $V_{H1}$ and $V_{L1}$ are detected by the rising edge detector and the falling edge detector, respectively. The voltage level of $V_{O1}$ is then identified by an SR latch, whose output will be buffered, level-shifted, and finally provided to the upper power path as the control signal $V_{\mathrm{CTP}}$, for the regulation of $V_{O1}$. The $V_{O2}$ detector operates similar to the $V_{O1}$ detector, which directly controls the lower power path by $V_{\mathrm{CTN}}$ for the regulation of $V_{O2}$. The gate control signal for $S_{\mathrm{FW}}$, $V_{\mathrm{CTFW}}$ is generated by a NAND gate that takes inputs from both output detectors, turning $S_{\mathrm{FW}}$ ON when both upper and lower power paths are

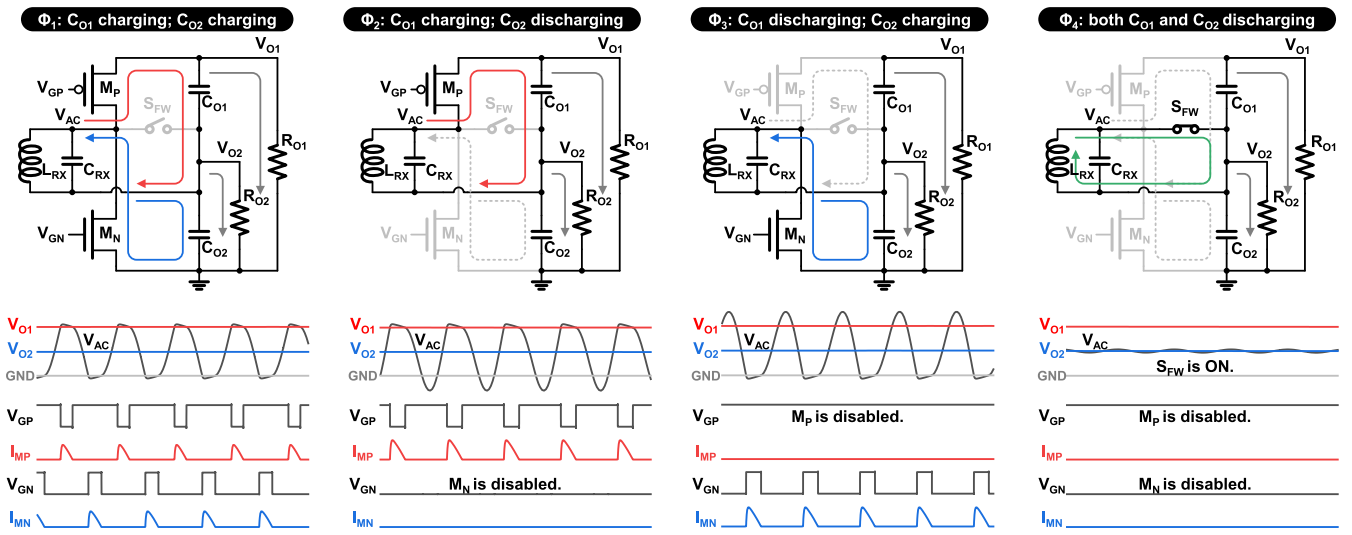



Fig. 7. Operational principle of the proposed DOVD: four-phase operation.

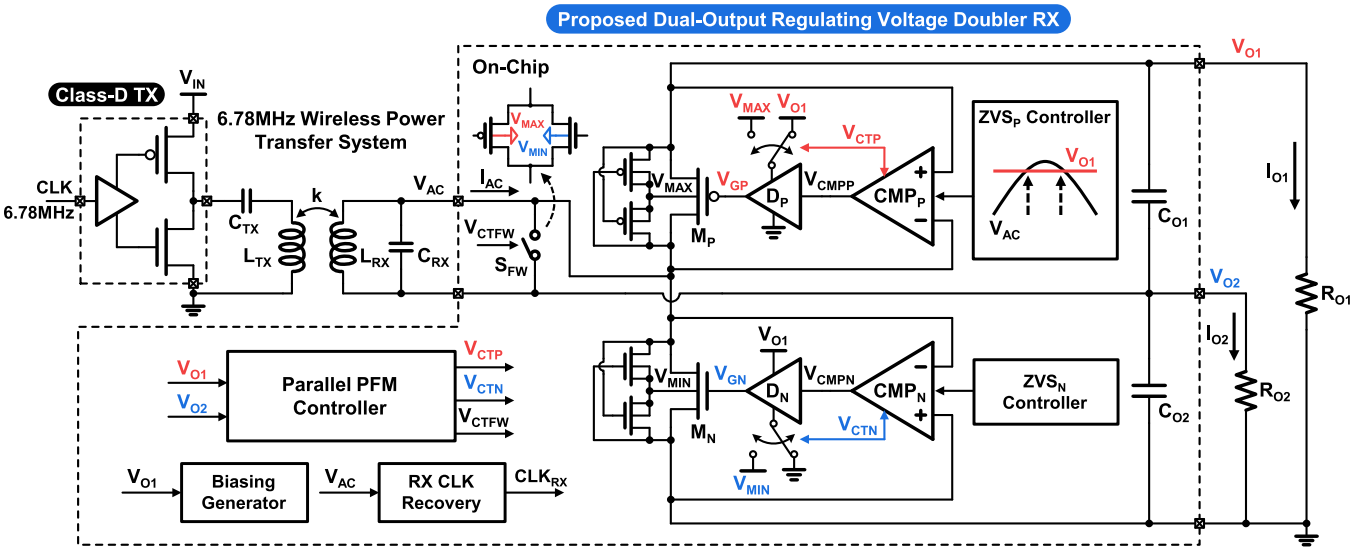



Fig. 8. System diagram of the proposed DOVD.

idle. Fig. 10(a) shows the simulated operational waveforms of the PPFM controller during $I_{O2}$ load transient, and Fig. 10(b) shows zoomed-in steady-state waveforms.

### B. Digital-Tuning Adaptive Delay Compensation

The control loop delay from $\text{CMP}_P$ (or $\text{CMP}_N$) to $M_P$ (or $M_N$) can result in significant turn-on and turn-off errors of $M_P$ (or $M_N$). To address this issue, delay compensation techniques should be applied. Furthermore, since the DOVD distributes power between the upper and lower paths by the four-phase operation, the turn-on/off errors of $M_P$ and $M_N$ can vary across different phases. As a result, the delay compensation block should be fast enough to deal with such variations.

In [6], [7], [10], and [22], fixed delay compensation is introduced by adding switched biasing branches into a push-pull comparator. This features simple implementation and reliable operation; however, it is subject to fluctuating input/load conditions and process, voltage, and temperature (PVT) variations. In [35] and [36], adaptive delay compensation is implemented by establishing switched voltage-controllable biasing branches in a push-pull comparator; in [37] and [38], this is done by adding tunable voltage offsets to the inputs of a comparator. Although these methods can effectively compensate for dynamic delay variations, they are based on analog feedback loops, which are typically rather slow.

In this work, a digital adaptive delay compensation technique is proposed, which provides fast responses to both turn-on and turn-off delay variations. The circuit implementation of the $\text{CMP}_P$ and $\text{ZVS}_P$ controller is shown in Fig. 11. The $\text{CMP}_P$ has a common-gate structure in which $M_1$ and $M_2$ form the input pair. Two resistor banks (RBs) are added in front of the inputs to provide turn-on/off delay compensation by giving voltage offsets. Each RB consists of eight identical unit resistors and eight bypass switches. Before $V_{\text{ac}}$ rises to

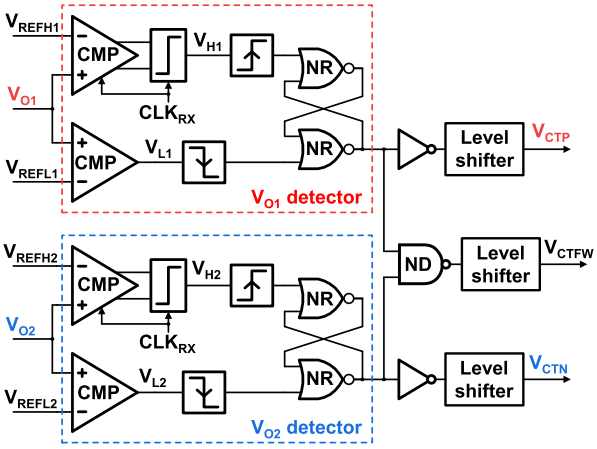



Fig. 9. Circuit implementation of the PPFM controller.

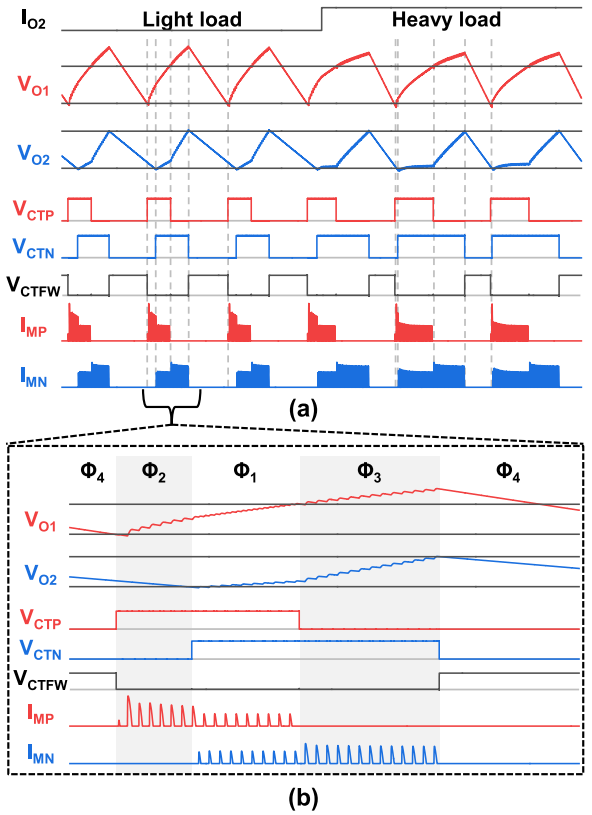



Fig. 10. Simulated waveforms of the PPFM controller. (a) Waveforms during $I_{O2}$ load transient. (b) Zoomed steady-state waveforms.

approach $V_{O1}$, $V_{\rm GP}$ is high. The $\rm ZVS_{OFF}$ RB is short-circuited by $M_{\rm RB2}$, and the $\rm ZVS_{ON}$ RB is involved into the $V_{O1}$ input path. Hence, the $\rm ZVS_{ON}$ RB provides an offset voltage on $V_{O1}$ to achieve ZVS turn-on of $M_P$. A similar ZVS turn-off operation applies to the case when $V_{\rm ac}$ is about to fall below $V_{O1}$. The $V_{\rm CMPP}$ locker is implemented to avoid multiple pulsing problems.

To tune the voltage offsets, the $\rm ZVS_P$ controller adjusts the number of engaged unit resistors in the RBs. In the $\rm ZVS_P$ turn-off controller, the polarity of the voltage error between $V_{\rm ac}$ and $V_{O1}$ is detected by a latched comparator (latched CMP). The detection moment is synchronized with the rising edge of $V_{\rm GP}$, corresponding to the turn-off moment of $M_P$. Since the latched comparator is designed to have a short response time of less than 300 ps, the conventional sample-and-hold circuits storing the information of $V_{\rm ac}$ and $V_{O1}$ can be removed. The output of the latched comparator determines the shift direction of an 8-bit bidirectional shift register (Bi. SR), which subsequently controls the number of engaged unit resistors in the $\rm ZVS_{OFF}$ RB. By running this feedback loop, a proper voltage offset can be eventually given for the ZVS turn-off of $M_P$. The $\rm ZVS_P$ turn-on controller is implemented similarly.

Fig. 12 shows the operational waveforms of the $\rm CMP_P$ and $\rm ZVS_P$ controller. When phase switching happens, the delay compensation applied in $\rm CMP_P$ can recalibrate in a few periods thanks to the proposed digital-tuning adaptive delay compensation technique. In the steady state, $M_P$ can operate with near-optimal ZVS turn-on and turn-off, which will be further validated in the measurement results.

### C. Adaptive-Biasing-Based $V_{ac}$-Swing Isolation

In the operational phase $\Phi_2$ or $\Phi_3$, the $L_{\rm RX}$–$C_{\rm RX}$ tank can freewheel for half a period as the DOVD disengages one side of the power stage, resulting in resonance energy accumulation. Consequently, $V_{\rm ac}$ can drop below GND in $\Phi_2$ or exceed $V_{O1}$ in $\Phi_3$. If, in $\Phi_2$, the DOVD disables $M_N$ by simply tying $V_{\rm GN}$ to GND, unintentional turn-on of $M_N$ may happen once $V_{\rm ac}$ falls below $-V_{\rm THN}$. A similar situation can occur at $M_P$ when the DOVD operates in $\Phi_3$. Thus, it is crucial to appropriately bias $M_P$ and $M_N$ during these phases to ensure reliable regulation of both outputs.

Fig. 13 shows the circuit diagrams of the adaptive-biasing gate drivers. When $V_{\rm CTP}$ is high, meaning the upper power path should be activated, the gate driver $D_P$ operates as a four-stage inverter-based voltage buffer supplied by $V_{O1}$; the output $V_{\rm GP}$ is the buffered version of $V_{\rm CMPP}$. When $V_{\rm CTP}$ becomes low, the last stage in $D_P$ is disconnected from the prior three stages, and both PMOS and NMOS in the last stage are turned off. Subsequently, $D_P$ switches its operation to a voltage follower by connecting $V_{\rm GP}$ to $V_{\rm MAX}$. This ensures that $V_{\rm GP}$ follows $V_{\rm MAX}$ when the upper power path should be disabled, consolidating a robust open-circuit $M_P$ when $V_{\rm ac}$ can exceed $V_{O1}$. The gate driver $D_N$ is implemented similarly.

The $V_{\rm ac}$-swing isolation concern extends to $\rm CMP_P$, $\rm CMP_N$, and the driving block of $S_{\rm FW}$ as they all interface $V_{\rm ac}$ through non-isolated transistor terminals. In $\rm CMP_P$ (see Fig. 11), for instance, the gate terminals of the input pair, $M_1$ and $M_2$, can be biased to $V_{\rm MAX}$ through $M_{\rm AB}$ when the upper power path should be disabled. This prevents potential false switching at $V_{\rm CMPP}$, reducing unnecessary power loss and improving system reliability. Similar design principles are applied in implementing $V_{\rm ac}$-swing isolation in other blocks.

## IV. Measurement Results

The proposed DOVD was fabricated in a 180-nm Bipolar-CMOS-DMOS (BCD) process, occupying a silicon area of 0.34 $\rm mm^2$ excluding pads, as shown in Fig. 14. 5-V devices are used in the power stage to achieve high-voltage power delivery, and 1.8-V devices are used in the control circuitry. $C_{O1}$ and $C_{O2}$ were implemented on-chip and each has the capacitance of 100 pF. The integrated on-chip output capacitors are ideal for light-load operations; additional off-chip capacitors can be added for heavy loads.

Fig. 15 shows the measurement setup. A waveform generator (Keysight 33600A) imitates the class-D power amplifier at

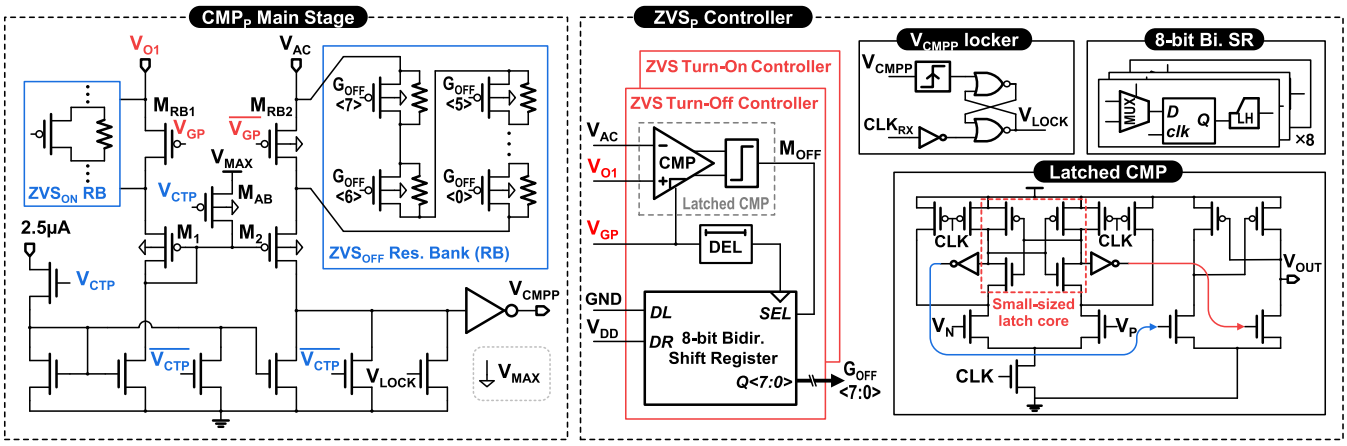



Fig. 11. Circuit implementation of CMP$_P$ with digital-tuning adaptive delay compensation (ZVS$_P$ controller).

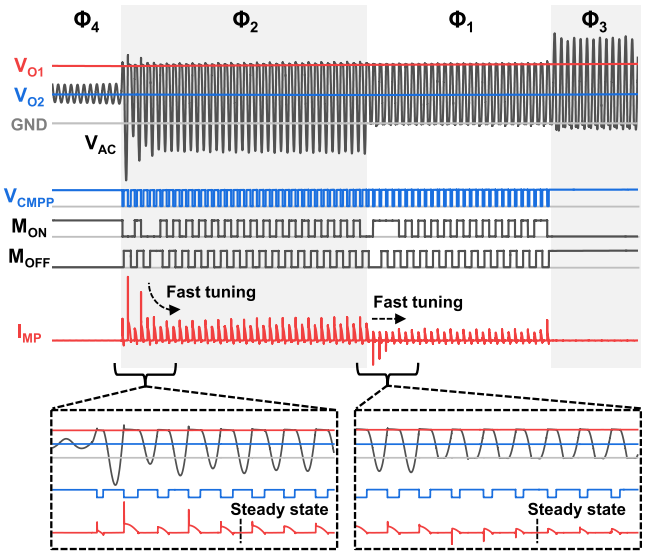



Fig. 12. Simulated waveforms of CMP$_P$ with digital-tuning adaptive delay compensation.

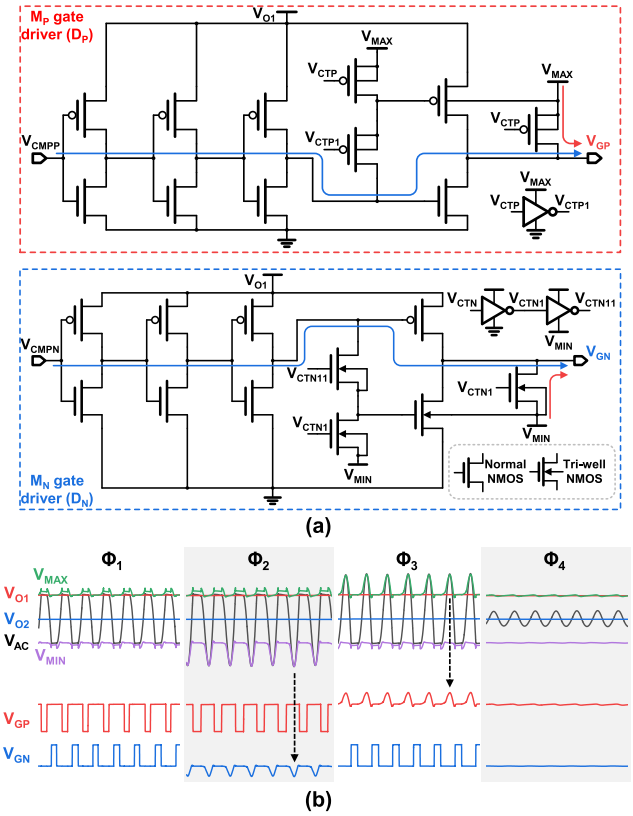



Fig. 13. Adaptive-biasing gate drivers. (a) Circuit implementation. (b) Simulated waveforms.

the TX side and generates a 6.78-MHz square wave. A series-parallel resonant inductive link is used as the wireless power link. The inductance of TX and RX coils are 951 and 540 nH, respectively, and the distance between TX and RX coils was fixed at 7 mm. Two 4.5-$\mu$F output capacitors were added to $C_{O1}$ and $C_{O2}$, respectively, as extra buffers in the tested PCB.

Fig. 16 shows the measured steady-state waveforms of the proposed DOVD, with $I_{O1} = 1.65$ mA ($R_{O1} = 2$ k$\Omega$) and $I_{O2} = 1.8$ mA ($R_{O2} = 1$ k$\Omega$) as the demonstrated load conditions. $V_{O1}$ and $V_{O2}$ are regulated at 3.3 and 1.8 V with voltage ripples of 125 and 75 mV, respectively. The percentage voltage ripples of $V_{O1}$ and $V_{O2}$ are 3.72% and 4.1%, respectively. The control signals $V_{\mathrm{CTP}}$ and $V_{\mathrm{CTN}}$ validate the four-phase operation managed by the proposed PPFM controller. Fig. 17 displays the measured steady-state waveforms with the ac input voltage $V_{\mathrm{ac}}$. Different operational phases can be explicitly distinguished by observing the amplitude of $V_{\mathrm{ac}}$. In $\Phi_2$ and $\Phi_3$, it is noticeable that $V_{\mathrm{ac}}$ can fall below GND and surpass $V_{O1}$, respectively, because of the freewheeling $L_{\mathrm{RX}}$–$C_{\mathrm{RX}}$ tank. In $\Phi_4$, the amplitude of $V_{\mathrm{ac}}$ significantly decreases since $L_{\mathrm{RX}}$ is short-circuited. The zoomed-in steady-state waveforms of the four operational phases are shown in Fig. 18. The ac input current $I_{\mathrm{ac}}$ was measured by using a 2-GHz bandwidth differential probe monitoring the voltage across a 7.5-$\Omega$ current sensing resistor, which is inserted in the input path close to $V_{O2}$. It can be observed that the proposed digital-tuning adaptive delay compensation helps the DOVD realize near-optimal turn-on and turn-off ZVS of both $M_P$ and $M_N$ in all charging phases.

Fig. 19 shows the measured waveforms of the proposed DOVD during the load transient at $V_{O1}$. Thanks to the fast

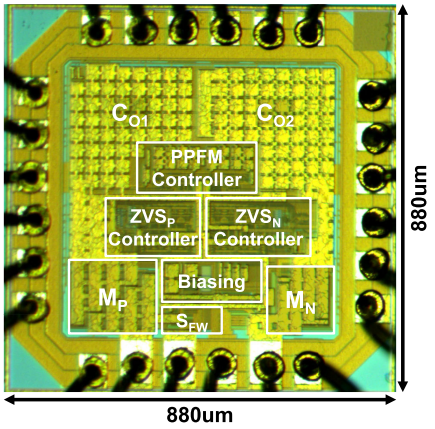
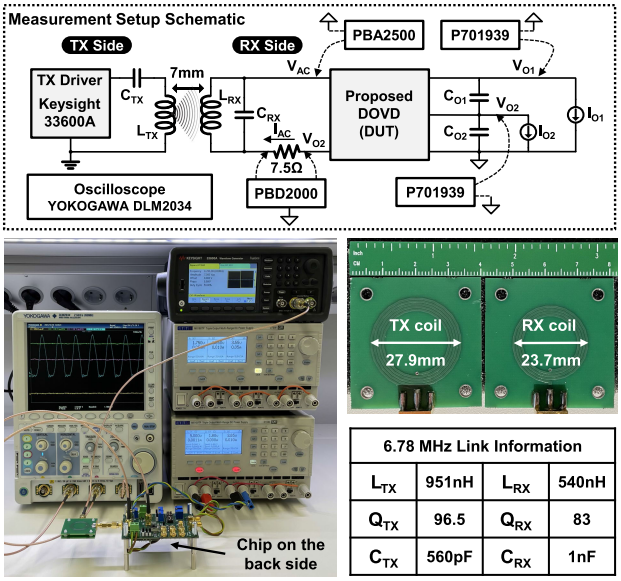



Fig. 14. Die micrograph of the proposed DOVD.




| 6.78 MHz Link Information | | | |
|---|---|---|---|
| $L_{TX}$ | 951nH | $L_{RX}$ | 540nH |
| $Q_{TX}$ | 96.5 | $Q_{RX}$ | 83 |
| $C_{TX}$ | 560pF | $C_{RX}$ | 1nF |

Fig. 15. Measurement setup with link information.

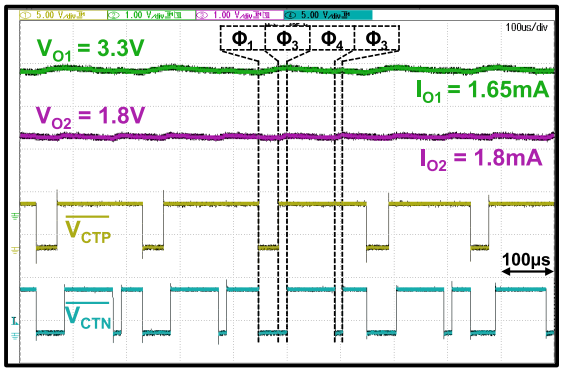



Fig. 16. Steady-state waveforms showing PPFM output regulation.

hysteresis-based PFM controller, the undershoot or overshoot voltage on $V_{O1}$ keeps unnoticeable when $I_{O1}$ changes between 0.66 mA ($R_{O1}$ = 5 kΩ) and 16.5 mA ($R_{O1}$ = 200 Ω) while $I_{O2}$ is fixed at 1.8 mA ($R_{O2}$ = 1 kΩ). Moreover, since the proposed DOVD adopts the PPFM control strategy, no cross-

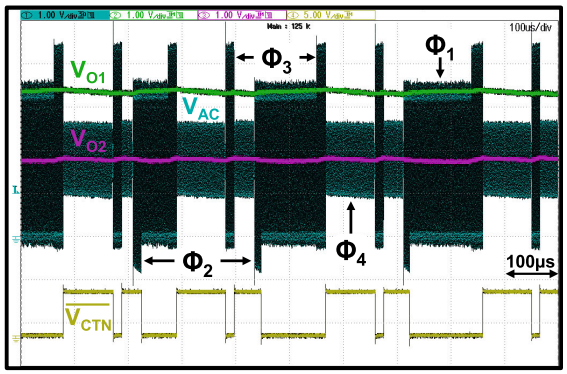



Fig. 17. Steady-state waveforms with $V_{ac}$ signals.

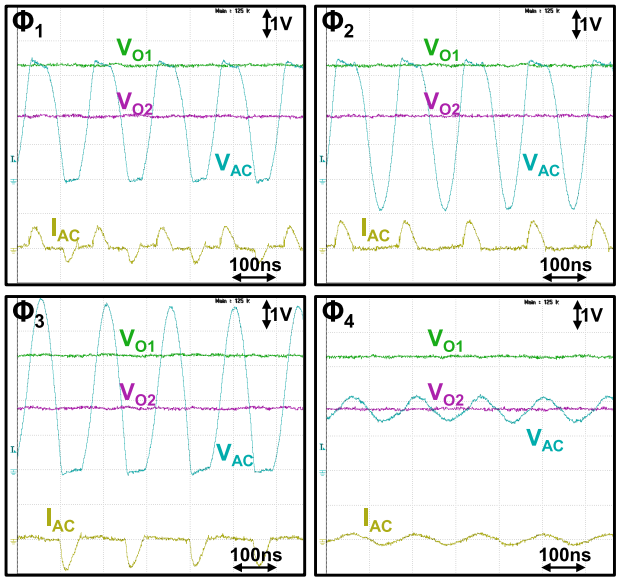



Fig. 18. Zoomed steady-state waveforms in four phases.

regulation is observed at $V_{O2}$ during $I_{O1}$ load transient, endorsing a reliable dual-output regulation. Similarly, Fig. 20 shows the measured waveforms during the load transient at $V_{O2}$. When $I_{O2}$ changes between 0.36 mA ($R_{O2}$ = 5 kΩ) and 9 mA ($R_{O2}$ = 200 Ω) while keeping $I_{O1}$ constant at 3.3 mA ($R_{O1}$ = 1 kΩ), neither undershoot/overshoot voltage on $V_{O2}$ nor cross regulation at $V_{O1}$ is observed.

Fig. 21 shows the measured PCE of the proposed DOVD at different load conditions. The PCE is defined as

$$\text{PCE} = \text{Average}\frac{\frac{V_{O1}^2}{R_{O1}} + \frac{V_{O2}^2}{R_{O2}}}{(V_{\text{ac}} - V_{O2}) \times I_{\text{ac}}} \times 100\%. \qquad (10)$$

Considering the oscilloscope has a certain sample rate, averaged instantaneous power is used to calculate PCE. Observed from the PCE 3-D color map, as shown in Fig. 21(a), the DOVD can sustain a high PCE >85% over a wide load range. When both outputs are in very light-load conditions (<5 mA), the PCE decreases because the freewheeling conduction loss from $\Phi_4$ becomes dominating. The peak PCE of 92.95% is obtained when both outputs are in heavy-load conditions ($I_{O1}$ = 15 mA and $I_{O2}$ = 20 mA) and the DOVD is mostly in the charging phases. With varying $I_{O1}$ under several certain $I_{O2}$ conditions [see Fig. 21(b)], the DOVD can sustain a

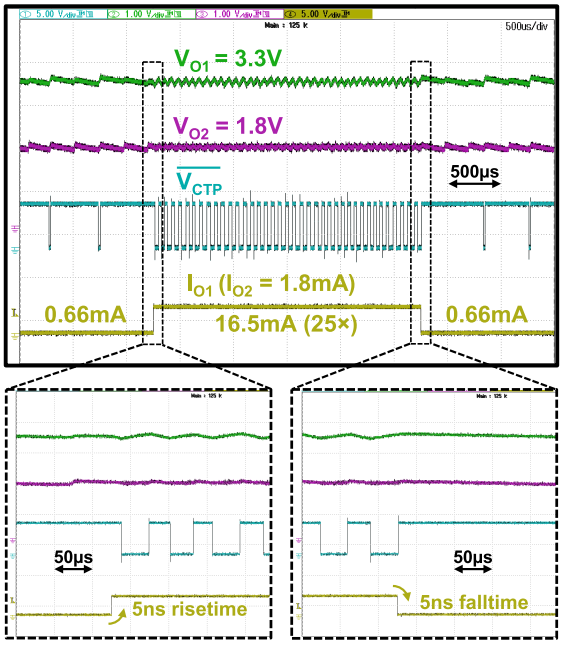



Fig. 19. Load-transient waveforms at $I_{O1}$ with $I_{O2} = 1.8$ mA.

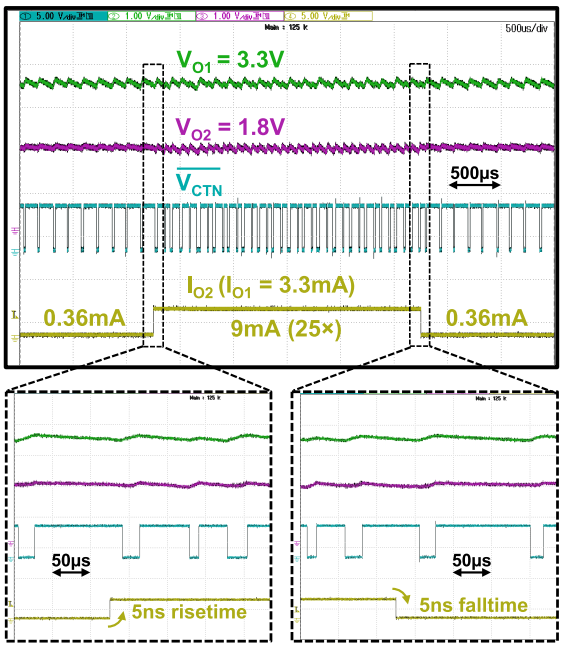



Fig. 20. Load-transient waveforms at $I_{O2}$ with $I_{O1} = 3.3$ mA.

$I_{O1}$ range from 0 to 25 mA. Remarkable PCE (>90%) is achieved in a wide $I_{O1}$ range. With varying $I_{O2}$ under several certain $I_{O1}$ conditions [see Fig. 21(c)], the DOVD can sustain a $I_{O2}$ range from 0 to 30 mA. Compared to $I_{O2}$, it can be observed that the PCE exhibits a stronger relation with $I_{O1}$. The measured load ranges of both $I_{O1}$ and $I_{O2}$ cover most of the possible load conditions of biomedical implantable devices.

Fig. 22 depicts the measured VCR at $V_{O1}$ at different load conditions. The VCR is defined as

$$\text{VCR} = \frac{2V_{O1}}{(V_{\text{ac}} - V_{O2})_{\text{PP}}} \tag{11}$$

which is measured during $\Phi_1$. A VCR higher than 1.72 is achieved over the entire load range, as shown in Fig. 22(a). The peak VCR of 1.875 is obtained when $I_{O1} = 1.65$ mA and $I_{O2} = 5$ mA. With varying $I_{O1}$ under several certain $I_{O2}$ conditions [see Fig. 22(b)], the DOVD shows a clear negative correlation with $I_{O1}$. With varying $I_{O2}$ under several certain $I_{O1}$ conditions [see Fig. 22(c)], the DOVD displays gentler changes in VCR versus $I_{O2}$ since $I_{O2}$ is not directly loading $V_{O1}$.

Fig. 23 shows the simulated power breakdown under the measured maximum output power condition, which reaches 90.5 mW with $I_{O1} = 22.5$ mA and $I_{O2} = 9$ mA. At the moment, about 6.2% of input power is consumed by the DOVD system, in which most is from the conduction losses and switching losses of $M_P$ and $M_N$, $P_{\text{CDP/N}}$ and $P_{\text{SWP/N}}$. $P_{\text{FW}}$ represents the freewheeling loss.

Table I compares the proposed DOVD with recently reported single-stage dual-output/high-VCR RX designs. The DOVD uses only two power transistors, which is the minimized utilization among state-of-the-art. Moreover, it achieves a VCR as high as 1.875, roughly two times higher than that of FBRs. Thanks to the proposed PPFM control strategy, instant load-transient response and unnoticeable cross-regulation can be achieved. The proposed digital-tuning adaptive delay compensation further facilitates near-optimal turn-on/off ZVS of the DOVD and provides fast error-variation responses. Benefiting from both the topology and considerate control circuitry, the proposed DOVD achieves the highest power efficiency.

## V. Discussion

### A. End-to-End Efficiency (TX to Load)

Regulating rectifiers are a recently hot topic in the field of WPT integrated circuits. This is motivated by the fact that these WPT systems, mostly for biomedical implants or portable electronic devices, have stringent requirements for both size and cost. However, the advantages of regulating rectifiers come with trade-offs. Such rectifiers give up the merit of doing impedance transformation, which is crucial for achieving optimal end-to-end (E2E) efficiency point tracking (OEPT) at the system level [39]. A cascaded dc–dc converter, however, has the advantage of reflecting optimal impedance reliably to TX, thus achieving OEPT. This trade-off can be a fair concern when designing a WPT system and should be optimized based on the essentialities of target specifications. Without impedance transformation, the E2E efficiency would degrade when the RX output voltages deviate from their optimal values. Though the RX can probably maintain a decent PCE at the moment, increased power losses are likely to occur at the TX side and within the inductive link.

The above analyses apply to the proposed DOVD. Since the optimal voltages of the two outputs are determined by the topology, the users of the DOVD can specify the output conditions freely and independently but at a potential cost of E2E efficiency. To prolong the lifetime of the WPT system and minimize local heating, addressing regulating rectifiers with the capability of OEPT stands as a promising avenue for future research.

### B. Output Dependency in the DOVD

Since the DOVD incorporates two capacitors stacked at the output side, it is worthwhile to discuss the dependence

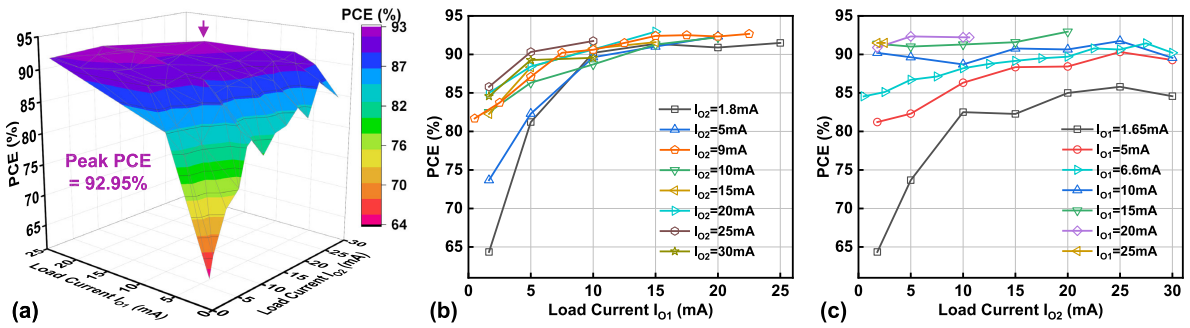



Fig. 21. Measured PCE versus load currents. (a) 3-D colormap of PCE. (b) PCE versus $I_{O1}$. (c) PCE versus $I_{O2}$.

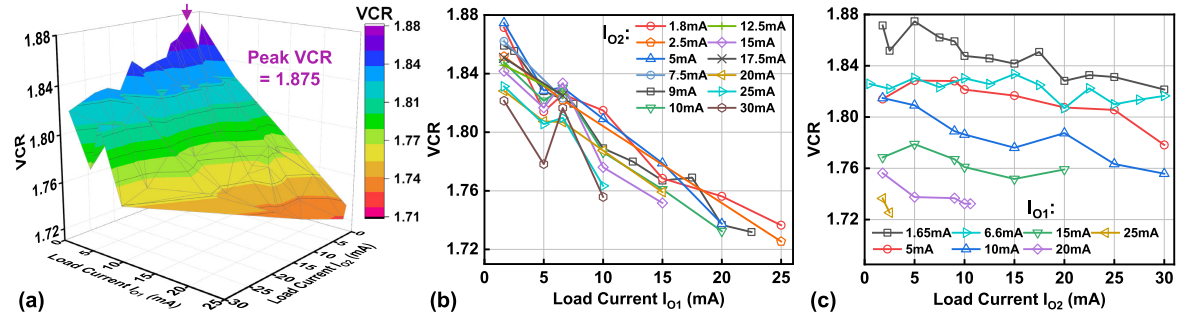



Fig. 22. Measured VCR at $V_{O1}$ versus load currents. (a) 3-D colormap of VCR. (b) VCR versus $I_{O1}$. (c) VCR versus $I_{O2}$.

TABLE I
COMPARISONS WITH STATE-OF-THE-ART DESIGNS

| | JSSC'19 [28] | TBCAS'20 [21] | JSSC'21 [17] | ISSCC'23 [23] | JSSC'23 [16] | TCAS-I'23 [29] | **This work** |
|---|---|---|---|---|---|---|---|
| **Technology** | 350 nm CMOS | 180 nm CMOS | 180 nm CMOS | 65 nm CMOS | 180 nm CMOS | 180 nm CMOS | **180 nm BCD** |
| **Chip Area** | 2.4 $mm^2$ | 6 $mm^2$ | 0.6 $mm^2$ | 0.74 $mm^2$ | 2.32 $mm^2$ | 2.7 $mm^2$ | **0.34 $mm^2$** |
| **Operation Frequency** | 1 MHz | 2 MHz | 6.78 MHz | 40.68 MHz | 6.78 MHz | 6.78 MHz | **6.78 MHz** |
| **LC Topology** | Parallel | - | Series | Parallel | Parallel | Series | **Parallel** |
| **Receiver Topology** | VM/CM Rectifier | VM Full-Bridge Rectifier | VM Full-Bridge Rectifier | VM Full-Bridge Rectifier | VM Full-Bridge Rectifier | RCM Rectifier | **VM Voltage Doubler** |
| **No. of Power Transistors** | 3 | 6 | 4 | 5 | 6 | 5 | **2** |
| **$V_{OUT}$ (No. of $V_{OUT}$)** | 3V (1) | 1.5V, 2.5V (2) | 1.8V, 3.3V (2) | 1.1V, 2.2V (2) | 3.7V, 5V (2) | 1.8V, 3V (2) | **1.8V, 3.3V (2)** |
| **Output Regulation** | Reverse Conduction | PFM + PWM | PFM | PFM | PFM | PFM | **Parallel PFM** |
| **Adaptive Delay Compensation** | No | Analog-Based Turn-On/Off ZVS | No | Analog-Based Turn-On ZVS | Digital-Tuning Turn-On/Off ZVS | Digital-Controlled Delay Line | **Digital-Tuning Turn-On/Off ZVS** |
| **Load-Transient Response** | - | - | Instant | Instant | Instant | 2 ms# | **Instant** |
| **Cross Regulation** | - | - | Unnoticeable | Unnoticeable | - | 100 mV/mA# | **Unnoticeable** |
| **Peak VCR** | 1.4 | 0.83* | 0.92* | 0.91* | 0.85* | 1.5 | **1.875** |
| **$P_{OUT}$** | 0.18mW – 18mW | 7.3mW - 65mW | 102mW - 1.02W | 6mW – 60.5mW | 0.5mW – 180mW | 1mW – 7mW | **2.6mW - 90.5mW** |
| **Peak PCE** | 75% | 90.75% | 91.9% | 90.1% | 91.8% | 85.1% | **92.95%** |

*Estimated from plotted data. #Related to the transmitter-side power regulation in [29].

between the two outputs. From the ripple aspect, the ripple of $V_{O2}$ can be added to $V_{O1}$ under certain load conditions, resulting in increased ripples at $V_{O1}$ (see Fig. 10). This may not be problematic if $V_{O1}$ serves as a supply for high-voltage stimulators or digital I/O's; however, load circuits that are sensitive to the power supply rejection ratio (PSRR) may show

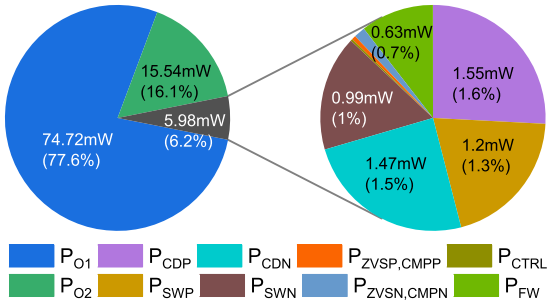



Fig. 23. Simulated power breakdown under the measured maximum output power condition ($I_{O1} = 22.5$ mA, $I_{O2} = 9$ mA).

degraded performances. This ripple dependency is derived from the implemented PFM control, which exhibits a limited output pull-down ability. To further mitigate this effect, the proposed PFM control can be improved with linear current sink stages [19] or refined by linear control techniques showing tighter regulations, such as pulsewidth modulation (PWM) [20]. Hence, this circuit-level concern can be circumvented by incorporating proper techniques and refinements.

Another aspect is the load dependency (or cross-regulation). In prior structures [see Fig. 3(a)–(c)], the cross-regulation is an unavoidable issue because they use multiplex power paths connected to their outputs; when one output has heavy loads, the other output can suffer from the lack of power input. This problem was avoided in [17]. The proposed DOVD avoids this issue by naturally separating power paths, which ensure that the input power is always accessible to both outputs simultaneously. However, the situation becomes more complex in the DOVD since $V_{O1}$ and $V_{O2}$ have a shared energy element $C_{O2}$, while a part of the loading at $V_{O2}$ comes from $R_{O1}$. It is worth noting that the complex loading conditions do not translate to a fragile system or a complicated design. By fully utilizing the separated power paths with the proposed parallel control strategy, the cross regulation is not observed from the load transient and PCE measurement results.

## VI. Conclusion

This article presents a single-stage DOVD for wirelessly powering biomedical implantable devices. The DOVD topology achieves up-to-1.875-VCR ac-to-dc rectification and dual-output voltage regulation using only two power transistors. Thanks to the PPFM output regulation, instant load-transient response and unnoticeable cross-regulation can be realized. With the help of digital-tuning adaptive delay compensation, near-optimal turn-on/off ZVS of power transistors is adopted with fast error-variation responses. The overall DOVD system achieves a wide output power range of 2.6–90.5 mW and a high power efficiency of 92.95%.

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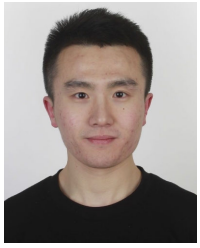

**Tianqi Lu** (Graduate Student Member, IEEE) received the B.Sc. degree in physics from Nanchang University, Nanchang, China, in 2018, and the M.Sc. degree in integrated circuit engineering from Tsinghua University, Beijing, China, in 2021. He is currently pursuing the Ph.D. degree with the Department of Microelectronics, Delft University of Technology, Delft, The Netherlands.

His research interests include power management integrated circuits for wireless power transfer and dc–dc power converters.

**Kofi A. A. Makinwa** (Fellow, IEEE) received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Ife, Nigeria, in 1985 and 1988, respectively, the M.E.E. degree from the Philips International Institute, Eindhoven, The Netherlands, in 1989, and the Ph.D. degree from Delft University of Technology, Delft, The Netherlands, in 2004.

From 1989 to 1999, he was a Research Scientist with Philips Research Laboratories, Eindhoven. Since 1999, he has been with Delft University of Technology, where he is currently an Antoni van Leeuwenhoek Professor and the Head of the Microelectronics Department. His research interests include the design of mixed-signal circuits, sensor interfaces, and smart sensors. This has led to 20+ books, 350+ technical articles, and 30+ patents.

Dr. Makinwa is a member of the Royal Netherlands Academy of Arts and Sciences. He is currently a member of the Executive Committee of the VLSI Symposium and a Co-Organizer of the Advances in Analog Circuit Design (AACD) Workshop and the IEEE Sensor Interfaces Meeting (SIM). He was a co-recipient of 18 best paper awards, from the JSSC, International Solid-State Circuits Conference (ISSCC), and VLSI Symposium, among others. At the 70th anniversary of ISSCC, he was recognized as its top contributor. He was the Analog Subcom Chair for ISSCC and has served on the program committees of several other IEEE conferences. He has also been a Distinguished Lecturer of the Solid-State Circuits Society and an Elected Member of its Adcom.

**Sijun Du** (Senior Member, IEEE) received the B.Eng. degree (Hons.) in electrical engineering from University Pierre and Marie Curie (UPMC), Paris, France, in 2011, the M.Sc. degree (Hons.) in electrical and electronic engineering from Imperial College London, London, U.K., in 2012, and the Ph.D. degree in electrical engineering from the University of Cambridge, Cambridge, U.K., in January 2018.

He was with the Laboratoire d'Informatique de Paris 6 (LIP6), UPMC, and then was an IC Engineer in Shanghai, China, from 2012 to 2014. He was a Summer Engineer Intern at Qualcomm Technology Inc., San Diego, CA, USA, in 2016. He was a Visiting Scholar at the Department of Microelectronics, Fudan University, Shanghai, in 2018. He was a Post-Doctoral Researcher at Berkeley Wireless Research Center (BWRC), Department of Electrical Engineering and Computer Sciences (EECS), University of California at Berkeley, Berkeley, CA, USA, from 2018 to 2020. In 2020, he joined the Department of Microelectronics, Delft University of Technology (TU Delft), Delft, The Netherlands, where he is currently an Assistant Professor. His current research is focused on energy-efficient integrated circuits and systems, including power management integrated circuits (PMIC), energy harvesting, wireless power transfer, and dc/dc converters used in the Internet-of-Things (IoT) wireless sensors, wearable electronics, biomedical devices, and microrobots.

Dr. Du is a Technical Committee Member of the IEEE Power Electronics Society (PELS) and IEEE Circuits and Systems Society (CASS). He received the Dutch Research Council (NWO) Talent Program-VENI Grant in the 2021 round. He was a co-recipient of the Best Student Paper Award in IEEE International Conference on Electronics Circuits and Systems (ICECS) 2022. He served as a Sub-Committee Chair for IEEE ICECS 2022 and a Review Committee Member for IEEE International Symposium on Circuits and Systems (ISCAS) from 2021 to 2023, and has been serving as an IEEE International Solid-State Circuits Conference (ISSCC), Student Research Preview (SRP) Committee Member since 2023.