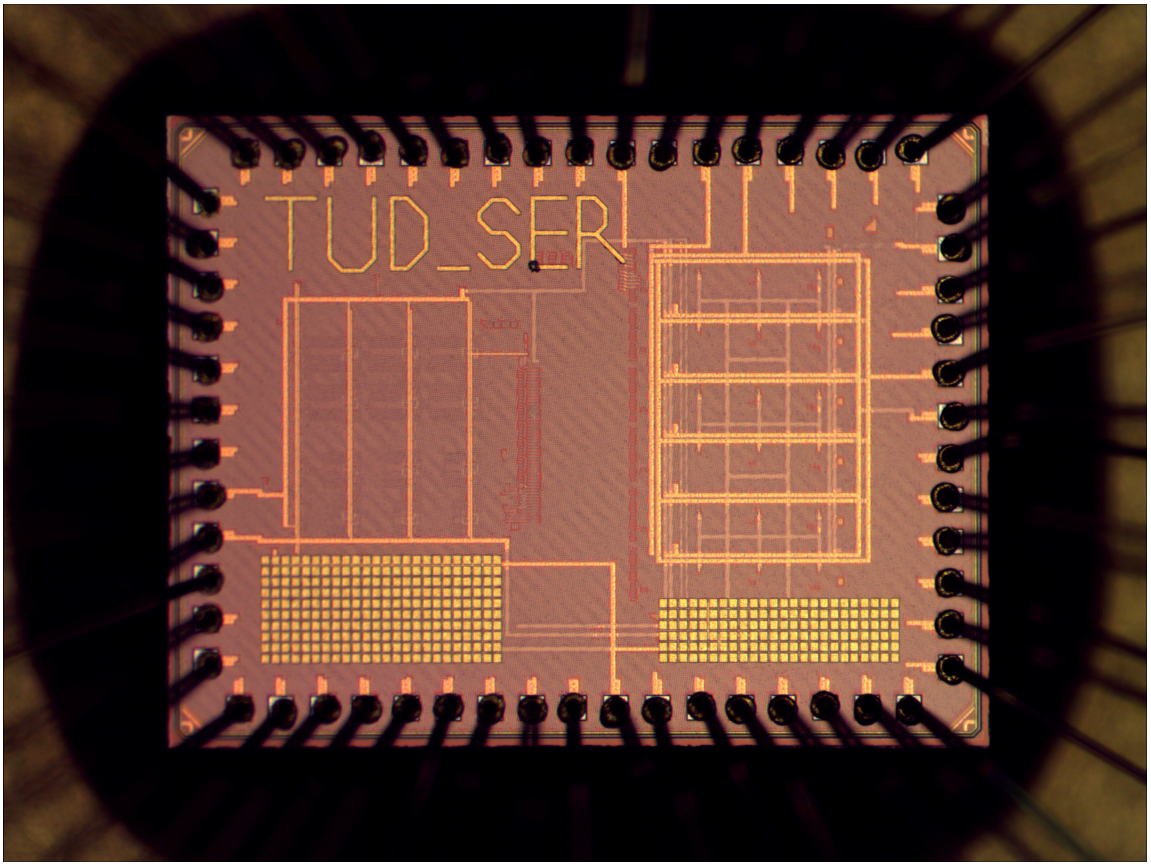
High-Speed Readout Circuit for PIN Single Electron Detector in Voltage Mode

by

Lars Bouman



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Abstract

This thesis proposes the design of a new type of read-out circuit for a PIN diode used in Scanning Electron Microscope (SEM) applications. The circuit operates in voltage mode (with high input impedance), which offers significant power-saving advantages over the traditionally used current mode (with low input impedance). The final read-out circuit can detect the incoming charge of $\sim 1000e^-$ with a temporal resolution of 2.5 ns at a frequency of 400 MHz. Post-layout simulation results indicate a promising reduction in power consumption to 188 µW per pixel.

At the core of the read-out circuit is a dynamic comparator. The dynamic comparator is designed to operate with low noise at high frequencies while still having a low power consumption. The final comparator has a delay of 240 ps and 140 µV of input-referred noise while consuming 71 fJ/conversion. The comparator has active offset compensation which reduces the offset from $1\sigma = 5.87$ mV to $1\sigma = 172$ µV in 100 ns.

The threshold for the dynamic comparator is created by inserting a small charge of $500e^-$ on the detector, whose polarity is opposite to that of the signal. By creating the threshold as a charge, the ratio between the threshold and the signal is made independent of the detector capacitance.

The final pixel is implemented in 40 nm TSMC CMOS technology and occupies an area of 80 µm x 98 µm which includes additional circuits designed to measure and quantify the performance of the pixel. The measurement setup is designed but unfortunately, due to delays in the chip delivery, no measurements could be performed.

Acknowledgements

I would like to express my gratitude to all the people who contributed to the successful completion of this thesis. In the past year, I have learned a lot about project management and gained a lot of knowledge on circuit design. I could not have reached this important milestone without the help and support of the people around me.

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This thesis closes the door of my Master's Electrical Engineering, and I would like to thank you all for being a part of this academic endeavor.

- Lars Bouman
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Contents

Acronyms

ADC Analog to Digital Converter. 9

BSE Back Scattered Electron. 4, 5

CDS Correlated Double Sampling. 14, 15, V

CLK CLocK. 14, 16, 20–22, 33–36, 38, 43, 44, 49, 51, 54, 55

CMOS Complementary MOSFET. 14, I

CSA Charge Sensitive Amplifier. 9, 10, 12

DAC Digital to Analog Converter. 43, 44, 46, 57, I

DCR Dark Count Rate. 8

DFT Design For Testibility. 45

ENC Equivalent Noise Charge. 10

FPGA Field Programmable Gate Array. 6, 33–35, 47–49, 51, 52, I

GPIO General Purpose Input Output. 48, 49

HSMC High-Speed Mezzanine Card. 49, 50

HVT High Voltage Threshold. 24

ISI Inter Symbol Interference. 9, 11

LVDS Low Voltage Differential Signaling. 49, 54

LVT Low Voltage Threshold. 24

MOSFET Metal Oxide Semiconductor Field Effect Transistor. 2, 8, 12, 30

MUX MUltipleXer. 43

NMOS N-type MOSFET. 13

PCB Printed Circuit Board. 6, 47, 49, 50, I

PE Primary Electron. 4

PIN P-type Insulator N-type. 4, 6, 7, 11

PMOS P-type MOSFET. 13

PVT Process, Voltage, Temperature. 29

RMS Root Mean Square. 24

ROIC Read-Out Integrated Circuit. 7, 8, 11

SE Secondary Electron. 4, 5

SEM Scanning Electron Microscope. 4, 26, 35, I, V

SMA Sub-Miniature version A. 49

SNR Signal-to-Noise Ratio. 16

TDC Time to Digital Converter. 9, 38

TIA Trans-Impedance Amplifier. 10

TSMC Taiwan Semiconductor Manufacturing Company. I

1. Introduction

In modern electronics, the size of transistors keeps shrinking down to the nanometer scale. The functionality of these devices depends largely on the accuracy and precision of the lithography process, while their price depends on the throughput: the number of wafers processed per hour/day/week. This gives rise to the need for in-production-line inspection and metrology, for timely discovery of any deviation from the process parameters leading to the production of a large amount of defect wafers. Optical microscopy can only reach amplification factors of 1000, or a spatial resolution of $\sim 0.2\,\mu m$ [1]. This resolution is not sufficient to verify the quality of the nanometer-scale exposed patterns. Scanning electron microscopy, on the other hand, can achieve amplification factors of $3 \cdot 10^6$ [2], which is the reason it is often used when imaging at the nanometer scale is required [3].

Scanning electron microscopes operate by firing a beam of electrons at a sample, and measuring the secondary and back-scattered electrons from the target. Measuring the returning electrons poses quite an engineering challenge, as the signal amplitude is often quite low, and the entire system needs to operate at very high frequencies with limited power consumption. This thesis focuses on building the read-out circuit required to obtain the signal from the detector. The detector is a PIN diode. Its design lies outside the scope of this thesis, and the performance metrics of an existing PIN diode are taken as a given in this work.

1.1 Application background

The read-out circuit in this thesis is designed for a specific detector and a specific application: Scanning Electron Microscopy. However, the proposed solutions can be applied to any diode-based detectors with other parameters and requirements as well.

1.1.1 Scanning Electron Microscope (SEM) imaging

The high magnification SEM provides is the major reason it is heavily used within the scientific community. Possible applications of SEM can vary widely but it can, for example, be used in material sciences, to investigate the surface morphology of metals, polymers and composite materials. It can help analyze the effects of stress on these materials. It is also used in biology to examine the surface features of cells or small organisms, improving our understanding of their functionality. Geologists use SEM to acquire high-resolution images and chemical maps for the mining and mineral processing industries [4]. SEM is also widely used for quality control analysis in different fields, including the semiconductor manufacturing industry, which is the focus of the target application of this thesis.

As mentioned earlier, the Scanning Electron Microscope fires a beam of electrons on a sample, these electrons are called the Primary Electrons (PEs). This beam is moved across the sample with high precision using electromagnetic lenses. The electrons and radiation that come back are then measured to obtain information about the sample. There are multiple mechanisms in which the electrons can interact with the sample to generate a useful signal, these mechanisms are illustrated in Figure 1.1. All of these emissions are useful for determining different specifications of the sample and are often used in combination. Although the focus usually lies on the Secondary Electrons (SEs) and Back Scattered Electrons (BSEs), as these contain the most information about the surface topology [5].

In the first mode, the electron can collide with the sample via an inelastic collision, which results in a Secondary Electron (SE) being emitted back towards the detector. SEs often have lower energies ($< 50\,\text{eV}$) [5, p. 89], which limits the depth at which these electrons can come back to the detector. The SEs are therefore often used for imaging the surface morphology of the sample. SEs also have the highest accuracy of all three modes, which can be a low as 1 nm [6].
The Back Scattered Electron (BSE) collide with the sample via an elastic collision, which allows the BSE to carry information about sub-surface features of the sample. The energy of a BSE is a lot higher than that of a SE and is highly correlated with the atomic number of the atom it collided with. Hence BSE are often used to gather information about the material composition, rather than the surface topology. The BSE mode has a lower accuracy than the SE mode, which typically lies around 50 nm
A third possibility is that the primary electron removes an inner shell electron from the sample. The high-energy electron then takes its place and emits X-rays to release its abundant energy. The energy/wavelength of the emitted X-ray contains information about the energy levels inside the atom it interacted with. This allows the X-ray mode to provide the elemental distribution of the sample. It has the lowest accuracy of all three modes, it varies with sample material and beam energy but is typically around 1 µm.

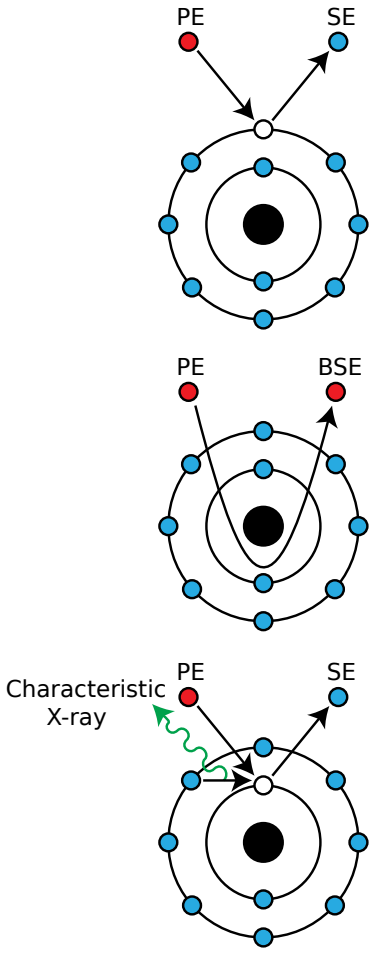

Fig. 1.1: Different electron emission mechanisms [7]

1.1.2 Application requirements

The application requires a very high temporal resolution (2.5 ns) for measuring the BSEs and a high accuracy ($> 95\%$) in doing so. This combination alone poses quite a challenge as the high temporal resolution requires high-bandwidth amplifiers, which have more noise than low-bandwidth amplifiers, lowering the accuracy. Another consideration is that the application requires a large number of these detectors (x1000) to be placed in parallel. Meaning that the read-out circuit should be as power-efficient as possible.

Besides the requirements from the application, another consideration is the performance of the detector itself. The main characteristics of the detector are given in Table 1.1. The detector capacitance C_D and transit time $t_{transit}$ are both preferred to be as small as possible, but a trade-off has to be made. More about the trade-off between these numbers will be discussed in 2.1.

Table 1.1: Detector specifications

Specification	Value	Unit
C_D	$30 \pm 10\%$	fF
$t_{transit}$	1.8	ns
Q_{hit}	$800e^- - 1200e^-$	C
I_{leak}	~ 10	fA

1.1.3 Voltage read-out mode

The signal is a charge generated in the capacitance of the pin detector. Typically to make the measurement independent of the detector impedance, the detector is interfaced with a low-impedance input stage of the readout circuit (this mode of operation is often called "current mode" or "short-circuit mode"). This ensures that the charge signal will be transferred from the detector capacitance into a well-defined component (usually another capacitance), converting it into a voltage with a value independent of the detector capacitance.

However, for this project, the value of the signal is not of importance, but just its occurrence. This allows to interface the detector with a high input impedance stage and operate it in "voltage mode", also called "open circuit mode". In this way, the charge signal is directly converted into voltage in the capacitance of the detector itself. This removes the need to use a power-hungry charge-to-voltage conversion stage (trans-impedance amplifier or charge-sensitive amplifier).

This thesis will focus on the voltage read-out mode of the detector and will investigate its power efficiency, compared with the previously investigated current read-out mode. The major challenges to be addressed by using this method are listed below:

Small signal. The charge signal Q_{sig} generated in the detector is only $800e^- - 1200e^-$, which results in a voltage signal dependent on the detector capacitance $V_{sig} = Q_{sig}/C_D = 5.3\,\mathrm{mV}$. This signal is not only quite small, but if the input impedance of the front-end stages is not sufficiently high (the input capacitance sufficiently low), it will further lower the signal amplitude.

Charge removal. With the current read-out mode, the charge is automatically pulled out from the detector to convert it to a voltage, by keeping the detector in the short-circuit mode. In the voltage read-out mode, the charge will stay on the detector capacitance. If the charge is not removed, the accumulated charge will push the detector out of its biasing point.

Signal dependence on C_D. The voltage signal amplitude will depend on the detector capacitance C_D, which might vary and is prone to parasitics, resulting in additional signal variation. Although only a binary output is required, the variation of the signal amplitude still poses challenges for the selection of the detection threshold level.

1.2 Thesis synopsis

In this thesis, the design of a voltage mode read-out circuit in 40 nm technology for a PIN is discussed.

In Chapter 2, the workings of the PIN diode are discussed. A state-of-the-art analysis is also provided to compare the voltage read-out mode with existing solutions.

The architecture-level decisions made for the read-out will be discussed in Chapter 3. This chapter highlights the main advantages and limitations of using voltage mode.

In Chapter 4, the design decisions of the different blocks in the read-out are discussed. The post-layout simulation results after the design process are presented.

The circuits required to test the performance of the read-out will be presented in Chapter 5. Besides the on-chip circuitry, the PCB and FPGA code used for the chip testing are also discussed.

In Chapter 6, the measurements planned to be performed on the chip are presented. Due to delays in the shipment of the chip, not all results are present.

Finally, a conclusion will be provided in Chapter 7. There will also be some recommendations for future improvements to the system.

2. Feasibility analysis

In this chapter some initial analysis will be done on the feasibility of this project. The physics behind the detector will be introduced, and the design considerations resulting from this are presented. Finally a comparison is made with existing particle ROICs.

2.1 Physics of the detector

The detector itself is a PIN-diode, which is similar to a regular PN-junction diode, but with a layer of intrinsic semiconductor material in between. An overview of the diode structure is shown in Figure 2.1. This intrinsic layer has a large resistivity and helps to increase the total depletion width of the diode [8]. For particle and photon detection the PIN diode is used in reverse bias. The reverse bias across the diode creates an electric field and removes any free charge carriers still left in the intrinsic layer. At a certain reverse bias voltage, called the swept-in voltage, the intrinsic layer will be completely depleted from any free charge carriers. PIN diodes used for particle detection are usually biased beyond this voltage.

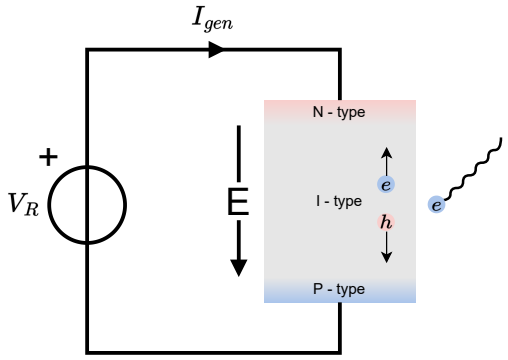

Fig. 2.1: PIN-diode structure

2.1.1 Internal physical behavior

For the application of this project, the diode will be used to detect incoming electrons. When an electron with enough energy (Bandgap of silicon is 1.12 eV) hits the diode, it can promote electrons from the valence band to the conduction band, creating electron-hole pairs. If the electron-hole pairs are generated outside the depletion region, they will quickly recombine and can't be measured. However, if the electron-hole pairs are generated inside the depletion region, the electrons and holes will be accelerated away from each other by the electric field and be swept to opposite electrodes. This can electrically be seen as a small current, I_{gen}, which flows from the n-type to the p-type of the diode.

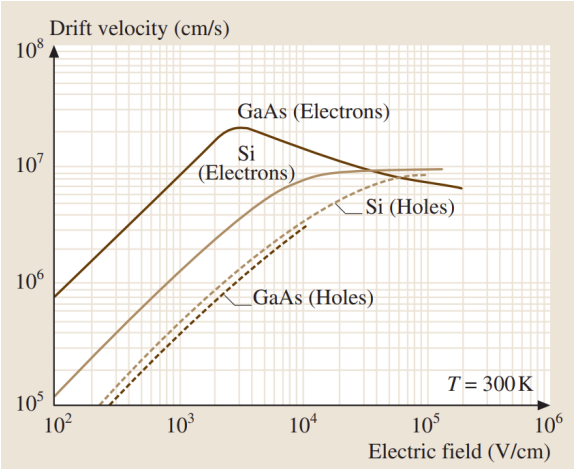

Fig. 2.2: Drift velocity saturation of electrons and holes in Si and GaAs [9, p. 37]

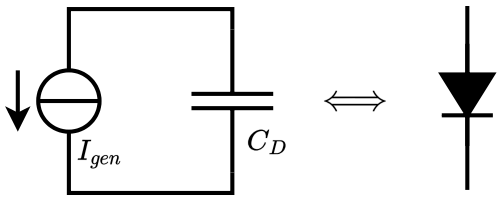

Fig. 2.3: PIN-diode equivalent circuit

To have the highest chance possible of creating a current, the depletion region of the diode is made larger by inserting a large intrinsic region and applying a reverse bias. There will be an electric field across the intrinsic region due to the diffusion of charge carriers and the reverse bias that is applied. The time it takes for the electric field to transfer all the generated charge to the electrodes is called the transit time [9]. A larger intrinsic layer will result in a larger transit time. A larger electric field will reduce the transit time by increasing the drift velocity of the electrons and holes, up until it saturates. The drift velocity in silicon for different electric field strengths can be seen in Figure 2.2.

2.1.2 Equivalent circuit

The reverse biased pin diode can electrically be modeled by the schematic shown in Figure 2.3. The source I_{gen} represents the current generated in the detector due to the generation of electron-hole pairs. The capacitor C_D is the parasitic capacitance of the diode, this capacitance is decreased by increasing the width of the intrinsic layer. For the application of this thesis project, the detector capacitance is approximately 30 fF. Although there is also some leakage current through the capacitor, it is omitted because its value is negligible in comparison to the gate leakage current from the connected MOSFETs. Nevertheless, the leakage, either from the detector or transistors, is often the main contributing factor for the Dark Count Rate (DCR) (The rate at which hits are counted when no hits arrive). As the detector will be operated in voltage mode, the detector node is initially floating. The biasing of the detector should ensure the DC stays at the correct level such that the detector remains biased correctly and the DCR remains low.

2.1.3 Design considerations

The amount of electron-hole pairs generated is proportional to the energy of the incoming electron, and can't be altered by the design of the PIN diode. Since the electrons can only be measured if they hit the diode in the depletion region, a larger depletion width will result in a larger probability of detecting bypassing electrons. A larger depletion width will however also result in a larger transit time since the electron-hole pairs need to travel a longer distance.

$$t_{transit} = \frac{W_{depl}}{v_d} \quad \text{with} \quad v_d = \mu_d E$$

Where the drift velocity v_d will be limited by the saturation velocity as shown in Figure 2.2. As a final consideration, the parasitic capacitance of the diode C_D will decrease for wider depletion widths, which will increase the signal amplitude:

$$V_{sig} = \frac{Q_{sig}}{C_D} \quad \text{with} \quad C_D \propto \frac{1}{W_{depl}}$$

Following the specifications of this project, the amount of electron-hole pairs generated by an incoming electron varies between $800e^-$ and $1200e^-$. The generated electron-hole pairs are generated in a confined space inside the depletion region and move at a constant velocity toward the electrodes. This is modeled by a square wave current I_{gen}. The transit time of the PIN diode is given to be 1.8 ns, which means that the value of the current will be on average $\frac{1000e^-}{1.8\text{ ns}} = 89.0$ nA.

2.2 Previous work

This section provides an overview of the existing knowledge and research on particle ROICs. It begins by reviewing foundational concepts and limits that arise when designing a high-speed, high-accuracy and low-power ROIC. Several existing methods are given, and some example read-out circuits are shown. Finally, a comparison between several existing solutions will be presented.

2.2.1 Foundational limits

In the target application, high speed, high accuracy and low power consumption are required. To achieve a high accuracy, the noise should be minimized. However, this comes at the cost of reducing the bandwidth. When the bandwidth becomes too low the signals pile up on top of each other and the error rate rises due to the introduced ISI-errors (Inter Symbol Interference). This leads to an optimum bandwidth where the minimum error rate is achieved. A conceptual plot of this trade-off is shown in Figure 2.4.

To get around the limitation of the error rate introduced by this effect. Designers have tried to compensate for the ISI induced errors, such that they could lower the bandwidth further to reduce the error rate. This has been done by using multiple thresholds in the subsequent stages [10] [11]. This allowed the initial amplifier to have a significantly lower bandwidth and lower noise. However, these solutions did require an additional amplifier which also increases the power consumption of the complete read-out circuit.

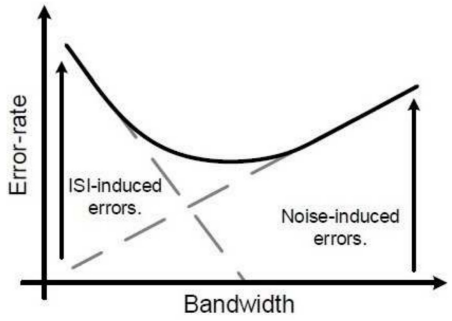

Fig. 2.4: Trade-off between bandwidth and error rate [12]

2.2.2 Frequently used readout circuits

Instead of using multiple thresholds, designers often use a Charge Sensitive Amplifier (CSA) in combination with a shaper. The CSA pulls the generated current from the detector into a feedback capacitor C_f, this charge then slowly depletes over a parallel resistor R_f. This acts as an integrator and creates a sharp rise in the signal followed by a very shallow decay. In the shaper, the DC component is filtered out using a band-pass filter. This only allows the sharp edges to pass the filter. The output from the shaper is then connected to an Analog to Digital Converter (ADC) to obtain a digital output. A high-level overview of the signal path is shown in Figure 2.5.

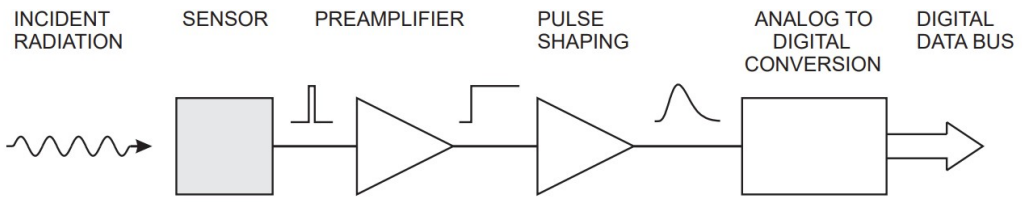

Fig. 2.5: High-level diagram of the pulse shaping technique. The short current pulse is integrated by the CSA, and the resulting step function is passed into the shaper to retrieve a short pulse [13]

The complexity of the ADC at the end of the signal chain depends on the target application. It can be a discriminator with a single digital output, which compares the output of the shaper with a threshold [14], or it can be more complex, using a TDC to measure the time the signal is above a given threshold [15]. Below are listed some examples of read-out circuits.

2.2.3 Comparison

For this comparison, 5 different read-out circuits are used. PXF40 [14], UFXC32k [16], EIGER [17] and Medipix3 [11] all use a CSA in combination with a shaper. The ADC differs per read-out but

most often consists of a discriminator in combination with a counter. The 2Vth TIA [12] readout addresses the same project this thesis addresses. An overview of different parameters of each read-out circuit is shown in Table 2.1. As the signal is often expressed in an amount of electrons, the input referred noise is converted into an Equivalent Noise Charge (ENC) for comparison.

Table 2.1: Comparison between the different read-out circuits

	PXF40 [14]	**UFXC32k** [16]	**EIGER** [17]	**Medipix3** [11]	**2Vth TIA** [12]
Pixel size [µm^2]	100 x 100	75 x 75	75 x 75	55 x 55	200 x 200
Process	40 nm	130 nm	250 nm	130 nm	65 nm
ENC [e^-]	212 / 185	123	110	80	174
P_{pix} [µW]	45 / 100	26	-	9	2850
Count rate [Mcps/mm^2]	1224 / 1216	220	146	87	10000

For the application of this project, the idea is to remove the power-hungry preamplifier, and instead use the detector capacitance itself to integrate the signal charge. A new architecture will be proposed in Chapter 3 that removes both the CSA and the shaper which will result in a more power-efficient solution.

3. Architecture design

The final system will consist of a few thousand pixels in parallel, which all have their own Read-Out Integrated Circuit (ROIC) to convert the small signal produced by the detector to a digital output. A generic overview of a pixel is shown in Figure 3.1.

The detector itself should be biased with a high voltage to ensure the generated electron-hole pairs are moving at sufficiently high drift velocities. Since the technology only has 1.1 V and 2.5 V devices, a large reverse bias is applied at the detector anode. The top of the detector can now be biased at a smaller voltage to ensure the subsequent stages are biased correctly, while V_R can be selected such that the detector is correctly biased. Next, the detector voltage should be compared with a certain threshold to determine if a hit has landed. While it is still incomplete, this simplified diagram will be used as a basis for the system architecture. It should be noted that the biasing of the detector cathode is not yet shown, as it requires some design trade-offs to be made.

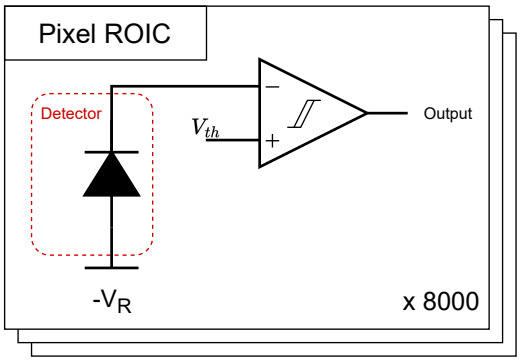

Fig. 3.1: Generic system overview

3.1 Charge depletion

Since voltage read-out mode is used, the charge remains on the detector. If this charge is not removed, the hits will be integrated on the detector capacitance, and push the PIN diode out of its operating region. The pile-up of a few hits can be tolerated, as the voltage deviation is only a few mV per hit. However, it is necessary to eventually remove the generated charge.

There are several solutions for removing the charge, each of them has its advantages and disadvantages.

3.1.1 Depleting resistor

The most straightforward solution would be to use a resistor connected to a biasing voltage to deplete the charge in the detector, shown in Figure 3.2. If a hit arrives, it will deplete with the time constant $\tau = R_{dep}C_D$. An important consideration about this solution is that it will add $\mathrm{kT/C}$ noise, which is independent of the resistor value. The noise is equal to $V_{n,rms} = \sqrt{\mathrm{kT/C_D}} = 372\,\mu\mathrm{V}$ (for $\mathrm{T} = 300\,\mathrm{K}$). This will limit the theoretically maximum SNR to be $\mathrm{SNR}_{max} = 14.2$. Although this value would be sufficient for the application, it is important to consider that this is only considering the noise coming from the resistor, any other sources of error or noise will lower this value. Leaving the following stages with more stringent noise requirements to achieve, which often leads to a higher power consumption.

The selection of the time constant plays an important role in the voltage waveform of the resulting signal. If the time constant is taken too small, a lot of the generated charge will already be depleted when it arrives, losing a lot of the signal amplitude. Taking a too large time constant, can result in a pile-up of the signals, which leads to ISI-errors. An example of both these problems is shown in Figure 3.3.

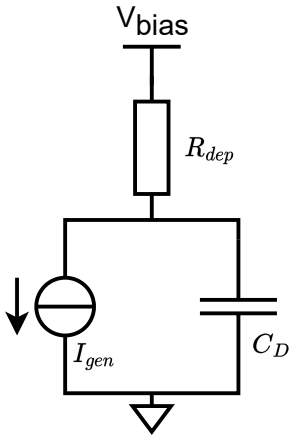

Fig. 3.2: Depleting resistor circuit

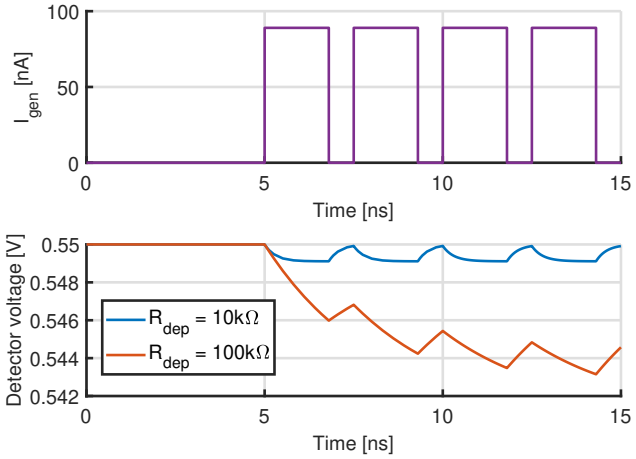

Fig. 3.3: Results of a pulse train when the depleting resistor is too small, or too large

The signal amplitude when $R_{dep} = 10\,\text{k}\Omega$ is only 1 mV, even though the maximum achievable signal is 5.3 mV. On the other hand, if a value of $R_{dep} = 100\,\text{k}\Omega$ is used, the signal is not depleted fast enough and the hits stack on top of each other. This eliminates the option of using a single threshold to determine whether a signal has arrived.

If the value of R_{dep} is optimized such that the maximum amplitude is achieved while still utilizing a single threshold to identify incoming signals, a value of $R_{dep} \approx 25.6k$ is obtained, which leads to a signal amplitude of $V_{sig} = 1.20\,\text{mV}$. This would reduce the maximum achievable SNR to $\text{SNR}_{max} = 3.2$, which is insufficient for the application.

Another option would be to use a very large resistor and compensate for the signal pile-up. This can for example be done by applying a band-pass filter, such that only the sharp edges of the signal arriving are shown at the output. Similar to the technique also frequently used in previous work done on this subject [13] [14] [16]. However, in those cases the filtering is done after a CSA stage, which has already increased the signal amplitude. As our signal amplitude is quite low without the amplifier, an active filter is required to keep the SNR close to SNR_{max}. The active filter has very little design margin for the noise, as the SNR cannot be degraded much further. An initial design showed that the resulting active filter would consume around $300\,\mu\text{W} - 400\,\mu\text{W}$, which already exceeds the power consumption of the previously designed solutions. Hence the depleting resistor is discarded as a viable solution.

3.1.2 Reset switch

Another solution would be to deplete the charge using a reset switch. A reset switch would be implemented using a MOSFET. This causes the switch to have significantly lower noise than the resistor. In this case the noise is dependent on the sizing of the switch ($\sim 10\,\mu\text{V}$). Although the lower noise is a very nice feature and leaves a lot more freedom in the design of the subsequent stages, there are some downsides. A few major drawbacks of the reset switch are listed below:

Short reset timing As the charge-to-voltage conversion of the detector takes about 1.8 ns to reach the maximum voltage value, and hits can arrive with a frequency of 400 MHz, this only leaves 0.7 ns for the detection of the event, and resetting the detector voltage. This short duration means the switches need to have a sufficiently low ON resistance, to ensure the voltage is reset correctly.

Larger switches also produce more noise and use more power to switch, so there is a trade-off to be made.

Charge injection As the switch closes, it creates a channel to connect the detector voltage to its bias. This channel consists of either electrons or holes (depending on if an NMOS or PMOS is used). To create the channel, the electrons or holes are pulled from the source and drain towards the gate by the applied gate voltage. After the reset is done, and the switch opens again, the electrons and holes from the channel move back towards the source and drain. This charge gets injected into the source and drain of the transistor, creating a voltage difference from the correct bias voltage. This issue becomes more significant for larger switch sizes, as they have more charge inside their channel.

Clock feedthrough A final important issue when using reset switches is the feedthrough of the control signal. This is the coupling between the transistor control signal of the switch, and the source/drain, through the C_{gd} and/or C_{gs}. Due to this coupling, a small portion of the control signal will appear on the detector voltage when the switch is opened again. This difference is given by $V_{error} = V_{step} \cdot C_{gd}/(C_D + C_{gd})$, which for unit size transistors corresponds to approximately 550 µV. This is a large value compared to the signal, and it will only become worse for larger switches. However, there are possible solutions for this issue, such as using complementary switches to cancel out the feedthrough or compensating for the additional voltage in some other manner.

For the final application, a reset switch is used to remove the charge from the detector capacitance. It does present some challenges for the design, but none of them are insurmountable, and it leaves more room for the noise performance of subsequent stages.

3.2 Sync vs. async operation

As the charge now stays on the detector capacitance until the reset switch is closed, it presents the possibility to monitor the detector voltage periodically, instead of continuously. Periodically monitoring the detector voltage can allow for power savings, as dynamic circuits are much more efficient than their time-continuous counterparts. There are however also drawbacks of using this method, which will be discussed in the following subsections. These drawbacks should be taken into consideration when considering the periodic monitoring of the detector voltage instead of continuous monitoring.

3.2.1 Sampling at 400 MHz

Initially one might compare the detector voltage to a threshold at each time interval to detect if a hit has occurred and reset the detector if needed. However, this will result in the possibility of missing hits.

The main problem is that it is unknown in which phase of the clock signal the hit arrives. And since the hits arrive according to a Poisson distribution it is not possible to predict the phase in which they arrive. In Figure 3.4, the sampling happens at the positive clock edges, and for now, it is assumed to happen instantaneously. When the hit crosses the threshold right after the sampling happens, it is not yet detected but will be detected in the following clock cycle. Once it is detected, the charge at the detector needs to be reset, so the reset switch will pull the detector voltage back to its bias. However, the next hit can arrive only 2.5 ns after the previous one, and will partially be removed by the reset switch.

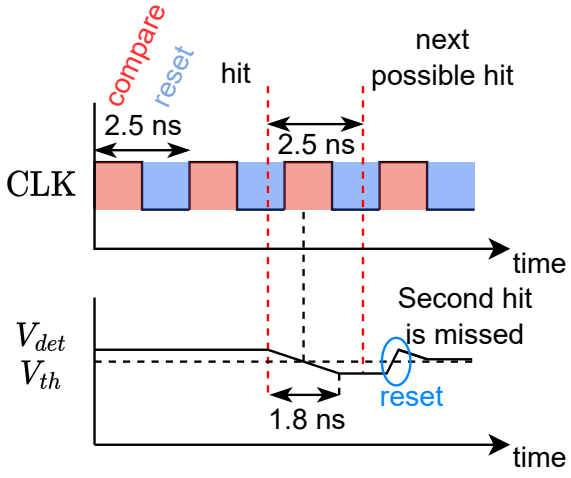

Fig. 3.4: Illustration of the 400 MHz sampling issue

The amount of voltage signal that can be removed in the worst case $V_{removed}$, is expressed by:

$$V_{removed} = V_{th} + V_{sig} \cdot \frac{T_{rst} + T_{comparison}}{t_{transit}} \tag{3.1}$$

Where V_{sig} is the amount of voltage that is generated when all the signal charge is converted to a voltage by the detector capacitance, V_{th} is the threshold voltage, T_{rst} is the time it takes for the switch to reset the detector voltage, $T_{comparison}$ is the time it takes for the system to compare V_{det} with V_{th} and $t_{transit}$ is the transit time of the detector diode.

A full derivation of Equation 3.1 can be found in Appendix A.1. One important conclusion from this equation is that there will always be some charge that is removed if the hits land in the wrong phase of the clock cycle. This can be minimized by setting the threshold very close to the bias voltage, such that hits are much more easily detected. One issue of placing the threshold very close to the bias voltage is that the noise will more easily be able to push the voltage across the threshold and count towards a hit, even though no hits arrived. This will cause the noise to become more prominent and increase the dark count rate.

Removing a large portion of the hit if it lands in the wrong clock phase is undesirable, as the initial signal already has a very low amplitude. The effect of such a small signal is that the subsequent stages will require more amplification and a lower noise floor. Since the power consumption scales with $P = 1/V_{n,rms}^2$, lowering the noise floor by a factor of 2 would quadruple the power consumption. Because of this simply sampling at 400 MHz is not a desirable solution.

There also exists alternative solutions that use sampling, but do not delete a large portion of the signal if the hit lands in the wrong CLK phase. These solutions are also worth investigating and will briefly be discussed next.

3.2.2 Correlated Double Sampling (CDS)

Correlated Double Sampling is often used in CMOS image sensors [18] [19] to remove offset of individual pixels. This principle can also be applied here. The idea behind CDS is that the state of the detector is sampled twice: First, after a reset to obtain the baseline value, and a second time after a possible signal has arrived. These two samples are then subtracted from each other.

By subtracting the signals, the offset of the pixel will be removed, and only the difference will be measured. In CDS the idea is to take these samples in very quick succession. In that case not only the offset but also a lot of the low-frequency noise will be removed since the low-frequency noise of these samples will be correlated. The subtraction can be done by giving both samples to different inputs of a subsequent stage with a differential input. An example circuit is shown in Figure 3.5.

The final output voltage will be given by: $V_{out} = A \cdot (V_{det}(t = \phi_1) - V_{det}(t = \phi_2))$. The two capacitors are used to store the value of the signal at a specific time. By comparing the signal to its previous value, the reset does not need to happen after every hit. It only needs to happen if the detector is going to be pushed outside its biasing point. Because there is no need for a reset, the timing issue discussed in 3.2.1 is no longer present. There will be some dead-time introduced whenever the detector is reset. This dead-time will lead to errors in the read-out circuitry, but as the hits do not have a high probability of occurring, the resulting inaccuracy is still manageable.

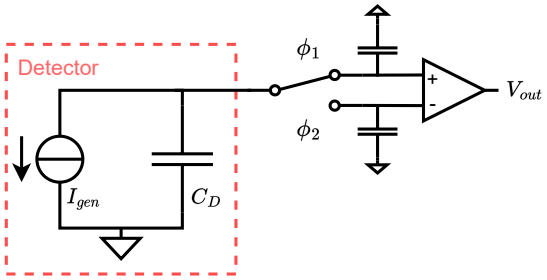

Fig. 3.5: Correlated Double Sampling using two storage capacitors (detector biasing not shown)

Although the reset timing is solved by using CDS, there is a new timing issue introduced by not resetting. This new issue is illustrated in Figure 3.6.

Ideally, a hit falls in between two sampling moments. In that case, the subsequent stage can measure the full signal amplitude, this is illustrated in Figure 3.6 for the first hit. But what can also happen is that the detector voltage is sampled halfway through a hit arriving. In that case, the subsequent stage will measure half the signal twice, instead of the full signal once. This will either double count or miss the hit depending on if the threshold is set above or below half the signal amplitude. This effect is shown for the second hit and will lead to errors that cannot be corrected by subsequent stages. Because of this, and the dead-time that the occasional reset will introduce, CDS is not a promising solution for the application.

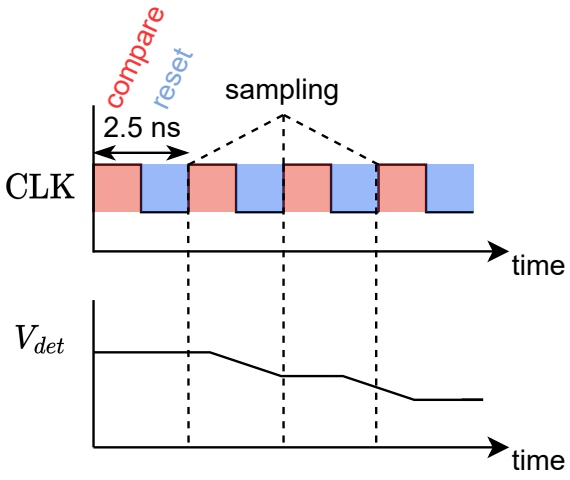

Fig. 3.6: Illustration of the timing issue when using CDS

3.2.3 Higher sampling frequencies

Another solution would be to sample at a higher frequency. This will ensure that even if the hit lands in the undesired part of the clock phase, there will be another sampling moment shortly after that which can still measure the hit, and reset the detector in time for the next hit. The working principle is illustrated in Figure 3.7.

As can be seen, even if the detector voltage crosses the threshold right after a sampling moment (positive CLK edges), the next CLK cycle will arrive in time to reset the detector before the next hit arrives. Since the hits should be classified in 2.5 ns time slots, an 800 MHz CLK will allow for easy assignment to the correct time slot, while also solving the 400 MHz sampling issue. Of course, this will also consume twice the power as the sampling needs to happen twice as often. Though significant, this should be compared with the power consumption of a time-continuous solution, before drawing any conclusions.

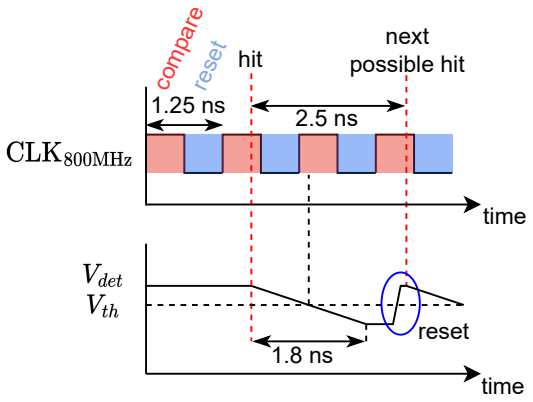

Fig. 3.7: Detector voltage when sampling at 800 MHz

After some investigations, it was found that the power reduction caused by having discrete sampling intervals outweighs the additional power consumption caused by sampling at 800 MHz.

3.2.4 Reset width

Although sampling at 800 MHz seems to be a good solution, the reset should happen fast to prevent any loss of the next signal, as might be seen in Figure 3.7. To ensure no part of the next hit can be deleted, Equation 3.2 needs to hold.

$$T_{reset} < 1/f_{hits,max} - T_{clk} - t_{transit} \cdot \frac{V_{th}}{V_{sig}} \tag{3.2}$$

Where $f_{hits,max}$ is the maximum frequency at which events can arrive, T_{clk} the period of the clock signal, $t_{transit}$ the transit time of the detector diode, V_{th} is the threshold voltage and V_{sig} is the amount of voltage that is generated when all the signal charge is converted by the detector capacitance.

Since the hits are assumed to arrive at least 2.5 ns apart, $f_{hits,max}$ is 400 MHz. If the threshold is placed at half the signal amplitude, the equation becomes: $T_{reset} < 350$ ps. Although this is a short time frame, it is possible in the 40 nm technology used for this project. If the reset exceeds Equation 3.2, part of the next hit will be deleted, which lowers the SNR.

Comparing all the different solutions, sampling at 800 MHz seems to be the most viable solution. It will consume the least amount of power and can compare the full signal amplitude. This leaves the subsequent stages with some design room, as the only error sources added thus far are the errors coming from the reset switch.

The next part will focus on the design of the discrete-time comparator and the design challenges that arise there.

3.3 Offset limitations

The detector voltage should be compared with a certain threshold. All comparator circuits suffer from a non-ideal offset that shifts this threshold up and down. If the offset is too large, it can even push the threshold so far away that it counts a hit every single CLK cycle, or never at all. Limiting this offset is an important design consideration that needs to be taken into account when designing a dynamic comparator.

3.3.1 Passive offset compensation

The most common way of offset compensation is the passive offset compensation. To understand exactly why it works, it is important to understand where exactly the offset in comparators is coming from.

A comparator tries to compare the two input signals and gives a digital output based on which is larger. In a comparator, offset arises from any asymmetries within the circuit. This means that any mismatch between the two input sides will push the comparator more towards one output. To minimize the offset the mismatch between the two input sides should be minimized. Most of the offset in amplifiers comes from the input pair of transistors [20]. Every mismatch effect after the input pair will be divided by the gain of the input transistors. Because of this designers often match the input pair very well to minimize the offset, while the other transistors do not have such strict requirements.

Besides layout techniques, mismatch between the input transistors can also be reduced by increasing their size. Most of the offset in the input pair comes from the mismatch in threshold voltage. Pelgrom's law [20] states that the standard deviation of the threshold voltage scales inversely proportional to the square root of the transistor area:

$$\sigma(\Delta V_{th}) = \frac{A_{V_{th}}}{\sqrt{WL}} \tag{3.3}$$

In this equation $A_{V_{th}}$ is a constant that is defined by the technology, for the technology used it is 2.77 nVm. For minimum-sized transistors, this would give $\sigma(\Delta V_{th}) = 40\,\text{mV}$.

However, the size of the input pair cannot be increased without limit. By increasing the size of the input pair, their gate capacitance also increases. Since the gate will be directly connected to the detector, this capacitance will be placed in parallel with C_D and lower the amount of voltage generated by the incoming charge according to:

$$V_{sig} = \frac{Q_{sig}}{C_D + WL \cdot A_{C_{gg}}} \tag{3.4}$$

Here $WL \cdot A_{C_{gg}}$ is the equivalent input capacitance, C_{gg}, where $A_{C_{gg}}$ is a constant defined by the technology. $A_{C_{gg}}$ has a value of $11.09\,\text{mF}\,\text{m}^{-2}$ for the technology used. There is a trade-off between signal amplitude and offset from the input pair. The ratio $\phi_{offset} = V_{sig}/\sigma(\Delta V_{th})$ can be maximized, to obtain an optimum sizing for the offset of the input pair. The optimum for ϕ_{offset} occurs when $C_{gg} = C_D$, and is given by:

$$\phi_{offset,max} = \frac{Q_{sig}}{2\sqrt{C_D A_{C_{gg}} A_{V_{th}}^2}} \tag{3.5}$$

Evaluating Equation 3.5, gives a value $\phi_{offset,max} = 1.59$ or 4.0 dB. This ratio falls short of meeting the requirements for the application, as it will lead to high probabilities of errors occurring. While leveraging the size of the input pair can help minimize the offset passively, an active compensation is necessary to remove the offset further. The specific implementation details regarding the active offset compensation will be discussed in 4.2.

3.4 Threshold generation

The dynamic comparator needs to compare the detector voltage with a threshold to conclude if a hit has landed. To ensure a zero output when there are no hits, a threshold needs to be put in place to tilt the comparator towards a '0' output. The threshold can be seen as a fixed offset that is deliberately added to the comparator. This threshold should be very accurate, as any inaccuracies

will add to the inaccuracy of the final offset. It can be implemented at different locations in the circuit, namely:

At the input of the comparator The threshold can be implemented by placing a voltage slightly lower than the bias voltage at the positive input of the comparator. This will tilt the comparator towards '0' when the detector voltage is at its bias. When a hit lands, the detector voltage will drop below the threshold voltage V_{th} and the comparator will give a '1' as output.

Inside the comparator The threshold can also be implemented by designing the comparator itself such that it tilts more toward one side. This can be done by creating an asymmetry in the design of the comparator. It should be noted that this should be switchable, as the active offset calibration should not calibrate for the threshold. So the asymmetry needs to be able to be added and removed using digital logic.

While both methods appear to be viable solutions at this stage, the first method has a significant advantage that will be elaborated on below.

3.4.1 C_D inaccuracies

Previously, the threshold was indicated by a voltage V_{th}. But the signal is defined by an incoming charge Q_{sig}. This charge is converted to a voltage through the detector capacitance C_D. However, C_D may have some deviation from its nominal value (Indicated in Table 1.1). Instead of adding a fixed amount of voltage offset as a threshold, it would be better to add a fixed amount of charge offset as a threshold. In that case, both the threshold and the signal will be converted to a voltage with the same factor C_D. This keeps the ratio between the threshold and the signal constant.

As the comparator itself compares voltages after the charge has been converted to a voltage, implementing an offset inside the comparator is no longer a possibility. Instead, the threshold should be generated at the input of the comparator. On the **negative** terminal of the comparator, where the detector is also connected. In this case, the generated Q_{th} will be converted to a voltage on the detector capacitance.

Generating such a small Q_{th} poses a significant design challenge, as it should be smaller than the signal ($Q_{sig} = 1000e^-$). The details of implementing the Q_{th} generator will be discussed in 4.3.

3.5 Architecture overview

The final architecture is shown in Figure 3.8.

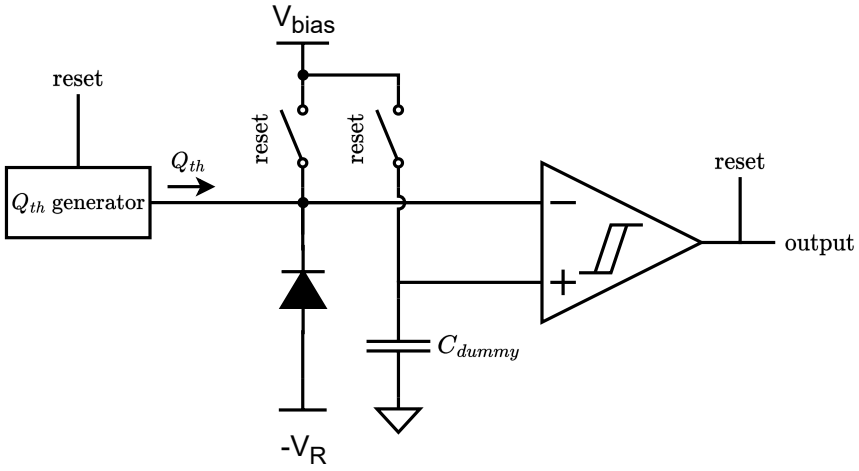

Fig. 3.8: Architecture overview of the read-out circuitry.

The comparator works at 800 MHz and utilizes active offset compensation to remove the offset. When the comparator detects a hit, it resets the detector voltage to the bias and injects a threshold charge onto the detector capacitance C_D. A second capacitor, C_{dummy}, is placed on the other terminal of the comparator. It is also connected via a reset switch to the bias voltage, to mimic the detector behavior. Any charge injection from the switches or kickback from the comparator are now common mode errors, which the comparator can tolerate. It should be noted that the `reset` signal from Figure 3.8 is also the output of the system, where a '1' is indicative of a hit.

3.5.1 C_D and C_{dummy} mismatch

The errors caused by the kickback and charge injection are only common mode if C_D and C_{dummy} are equal. However, this cannot be guaranteed due to variations of both capacitors. This makes matching these two capacitors to the usual degree of accuracy very difficult. Some differential signal will be introduced from the kickback of the comparator and the charge injection from the switches.

The result of these errors is that the comparator will become unbalanced and create an additional offset. If however, these errors are also present during the offset calibration, their contribution will be incorporated in the calibration and their effect is significantly reduced. Still, it is important to minimize these effects, as they will necessitate a larger compensation range for the offset calibration. The compensation range of the offset calibration is a design parameter that requires careful consideration and is not readily available without additional cost.

4. Design and implementation

The design of the readout is subdivided into different blocks, which will be discussed separately. An overview of all the blocks is given in Figure 3.8. Besides the blocks present in the figure, some additional blocks are also required to generate the 800 MHz CLK and control the width of the reset pulse. These will be discussed in Section 4.4.

4.1 Dynamic comparator

The dynamic comparator is the core component of the system. It needs to compare the voltage on the detector capacitance V_{det} with the voltage on the dummy capacitor V_{dummy}. Although there exist many different topologies for dynamic comparators, most of them follow a similar structure. An overview of this structure is shown in Figure 4.1.

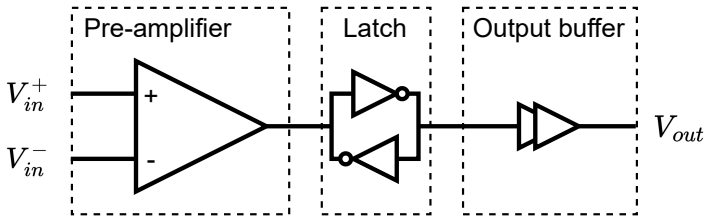

Fig. 4.1: Generic implementation of a dynamic comparator

The differential signal is first amplified in a pre-amplifier. Because of this amplification, the offset of the latch, which can reach 100 mV, can be tolerated. The latch itself implements positive feedback and is held at the unstable equilibrium during the reset phase. When the comparison needs to be made, the latch is released and goes into one of its stable states. The latch is pulled towards a specific direction via the pre-amplifier, which determines if the final output is a '1' or a '0'.

Below the main challenges, advantages and performance requirements of the comparator are discussed:

Speed The comparator should be able to compare the two voltages within 1.25 ns, as it needs to operate at 800 MHz. Within this time it also needs to reset itself and be ready for another hit.

Static power consumption The main reason a dynamic comparator can be more power efficient than a high-bandwidth time-continuous comparator is because it only consumes dynamic power. Once it has made a decision, or once it has been reset, it no longer consumes any static power. The energy required for making a decision is based on the parasitics that need to be charged/discharged when switching between the comparison and reset state.

Pre-amplifier gain The pre-amplifier is in an open loop configuration to reduce the noise and offset coming from the latch. By separating the pre-amplifier and the latch, the pre-amplifier can be used to reduce the noise and offset, whereas the latch is used to speed up the decision-making. The result is a very fast comparator which also can achieve low offset and noise. To separately design the pre-amplifier and the latch, they should have a different biasing current. Since the pre-amplifier needs a lot of gain, it should be biased in weak inversion and have a relatively low biasing current. The latch on the other hand needs to make a decision fast and requires a larger biasing current. Due to the different required biasing currents, the pre-amplifier and latch are often on separate current branches in most modern dynamic comparator designs.

Kickback When a dynamic comparator makes its decision, the voltage on the drain of the input transistors often changes over the entire supply. This variation is carried over to the input through the gate-drain capacitance. This change on the input can affect the final decision of the comparator if the magnitude of the variation is of the same order as the signal.

The most common methods to reduce kickback are: reducing the gate-drain capacitance, reducing the voltage variation on the drain nodes of the comparator, or ensuring the kickback is equal on both terminals of the comparator. If the kickback is common-mode the comparator can still differentiate the differential-mode signal.

Noise When making a decision, the comparator is influenced by the noise created by its components. Since the output of the comparator is a digital signal, only the input-referred noise will be taken into consideration when building the comparator. The analysis of the noise is not as straightforward as in time-continuous circuits, as there is no operating point at which the comparator works. More on the analysis of the noise will be discussed in 4.1.3.

CLK timing Finally, the comparator will be triggered with the CLK signal. In some comparators however, the latch and pre-amplifier have a different trigger [21]. This is done to ensure the latch only triggers after the pre-amplifier has already amplified the signal. However, this timing can be very process-dependent, which in turn makes the pre-amplifier gain process-dependent. Therefore it is preferred to use a single CLK signal to ensure the comparator performs similarly in all process corners.

4.1.1 Miyahara's dynamic comparator

For the dynamic comparator topology, Miyahara's dynamic comparator [22] was chosen. A schematic diagram is shown in Figure 4.2. The topology was chosen due to fact that it tackles many of the challenges highlighted above. Below is a short explanation on how the comparator operates and what advantages it has.

During the reset phase (CLK = 0), the Di nodes are pre-charged to V_{DD} by M4/M5. Since both Di nodes are at V_{DD}, M6-M9 turn off the latch, and M10/M11 ensure both outputs are at 0 V. When the comparison starts, the CLK goes to V_{DD} and M3 starts to discharge the parasitic capacitance at the Di nodes through M1/M2. The discharging happens at different rates based on the input voltage. When the Di nodes have discharged far enough, M6-M9 pull the top of the latch to V_{DD}, and M10/M11 pull the latch in different directions. M6/M7 also ensure each side of the latch gets a different current based on the differential signal at the Di nodes. This allows for a better control of the latch with the signal from the Di nodes. The latch itself uses positive feedback to quickly amplify the differential signal at the Di nodes to a full digital signal.
The comparator has a separate current branch for the pre-amplifier and the latch such that their currents can be tuned separately. Furthermore, the latch does not require a separate CLK phase and is enabled automatically when the pre-amplifier has amplified the input signal by a fixed amount. It also has no static power consumption. There is some significant kickback present from the Di nodes since they vary between V_{DD} and GND, but this is needed to obtain a high gain in the pre-amplifier. The kickback from the comparator will instead be reduced by ensuring the kickback is a common-mode error.

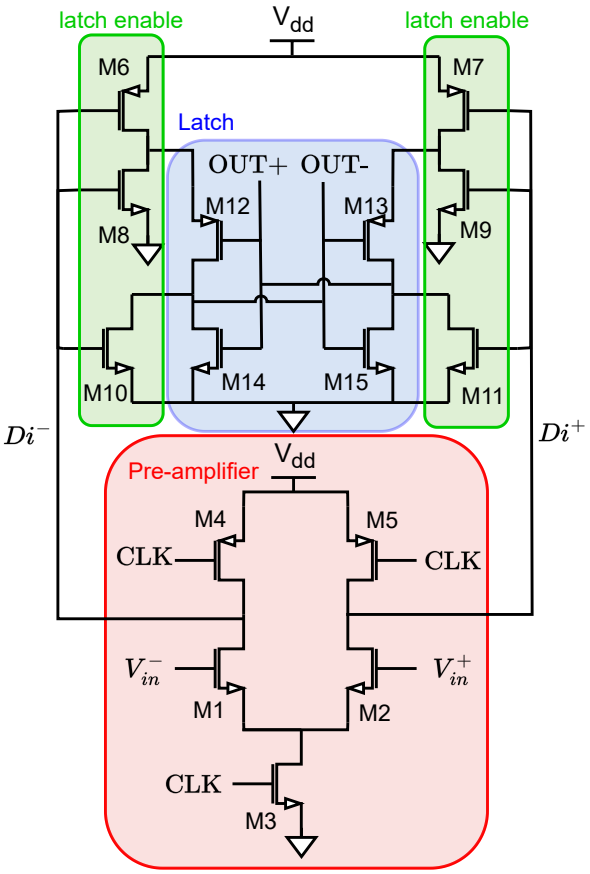

Fig. 4.2: Miyahara's dynamic comparator

4.1.2 Pre-amplifier gain

The pre-amplifier should preferably have a high gain such that it reduces the noise and offset coming from the latch. To ensure this, an expression can be written for the gain. The differential voltage difference that is generated on the Di nodes is given by:

$$\Delta V_{Di}(t) = \frac{g_{m1,2}\Delta V_{in}}{C_{Di}} \cdot t \tag{4.1}$$

This equation only holds while the latch is still disabled, as soon as M6/M7 pull the top of the latch to V_{DD}, the latch makes its decision based on the differential voltage present at the Di nodes at that moment. M6/M7 will enable the latch if the voltage on the Di nodes gets pulled below the threshold of the top inverters (M6-M9), $V_{th,inv}$.

If the rate at which the Di nodes discharge is taken to be approximately equal, the average current flowing through M1/M2, I_{cm}, can be used to get an approximation for the time after which the inverters will be enabled.

$$t \approx C_{Di} \cdot \frac{V_{DD} - V_{th,inv}}{I_{cm}} \tag{4.2}$$

Combining Equation 4.1 and 4.2 gives:

$$A_{pre-amp} = \frac{\Delta V_{Di}}{\Delta V_{in}} = \frac{g_{m1,2}}{I_{cm}} \cdot (V_{DD} - V_{th,inv}) \tag{4.3}$$

Equation 4.3 shows that the gain of the pre-amp is independent of the parasitic capacitance at the Di nodes. It should be noted that this equation only holds if the input signal is kept constant. If the hit is still arriving when the comparator takes its measurement, the equation will become dependent on the parasitic capacitance. A full derivation of this situation is given in Appendix A.2.

Although the reality will be slightly different, Equation 4.3 gives a good approximation for designing. The conclusion that can be drawn to maximize the pre-amplifier gain are:

- **Limit the current going through the input pair by sizing M3.** This pushes the input pair into weak inversion while the comparison is happening. In this region, they will have the maximum g_m/I_d, which optimizes the pre-amplifier gain.
- **Place threshold of the M6/M8 and M7/M9 inverters close to GND.** This also increases the pre-amplifier gain, as the signal will get integrated on the Di nodes for longer.

Although both these methods increase the pre-amplifier gain, they also reduce the speed of the comparison. As the final comparator should operate at 800 MHz, the amount of gain that can be obtained by the pre-amplifier will be limited.

4.1.3 Noise

Dynamic comparators do not have a steady-state operating point. This means that standard noise analysis is not possible as all the transistors change their operating region during operation. Although an AC noise analysis is not possible, a time-domain noise analysis can still be done. An example of such an analysis is done in [23]. Here stochastic calculus is used to obtain a final expression from the noise. Although the comparator used in [23] is different from the one shown in Figure 4.2, the same conclusions are still applicable. The overdrive voltage of the input pair should be minimized, 3 examples are given on how to achieve this:

- **Increase the W/L ratio of the input transistors.** Although this would decrease the noise, this also increases the input capacitance of the comparator. This in turn will lower the signal amplitude, which makes this solution undesirable.
- **Decrease the discharging current by adjusting the size of M3.** The current through the input pair is limited by the tail transistor M3. By decreasing its W/L ratio, the noise of the pre-amplifier can effectively be reduced.
- **Decrease the input common-mode voltage V_{CM}.** This has a similar effect to the previous point, where the current will be limited. This technique can also be used to reduce the noise.

In conclusion, the primary noise reduction technique that will be implemented is to adjust the size of M3 and the value of V_{CM}, to ensure a low current will flow through M1/M2. This will in turn lower the speed of the comparator, so there is a trade-off to be made.

4.1.4 Power consumption

The power consumption of the comparator is dependent on the amount of parasitics that need to be charged and discharged every comparison. The largest of these capacitors is located on the output and the Di nodes. A rough estimate of the power consumption is given by:

$$P = f_{clk} \cdot V_{DD}^2 \cdot (2C_{Di} + 1.25C_{out}) \tag{4.4}$$

The factor 2 is there because of the 2 Di nodes that need to charge and discharge, while only a single output needs to fully charge and discharge. The other output reaches approximately $V_{DD}/2$, before going to GND again, resulting in the factor 1.25.

To minimize the power consumption, the main design strategy is to minimize the parasitics at the Di nodes.

4.1.5 Final circuit and simulation results

For the final comparator, the input common-mode V_{CM} is set at 600 mV. This value allows for more gain and less noise in the pre-amplifier, while still meeting all the speed requirements. The input pair is sized with a W/L of 4.8 µm/100 nm, to ensure the non-calibrated offset is not too large. It also ensures they have a higher g_m, which helps with the overall gain of the pre-amp. The resulting input capacitance of the comparator is equal to 3.29 fF The M6/M7 transistors are High Voltage Threshold (HVT) devices, while M8/M9 are Low Voltage Threshold (LVT) devices. This pushes the threshold of the top inverters close to GND, which also gives the pre-amplifier more gain. M10/M11 are also LVT devices, to ensure they can still pull the latch when the Di nodes have been dropped to $V_{inv,th}$.

First, the noise of the comparator is measured. To measure the noise of a dynamic comparator, ΔV_{in} is swept for small values around 0. For every value, the probability that the comparator gives a '1' is measured. The resulting curve of P(OUT = 1) vs. ΔV_{in} is an integrated normal distribution. This normal distribution has a mean that is equal to the offset of the comparator, and a standard deviation that is twice the amount of input-referred RMS-noise. The probability vs ΔV_{in} curve is shown in Figure 4.3. It shows both the schematic and post-layout results.

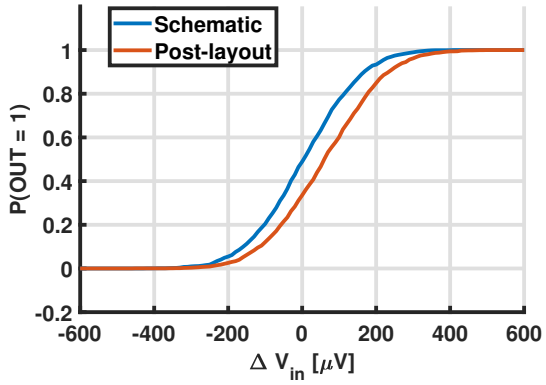

Fig. 4.3: Probability of a positive output for different values of ΔV_{in}

The final non-calibrated offset of the comparator had a standard deviation of around 5.6 mV. Equation 3.3 can also be used to see that the V_{th} mismatch on its own creates 4.0 mV of standard deviation in the offset. The additional offset is caused by other mismatches in the comparator. But the statement that most of the offset is caused by the V_{th} mismatch of the input pair is verified.

A final summary of all the simulation results of the dynamic comparator is shown in Table 4.1

Table 4.1: Dynamic comparator performance

Category	Schematic	Post-layout
Power consumption ($f_{clk} = 800\,\text{MHz}$)	36.0 µW	56.9 µW (+58%)
Energy per conversion	45.0 fJ/conversion	71.1 fJ/conversion (+58%)
Comparison delay ($\Delta V_{in} = 2\,\text{mV}$)	153 ps	240 ps (+57%)
Input referred noise	$1\sigma = 125\,\mu\text{V}$	$1\sigma = 140\,\mu\text{V}$ (+12%)
Offset	$\mu = 0\,\text{V}$, $1\sigma = 5.59\,\text{mV}$	$\mu = 163\,\mu\text{V}$, $1\sigma = 5.87\,\text{mV}$

4.2 Offset compensation

Miyahara originally also used a method of active offset compensation when he originally published his comparator design [22]. In Section 3.3 it was described how, for the case of the application in this work, active offset compensation is also required. The offset compensation technique used here will expand on the concept from Miyahara.

Before starting the design of the offset compensation, it is important to realize that some commonly used techniques for offset compensation in analog circuits are not suitable for this application. Some of the most commonly used techniques are Chopping and Auto-zeroing [24], but both of these techniques require linear amplifiers to operate correctly. Since the comparator has a digital output, the output cannot be used to determine the magnitude of the offset left, but just its polarity. Hence these techniques cannot be used in dynamic circuits.

In [22], the active offset compensation was implemented by an auxiliary input pair, this is illustrated in Figure 4.4. The voltage V_C^- on one side is kept fixed, while on the other side, the voltage V_C^+ is used to compensate for the offset. The voltage needed to compensate for the offset is determined during a calibration phase. During this phase, the voltage is linearly stepped by a charge pump that inserts charge into the storage capacitor C_C on the V_C^+ node. The charge pump inserts or removes charge based on the output sign of the comparator. An overview of example waveforms is shown in Figure 4.5.

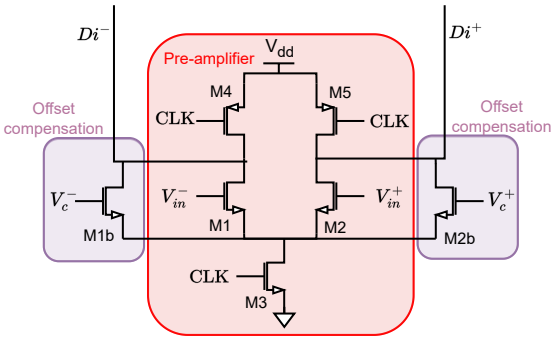

Fig. 4.4: Adjusted pre-amplifier with auxiliary input pair to allow for offset calibration

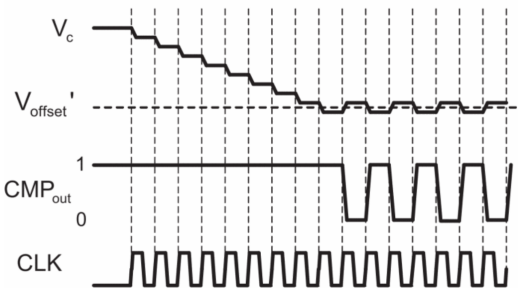

Fig. 4.5: Offset compensation technique used in [22]

After the calibration, both V_C voltages are kept constant. The post-calibrated comparators offset is limited to a maximum of one step of the charge pump. Ideally, the voltage on the capacitors remains there indefinitely. In practice, however, the compensation voltage slowly leaks away due to the gate leakage of M1b/M2b. This is why the storage capacitor is generally quite large, to ensure the compensation persists for longer.

4.2.1 Two-sided compensation

Initially, it might seem logical to only compensate a single side, as this only requires one big capacitor. It does, however, also reduce the compensation range, since one side is always fixed. If a two-sided compensation is used, there would need to be two big capacitors, but the maximum compensation range would also increase by at least a factor 2. The maximum compensation range is generally controlled by sizing the M1b/M2b transistors. If two-sided compensation is used, while the compensation transistors are reduced in size, the maximum compensation range does not change. If the M1b/M2b transistors are made smaller, their gate leakage also decreases. This will allow for a smaller capacitance required to hold the V_C voltage. Hence, the total area might not even change if the M1b/M2b transistors are sized accordingly. Whether the area is reduced or increased by two-sided compensation depends on the respective sizing of M1b/M2b compared to M1/M2.

Pre-amplifier gain

In addition to the potential area reduction, another advantage of two-sided compensation becomes evident when its impact on the pre-amplifier gain is considered. Adding the auxiliary input pair increases the amount of current draining the Di nodes by a fixed, non-signal-dependent amount. Because the Di nodes are now drained through these transistors as well, the common mode current I_{CM} from Equation 4.3 is increased. This reduces the gain in the pre-amplifier, and in turn increases the noise and offset of the comparator.

To prevent the additional transistors from degrading the performance of the comparator too much, the current flowing through them should be reduced as much as possible. In the case of two-sided compensation, not only is the size of the transistors reduced, which results in less total current flowing through them. The resulting compensation voltages V_C are also lower on average, since one side isn't always halfway on, but can instead remain completely off if needed.

4.2.2 Compensation speed

If the charge has leaked away too much, the comparator needs to be re-calibrated. During this time the system will be blind for any incoming signals. This time window is known beforehand, and it is possible to deactivate the Scanning Electron Microscope (SEM) during this period, or even better: for the re-calibration to be synchronized with the operation of the SEM. Still, the calibration window should preferably be as short as possible. In the case of using linear steps similar to [22], the maximum compensation time is given by:

$$T_{comp} = T_{clk} \cdot \frac{V_{comp,range}}{V_{comp,step}} \tag{4.5}$$

If the offset compensation needs to be done very precisely, $V_{comp,step}$ should be very low, and in turn, the calibration time becomes very large. A better solution would be to implement a binary search algorithm to find the offset. This would make the first step have a size of $V_{comp,range}/2$. Each step afterward has half the magnitude of the previous one. Using this method, the calibration time would be:

$$T_{comp} = T_{clk} \cdot \left\lceil \log_2 \left(\frac{V_{comp,range}}{V_{comp,step}} \right) \right\rceil \tag{4.6}$$

Although this is significantly lower than using linear steps, implementing binary scaled steps is quite a challenge, and instead decreasing step sizes are used. This is not as effective as using binary scaled steps but still reduces the calibration time significantly. Each time the output flips the step size can be decreased. To achieve this functionality two blocks are needed: A block that detects the swapping of the output sign, and a charge pump that has a lower step size each time the output sign swaps.

Output sign swap detector

To detect a swap in the sign of the output, the circuit in Figure 4.6 is used. Each time an output is high, it sets the value of its respective latch to '1'. If both latches are set to '1', meaning both outputs have been high before, the latches are reset and the output `swap` gives a short pulse. The simulation results of the circuit are shown in Figure 4.7.

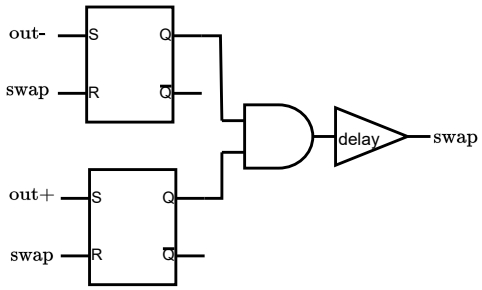

Fig. 4.6: Circuit used to detect swapping of the output sign

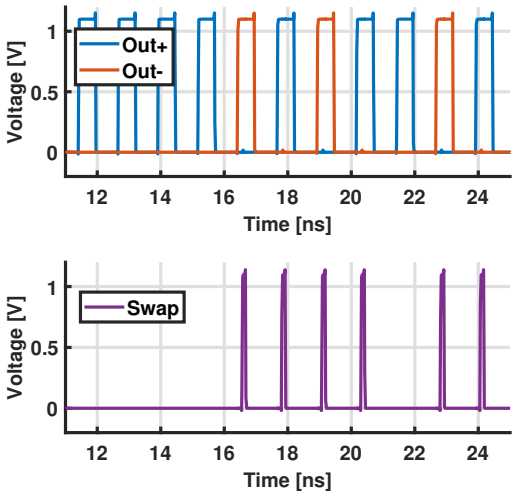

Fig. 4.7: Simulation results of the output swap detector circuit

Charge pump with decreasing step size

The charge pump places and removes charge into a storage capacitor to calibrate the offset. It needs to be able to add or remove charge based on the output of the comparator. This should only happen during the calibration, the calibration phase is indicated by the active high `calb` signal. When the system is working as intended, it should decrease the step size each time the swap signal goes high. The implementation of this functionality is shown in Figure 4.8. It only shows the charge pump for the V_C^+ side, for the V_C^- side, the signals `out+` and `out-` are swapped.

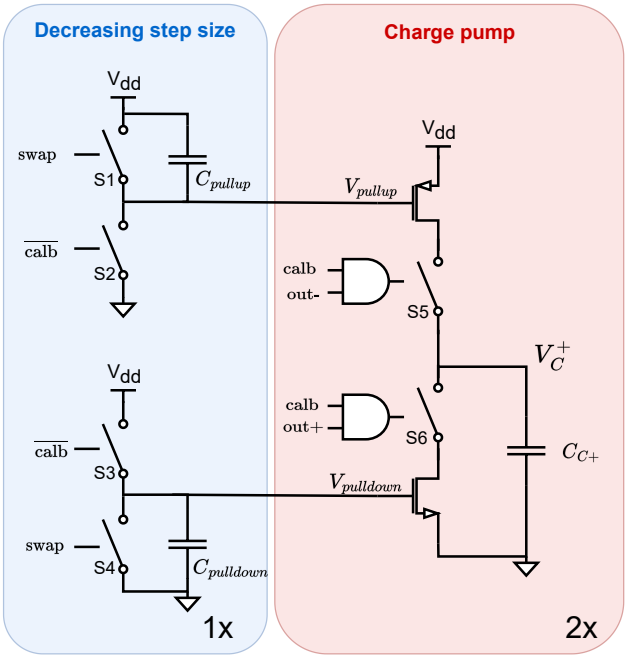

Fig. 4.8: Charge pump implementation

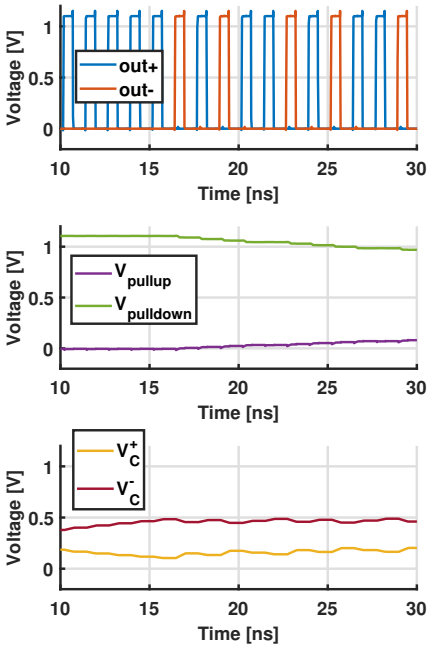

Fig. 4.9: Simulation results of the charge pump circuit with decreasing step size

Before the calibration starts, the signal `calb` is low, the voltages V_{pullup} and $V_{pulldown}$ are pulled to `VSS` and `VDD` respectively. During calibration, some charge is removed from the C_{pullup} and $C_{pulldown}$ capacitors each time the swap signal goes high. The lower charge on the capacitor decreases the V_{gs} of the current source/sink transistors. This lowers the current they allow through. Finally, some switches at the output are used to control the direction of the charge pump based on the output of the comparator. The simulation results are shown in Figure 4.9.

4.2.3 Maximum calibration range

The size of the M1b/M2b transistors, relative to the M1/M2 transistors determines the maximum offset that can be calibrated. The maximum calibration can be found by setting V_C^+ to `VDD` and V_C^- to `VSS` or vice versa. For the target application, it should be set sufficiently high such that the probability of all comparators falling within this range is high enough. As an example, if the maximum calibration range is set at 6x the standard deviation of the offset, $V_{calb,max} = 6{\cdot}\sigma(V_{offset})$, the probability of all 8000 pixels working would be 99.5%.

It is important to realize that not all offset is coming from the comparator. Other sources of offset are the mismatch in the reset switches and differences in C_{gd} of the input pair, resulting in a mismatch in the kickback of the comparator. The mismatch between C_D and C_{dummy} also results in a difference in kickback. An estimation of the total offset is $\sim 10\,\text{mV}$, which will be used to size the M1b/M2b transistors.

As this application is a proof of concept, the maximum calibration range is set quite high, at 330 mV, to ensure the concept of the system works. For the final application, the transistors M1b/M2b can be sized a factor 5 smaller, such that $V_{calb,max} = 6 \cdot \sigma(V_{offset})$. This means that also

for this proof of concept, the size of the storage capacitors will be quite large compared to the final version.

In the post-layout simulation, the offset compensation is able to reduce the offset of the dynamic comparator from $1\sigma = 5.59\,\text{mV}$ to $1\sigma = 172\,\mu\text{V}$.

4.2.4 Charge leakage

Another problem arises when the calibration mode is left on for too long. When this happens, the charge in the C_{pullup} and $C_{pulldown}$ capacitors will be completely removed because of all the swap signals. This means that the calibration mode is practically turned off. However, due to the leakage of the M1b/M2b transistors, the calibration will drift away. To ensure the system is calibrated after the `calb` signal becomes '0' again, the switches S2/S3 in Figure 4.8 are sized considerably larger than the switches S1/S4.

As a result, if the system remains in calibration mode for too long, the capacitors C_{pullup} and $C_{pulldown}$ will slowly be charged again because the leakage of the S2/S3 switches is higher than that of the S1/S4 switches. This means that the step size will increase again very slowly if the output remains with the same polarity.

4.3 Threshold generation

As mentioned in Section 3.4, the goal is to generate a charge on the detector with the opposite sign compared to the signal charge. This charge first needs to be removed by the incoming signal and will act as a threshold for the comparator. To generate the charge, either a current can be integrated over time, or a voltage can be converted into a charge using a capacitor.

Integrating a current If the charge is generated by a current source, both an accurate current and precise timing is needed. Since the charge should be generated after the detector has been reset and before the comparator starts its next comparison, the time window to generate the charge is very small. If $T_{reset} = 300\,\text{ps}$ and $T_{comp} = 350\,\text{ps}$, the time left for the charge generation is 600 ps. To make this short time window Process, Voltage, Temperature (PVT) resilient poses quite a challenge. Also, the switching of the current source will inject some switching noise into the system, which is directly added to the generated threshold. Hence integrating a current is not the preferred solution.

Converting voltage to charge To convert a voltage to a charge, a conversion through a capacitor is needed. The principle is illustrated in Figure 4.10. By stepping the voltage on the right by V_{step}, the detector voltage rises by:

$$V_{D,step} = V_{step} C_{dep} / (C_{dep} + C_D)$$

If $C_{dep} \ll C_D$,

$$V_{D,step} = V_{step} C_{dep} / C_D$$

$$Q_{D,step} = V_{step} C_{dep}$$

This ensures the amount of charge generated is independent of C_D.

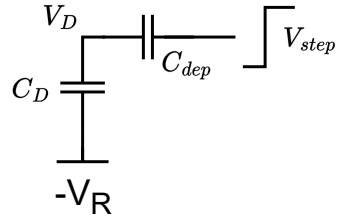

Fig. 4.10: Circuit diagram to convert voltage to charge

Although this type of threshold generation can happen very fast, there are some notable disadvantages. If it is required that $C_{dep} \ll C_D$, meaning C_{dep} should be in the order of a few fF, but still be very accurate. Although it can be challenging, capacitors with similar magnitudes have been made

before with success. In previous literature, 2 fF capacitors have been made with accuracies up to 0.43% in a 0.35 µm technology [25].

Furthermore the addition of C_{dep} will increase the equivalent capacitance at the input, which in turn lowers the signal amplitude. The final accuracy of the charge generation depends on the accuracy of the voltage step V_{step} and the depletion capacitor C_{dep}. The voltage step can be generated by stepping between `VSS` and `VDD` and using a capacitive divider for the desired step size. This will create a dependence on `VDD`, but as the power comes from an external power supply it is fairly constant. The main consideration is the ripple voltage, which can be reduced by decoupling caps and wide power traces near the threshold generation blocks.

4.3.1 C_{dep} design

The depletion capacitor should be designed with high accuracy, and at very small values. The capacitors with the least variance in a Monte Carlo simulation for this technology are MOSCAPs. MOSCAPs however, have a varying capacitance that depends on the applied voltages. If the applied step voltage V_{step} is kept small enough, the capacitance of the MOSCAP can be assumed constant. Their value can also change quite drastically over corners, but as this variation is constant for all pixels, it can be manually compensated for.

MOSCAPs also have a different capacitance, depending on from which terminal you look. To minimize the load on the detector, both situations are tested. In the case that the MOSCAP is connected with the gate to the detector, the load on the detector was minimized for the amount of threshold generated. Hence that configuration is chosen.

Since the detector voltage is known (V_D = 600 mV), the capacitance vs. the V_{step} voltage can be plotted to determine the best operating region. The situation for a minimum size MOSFET is shown in Figure 4.11.
When V_{step} stays near `VDD`, the capacitance remains approximately constant. Therefore V_{step} voltage should preferably be biased near `VDD`. For the final implementation, an NMOSCAP is used of size 800 nm x 400 nm. This gives an additional load capacitance of 960 aF.

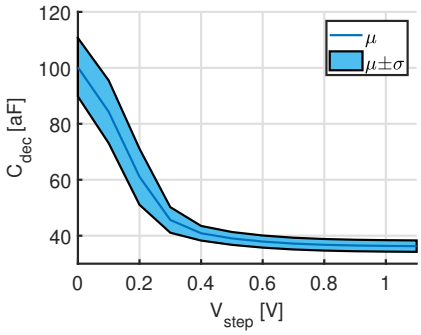

Fig. 4.11: Capacitance C_{dep} vs V_{step} voltage. The C_{dep} is implemented using a MOSFET with the source and drain shorted together

4.3.2 Circuit design

To generate the small step and keep one terminal of the MOSCAP near `VDD`, the circuit in Figure 4.12 was used.

During the reset (`reset` = 1), the detector capacitance is pulled towards V_{bias}. If the Qth generation is enabled, $V_{step,big}$ will drop from `VDD` to `GND`. This step will also decrease the voltage V_{step} according to the capacitive divider. The voltage V_{step}, which was previously at `VDD`, will now be at `VDD` $- \Delta V$. Since V_{step} is also connected to V_D through C_{dep}, the V_D node will be pulled down slightly, but as the reset switch is closed it will quickly return to V_{bias}.

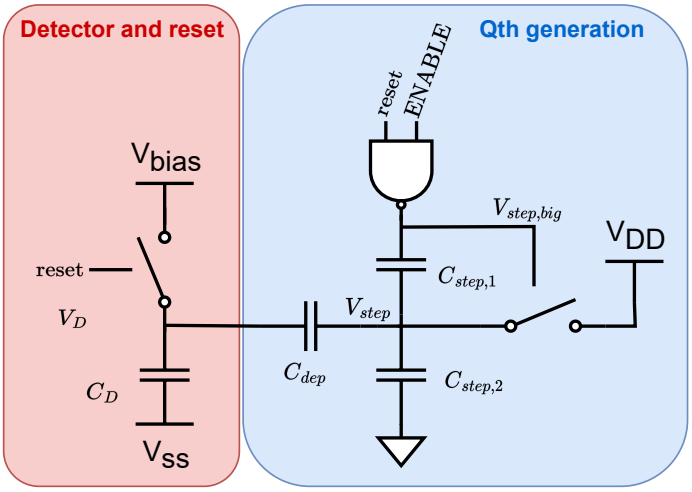

Fig. 4.12: The circuit used to generate a threshold charge on the detector capacitance.

When the reset is done, `reset` returns to 0. This pulls $V_{step,big}$ to `VDD` again, and closes the switch on the right, such that V_{step} is pulled towards `VDD`. Where V_{step} previously stepped down, it is now pulled to `VDD` again. This increase again translates to V_D through C_{dep}. However, as the reset switch is now turned off, the detector voltage will not be pulled towards V_{bias} again, but instead, the threshold charge will be added on top of the bias voltage. The waveforms are shown in Figure 4.13. First, the detector is reset without generating a threshold to measure the charge injected from the reset switch. Afterwards, the Qth generator is enabled and the threshold is added to the detector capacitance.

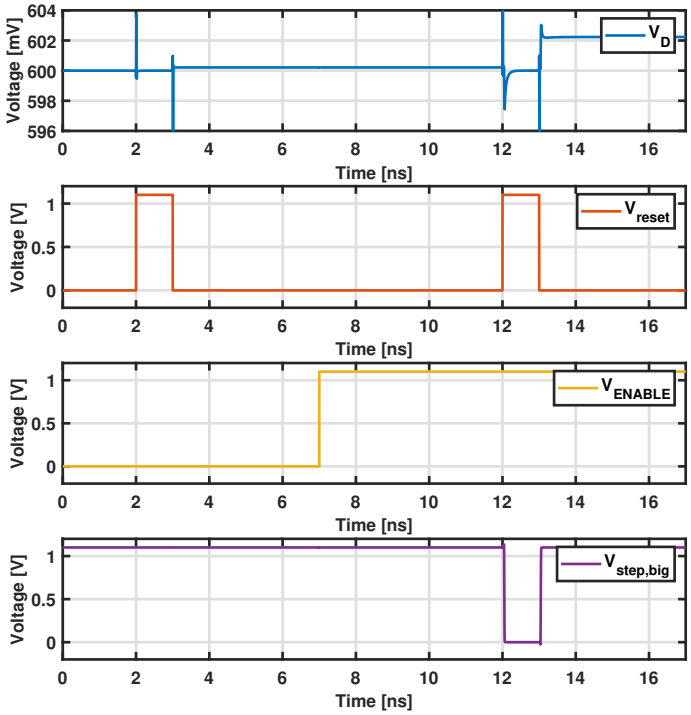

Fig. 4.13: Signal waveforms of the Qth generation block

To ensure the threshold charge can be selected, the value of $C_{step,2}$ is made adjustable using digital

logic. The subsequent values for the thresholds are shown in Figure 4.14.

The difference between the schematic and post-layout simulation results is mainly caused by the inaccurate modeling of the parasitics of the MOSCAP. When a post-layout extraction is done of just the MOSCAP, the capacitance is $\sim 20\%$ larger than in the schematic. This increased capacitance will result in a larger threshold generated.

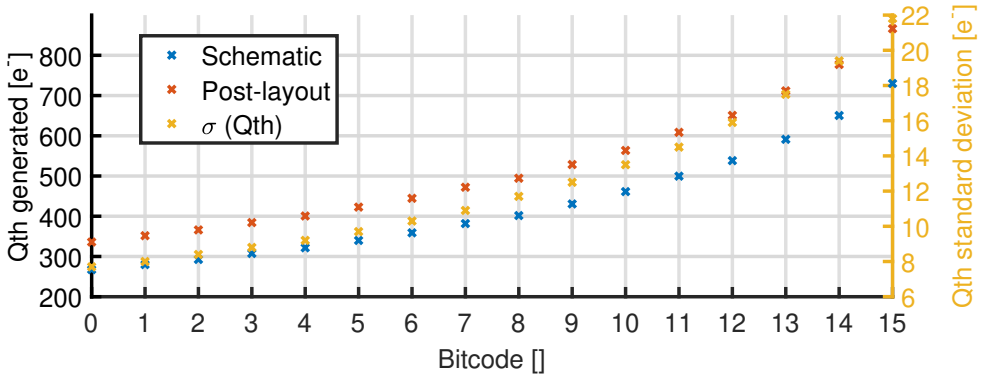

Fig. 4.14: Simulation results of the charge generated by the Qth generator. The charge generated is expressed as a number of electrons

The standard deviation of the Qth generator is shown in Figure 4.14. It can be seen that at a value of $500e^-$, the system is accurate with a σ of $12e^-$. It also remains quite constant for different values of C_D, varying only by $1e^-$ when C_D goes from 20 fF to 50 fF It does increase linearly for different temperatures, with a temperature coefficient of $0.272e^-/°C$.

4.3.3 Layout considerations

For the layout the capacitor C_{dep} is the most design critical. To minimize the parasitics, the connections of the MOSCAP are routed away in poly and n-type silicon, before going to metal 1. This minimizes the additional parasitic capacitance created by the metal traces. The entire MOSCAP is also placed within a guard ring to ensure it is sufficiently isolated from the p-substrate. Finally, some additional buffers are used to drive the capacitive divider.

4.4 Additional blocks

Besides the main components of the readout, some additional blocks are required for the full operation. In this section, the design of 3 additional blocks will be discussed.

4.4.1 Reset generation

The reset generator is used to generate a reset signal of programmable width. It is also required that the system will always reset when the system is in calibration mode. This is needed to ensure the input voltages of the comparator are equal, and the comparator is calibrated towards 0 offset. The circuit used for this is shown in Figure 4.15. Using a programmable delay line allows for the selection of the desired reset pulse width. The latch is designed in such a way that it gives a $\overline{\texttt{nreset}}$ = '1' output when both set and reset are '1'. This ensures that no matter how long the comparator gives an output, the reset pulse on the other end will have the same length.

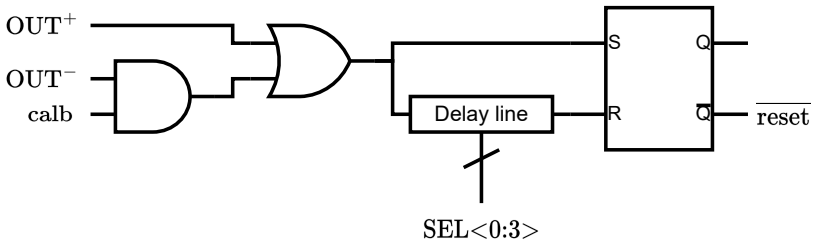

Fig. 4.15: Circuit diagram of the reset generator, the latch is designed such that it gives a $\overline{\texttt{nreset}}$ = '1' output whenever set and reset are both '1'

The post-layout simulation results of the circuit are shown in Figure 4.16 and 4.17.

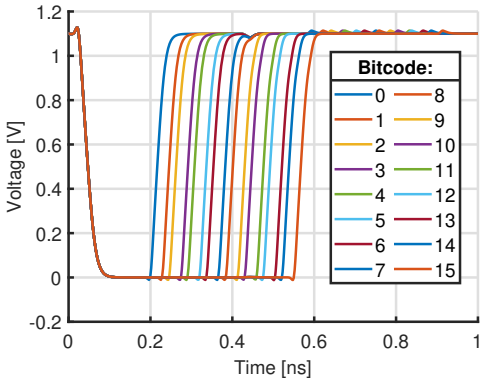

Fig. 4.16: The output waveform of the reset generator, $\overline{\texttt{nreset}}$

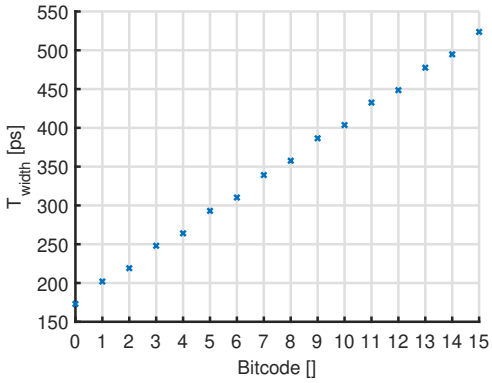

Fig. 4.17: Values for the different reset widths possible given an input bitcode

As can be seen, the reset network allows for precise control of the reset pulse width, and the system is invariant to the width of the input pulse `OUT+` or `OUT-`.

4.4.2 Asynchronous reset

A 800 MHz is necessary for the correct operation of the readout. However, only a 400 MHz CLK is available from the FPGA (The FPGA used for this project is the DE10-Standard development board with the Intel Cyclone® V SE 5CSXFC6D6F31C6N). To generate this frequency, the incoming clock, `CLK` of 400 MHz, is converted into $\texttt{CLK}_{\texttt{comp}}$ of 800 MHz using the circuit shown in Figure 4.18.

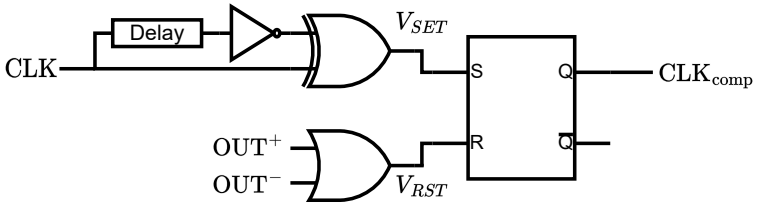

Fig. 4.18: Circuit used to asynchronously reset the comparator and generate a 800 MHz CLK

The top part of the circuit consists of an edge detector, which gives a short pulse, V_{SET}, whenever there is a rising or falling edge of the CLK. When an edge is detected, $\texttt{CLK}_{\texttt{comp}}$ is set to '1', and the comparator starts to compare its inputs. When either $\texttt{OUT}^+$ or $\texttt{OUT}^-$ becomes '1', the comparison is done and the comparator can be reset again. The value of $\texttt{CLK}_{\texttt{comp}}$ is set to '0' again using an OR-gate. This system ensures the comparator is only reset once it is done with its comparison and will not be reset prematurely. The resulting $\texttt{CLK}_{\texttt{comp}}$ will most likely not have a duty cycle of 50%, to ensure the comparator resets fast enough, the reset switches M4 and M5 from Figure 4.2 are sized relatively large. This ensures that the comparator will reset fast enough even if the comparison takes a bit longer.

The resulting waveforms are shown in Figure 4.19. The duty cycle of $\texttt{CLK}_{\texttt{comp}}$ is 21.0% for the schematic simulation and 30.3% for the post-layout simulation. The increase in duty cycle is mainly caused by the additional delay of the dynamic comparator, as mentioned in Table 4.1. The simulation is done with the dynamic comparator connected as well, to mimic the behavior in the final pixel.

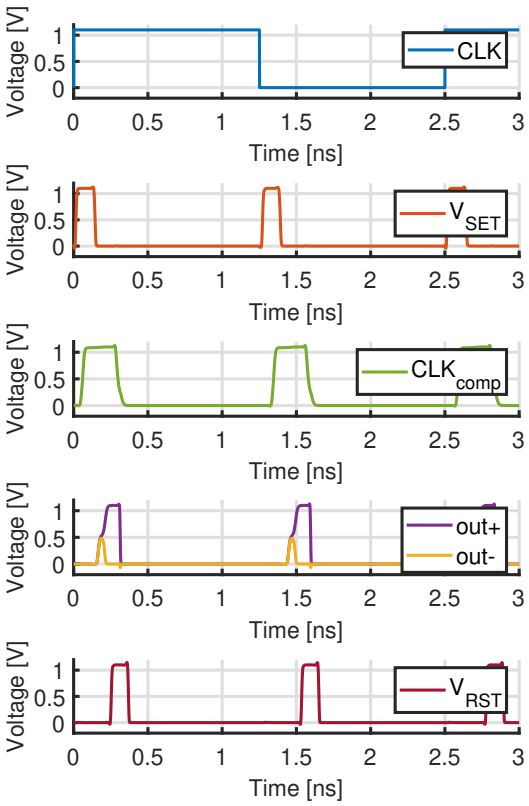

Fig. 4.19: Simulation results of the asynchronous reset circuit, simulated in combination with the dynamic comparator

4.4.3 Output buffer

The comparator gives an output stream which consists of short pulses on the $\texttt{OUT}^+$ and $\texttt{OUT}^-$ lines at a frequency of 800 MHz. However, the FPGA cannot detect these short pulses, so an intermediate buffer is used. The output buffer takes the signals $\texttt{OUT}^+$ and $\texttt{OUT}^-$, and gives 2 output lines which both have a frequency of 400 MHz. One is for the output of the comparator in the first phase in the CLK cycle and the other is for the output in the second phase of the CLK cycle. The circuit diagram is shown in Figure 4.20.

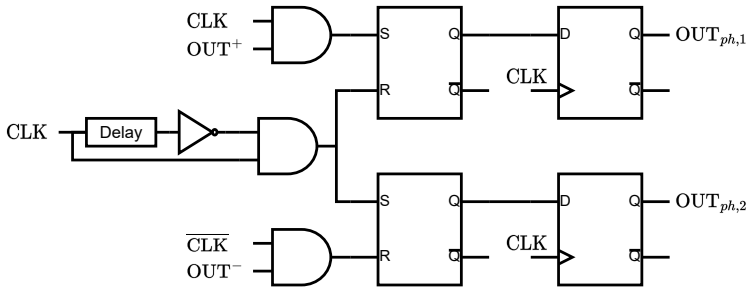

Fig. 4.20: Circuit diagram of the output buffer, there is a single clock cycle of delay between the input and the output of the buffer

The latches are reset to their base value on each rising edge of the CLK cycle. The top latch has a base value of '0', while the bottom latch has a base value of '1'. If, during the first phase of the CLK cycle (CLK = '1'), $\texttt{OUT}^+$ becomes high, the output of the top latch is set to '1'. For the bottom latch, the system works in reverse. If the $\texttt{OUT}^-$ becomes high during the second phase of the CLK cycle (CLK = '0'), the latch has its value set to '0'. At a new CLK cycle, both values are sampled onto the flipflops to ensure the width of each pulse is a single CLK cycle.

The simulation results are shown in Figure 4.21. Although all samples are now delayed with a CLK cycle, this error is predictable and can be corrected for when reconstructing an image for the SEM. The two outputs of the output buffer are both routed to separate inputs of the FPGA so they can be processed further. In a final system, both outputs from the latch can be combined using an OR gate to give a single output bitstream at 400 MHz. However, as this is a prototype, both outputs will be monitored for classification purposes.

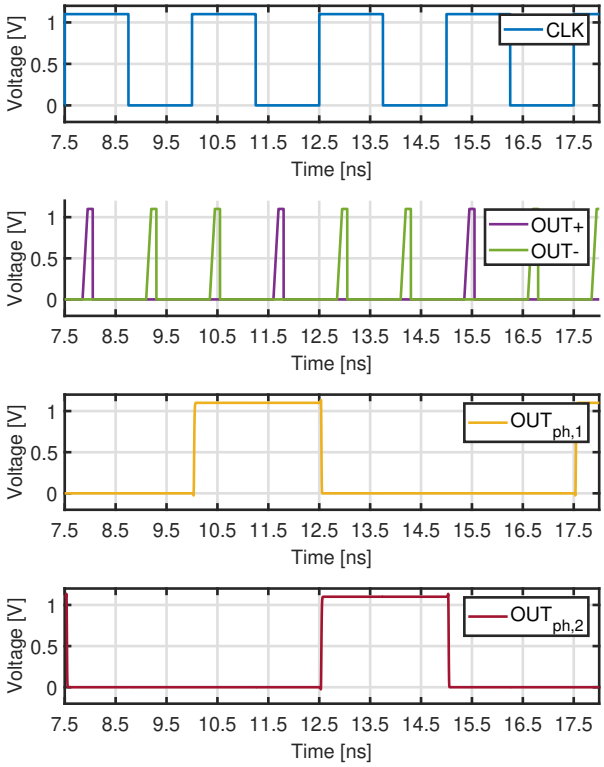

Fig. 4.21: Simulation results of the output buffer given every third output of the comparator is positive

4.5 Pixel overview

With all these blocks in place, the pixel is operational and can detect incoming signals. The complete functional block diagram of one pixel, as introduced in this chapter, is shown in Figure 4.22

To be able to qualify experimentally the performance of the readout circuit, several auxiliary blocks are required. The design of these blocks will be discussed in Chapter 5.

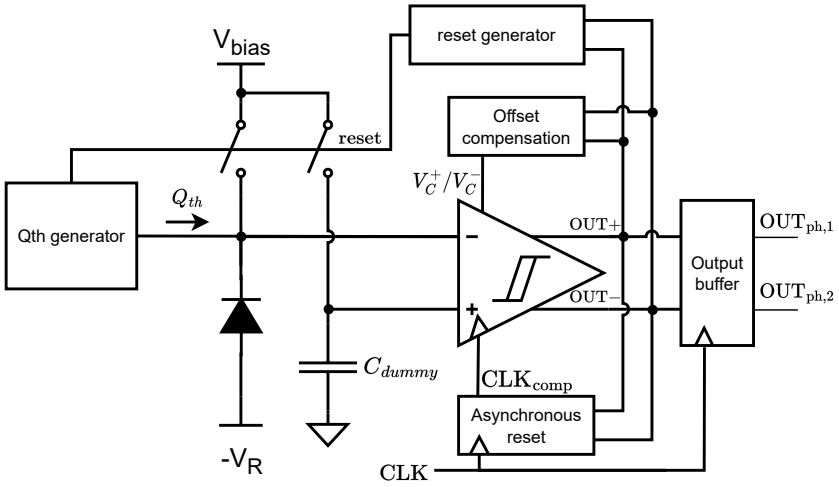

Fig. 4.22: Functional block diagram of the pixel

The pixel in operation will be tested with an ideal detector. The simulation results are shown in Figure 4.23. The current pulse generated by the detector representing an input signal is given by I_{gen}. The signal is drowned out underneath the kickback of the comparator, however, the kickback is common mode. The incoming signal is still visible in the differential part, $\Delta V_{in} = V_{dummy} - V_{det}$. This allows the comparator to ignore the kickback and still make the correct decision.

The outputs of the comparator are used by the output buffer to generate the $\texttt{OUT}_{\texttt{ph,1}}$ and $\texttt{OUT}_{\texttt{ph,2}}$ signals. The asynchronous reset also uses the outputs of the comparator to generate the $\texttt{CLK}_{\texttt{comp}}$ signal. The outputs of the comparator are also used by the reset generator to reset the voltages on the detector and dummy and generate a new threshold that is placed on the detector. The threshold can also be seen in the ΔV_{in} signal as the value lies at $\sim 2.5\,\text{mV}$ when no hits are arriving.

The first 100 ns of the simulation is used to calibrate the dynamic comparator. The values of V_C^+ and V_C^- are adjusted to ensure the comparator has 0 offset. At $t = 130\,\text{ns}$ the hits arrive in the pattern "1110 0011 0010" which repeats forever.

The system is tested and verified in all process corners, as well as over a temperature range of $0\,°\text{C} - 100\,°\text{C}$. To test the calibration the system is also verified using Monte-Carlo simulations. The CLK phase in which the hits arrived is also adjusted to verify the system's functions whenever a hit arrives. Lastly, the mismatch between the dummy and detector capacitance is also analyzed, and the system worked with a mismatch of $\pm 5\,\text{fF}$.

The final power consumption of a single pixel is 188 µW, which is an improvement on the current mode read-out circuits designed previously, which had a power consumption of 320 µW.

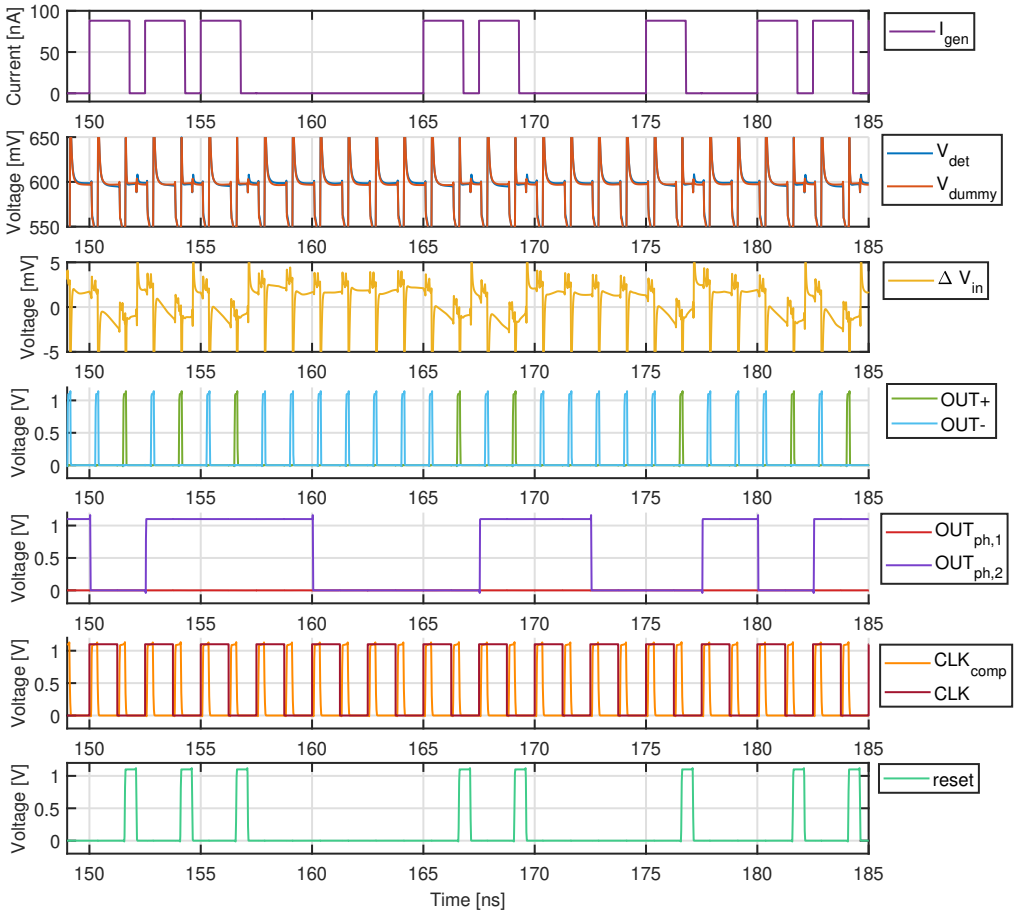

Fig. 4.23: Simulation results of a single pixel, using an ideal detector model

5. Design For Testability (DFT)

In addition to examining the comparator output, other individual parameters of the chip need to be measured to verify if the readout is working correctly. These parameters can also be used to determine any sources of error in the chip and classify its overall performance. A circuit that mimics the behavior of the detector is also required, as the actual detector is not available to be bonded to the chip for this thesis. This chapter will focus on all the project parts used to test the readout and its functionality.

5.1 Delay measurement

The delay of the comparator, as well as the width of the reset pulse, needs to be measured. These timings are quite short, in the order of a few hundred ps, which makes them not measurable on an external oscilloscope. These signals should be measured internally and converted to a readable output for the external scope. To do this, the delay measurement block is designed.

5.1.1 PWM delay measurement

Both the comparator's delay and the reset pulse's width are assumed to be constant over a long period of time if given the same input conditions. This means that repeated measurements can be used to obtain a more accurate value. The method used is to first convert the delay of the comparator into a pulse with a width equal to the delay using digital logic ($\texttt{CLK}_{\texttt{comp}} \cdot \overline{\texttt{RST}_{\texttt{det}}}$). This pulse is generated every CLK cycle. The average voltage of this signal is now equal to the average time the pulse is on. To obtain this average a low-pass RC filter is used. The schematic is shown in Figure 5.1.

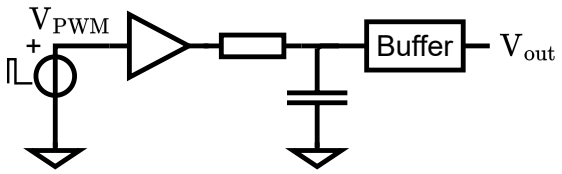

Fig. 5.1: The circuit used for measuring the delay of the comparator and reset width

The voltage V_{PWM} is the signal to be measured. In the final system, a control signal allows for a selection to be made. The V_{PWM} can either be set to $\texttt{CLK}_{\texttt{comp}} \cdot \overline{\texttt{RST}_{\texttt{det}}}$ or $\texttt{RST}_{\texttt{det}}$, allowing for both the measurement of comparator delay, as well as the measurement of reset width.

If the ripple created by the RC filter is neglected, the voltage V_{out} is defined by:

$$V_{out} = V_{DD} \cdot \frac{T_{pulse}}{T_{CLK_{comp}}} \tag{5.1}$$

Using Equation 5.1, a variation of 10 ps would result in a variation of 8.8 mV. Which can quite accurately be measured using a simple multimeter. It should be noted that more accurate Time to Digital Converters (TDCs) can be made in 40 nm technology [26] [27], but this solution was chosen due to its simplicity to implement. In the design of the digital buffer on the left of Figure 5.1, a fan-out of 2 was chosen. This allows for sharp rise and fall timings, which minimally distort the digital signal. The total delay is not important as the signal gets filtered to DC afterward.

5.1.2 Buffer design

An output buffer driving the pad is required in order to prevent distortion. This buffer should have quite a large input voltage range and output voltage range because the signal from the RC filter can vary from `VSS` for $T_{pulse} = 0\,\text{ns}$ to `VDD` for $T_{pulse} = 1.25\,\text{ns}$. Such a buffer is very hard to design; instead, a different approach will be used. Instead, the amplitude will be reduced by placing additional resistors at the output going to V_{DD} and V_{SS}. This will lower the signal amplitude, while still keeping the range in the middle of the voltage range. If both resistors have a value double that of the previous resistor, the output voltage will vary between $V_{DD}/4$ and $3V_{DD}/4$. This range is easier to design for. Both these new schematics can be seen in Figure 5.3 and 5.4. The amplifier used is a folded cascode with both PMOS and NMOS input pair to improve the common mode range. The error resulting due to the non-idealities of the buffer are shown in Figure 5.2. The errors are mainly caused due to the limited gain of the amplifier at these input voltages.

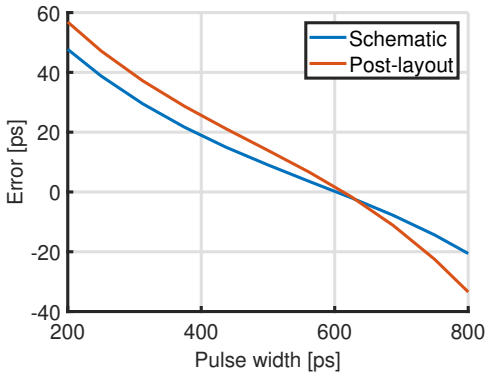

Fig. 5.2: Error of the pulse width measurement after the final buffer

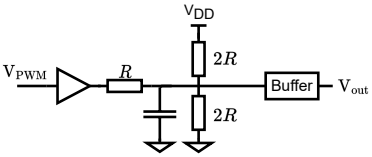

Fig. 5.3: Adjusted schematic for the delay measurement

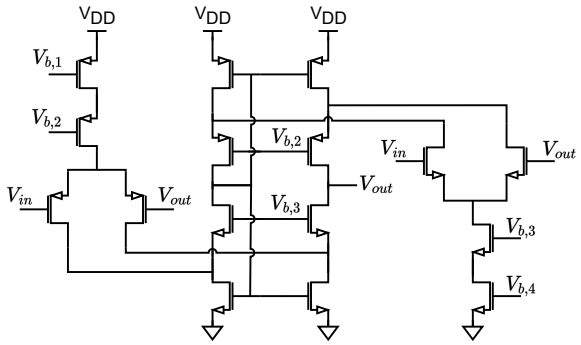

Fig. 5.4: Circuit used for the delay measurement buffer

5.2 Offset and noise

To measure the noise and offset coming from the comparator and the reset switches, a small differential input needs to be applied to the input of the comparator.

5.2.1 ΔV_{in} generator design

Since the required differential signal is in the order of tens of µV, an external supply is insufficiently accurate. To generate the differential signal, internal circuitry is used. The diagram of the circuit used is shown in Figure 5.6. The configuration used is a resistive divider to obtain the approximate value of 600 mV for the common mode voltage of V_{ref}, and a Wheatstone bridge to generate the small differential signal. The resistor R_4 can be programmed to different values using digital control signals, to obtain different values for a differential signal. The final results are shown in Figure 5.5.

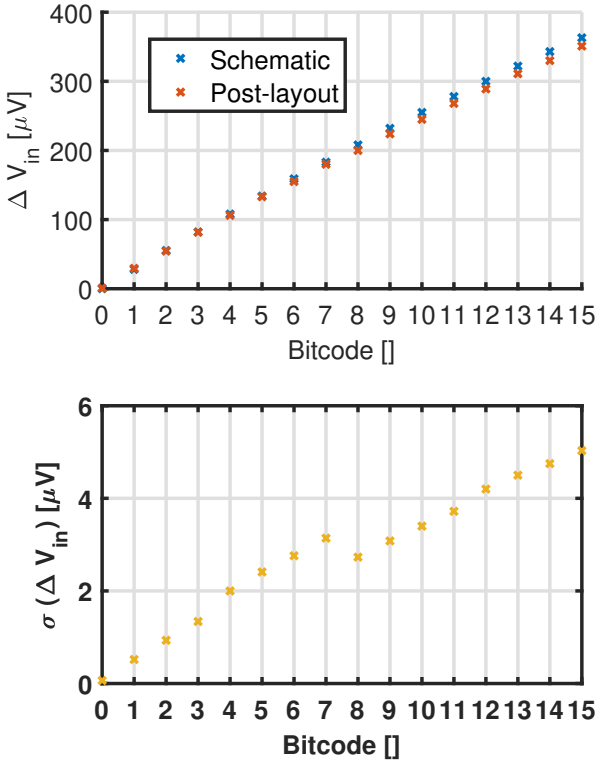

Fig. 5.5: Mean and standard deviation of the generated V_{ref}, for both schematic and post-layout simulation results

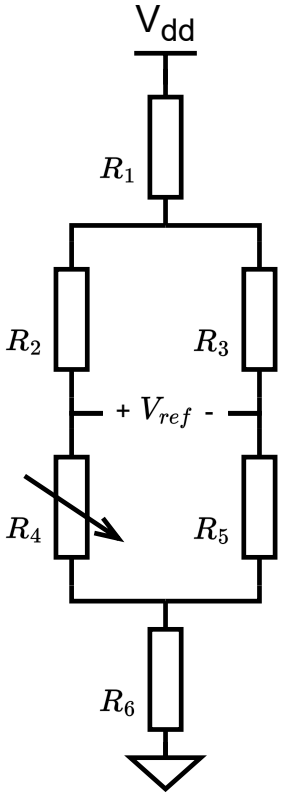

Fig. 5.6: The circuit used for the ΔV_{in} reference generator

5.2.2 Bias selection

To apply the small differential signal at the input, the voltages to which the detector and dummy capacitor are reset were modified. While calibrating, both signals should be linked to an identical reset voltage. However, for the subsequent measurements, they need to be connected to a differential voltage. This can be either the internal voltage reference or an external voltage reference. The internal reference requires to be able to be connected both ways around. To select between all the different options, a multiplexer is used as shown in Figure 5.7.

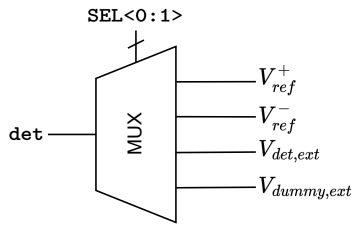

Fig. 5.7: The bias selection circuit is used to determine to which voltage the detector and dummy capacitor should reset

The `SEL` signal is generated based on 4 control signals, namely: `calb`, `int_ref`, `ext_ref` and `pol`. They are used to indicate if the system is calibrating, should use an internal reference an external reference and in which polarity the internal reference should be connected respectively.

Whenever `calb` = 1, both the detector and dummy capacitor are set to the same external bias $V_{det,ext}$. This ensures that during calibration the offset is always brought to 0. The signals `int_ref` and `ext_ref` are used to indicate if the internal or the external reference should be used after the calibration. In case both are 0, the same voltage is used for both the detector and dummy capacitor. Finally, when using the internal reference, the signal `pol` can be used to select the orientation of the internal reference. A truth table of all the connections is given in Table 5.1.

Table 5.1: Bias selection truth table

calb	int_ref	ext_ref	pol	det	dummy
0	0	0	0	$V_{det,ext}$	$V_{det,ext}$
0	0	0	1	$V_{det,ext}$	$V_{det,ext}$
0	0	1	0	$V_{det,ext}$	$V_{dummy,ext}$
0	0	1	1	$V_{det,ext}$	$V_{dummy,ext}$
0	1	0	0	V_{ref}^{+}	V_{ref}^{-}
0	1	0	1	V_{ref}^{-}	V_{ref}^{+}
0	1	1	0	$V_{det,ext}$	$V_{dummy,ext}$
0	1	1	1	$V_{det,ext}$	$V_{dummy,ext}$
1	0	0	0	$V_{det,ext}$	$V_{det,ext}$
1	0	0	1	$V_{det,ext}$	$V_{det,ext}$
1	0	1	0	$V_{det,ext}$	$V_{det,ext}$
1	0	1	1	$V_{det,ext}$	$V_{det,ext}$
1	1	0	0	$V_{det,ext}$	$V_{det,ext}$
1	1	0	1	$V_{det,ext}$	$V_{det,ext}$
1	1	1	0	$V_{det,ext}$	$V_{det,ext}$
1	1	1	1	$V_{det,ext}$	$V_{det,ext}$

5.3 Signal generation

To test the functionality of the system, the signal generated by the detector was replicated by some internal circuitry to mimic the detector's behavior. To do this, three different blocks were designed: A block to convert the rising edge of the trigger signal to a pulse with a specified width of $\sim 1.8\,\text{ns}$, a block to generate multiple pulses in short succession of each other, and a block to convert the digital voltage pulse into a current pulse with a programmable amplitude. All the blocks in this section have previously been designed by Alireza Mohammad Zaki, the daily supervisor of this project, and are not designed by the author of this thesis. Nevertheless, their functionality will briefly be described.

5.3.1 Trigger generator

This block generates a pulse of a pre-programmed length, the schematic overview is shown in Figure 5.8. It consists of a rising edge detector, with a programmable delay line to select the desired pulse width. An enable is added and buffers are placed inside the delay line to ensure adequate signal strength. The waveforms resulting from an input step are shown in Figure 5.9.

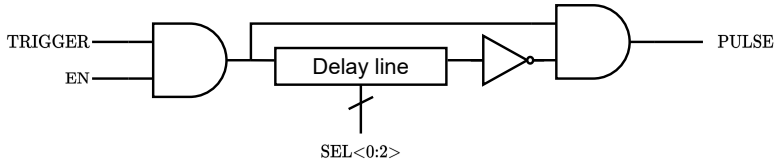

Fig. 5.8: Trigger generator schematic diagram

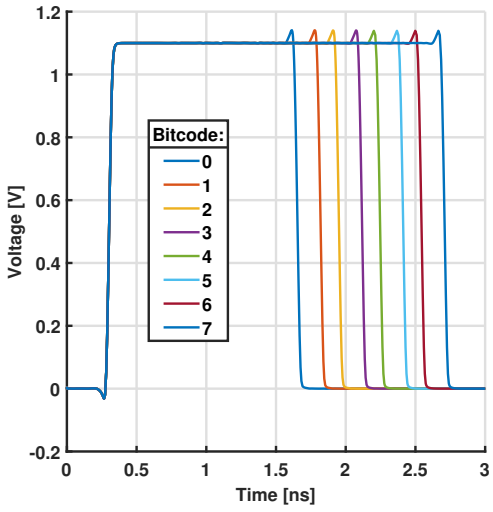

Fig. 5.9: Simulation results of the trigger generator circuit

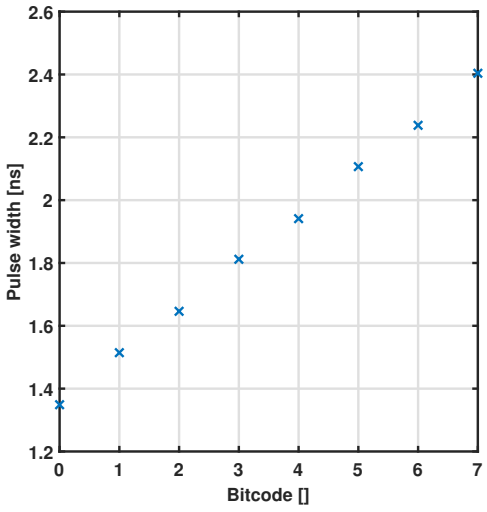

Fig. 5.10: The width of the trigger pulse vs. the input bitcode

5.3.2 Multiple pulse generator

The pulse width generator can only generate a pulse every other CLK cycle. However, in the real setup hits can arrive 2.5 ns spaced apart. To test the system under this condition the multiple pulse generator is used. It can convert the single pulse from the trigger generator into two or three pulses, with programmable spacing between them. The circuit used to achieve this is shown in Figure 5.11.

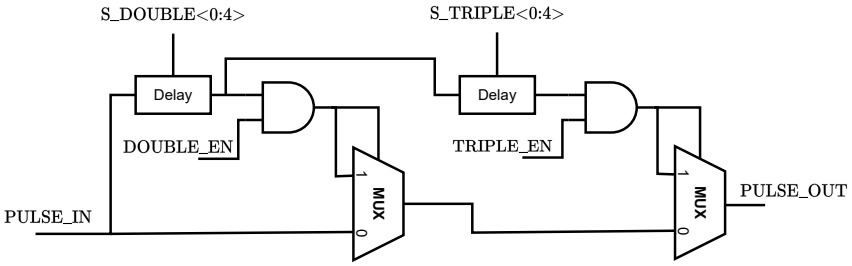

Fig. 5.11: Schematic diagram of the multiple pulse generator

The second pulse arrives after the first programmable delay block, and the third pulse arrives after both programmable delay blocks. Both the second and third pulse can be activated or deactivated independently using `DOUBLE_EN` and `TRIPLE_EN` respectively. An example simulated waveform is provided in Figure 5.12. Due to the time the MUX requires to turn on, each pulse shrinks slightly.

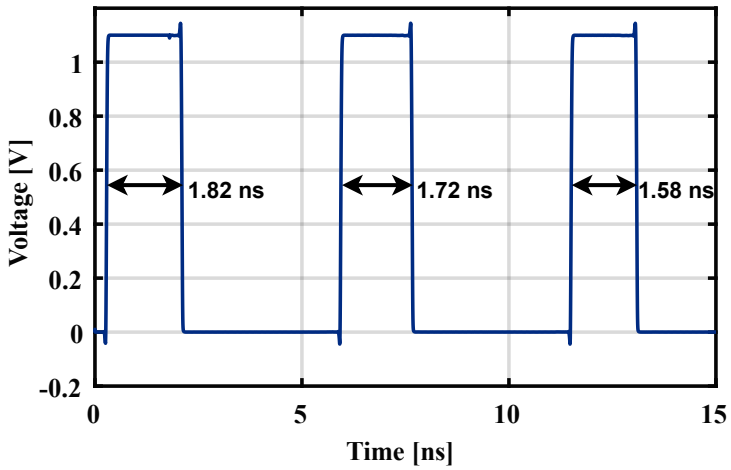

Fig. 5.12: The post-layout simulation results of the multiple pulse generator, `S_DOUBLE` and `S_TRIPLE` are both set to 15, the input pulse is 1.8 ns wide

5.3.3 Current DAC

The current DAC is able to mimic the current generated by the detector, which has a value of ~ 89 nA. This value is also made adjustable so different hits can be tested to monitor the response of the readout. As these step sizes need to be quite small (8.8 nA), they are generated a factor 10x larger. A current mirror is then used to divide the current by 10. Figure 5.13 shows a schematic overview of this. The simulation results can be seen in Table 5.2.

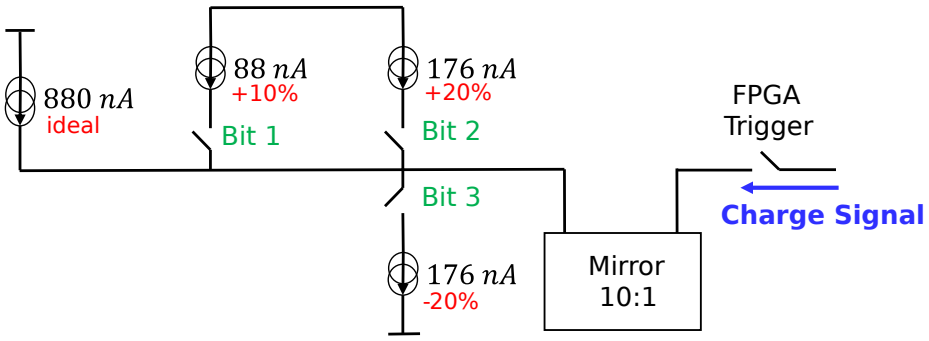

Fig. 5.13: High level diagram of the current DAC operation

Table 5.2: Simulation results of the current DAC

Amplitude	Target Current [nA]	Generated Current [nA]	Bit 1	Bit 2	Bit 3
Ideal − 20%	70.4	71.32	0	0	1
Ideal − 10%	79.2	79.2	1	0	1
Ideal	88	86.97	0	0	0
Ideal + 10%	96.8	95.14	1	0	0
Ideal + 20%	105.6	103.24	0	1	0
Ideal + 30%	114.4	111.3	1	1	0

5.4 Detector and dummy

The detector and dummy capacitor are the final on-chip components needed to test the system. Their main requirement is to have an accurate, adjustable value. To achieve this, MOSCAPs are used as they have a very accurate value when biased in the correct region.

To reset the voltages to the correct values, complementary switches are used. These switches minimize the amount of charge injection and CLK feedthrough. They do come at the cost of additional logic circuitry to generate the inverse control signal.

The final simulation results are shown in Figure 5.14. The step size is $\sim 6\,\text{fF}$, with a range of 10 fF - 100 fF. In the schematic simulation, the system is ideal so there is no difference between the detector and dummy capacitor. After the layout was done a difference in capacitance of at most 1 fF is observed. The increase in capacitance in the post-layout simulation is mainly due to the various parasitics present on the detector and dummy nodes.

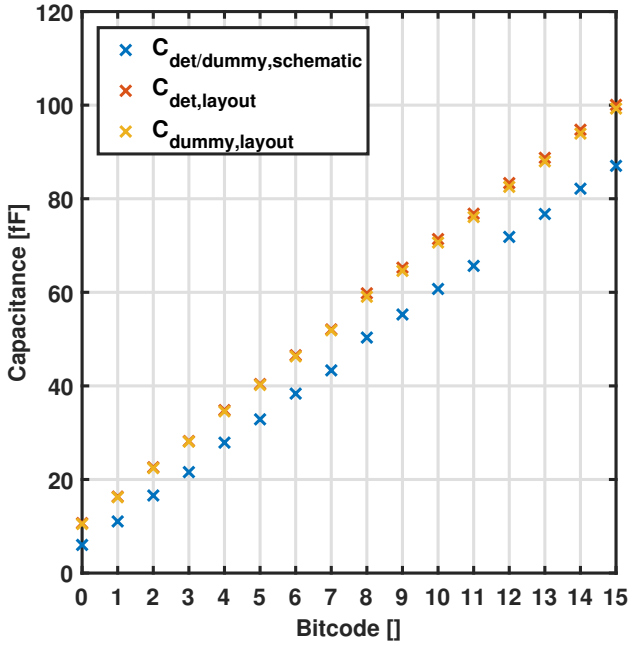

Fig. 5.14: Detector and dummy capacitance vs. the input bit-code

5.5 Power consumption

The total power consumption depends on whether a pixel is detecting incoming hits or is in calibration mode. The total power consumption of a pixel during detection is 343 µW and the power consumption of a pixel during calibration is 354 µW. Although these numbers are relatively high, they also include the power consumption from the signal generation blocks and the measurement blocks. Just the readout required 188 µW during detection and 198 µW during calibration. A full breakdown of the power consumption for both scenarios can be found in Appendix B.

5.6 Layout overview

With all blocks in place, the interconnects between them were made. Four different pixels were designed, each with a different value for the offset compensation capacitors C_C. The values are: 2 pF, 5 pF, 10 pF and 20 pF. For a final product a value of 2 pF would suffice, but for testing purposes, larger values were also tested and evaluated. The layout of the 2 pF pixel is shown in Figure 5.15.

The control signals are all the vertical traces, which are mostly placed in M4. The x-coordinates where the control signals enter and leave the pixel are aligned, such that multiple pixels can be stacked on top of each other. The main power traces are routed in M7. They are also aligned on the left and right of the pixel to allow for stacking of the pixels in the horizontal direction.

The total pixel uses an area of 80 µm x 98 µm, but it is important to realize that this also includes DFT blocks. When the chip is directly bonded to the detector, Blocks 1, 8, and 10 can be eliminated, resulting in approximately a 50% reduction in the area.

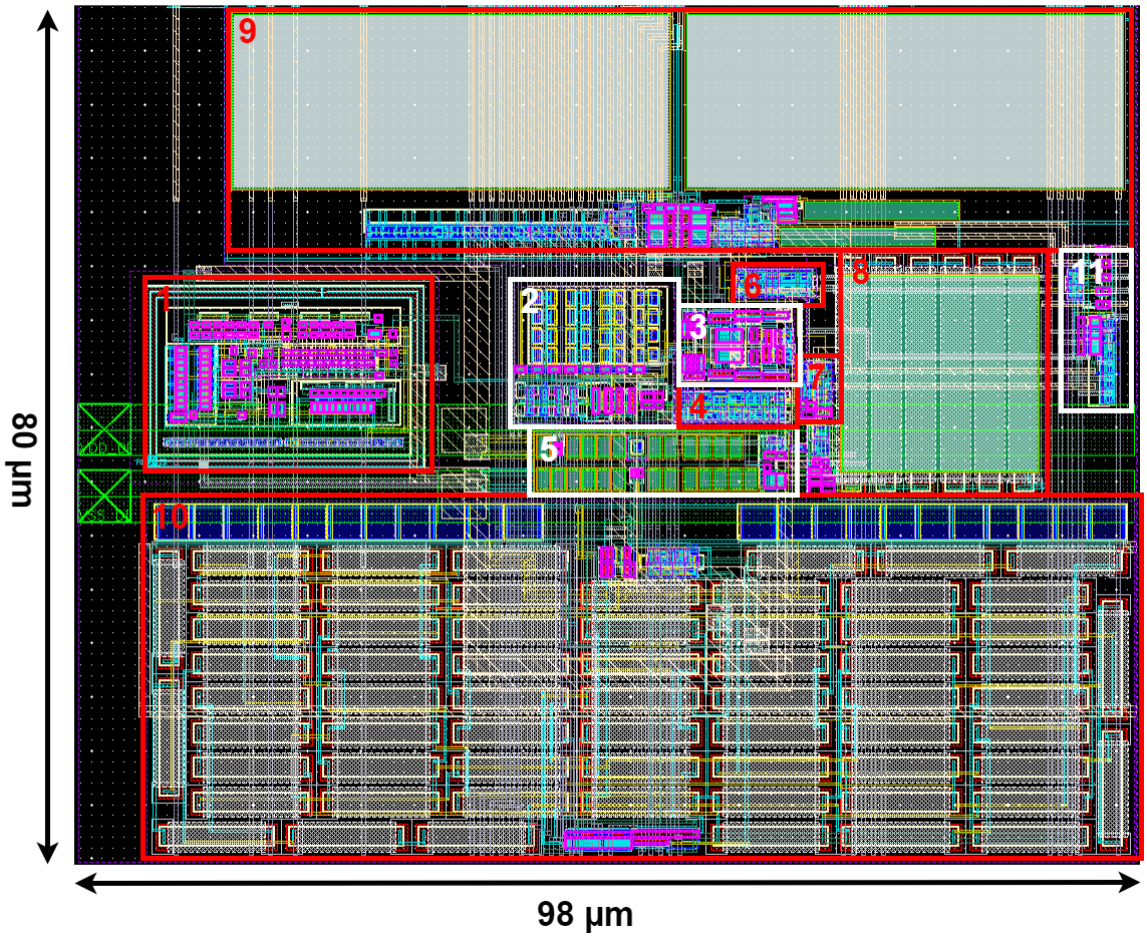

Fig. 5.15: Layout of the 2 pF pixel. 1. Current DAC, 2. Detector and dummy capacitor, 3. Dynamic comparator, 4. Reset generator, 5. Qth generator, 6. Output buffer, 7. Asynchronous reset, 8. Delay measurement, 9. Offset compensation, 10. ΔV_{in} reference and 11. `PIXEL_SEL` (will be elaborated on below)

A total of 12 pixels are placed in the final layout, 3 pixels for each value of C_C. All pixels are connected to the same bus wires through the `PIXEL_SEL` block. Four signals are used to select a pixel from the grid. Each pixel has its own address, when a pixel detects that the address requested is equal to its own, it connects all the inputs and outputs of the pixel to the bus wires. An overview of all 12 pixels and their interconnects is shown in Figure 5.16.

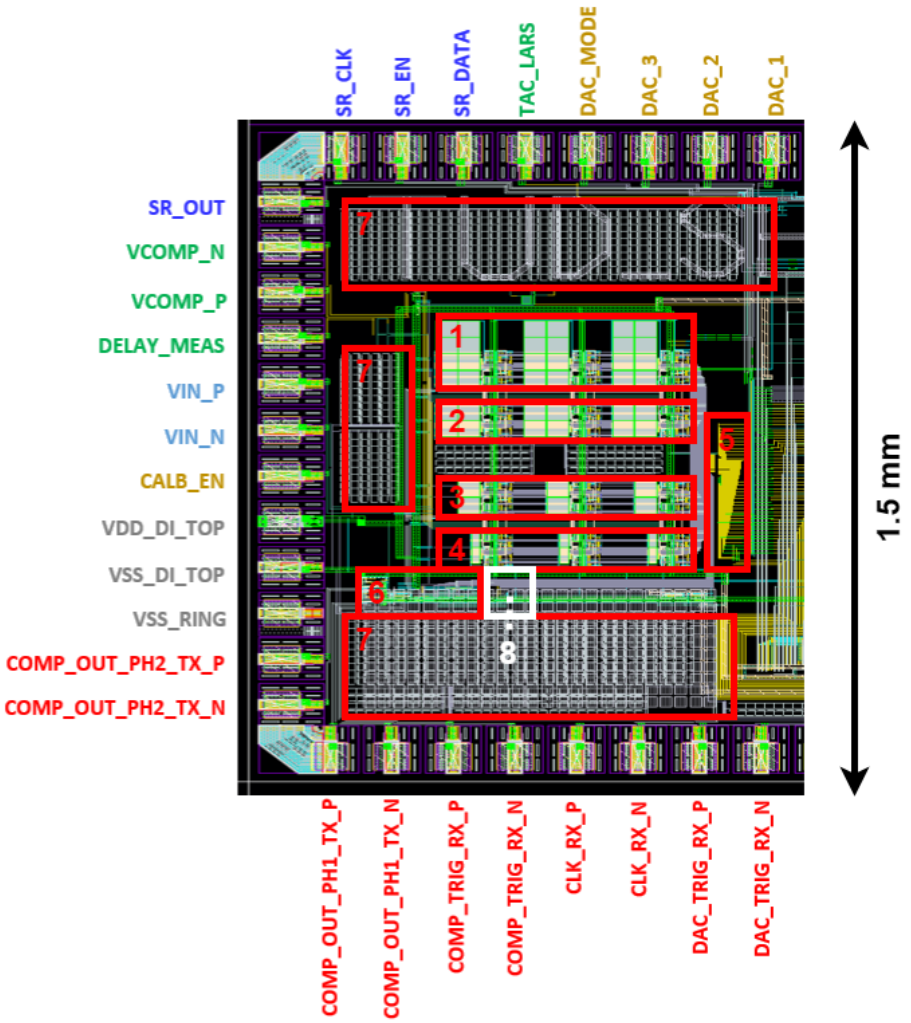

Fig. 5.16: Layout of all 12 pixels and additional blocks. The chip was shared with another project, and only the parts of the chip relevant to this project are shown. 1. 20 pF pixels, 2. 10 pF pixels, 3. 5 pF pixels, 4. 2 pF pixels, 5. Shift register, 6. Multiple pulse generator, 7. Decoupling capacitor and 8. Trigger generator

5.7 Measurement setup

To verify and quantify the performance of the final chip, the setup present off-chip is also important. The design of the FPGA code and PCB will be discussed in this section.

This project was combined with another project on the same chip. Hence some parts of the pad-ring and PCB design are not related to this project. Where applicable, the parts relevant to this project will be indicated in the figures.

5.7.1 FPGA code

The FPGA used in this project has to perform several tasks: First program the shift register with the correct settings, calibrate the system if required, send trigger pulses if required and lastly, read

back the outputs from the chip.

The different settings of the chip were made easily adjustable to make sure the FPGA does not need to be resynthesized every time something needs to be adjusted. To ensure ease of testing, the pixel to be tested is made selectable using switches on the FPGA. Furthermore, the FPGA also has switches that control the type of test to be performed. Based on the selection of the test different control signals are loaded onto the shift register. A list of all the different tests is given in Chapter 6.

For certain tests, a variable is swept to see the effects on the system performance. For this, a sweep variable is introduced. Based on the test selected the sweep variable controls a different control signal inside the chip. Some examples are the value of Q_{th} or T_{rst}.

An overview of the functionality of all the different buttons and displays is given in Figure 5.17.

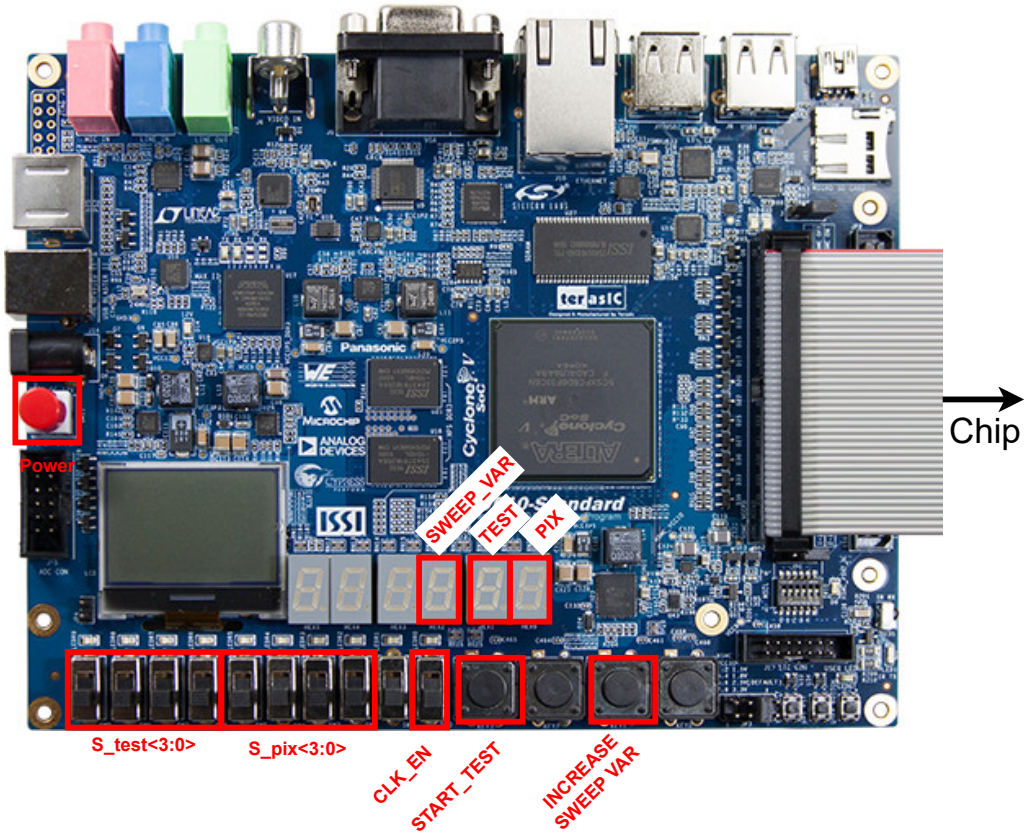

Fig. 5.17: Top view of the FPGA and the different functions of the buttons and displays

The FPGA was tested beforehand to ensure it works correctly. The outputs of the system are routed to the chip, as well as to a GPIO header pin. The GPIO pin was monitored on the oscilloscope to validate the programming, calibration and trigger worked as expected. The oscilloscope used for this project is the Tektronix MSO6B. The measured waveforms for the shift register programming are shown in Figure 5.18. The full FPGA code is given in Appendix C.

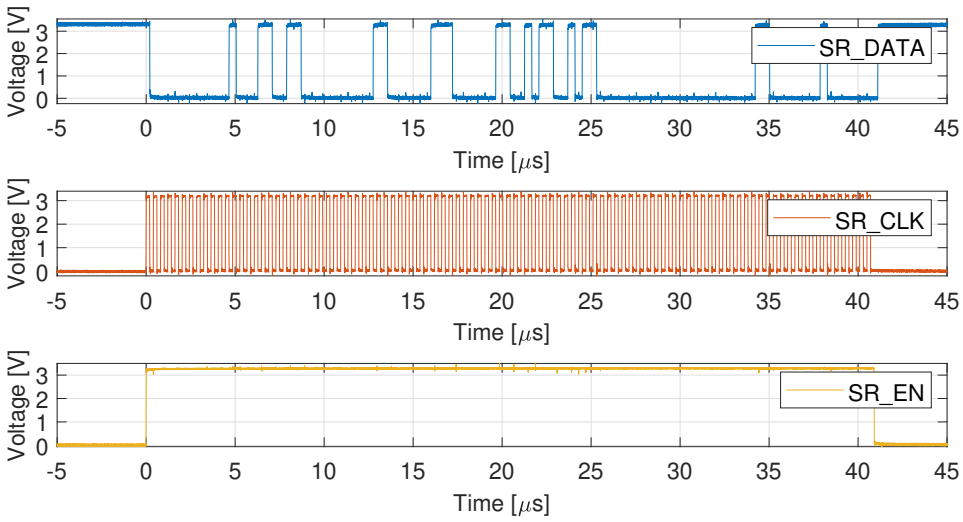

Fig. 5.18: SR programming bits generated by the FPGA. The signals are routed to GPIO pins which are monitored by the oscilloscope

5.7.2 PCB design and lab setup

The design of the PCB for this project was outsourced. The requirements for the PCB delivered to the external party will be discussed, as well as the lab setup used. A high-level overview of the PCB and lab setup is shown in Figure 5.19.

All digital signals that are operating at the CLK frequency of the FPGA ($f_{FPGA} = 400\,\text{MHz}$), are connected to the chip through LVDS connections. This ensures the signals are minimally distorted and can operate at the desired frequency. The signals that are connected through an LVDS connection are: `OUT_COMP_PH1`, `OUT_COMP_PH2`, `COMP_TRIG` and `CLK`.

The programming of the shift register only needs to be done at the start of the test and does not need to operate at 400 MHz. The `SR_CLK` operates at 5 MHz and hence does not use LVDS signaling.

The voltages used to compensate the dynamic comparator, V_C^+/V_C^-, are called `VCOMP_P` and `VCOMP_N` in Figure 5.19. These are given to an analog buffer and routed to an oscilloscope through SMA connectors. By observing these voltages the calibration time of the system can be measured.

The `DELAY_MEAS` signal is used to measure the reset width and the delay of the comparator, as described in Section 5.1. The signal `TAC_LARS` is similar to the `DELAY_MEAS` signal, but it is used to measure the width of the input trigger pulse. This allows for the verification of the performance of the trigger generator and consecutive pulse generator.

The biasing voltages of the detector and dummy capacitor are set by the voltages `VIN_P` and `VIN_N` respectively, which can be set using an external supply. Finally, all the connections to the FPGA are made through an HSMC connector cable. The signals from the FPGA are also buffered and isolated from the chip.

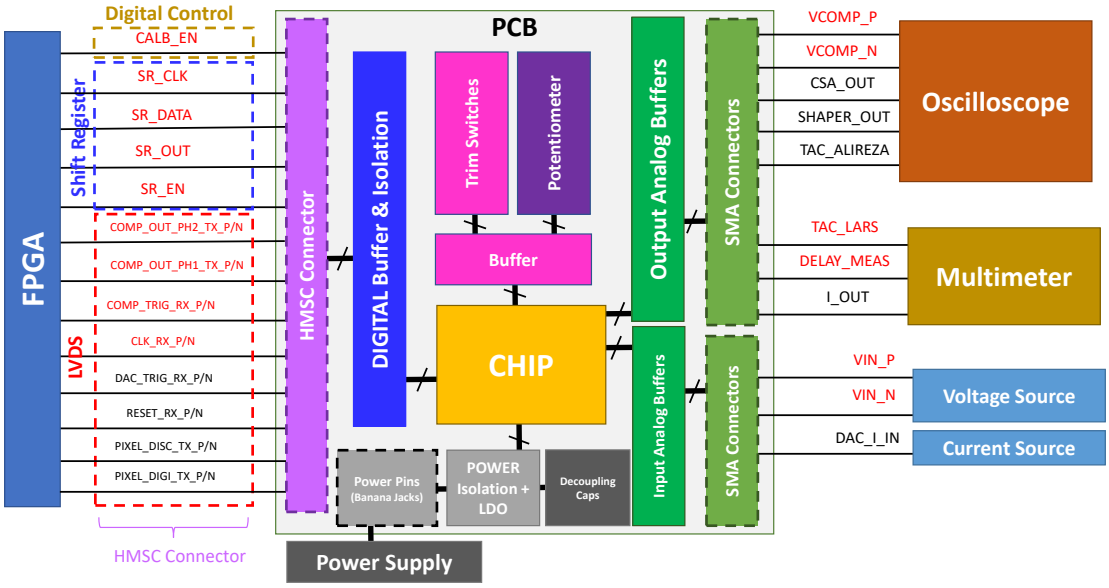

Fig. 5.19: High-level overview of the PCB structure. All the signals relevant to this project are marked red. The multimeter used is the Keithley 2002, and the voltage source used is the Keysight B2912B.

The chip itself is bonded directly onto a small PCB, which can be plugged into the main PCB for measurement. A picture of the PCB with a chip connected is shown in the figure below.

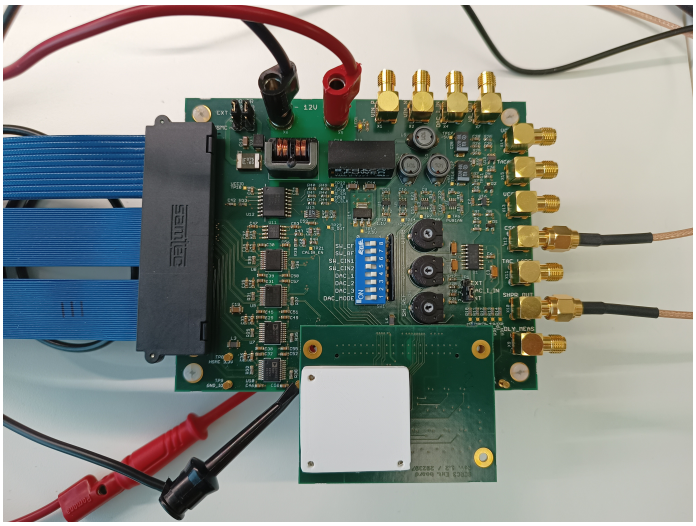

Fig. 5.20: Picture of the PCB with the chip connected. The white cap is used to protect the chip after bonding. The HSMC connector cable can be seen on the left.

With the entire measurement setup prepared. The measurements can be performed and compared with the simulated values to validate the chip performance.

6. Planned measurements

All the desired measurements of the chip are given their own test. The test to be performed is selectable on the FPGA, which in turn programs the shift register and sends the correct control signals to the chip. This chapter will provide a list of all tests to be performed. Unfortunately, due to delays in the chip delivery, none of the tests have been performed yet.

Test 0

Goal: Measuring the input-referred offset of the comparator without calibration.

Setup: The biasing voltage of the detector and dummy is set to use the external reference (voltage supplies). Calibration is turned off and no triggers are applied. The output of the comparator is monitored on the oscilloscope. When the output switches from positive to negative, the resulting differential voltage is measured using a multimeter.

Results: Due to delays in the chip delivery, the test could not be performed.

Conclusion: n/a

Test 1

Goal: Measure the delay of the dynamic comparator

Setup: The `CALB` signal from the FPGA is continuously pulled towards V_{DD}. The delay measurement block is set to measure the delay of the dynamic comparator. The voltage of the `DELAY_MEAS` signal is monitored using a multimeter. The voltage is converted into a delay using Equation 5.1.

Results: Due to delays in the chip delivery, the test could not be performed.

Conclusion: n/a

Test 2

Goal: Measure the width of the reset pulse.

Setup: The `CALB` signal from the FPGA is continuously pulled towards V_{DD}. This causes the reset to be applied every CLK cycle. The delay measurement block is set to measure the width of the reset pulse. The voltage of the `DELAY_MEAS` signal is monitored using a multimeter. The voltage is again converted into a delay using Equation 5.1.

Results: Due to delays in the chip delivery, the test could not be performed.

Conclusion: n/a

Test 3

Goal: Measure the input-referred offset of the comparator after calibration, using an external voltage supply.

Setup: The setup is similar to the one of TEST 0. The biasing voltage of the detector and dummy is set to use the external reference (voltage supplies). No trigger signals are applied, but the system is calibrated. The output of the comparator is monitored on the oscilloscope. When the output switches from positive to negative, the voltage difference between the two supplies is measured using a multimeter.

Results: Due to delays in the chip delivery, the test could not be performed.

Conclusion: n/a

Test 4/5

Goal: Measure the input-referred offset of the comparator after calibration, using the internal ΔV_{in} generator.

Setup: During calibration, the biasing voltages of the detector and dummy are set equal. When the calibration is over, the biasing voltages are switched to the ΔV_{in} generator. The output of the comparator is monitored on the oscilloscope, meanwhile, the sweep variable is used to adjust the voltage applied at the input of the comparator. When switching between TEST 4 and 5, the control signal `ref_pol` is set to '0' and '1' respectively. When the output of the comparator switches from positive to negative, the corresponding settings are noted.

Results: Due to delays in the chip delivery, the test could not be performed.

Conclusion: n/a

Test 6/7/8

Goal: Measure the performance of the chip for different values of the threshold.

Setup: First, the system is calibrated, afterwards the FPGA generates 4 trigger pulses, each 2.5 ns long and separated by 10 ns. The output of the readout is monitored to see if the input pulses are detected correctly. When switching between TEST 6, 7 and 8, 1 consecutive, 2 consecutive or 3 consecutive pulses are generated respectively.

Results: Due to delays in the chip delivery, the test could not be performed.

Conclusion: n/a

Test 9/10/11

Goal: Measure the performance of the chip for different values of the reset width.

Setup: This test is similar to test 6/7/8, but instead of varying the threshold the reset width is varied and the response of the readout is monitored. Similarly, when switching between TEST 9, 10 and 11, 1 consecutive, 2 consecutive or 3 consecutive pulses are generated respectively.

Results: Due to delays in the chip delivery, the test could not be performed.

Conclusion: n/a

Test 12/13/14

Goal: Measure the performance of the chip for different values of the detector capacitance.

Setup: This test is similar to test 6/7/8, but instead of varying the threshold both the detector and dummy capacitors are varied and the response of the readout is monitored. Similarly, when switching between TEST 12, 13 and 14, 1 consecutive, 2 consecutive or 3 consecutive pulses are generated respectively.

Results: Due to delays in the chip delivery, the test could not be performed.

Conclusion: n/a

Test 15

Goal: Measure the read-out system's dark count and the time the calibration voltages remain on the storage capacitors.

Setup: The system is calibrated and the output of the comparator is monitored on the oscilloscope. The time it takes for the comparator to give a false positive is measured to obtain an estimate for how frequently re-calibration is required. The voltages V_C^+/V_C^- are also monitored to see if the readout is able to calibrate itself within the estimated 100 ns.

Results: Due to delays in the chip delivery, the test could not be performed.

Conclusion: n/a

7. Conclusions

The primary goal of this project was to design a read-out circuit using voltage mode and evaluate its potential for increased power efficiency compared to current mode. In this thesis, the architecture design decisions, as well as the design decisions on the circuit level have been discussed. Based on the post-layout simulation results, it can be seen that the solution effectively reduces the power consumption per pixel to an impressive 188 µW during operation.

The chip has also been designed with verification and quantification tests in mind. Unfortunately, due to the delays in the shipment and production, the measurements have not been performed. Nevertheless, based on the post-layout simulation results, the new architecture appears to be a promising solution.

Summary of the main achievements

- A low noise, low power, fast dynamic comparator has been designed. In the post-layout simulation it consumed 56.9 µW at an operating frequency of 800 MHz. The input referred noise was only 140 µV while the input capacitance was kept at 3.29 fF.
- Offset compensation for the dynamic comparator was designed. It is successfully able to reduce the offset of the comparator from $1\sigma = 5.87\,\text{mV}$ to $1\sigma = 172\,\mu\text{V}$.
- To ensure the threshold generated is independent from the detector capacitance, a threshold charge was generated on the detector capacitance. A threshold of $500e^-$ could be generated with a standard deviation of just $12e^-$.
- All additional blocks were designed, and the total read-out system was verified in all process corners and for different temperatures. The final layout consists of 12 pixels, which can each be verified independently during measurements.

7.1 Future recommendations

Although the system obtained a higher power efficiency, several opportunities for improvement exist. A few suggestions for future enhancements are listed below:

Digitized offset compensation. Instead of storing the value of the offset compensation as a voltage on a capacitor, the value can also be stored as a digital number. The required number of bits would depend on the calibration range and required accuracy. Overcoming the challenge of achieving sufficiently small step sizes (around 50 µV) is crucial. Even the addition of a few hundred aF of additional capacitance at the comparator's output can shift the offset by more than the desired step size. Research into the feasibility still needs to be done, possibly drawing inspiration from approaches like the one presented in [25].

Dynamic logic. In the current system, a substantial amount of power is dissipated due to driving all the digital logic at 800 MHz. The power dissipation primarily arises from the charging and discharging of parasitic capacitances each CLK cycle. For the sake of this project, static logic is implemented for improved system reliability. However, future implementations could explore the use of dynamic logic to save power. Dynamic logic generally has fewer nodes in a circuit diagram, leading to reduced parasitic capacitances and lower power consumption.

Non-buffered delay measurement. To enhance the accuracy of the delay measurement, a possible improvement could be to remove the buffer and instead route the digitized signals to the pads. It might be needed to use LVDS in case the signals operate at high frequencies. This adjustment could significantly reduce the error in the delay measurement, as it overcomes the limited gain from the buffer.

A. Mathematical derivations

A.1 400 MHz sampling

Equation 3.1 gives the voltage removed in the worst-case scenario. The worst case is when the signal crosses the threshold exactly when the comparator makes its comparison, leaving the hit undetected. The hit will be detected in the next CLK cycle, but when resetting the detector voltage part of the subsequent hit will be deleted. The portion that is deleted is equal to the area of the green and orange blocks on the right in Figure A.1. As both the CLK frequency and $f_{hits,max}$ is equal to 400 MHz, the green triangle on the left and right are equal. The voltage removed by the first green triangle can easily be seen as:

$$V_{removed,green} = V_{th}$$

To determine how much voltage is removed by the orange block, the time it takes the comparator to detect a hit and reset the voltage is divided by the total time in which the signal arrives, $t_{transit}$. This fraction of time is equal to the fraction of the total signal removed. So that the signal removed is given by:

$$V_{removed,orange} = V_{sig} \cdot \frac{T_{rst} + T_{comparison}}{t_{transit}}$$

Summing both these parts gives back Equation 3.1:

$$V_{removed} = V_{th} + V_{sig} \cdot \frac{T_{rst} + T_{comparison}}{t_{transit}} \tag{A.1}$$

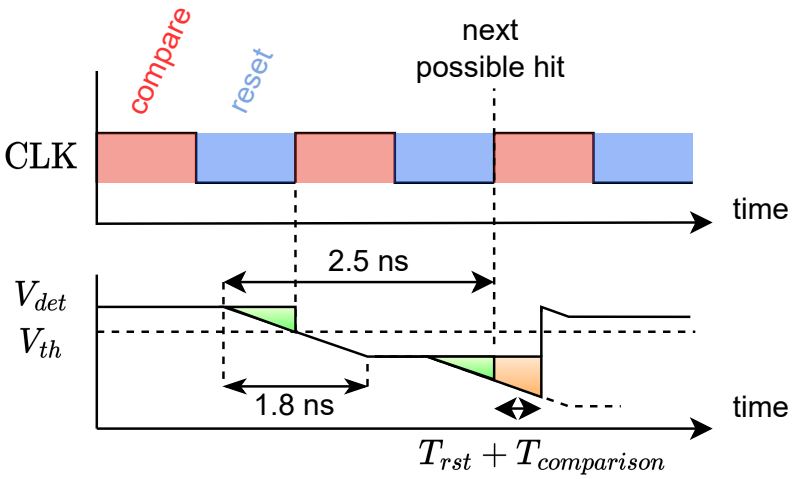

Fig. A.1: Worst case scenario of a signal crossing the threshold exactly when the comparison is made, requiring it to be detected in the next CLK cycle. $f_{clk} = 400$ MHz

A.2 Adjusted pre-amplifier gain

When the signal just starts to arrive, the voltage difference at the input of the comparator, ΔV_{in} does not remain constant. Instead it is given by:

$$\Delta V_{in}(t) = \frac{t}{t_{transit}} \cdot V_{sig} \tag{A.2}$$

Entering this equation into Equation 4.1 gives:

$$\Delta V_{Di}(t) = \frac{g_{m1,2} V_{sig}}{C_{Di} t_{transit}} \cdot t^2 \tag{A.3}$$

Again t is given by Equation 4.2, combining these equations gives:

$$\Delta V_{Di} = \frac{g_{m1,2} V_{sig}}{C_{Di} t_{transit}} \cdot C_{Di}^2 \cdot \frac{(V_{DD} - V_{th,inv})^2}{I_{cm}^2} \tag{A.4}$$

$$A_{pre-amp} = \frac{\Delta V_{Di}}{V_{sig}} = \frac{g_{m1,2}}{I_{cm}^2} \cdot \frac{(V_{DD} - V_{th,inv})^2}{C_{Di} t_{transit}} \tag{A.5}$$

As can be seen from Equation A.5, it is still important to maximize the g_m/I_D of the input pair. It becomes even more important to minimize the drain current, as it is now squared in the denominator of the equation. The importance of the threshold of the value of $V_{th,inv}$ is also increased, as it is also squared. Lastly, pre-amplifier gain is no longer independent of the parasitics on the Di nodes, but instead these should be minimized.

B. Power distribution

In the figures below the power consumption for a pixel in detection mode vs. a pixel in calibration mode is given. This is only the consumption when a pixel is selected. When a pixel is not selected the power consumption is 128 µW. This is primarily caused by the current DAC and the ΔV_{in} reference which do not turn off.

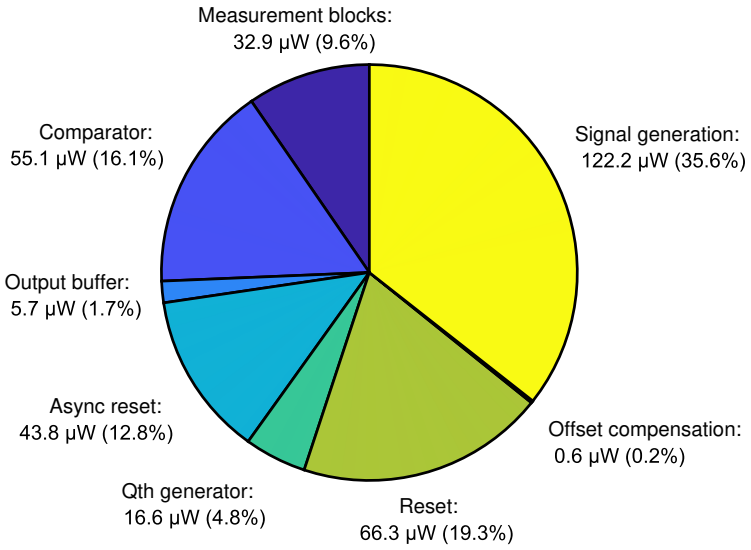

Fig. B.1: Power consumption of a single pixel during operation (1 hit every 5 ns), total power consumption is 343 µW

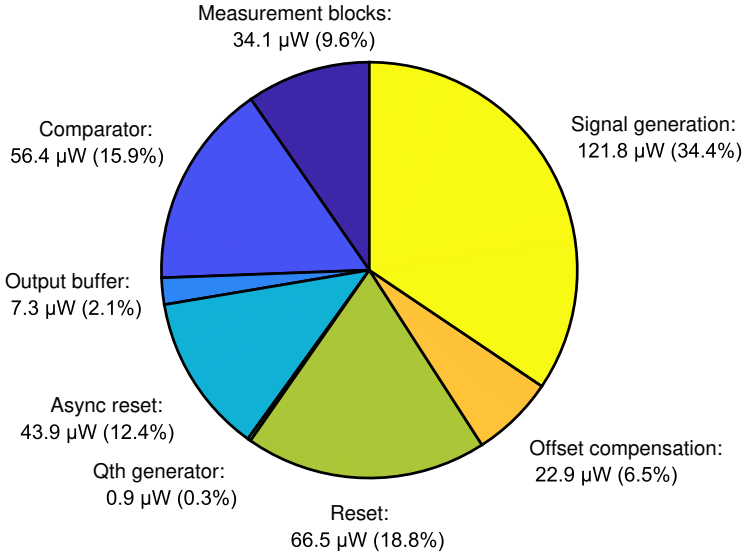

Fig. B.2: Power consumption of a single pixel during calibration, total power consumption is 354 µW

C. FPGA code

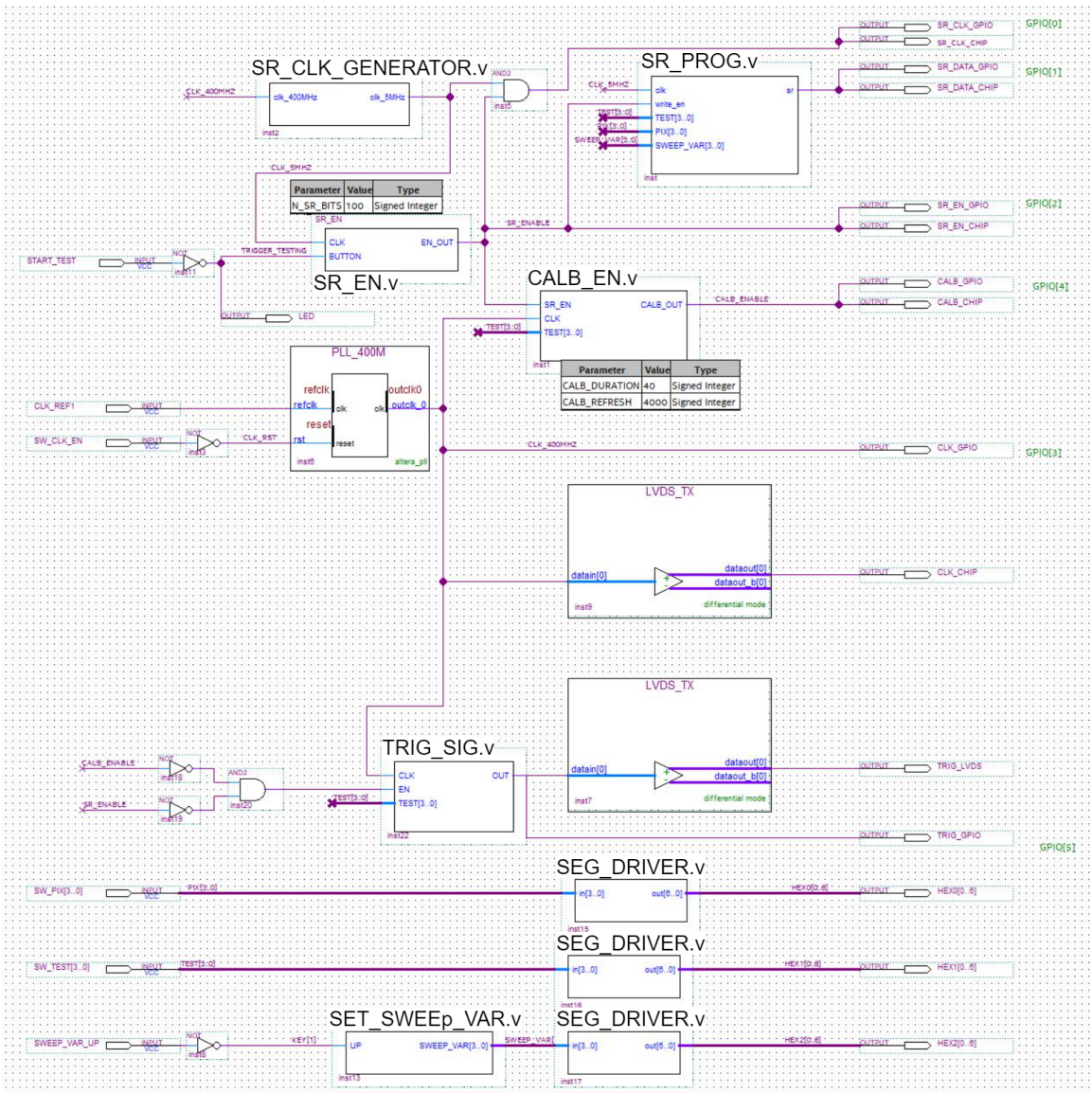

Fig. C.1: Overview of the top-level schematic used for programming the FPGA

```
module SR_EN
#(parameter N_SR_BITS = 100)
(

    input CLK, BUTTON,
    output reg EN_OUT

);

integer count;
reg BUTTON_PREV;

    initial begin

        count = 0;
        EN_OUT = 1'b0;
        BUTTON_PREV = 1;

    end

    always @(negedge CLK) begin
        if(BUTTON == 1'b1 && BUTTON_PREV == 1'b0) begin
            count = N_SR_BITS + 1;
        end else if (count > 0) begin
            count = count - 1;
        end

        BUTTON_PREV = BUTTON;
    end

    always @(count) begin
        if (count > 0) begin
            EN_OUT = 1'b1;
        end else begin
            EN_OUT = 1'b0;
        end
    end
endmodule
```

Fig. C.2: SR_EN.v

```
module SR_CLK_GENERATOR (
    input clk_400MHz,
    output reg clk_5MHz
);

    integer counter;

    initial begin
        counter = 0;
        clk_5MHz = 1'b0;
    end

    always @(posedge clk_400MHz) begin
        if (counter < 40)
            counter = counter + 1;
        else
            counter = 0;
    end

    always @(counter) begin
        if (counter < 80)
            clk_5MHz = 1'b1;
        else
            clk_5MHz = 1'b0;
    end
endmodule
```

Fig. C.3: SR_CLK_GENERATOR.v

```
// Shift register programming
module SR_PROG
(

    input clk, write_en,
    input [3:0] TEST,
    input [3:0] PIX,
    input [3:0] SWEEP_VAR,
    output reg sr

);


reg [99:0] trim_settings;
integer counter, negedge_first;

reg [3:0] S_Qth, S_dummy, S_det, S_rst, S_ref, S_pix;
reg ref_pol, int_ref, ext_ref, S_del_meas;
reg double_en, triple_en;
reg enable_all, enable_trig;
reg [2:0] S_pulse;
reg [4:0] S_double, S_triple;


    // Default settings
    initial begin
        trim_settings = {100{1'b0}};


        counter = 99;
        negedge_first = 0;
    end



    always @ (TEST, SWEEP_VAR, PIX) begin
        // Default values
        S_dummy = 4'b0011;
        S_det = 4'b0011;
        S_rst = 4'b0011;
        S_Qth = 4'b1011;
        S_ref = 4'b0000;
        ref_pol = 1'b0;
        int_ref = 1'b0;
        ext_ref = 1'b0;
        S_del_meas = 1'b0;
        S_pulse = 3'b011;
        S_double = 5'b00101;
        S_triple = 5'b00101;
        double_en = 1'b0;
        triple_en = 1'b0;
        S_pix = PIX;
        enable_all = 1'b1;
        enable_trig = 1'b1;

        // Based on the selection, change the SR bits
        case(TEST)
            4'b0000 : begin
                ext_ref = 1'b1;
            end
            4'b0001 : begin
                S_del_meas = 1'b1;
            end
```

```
64              4'b0010 : begin
65                  S_del_meas = 1'b0;
66              end
67              4'b0011 : begin
68                  ext_ref = 1'b1;
69              end
70              4'b0100 : begin
71                  ref_pol = 1'b0;
72                  int_ref = 1'b1;
73              end
74              4'b0101 : begin
75                  ref_pol = 1'b1;
76                  int_ref = 1'b1;
77              end
78              4'b0110 : begin
79                  S_Qth = SWEEP_VAR;
80              end
81              4'b0111 : begin
82                  double_en = 1'b1;
83                  S_Qth = SWEEP_VAR;
84              end
85              4'b1000 : begin
86                  double_en = 1'b1;
87                  triple_en = 1'b1;
88                  S_Qth = SWEEP_VAR;
89              end
90              4'b1001 : begin
91                  S_rst = SWEEP_VAR;
92                  S_del_meas = 1'b0;
93              end
94              4'b1010 : begin
95                  double_en = 1'b1;
96                  S_rst = SWEEP_VAR;
97                  S_del_meas = 1'b0;
98              end
99              4'b1011 : begin
100                 double_en = 1'b1;
101                 triple_en = 1'b1;
102                 S_rst = SWEEP_VAR;
103                 S_del_meas = 1'b0;
104             end
105             4'b1100 : begin
106                 S_det = SWEEP_VAR;
107                 S_dummy = SWEEP_VAR;
108             end
109             4'b1101 : begin
110                 double_en = 1'b1;
111                 S_det = SWEEP_VAR;
112                 S_dummy = SWEEP_VAR;
113             end
114             4'b1110 : begin
115                 double_en = 1'b1;
116                 triple_en = 1'b1;
117                 S_det = SWEEP_VAR;
118                 S_dummy = SWEEP_VAR;
119             end
120             4'b1111 : begin
121
122             end
123
124             default : begin
125
126             end
127         endcase
```

```
128
129     end
130
131     // Write the data to the SR
132     always @(negedge clk) begin
133
134         if (write_en == 1) begin
135             negedge_first = 1;
136             sr = trim_settings[counter];
137         end else begin
138             sr = 1'b1;
139             negedge_first = 0;
140         end
141     end
142
143     always @(posedge clk) begin
144
145         trim_settings[0]  = 1'b0; // Q1   //OVER_EN
146
147         trim_settings[1]  = 1'b0; // Q2   //SW_CLPF_1
148         trim_settings[2]  = 1'b0; // Q3   //SW_CLPF_2
149         trim_settings[3]  = 1'b0; // Q4   //SW_CLPF_3
150         trim_settings[4]  = 1'b0; // Q5   //SW_CLPF_4
151
152         trim_settings[5]  = 1'b0; // Q6   //PIX_SEL_1
153         trim_settings[6]  = 1'b1; // Q7   //PIX_SEL_2
154         trim_settings[7]  = 1'b0; // Q8   //PIX_SEL_3
155         trim_settings[8]  = 1'b0; // Q9   //PIX_SEL_4
156         trim_settings[9]  = 1'b0; // Q10  //PIX_SEL_5
157         trim_settings[10] = 1'b0; // Q11  //PIX_SEL_6
158         trim_settings[11] = 1'b0; // Q12  //PIX_SEL_7
159         trim_settings[12] = 1'b0; // Q13  //PIX_SEL_8
160         trim_settings[13] = 1'b0; // Q14  //PIX_SEL_9
161         trim_settings[14] = 1'b1; // Q15  //PIX_SEL_10
162         trim_settings[15] = 1'b1; // Q16  //PIX_SEL_11
163         trim_settings[16] = 1'b0; // Q17  //PIX_SEL_12
164         trim_settings[17] = 1'b0; // Q18  //PIX_SEL_13
165         trim_settings[18] = 1'b0; // Q19  //PIX_SEL_14
166         trim_settings[19] = 1'b0; // Q20  //PIX_SEL_15
167         trim_settings[20] = 1'b0; // Q21  //PIX_TEST_16
168         trim_settings[21] = 1'b0; // Q22     //PIX_TEST_17
169         trim_settings[22] = 1'b0; // Q23  //PIX_TEST_18
170
171         trim_settings[23] = 1'b0; // Q24     //S62
172         trim_settings[24] = 1'b0; // Q25     //S61
173         trim_settings[25] = 1'b0; // Q26     //S52
174         trim_settings[26] = 1'b0; // Q27     //S51
175         trim_settings[27] = 1'b0; // Q28     //S42
176         trim_settings[28] = 1'b0; // Q29     //S41
177         trim_settings[29] = 1'b0; // Q30     //S32
178         trim_settings[30] = 1'b0; // Q31     //S31
179         trim_settings[31] = 1'b0; // Q32     //S22
180         trim_settings[32] = 1'b0; // Q33     //S21
181         trim_settings[33] = 1'b0; // Q34     //S12
182         trim_settings[34] = 1'b0; // Q35     //S11
183
184         trim_settings[35] = 1'b0; // Q36     //DISC_SEL
185
186         trim_settings[36] = 1'b0; // Q37     //DIGI_SEL_1
187         trim_settings[37] = 1'b0; // Q38     //DIGI_SEL_2
188
189         trim_settings[38] = double_en;   // Q39     //DOUBLE_EN
190         trim_settings[39] = S_double[0]; // Q40     //DOUBLE_DEL_1
191         trim_settings[40] = S_double[1]; // Q41     //DOUBLE_DEL_2
```

```
192         trim_settings[41] = S_double[2]; // Q42     //DOUBLE_DEL_3
193         trim_settings[42] = S_double[3]; // Q43     //DOUBLE_DEL_4
194         trim_settings[43] = S_double[4]; // Q44     //DOUBLE_DEL_5
195
196         trim_settings[44] = triple_en; // Q45     //TRIPLE_EN
197         trim_settings[45] = S_triple[0]; // Q46     //TRIPLRE_DEL_1
198         trim_settings[46] = S_triple[1]; // Q47     //TRIPLRE_DEL_2
199         trim_settings[47] = S_triple[2]; // Q48     //TRIPLRE_DEL_3
200         trim_settings[48] = S_triple[3]; // Q49     //TRIPLRE_DEL_4
201         trim_settings[49] = S_triple[4]; // Q50     //TRIPLRE_DEL_5
202
203         trim_settings[50] = S_pulse[0]; // Q51     //PULSE_WIDTH_1
204         trim_settings[51] = S_pulse[1]; // Q52     //PULSE_WIDTH_2
205         trim_settings[52] = S_pulse[2]; // Q53  //PULSE_WIDTH_3
206
207         trim_settings[53] = 1'b0; // Q54  //DUMMY
208         trim_settings[54] = 1'b0; // Q55  //DUMMY
209         trim_settings[55] = 1'b0; // Q56  //DUMMY
210         trim_settings[56] = 1'b0; // Q57  //DUMMY
211         trim_settings[57] = 1'b0; // Q58  //DUMMY
212         trim_settings[58] = 1'b1; // Q59  //DUMMY
213
214         trim_settings[59] = enable_trig; // Q60  //ENABLE_TRIG
215         trim_settings[60] = enable_all; // Q61  //ENABLE_ALL
216
217         trim_settings[61] = S_pix[3]; // Q62  //S_PIX_3
218         trim_settings[62] = S_pix[2]; // Q63  //S_PIX_2
219         trim_settings[63] = S_pix[1]; // Q64  //S_PIX_1
220         trim_settings[64] = S_pix[0]; // Q65  //S_PIX_0
221
222         trim_settings[65] = S_rst[3]; // Q66  //S_RST_3
223         trim_settings[66] = S_rst[2]; // Q67  //S_RST_2
224         trim_settings[67] = S_rst[1]; // Q68  //S_RST_1
225         trim_settings[68] = S_rst[0]; // Q69  //S_RST_0
226
227         trim_settings[69] = S_del_meas; // Q70  //S_DAC_MEAS
228
229         trim_settings[70] = ext_ref; // Q71  //EXT_REF
230         trim_settings[71] = int_ref; // Q72  //INT_REF
231
232         trim_settings[72] = ref_pol; // Q73  //REF_POL
233         trim_settings[73] = S_ref[3]; // Q74  //S_REF_3
234         trim_settings[74] = S_ref[2]; // Q75  //S_REF_2
235         trim_settings[75] = S_ref[1]; // Q76  //S_REF_1
236         trim_settings[76] = S_ref[0]; // Q77  //S_REF_0
237
238         trim_settings[77] = S_det[3]; // Q78  //S_DEL_3
239         trim_settings[78] = S_det[2]; // Q79  //S_DEL_2
240         trim_settings[79] = S_det[1]; // Q80  //S_DEL_1
241         trim_settings[80] = S_det[0]; // Q81  //S_DEL_0
242
243         trim_settings[81] = S_dummy[3]; // Q82  //S_DUMMY_3
244         trim_settings[82] = S_dummy[2]; // Q83  //S_DUMMY_2
245         trim_settings[83] = S_dummy[1]; // Q84  //S_DUMMY_1
246         trim_settings[84] = S_dummy[0]; // Q85  //S_DUMMY_0
247
248         trim_settings[85] = S_Qth[3]; // Q86  //S_QTH_3
249         trim_settings[86] = S_Qth[2]; // Q87  //S_QTH_2
250         trim_settings[87] = S_Qth[1]; // Q88  //S_QTH_1
251         trim_settings[88] = S_Qth[0]; // Q89  //S_QTH_0
252
253         trim_settings[89] = 1'b0; // Q90  //DUMMY
254         trim_settings[90] = 1'b0; // Q91  //DUMMY
255         trim_settings[91] = 1'b0; // Q92  //DUMMY
```

```
256         trim_settings[92] = 1'b0; // Q93  //DUMMY
257         trim_settings[93] = 1'b0; // Q94  //DUMMY
258         trim_settings[94] = 1'b0; // Q95  //DUMMY
259         trim_settings[95] = 1'b0; // Q96  //DUMMY
260         trim_settings[96] = 1'b0; // Q97  //DUMMY
261         trim_settings[97] = 1'b0; // Q98  //DUMMY
262         trim_settings[98] = 1'b0; // Q99  //DUMMY
263         trim_settings[99] = 1'b0; // Q100 //DUMMY
264
265
266         if (write_en == 1) begin
267             if (negedge_first == 1) begin
268                 if (counter > 0) begin
269                     counter = counter-1;
270                 end
271             end
272         end else begin
273             counter = 99;
274         end
275     end
276
277 endmodule
```

Fig. C.4: SR_PROG.v

```
module CALB_EN
#(parameter CALB_DURATION = 40, CALB_REFRESH = 4000)
(
    input SR_EN, CLK,
    input [3:0] TEST,
    output reg CALB_OUT
);

integer count;
reg calb_on_refresh;
reg calb_started;
reg calb_on_always;

    initial begin
        count = 0;
        CALB_OUT = 1'b0;
        calb_on_refresh = 1'b0;
        calb_on_always = 1'b0;
        calb_started = 1'b0;
    end

    // Enable the calibration based on the current test
    always @ (TEST) begin
        case (TEST)
            4'b0000 : calb_on_refresh = 1'b0;
            4'b0001 : calb_on_refresh = 1'b0;
            4'b0010 : calb_on_refresh = 1'b0;
            4'b0011 : calb_on_refresh = 1'b1;
            4'b0100 : calb_on_refresh = 1'b1;
            4'b0101 : calb_on_refresh = 1'b1;
            4'b0110 : calb_on_refresh = 1'b1;
            4'b0111 : calb_on_refresh = 1'b1;
            4'b1000 : calb_on_refresh = 1'b1;
            4'b1001 : calb_on_refresh = 1'b1;
            4'b1010 : calb_on_refresh = 1'b1;
            4'b1011 : calb_on_refresh = 1'b1;
            4'b1100 : calb_on_refresh = 1'b1;
            4'b1101 : calb_on_refresh = 1'b1;
            4'b1110 : calb_on_refresh = 1'b1;
            4'b1111 : calb_on_refresh = 1'b0;
        endcase;

        case (TEST)
            4'b0000 : calb_on_always = 1'b0;
            4'b0001 : calb_on_always = 1'b1;
            4'b0010 : calb_on_always = 1'b1;
            4'b0011 : calb_on_always = 1'b0;
            4'b0100 : calb_on_always = 1'b0;
            4'b0101 : calb_on_always = 1'b0;
            4'b0110 : calb_on_always = 1'b0;
            4'b0111 : calb_on_always = 1'b0;
            4'b1000 : calb_on_always = 1'b0;
            4'b1001 : calb_on_always = 1'b0;
            4'b1010 : calb_on_always = 1'b0;
            4'b1011 : calb_on_always = 1'b0;
            4'b1100 : calb_on_always = 1'b0;
            4'b1101 : calb_on_always = 1'b0;
            4'b1110 : calb_on_always = 1'b0;
            4'b1111 : calb_on_always = 1'b0;
        endcase;
    end

    // Start the calibration when the SR programming is done
```

```
64
65      always @(SR_EN) begin
66          if(SR_EN == 1)
67              calb_started = 1'b0;
68          else
69              calb_started = 1'b1;
70      end
71
72      always @(posedge CLK) begin
73          // start counting if the calibration is started
74          if (calb_started == 1 && calb_on_refresh == 1) begin
75
76              count = count + 1;
77
78              // Set the calbiration signal to high
79              if(count == 1)
80                  CALB_OUT = 1'b1;
81
82              // Set the calibration signal to low again
83              if(count > CALB_DURATION)
84                  CALB_OUT = 1'b0;
85
86              // Return the counter to 0 to start a new calibration sequence
87              if(count > CALB_REFRESH) begin
88                  count = 0;
89              end
90          end else if (calb_started == 1 && calb_on_always == 1) begin
91              CALB_OUT = 1'b1;
92          end else begin
93              CALB_OUT = 1'b0;
94          end
95      end
96  endmodule
```

Fig. C.5: CALB_EN.v

```
module TRIG_SIG
(
    input CLK, EN,
    input [3:0] TEST,
    output reg OUT
);

integer counter;
integer n;
reg trig_en;
    initial begin

        counter = 0;
        OUT = 1'b0;
        n = 4;
        trig_en = 1'b0;
    end

    always @ (TEST) begin
        case(TEST)
            4'b0000 : trig_en = 1'b0;
            4'b0001 : trig_en = 1'b0;
            4'b0010 : trig_en = 1'b0;
            4'b0011 : trig_en = 1'b0;
            4'b0100 : trig_en = 1'b0;
            4'b0101 : trig_en = 1'b0;
            4'b0110 : trig_en = 1'b1;
            4'b0111 : trig_en = 1'b1;
            4'b1000 : trig_en = 1'b1;
            4'b1001 : trig_en = 1'b1;
            4'b1010 : trig_en = 1'b1;
            4'b1011 : trig_en = 1'b1;
            4'b1100 : trig_en = 1'b1;
            4'b1101 : trig_en = 1'b1;
            4'b1110 : trig_en = 1'b1;
            4'b1111 : trig_en = 1'b0;
        endcase;
    end

    always @(posedge CLK) begin
        counter =  counter + 1;
        if (trig_en && EN) begin
            if (counter == n + 1 || counter == 2*n + 1|| counter == 3*n + 1 || counter == 4*n + 1)
                OUT = 1'b1;
            else
                OUT = 1'b0;

            if (counter > 2000)
                counter = 0;
        end else begin
            OUT = 1'b0;
        end
    end
endmodule
```

Fig. C.6: TRIG_SIG.v

```
module SEG_DRIVER
(
    input [3:0] in,
    output reg [6:0] out
);
    initial begin
        out = 7'b0000000;
    end

    always @ (in) begin
        case(in)
            4'b0000 : out = 7'b0000001;
            4'b0001 : out = 7'b1001111;
            4'b0010 : out = 7'b0010010;
            4'b0011 : out = 7'b0000110;
            4'b0100 : out = 7'b1001100;
            4'b0101 : out = 7'b0100100;
            4'b0110 : out = 7'b0100000;
            4'b0111 : out = 7'b0001111;
            4'b1000 : out = 7'b0000000;
            4'b1001 : out = 7'b0000100;
            4'b1010 : out = 7'b0001000;
            4'b1011 : out = 7'b1100000;
            4'b1100 : out = 7'b0110001;
            4'b1101 : out = 7'b1000010;
            4'b1110 : out = 7'b0110000;
            4'b1111 : out = 7'b0111000;
            default : out = 7'b0000000;
        endcase;
    end
endmodule
```

Fig. C.7: SEG_DRIVER.v

```
module SET_SWEEP_VAR
(
    input UP,
    output reg [3:0] SWEEP_VAR
);
    initial begin
        SWEEP_VAR = 0;
    end

    always @ (posedge UP) begin
        SWEEP_VAR = SWEEP_VAR + 1;
    end
endmodule
```

Fig. C.8: SET_SWEEP_VAR.v

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