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**DOI**
10.1109/JSSC.2020.2987719

**Publication date**
2020

**Document Version**
Final published version

**Published in**
IEEE Journal of Solid-State Circuits

# A 64-Channel Transmit Beamformer With ±30-V Bipolar High-Voltage Pulsers for Catheter-Based Ultrasound Probes

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***Abstract*— This article presents a fully integrated 64-channel programmable ultrasound transmit beamformer for catheter-based ultrasound probes, designed to interface with a capacitive micro-machined ultrasound transducer (CMUT) array. The chip is equipped with programmable high-voltage (HV) pulsers that can generate ±30-V return-to-zero (RZ) and non-RZ pulses. The pulsers employ a compact back-to-back isolating HV switch topology that employs HV floating-gate drivers with only one HV MOS transistor each. Further die-size reduction is achieved by using the RZ switches also as the transmit/receive (T/R) needed to pass received echo signals to low-voltage receive circuitry. On-chip digital logic clocked at 200 MHz allows the pulse timing to be programmed with a resolution of 5 ns, while supporting pulses of 1 cycle up to 63 cycles. The chip has been implemented in 0.18-$\mu$m HV Bipolar-CMOS-DMOS (BCD) technology and occupies an area of 1.8 mm × 16.5 mm, suitable for integration into an 8-F catheter. Each pulser with embedded T/R switch and digital logic occupies only 0.167 mm$^2$. The pulser successfully drives an 18-pF transducer capacitance at pulse frequencies up to 9 MHz. The T/R switch has a measured ON-resistance of ∼180 Ω. The acoustic results obtained in combination with a 7.5-MHz 64-element CMUT array demonstrate the ability to generate steered and focused acoustic beams.**

***Index Terms*— Capacitive micro-machined ultrasonic transducer (CMUT), high-voltage (HV) bipolar pulser, HV driver, transmit beamformer, transmit/receive switching, ultrasound.**

## I. Introduction

ULTRASOUND imaging is a safe, cost-effective, and widely used imaging modality for the diagnosis and treatment of cardiovascular conditions. Miniaturized ultrasound devices mounted at the tip of a catheter or endoscope are becoming increasingly important as they can provide better image quality than external hand-held probes, for instance, to guide minimally invasive cardiac interventions [1]. A prime example is intra-cardiac echocardiography (ICE) probes, which generate ultrasound images from inside the heart using a transducer array mounted at the tip of a catheter [2]. The image construction relies on the transmission of acoustic waves and post-processing of the reflected echo signals. The acoustic waves are generated by exciting the elements of the transducer array with voltage pulses. Typically, these pulses are timed such that an acoustic beam is formed that is focused and steered at a particular angle. Different pulse timing in successive pulse-echo cycles allows the beam to scan the region of interest to form an image. Since the acoustic signal will be significantly attenuated as it propagates through tissue, high-voltage (HV) pulses (with amplitudes of tens of volts) are required to generate enough pressure so that the overall signal-to-noise ratio (SNR) is sufficiently high at the largest imaging depth [3].

In most commercial ICE catheters, the elements in the transducer array are connected to transmit (TX) and receive (RX) circuitry in an imaging system through long micro-coax cables. Given the signal attenuation caused by such cables and difficulties of the cable assembly, application-specific integrated circuits (ASICs) have been integrated closely to the transducer array to reduce the number of cables and increase the SNR by locally amplifying the echo signals [4]–[9].

An important challenge in the design of such in-probe ASICs is that the required HV TX circuitry cannot be implemented in standard CMOS technologies. This applies to the HV pulsers and to the transmit/receive (T/R) switches needed to protect the low-voltage (LV) RX circuitry during pulse transmission. Therefore, HV Bipolar-CMOS-DMOS (BCD) technologies are usually adopted in which HV MOS transistors are available [4], [5], [8]. Such transistors, however, tend to occupy a large die area, while the available area is limited in catheter-based devices. This calls for a compact pulser and T/R SW design.

Unipolar pulsers have been applied (which can only generate positive HV pulses), as they can be implemented using a small number of HV transistors [10], [11]. However, this comes with several disadvantages. Contrary to the bipolar pulses commonly generated by conventional imaging systems, unipolar pulses contain more low-frequency out-of-band energy and, thus, lead to lower SNR for the same peak-to-peak

Manuscript received November 29, 2019; revised February 13, 2020; accepted March 17, 2020. Date of publication April 29, 2020; date of current version June 29, 2020. This paper was approved by Guest Editor Lucien J. Breems. This work is a part of the ULIMPIA project funded by PENTA under Grant PENTA-2017-Call2-16101-ULIMPIA. *(Corresponding author: Mingliang Tan.)*

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Digital Object Identifier 10.1109/JSSC.2020.2987719

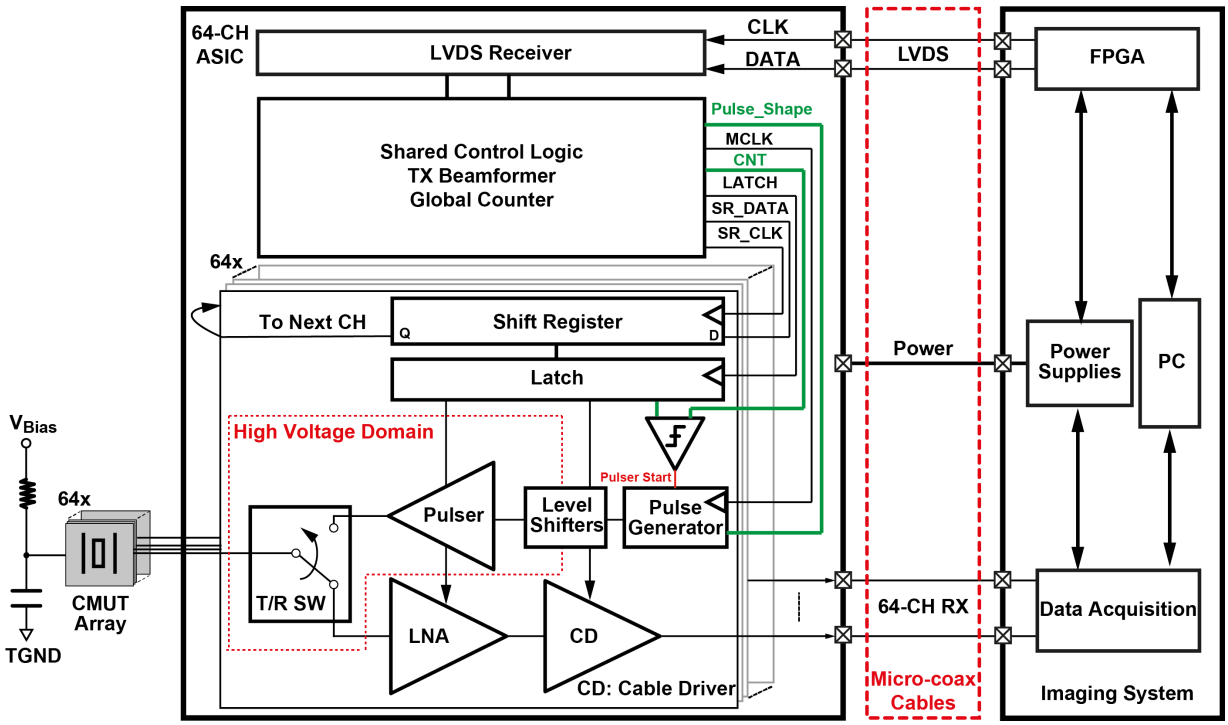


Fig. 1. System architecture.

amplitude [12]. Moreover, many image-enhancing techniques, such as pulse inversion and coded excitation, are easier to implement using bipolar pulses [13]. Therefore, it is worthwhile to design an on-chip bipolar pulser although the architecture is more complicated.

An added benefit of using bipolar pulsing is that it can reduce the dynamic power consumption of the pulser by at best a factor of 2 compared to a unipolar pulser with the same peak-to-peak output voltage, provided a return-to-zero (RZ) pulser is used [14]. This is an important advantage, since the overall power consumption of the ASIC should be minimized to avoid tissue overheating.

In this article, we present a front-end ASIC for a 64-element transducer array that includes an on-chip transmit beamformer and programmable bipolar pulsers. This article extends on our previous work [15], [16], in which the bipolar pulser has been described. Here, we present a complete ASIC intended for a capacitive micro-machined ultrasound transducer (CMUT)-based 2-D ICE probe. With a width of less than 2 mm, the ASIC is suitable for catheter integration and directly connects to the transducer elements in a pitch-matched fashion through a printed circuit board (PCB) interposer. The ASIC only needs two LV differential signaling (LVDS) clock and data lines to program the on-chip transmit beamformer. The electrical and acoustical measurement results are presented that successfully show the functionality of the bipolar pulser and the complete TX beamformer.

This article is organized as follows. Section II describes the system architecture. Section III discusses the design of the bipolar pulser, while Section IV presents the details of the circuit implementation. Sections V and VI present the experimental results and conclusion.

## II. System Architecture

Fig. 1 shows a block diagram of the proposed system. It consists of a 64-element CMUT transducer array, a front-end ASIC, and the imaging system. The elements of the transducer array are directly connected to channels of the ASIC at the tip of the catheter, while a bundle of micro-coax cables (∼2 m in length) is used to connect the ASIC with the imaging system.

We employ a CMUT transducer array with a center frequency of 7.5 MHz, targeting ICE applications [9], [11]. All the CMUT elements are DC biased at $V_{\text{bias}}$ and AC coupled to the transducer ground (TGND) through a shared *RC* network. To interface with the CMUT elements, each channel of the ASIC contains a T/R switch, an HV TX pulser with associated level shifters and pulse generator, a low-noise amplifier (LNA), a cable driver (CD), and a latched shift register (SR) for the configuration.

Clock and data are provided to the ASIC by a field-programmable gate array (FPGA) through LVDS signals, which are first converted to 1.8-V standard logic levels through an on-chip LVDS receiver. Then, shared control logic will generate a clock (SR_CLK) and data (SR_DATA) for the element-level SRs, a latch signal (LATCH) for the element-level latches, and a master clock (MCLK) and counter (CNT) for the timing control of the pulse generators. The SR of each channel provides the configuration data for the RX amplifiers and HV pulsers, as well as a counter value, which is compared to CNT to define the start time of the pulse. The SRs are daisy chained to allow the element-level configuration data to be loaded sequentially from the shared control logic. According to the loaded data in the SR, the pulse generator will generate LV signals to control the HV pulser through the level shifters with a proper timing.

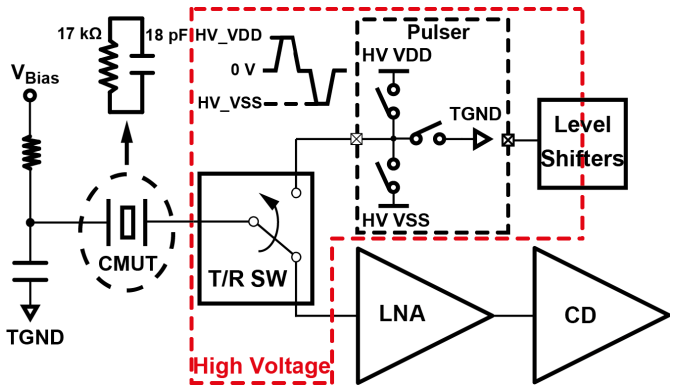


Fig. 2. Simplified block diagram of a single transceiver channel of the ASIC.

When the CMUT transducer element is excited by the HV pulses, ultrasonic waves are emitted into the medium. The resulting echo signals are amplified by the LNAs, which are connected to the transducer elements via the T/R switches after pulsing, and then transferred to the imaging system through micro-coax cables with the help of CD. The details of the LNA and CD are presented in [17]. The imaging system will record the echo signals and process them for image reconstruction.

## III. Bipolar Pulser Design

Fig. 2 shows the simplified block diagram of a single ultrasound transceiver channel of the ASIC. To generate RZ bipolar pulses, the pulser consists of a pull-up switch that drives the CMUT transducer to a positive HV supply (HV_VDD), a pull-down switch that drives it to a negative HV supply (HV_VSS), and an RZ switch that pulls the transducer back to ground. The impedance of the CMUT element used in this work can be modeled as 18 pF//17 kΩ.

### A. Switch Configurations With Bidirectional Isolation

The RZ switch needs to provide bidirectional HV isolation, in the sense that when it is OFF, it should be able to handle both positive voltage drop and negative voltage drop. Similarly, the T/R switch, which connects the transducer to the LNA during echo reception, needs to provide bidirectional HV isolation during pulsing. Two technology-related limitations of the HV MOS transistors in BCD technologies, the body diode and the limited gate-oxide breakdown voltage, increase the implementation complexity of the T/R switch and the RZ switch. The presence of the body diode implies that two back-to-back connected HV transistors are needed to provide bidirectional isolation. The relatively low gate-oxide breakdown voltage requires a more complicated gate-driver design compared to HV technologies with thick gate oxide.

Fig. 3 shows the eight possible back-to-back configurations of HV NMOS and PMOS transistors. The body-diode orientation in configurations shown in Fig. 3(a)–(d) is such that the middle node between the transistors ($V_{\text{mid}}$) swings up with the positive HV pulse, while in configurations shown in Fig. 3(e)–(h), it swings down with the negative HV pulse. In all configurations, at least one of the sources of the

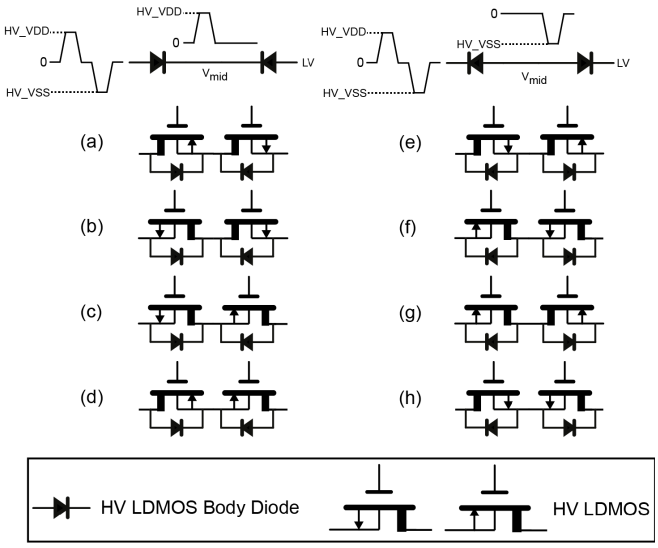


Fig. 3. Overview of HV MOS configurations that can provide back-to-back isolation. (a)–(d) Middle node $V_{\text{mid}}$ swings up with the signal. (e)–(h) $V_{\text{mid}}$ swings down with the signal.

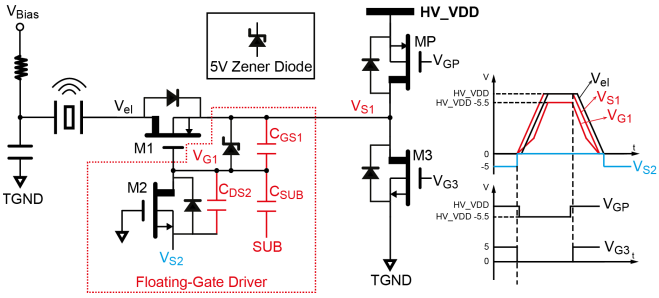


Fig. 4. Circuit diagram of a high-side pulser employing the single-transistor HV floating-gate driver circuit.

transistors swings up and/or down with the HV pulse, implying that an HV gate driver is needed that keeps the gate–source voltage below the gate-oxide breakdown limit (5.5 V in our technology). To prevent this HV floating-gate driver from having to operate at both positive and negative HVs, configurations in which the source of the left-hand transistor connects to the transducer should be avoided. Driving the source of the right-hand transistor is easier if it connects to the LV circuitry rather than to $V_{\text{mid}}$. This leaves configurations shown in Fig. 3(a) and (e) as the preferred choice, both of which are applied in parallel in our implementation.

### B. Floating-Gate Driver

In previous HV switch designs [5], [8], [18], bootstrapped gate drivers have been employed. However, they cannot be applied in an RZ switch, because they only allow the switch to be turned on when it is at ground level, while the RZ switch needs to be turned on when the pulser output is at HV_VDD or HV_VSS. Therefore, we propose a compact and energy-efficient floating-gate driver that utilizes parasitic capacitance to control the gate–source voltage and requires only one additional small HV MOS transistor.

This circuit is shown in Fig. 4, in the context of a unipolar (high-side) pulser. HV transistors MP and M1 are used to

pull the transducer to HV_VDD, while M1 and M3 together form the switch configuration of Fig. 3(a) to provide the RZ switching. The gate of MP is driven relative to HV_VDD using a conventional level-shifter circuit. The gate of M1 is driven by our new gate-drive approach using transistor M2. Initially, to short the transducer to ground, M3 and M1 are turned on. M1 is turned on through M2 by connecting M2 source to −5 V and its gate to ground, so that the gate of M1 is pulled to −5 V. Before the HV pulsing starts, the source of M2 is switched to ground, so that the gate of M1 is discharged to ground through the body diode of M2. After this, M2 is OFF and the gate of M1 floats. When MP is turned on and M3 is turned off, the voltage step on $V_{S1}$ will also create a step on the gate of M1 because of the capacitive divider formed by $C_{GS1}$ and $C_{DS2} + C_{SUB}$, where $C_{SUB}$ is the capacitance from the gate of M1 to the substrate. By properly sizing M2 to make $C_{DS2} + C_{SUB}$ larger than $C_{GS1}$, $V_{GS1}$ will increase, turning on M1 and, thus, allowing the transducer to be charged to HV_VDD. A Zener diode prevents $V_{GS1}$ from exceeding the breakdown voltage. At the beginning of the RZ phase, MP is turned off and M3 is turned on, while M1 remains ON. This discharges the transducer until $V_{el}$ reaches the threshold voltage of M1 of 0.7 V (∼85 times smaller than the pulse peak-to-peak amplitude), thus realizing an almost complete RZ operation. Finally, the gate of M1 is pulled to −5 V through M1.

### C. Embedded T/R Switch

The circuit of Fig. 4 can be extended with one additional LV transistor M0 to allow it to act also as a T/R switch, as shown in Fig. 5. This transistor is placed in series with the source of M3 and is turned on during the TX phase, allowing the circuit to operate as before and preventing any feedthrough of the HV pulse from reaching the RX circuitry. Although M0 will increase the total series resistance for the RZ phase, it can be sized to have a low ON-resistance compared to that of M1 and M3 without significantly affecting the total die area since it is an LV MOS transistor. During the TX phase, when the HV pulsing finishes and $V_{S1}$ and $V_{G1}$ are at ground level, M1, M3, and M0 are turned on to short the transducer to TGND. During the RX phase, M0 is turned off so that the received echo signal can pass through M1 and M3 to the LV receive circuitry. Since the parasitic capacitance of the LV transistor M0 is relatively small, the transient introduced by the switching of M0 is negligible. Turning on M1 through M2 requires the source of M2 to be −5 V, which is realized using a simple LV charge-pump-based level shifter (see Section III-B). Thus, only four HV transistors are used to implement HV pull-up, RZ, and T/R switch functionality.

### D. Complete Bipolar Pulser

To realize a complete bipolar pulser, the high-side circuit of Fig. 5 is combined with a complementary low-side version. Fig. 6 shows the resulting circuit, including the various level shifters and the associated timing diagram. During the TX phase, M2 and M5 are turned off to float the gate of M1 and M4. Pulling up the pulser output from ground to HV_VDD and

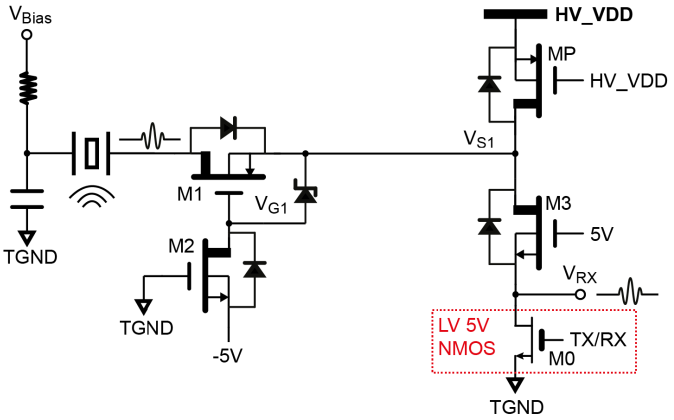


Fig. 5. Circuit diagram of the high-side pulser with an embedded T/R switch.

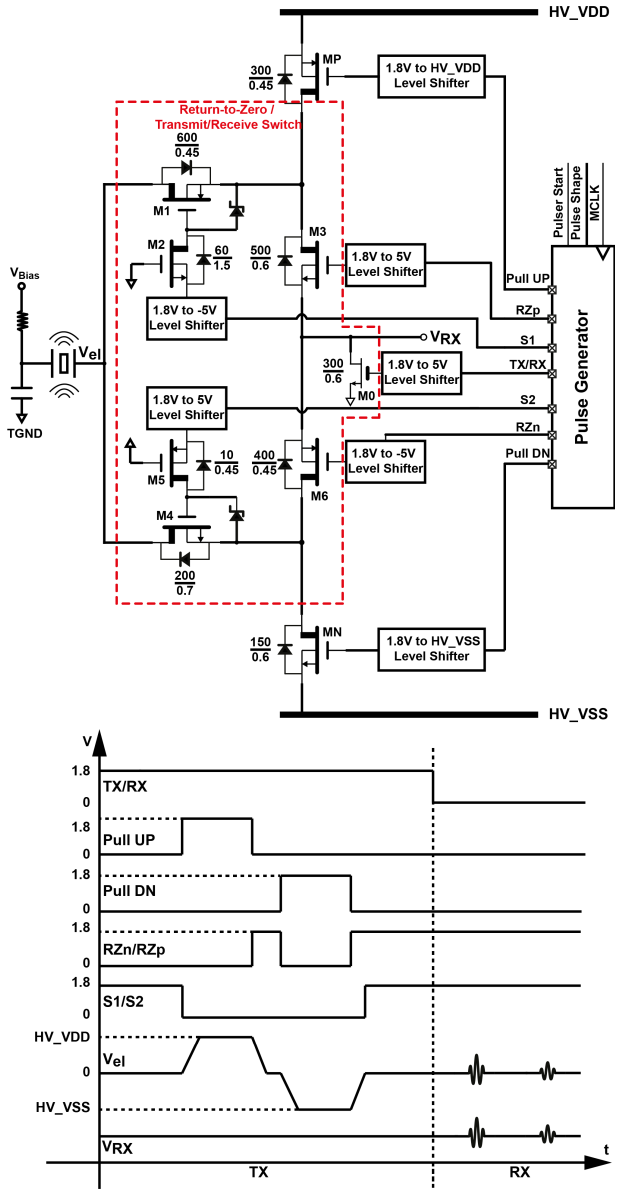


Fig. 6. Circuit diagram of the complete pulser, with the associated timing diagram.

pulling down the output from HV_VDD to ground (RZ phase) are done by turning on MP and M3, respectively, as discussed in Section III-C. The same concept is applied in the

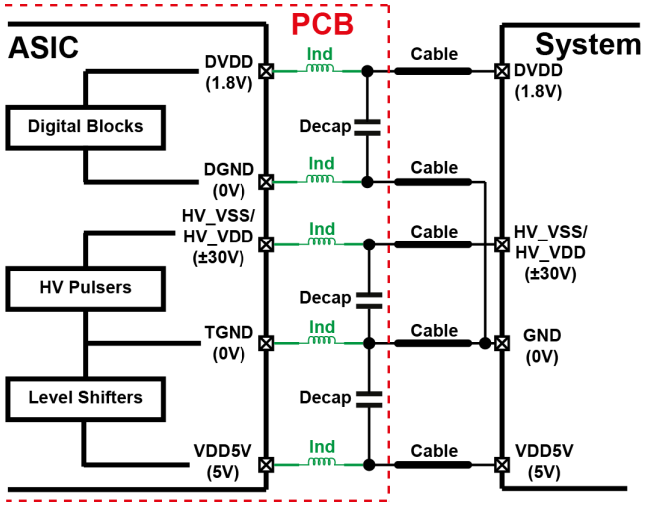


Fig. 7. Overview of the power supplies in the proposed system.

complementary low-side pulser for the transition from ground to HV_VSS and HV_VSS to ground, by turning on MN and M6, respectively. After the TX phase, the two sets of RZ switches (M1 and M3) and (M4 and M6) are turned on in parallel to serve as a T/R switch, reducing the ON-resistance (and the associated noise) by 2× and saving substantial area compared to a separate T/R switch.

Depending on configuration bits stored in the element-level SR, the pulse generator can provide the following operating modes: 1) bipolar RZ pulsing as shown in the timing diagram of Fig. 6; 2) bipolar non-RZ (NRZ) pulsing (by setting the RZ time to 0); and 3) unipolar pulsing (by setting the pull-up time or the pull-down time to 0). Moreover, the width of the pulses can be defined (in terms of cycles of the 200-MHz clock) to enable pulsewidth programming, allowing the pulser to be used at different frequencies.

## IV. Circuit Implementation Details

### A. Supply Domains

Fig. 7 shows the power supplies used in the proposed system. The power supply for the digital blocks (DVDD) is locally decoupled to the digital ground (DGND) on the PCB, while HV_VDD, HV_VSS, and the 5-V supply for the level shifters (VDD5V) are locally decoupled to TGND. These supplies and grounds are connected to the system side through cables. To prevent transients associated with the operation of the digital circuits from affecting the analog circuitry, DGND and TGND are joined together on the system side. A limited set of decoupling capacitors, sized to be able to fit inside a catheter, is placed as close to the ASIC as possible to provide transient supply currents. Nevertheless, there is still certain inductance between these decoupling capacitors and the on-chip circuitry, which will give rise to $di/dt$ transients on the supplies. The level shifters need to be designed to be immune to these transients.

### B. Level Shifters

The level shifters shift the 1.8-V logic-level signals to 5-V signals relative to ground, HV_VDD, and HV_VSS to drive

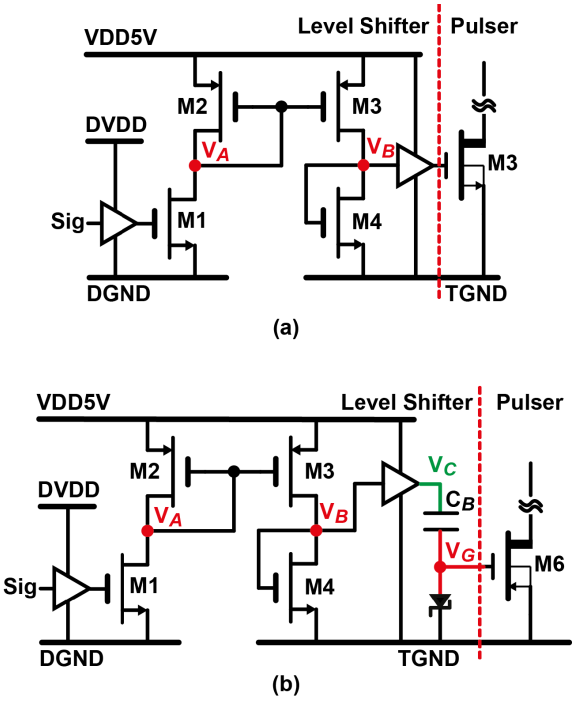


Fig. 8. (a) 1.8–5 V level shifter. (b) 1.8 V to −5 V level shifter.

the gates of the HV MOS transistors (see Fig. 6). To reliably level-shift logic-level signals in the DGND–DVDD domain to the TGND–VDD5V domain, in the presence of potential voltage transients between DGND and TGND, we propose the current-mode level-shifter architecture shown in Fig. 8(a). When the logic input is high, a current provided by M1 is copied to the 5-V domain by current mirror M2, M3, causing a high level on diode-connected transistor M4, which is buffered to a proper 5-V level to drive HV MOS MN. When the logic input is low, the absence of current in M4 leads to a low level that turns off MN.

To turn on HV PMOS M6 in Fig. 6, a negative 5-V level is required. Instead of using an external −5 V supply, a charge-pump-based architecture is used. Fig. 8(b) shows the circuit diagram. During the start-up, $V_G$is discharged to TGND through diode leakage. Then, the bootstrap capacitor is pre-charged to VDD5V through a 1.85-V level shifter. Therefore, $V_G$will be pulled down to −5 V when the level shifter output is 0 V in the ideal case. The bootstrap capacitor $C_B$ is sized to ∼5.4 pF so that MP gets enough over-drive voltage even though some charge will be lost due to the gate capacitance at node $V_G$.

Because HV_VDD and HV_VSS are also suffering from $di/dt$ noise, the 1.8 V to HV_VDD and HV_VSS level shifters also apply a current-mode architecture, as shown in Fig. 9. $V_{GS}$of MP and MN in the pulser is determined by the IR drop on resistors $R1$ and $R2$, while the current mainly depends on the over-drive voltage and the transistor size of M1 and M2. By applying the architecture shown in Fig. 8(a) for the 1.8–5 V level shifter, an over-drive voltage that is insensitive to the $di/dt$ noise of HV_VDD/HV_VSS is obtained. Thus, MP and MN of the pulser can be turned on or off safely. Monte Carlo simulations indicate that the expected channel-to-channel mismatch introduced by the level shifters is less

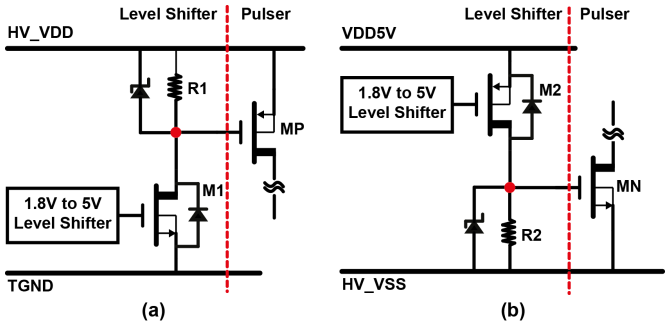


Fig. 9. (a) 1.8 V to HV_VDD level shifter. (b) 1.8 V to HV_VSS level shifter.

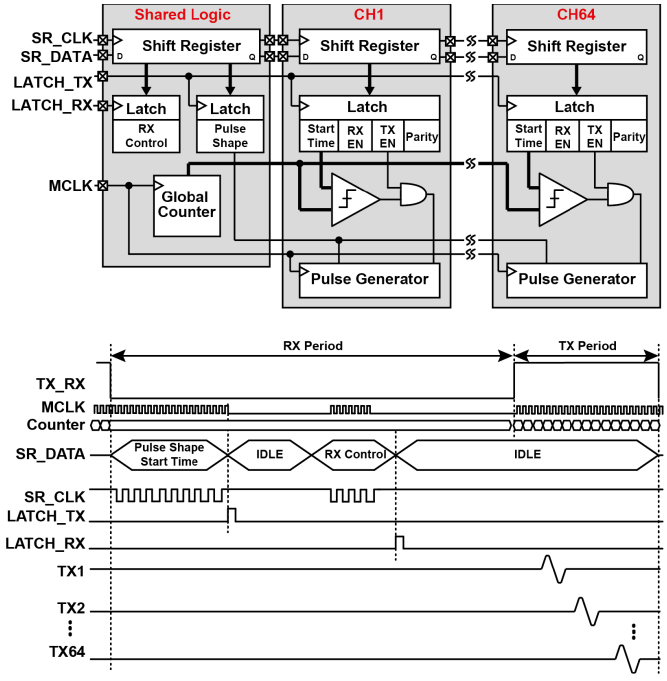


Fig. 10. Block diagram and timing diagram of the TX beamformer logic.

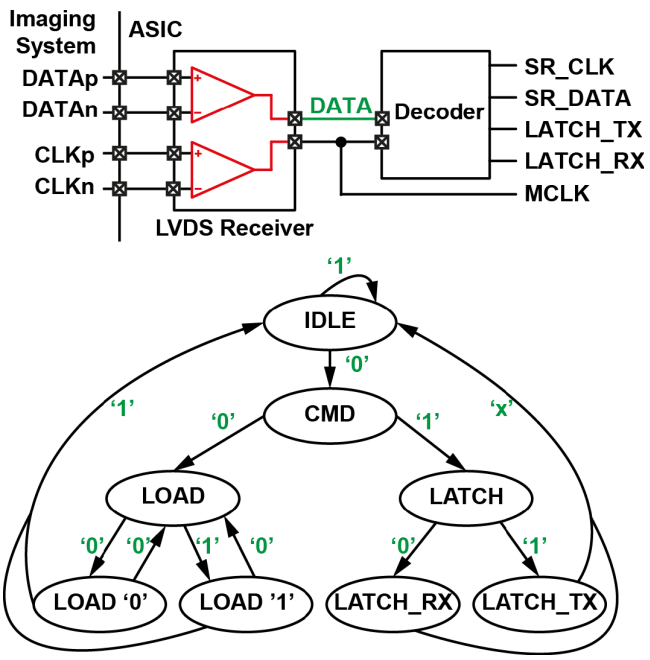


Fig. 11. Shared control logic, with state diagram of the associated FSM.

than 1% of the cycle time of the 7-MHz pulse, which has a negligible impact on the beamforming.

### C. TX Beamformer Logic

For TX beamforming, the pulser in each channel should start generating an HV pulse at a well-defined time. This is done by comparing the start time pre-programmed in each channel with a global counter output (CNT in Fig. 1) clocked at 200 MHz (MCLK). Fig. 10 illustrates the block diagram and associated timing diagram of the TX beamformer logic. At the start of the RX period, configuration data (SR_DATA) are loaded sequentially into the daisy-chained shift registers of the shared logic and the 64 channels. The data for controlling the pulse shape and the pulse start time are loaded first and latched by LATCH_TX. These data will be used in the TX period and updated in the next RX period. During the remaining part of the RX period, the SR clock, SR data, and the global clock are quiet unless RX control data (like the gain setting of the LNAs) need to be updated. This leads to low average power consumption and minimizes the interference with the sensitive RX circuitry. At the start of the TX period, the global counter starts to run at the frequency of MCLK of 200 MHz. The counter output is distributed across the 64 channels and is compared to the start time which is pre-stored in the latch of each channel. If the counter output matches the stored start time and the channel is enabled, a pulser start signal will be generated to start the HV pulsing with a pre-defined pulse shape determined by the pulse-shape configuration data stored in the shared logic. Approximately 10 $\mu$s is needed to load all the configuration data with an SR_CLK of 100 MHz. This leads to a maximum pulse-repetition frequency (PRF) of 100 kHz, which is sufficiently high in this application.

### D. Shared Digital Logic

Fig. 10 shows that a total of five signals are needed for the TX beamformer, which are SR_CLK, SR_DATA, LATCH_TX, LATCH_RX, and MCLK. To avoid an unnecessary increase in the cable count, the SR_CLK, SR_DATA, LATCH_TX, and LATCH_RX are encoded into the LVDS data line, while MCLK is derived from the LVDS clock line. Fig. 11 illustrates the decoder and associated finite-state machine (FSM). The LVDS clock and data are first converted to single-ended signals by the LVDS receiver. The single-ended clock output serves as MCLK and as the clock of the FSM, while the singled-ended data output controls the state transitions of the FSM.

As shown in the state diagram in Fig. 11, the bit sequence of "010" corresponds to the latch signal for the RX shift registers (LATCH_RX), while the bit sequence of "011" generates the LATCH_TX signal for the TX shift registers. The data loading of the SR starts with a bit sequence of "100." After that, the bits are loaded sequentially with the DATA bit "0" and

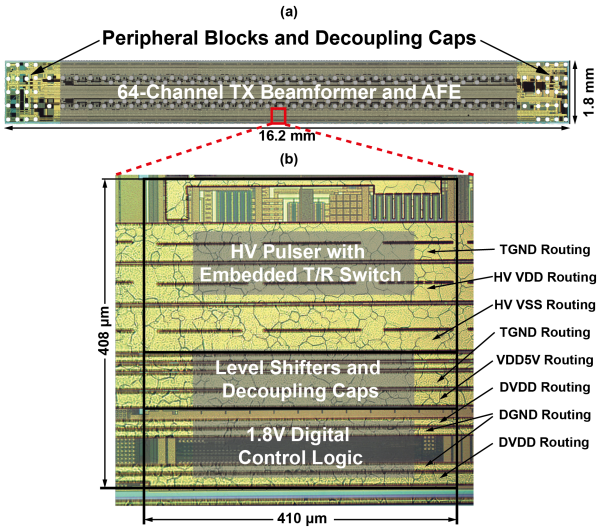


Fig. 12. (a) Chip photograph of the 64-channel ASIC with (b) zoomed-in view of the element-level transmit circuits.

"1" being encoded as "00" and "01," respectively. When the data loading finishes, the FSM will return to the IDLE state in which both clock and data lines remain quiet.

## V. Experimental Results

### A. Experimental Prototype

The ASIC has been realized in TSMC 0.18-$\mu$m HV BCD technology with a total area of 1.8 $\times$ 16.5 mm$^2$, as shown in Fig. 12. The 64 element-level circuit blocks (TX beamformer, HV pulsers, LNAs, and CDs) are located at the center of the chip, occupying an area of 1.8 $\times$ 13.12 mm$^2$. They are arranged in two rows of 32 blocks with a pitch of 410 $\mu$m, allowing direct connections to the 64-element CMUT transducer. Fig. 12(b) shows a zoomed-in view of the element-level TX circuitry, which occupies an area of 410 $\times$ 408 $\mu$m$^2$. The power supplies and grounds are routed horizontally across the chip in the top metal. The power consumption strongly depends on the ultrasound imaging mode and is dominated by the dynamic power consumed in driving the transducer capacitance.

### B. Electrical Measurement Results

To electrically characterize the prototype, an 18-pF capacitor is used as the load of the HV pulser, mimicking the transducer capacitance. To demonstrate the programmability of the proposed bipolar pulser, different configurations are applied to the pulser via the shift register. Fig. 13 shows the measured output voltage of a single pulser channel with RZ times of 50, 25, and 0 ns. The pulser can also be configured to generate pulses with different frequencies, allowing it to interface with different transducer elements for different applications. Fig. 14 shows the measured output voltage for 4-, 7-, and 9-MHz RZ and NRZ pulsing. Moreover, the proposed pulser can also be programmed to generate bursts of up to 63 pulses, which is suitable for Doppler imaging, as shown in Fig. 15(a). It is also possible to trade-off power consumption

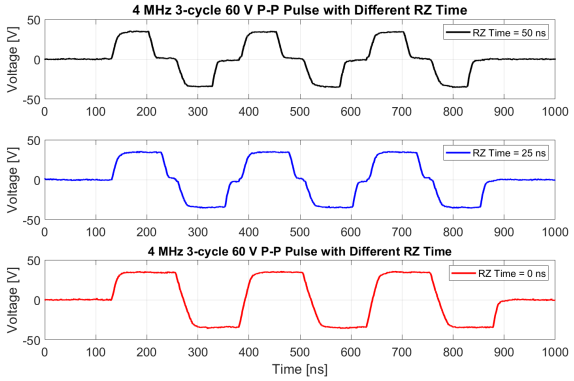


Fig. 13. Measured output voltage for different programmed RZ times.

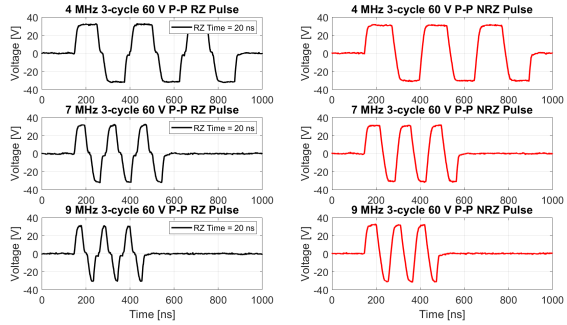


Fig. 14. Measured output voltage for different programmed pulse frequencies.

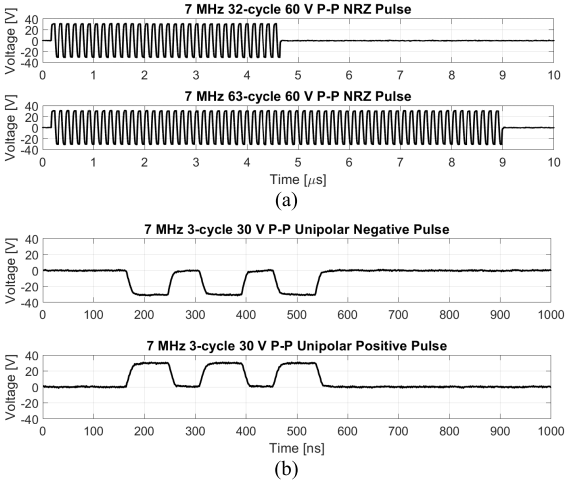


Fig. 15. Measured output voltage for (a) 7-MHz 32- and 63-cycle NRZ pulses and (b) 7-MHz 3-cycle 30-V unipolar negative and positive pulses.

with penetration depth by configuring the pulser to generate unipolar negative or positive pulses, as shown in Fig. 15(b). Note that there is some slew-rate mismatch between the rising and falling edges of the pulses. The associated second-order harmonic content of the pulse can be an issue in harmonic imaging, but this is not targeted in this work. If needed, slew-rate matching can be improved by optimizing the sizing of the HV pull-up or pull-down transistor, or by trimming their overdrive voltages by means of adjustable level shifters.

To electrically demonstrate the delay-control functionality of the beamformer, different start times are programmed into the shift registers of two channels in the ASIC. When the start

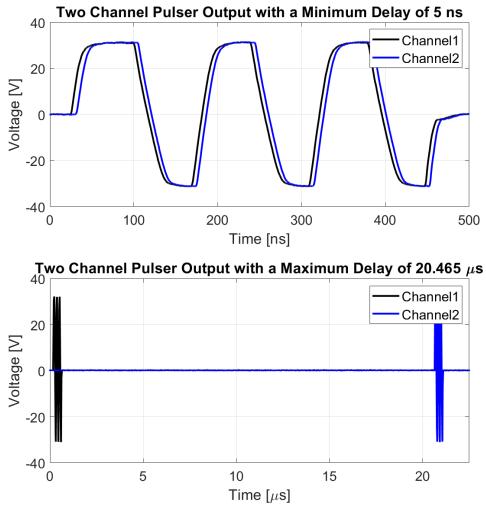


Fig. 16. Measured minimum and maximum delays of two pulser channels.

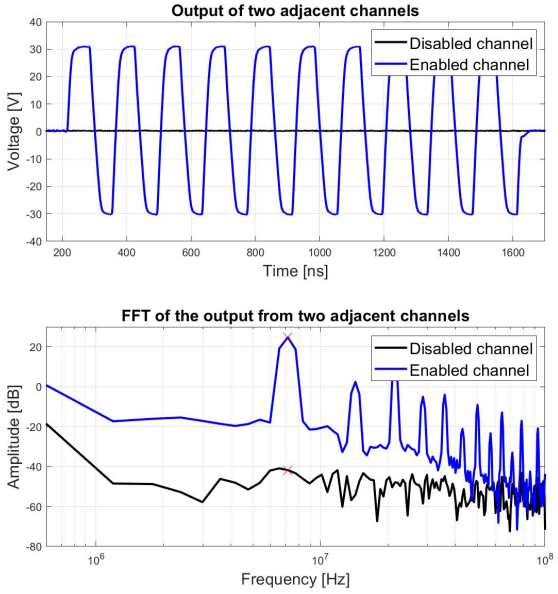


Fig. 17. Measured crosstalk between two adjacent channels.

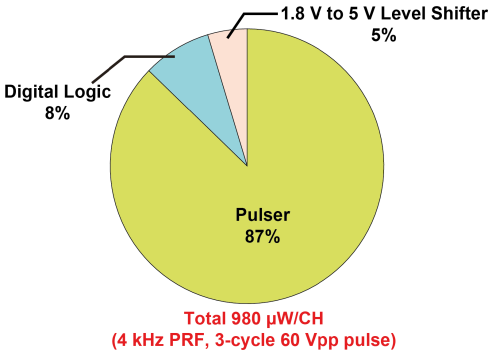


Fig. 18. Power-consumption breakdown.

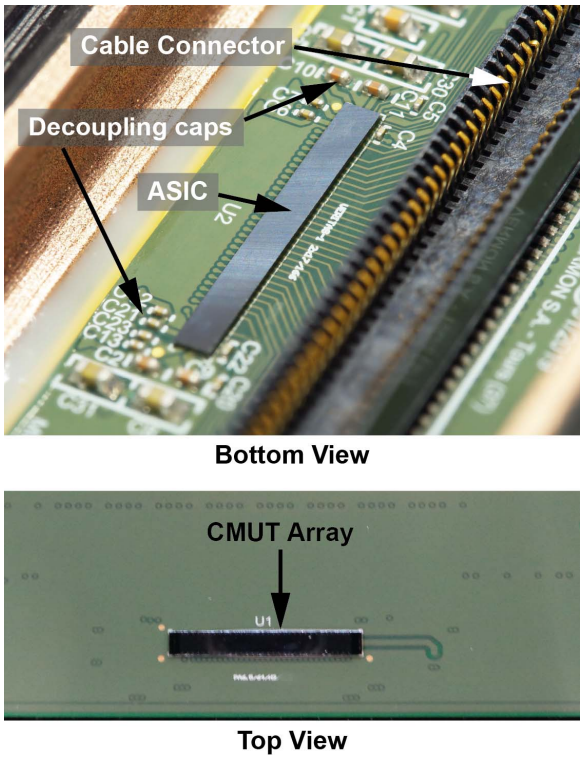


Fig. 19. Assembled ASIC-PCB-CMUT prototype.

time difference is set to a minimum value of 1 for channel 1 and channel 2, the measured delay is around 6.3 ns as shown in Fig. 16(a), which is slightly larger than the intended delay of 5 ns. When the start time difference is set to a maximum value of 4093 for channel 1 and channel 2, the measured delay is around 20.4714 $\mu$s as shown in Fig. 16(b), which is slightly larger than the intended value of 20.465 $\mu$s. The mismatch between the measured delay and intended delay is less than 5% of the cycle time of the 7-MHz pulses and has a negligible impact on the beamforming. It is likely caused by the imperfect clock distribution across the ASIC and mismatch of the level shifters among different channels.

Crosstalk performance has also been evaluated by disabling one channel and pulsing on an adjacent channel. The measured output voltages and the corresponding spectra of both channels are shown in Fig. 17. The measured crosstalk is around +66 dB at 7 MHz, which makes its impact on the beamforming negligible.

An important performance metric of the T/R switch is its ON-resistance. Since the T/R switch is placed in between the CMUT element and the transimpedance amplifier (TIA), its finite ON-resistance adds noise to the received echo signal. This should be smaller than the noise of the CMUT element (which in our design can be modeled as 18 pF//17 kΩ at resonance) so as to not degrade the noise figure. The measured ON-resistance of 180 Ω is in reasonable agreement with the simulated value of 155 Ω. At this level, the T/R switch increases the noise figure by 4.7 dB, which indicates that there is room for improvement by reducing the ON-resistance of the switches.

The ASIC power consumption is highly dependent on the PRF and the number of pulse cycles programmed. The power consumption of the TX circuitry strongly depends on the ultrasound imaging mode and is dominated by the dynamic power consumed in driving the transducer capacitance. The

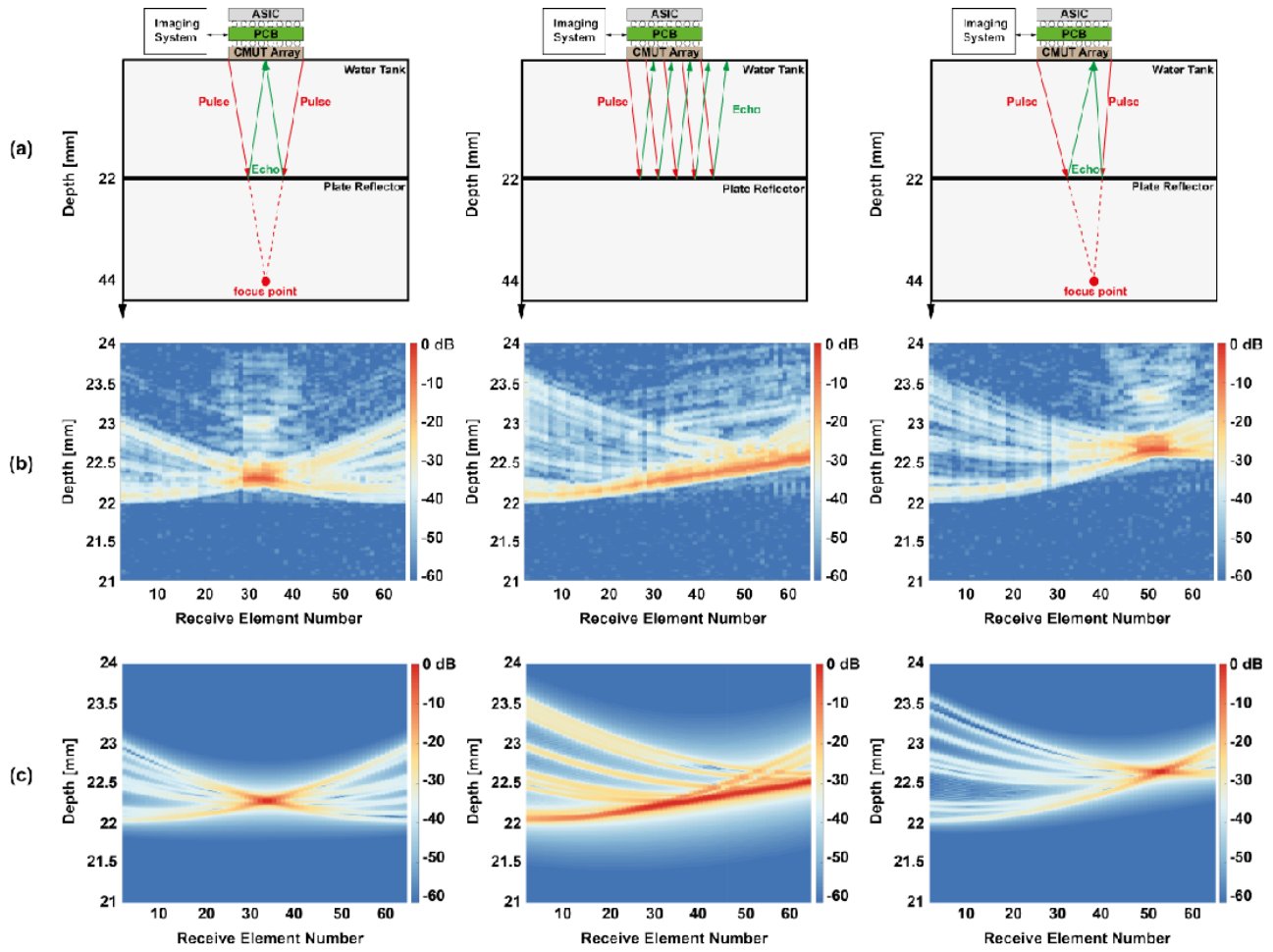


Fig. 20. Acoustic transmit beamforming experiment with a focused beam (left), a steered beam (middle), and a focused and steered beam (right). (a) Acoustic measurement setup with a sketch of the beam. (b) Measured echo signals from a pulse-echo experiment using the ASIC. (c) Simulated echo signals.

RX circuitry, which is described in more detail in [17], consumes on average 4.9 mW per channel. Fig. 18 shows the power breakdown for 3-cycle pulses at a PRF of 4 kHz. The total power per channel is then around 1 mW, which is dominated by the pulser.

### C. Acoustical Measurement Results

To acoustically evaluate the transmit beamforming, the ASIC and the CMUT transducer have been flip-chip mounted on two sides of a PCB, as shown in Fig. 19. To provide a test medium that is acoustically similar to the human body, this prototype was placed at the surface of a water tank, with the CMUT side immersed. Via a connector on the PCB, the ASIC was connected to power supplies, an FPGA that provides the clock and data signals to program the ASIC, and a Verasonics imaging system that records the received echo signals.

To demonstrate the beamforming capability, the ASIC was configured to drive the CMUT array so that it generates various ultrasound beams (focused, steered, and both), as shown in Fig. 20(a). A plate reflector was placed at 22 mm from the transducer array, causing the transmitted acoustic waves to reflect back to the transducer array, where they are recorded through the RX channels of the ASIC. As shown in Fig. 20(b), programming the TX beamformer to focus at 44 mm (round-trip distance between the transducer and the plate reflector) causes the reflected pulse to focus at the transducer array, as expected, even when steering delays are added. Transmission of a plane wave at an angle of 5° results in the reception of the expected reflected plane wave at the same angle. Fig. 20(c) shows, for comparison, echo signals that are simulated using DREAM MATLAB toolbox [20]. It should be noted that nine elements in the array were not working, which was also taken into account in the simulation. [These missing elements (spread across the array) are responsible for additional edge waves that can be observed in both the measurements and simulations.] The measurement results are in very good agreement with the simulations, confirming the correct operation of the beamformer.

Table I lists the comparison of the proposed HV pulser, floating-gate driver, and transmit beamformer with the prior art. Contrary to earlier pulsers [4], [19], this article provides embedded T/R switch functionality without increasing the number of the HV transistors. Note that an area comparison is somewhat arbitrary, given different pulser specifications and given that [4] uses SOI technology with smaller lateral dimensions for HV isolation than the junction-isolated technology

TABLE I
COMPARISON WITH THE PRIOR ART

| **HV 3-level Pulser** | | | |
|---|---|---|---|
| | **This Work** | JSSC'19 [4] | JSSC'13 [19] |
| Technology | **TSMC 180nm HV BCD** | XFAB 180nm HV SOI | TSMC 180nm HV CMOS[a] |
| T/R embedded | **Yes** | No | No |
| Bipolar pulse | **Yes** | Yes | No |
| # HV MOS[b] | **10** | 10 [c] | 10 [c] |
| # HV diodes | **0** | 2 | 0 |
| Max output | **60 $V_{pp}$** | 138 $V_{pp}$ | 30 $V_{pp}$ |
| Pulse freq. | **9 MHz @ 18pF** | 2 MHz | 3.3 MHz @ 40pF |
| Area | **0.167 mm²** | 0.09 mm² [d] | 0.33 mm² [d] |
| **Floating-Gate Driver** | | | |
| | **This Work** | ESSCIRC'18 [18] | JSSC'18 [5] |
| Technology | **TSMC 180nm HV BCD** | N/A | TSMC 180nm HV BCD |
| Application | **RZ & T/R switch** | HV switch (bipolar) | HV switch (unipolar) |
| # HV MOS | **1** | 3 | 1 |
| # HV diodes | **0** | 3 | 0 |
| # Passives[e] | **1** | 6 | 4 |
| **Transmit Beamformer** | | | |
| | **This Work** | TBCAS'18[11] | JSSC'19 [4] |
| Delay Resolution | **5 ns** | 5 ns | 25 ns |
| Delay Dynamic Range[f] | **72 dB** | 66 dB | 54 dB |
| # Channels | **64** | 64 | 3072 |

a) Gate-oxide can handle 30 V swing. b) Including HV MOS in level shifters c) excluding HV transistors in T/R switch. d) Area for RX circuitry also included. e) Capacitors, resistors and Zener diodes. f) Delay Dynamic Range = 20 · log10(max_delay / min_delay).

used in this article. We expect our proposed pulser topology is equally applicable in such technology and would provide an area benefit when optimized for the much smaller matrix transducer elements used in [4]. Moreover, the floating-gate driver requires fewer HV components than those used in earlier HV switches [5], [18]. The transmit beamformer achieves the same delay resolution of 5 ns and the same number of elements of 64 with the highest delay dynamic range of 74 dB.

## VI. CONCLUSION

This article has described a 64-channel transmit beamformer with programmable bipolar pulsers for catheter-based ultrasound probes. The transmit beamformer is programmed and configured through a single clock and data line to steer and focus an ultrasound beam at an angle and depth that are defined in the imaging system. The compact HV pulser design includes an RZ switch that has been constructed such that it can also serve as a T/R switch. A new floating-gate driver that uses only a single HV transistor provides level-shifting functionality to turn on and off the MOS transistors in the switch. Thus, the number of HV transistors and passive components required is reduced. The electrical and acoustical experimental results obtained in combination with a 64-element CMUT array successfully demonstrate the functionality of the HV pulser and TX beamformer.

## ACKNOWLEDGMENT

The authors thank Dominique Gross for his support on the acoustical simulations and the nice photographs he took.

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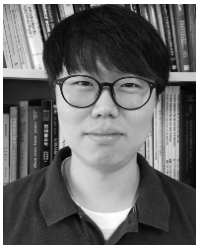

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