The Development of a Low-Stress Polysilicon Process Compatible with Standard Device Processing

Patrick J. French, Associate Member, IEEE, Bert P. van Drieënhuizen, Student Member, IEEE, Daniel Poenar, Student Member, IEEE, Johannes F. L. Goosen, Student Member, IEEE, Rolf Mallée, Pasqualina M. Sarro, Member, IEEE, and Reinoud F. Wolffenbuttel, Member, IEEE

Abstract-When surface micromachined devices are combined with on-chip circuitry, any high-temperature processing must be avoided to minimize the effect on active device characteristics. High-temperature stress annealing cannot be applied to these structures. This work studies the effects of deposition parameters and subsequent processing on the mechanical properties of the polysilicon film in the development of a low-strain polysilicon process, without resorting to high-temperature annealing. The films are deposited as a semi-amorphous film and then annealed, in situ at 600°C for 1 h, to ensure the desired mechanical characteristics for both doped and undoped samples. This low temperature anneal changes the strain levels in undoped films from -250 to $+1100 \ \mu \epsilon$. The best results have been obtained for an 850°C anneal for 30 min which is used to activate the dopant (both phosphorus and boron). No further stress annealing was used, and 850°C does not present problems in terms of thermal budget for the electrical devices. It is shown that these mechanical characteristics are achieved by forming the grain boundaries during subsequent low temperature annealing, and not during deposition. TEM (transmission electron microscopy) studies have been used to investigate the link between the structure and mechanical strain. This has shown that it is the formation of the grain boundary rather than the grain size which has a significant effect on strain levels, contrary to reports in the literature. Using the above-mentioned deposition process, a series of experiments have been performed to establish the flexibility in subsequent processing available to the designer. Therefore, by careful consideration of the processing, a low-temperature polysilicon process, which can be used to fabricate thin micromachined structures, has been developed. [138]

I. INTRODUCTION

POLYSILICON is a material frequently used for both electronics and sensors. In the field of electronics it has been applied to polysilicon emitter bipolar [1], polysilicon gate MOS [2], and interconnects. Since the piezoresistive effect in polysilicon was first studied in the early 1970's [3], there have been many studies of its electrical [4]–[6] and piezoresistive properties [7]–[10]. A review of the use of polysilicon for integrated circuit applications is given by Kamins [11]. In a

Manuscript received January 13, 1995; revised January 18, 1996. Subject Editor, S. D. Senturia. This work was supported in part by FOM/STW under Projects DEL 99.2136 and DEL 11.2524.

P. J. French, B. P. van Drieënhuizen, D. Poenar, J. F. L. Goosen, and R. F. Wolffenbuttel are with DIMES, Department of Electrical Engineering, Laboratory for Electronic Instrumentation, Delft University of Technology, 2600 GA, Delft, The Netherlands.

R. Mallée and P. M. Sarro are with DIMES, Department of Electrical Engineering, Laboratory of Electronic Components Technology and Materials, Delft University of Technology, 2600 GB Delft, The Netherlands.

Publisher Item Identifier S 1057-7157(96)06838-2.

surface micromachining process it is important to control the strain levels in the mechanical layers.

To fabricate freestanding surface-micromachined structures, it is often desirable to construct the structures in materials which have low tensile intrinsic strain. Films in compressive strain tend to buckle, causing severe limitations on the dimensions of freestanding structures. High tensile strain is also unsuitable as it may result in fracturing of structures.

Processing parameters have a considerable effect on the electrical and mechanical properties of polysilicon [5], [10]. Directly after deposition, polysilicon is usually in compressive strain. This can be minimized by depositing layers with a dominant grain orientation such as $\langle 111 \rangle$ [12], which greatly reduced the strain, although these films were still in compressive strain. Intrinsic compressive strain can be released by high temperature annealing (>1000°C) [13], but this is not compatible with standard silicon processing. It is therefore necessary to develop a process where low tensile strain can be achieved without any high-temperature steps.

One method to avoid this high thermal budget is to employ rapid thermal annealing (RTA) [19]. Although this entails a high temperature (1150°C), the time of the anneal is only 3 min and therefore does not adversely affect the electronics. This was successful in reducing the strain but created additional problems for the phosphosilicate glass (PSG) and modifications to the PSG had to be made. RTA processing presented by Ristic *et al.* [20] used temperatures from 850–1050°C and a maximum time of 5 min. In this work, no problems with the PSG was presented.

An *in situ* anneal directly after deposition was first proposed by Guckel *et al.* [21], [22]. An anneal temperature of 600°C for 3 h was found to remove all the compressive strain. Alternatively, an *in situ* anneal of 850°C for 30 min was used to achieve strain levels of 2500 $\mu\varepsilon$ for film of thickness 2 μ m. To achieve a lower tensile strain a higher temperature anneal was used. This low temperature anneal presented a considerable improvement over previously used techniques and was therefore included in these studies.

Recently cross-sectional TEM (transmission electron microscopy) studies have been used to correlate the microstructure with the mechanical properties [23]–[26]. These showed the differences in mechanical properties of columnar and noncolumnar structure and further confirmed the importance of film texture previously reported [12]. Furthermore the film contraction of films during crystallization, resulting in a shift from compressive to tensile strain, was examined [26].

1057-7157/96\$05.00 © 1996 IEEE

Processing parameter	Range
Dopant type	Boron/phosphorus
Implant energy	40-100keV
Implant dose	$5x10^{14}$ cm ⁻² , $1x10^{15}$ cm ⁻² or $5x10^{15}$ cm ⁻²
Post implant anneal	(850°C - 1100°C), 30 minutes in N ₂

TABLE I PROCESS VARIABLES INVESTIGATED

The studies presented here have included the effect of deposition temperature [27], in situ annealing [21], [22], doping, and post implant annealing [27]. The studies have also included the effect of changes in the processing for the underlying, sacrificial layer. From these studies, processes yielding the desired strain and freestanding structures for thin polysilicon films ($<0.5 \mu$ m), with a small air gap (0.4–0.6 μ m) have been developed. A further important consideration for the designer is the degree of flexibility available. For this reason the study has been extended to the effect of subsequent processing parameters such as ion implantation energy, doping concentration, and post anneal temperature. Most of these studies in the literature have concerned phosphorus doped silicon (for an example of the effect of phosphorus doping see [28]), although there have been examples of boron doping [29]. To complete the investigation into process flexibility, this study also included a detailed study of boron doped material.

Throughout these studies the effect of the polysilicon processing on bipolar circuitry was the main consideration.

II. PROCESSING

Sacrificial layers of 4000–6000 Å thickness were formed by PSG deposition. Undoped thermal oxides, using oxidized polysilicon, have also been examined as a sacrificial material and although some differences were found, the mechanical properties of the subsequently deposited polysilicon were similar. An important consideration for surface micromachining is the under-etch rate in hydrofluoric acid (HF) of the sacrificial material. PSG has the advantage of a higher under etch rate with values up to 30 μ m/min, in 20% HF (40% HF : H₂O 1 : 1), having been achieved for PSG [30] compared to 0.2 μ m/min for oxidized polysilicon. The PSG process used in this work had a phosphorus content of 3% which yielded an under-etch rate of 5.5 μ m/min [30].

Polysilicon films of 4000 Å were deposited, to form the mechanical structures, using a Tempress PROMAGA-M diffusion LPCVD system (2000 Å and 7500 Å films were also examined for comparison). The reactor pressure and the silane flow were kept constant throughout the experiments at values of 150 mtorr and 45 sccm, respectively, for a tube diameter of 15 cm. The temperature range of deposition was 560–610°C yielding deposition rates between 25–50 Å/min. Once the optimum deposition temperature had been established, further depositions were followed by an *in situ* anneal in nitrogen to adjust the mechanical properties of the material. This anneal was performed at 600°C in the LPCVD reactor in an N₂ flow at a pressure of 150 mtorr. This anneal is only effective if the polysilicon structure is not formed during deposition and the film is semi-amorphous. Once the structure is polysilicon, temperatures above 1000°C are required to significantly change the structure. Once a deposition process had been established, the flexibility to subsequent processing was examined. The processing variables are summarized in Table I.

The polysilicon was patterned by plasma etching and the sacrificial oxide removed using 20% HF.

III. STRAIN MEASUREMENT TECHNIQUES

There have been a variety of stress/strain measurement methods presented in the literature. One technique is wafer curvature [28], [31], where the curvature of the wafer is measured before deposition and after the layer has been deposited and stripped from the backside. In micromachining it is advantageous to be able to measure micromachined structures which have experienced the same processing as the device. The buckling technique is based on the maximum length of a beam which will remain unbuckled under compressive strain [17]. This has been modified to be able to measure tensile strain [21]. There are two disadvantages of the buckling technique. The first is the requirement of an array of devices, which consumes chip area, and the second is that the accuracy is dependent upon the step size in the array. A single structure, which measured the displacement of a junction between wide and narrow beams, has been developed to avoid this problem [32]. When measuring low strain levels, however, this displacement is extremely small and therefore difficult to measure.

For these studies a technique has been developed and tested to measure the strain in micromachined structures, and these have been described elsewhere [33]. The structure is basically a pointer where the expansion of two beams is converted into the rotation of a third beam, as shown in Fig. 1(a). This structure can be used to measure both compressive and tensile strain and furthermore, the displacement of the tip is sufficiently large that low strain levels can be measured using an SEM. This measurement structure measures strain FRENCH et al.: DEVELOPMENT OF LOW-STRESS POLYSILICON PROCESS



(a)

(b)



(c)

Fig. 1. (a) Planar view of strain measurement structure, (b) SEM photograph of the end of the pointer, and (c) SEM photograph of the turning point.

and therefore knowledge of Young's modulus is not required. SEM photographs of a released pointer and turning point are illustrated in Fig. 1(b) and (c), respectively.

In the ideal case, the turning point has no effect on the strain, ε , and the rotation is a direct measure of the strain. This is not the case, however, and a correction factor, K, is required; the strain is therefore given in terms of the displacement of the tip, y, by

$$\varepsilon = \frac{Oy}{K\left[(2L_1 + O) + \frac{A + W}{2}\right]}$$

where the other parameters are defined in Fig. 1(a). Computer simulations have been used to calculate the effect of the turning point thickness, K, on the measured value of rotation. Through these simulations a correction factor has been calculated to compensate for this error. A more detailed description of the use of the correction factor has been presented elsewhere [33]. In these experiments the following dimensions were used:

 $L_1 = 60 \,\mu \mathrm{m}$ $O = 5 \,\mu \mathrm{m}$ $A = 45 \,\mu \mathrm{m}$ $W = 8 \,\mu \mathrm{m}$

and a turning point width of 1, 2, and 3 μ m.

IV. MEASUREMENT RESULTS

As mentioned above, initial studies concerned the development of an optimum polysilicon process. The main criteria was the effect of strain levels, although sheet resistance was also of interest. Firstly, a deposition process yielding the desired strain levels for both doped and undoped material was investigated. Once this process was established a more detailed examination of phosphorus and boron doping was performed, thus resulting in a complete characterization of the polysilicon process.

A. Deposition Parameters

Deposition temperature is known to have a strong effect on both the electrical and mechanical properties of polysilicon.

Above a certain temperature, which depends on both pressure and gas flows, for a given reactor, the films are deposited as polysilicon with fully formed grains and grain boundaries. The grain boundary is the thin region (of a few atoms thickness) required to change from one crystal orientation to another [10], [11]. Below this transition temperature a semi-amorphous film is deposited. In this case grains are formed but separated from each other by an amorphous region. The effect of this transition on sheet resistance of doped polysilicon, deposited on oxidized polysilicon, is shown in Fig. 2(a). An implantation dose of $1 \times$ 10^{15} cm⁻² was chosen for this test to achieve high sensitivity to changes in the polysilicon structure. Lower doping levels have a still higher sensitivity to changes in the polysilicon structure, but these films have a high sheet resistance and thus have fewer practical applications. The sharp transition is due to a change in the barrier height at the grain boundary [10]. A sharp transition was also found in the measured strain as shown in Fig. 2(b). It can be seen that the transition is slightly higher for strain than for sheet resistance. This is likely due the narrowing of the grain boundary causing a change in the electrical characteristics before a change in the mechanical characteristics.

Depositing as semi-amorphous ensured that the thin grain boundary was formed by annealing and not during deposition, which reduced the strain contribution from the grain boundary. Furthermore, the resulting small grains lead to improved strain distribution, greater repeatability, and a smoother surface (the last factor is of particular importance where moving parts are required). The structure of the polysilicon has been confirmed using TEM, and this is discussed in Section V. It can be seen from Fig. 2(b) that a further reduction in deposition temperature, within the range under consideration here, does not greatly effect the strain levels. Thus, maintaining a deposition temperature as close to the transition as possible maximizes the deposition rate while maintaining the desired mechanical properties. Films deposited near, but above, the transition temperature, where the grain size was small, were also found to have the higher compressive strain.

Films deposited below the transition and subsequently doped by implantation and annealed at 850°C were found to be in tensile strain, whereas those deposited above this temperature were still in compressive strain even after doping and annealing.

As shown in Fig. 2(b), undoped and unannealed films were in compressive strain for all deposition temperatures. A low temperature, 600°C, *in situ* anneal as short as 30 min was sufficient to have a significant effect on the strain levels in the films resulting in a change from a compressive strain of $\sim -300 \,\mu\varepsilon$ to a tensile strain of $\sim +1000 \,\mu\varepsilon$ for undoped films (see Fig. 3). Higher anneal temperatures were investigated but this did not result in any further improvement. Temperatures lower than 600°C are also not suitable as this may not complete the crystallization process. As expected doped films were less influenced by the use of the *in situ* anneal. The sheet resistance of the doped films was found to increase when an *in situ* anneal was used. This is due to the fact that the implantation was into a polysilicon structure, rather than the semi-amorphous phase. The measured strain for these





Fig. 2. Effect of deposition temperature on: (a) polysilicon sheet resistance and (b) the measured strain. Doped samples were implanted with phosphorus at an implant dose of 1×10^{15} cm⁻², and a post implant anneal of 850°C for 30 min in N₂. The underlying layer was thermal oxide.

films is shown in Fig. 3. Once again, if the grain boundary is not formed during deposition, low temperatures can be used to remove any compressive strain. If a polysilicon structure is formed during deposition, such a low temperature anneal cannot be used as temperatures above 1000°C are required to significantly change the structure.

Although the *in situ* anneal is not essential if the film is later implanted and annealed, it was incorporated into the standard process to achieve repeatable tensile strain in both doped and undoped material. Therefore the standard process was chosen as:

deposition temperature: 575°C;

in situ anneal: 600°C, 60 min.

An SEM photograph of a released structure, using the above described process, is shown in Fig. 4. In this case both the film thickness and the air gap are 4000 Å.

To fully characterize the process, a more detailed study of the effect of doping and anneal was required, and these are discussed below. In all further studies the deposition temperature and *in situ* anneal were kept constant.



Fig. 3. Measured strain as a function of *in situ* anneal time at a temperature of 600°C for films deposited at 575°C. Doped films were implanted with phosphorus at 1×10^{15} cm⁻², and annealed of 850°C for 30 min in N₂.



Fig. 4. SEM photograph showing released surface micromachined structure using optimized process.

B. Doping Level

In the above section a process has been established which yields the desired mechanical properties for both doped and undoped films. For the process designer it is important to know the flexibility in subsequent processing. In this section the effect of phosphorus and boron doping by implantation is examined in detail.

The effect of implantation energy and implant dose was examined for film deposited at 575°C and using an in situ anneal of 60 min at 600°C. The implant doses and energies used in this test were as follows:

implantation dose (cm⁻²): 5×10^{14} , 1×10^{15} , and 5×10^{15} ; implantation energy (keV): 25, 40, 80, and 100.

A post-implant anneal of 850°C for 30 min in N₂ was used for all devices. The sheet resistance as a function of implantation energy for the three implantation doses are shown in Fig. 5(a). The resistance is relatively independent of implant energy for the range used in these experiments. For higher energies or thinner films an increase was found due to loss of dopant in the underlying oxide. As expected, this effect is



more pronounced for boron than for phosphorus due to the higher implantation depth. The strain measurements revealed no measurable difference in the strain levels for the range considered as illustrated in Fig. 5(b). The strain is also relatively

Fig. 5. Effect of implant energy on: (a) polysilicon sheet resistance and (b)

measured strain for an implant dose of 1×10^{15} cm⁻² and a post implant

40

Implant Energy [keV] (b)

60

80

100

independent of doping levels as shown in Fig. 6. Thus using this process the polysilicon can be doped with both phosphorus and boron and is relatively independent of both implant dose and implant energy, within the range investigated in this work.

C. Post Implant Anneal

400 200 0

n

anneal of 850°C for 30 min in N2.

20

A range of post implantation annealing temperatures (850-1100°C) were investigated. The effect on sheet resistance, for polysilicon films deposited on both oxidized polysilicon and PSG, is shown in Fig. 7(a). The rise in sheet resistance for the higher anneal temperatures is most likely due to loss of dopant, as these layers were not capped during annealing. This is more pronounced with the thermal oxide substrate as the PSG serves as an extra dopant source. This effect has been discussed elsewhere [30] and has also been noted by Ristic et al. [20].

Wafers Film thickness (Å)	Film	Implantation		Anneal
	dose (cm ⁻²)	Energy (keV)		
a	4000	-	-	-
b	4000	-	-	850°C, 30 mins
с	4000	1x10 ¹⁵	40	850°C, 30 mins

 TABLE II

 PROCESSING VARIATIONS USED FOR MEASURING DOPING PROFILES IN POLYSILICON FILM



Fig. 6. Measured strain as a function of implant dose, with an energy of 80 keV, for the optimized polysilicon deposition process and a post implant anneal of 850°C for 30 min in N_2 .

Fig. 7(b) shows the measured strains for films deposited at 570°C (below the transition) and 610°C (above the transition) as a function of anneal temperature after doping by phosphorus implantation at a dose of 1×10^{15} cm⁻², using both thermal oxide and PSG as a sacrificial material. For films deposited as semi-amorphous, strain levels were found to reduce with increasing anneal temperature, crossing over to a compressive strain at anneal temperatures above 1000°C. The strain levels for the 850°C anneal were satisfactory, however, and the most compatible with other processing. For depositions above the transition temperature, the films were in compressive strain for all anneal temperatures, although the strain approached zero as the anneal temperature was increased. This shows that if the deposition parameters are not optimized, hightemperature annealing as reported in the literature [13], [14] is indeed required to remove the compressive strain. Further investigations have been carried out on the effect of the PSG processing on the polysilicon, and these results have been published elsewhere [30]. This showed that, due to outdiffusion during annealing, higher phosphorus levels in the PSG resulted in a lower polysilicon sheet resistance. The strain levels, however, were relatively unaffected.

D. Strain Profiles

A further important factor is the strain profile through the film, and this effects the flatness of single supported structures







Fig. 7. Effect of post implant anneal on: (a) polysilicon sheet resistance and (b) measured strain. In all cases an implant dose of 1×10^{15} cm⁻², phosphorus was used for films deposited on both oxidized polysilicon [curves a, Fig. 7(b)] and PSG [curves b, Fig. 7(b)].

after etching. To give some indication of this profile, four wafers were processed as shown in Table II. All wafers were processed using the 575°C deposition and 600°C *in situ* anneal.

After doping and annealing, the polysilicon was thinned in three of the four quarters of the wafer to yield film thicknesses of 4000, 3000, 2500, and 2000 Å. The polysilicon was then patterned and the strain measured, and these measurements are



Fig. 8. Measured strain for thinned polysilicon layers for: a—undoped with no further processing, b—undoped but with an 850°C anneal, and c—implanted with phosphorus (1 $\times 10^{15}~{\rm cm^{-2}})$ and annealed at 850°C.



Fig. 9. Single ended beams of length 100 μ m and thickness 4000 Å. These beams were implanted with phosphorus with a dose of 1×10^{15} cm⁻² and energy 40 keV followed by an anneal of 30 min at 850°C.

shown in Fig. 8. This shows how the anneal has considerably reduced the profile, and in the case of doped samples no profile could be seen. Fig. 9 shows 100 μ m long, 4000 Å thick single ended beams. These beams were implanted with phosphorus with a dose of 1×10^{15} cm⁻² and energy 40 keV followed by an anneal of 30 min at 850°C. Minimal deflection out of the plane was found.

Although a standard thickness of 4000 Å was used throughout this work, films of 2000 and 7500 Å were also examined for comparison. Fig. 10 shows the measured strain as a function of film thickness for both doped and undoped films. As with the strain profile measurements, shown in Fig. 8, undoped films show a greater effect than doped films.

V. MATERIAL STUDIES

In Section IV the effect of all processing steps on the mechanical strain in the polysilicon has been characterized.



Fig. 10. Measured strain as a function of films thickness for undoped films and films implanted with phosphorus, $\times 10^{15}$ cm⁻², and annealed at 850°C.







(b)

Fig. 11. Film deposited at 570° C and no further processing: (a) a TEM photograph and (b) X-ray diffraction rings.

To correlate the relationship between crystal structure and mechanical strain TEM was used. Polysilicon films were



(a)



(b)

Fig. 12. Film deposited at 570°C after an in situ anneal at a temperature of 600°C for 1 h: (a) a TEM photograph and (b) x-ray diffraction rings.

completely under-etched in HF and floated off onto TEM sample grids. X-ray diffraction patterns of doped and undoped samples showed no dominance by a small number of crystal orientations, indicating that crystal orientations were not responsible for differences in mechanical strain. This shows a difference in structure from the films studied by Krulevitch et al. [26] where films were dominated by a small number of crystal orientation and a change in the texture corresponded to a change in strain levels. Therefore a similar transition in strain levels has been found in this work without the corresponding change in film texture. Fig. 11(a) and (b) show the x-ray diffraction rings and microphotograph, respectively, of films deposited at 570°C, with no further processing. The x-ray diffraction results shown in Fig. 11(a) reveal some rings indicating the presence of a number of grains but these rings are not sharp due to the presence of amorphous material. If the same film is annealed, in situ at 600°C for 1 h. it is converted into a full polysilicon structure as shown in Fig. 12(a) and (b). For these films the x-ray rings are clearly defined with the bright spots indicating the presence





Fig. 13. Film deposited at 610°C and no further processing: (a) a TEM photograph and (b) x-ray diffraction rings.

of a number of large grains. The average grain size was estimated to be 1000 Å. Films deposited at 610°C were found to have an average grain size of 800 Å, and these films are shown in Fig. 13(a) and (b). The x-ray rings, shown in Fig. 13(a), reveal that there are fewer large grains than found for the films shown in Fig. 12 and the film has a relatively uniform grain size. Neither film was changed greatly after doping and annealing at 850°C but the film in Fig. 13 displayed a considerable reduction in strain levels, although still compressive. Extensive TEM examinations of various films have revealed no connection between grain size and strain. Considerably larger grains were formed by depositing films below the transition and annealing at 1100°C for 30 min, as shown in Fig. 14. The grain size was estimated to be 2200 Å. Strain measurements showed a strain level similar to that of the films shown in Fig. 13, but the grain structure is obviously quite different.

Depositing as a semi-amorphous film and annealing at 600°C resulted in a film similar in structure to the polysilicon



Fig. 14. TEM photograph rings of a film deposited at 570°C, implanted with phosphorus to a dose of 1×10^{15} cm⁻² and annealed at a temperature of 1100°C for 30 min.

deposited samples, but in tensile strain. The material studies have confirmed that it is the grain boundary formation rather than the grain size which is the main factor in determining the strain. The film contraction due to crystallization of the amorphous regions between grains which is in agreement with the work of Krulevitch et al. [26]. This work has shown that the grain size, within the range of values measured here, has no effect on the strain, contrary to need for small grain suggested in the literature [18]. When the grain boundaries are not formed at deposition, the films were found to be in low compressive strain. These amorphous areas between grains can be crystallized at low temperatures relieving the compressive strain and pulling the films into tensile strain. Further processing such as doping and annealing at 850°C has little effect on the grain size but changes the strain levels due to dopant incorporation in the film and adjustments to the grain boundary. The film, however, remains in tensile strain.

VI. CONCLUSIONS

The effect of processing parameters on the film structure and the built-in strain of polysilicon films has been studied. These tests have indicated that the formation of the grain boundary is the major factor in determining the strain. Deposition as a semi-amorphous material, and thus not forming the grain boundaries during deposition, results in a low compressive strain. This can easily be converted to a tensile strain by low temperature (600°C for 30 min) annealing. Subsequent processing such as doping and annealing (850°C) further modifies the strain levels but the films remain in low tensile strain. Films deposited as polysilicon can yield small grains but the high compressive strain in the films must be removed using high temperature annealing. Therefore the grain size appears not to be the major factor in determining the strain levels, as frequently quoted in the literature. Therefore, by careful consideration of the deposition parameters, satisfactory levels of strain have been achieved with anneal temperatures and film thicknesses compatible with on-chip circuitry processing.

ACKNOWLEDGMENT

The authors wish to thank the members of DIMES for their help in fabrication of the devices. Thanks are also due to D. de Haan of Materials Research, TU Delft, for performing the TEM analysis.

REFERENCES

- [1] P. Ashburn, D. J. Roulston, and C. R. Selvakumar, "Comparison of experimental and computed results on arsenic- and phosphorus-doped polysilicon emitter bipolar transistors," IEEE Trans. Electron Devices, vol. ED-34, pp. 1346–1353, 1987.
 [2] H. Mikoshiba, "Stress-sensitive properties of silicon gate MOS devices,"
- Solid State Electron., vol. 24, pp. 221-232, 1981.
- Y. Onuma and K. Sekiya, "Piezoresistive properties of polycrystalline [3] silicon thin films," Jpn. J. Appl. Phys., vol. 11, pp. 420-421, 1974.
- [4] J. Y. W. Seto, "The electrical properties of polycrystalline silicon films,"
- J. Appl. Phys., vol. 46, pp. 5247–5254, 1975. [5] M. M. Mandurah, K. C. Saraswat, and T. I. Kamins, "A model for conduction in polysilicon: Part 1-Theory, Part 2-Comparison of theory and experiment," IEEE Trans. Electron Devices, vol. ED-28, pp. 1163-1176, 1981.
- [6] N. G. C. Lu, L. Gerzberg, C.-Y. Lu, and J. D. Meindl, "Modeling and optimization of monolithic polycrystalline silicon resistors," IEEE Electron Devices, vol. ED-28, pp. 818-830, 1981.
- [7] J. Y. W. Seto, "Piezoresistive properties of polycrystalline silicon films," J. Appl. Phys., vol. 47, pp. 4780-4783, 1976.
- [8] O. Dössel, "Longitudinal and transverse gauge factors of polycrystalline silicon gauges," Sens. Actuators, vol. 6, pp. 169-179, 1984.
- P. J. French and A. G. R. Evans, "Polycrystalline silicon as a strain [9] gauge material," J. Phys. E, vol. 19, pp. 1055-1058, 1986.
- [10] "Piezoresistance in polysilicon and its applications to strain gauges," Solid State Electron., vol. 32, pp. 1-10, 1989.
- T. I. Kamins, Polycrystalline Silicon for Integrated Circuit Applications. [11] Norwell, MA: Kluwer, 1988.
- L.-S. Fan and R. S. Muller, "As-deposited low-strain LPCVD polysili-[12] con," in Tech. Digest, IEEE Solid-State Sensors and Actuators Workshop, Hilton Head Island, SC, June 1988, pp. 55–58.
 [13] K. L. Yang, D. Wilcoxen, and G. Gimpelson, "The effects of post
- processing techniques and sacrificial layer materials on the formation of free standing polysilicon microstructures," in Proc. IEEE Micro-Mechanical Systems, UT, Feb. 20-22, 1989, pp. 66-70.
- R. S. Hajab and R. S. Muller, "Residual strain effects on large aspect [14] ratio micro-diaphragms," in Proc. IEEE Micro Electro Mechanical Systems Conf. (MEMS), Salt Lake City, UT, Feb. 20-22, 1989, pp. 133-138.
- [15] R. T. Howe and R. S. Muller, "Polycrystalline and amorphous silicon micromechanical beams: Annealing and mechanical properties," Sens. Actuators, vol. 4, pp. 447-454, 1983.
- [16] 'Stress in polycrystalline and amorphous silicon thin films," J. Appl. Phys., vol. 54, pp. 4674-4675, 1983.
- H. Guckel, T. Randazzo, and D. W. Burns, "A simple technique for the determination of mechanical strain in thin films with applications to polysilicon," J. Appl. Phys., vol. 57, pp. 1671-1675, 1985.
- [18] H. Guckel, D. W. Burns, C. R. Rutigliano, D. K. Showers, and J. Uglow, "Fine grained polysilicon and its application to planar pressure transducers," in Proc. Transducers 87, Tokyo, 1987, pp. 277-282
- [19] M. W. Putty, S.-C. Chang, R. T. Howe, A. L. Robinson, and K. D. Wise, "Process integration for active polysilicon resonant microstructures," Sens. Actuators, vol. 20, pp. 143-151, 1989.
- [20]L. Ristic, M. L. Kniffin, R. Gutteridge, and H. G. Hughes, "Properties of polysilicon films annealed by a rapid thermal annealing process," Thin Solid Films, vol. 220, pp. 106-110, 1992.
- H. Guckel, D. W. Burns, C. C. G. Visser, H. A. C. Tilmans, and D. [21] Deroo, "Fine grained polysilicon films with built-in tensile strain," IEEE Trans. Electron Devices, vol. 35, pp. 800–801, 1988. [22] H. Guckel, J. J. Sniegowski, T. R. Christenson, S. Mohney, and T. F.
- Kelly, "Fabrication of micromechanical devices from polysilicon films with smooth surfaces," Sens. Actuators, vol. 20, pp. 117-122, 1990.
- [23] P. Krulevitch, R. T. Howe, G. C. Johnson, and J. Huang, "Stress in undoped LPCVD polycrystalline silicon," in Proc. Transducers 91, San Francisco, June 1991, pp. 949–952. P. Krulevitch, T. D. Nguyen, G. C. Johnson, R. T. Howe, H. R.
- [24] Wenk, and R. Gronsky, "LPCVD polycrystalline silicon thin films: The evolution of structure, texture and stress," in Proc. Mat. Res. Soc. Symp., 1991, pp. 167-172.

- [25] P. Krulevitch, G. C. Johnson, and R. T. Howe, "Stress and microstructure in phosphorus doped polycrystalline silicon," in *Proc. Mat. Res. Soc. Symp.*, San Francisco, 1992, pp. 79–84.
- [26] _____, "Stress and microstructure in LPCVD polycrystalline silicon films: Experimental results and closed form modeling of stresses," in *Proc. Mat. Res. Soc. Symp.*, San Francisco, 1992, pp. 13–18.
- [27] P. J. French, B. P. van Drieënhuizen, D. Poenar, J. F. L. Goosen, P. M. Sarro, and R. F. Wolffenbuttel, "Low-stress polysilicon process compatible with standard device processing," in *Proc. Sensors and Applications VI*, Manchester, UK, Sept. 1993, pp. 129–134.
- [28] S. P. Murarka and T. F. Retajczyk, Jr., "Effect of phosphorus doping on stress in silicon and polycrystalline silicon," *J. Appl. Phys.*, vol. 54, pp. 2069–2072, 1983.
- [29] M. S. Choi and E. W. Hearn, "Stress effects in boron-implanted polysilicon films," *J. Electrochem. Soc.*, vol. 131, pp. 2443–2446, 1984.
 [30] D. Poenar, P. J. French, R. Mallée, P. M. Sarro, and R. F. Wolffen-
- [30] D. Poenar, P. J. French, R. Mallée, P. M. Sarro, and R. F. Wolffenbuttel, "PSG for surface micromachining," Sens. Actuators, vol. 41, pp. 304–309, 1994.
- [31] R. Glang, R. A. Holmwood, and R. L. Rosenfeld, "Determination of stress in films on single crystalline silicon substrates," *Rev. Sci. Instr.*, vol. 36, pp. 7–10, 1965.
- [32] M. G. Allen, M. Mehregany, R. T. Howe, and S. D. Senturia, "Microfabricated structures for the in situ measurement of residual stress, Young's modulus and ultimate strain of thin films," *Appl. Phys. Lett.*, vol. 51, pp. 241–243, 1987.
- [33] B. P. van Drieënhuizen, J. F. L. Goosen, P. J. French, and R. F. Wolffenbuttel, "Comparison of techniques for measuring both compressive and tensile stress in thin films," *Sens. Actuators*, vol. A37-38, pp. 756–765, 1993.

Patrick J. French (M'95–A'96) received the B.Sc. degree in mathematics and the M.Sc. degree in electronics from Southampton University, UK, in 1981 and 1982, respectively. In 1986, he obtained the Ph.D. degree, also from Southampton University, which was a study of the piezoresistive effect in polysilicon.

After 18 months as a Post-Doctoral at Delft University, The Netherlands, he moved to Japan in 1988. For three years, he worked on sensors for automobiles at the Central Engineering Laboratories of Nissan Motor Company, in Yokosuka, Japan. He returned to Delft University in May, 1991, and is now a staff member of the Laboratory for Electronic Instrumentation with interests in micromachining and process optimization related to sensors.

Bert P. van Drieënhuizen (S'95) received the M.Sc. degree (cum laude) in electrical engineering from Delft University of Technology, The Netherlands, in 1991, his diploma work dealing with optical isolating amplifiers based on silicon avalanche light emission.

Since 1991, he has been working toward the Ph.D. degree, at the Laboratory for Electronic Instrumentation, in the field on micromachined sensors and actuators. His research is concentrated on an electrostatic RMS-to-DC converter, fabricated in a BiFET-compatible surface micromachining process. **Daniel Poenar** (S'95) was born in Bucharest in 1964. He received the M.Sc. degree in electrical engineering in 1989 from the Polytechnic University, Bucharest, Romania, where his thesis dealt with functional integration of bipolar-MOS power devices. Since November, 1991, he has been working toward the Ph.D. degree at the Laboratory for Electronic Instrumentation on thin film color sensors.

Johannes F. L. Goosen (S'95) was born in The Netherlands in 1966. He received the Electrical Engineering degree in 1991 from the Delft University of Technology, Delft, The Netherlands, and is currently working toward the Ph.D. degree at the Electronic Instrumentation Laboratory of this University. The work concerns the design of a positioning device using a distributed system of electrostatically driven, surface micromachined actuators. He is also closely involved in the development of a two-layer surface micromachining process compatible with standard electronic processing, for the fabrication of surface micromachined sensors and actuators.

Rolf Mallée was born in The Hague in 1949. He joined the instrumentation division of the central electronic service at Delft University, The Netherlands, in 1971. In 1987, he transferred to the IC processing laboratory since which time he has been responsible for CVD processing.

Pasqualina M. Sarro (S'84–M'87) received the Laurea degree in solid-states physics from the University of Naples, Italy, in 1980. In 1987, she received the Ph.D. degree in electrical engineering at the Delft University of Technology, The Netherlands.

From 1981 to 1983, she was a Post-Doctoral Fellow in the Photovoltaic Research Group of the Division of Engineering, Brown University, RI. Since then, she has been with the Delft Institute of Microelectronics and Submicron Technology (DIMES), at the Delft University, where she is responsible for research on integrated silicon sensors and microsystems technology.

Reinoud F. Wolffenbuttel (S'86–M'88) was born in Abcoude, The Netherlands, in 1958. He received the M.Sc. degree in 1984 from the Delft University of Technology. In 1988, he received the Ph.D. degree on the application of silicon color sensor sensing.

Since 1986, he has been a Staff Member of the Laboratory of Electronic Instrumentation, Delft University of Technology, and is involved in digital instrumentation and integrated smart sensors.

196