Characterization of Surge Arresters for Harmonic Overvoltage studies.

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Summary

This thesis presents the development of a frequency-dependent model for metal oxide surge arresters (MOSAs) to better understand their behaviour under temporary overvoltages with a high harmonic content. This topic has gained importance due to the increasing use of long AC cables in connecting offshore wind farms to the transmission grid, which introduces a high capacitance to the grid and raises the risk of harmonic resonances. These resonances can lead to sustained temporary overvoltages, making accurate arrester modelling essential for selecting appropriate surge arresters to withstand these conditions.

Surge arresters are critical components for protecting high-voltage equipment from overvoltage events. The main objective of this work was to investigate the response of the arrester under both AC and DC voltages at a variety of frequencies, with particular focus on the low-current region of the characteristic voltage-current (V-I) curve.

To achieve this, High-voltage AC and DC tests were performed on a surge arrester block. The measured data were used to extract the resistive and capacitive components of the current, as well as to calculate the power losses. These results formed the basis for developing a four-branch nonlinear model. Curve-fitting techniques and various algorithms in MATLAB simulations were used to determine the model parameters, which were then validated against the experimental data. The model demonstrated good accuracy for peak voltages up to 9 kV and showed clear frequency-dependent behaviour, particularly in the 50 to 500 Hz range.

Overall, the final model aligned well with the RMS values of total current as well as the average power losses, with only minor deviations from the measured results. This work contributes to improving surge arrester modelling and lays the groundwork for further developments in frequency-dependent modelling within simulation tools such as ATP-EMTP.

Acknowledgment

I am deeply thankful to my thesis supervisors, Christiaan Engelbrecht and Dr. Mohamad Ghaffarian, for their guidance and mentorship. Christiaan has supported me through every step of this project with patience and clarity, while Dr. Ghaffarian has been a consistent source of academic and professional support throughout my Master's studies. Your expertise and encouragement have been invaluable.

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1

Introduction

1.1. Introduction

Metal oxide surge arresters play a vital role in electrical power systems by protecting against overvoltages caused by switching operations or lightning strikes. Its primary function is to limit overvoltage levels and prevent insulation failure, ensuring the safety of critical equipment such as power transformers.[2][22] The shift toward a more sustainable energy system, along with the increasing demand for electricity, is adding complexity to electrical networks. This is particularly evident with the large-scale integration of wind turbines through converter-based generation and the expansion of new HVDC connections between countries.[9]

As a result, uncertainties in power system operation are expected to grow. Surge arresters, as key protective devices, may be affected by new types of temporary overvoltages (TOVs) introduced by these evolving network conditions. To ensure the stability and security of power system operations, a detailed analysis using electromagnetic transient (EMT) simulation tools is essential. However, these studies demand significant computational resources and require detailed modeling to generate accurate and reliable data.

1.2. Thesis description

1.2.1. Project Description

The long AC cables used to connect offshore wind farms to the onshore transmission network introduce high capacitance (see Figure 1.1), creating the potential for harmonic resonances. These resonances may result in sustained temporary overvoltages (TOVs), particularly when triggered by phenomena such as transformer inrush currents during energisation. Surge arresters are highly sensitive to such overvoltages and must be properly selected and dimensioned to ensure reliable protection under these conditions.

The primary object of this thesis is to characterise metal oxide (MO) surge arrester blocks in the low-current region (Region I). An electrical model is developed that accounts for both voltage and frequency dependence in this region. The aim is to enable more accurate assessment of failure risks under TOV conditions caused by low-order harmonic resonances.

The proposed model will be implemented in ATP-EMTP and tested alongside a simplified network model to evaluate the frequency-dependent response of the surge arrester under harmonic excitation.

The low current region has been selected for modelling because most thermal runaway and long-term degradation processes originate here. If the leakage current becomes excessive, it may cause localised heating within the arrester, potentially leading to accelerated ageing or failure. Accurate modelling and measurement in this region are essential for design validation, quality control, and early fault detection.

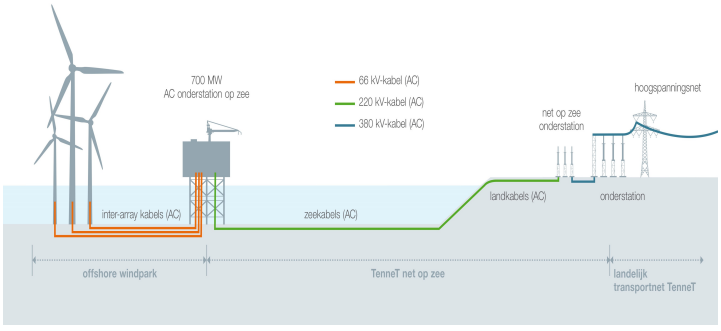

Figure 1.1: Long AC cables connections to offshore introduces a very high capacitance to the network [20],

1.2.2. Introduction to Harmonic resonance overvoltages

Power systems can be modeled using series and parallel combinations of capacitances and inductances, leading to the formation of resonant conditions at different frequencies.[3] A low impedance typically indicates the presence of a series resonance, while a high impedance is characteristic of a parallel resonance. The interaction between series and parallel resonances, combined with harmonic current injection, can lead to temporary overvoltages in the power grid. The resonant frequency of a power system is determined by the interaction between its equivalent inductance and capacitance. Low-frequency resonances can occur in scenarios such as:

a) The addition of long AC cables with high capacitance to a network with moderate inductance.

b) The integration of a long compact transmission line (with moderate capacitance) into a weak system with high equivalent inductance.
These phenomena can cause the network to resonate at low-frequency levels. To mitigate potential issues, it is essential to conduct harmonic studies to identify resonance conditions and implement appropriate countermeasures. Such studies may include:
1) Energization and re-energization of large transformers and reactors.
2) Switching operations involving cables and capacitor banks.
3) Fault clearing and system islanding scenarios.
4) Auto-reclosing of circuit breakers.

A specific concern in this regard is the excitation of resonance due to the harmonic-rich inrush current of transformers, which arises from their nonlinear saturation characteristics.

Figure 1.2 illustrates the switching of a nonlinear inductance within a network modeled as an RLC circuit, demonstrating the potential impact of transformer energization on system resonance.

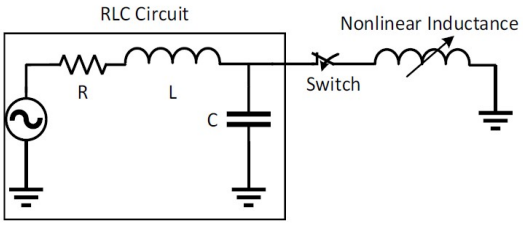

Figure 1.2: Switching of non-linear inductance in front of an RLC circuit [3],

The resonance frequency of a network containing an inductance L and a capacitance C is given by:

$$f_r = \frac{1}{2\pi\sqrt{LC}} \tag{1.1}$$

where f_r is the resonance frequency in hertz (Hz), and L and C are the inductance and capacitance of the circuit, respectively.

1.2.3. Resonant overvoltages caused by transformer saturation

Transformer saturation might happen during the energizing of a transformer or because of fault clearing.[9] During a transformer energizing, a mismatch will happen between the remanent flux of the transformer and the flux imposed by the network voltage, causing saturation and a possibility of a high inrush current. A transformer at a saturation state is compared to a harmonic current source.

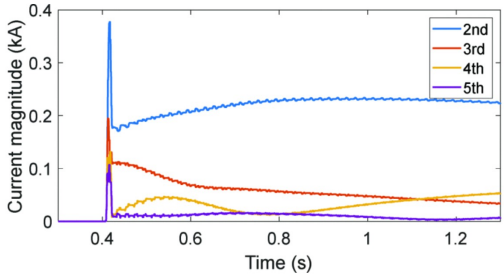

Figure 1.3: Harmonic content of inrush current following transformer energization [9],

This harmonic current source carries a remarkable harmonic component at low harmonic orders, including 2nd, 3rd, etc. When a grid contains parallel resonances at the same frequencies as the harmonic current, the risk of high resonant overvoltages become very high. Figure 1.3 illustrates a case of a harmonic content inrush current when energizing a large power transformer (simulated in PSCAD).

Many methods can mitigate resosnat overvoltages due to transformer energization such as the usage of controlled switching, or operational constraints.

1.2.4. Impact of resonant overvoltages on equipment

Resonant overvoltages will put dielectric and thermal stresses on the grid appliances such as surge arresters and power transformers. CIGRE's publications include many curves representing the TOV withstand characteristics of different equipment. However, those curves are valid for only the basic frequency of the network(the fundamental frequency), and comparing them with resonant overvoltages must be done carefully. Currently, there are no guidelines that evaluate or diagnose the effect of resonance overvoltages on equipment, but CIGRE studies are in progress to address this case study.

The TOV curve is a valuable tool for selecting the rated voltage of a surge arrester, as it provides a fixed TOV magnitude for a given duration. However, in the case of resonant overvoltages, where both magnitude and frequency fluctuate, the standard TOV curve is not applicable.

A recent study suggests that it is possible to evaluate the energy dissipation of a surge arrester subjected to TOV conditions.[9] The proposed approach utilizes the TOV curve (without prior duty) to establish a minimum voltage-current characteristic curve, which can be integrated into EMT models to directly estimate the dissipated energy when the surge arrester experiences resonant overvoltages.

Additionally, Figure 1.4 illustrates the voltage at a studied station subjected to a fault, while Figure 1.5 presents a measured voltage case study under no-load conditions, along with the equivalent peak voltages of the TOV. For comparison, the withstand capability of transformers is also included(in blue colour). The highest TOV value recorded in the study is approximately 1.62 p.u., which remains below the transformer withstand curve, indicating that the overvoltage is within acceptable limits.

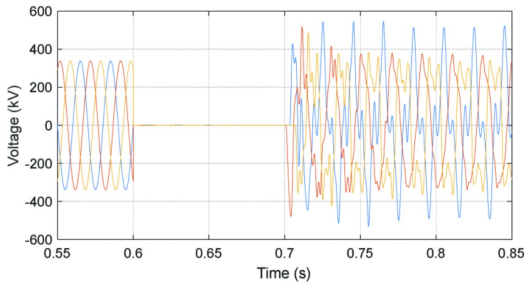

Figure 1.4: Calculated voltages before, during, and after a fault at a studied station[9],

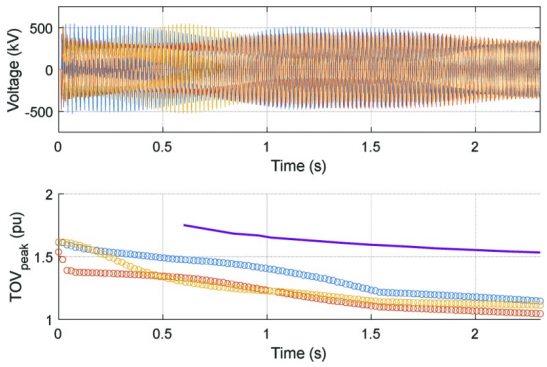

Figure 1.5: Calculated voltages (upper) and TOVpeak (lower) following fault clearing for a study case without loads. TOV peak compared against CIGRE withstand curve for transformers (shown by the solid line) [9]

2

Technical background of Surge arrester

The defining characteristic of metal oxide surge arresters is their highly nonlinear voltage-current behavior. Under continuous operating voltage (COV), they allow only a small leakage current in the milliamps range. However, when exposed to overvoltages, they conduct very high currents, often reaching tens of kiloamperes, effectively limiting excessive voltage levels in the system.[2][22]
Metal-oxide Surge arresters are also an essential part of the insulation coordination and high voltage transmission system, and it has many electrical characteristics that are important for facilitating the selection process of a surge arrester, some key parameters include:

- **Continuous Operating Voltage:** The voltage continuously applied across the surge arrester terminals under normal operating conditions.
- **Nominal Discharge Current:** The standard peak current that the arrester can safely discharge during temporary overvoltages (TOVs).
- **Residual Voltage:** The voltage that appears across the arrester terminals while it is conducting surge current during an overvoltage event.
- **Switching Impulse Current:** The current associated with slower, high-energy transients typically caused by switching operations in power systems.
- **Steep Front Current:** A fast-rising surge current with a short rise time, representing severe lightning or switching transients.

Thermal energy handling capability and pollution withstanding are characteristics that should be also considered.

2.1. Surge arrester classification

Surge arresters are broadly classified into **station** and **distribution** types, primarily distinguished by the following parameters [17]:

- I_n: Nominal discharge current
- I_{sw}: Switching impulse discharge current
- Q_{th}: Thermal charge transfer rating
- W_{th}: Thermal energy rating
- Q_{rs}: Repetitive charge transfer rating

Table 2.1 provides an overview of the main surge arrester classes and the criteria used for selecting the appropriate class for different applications. In addition, all surge arresters must meet specific minimum test requirements and performance characteristics, which vary based on their function in the power network. These requirements are outlined in the IEC standards [17].

Arrester class	Station			Distribution		
Designation	SH	SM	SL	DH	DM	DL
Nominal discharge current[a]	20 kA	10 kA	10 kA	10 kA	5 kA	2,5 kA
Switching impulse discharge current[a]	2 kA	1 kA	0,5 kA	--	--	--
Q_{rs} (C)	≥ 2,4	≥ 1,6	≥ 1,0	≥ 0,4	≥ 0,2	≥ 0,1
W_{th} (kJ/kV)	≥10	≥ 7	≥ 4	--	--	--
Q_{th} (C)	--	--	--	≥ 1,1	≥ 0,7	≥ 0,45
[a] Other currents may be specified upon agreement between manufacturer and user.						
NOTE The letters "H", "M" and "L" in the designation stand for "high", "medium" and "low" duty, respectively.						

Figure 2.1: Surge arrester classificatoins[17],

2.2. Electrical characteristics

2.2.1. Continuous operating voltage Vc

The continuous operating voltage (COV) is the maximum allowed voltage that can be continuously applied to the surge arrester terminals, using a sinusoidal power-frequency voltage wave. Vc is located in the pre-breakdown region of the voltage-current curve (see figure 2.3) and is calculated as $1.05 * U_{system}/\sqrt{3}$ in a solidly grounded neutral system. This value represents the minimum recommended Vc, and in systems with higher pollution levels, it may be increased to enhance operating stability. In compensated neutral systems, Vc may be equal to the system voltage (Vsystem).

2.2.2. Rated voltage Vr

The rated voltage of a surge arrester is the power-frequency voltage applied for at least 10 seconds during the operating duty test.[6] This voltage defines the capability of the surge arrester to withstand temporary overvoltages for 10 seconds and serves as a key parameter in characterising its performance.

2.2.3. Nominal discharge current In

The nominal discharge current is a key parameter used to classify surge arresters and serves as a primary protection characteristic. According to IEC 60099-4:2014, standard nominal discharge current ratings are 2.5, 5, 10, and 20 kA, with higher ratings corresponding to increased performance requirements (see Table 2.1). The selection of the nominal discharge current is critical for insulation coordination, as it directly determines the arrester's lightning impulse protection level (Upl), which is defined by its residual voltage at the specified discharge current.

2.2.4. Reference voltage Vref

The reference voltage can be measured when the reference current is passing through the surge arrester blocks or sections. On the voltage-current curve, The reference current value varies between 5 and 20 mA, and the measurements are done at room temperature of around 20°C ± 15 K

2.2.5. Residual voltage Ures

The residual voltage of a surge arrester refers to the peak voltage that appears across its terminals during the passage of a discharge current.

The purpose of residual voltage measurements is to determine the maximum residual voltage for a given surge arrester design under specified current impulses and waveforms. These values are obtained from type tests and the maximum lightning current impulse, as defined and published by the manufacturer.

Manufacturers typically provide the following residual voltage data for surge arresters:

- **Maximum Lightning Impulse Residual Voltage:** For impulse currents of at least 0.5, 1, and 2 times the nominal discharge current.
- **Maximum Switching Impulse Residual Voltage:** For applicable switching impulse current conditions.
- **Maximum Steep Current Impulse Residual Voltage (excluding inductive contribution):** For an impulse current with a peak equal to the nominal discharge current.

- **Maximum Steep Current Impulse Residual Voltage (including inductive contribution):** For an impulse current with a peak equal to the nominal discharge current of the arrester.

2.2.6. Thermal charge transfer rating Qth

It is the maximum charge that can pass through a surge arrester or one of its sections within a three-minute period, without causing thermal runaway during the thermal recovery test.

2.2.7. Thermal energy rating Wth

It is the maximum specified energy, given in kJ/kV of Ur, which can be injected into an arrester or a section in that arrester within a time limit of three minutes without causing a thermal runaway during a thermal recovery test.

2.3. Surge arrester voltage-current characteristic

The behaviour of a metal oxide (MO) surge arrester is commonly described by its voltage-current (V-I) characteristic curve, which consists of three distinct regions, illustrating its performance under normal and overvoltage conditions [21, 2].

Region I — Leakage Current Region:
Under normal system conditions, the surge arrester is subjected to the continuous operating voltage. In this region, shown in Figure 2.2, the arrester remains in a non-conducting state, and the current is dominated by capacitive effects. The resulting leakage current is typically in the milliampere range, and the V-I curve appears nearly linear.

The MO blocks in this region are temperature-dependent; an increase in temperature leads to an increase in the leakage current at the same voltage level, shifting the V-I curve to the right, and potentially stressing the arrester during continuous operation.

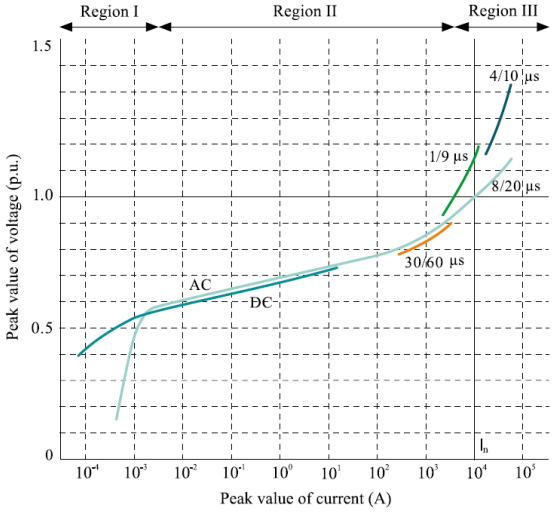

Figure 2.2: Voltage-current characteristics of a ZnO surge arrester with In = 10 kA. The voltage is normalized to the residual voltage of the ZnO surge arrester at In [2]

Region II is the intermediate region where the highly nonlinear behavior of the metal oxide surge arrester becomes dominant. In this region, the arrester experiences higher voltages due to switching surges or temporary overvoltages, and its response is primarily resistive (see Figure 2.2).

This middle region is crucial because the MOSA allows a significantly higher current to pass with only a small increase in voltage. The degree of nonlinearity is evident in the flatness of this section of the V-I characteristic curve (the flatter the curve, the better the MOSA's performance). This region, also known as the reference current region, is crucial for predicting the overall V–I characteristic curve of the arrester, as it reflects how the voltage responds to variations in current. For instance, between 1 and 10 mA.

Region III is where a surge arrester conducts extremely high currents, ranging from 100 A to 10 kA, due to

severe overvoltages caused by lightning surges or very fast transients (VFT). In this region, the current density exceeds 10^3 A/cm², and the arrester's dynamic characteristics become dominant.

Overvoltages dictate the conductivity of the arrester material, causing a rise in the temperature of the metal oxide blocks. A temperature range of 100°C to 300°C is generally acceptable, but exceeding this limit can cause permanent damage to the blocks. To prevent excessive heating beyond safe thresholds, the high current and increased conductivity should not persist for more than a few seconds.

This region represents the primary function of the surge arrester, providing protection by allowing a large current to flow within extremely short time intervals, typically in the millisecond or even microsecond range. The ability of the arrester to handle high currents is time-dependent, which is further explained in the power frequency versus time curve.

Each operational region of a surge arrester plays a critical role in the surge arrester overall performance and reliability.

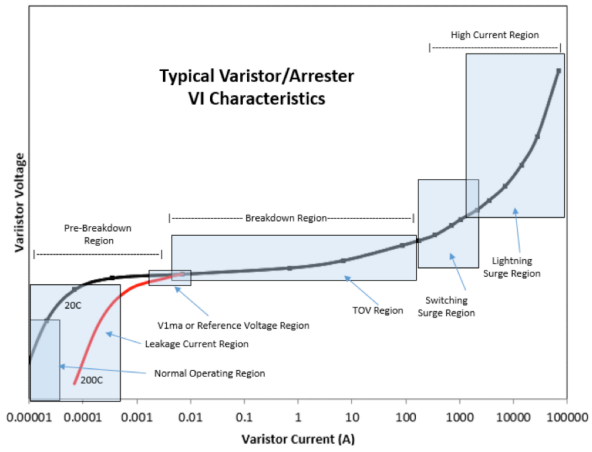

Figure 2.3: V–I characteristic of ZnO Surge arrester[21]

2.4. Mechanical characteristics

The surge arrester is a relatively simple device compared to other electrical equipment in substations, with minimal requirements for transportation and storage. However, it is important not to underestimate its importance along with its accessories, as some components remain continuously connected to the network and are subjected to stress throughout the lifetime of the arrester. Figure 2.4 shows a power transformer equipped with its protection and isolation system, which includes a surge arrester with its Key components such as the grading and corona rings,

flange covers or insulating bases, and highly nonlinear metal oxide resistive elements. Surge arresters are precisely designed by manufacturers to maintain a balance between continuous operating voltage and environmental stresses, ensuring a protection level and the ability to handle high-energy surges. Any disturbance, such as the removal of a protective element or installation errors, can disrupt this balance. Therefore, it is crucial to avoid mistakes and strictly follow the installation guidelines of the manufacturer.[6]

With regard to transportation and storage, specific instructions must be followed. For example, porcelain-housed surge arresters are particularly sensitive to mechanical stress, and transportation can potentially subject them to the highest mechanical loads they will experience in their lifetime. To minimise stress, transportation and storage may be recommended in a vertical position.

For polymer-housed surge arresters, the environmental conditions during storage must be carefully controlled. Moisture and organic growth, such as moss and fungi, can develop if the arrester is wrapped for an extended period. Manufacturers should provide clear guidelines for the removal of protective packaging.

Finally, grading and corona rings must always be installed, as they play a critical role in arrester performance and should never be ignored.

Figure 2.4: A power transformer accompanied by a surge arrester. [15]

2.5. Internal structure of a surge arrester block

Metal oxide varistors (MOVs) or surge arrester blocks are the most critical component and the core of modern surge arrester blocks. To ensure high performance and minimize faults, strict quality control must be maintained by MOV manufacturers.[19] MOVs consist of materials that behave similarly to millions of microscopic electronic switches that activate in response to a given signal, diverting excess energy to the ground and thereby protecting other equipment in the circuit. They are widely used in various applications, including surge arrester blocks and smaller household devices.

The electrical properties of a varistor are determined by its internal crystalline structure. At a microscopic level, MOVs are primarily composed of zinc oxide (ZnO) crystals (see Figure 2.6), formed through a high-temperature sintering process. Electrical behavior is largely influenced by the grain boundaries, where key electronic phenomena occur.

MOVs are typically composed of approximately 90% zinc oxide and 10% additive materials. These additives, which exist between the crystal grains, are responsible for the switching and nonlinear characteristics of the MOV. Common additive materials include bismuth, nickel, antimony, and manganese, with the specific composition of each material significantly affecting the MOV's electrical properties. Due to the high precision required to produce reliable MOVs, every stage of the manufacturing process is carefully controlled and systematically organized.

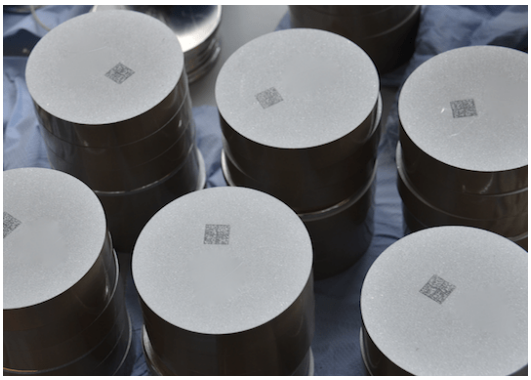

Figure 2.5: Zinc-oxide blocks[8]

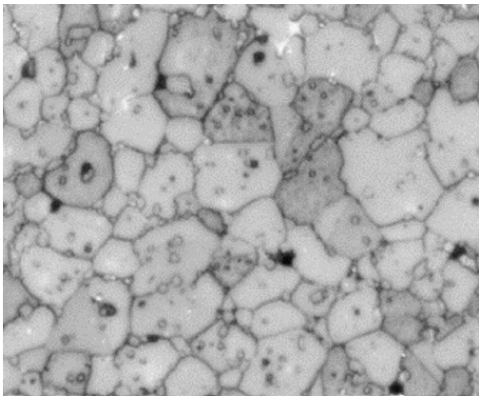

Figure 2.6: Structure of a zinc oxide Varistor grains and its boundaries[19]

2.6. Internal construction of a surge arrester

Zinc oxide blocks are nearly identical in all types of surge arresters. However, the internal design differs depending on whether the arrester has a polymer or porcelain housing (see Figure 2.7) [13].

In both designs, the surge arrester blocks are stacked and connected in series. The key distinction lies in their internal composition. Porcelain surge arresters contain a specific amount of dry air or other gases, whereas polymer-housed surge arresters do not have any internal gas. As a result, the methods for handling short-circuit withstand capability and internal corona discharges must differ.

Porcelain surge arresters, due to their internal gas content, can experience high internal pressure in the event of a short circuit, potentially leading to an explosion. To prevent this, they must be equipped with a pressure relief system. Additionally, to mitigate corona discharges, a sufficient distance should be maintained between the block column and the insulator surface. This helps prevent radial voltage differences between these surfaces, which could otherwise lead to partial discharges.

Polymer-housed surge arresters come in various designs, including open (cage-type), closed, and tubular

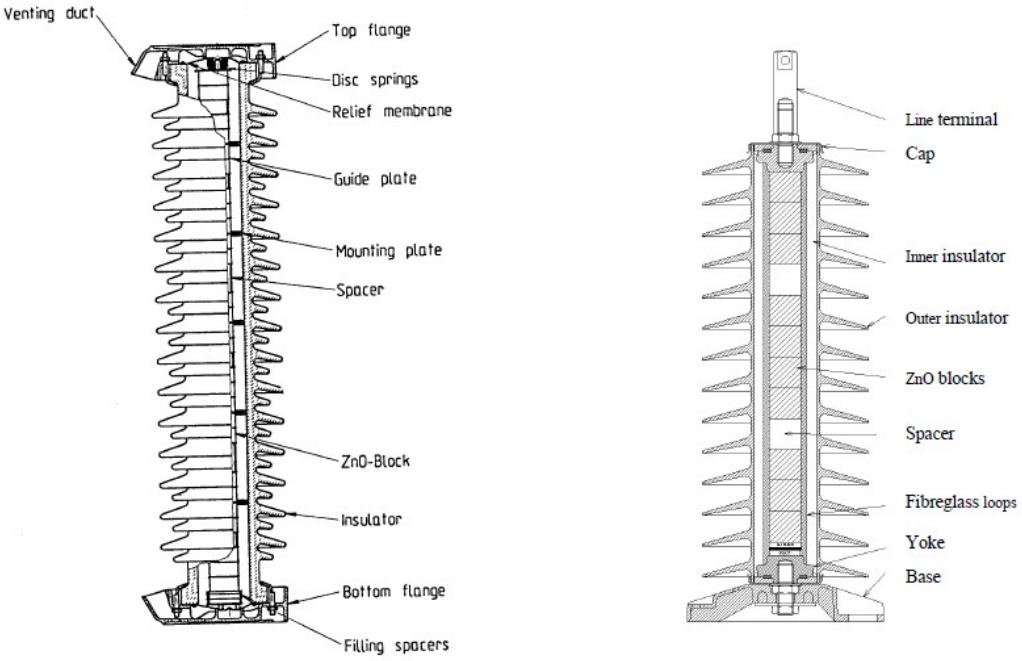

Figure 2.7: Internal design of a MOSA with polymer shedding on the right side and with porcelain shedding on the left side[13],

designs. In tubular designs, the space between the horizontal blocks and the external insulator is filled with gas.

The open or cage design, consists of a mechanical cage structure made of fiberglass braids or rods surrounding the central blocks. Zinc oxide blocks provide mechanical strength, while silicone rubber is cast around the internal components. The outer insulator, with its sheds, is then molded or inserted around the structure.

Since this design lacks internal gas volume, a short circuit can cause some internal materials to evaporate, increasing pressure and potentially tearing the rubber insulator either partially or along the entire length of the surge arrester. In such cases, the internal arc may extend outside the arrester due to air ionization in the surrounding area.

The second type without openings, surge arrester is designed without openings to minimize pressure buildup caused by internal short circuits. In this design, glass fiber may be woven around the metal oxide blocks, or a glass-fiber tube may be fitted around them.

The glass-fiber tube must be structurally strong to provide good mechanical withstand. However, if its strength is significantly higher than the force of the short circuit, excessive pressure may build up inside the surge arrester, potentially leading to an explosion before any fracture occurs to release the pressure. This can have severe consequences. To prevent such risks, several solutions are considered, including the use of slots.

In the case of a woven glass-fiber design, specific weak points are intentionally incorporated to allow pressure relief during a short circuit. These weak points ensure that excess pressure is safely released, preventing the surge arrester from exploding.

The third type with the tubular design, follows the same structural concept as a standard porcelain surge arrester. However, instead of porcelain, it uses an insulator made of glass-fiber-reinforced epoxy, with an outer layer composed of silicone or EPDM rubber.

Internally, this design is similar to porcelain-housed surge arresters, featuring cylindrical gas gaps between the block columns and other insulating materials. A pressure relief device is essential in this design, serving the same purpose as in porcelain surge arresters.

One of the advantages of this design is its high mechanical strength. However, it also has some drawbacks. For instance, cooling efficiency is lower, and there is a higher risk of corona discharges between the zinc oxide column and the insulation. To mitigate corona discharge, the width of the gap can be increased, but this may lead to higher manufacturing costs and reduced cooling efficiency.

Additionally, a surge arrester design without cylindrical air-gap insulation does not experience corona discharges under normal operating conditions in dry and clean environments. A routine test is performed to ensure the design remains corona-free under these conditions. However, during adverse weather conditions, such as rain or pollution accumulation on the outer insulation, radial electrical stress can increase significantly. This highlights the importance of high-quality insulation materials that are free from cavities, as internal corona discharges within the material can lead to long-term reliability issues.

To prevent material erosion or damage caused by radial voltage stress, ensuring sufficient insulation thickness is crucial. Proper thickness helps prevent the formation of holes in the insulator, thereby improving its durability and performance over time.

2.7. Temporary over-voltages

2.7.1. Introduction

Temporary overvoltages in power system networks can result from faults, switching operations, or lightning strikes [6]. These overvoltages may exceed the design limits of electrical equipment, potentially overstressing components and affecting system performance.

To ensure proper protection, it is crucial to identify the type of overvoltage present in the network. This allows for the selection of an appropriately designed surge arrester (SA) with the necessary temporary overvoltage (TOV) capability, protection margin, and energy-handling capacity.

For power equipment with non-self-restoring insulation, it is recommended that overvoltages be limited to below 85% of the insulation strength. However, in cases where flashover is acceptable, such as with self-restoring insulation materials, surge arresters can help control overvoltages and ensure the system operates within acceptable limits.

Surge arresters are primarily used to protect against lightning and switching overvoltages, as power system equipment is generally not at risk under normal operating and temporary overvoltage conditions.

Therefore, defining surge arrester duties must include an assessment of its cumulative energy absorption capability and the magnitude of the related current, particularly if the surge arrester is required to withstand extreme temporary overvoltage conditions.

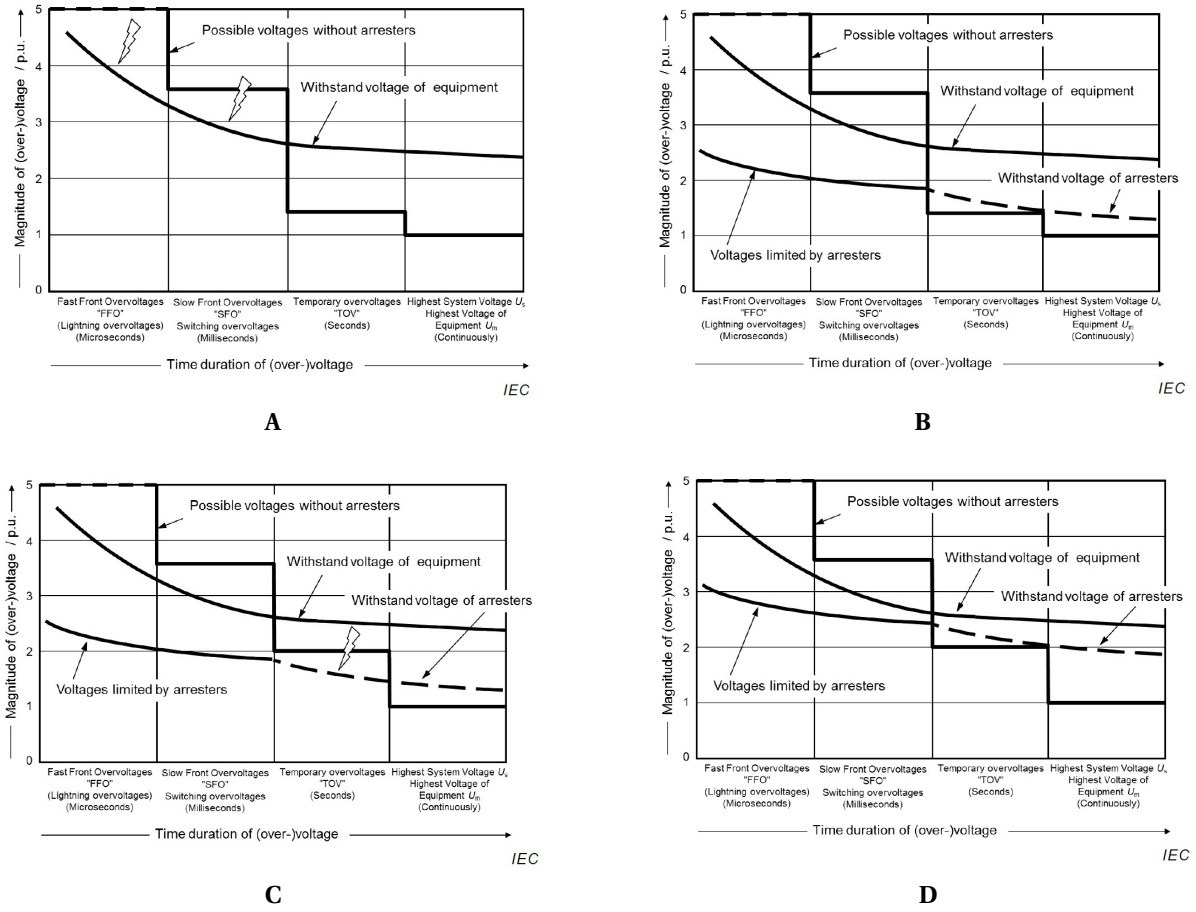

Figure 2.8: Typical voltages and duration examples for different earthed systems [6]

Figure 2.8 consists of four sub-figures (a, b, c, d) and illustrates the effects of different surge arrester ratings and grounding systems:

A) **Earthed system without surge arrester protection:** In this case, the withstand voltage of the equipment is exceeded in both the slow-front overvoltage (SFO) and fast-front overvoltage (FFO) regions, increasing the risk of insulation failure.

B) **Solidly grounded system with surge arrester:** The arrester effectively limits overvoltages in both SFO and FFO regions to acceptable levels below the equipment's withstand voltage. Additionally, it is rated appropriately to handle lower overvoltages during normal operation.

C) **Isolated neutral system with surge arrester protection:** While the arrester provides similar protective function as in (b), the system overvoltages exceed the withstand voltage of the surge arrester, leading to protection failure.

D) **Isolated neutral system with higher-rated surge arrester:** This configuration allows the arrester to withstand temporary overvoltages (TOVs) while still providing reliable protection in the SFO and FFO regions.

Surge arresters are primarily studied in the SFO and FFO regions, as these are their main areas of operation. However, it is also essential to analyze their performance in the TOV region. Long-term failures can occur due to harmonic overvoltage resonances and temperature accumulation, which may result in continuous overloading in the first and second regions of the voltage-current (V-I) curve.

2.7.2. Power frequency voltage versus time characteristic curve

Power grid faults and other factors can introduce overvoltages on surge arresters. Temporary overvoltages (TOVs) are power-frequency overvoltages that last for a short duration, typically less than 1 hour [19]. If not properly considered and evaluated, these overvoltages can overstress the surge arrester. The power-frequency voltage versus time characteristic curve illustrates the allowable duration and magnitude of power-frequency overvoltage that can be applied to the surge arrester without causing damage or thermal runaway.

Type tests are conducted to assess the capability of a surge arrester, with and without prior duty, to withstand overvoltages. The prior duty test simulates the impact of lightning or switching overvoltage discharges on the arrester. After undergoing a type duty test, the metal oxide blocks inside the arrester heat up, reducing their thermal recovery capability.

Figure 2.9 illustrates the effect of the duty type test, showing that the curve for an arrester subjected to prior duty is lower than that of an arrester without prior duty. This indicates that prior exposure to high-energy discharges affects the arrester's ability to handle subsequent overvoltages.

To accurately assess the arrester's ability to withstand a specific overvoltage, it is essential to compare the fault's duration and magnitude with the surge arrester's TOV capability curve. It is important to note that surge arresters do not limit normal power-frequency overvoltages. Instead, they are designed to handle short-duration overvoltage events such as switching and lightning surges.

Selecting an appropriately rated surge arrester is crucial for ensuring it can withstand the network's TOV conditions. In some cases, surge arresters are used as sacrificial devices to limit TOVs and protect critical power system components, such as power transformers, from excessive stress.

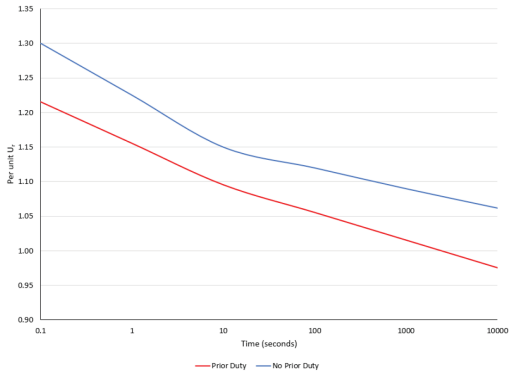

Figure 2.9: Power frequency versus time curve before and after duty[19]

2.8. lightning overvoltages

Lightning is one of the main causes of outages and damage to power system grids and equipment. When lightning strikes transmission lines, it generates a traveling wave in both directions along the line, subjecting insulators and other grid components to high electrical stress and increasing the risk of failure. [18][4]

Transient overvoltages caused by lightning can result from either a direct or an indirect stroke. A direct stroke occurs when lightning strikes the phase conductor, generating a traveling wave that applies voltage to the connected equipment terminals or across insulators. In the case of an indirect stroke, lightning strikes the transmission tower or shield wire, causing the surge to travel through the system and reflect at the tower footing resistance.

A back flashover happens when the transient voltage exceeds the critical flashover voltage of the insulator, leading to an electrical breakdown. This significantly affects the reliability of the transmission network. Additionally, transient overvoltages (especially those caused by lightning) can result in a large voltage increase at the far end of the line. If this voltage surpasses the basic insulation level (BIL) of the equipment, it can damage or even destroy power system components, particularly transformers.

To minimize these risks, it is important to model and monitor the effects of lightning. Real atmospheric lightning impulses typically consist of multiple current impulses, with an average of four individual impulses occurring about 40 ms apart. More than 80% of cloud-to-ground lightning strikes involve multiple impulses, and in some cases, this number can reach up to 30. While some approaches have attempted to replicate such high numbers of impulses, the observed effects in real systems are not always accurately reproduced.

Lightning overvoltage modelling is highly complex and cannot be performed with complete precision. However, standardised test methods have been developed by both scientific and industrial communities to assess the protection level and performance of surge arresters and surge protection equipment. These tests use impulse currents with specific waveforms, typically 10/350 µs or 8/20 µs, to simulate lightning events. The standard procedure involves applying a single impulse to the surge protection device at intervals of 50 to 60 seconds.

2.9. Switching overvoltages

Switching transients occur due to the operation of circuit breakers in power system networks [10]. There are two main types of switching operations:

- **Energization:** Includes operations such as reclosing and the energization of lines, cables, and other components.
- **De-energization:** Involves current interruption under both fault and non-fault conditions.

Studying switching transients is essential for the proper selection of surge arresters and for understanding the overvoltage stresses imposed on the system and its equipment. This includes evaluating the transient recovery voltage (TRV) across circuit breaker contacts. Moreover, such analysis helps in assessing the effectiveness of transient mitigation devices—such as controlled closing systems—in reducing these stresses.

2.10. Thermal effect on Surge arresters

Figure 2.10 illustrates the effect of temperature on the V-I characteristic curve of the surge arrester. A significant difference is observed between 20°C and 200°C, which can lead to thermal runaway at low voltages or even at the continuous operating voltage [16].

The four blue circles in the figure represent measurements of the resistive current at four different temperature levels, but with the same voltage applied. These measurements show an increase in resistive current, from approximately 0.2 mA at the lower temperature to around 1.3 mA at highest temperature.

2.10.1. The effect of temperature on MOSA leakage current

To evaluate the performance of a surge arrester under normal operating conditions, the voltage-current curve should be monitored in the region of low current (the first region).

By separating the capacitive current (shown in green) from the resistive current (shown in red), graph (a) in Figure 2.11 represents the currents under normal conditions at a temperature of 20°C. In contrast, graph (b) illustrates the effect of an increased temperature of 100°C on the surge arrester's characteristics. While the capacitive current remains relatively unchanged, the resistive leakage current increases significantly, with its

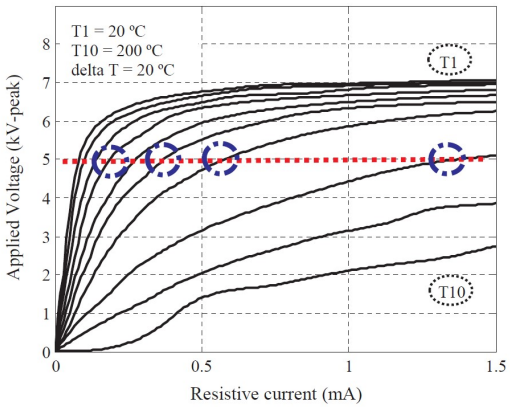

Figure 2.10: V-I characteristic of a SA at different temperature levels[16],

peak value tripling from approximately 25 µA to 75 µA. This indicates a notable rise in power losses, highlighting the strong influence of temperature on surge arrester.

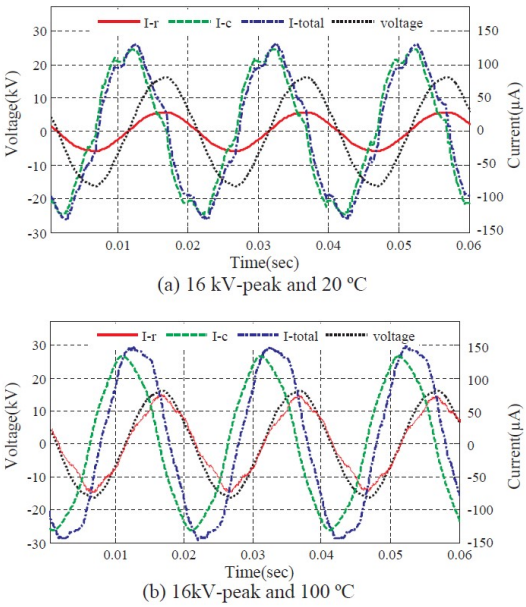

Figure 2.11: Power losses rise as the temperature increases[16]

2.11. Effect of harmonics on surge arrester aging

2.11.1. Introduction

Metal oxide surge arresters operating under continuous AC and DC conduction might degrade due to temporary overvoltages, a process that becomes more severe in harmonic-rich grids. Once degradation occurs, it is irreversible, leading to both physical and electrical changes in the surge arrester [1]. With the growing integration of renewable energy sources, such as solar panels and wind turbines, modern power networks are experiencing higher harmonic content. As a result, the likelihood of exposure to harmonic-induced temporary overvoltages (TOVs) is increasing. Previous studies have shown that voltage harmonics significantly impact leakage current, raising the failure probability of surge arresters.

2.11.2. Failure analysis under harmonic Voltage

An accelerated degradation test, incorporating higher temperatures and a distorted voltage, was conducted on multiple surge arresters [1]. The time-to-failure distribution was then analyzed using three Weibull prob-

ability methods, and the resistive component of the total leakage current was examined using the Fourier series.
The analysis revealed that an increase of 6.24% and 5.58% in the 3rd and 5th harmonic components of the applied distorted voltage led to a reduction in the mean lifespan of the surge arrester by up to 40%Às a result, the surge arrester's V-I characteristic curve shifted, and the magnitude of the resistive current under a harmonically distorted voltage increased. Furthermore, the degradation of the surge arrester population significantly impacts the V-I characteristic curve.

Figure 2.12 shows that under harmonic degradation, the reference voltage has decreased from around 160V to 100V for a reference current of 1 mA, whereas under normal degradation conditions, it has decreased to around 150V. These results indicate a severe effect of harmonics on the characteristic curve of surge arresters, which could significantly impact their function.
Figure 2.13 illustrates the resistive current components with and without harmonic injection, showing a significant increase in the 1st, 3rd, and 5th resistive current harmonics.

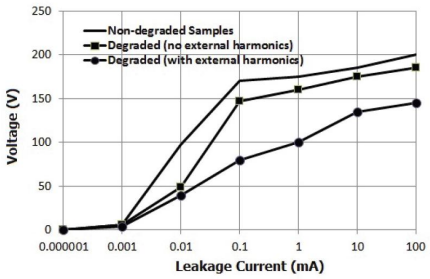

Figure 2.12: U-I curve of 3 Arrester samples (a new sample and 2 degraded samples without/with harmonics)[1]

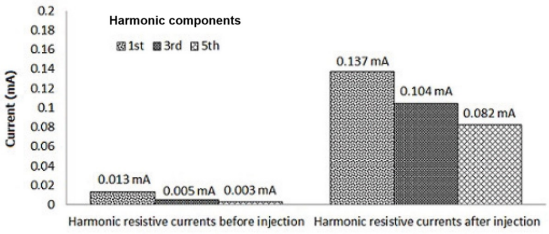

Figure 2.13: Resistive Current Components before and after harmonics aging(the 1st, 3nd, and 5th current harmonics)[1]

According to the test results, the resistive component of the total leakage current of a degraded surge arrester has increased in the presence of external harmonics, leading to an increase in the breakdown of the surge arrester population from approximately 45% to 61%

According to three-parameter Weibull distributions for each group of degraded arresters with and without harmonics, by analyzing and determining the probability density in [1], it is possible to extract and determine the failure rate functions h1,h2(see graph 2.14).

The failure rate function illustrates the effect of external harmonics, figure 2.14 shows that the failure rate without external harmonics h1(t) has a steep increase in the failures per hour from 0 to 2.64 x 10^{-4} in the time interval from 100.6 to 500 hours, and a decrease from 2.46x10^{-4} to 2.35x10^{-4} in the period between 500 and 4500.

The graph shows a further function h2(t), representing the failure rate for degraded surge arrester samples under the external harmonic effect, which illustrates that failures have a high initial rate of rise from 0 to 3.33x10^{-4} failure per hour in the time interval between 100.6 and 500. The failure rate then eases but continues to increase from 3.33x10^{-4} to 4.16x10^{-4} during the period between 500 and 4500 hours.

This behavior means that surge arresters fail at the beginning of their life cycle under normal conditions. Still, under external harmonics, the continued increase in the failure rate illustrates a continuous damage to the surge arrester, reducing their life cycle. To conclude, for the total test time, the failure rate has shown higher values under external harmonics with a nonstop elevation in the failure rate during the whole test.

2.12. Polarization

When an electric field is applied to a Metal Oxide Surge Arrester, leakage currents flow through the surge arrester blocks. These currents have two components: conduction and polarization currents. Both types are sensitive to any changes in the microstructure of the surge arrester blocks [14].
The polarization current is caused by the alignment of the dipoles within the blocks in the direction of the applied field, which can be seen as energy storage due to the external field. Once the field is removed, the dipoles return to their original state, but this relaxation process takes a considerable amount of time. Insulation polarization can be represented by parallel branches, each consisting of a resistance in parallel with a capacitor, and some R-C branches (see Figure 2.15). Each R-C branch represents a single polarization process,

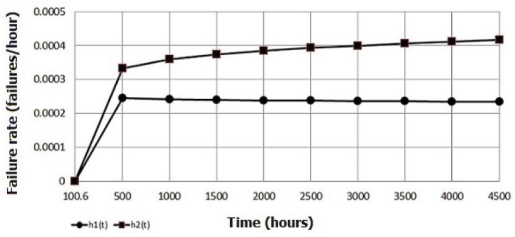

Figure 2.14: Failure rate as a function of exposure time without and with harmonics aging(h1, h2)[1]

with its own unique time constant (Rpn * Cpn), and each is treated as independent.

By using multiple R-C branches to describe the polarization processes, the theory of distributed relaxation time can be applied to predict the insulation's reaction. In most cases, the number of R-C branches used for modeling ranges between 5 and 10, depending on the depolarization current.

The insulation conditions play a key role in determining the boundary values of Rpn and Cpn, or in other words, the time constant.

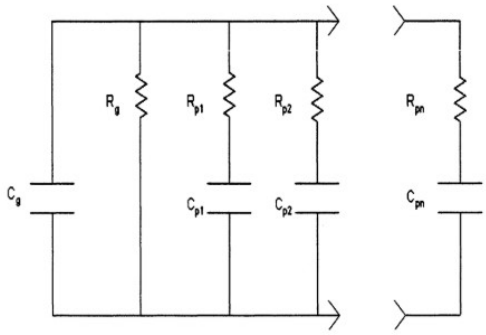

Figure 2.15: Equivalent circuit of insulation for polarization model [14]

Metal oxide surge arresters behave as insulators when working in normal conditions or at a voltage level lower than the rated voltage.[14] Thus monitoring the effect of polarization/depolarization on MOSA dipoles is possible using some diagnostics; up-to-date diagnostics have already been used successfully in many artificially degraded MOSAs and have been reported in many publications. For instance, return voltage measurement and polarization/depolarization current measurement. Furthermore, understanding the relationship between the basic insulation dielectric process and the measured dielectric parameters is the key to correctly translating the results of these diagnostics,

It is important to identify and recognize the polarization in every test object to avoid any measurement mistakes and get an accurate test measurement since polarization is a temporary state of the surge arrester blocks after high stress and temporary over-voltages.

2.12.1. De-polarizing

Generally depolarizing is automatically happened to surge arrester blocks in service, since they are under a continuous operating voltage. The depolarization with AC voltage might take a day or more to completely depolarize. However, under a DC current, depolarization can be performed in a range of one to two hours. DC current works similar to a discharging mechanism and will depolarize the varistors in a very short time.

2.13. Test to verify long-term stability under continuous operating voltage

Surge arresters in normal operation are typically subjected to a voltage lower than the reference voltage (Uref). However, in some designs, surge arresters in continuous operation may experience a voltage higher than Uref, making it difficult to perform the same tests as those conducted under standard conditions.

For MO blocks stressed below U_{ref}, the procedure is as follows:

1. The surge arrester blocks, along with their surrounding medium (identical to that used in the actual surge arrester), are placed in a temperature-controlled oven. The oven space must be at least twice the volume of the tested item.

2. The test blocks are heated until the surface temperature reaches approximately 115°C ± 4°C. Once the target temperature is achieved, the continuous operating voltage is applied. After 3 hours ± 15 minutes of voltage application, the initial power loss P_{start} is measured. Both the temperature and voltage must remain constant throughout the test duration of approximately 1000 hours (see Figure 2.16).

3. Power loss measurements are taken every 100 hours while maintaining the continuous operating voltage V_{ct} constant.

4. After the 1000-hour aging period, a final power loss measurement P_{end} is recorded. The lowest measured power loss over the test period is denoted as P_{min}.

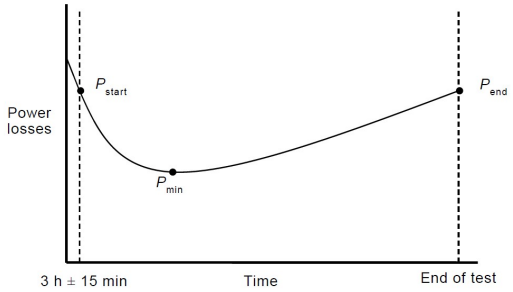

Figure 2.16: Power losses versus time curve during long term stability test [17]

A test subject can be considered to have passed if all three MO samples meet the following criteria:

- All power loss measurements taken after determining the minimum power loss P_{min} must not exceed $1.3 \times P_{\text{min}}$.
- Throughout the entire test duration, power loss measurements must not exceed $1.1 \times P_{\text{start}}$, where P_{start} is the initial power loss recorded after approximately 3 hours of testing.

3

Testing

3.1. Introduction

Temporary overvoltages caused by harmonic resonances might increase the risk of metal oxide arrester failure due to thermal runaway. To evaluate this risk, it is important to analyze the characteristics of surge arrester blocks in the continuous operating region, focusing on steady-state leakage current up to the rated voltage at different frequencies. A validated model based on these evaluations can then be used for system and transient studies, helping to understand better and mitigate potential failures.

3.1.1. Objective with test

The objective of this test is to measure the V-I characteristic of the surge arrester, which can be used to develop a validated electrical model for surge arresters under harmonic overvoltage conditions using a frequency-dependent approach. For this purpose, surge arrester blocks (type E64NR163E) were tested under different voltage and frequency conditions between 50 and 500Hz, typically identified with temporary overvoltages (See IEC 60071-1).[7]

A proposed circuit model by CIGRE[11] shown in figure 4.3, represents the surge arrester behaviour in both the low- and high-current regions, and consists of elements that represent the different behaviour of the SA.
This model consists of two parts: one representing the grain boundary and the other representing the ZnO grains, which will be evaluated in the next chapter.

3.2. Design of test setup

Blocks were tested under both AC and DC voltages to measure and analyse their response, with the purpose of building an electrical model.

3.2.1. Testing blocks

Two different MO blocks were used for testing. Almost all tests were performed on the second block, where we had a sufficient number of units and detailed electrical properties, as further testing might require many samples.

Therefore, only the frequency repeatability test was conducted on the first block while waiting for the delivery of the second set of blocks.

The first type of blocks, this block was used for the frequency repeatability test and had a reference voltage of 3 kV.

The second type of blocks, surge arrester metal oxide blocks (Type E64NR163E) with a 64.5 mm diameter and 44 mm thickness were used.

This block has the following characteristics:

Maximum continuous voltage	Reference voltage	Reference current	Rated voltage	Nominal discharge current
5.3 kV rms	6.51 to 7.43 kV rms	10 mA rms	6.12 kV rm	20 kA peak

The reference voltage can also be illustrated in peak values as the range between 9.2 and 10.5 kV peak.

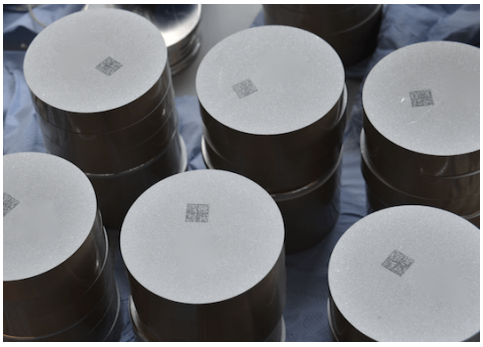

Figure 3.1: Zinc-oxide blocks[8]

3.2.2. Voltages Applied

Two types of voltages were applied during the testing process: AC (alternating current) and DC (direct current), each serving different purposes in evaluating the surge arrester blocks.

- **AC Voltage:** A sinusoidal AC voltage was applied with peak values ranging up to 10.5 kV. This level corresponds to the reference voltage of the MO (metal-oxide) blocks and allows testing within the first low-current region and the beginning of the second region.
- **DC Voltage:** A steady-state DC voltage of up to 10.2 kV was applied to characterize the nonlinear resistive behavior of the MO blocks. The resulting DC current reached a maximum of 16 mA. This setup allowed for the evaluation of the resistive current component without interference from capacitive effects.

3.2.3. Overview of test circuit

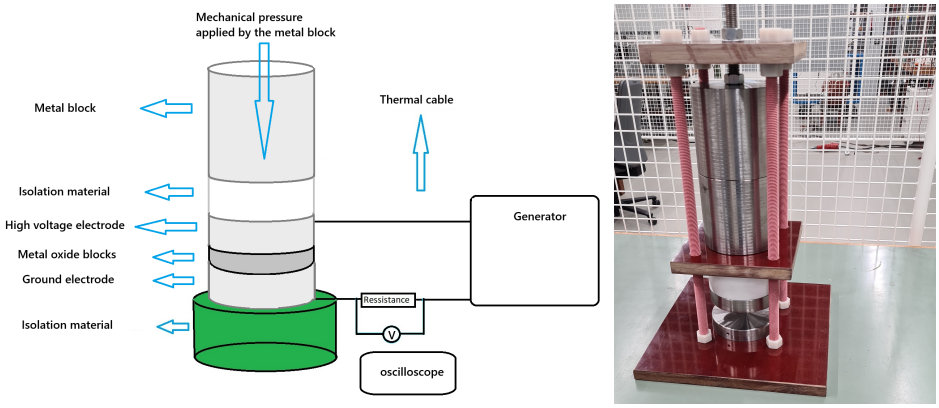

Figure 3.2: Testing circuit diagram and part of the testing set on the right

Figure 3.2 illustrates the test setup and its key components. During testing, the arrester block is positioned between two metallic electrodes, one energized by high voltage (HV) and the other grounded. Proper electrical contact must be ensured by applying mechanical pressure to the surge arrester blocks, with the force maintained between 0.1 kN and 10 kN to guarantee a reliable connection. This pressure is replicated in the test setup using static weight, where a force of 1 kN corresponds to a load of 101 kg.

For this test, an applied pressure of 0.2 kN was chosen, requiring a corresponding static weight of 20 kg. The test setup is designed to withstand voltages up to 12 kV peak and temperatures of up to 130 °C.

The high-voltage source is an amplifier capable of generating sinusoidal voltages at various frequencies and DC voltages. The test fixture, which houses the surge arrester, is placed inside a thermally controlled chamber (oven) to provide insulation and protection against high voltage. The chamber functions as a Faraday cage and is equipped with a door interlock to ensure the test setup can be energised safely. Proper ventilation is maintained to obtain accurate results, as the characteristics of the arrester block are temperature dependent. Current and voltage measurements are taken externally, with current measured at the ground connection using a 1000 ohm shunt, and voltage recorded at the calibrated amplifier output.

3.2.4. Test Equipment

1. **Oscilloscope** (see Figure 3.4):
   An oscilloscope was used to capture and store voltage and current waveforms for further analysis. The recorded data was saved on an external USB stick. The extracted data from each channel typically ranged between 10,000 and 60,000 measurement points, covering four cycles of voltage or current waves. Exceeding this range made data processing in MATLAB more challenging due to computational constraints.

2. **Signal Generator** (see Figure 3.3):
   The signal generator was used to produce the signal for both AC and DC voltages. This signal was then amplified by the high-voltage amplifier to generate a high-voltage output of up to 10.5–11 kV, which was applied to the arrester block.

3. **Amplifier / Voltage Source** (see Figure 3.5):
   Using the amplifier, the test circuit was supplied with voltage at different amplitudes and frequencies. The amplifier could also generate a DC voltage by utilizing the signal generator's offset function. The amplifier has a maximum output current of approximately 40 mA peak and a maximum voltage of 30 kV peak. It includes two measurement output channels—one for voltage and one for current. The voltage amplification ratio is 3000 V per 1 V input, and the amplifier is controlled via the signal generator. Both output channels were used during testing. The current output channel was monitored to ensure the amplifier's maximum current limit was not exceeded, with a current gain of 4 mA per 1 V. Meanwhile, the voltage output channel was used to measure and extract voltage data.

4. **Resistor / Shunt** (see Figure 3.7):
   A shunt resistor with a value of 1000 ohms was used to measure the current through the block. This setup provides a current reading of 1 mA for every 1 V measured.

5. **Two Metallic Electrodes** (see Figure 3.6):
   Metallic electrodes were used to securely hold the surge arrester blocks in place, connecting them directly to the high-voltage cable and ground. The electrodes measured approximately 90 mm in diameter and 40 mm in thickness. To prevent corona discharges, they were designed without any sharp edges, as the applied voltage was in the kilovolt range.

6. **Two Cotton Fibre Plates** (see Figure 3.6):
   Cotton fiber plates (around 40 mm thickness) were used to support the metal weight while applying a mechanical pressure to the blocks and to isolate the high-voltage electrode from the oven.

7. **A Metal Weight**:
   A mass of 20 kg was used to apply a mechanical pressure of 0.2 kN, ensuring good electrical contact.

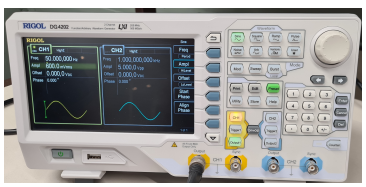

Figure 3.3: Signal generator

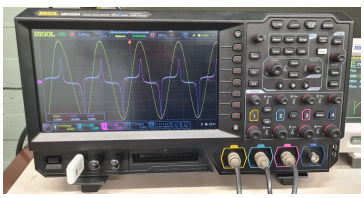

Figure 3.4: The oscilloscope

Figure 3.5: Amplifier(source)

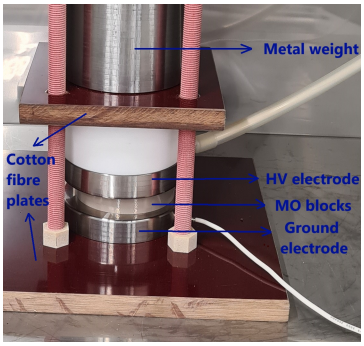

Figure 3.6: High voltage and the grounded Electrodes

Figure 3.7: Measurements shunt(1000 ohm)

3.2.5. Measurements Performed

- **Voltage:** Generated and measured using the amplifier. The voltage waveform was captured using an oscilloscope for four cycles and stored via flash memory for post-processing in MATLAB.
- **Current:** Measured through a 1000-ohm shunt resistor by recording the voltage drop across it. Each 1V corresponds to 1mA of current. The shunt resistor was placed on the ground cable to ensure that only the current through the surge arrester was captured, effectively eliminating interference from capacitive currents in surrounding equipment.
- **Waveform Recording:** Voltage and current waveforms were recorded using the oscilloscope and saved to a flash memory. These signals were then imported into MATLAB for further analysis, including filtering and current decomposition.
- **Frequency:** Generated and controlled by the signal generator, with the output frequency also monitored to ensure accuracy during testing.

3.3. Test procedures

3.3.1. Test Program

1. **Calibration of Test Equipment:** The voltage were calibrated to ensure accuracy and reliability of the readings throughout the testing process.
2. **Measurement Repeatability and Test Consistency;** A series of repeated measurements were conducted at selected voltage and frequency levels to verify the consistency and repeatability of the test results.
3. **Depolarization of the Current:** Prior to testing, the arrester was fully depolarized to ensure that the current readings were not influenced by prior test conditions.
4. **AC Testing:** The arrester was subjected to sinusoidal voltage inputs at various frequencies and amplitudes. Voltage and current waveforms were recorded to analyze impedance, capacitive behavior, and power losses.
5. **DC Testing:** A DC signal was applied to determine the nonlinear resistance characteristics of the arrester. Because of the noise in the signal, a multimeter was used to capture the steady-state values accurately.

3.3.2. Testing Considerations and Setup

1. **Thermal Management**
   Due to the thermal mass of the arrester blocks and electrodes, heat accumulation during testing was a concern. Cooling fans were used inside the oven to enhance airflow and stabilize the temperature of the test setup.

2. **AC Testing at Elevated Voltages and Frequencies**
   At higher frequencies and voltages, the capacitive nature of the arrester causes an increase in total current. To avoid overheating, testing durations were limited—especially when approaching or exceeding the rated voltage.

3. **Temperature Control Between Tests**
   After each test, blocks were cooled to room temperature before the next measurement. This helped maintain consistency and reduced the influence of thermal effects on test accuracy.

4. **DC-Induced Heating**
   A DC current of approximately 10 mA was found to raise the block temperature to around 100°C within 10 minutes. To avoid excessive heating and ensure reliable data, DC tests were kept brief. All DC tests were performed under stable temperature conditions. The V–I characteristics of the arrester are temperature-dependent, requiring consistent thermal control.

3.3.3. Calibration of test equipment

The amplifier was calibrated to ensure accurate voltage measurements, as the voltage was measured at the amplifier rather than directly at the test point. The resistance of the high-voltage connection cables might introduce a minor measurement error between the voltage at the HV electrode and the voltage measured at the amplifier.
Figure 3.8 shows the calibration setup. A voltage probe (with a gain factor of 1/1000) was used to measure the high-voltage output from the cable, which was then compared to the output voltage of the amplifier (with a gain factor of 1/3000).

Calibration was performed at different frequencies and voltages. Graph 3.9 presents the calibration results at two different frequencies (50 Hz and 1000 Hz). The X-axis shows the peak-to-peak applied voltage, while the Y-axis represents the deviation of the HV amplifier output from the HV probe measurements. The maximum deviation was around 4 percent for the peak-to-peak voltage, with a general trend of fluctuations across different voltage levels.

Graph 3.10 illustrates the average voltage deviation for each voltage level as a function of frequency. The X-axis represents the frequency, while the Y-axis shows the average voltage deviation for each frequency level. The line graph indicates a maximum deviation of approximately 3.5 percent for peak-to-peak voltage at a frequency of 50 Hz. Notably, the average deviation decreases as the frequency increases, reaching a very small value at 1000 Hz."

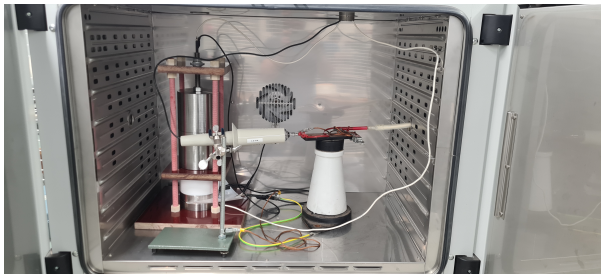

Figure 3.8: Calibration setup

In addition, the current calibration was not done in this test since the shunt was already calibrated previously.

3.3.4. Measurement Repeatability and Test Consistency

Many variables, such as temperature, can influence the characteristics of surge arrester blocks during testing. As discussed in the introduction, the voltage–current characteristic of the block is highly temperature-dependent. Other factors, such as contact resistance between the electrodes and the block, may also affect the measurements.

To ensure data reliability, each test was repeated at least three times. Any measurements showing significant deviation from the average were discarded and repeated. This process of repeated testing improves the accuracy of data used for both modelling and analysis.

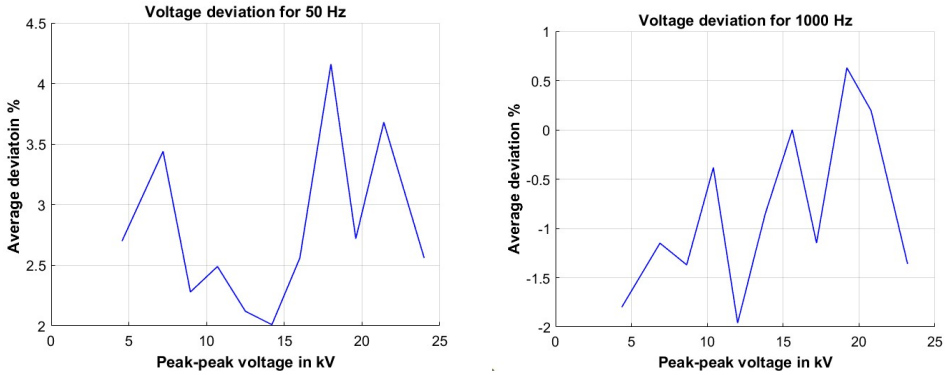

Figure 3.9: Calibration results(Average voltage deviation) for 50 Hz and 1000 Hz.

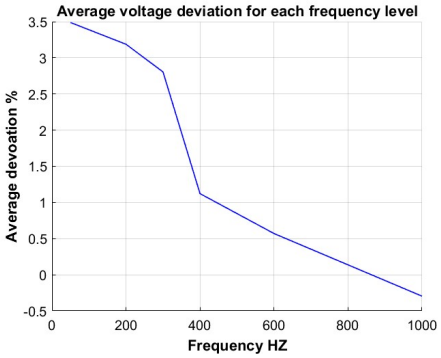

Figure 3.10: Average deviation for each voltage level as a function of frequency

1) Repeatability of Frequency–Current Tests

Figure 3.11 presents the current measured through the block as a function of frequency, performed at three different voltage levels. The highest applied voltage in this test was 3 kV, corresponding to the rated voltage of the tested block. This frequency sweep test was performed on the first block only.

At each voltage level, the frequency was varied between 50 Hz and 1000 Hz. Each measurement was repeated three times, and the block was removed from the setup after each run to ensure consistent electrical contact.

As shown in Figure 3.11, for frequencies between 50 Hz and 500 Hz, the test results demonstrated strong repeatability. The deviations from the average were minimal and considered negligible.

2) Repeatability of Voltage–Current Relationship

The second test focused on verifying the repeatability of the voltage–current characteristics and was performed on a different block wiht a rated voltage of approximately 6.12 kV RMS. This AC test aimed to ensure that voltage–current measurements remained consistent despite minor changes, such as testing on different days or repositioning the block.

As shown in Figure 3.12, tests were conducted at three different frequencies: 50 Hz, 150 Hz, and 500 Hz. The applied voltage ranged from approximately 2700 V up to over 10.5 kV peak, exceeding the block's rated peak voltage of 8.65 kV. The results showed only minor differences between individual tests and their averages, confirming high repeatability and stability of the measurements.

3.3.5. Polarizaiton/Depolarization

During testing, all blocks showed a high degree of polarization, induced by the surge testing, which was accompanied by high surge currents (done by the manufacturer). In contrast, blocks in service do not experience continuous polarization, as they naturally depolarize under the continuous operating voltage. To obtain results that accurately represent in-service arresters, this polarization must be eliminated.

Figure 3.14 shows that polarization mainly affects the resistive characteristic of the block. At low voltages, the capacitive current dominates, with the sinusoidal current leading the voltage by 90 degrees. As the voltage

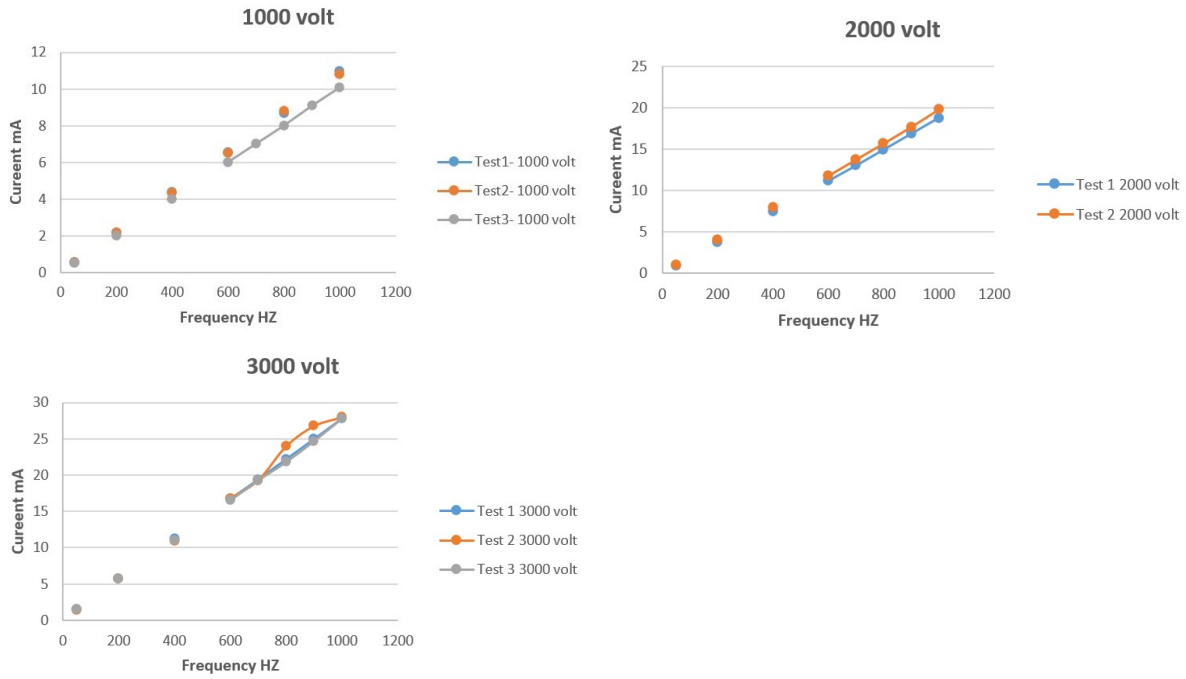

Figure 3.11: Repatibility test for 3 different voltage levels and a frequency from 50 to 1000 Hz.

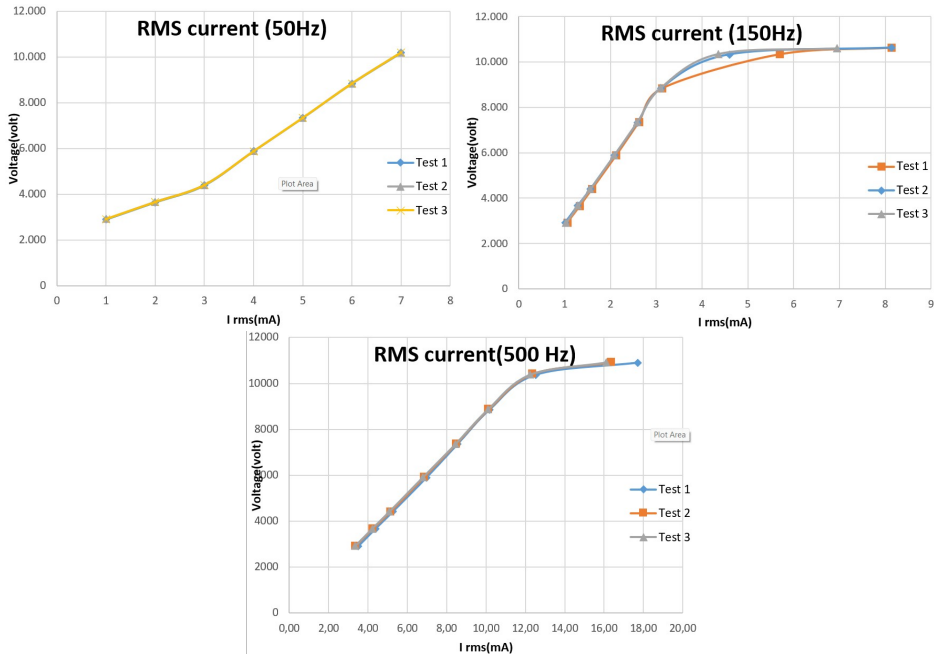

Figure 3.12: V-I curve for 3 frequencies (50, 150, 500) with 3 different tests for each frequency(current in rms and voltage in peak).

increases, the resistive current becomes more noticeable, appearing as a second peak that is in phase with the voltage. Figure 3.13 demonstrates that polarization has a significant impact on the resistive current, with the negative current peak being 40% higher than the positive peak.

The following procedures were attempted to depolarize the blocks:

1) **AC depolarization test:**
An AC voltage, slightly higher than the continuous operating voltage, was applied to the tested blocks. Each

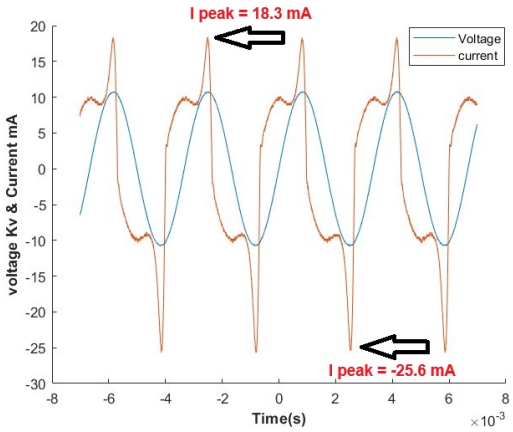

Figure 3.13: Polarization effect on the current

test lasted around two hours, with breaks in between to prevent excessive heating and to allow for inspection of the test setup. Despite nearly 30 hours of total testing time, the polarization was reduced but not completely eliminated. This demonstrated that AC depolarization is a slow and time-consuming process, highlighting the need for a more efficient alternative.

2) **DC depolarization test:**

Another approach involved using a DC current, so DC tests were applied to the blocks. The results were significant, as the depolarization process required only one to two hours of continuous DC current application. This method proved to be much faster and more effective than AC, efficiently realigning the dipoles to their original state.

The applied current was set at approximately 10 mA. Due to the high temperatures generated during testing, careful monitoring was necessary. To prevent overheating, 10-minute breaks were introduced after every 15 to 20 minutes of operation.

3.3.6. AC testing

This test was conducted at room temperature across four different frequencies: 50 Hz, 150 Hz, 300 Hz, and 500 Hz. For each frequency, voltage measurements were taken at six to seven levels, ranging from approximately 2.5 kV peak to 10.2 kV peak (within the reference voltage range of 9.2 kV to 10.5 kV peak). Figure 3.14 illustrates data from three measurements at three different voltage levels, with voltage shown in blue and current in red, all measured at a frequency of 150 Hz. The AC test was performed with a total current reaching up to 10 mA RMS for high voltages. In some cases, testing was extended slightly beyond this limit, with currents reaching up to 20 mA RMS.

When AC voltage was applied under different frequencies, the only limitation was the amplifier current (a maximum of 40 mA peak). Initial experiments were done to determine the optimal setup and oscilloscope setting to obtain good-quality measurement results for the analysis, including different oscilloscopes and data resolutions. During testing, it was found that:

a) The oscilloscope's averaging function was ineffective in removing noise from the captured signal due to inaccurate changes of the voltage and current peak, often cutting off peak values. As a result, filtering the noise in MATLAB proved to be a better approach.

b) The sampling frequency and time range of the oscilloscope were chosen to ensure optimal data quality. A balance was needed between capturing enough data points to effectively reduce noise and avoiding an excessive number that would make analysis too time-consuming. The selected data points ranged between 20,000 and 50,000 for every four cycles of the voltage wave.

3.3.7. DC measurements

DC testing was used to directly measure the block resistance since it eliminates the capacitive current and any dielectric losses. DC voltage can be easily generated using a signal generator and an amplifier. Although the signal generator doesn't have a DC waveform,A DC signal can be generated using the following method:

1. Applying an AC sinusoidal waveform with a very low frequency (in the millihertz range) with a small

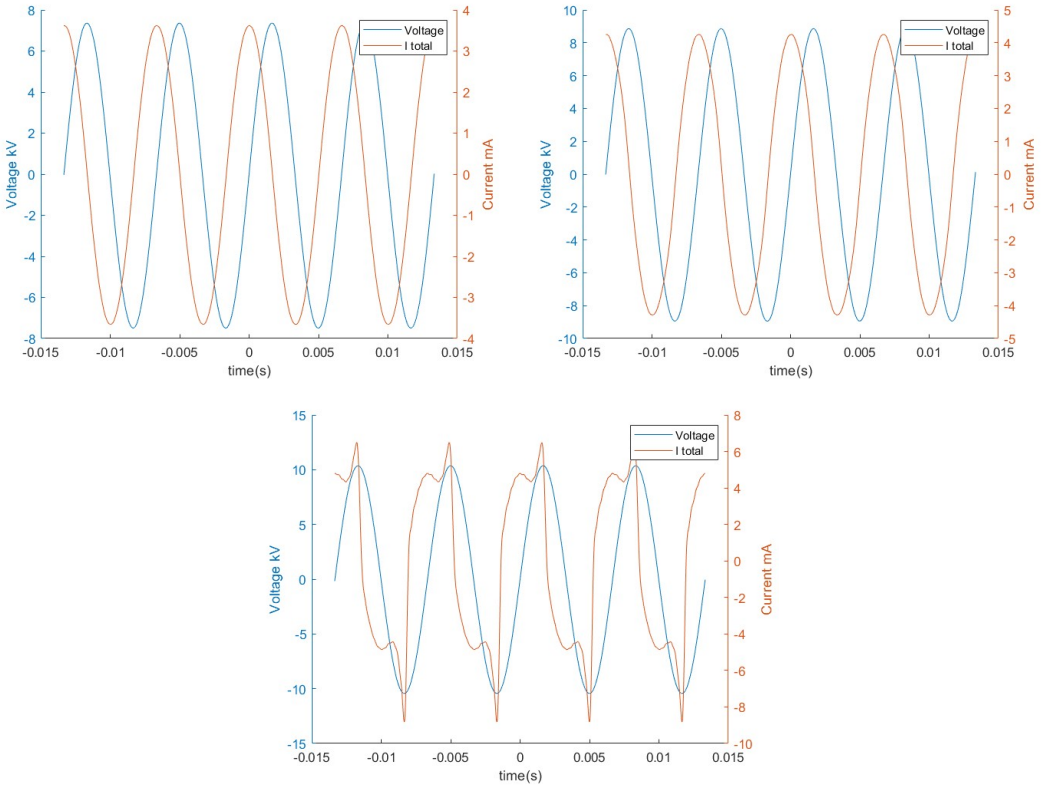

Figure 3.14: AC Testing Data for 150 Hz frequency and 3 voltage levels (7.4 8.9 and 10.3 kV)

amplitude (in the millivolt range).

2. Superimposing the AC signal with a DC offset of kilovolt amplitude to produce the desired DC waveform.

During testing, obtaining accurate DC results using a standard oscilloscope was challenging due to high noise levels in the signal. Therefore, a multimeter was used to measure the DC values more reliably.

Figure 3.15 shows the highest recorded value, approximately 16 volts, corresponding to a current of 16 mA.

Figure 3.15: DC current measurements showed a value of 16 mA, recorded using a multimeter.

Test 1		Test 2		Test 3	
V DC	I DC	V DC 2	I DC 2	V DC 3	I DC 3
2916	0,00005	2856	0,00005	2910	0,00005
4428	0,00011	4404	0,00015	4410	0,00014
5850	0,0005	5850	0,00066	5919	0,00066
7383	0,00349	7380	0,0044	7410	0,00485
8871	0,083	8865	0,093	8730	0,112
10110	14,6	10107	14,45	10110	16,63

Figure 3.16: DC testing results in voltage and milli Amps

DC testing was performed three times for each voltage level to improve the accuracy of the results(see table 3.16). The arithmetic average for the current was calculated for each voltage level, and the deviation from the mean for each measurement was within an acceptable range of 0% to ±17%.

Figure 3.17 presents the results of three different tests, using logarithmic values to highlight the nonlinearity.

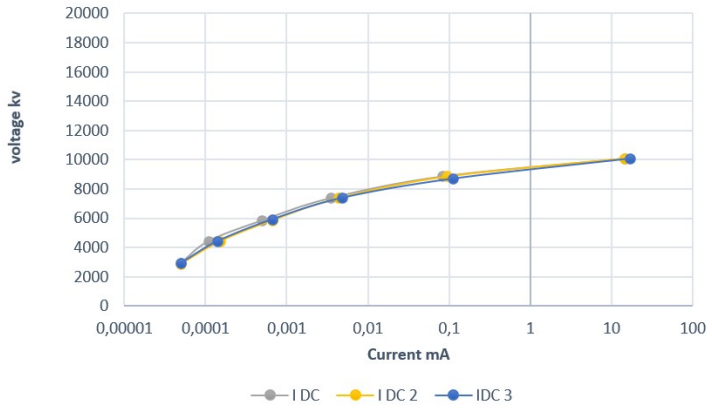

Figure 3.17: DC testing results for 3 different measurements

3.4. Conclusion

- The experiments highlighted the critical impact of depolarization effects, which can introduce substantial imbalances in voltage and current measurements if not properly addressed during testing.
- AC testing provided detailed voltage and current waveforms across multiple frequencies and voltage levels, which were crucial for analysing the surge arrester block characteristics.
- DC measurements were successfully performed to develop the nonlinear branch of the electrical model(RDC), which is always represented by a voltage-current relation.
- The accuracy of DC measurements can be improved in future work by increasing the number of data points for better curve fitting.
- Overall, the testing procedures formed a robust foundation for both evaluating the surge arrester's behavior and constructing an accurate electrical model further.

4

Analysis of modelling and testing results

4.1. Introduction

A new electrical model for representing metal oxide arrester blocks is being developed, which accounts for both voltage and frequency dependency of its characteristics. Several surge arrester models were introduced by researchers to represent SA characteristics in the high current region, particularly for being used in over-voltage studies. However, these models are not optimized to accurately represent the SA block behavior and its frequency dependency in the low current region. This highlights the need for a new model to study the impact of frequency variations caused by harmonic distortions on surge arresters.

4.2. Electrical models for surge arresters

4.2.1. Fast front surges model

This model represents the behavior of the surge arrester in the high-current region when it is subjected to fast-front overvoltages.[11] Figure 4.1, Circuit A, represents the equivalent electrical circuit of a simplified model consisting of three series elements: Ri, the nonlinear resistance; RT, the turn-on linear resistance; and L, the inductance of the current path. RI can be determined from the discharge voltage under 8/20 μs current impulses at different peak levels.

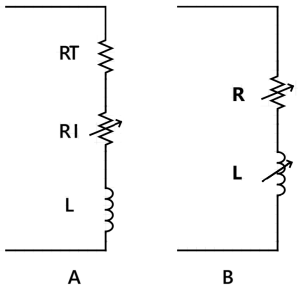

Figure 4.1: MO surge arrester models for fast front surges

Hysteretic model: Since the discharge voltage of a metal oxide surge arrester reaches its peak earlier than the discharge current, Circuit B in Figure 4.1 represents this hysteretic model, capturing the dynamic, frequency-dependent behavior by adding an inductance in series with the nonlinear resistance. This adjustment replicates the response of MO blocks under high-frequency discharge currents.

4.2.2. IEEE model

The IEEE model also represents the surge arrester behaviour in the high current region, but is slightly more complex than the previous one.[11] Figure 4.2 illustrates the IEEE electrical model for surge arresters under fast front surges, incorporating the following components:
two time-independent nonlinear resistors (A0 and A1), two linear inductors (L0 and L1) in parallel with two linear resistors (R0 and R1), and a single capacitor (C).

The characteristic V-I curve of A1 is slightly lower than the 8/20 μs curve, while the curve A0 is slightly higher. L1 and R1 function as a low-pass filter, with the voltage across them appearing as a decaying voltage.

Additionally, an inductance of approximately 1 μH/m must be added in series with the model. For transient simulations, the non-linear resistors should be modelled and approximated using an exponential segment, as described in the following equation.

$$i = p * (\frac{v}{Vref})^q \tag{4.1}$$

q: is an exponent
p: is a multiplier
Vref: is an arbitrary reference voltage that normalises the equation.

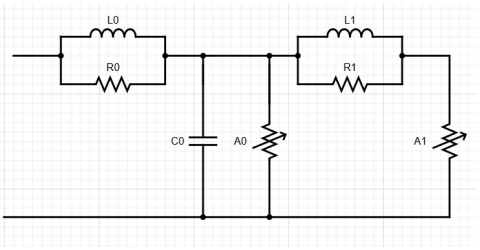

Figure 4.2: The IEEE MO surge arrester electric model for fast front surges,

4.2.3. CIGRE model

The CIGRE model, shown in Figure 4.3, represents the arrester's behavior in both low- and high-current regions [11]. It serves as a strong foundation for developing our own model, as it incorporates an electrical representation of the grain boundary, an essential factor when analysing power losses under temporary overvoltages.

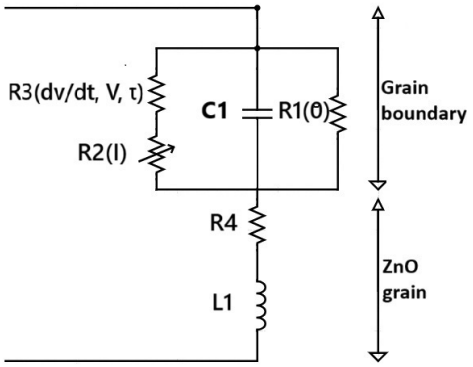

Figure 4.3: CIGRE model, the closest predicted Electrical model of the surge arrester under the testing conditions

This model consists of two parts: one representing the grain boundary and the other representing the ZnO grains.

- **Grain Boundary:** Determines the arrester behavior in the low- to medium-current region when subjected to normal operating voltages and temporary overvoltages.
- **ZnO Grains:** Governs the arrester behavior in the high-current region, when the arrester conducts surges.

The grain boundary model consists of three parallel branches, representing the voltage-dependent behavior of the grain boundary, where:

- $R_1(\theta)$ represents a linear temperature-dependent resistance.
- $R_2(I)$ is the non-linear, voltage-dependent characteristic of the boundary layer.
- $R_3\left(\frac{dv}{dt}, V, \tau\right)$ is the turn-on resistance (steady-state current-dependent resistance).
- C_1 represents the overall capacitance of the surge arrester intergranular layers.

The electrical characteristics of the bulk material of ZnO grains are represented by a resistance, R_4, and an inductance, L_1. The inductance, L_1, is approximately 1 µH/m and depends on the geometry of the current path through the overall surge arrester model as well as the internal structure of the surge arrester blocks.

For this work, the grain model can be ignored due to its low impedance value compared to the boundary layer.

4.3. Model Development Methodology

This section outlines the methodology followed to develop the surge arrester model in the low-current region. The process is divided into two main stages: the analysis of testing results and the modelling process. The goal is to accurately extract the electrical parameters of the arrester using measured data and refine the model to account for frequency and voltage dependency, as required for temporary overvoltage (TOV) studies. Several models exist for representing surge arresters, but for the low-current region, the CIGRE model is particularly suitable. Among the models introduced in this study, it is the only one capable of capturing both the low- and high-current behavior of the arrester. However, because it does not account for frequency dependence in the low current region, certain modifications were necessary to improve its accuracy. Figure 4.4 illustrates the overall methodology used to extract the elements of the surge arrester's electrical model, which consists of two main steps:

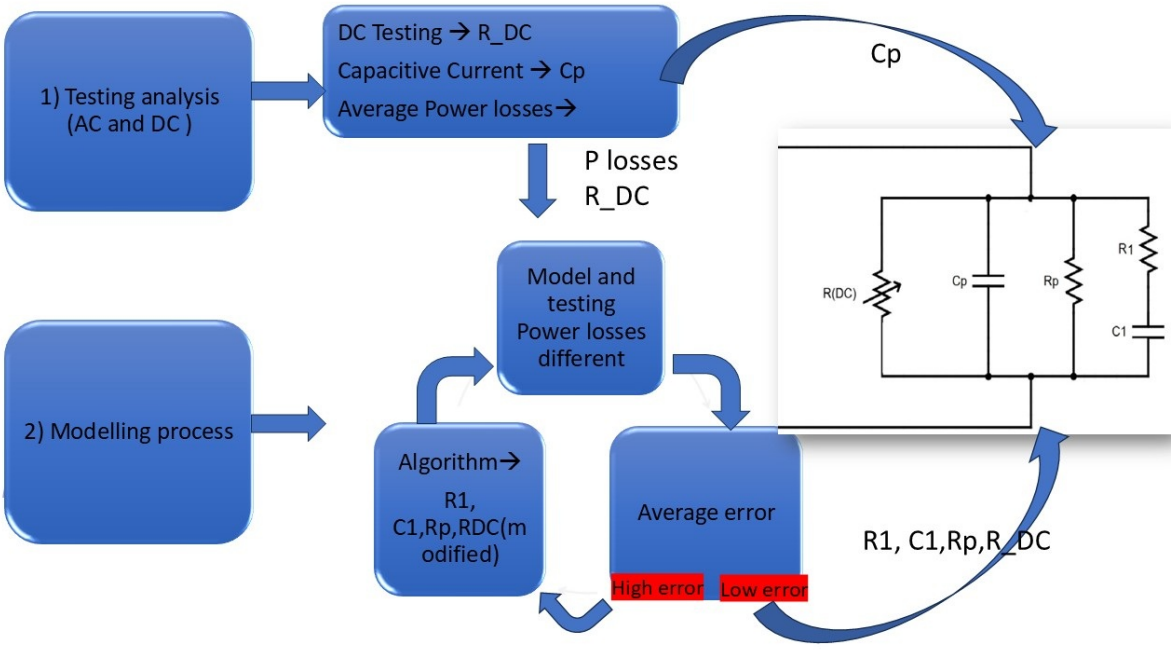

Figure 4.4: The process of getting the electrical model and the proposed electrical model on the left

Testing Results Analysis

In this step, the results from AC and DC testing were analyzed to extract a key characteristics of the arrester. This included determining the nonlinear resistive branch, the average power losses, and the parallel capacitance Cp.

1. **Fourier Filtering and Signal Processing**
   Voltage and current signals were filtered to remove high-frequency noise and reconstruct the fundamental waveforms.

2. **Current Decomposition**
   The total current was separated into capacitive and resistive components using the voltage derivative and extracted capacitance.

3. **Power Loss Calculation**
   Average power losses were computed by integrating the instantaneous power over time.

4. **Impedance and Frequency Analysis**
   Total impedance was analyzed across frequencies to confirm capacitance and study the resistance variation.

5. **Nonlinear Curve Fitting**
   DC Voltage-current characteristics were interpolated to form a nonlinear resistance curve used in modelling.

Modelling Process

The second step involves the development of the electrical model. An optimization algorithm was employed to minimize the error between the measured and simulated average power losses. Through this process, the nonlinear branch was refined, and the model parameters, R(DC) ,R1, C1, and Rp, were extracted.

1. **Initial Two-Branch Model**
   A simple model with one capacitive and one nonlinear resistive branch was built to capture either voltage or frequency dependence.

2. **Four-Branch Model Development**
   An extended model based on a modified CIGRE structure was created to account for both voltage and frequency dependencies.

3. **Parameter Optimization**
   A genetic algorithm was used to optimize the model parameters by minimizing the error between measured and simulated losses.

4. **Nonlinear Branch Refinement**
   The nonlinear current component was adjusted to improve the model fit across all test conditions.

5. **Final Model Evaluation**
   Model accuracy was validated by comparing power loss and RMS current results with test data across multiple voltages and frequencies.

4.4. Testing Results Analysis

4.4.1. Fourier Filtering and Signal Processing

Fourier analysis was employed for two main purposes:

- **Noise reduction:** High-frequency noise in the voltage and current signals was mitigated using Fourier transformation. The signals were transformed into the frequency domain, filtered by retaining only the fundamental harmonics, and then reconstructed. This filtering process is demonstrated in Figure 4.5 for voltage, and Figures 4.6 and 4.7 for current.

  Fourier analysis decomposes the voltage and current signals from the time domain into the frequency domain, representing them as a sum of sine and cosine waves. By selecting only the first few harmonics of the decomposed signal, high-frequency noise was eliminated while preserving the essential measurement data.

  Different numbers of fundamental harmonics, ranging from the first 1 to 30, were tested to find an optimal balance between noise reduction and signal accuracy. It was found that for voltage signals,

using only the first 1 to 10 harmonics (i.e. 50 to 500 Hz) provided the best results, as accurate voltage data was crucial for correctly extracting the capacitive current through differentiation(see figure 4.5).

However, for current signals, it was not possible to reconstruct the waveform using only one harmonic(50Hz), particularly at higher current levels where the waveform is non-sinusoidal. Instead, up to 20 harmonics were used to effectively reconstruct the signal while minimizing noise(see the results in figure 4.6 and4.7).

- **Extraction of capacitive current:**Fourier analysis facilitated the differentiation of the voltage signal, allowing for the accurate extraction of the capacitive current component.

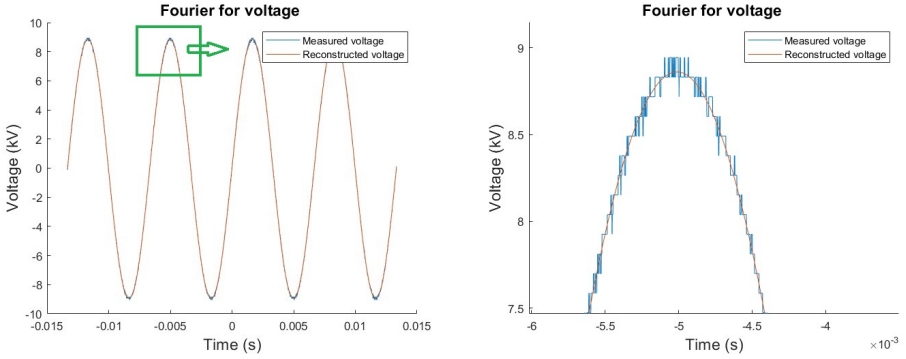

Figure 4.5: Fourier analysis for filtering high-frequency noise in the voltage wave.

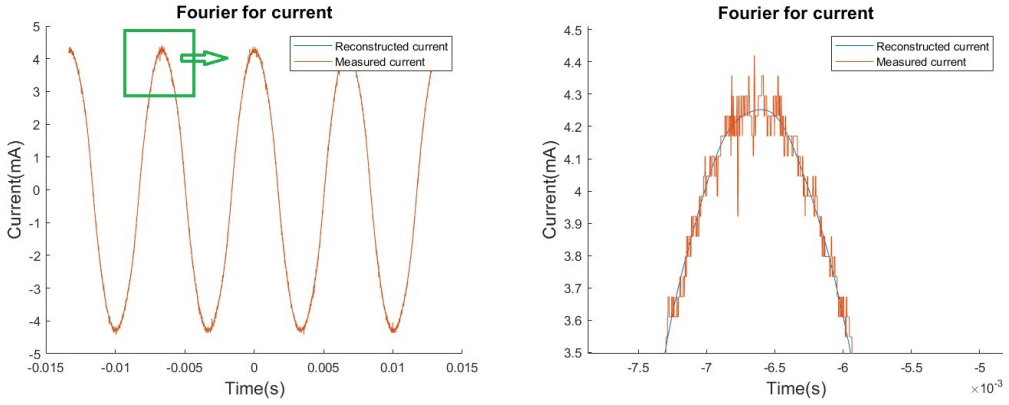

Figure 4.6: Fourier analysis for filtering high-frequency noise in the current wave.

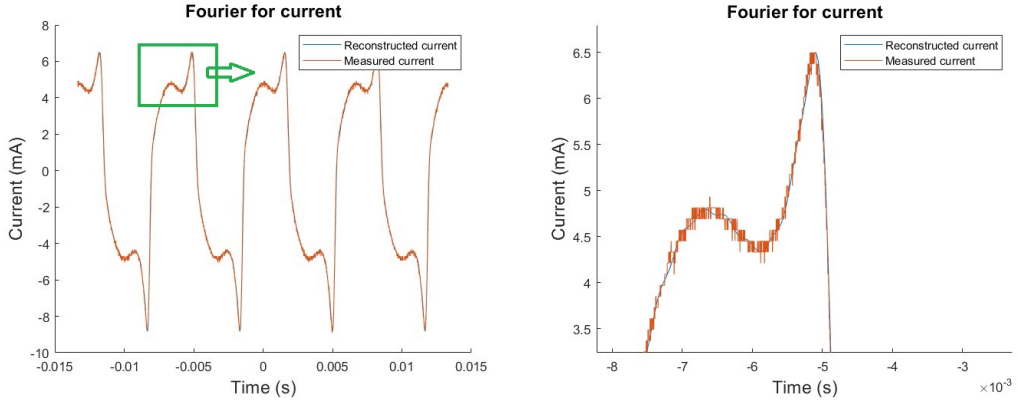

Figure 4.7: Fourier analysis for filtering high-frequency noise in non-sinusoidal current waves.

4.4.2. Decomposing the Total Current in Capacitive and Resistive components

Deriving the Capacitive current: In Graph 4.8, the capacitive current was obtained by differentiating the voltage, as described by the following equation:

$$I_c = C \cdot \frac{dV}{dt} \tag{4.2}$$

I_c Capacitive current (A).

C Total capacitance (F).

$\frac{dV}{dt}$ Rate of change of voltage.

Since the exact value of the capacitance C was not directly available, an alternative method was developed. Instead of calculating the capacitive current using $I_C = C \cdot \frac{dV}{dt}$ with a known C, the approach relied on scaling the differentiated voltage waveform to match a known reference.

It is known that the peak of the capacitive current occurs when the voltage crosses zero. Therefore, the total current at the zero-crossing point of the voltage waveform was recorded and used as a reference to scale the differentiated waveform.

Consequently, an average capacitance value of approximately **0.53 nF** was obtained. This estimated value was later validated by comparing it with the total impedance derived from the testing results.

Figures 4.10 and 4.9 illustrates the final results for two different voltage levels at a frequency of 150 Hz, showing the measured voltage and current signals in the graphs on the left and the decomposition in capacitive and resistive current components on the right.

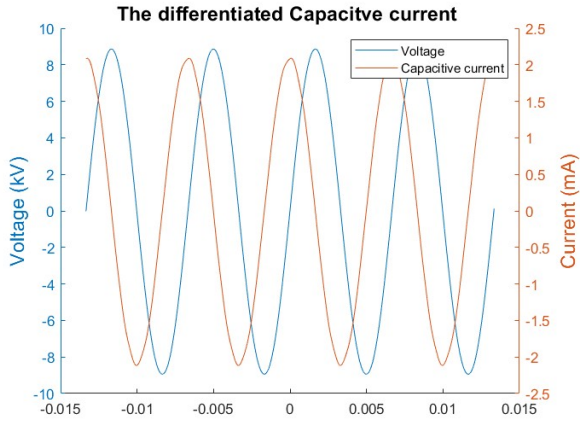

Figure 4.8: Final Capacitive current extraction from voltage wave

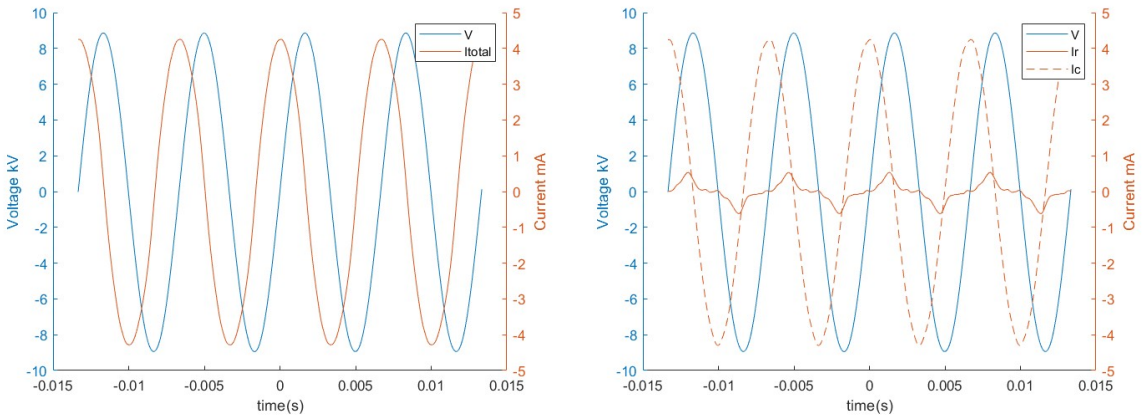

Figure 4.9: Total current on the left, extracted resistive and capacitive current on the right(voltage at 8.8 kV and 150 Hz)

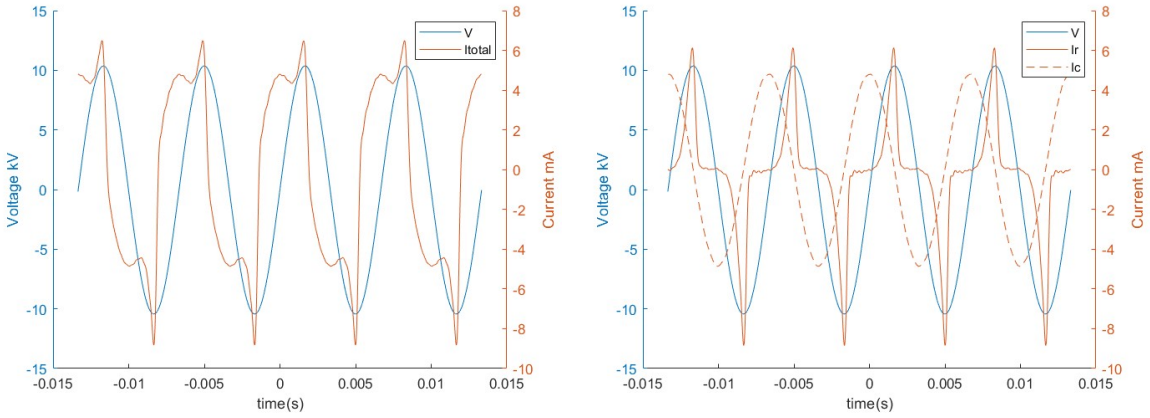

Figure 4.10: Total current (left) and extracted resistive and capacitive currents (right) at 10,4 kV and 150 Hz.

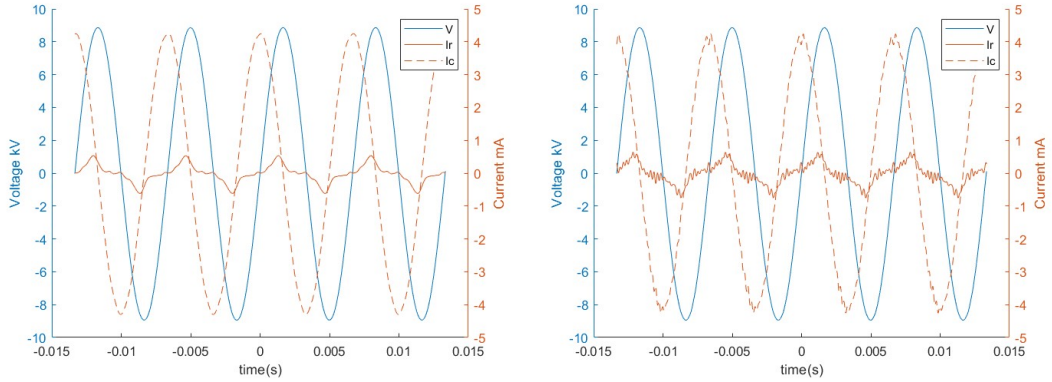

Figure 4.11: Fourier analysis to obtain the capacitive current using 10 harmonics on the left and 30 on the right

Resistive current Calculation: The resistive current was obtained by subtracting the derived capacitive current from the total current signal. It consists of both linear and non-linear components, represented by R1 and R2+R3 in the CIGRE model, respectively. This resistive current served as a reference for comparison with the resistive current of the final model, helping to evaluate and enhance the model's overall accuracy. Figure 4.12 presents the voltage and current waveforms on the left, while the extracted capacitive and resistive currents (Ic and Ir) are shown on the right. The figure illustrates measurements at three different voltage levels: 7.4 kV, 8.8 kV, and 10.3 kV. As the total current increases with voltage, the resistive current specifically

becomes more pronounced and non-linear.

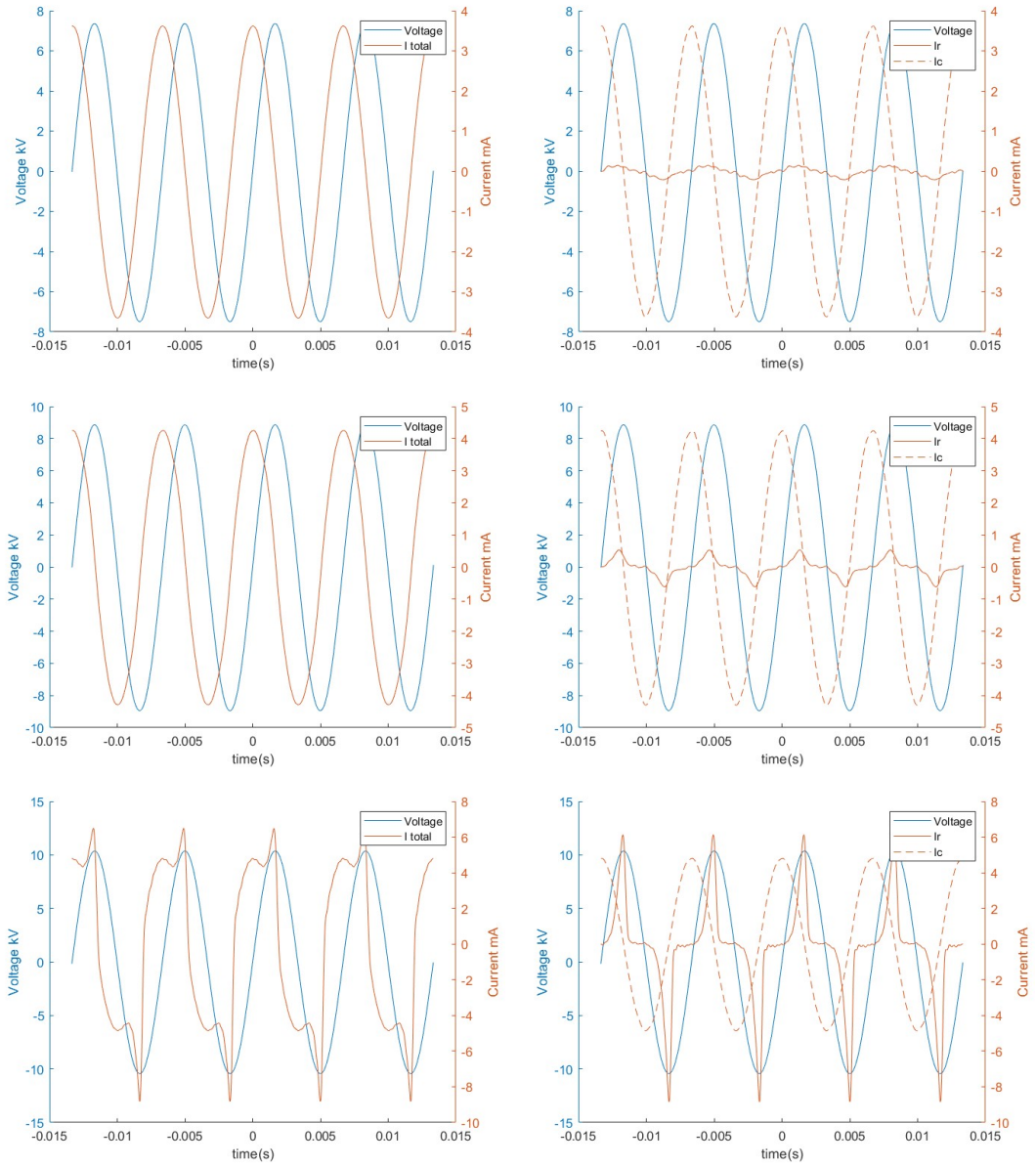

Figure 4.12: Illustration of the current increase at voltage levels of 7.4 kV, 8.8 kV, and 10.3 kV. On the right side, the total current is decomposed into its resistive and capacitive components.

Figure 4.11 illustrates the effect of noise on the extracted resistive and capacitive currents. The right side of the figure shows that increasing the number of harmonic components used to reconstruct the measured signals also increases the noise in the extracted currents.

4.4.3. Power Loss Calculation

The average power losses from the test were used as a reference to develop the electrical model. In Graph 4.13, the total power was calculated by multiplying the voltage and current waveforms. The graph clearly shows the change in the total power as the voltage rises.

By integrating the total power waveform and dividing it by time, the average power losses were determined. These losses were calculated for each voltage level and across the four tested frequencies to assess the impact of higher frequencies.

Figure 4.14 illustrates the increase in power losses due to higher-frequency testing. At each voltage level, power losses were found to be higher at increased frequencies. For instance, at the highest voltage level of approximately 8.9 kV, power losses rose from around 1 watt at 50 Hz to about 3 watts at 500 Hz. This significant increase suggests that higher frequencies could lead to temperature rises in the blocks, placing additional thermal stress on the surge arrester. Over time, this added stress may accelerate the aging process of the surge arrester blocks under non-standard operating conditions. [1]

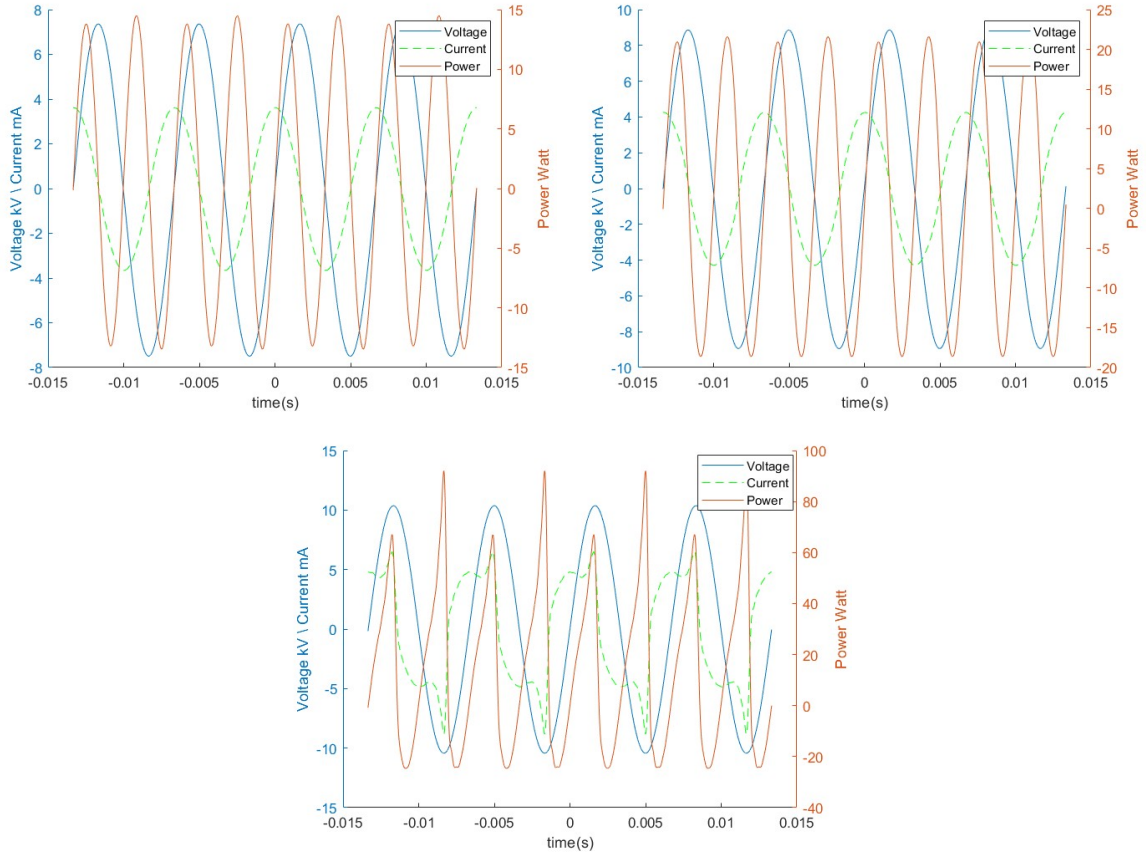

Figure 4.13: Total power at three different voltage levels: 7.4 kV, 8.8 kV, and 10.3 kV.

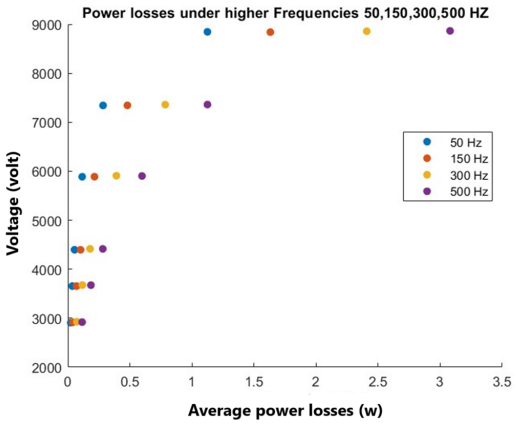

Figure 4.14: Average power losses increase with higher frequencies across different voltage levels.

4.4.4. Results according to the total impedance

Analysis of the testing results allows for the calculation of the average power losses and the value of both the voltage and current in the phasor domain, and then the total impedance of the surge arrester Z-total was calculated according to the following equations:

$$P_{\text{losses}} = V_{\text{rms}} \cdot I_{\text{rms}} \cdot \cos(\theta) \tag{4.3}$$

$$I_{\text{rms,phasor}} = I_{\text{rms}} \cos(\theta) + I_{\text{rms}} \sin(\theta) \cdot j \tag{4.4}$$

$$Z_{\text{total}} = \frac{V_{\text{rms}}}{I_{\text{rms,phasor}}} \tag{4.5}$$

- $\mathbf{P_{losses}}$: Average power losses (W).
- $\mathbf{V_{rms}}$: Root-mean-square (RMS) value of the voltage (V).
- $\mathbf{I_{rms}}$: Root-mean-square (RMS) value of the current (A).
- $\boldsymbol{\theta}$: Phase shift between voltage and current in the phasor domain (radians).
- $\mathbf{I_{rms,phasor}}$: Root-mean-square (RMS) value of the current in the phasor domain (A).

By extracting the resistance and capacitance values from the total impedance of the surge arrester blocks, the results show the following: According to Figure 4.15, the total capacitance remains nearly constant and does not show any significant dependency on either frequency or voltage, up to a peak voltage of 9 kV. In contrast, as illustrated in Graph 4.16, the total resistance exhibits noticeable variation with changes in both voltage and frequency, indicating a clear dependency on these parameters. Specifically, the reduction in resistance observed at 500 Hz correlates with an increase in power losses, as shown previously in Figure 4.14.

Moreover, the total capacitance values in Figure 4.15 average slightly above 0.5 nf, which closely aligns with the previously estimated capacitance obtained from waveform analysis. The capacitance values observed beyond 9 kV reflect a different behaviour, attributed to the onset of the second region of the V–I characteristic. However, this region was beyond the scope of the current study and was therefore not considered in the analysis.

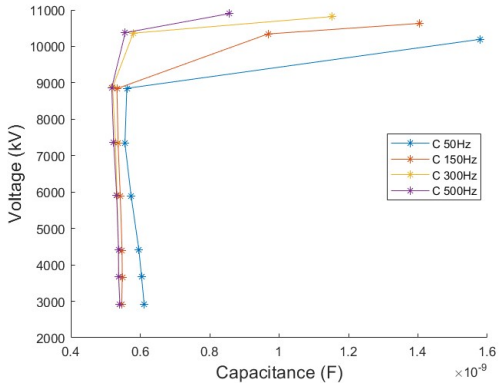

Figure 4.15: The changes in the total capacitance of the tested block under different frequencies,

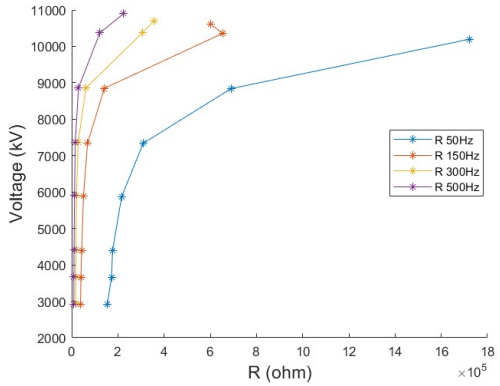

Figure 4.16: The changes in the total resistance of the tested block under different frequencies,

4.4.5. Nonlinear Curve Fitting

The DC voltage–current relationship was used as a representative for the non-linear resistance of the surge arrester block (corresponding to R2 + R3 in the CIGRE model). The non-linear branch can potentially be extracted from the DC testing results. To do this, curve fitting was applied to interpolate between the measured points and generate the non-linear current waveform. The power function used to fit the DC testing results for the non-linear resistance is given by:

$$I_{\mathrm{DC}} = A \cdot V^{B} + C \tag{4.6}$$

- I_{DC} **(A):** The resulting direct current (DC) through the surge arrester block.
- V **(V):** The applied DC voltage across the component.
- A **:** A scaling factor that defines the amplitude of the current response to the voltage.
- B **:** The exponent that determines the degree of nonlinearity in the current–voltage relationship.
- C **:** An offset current that accounts for any baseline or leakage current not dependent on the voltage.

DC curve fitting:

Figure 4.17 illustrates a power function fitted to the DC testing data points.

Curve fitting Results:

The previously fitted curves are used to generate the nonlinear DC current. This is essential for extracting the power losses of the nonlinear branch, which will later be used to refine the final electrical model (see the waveforms in Figure 4.18).

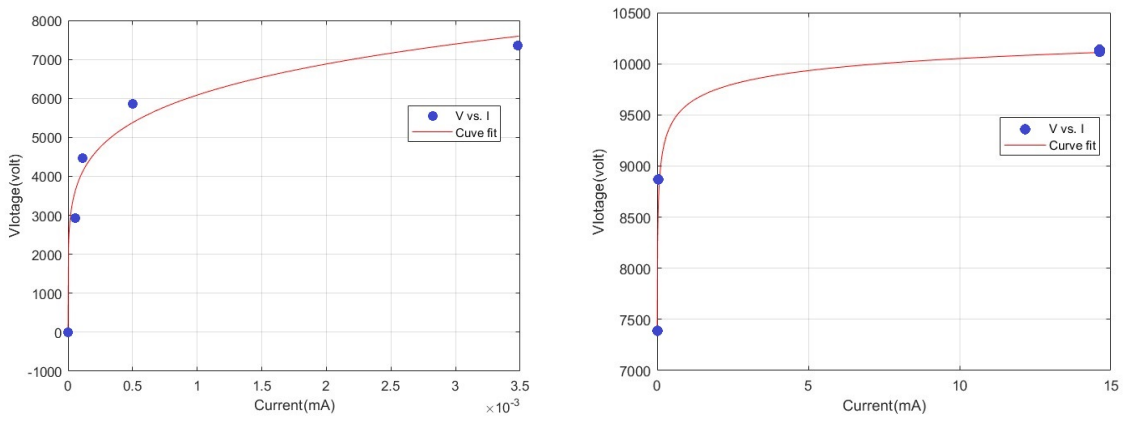

Figure 4.17: Curve fitting using a power function

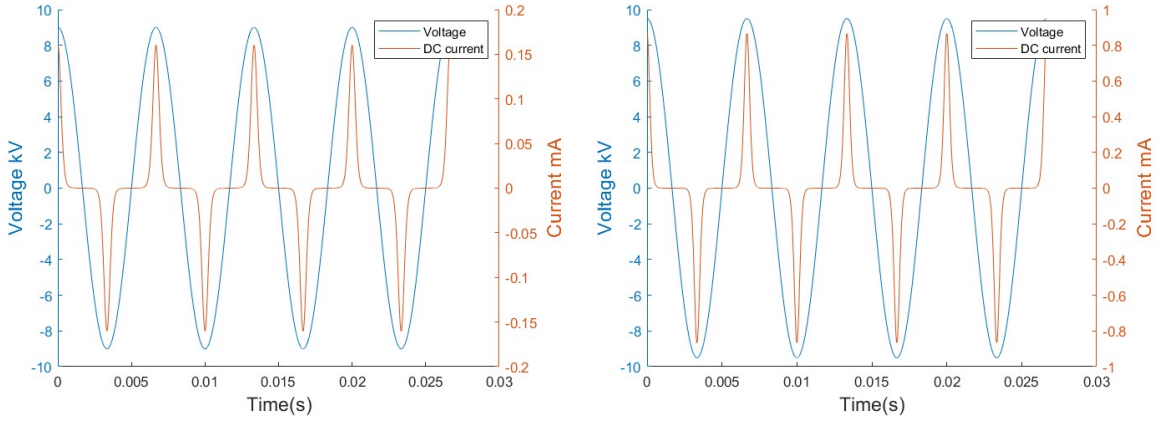

Figure 4.18: Generated Non-Linear DC Current Using Two Curve-Fitting Equations, Showing Results for Waves at Peak Voltage Levels of 9 kV (Left) and 9.5 kV (Right)

4.5. Modeling Process

4.5.1. Electrical Model Developments

1) Two-Branch Model

The first approach explored whether it was possible to build a model using only two branches—a DC and an AC branch—as shown in Figure 4.19. One branch represents the nonlinear DC resistance, while the other branch represents the grain boundary using a linear RC branch. This method was based on using the previously extracted total impedance and nonlinear DC resistance. The fitting results, shown in Figure 4.20, demonstrate a good match between the test data and the model across four different frequencies at a single voltage level, with only minor errors observed. Similarly, Figure 4.21 shows acceptable results for one frequency across six different voltage levels, again with only small differences in power loss between the model and the measurements. However, a major limitation of this simple two-branch model is its inability to accurately reflect power losses across all voltage levels and all frequencies. Since the error between the model and the test data becomes significantly larger and unacceptable.

2) Four-Branch Model

Fitting both frequency and voltage dependency into a simple two-branch model proved to be unfeasible. As a result, the CIGRE model was adopted. The grain model was excluded due to its low impedance compared to the boundary layer. Several modifications were made to the original structure, including the addition of an extra RC branch (R1 and C1) to account for the frequency-dependent impedance, as shown in Figure 4.22.

The average power losses from the test were used as a reference to guide the development of the electrical model. Since the total capacitance remained nearly constant across all voltage levels and frequencies, its value was approximated as 0.5 nF (represented by Cp). The remaining component values were determined

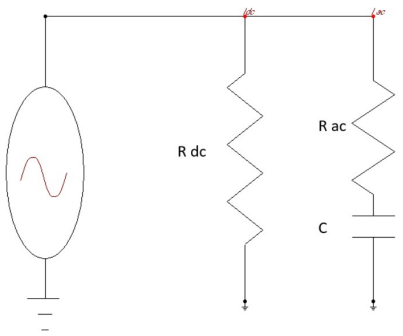

Figure 4.19: The first predicted Electrical model of the surge arrester.

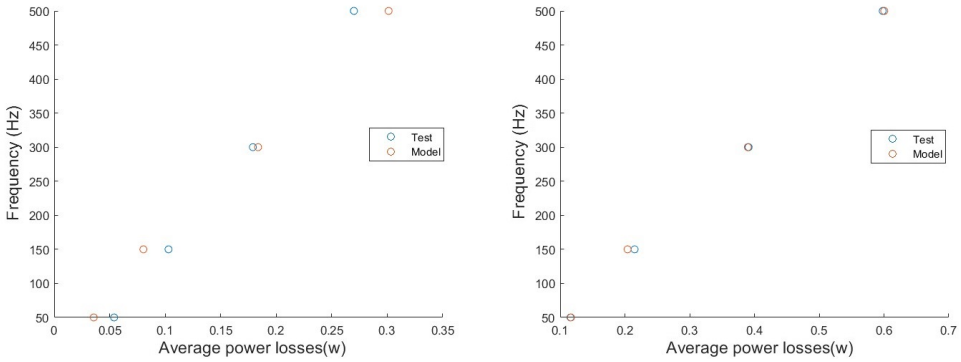

Figure 4.20: Average power losses comparison between testing and modeling across **one voltage** levels and **4 frequencies**, using a two-branch model at 4.4 kV (Left) and 5.9 kV (Right)

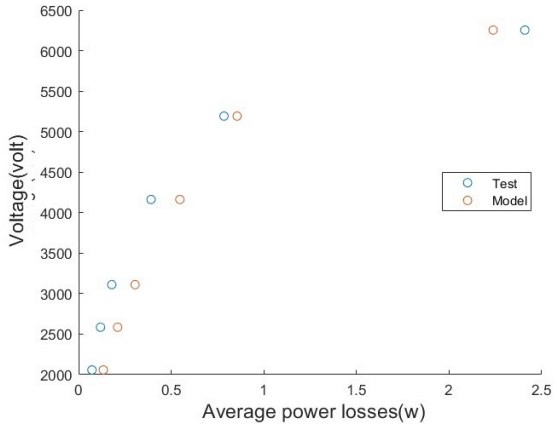

Figure 4.21: Average power losses comparison between testing and modeling across **six voltage** levels and **one frequency**, using a two-branch model

using an optimization algorithm that adjusted the parameters to minimize the difference between the average power losses of the model and those observed in the test.

While a basic MATLAB script was sufficient to construct a two-branch model that captured either frequency or voltage dependence, its accuracy was limited and the resulting errors were relatively high. To achieve a more accurate representation of the behavior across all six voltage levels and four frequencies, a more advanced optimization technique—such as the genetic algorithm—was implemented.

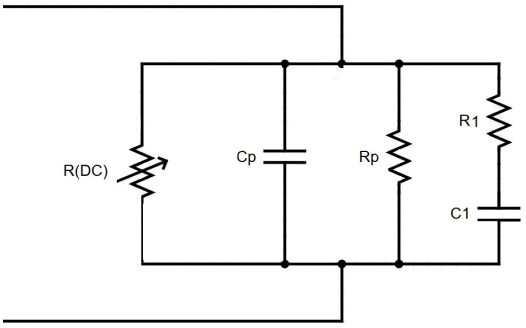

Figure 4.22: The final electrical model.

4.5.2. Model Optimization

Porblem definition: The electrical model shown in Figure 4.22 required optimization using MATLAB to accurately determine the model parameters. Developing a model that captures both frequency and voltage dependencies is inherently complex, as it involves evaluating the model elements' variations across four frequency levels and six voltage levels.

To address this complexity, a script utilising a genetic algorithm was implemented. This algorithm iteratively adjusted three key parameters to minimise the overall deviation between the simulated and measured average power losses, ultimately achieving a good match with minimal error.

The model comprises four branches. While the resistance R_{DC} and capacitance C_p were directly extracted from the test data, the optimization process focused on determining the values of R_1, C_1, and R_p.

Introduciton to genetic algorithm:

The genetic algorithm is an advanced method for finding optimal solutions to various constrained or unconstrained problems, mimicking the principles of biological evolution and natural selection [12]. This algorithm continuously modifies a population of possible solutions. At each step, it randomly selects individuals from the current population and uses them as parents to generate the next generation. Over multiple generations, the population evolves, gradually approaching the best possible solution.

The key differences between a normal optimization algorithm and a genetic algorithm are as follows:

1) A classical optimization algorithm generates a single solution point per iteration, refining a sequence of points to reach an optimal solution. In contrast, a genetic algorithm works with a population of solutions at each iteration, with one solution eventually converging to the best result.

2) In a classical algorithm, the next solution point is chosen sequentially based on a deterministic calculation. However, in a genetic algorithm, the next population is generated based on calculations with elements of randomness.

3) Classical algorithms typically converge quickly to a local optimum. Genetic algorithms, on the other hand, require many function evaluations and may take longer to converge. They may or may not find a local or global minimum, depending on the problem and the algorithm's configuration.

Application:

Figure 4.23 illustrates the results of the genetic algorithm for power losses across **six voltage levels** and **four frequency** levels. The final model was obtained, and the next steps in the process will be discussed in the following section.

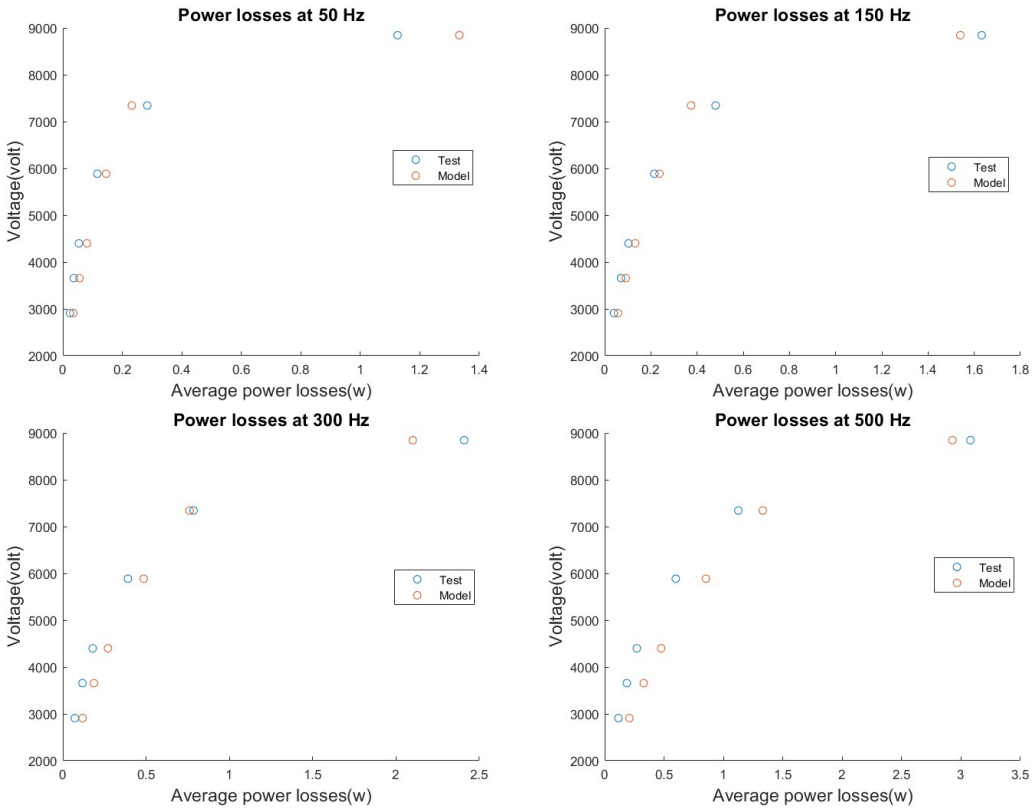

Figure 4.23: Average power losses comparison between testing and modeling across **six voltage levels** and **four frequencies**, based on a four-branch model.

4.5.3. Nonlinear Branch Refinement

After constructing the model, it became clear that the non-linear current of the model was lower than the test results. As a result, the model predicted much lower power loss values at the last voltage level compared to the test data. Figure 4.24 contains four diagrams: A and C show the current and power losses before modifying the current, while B and D display the results after the non-linear current was adjusted. These plots clearly illustrate the improvements achieved by the modification, where the error between the model and the test results has been noticeably reduced. Diagram A highlights the difference in peak resistive currents between the model and the test, showing a mismatch. Similarly, diagram C shows that the model underestimates power losses at the highest voltage level, while overestimating them at all other voltage levels. This pattern is consistent across all frequencies. Therefore, modifying the non-linear current by putting it as another variable into the genetics algorithm, and consequently the power losses, was essential to improve the accuracy and reliability of the model. Modifying the non-linear current was based on a limited increase in its value, specifically at the last 3 voltage levels.

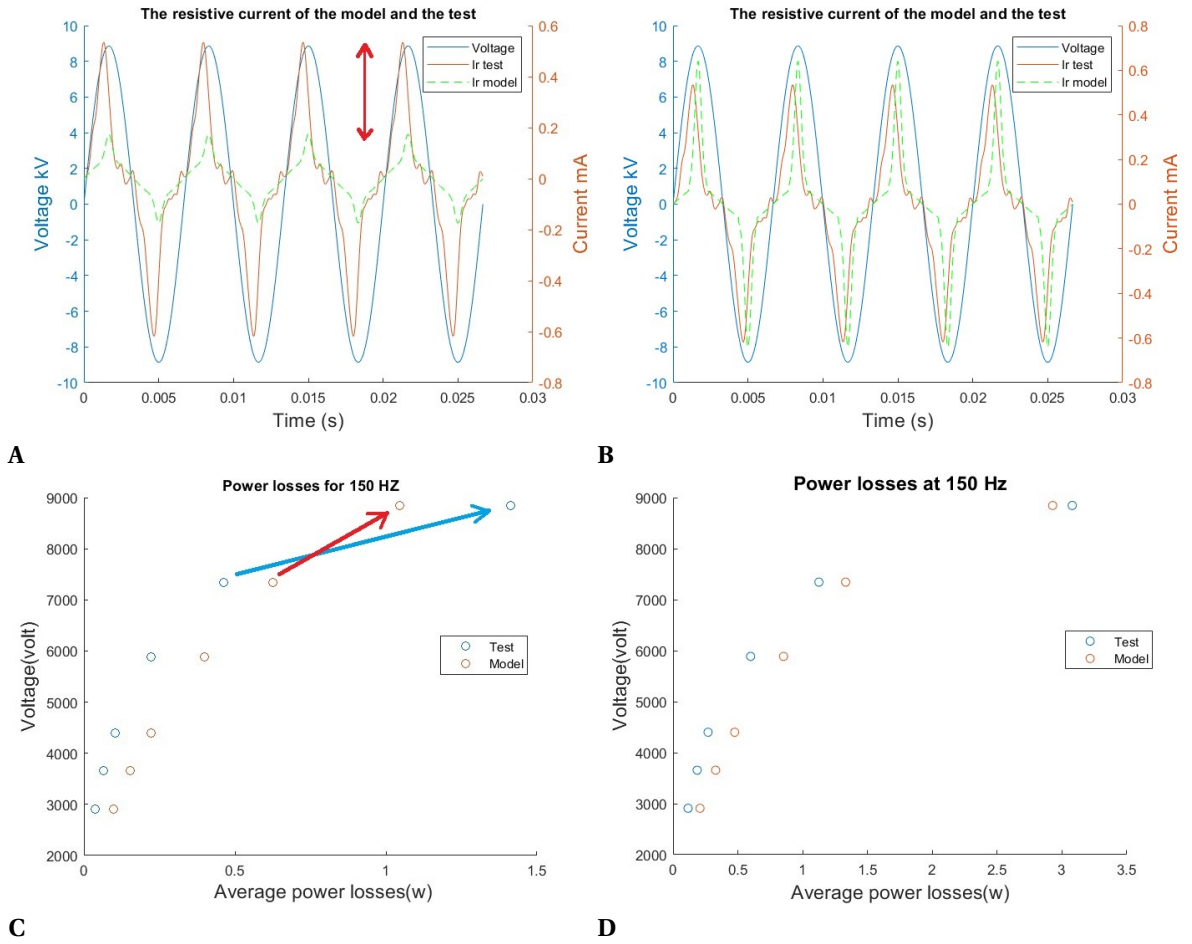

Figure 4.24: The impact of modifying the DC nonlinear current on the average power losses at 8.8 kV and 150 Hz is shown, with the final model, after adjusting the nonlinear branch, displayed on the right side.

4.5.4. Final Model Evaluation

The generated model remains accurate up to a peak voltage of approximately 9 kV, which marks the end of the first region in the voltage–current characteristic curve. This was intentional, as the goal was to characterize the surge arrester blocks specifically within the low current region. Beyond this point, MO blocks exhibit a different physical behavior that is not accounted for in the electrical model. Figure 4.25 illustrates the model results extend slightly beyond this limit, up to 9.2 kV, for illustration purposes only. Model elements are represents in table 4.29, and the nonliear branch is represented in figure 4.26.

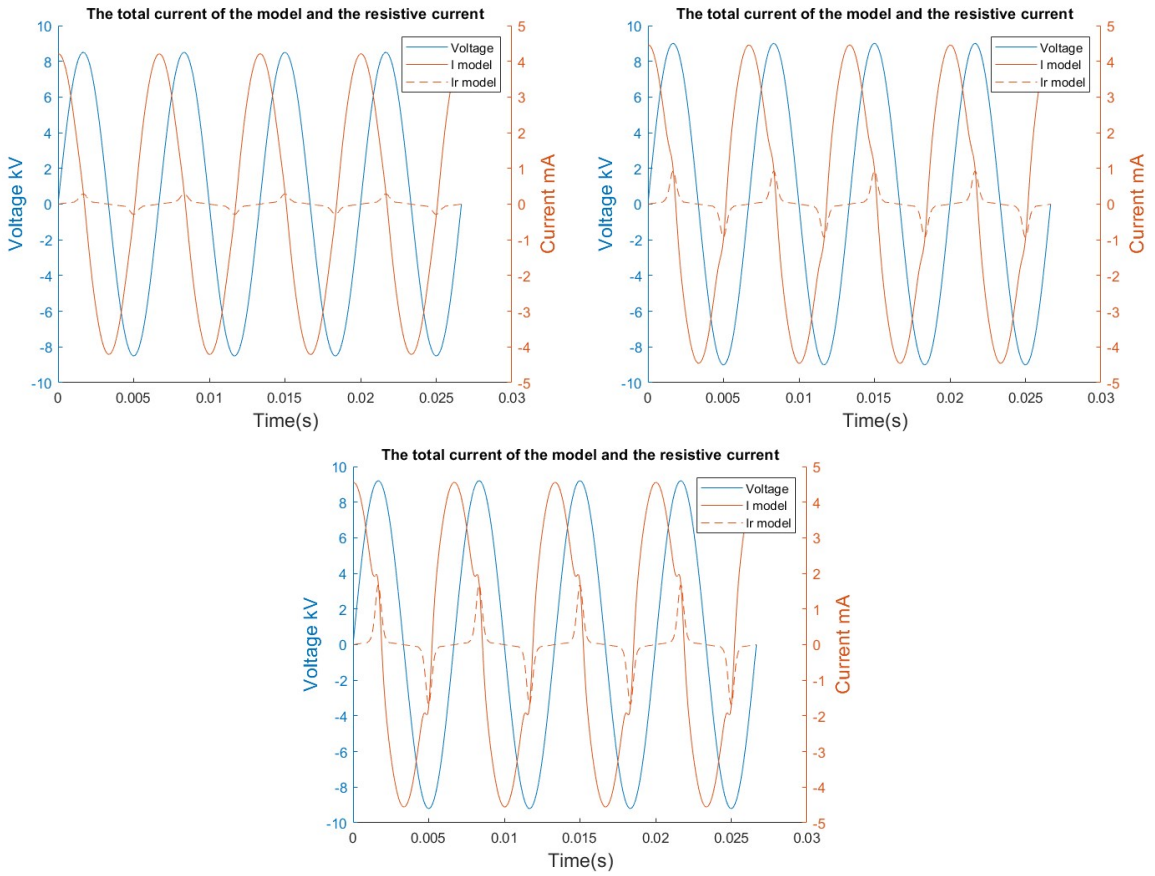

Figure 4.25: Final model wave results for voltage levels of 8.5 kV, 9 kV, and 9.2 kV at 150 HZ

4.5.5. ATP results

Alternative transient program ATP-EMTP is an electromagnetic transient program capable of analyzing a wide range of transients, including lightning, switching phenomena, temporary overvoltages, and sub-synchronous resonance.[5] It features steady-state initialisation, robust multi-conductor analysis support, and powerful scripting capabilities through MODELS. Figure 4.26 consists of two parts: on the left is the final model at ATP, and on the right is the characteristic curve of the non-linear branch (RDC), and the other elements are given in table 4.29. Furthermore, Figure 4.27 shows the total current of the model in the ATP program at three different voltage levels.

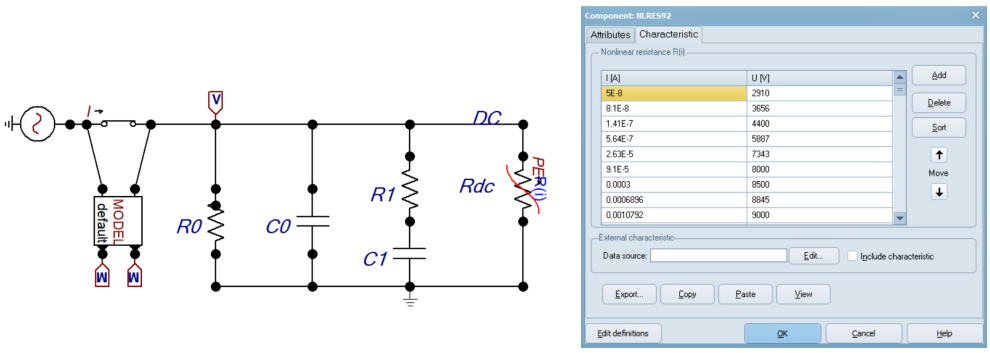

Figure 4.26: The ATP model is shown on the right, and the voltage-current characteristics of the non-linear branch are shown on the left.

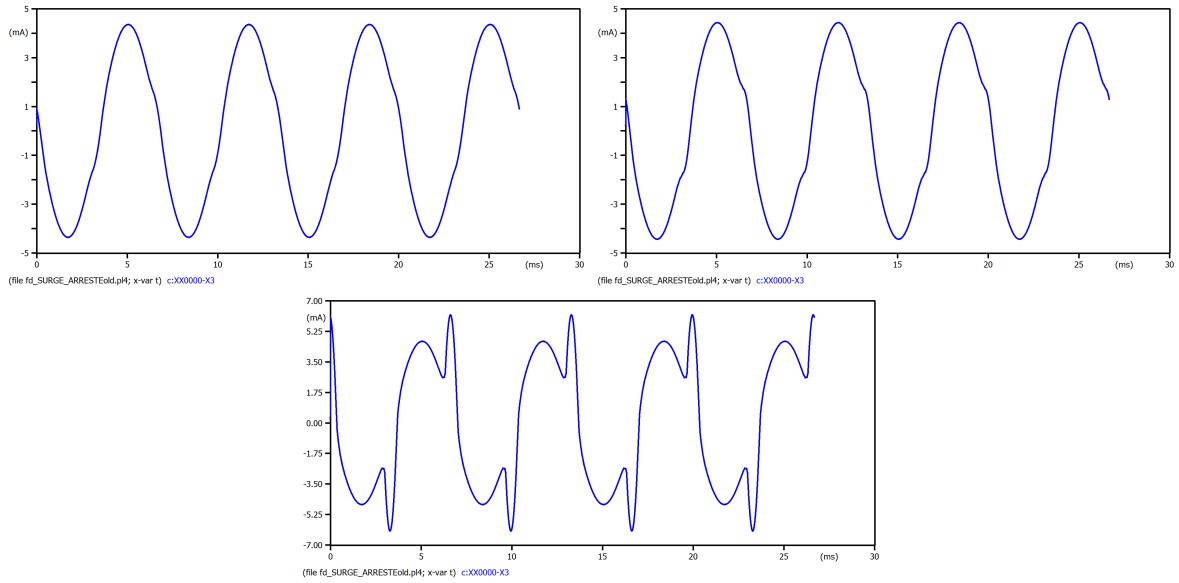

Figure 4.27: Final model current waveforms extracted from ATP for voltages of 8,8 kV, 9 kV, and 9.5 kV.

4.5.6. Rms current comparison

Figure 4.28 illustrates the model's RMS currents, showing that the average deviation from the testing results remains around 10% for voltages below 9 kV. It also confirms that the model is only valid for peak voltages up to 9 kV across the 4 studied frequencies.

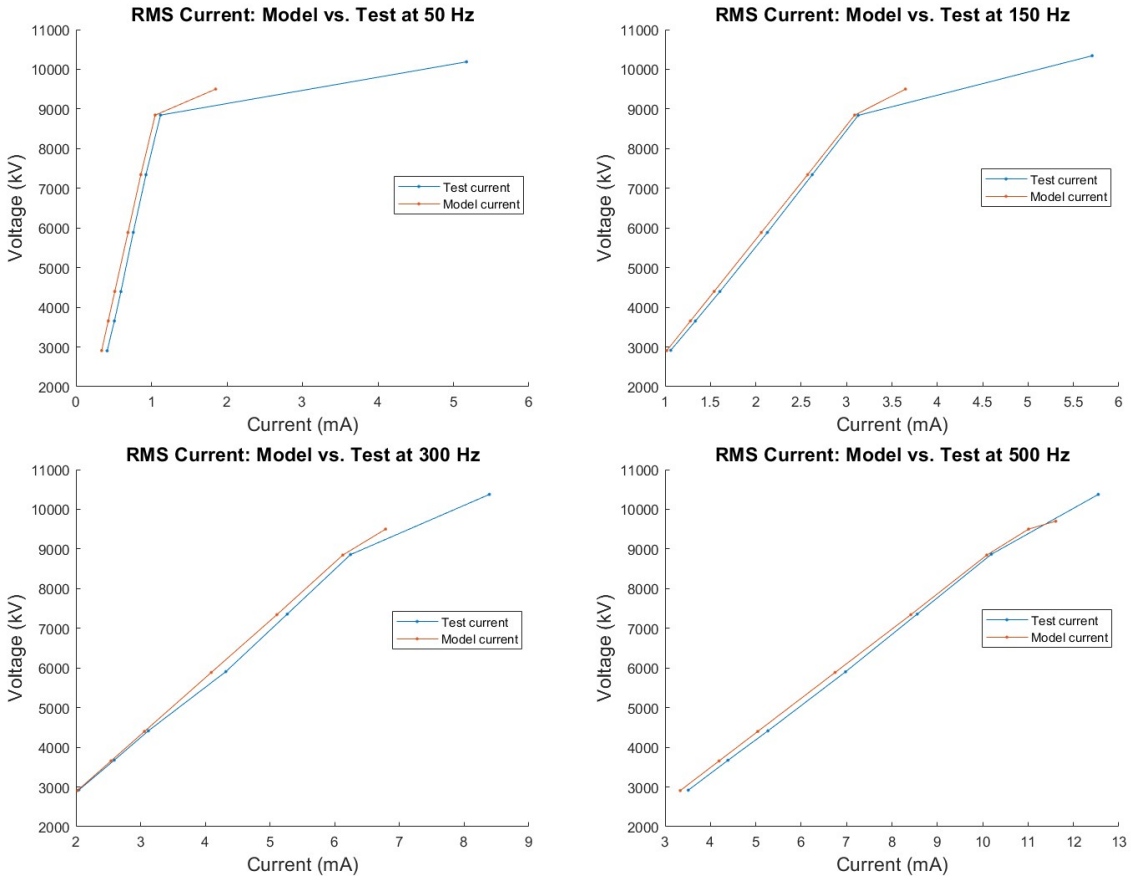

Figure 4.28: Comparison of RMS Current Waveforms from Model and Testing at 50, 150, 300, and 500 Hz

4.6. Final model results for three different tests

4.6.1. Model for test 1

Test 1				
Element	R1	C1	Rp	Cp
Unit	MΩ	nF	MΩ	nF
Value	10	0,0268	131	0,5

Figure 4.29: Elements value of the first generated model.

The component values of the electrical model are shown in Figure 4.29, while the same non-linear DC branch was previously presented in Figure 4.26. The final average power losses are presented in Figure 4.30, where the difference between the model and the measured average power losses shows only a small error.

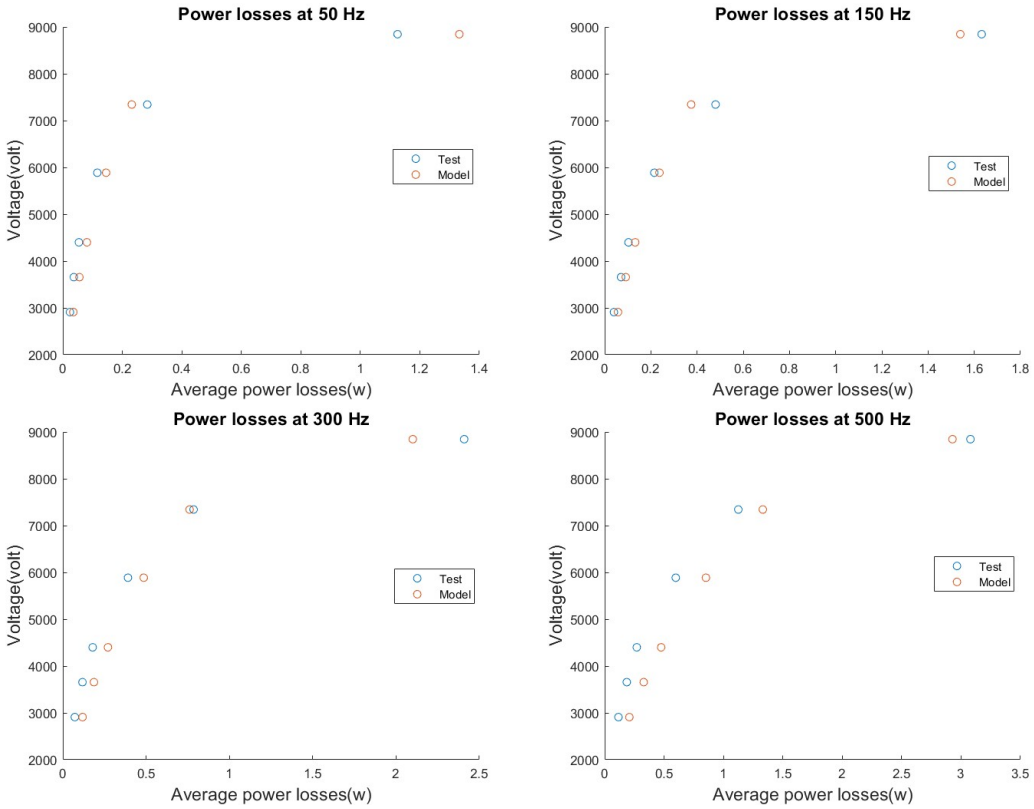

Figure 4.30: Comparison between the generated model and the measured average power losses from Test 1, across six voltage levels and four frequencies.

4.6.2. Model for test 2

Test 2				
Element	R1	C1	Rp	Cp
Unit	MΩ	nF	MΩ	nF
Value	10,56	0,0224	75	0,5

Figure 4.31: Elements value of the second generated model.

The component values of the electrical model are shown in Figure 4.31, while the same non-linear DC branch was previously presented in Figure 4.26. The final average power losses are presented in Figure 4.32, where the difference between the model and the measured average power losses is presented.

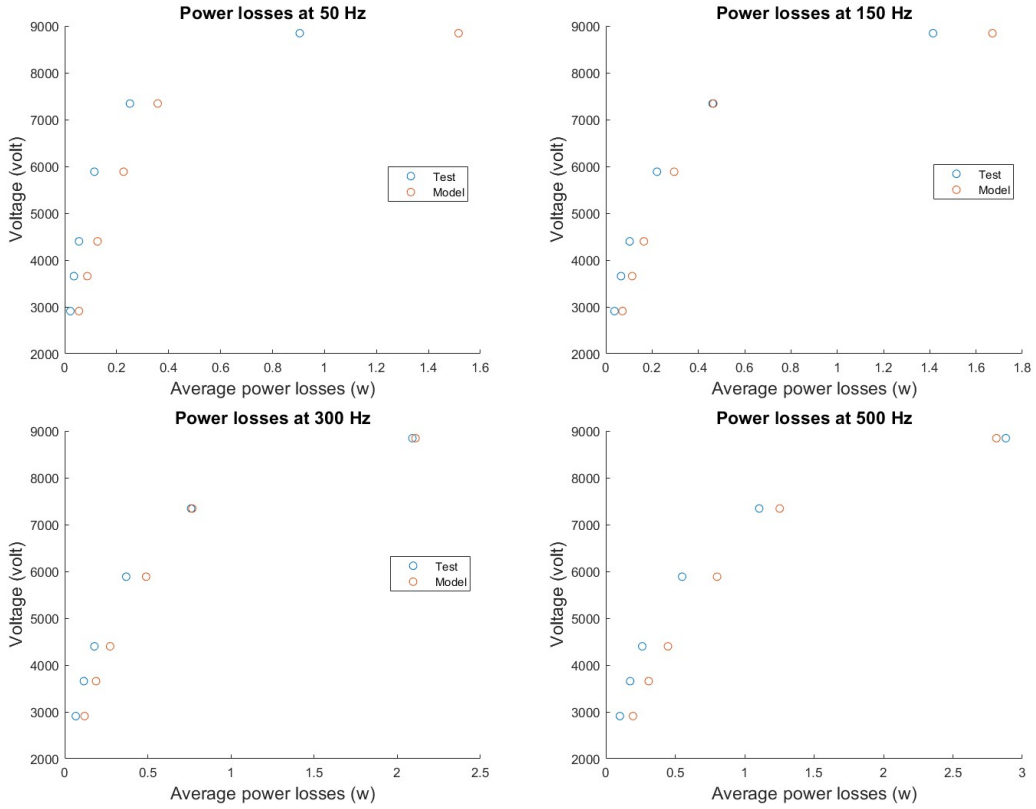

Figure 4.32: Comparison between the generated model and the measured average power losses from Test 2, across six voltage levels and four frequencies.

4.6.3. Model for test 3

Test 3				
Element	R1	C1	Rp	Cp
Unit	MΩ	nF	MΩ	nF
Value	10	0,0268	401	0,5

Figure 4.33: Elements value of the third generated model.

The component values of the electrical model are shown in Figure 4.33, with the same non-linear DC branches the previous model. The final average power losses are presented in Figure 4.34, where the difference between the model and the measured average power losses is presented.

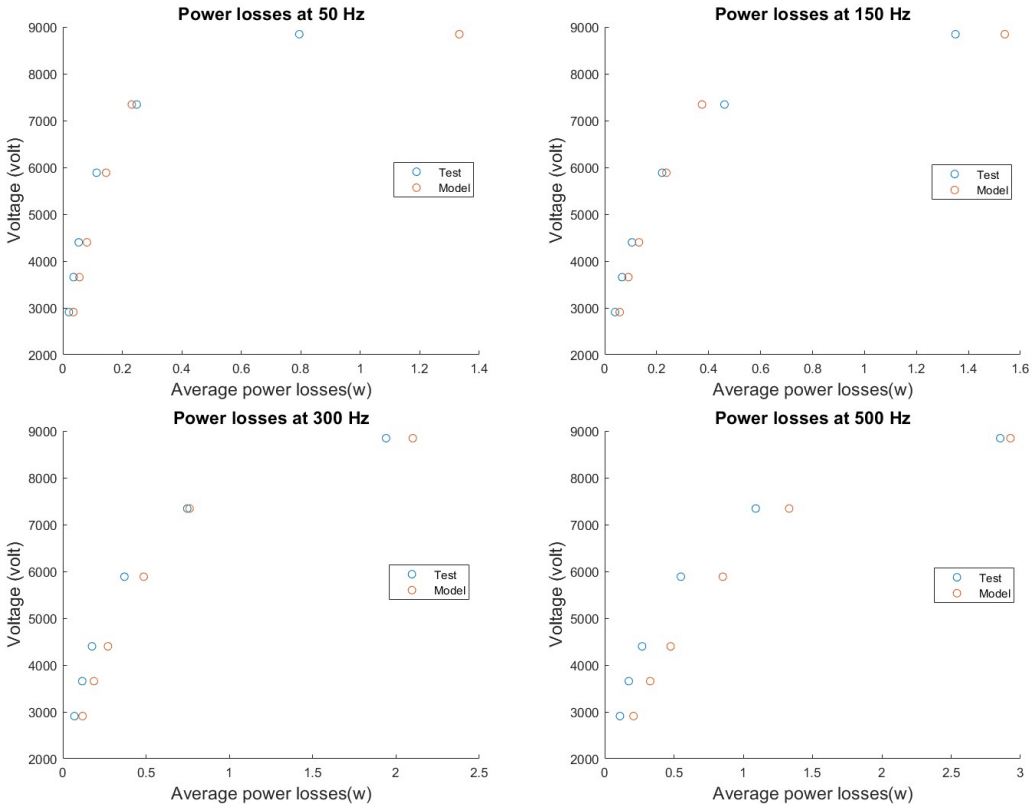

Figure 4.34: Comparison between the generated model and the measured average power losses from Test 3, across six voltage levels and four frequencies.

To better reflect on higher power losses of higher voltages, a weighted average deviation was calculated for the models across all frequencies and voltage levels. This approach gives more importance to operating points with greater power losses, ensuring that the small losses at low voltage levels (e.g., below 4 kV) do not disproportionately affect the evaluation. The resulting weighted errors for model one were 20% at 50 Hz, 11% at 150 Hz, 18% at 300 Hz, and 24% at 500 Hz.

The three generated models provide a reasonably valid representation of the surge arrester block. Among them, **Model 1** demonstrates consistent accuracy across all frequency levels, with an average error ranging between 10% and 25%. In contrast, the other models show higher error at the lowest frequency (at 50 Hz), although their performance at higher frequencies remains similar to that of Model 1. This emphasises the need for further refinement to improve low-frequency accuracy.

These differences in accuracy between models stem from the optimisation algorithm, which minimises the total average error across all voltage and frequency levels. As a result, one model may perform better at a specific frequency, while another may offer improved accuracy under different conditions.

4.7. Analysis and discussion

1) Voltage range:
The extracted model is valid only for voltages up to a 9 kV peak, corresponding to the first region of the voltage-current characteristic curve. This focus was intentional, as the project aimed to assess whether the surge arrester might experience heavy-duty conditions within this region because most thermal runaway and long-term degradation processes originate there.

2) DC Measurements:
The DC measurements require further investigation; the differences observed in the DC non-linear branch current suggest that the surge arrester's response might differ depending on whether the applied voltage is DC or AC — a topic that could be interesting for future research.

3) Frequency range:
The model has been validated across a frequency range of 50 to 500 Hz, covering the spectrum typically associated with temporary overvoltages (TOVs), as defined by IEC 60071-1. However, the relatively higher average error observed at 50 Hz suggests a limitation in the model's accuracy at lower frequencies. To improve performance, the inclusion of an additional RC branch in the model may enhance the representation of frequency-dependent behavior across a wider spectrum.

4) Measurement method of resistive current:
Peak current measurements are highly susceptible to noise, making them unreliable for assessing resistive components. Instead, the use of RMS current values has proven to be a more stable and accurate method, especially given the highly nonlinear current peaks observed during testing. RMS-based analysis ensures better repeatability and reduces measurement error.

5) Resistive Current Analysis:
The final model showed good agreement with the RMS value of the total current, although a small phase shift at the time domain was observed. This shift might be due to hysteretic behaviour within the non-linear branch. In future work, introducing a parallel inductor tuned to the block's capacitive current might help achieve resonance, allowing for a more accurate separation and measurement of the resistive current via the grounding path.

5

Conclusion

This thesis successfully developed and validated a frequency-dependent model for a single surge arrester block, focusing on the low-current region relevant for harmonic overvoltage conditions. The experimental testing confirmed that frequency significantly influences the current behaviour of the arrester. Thus, the resistive current was found to be frequency dependent, particularly through capacitive effects at higher frequencies.

The four-branch model provided accurate results across a wide operating range, demonstrating its suitability for time-domain simulations.

The study also highlighted the importance of modelling the low-current region, where small changes in leakage current might lead to thermal stress and long-term degradation. As power systems integrate more offshore wind capacity, understanding and modelling the frequency-dependent response of surge arresters becomes increasingly important.

The model lays the groundwork for future simulations under a network model in ATP-EMTP, to evaluate the impact of harmonic resonances on the surge arrester performance. Further work is recommended to improve accuracy at lower frequencies and to extend the model under more complex operating conditions.

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