

Thesis:

Ultra low power switched-capacitor wavelet-based ADC for ECG analyzer

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Abstract

A huge number (40%) of all human deaths are caused by cardiovascular diseases. In the past decades, a lot of research was done about the cause and the prevention of cardiovascular diseases. An implantable device, such as a pacemaker, is a well known method to prevent death by cardiac problems. This thesis explores the possibility of improving detection and reducing power consumption of ECG detectors.

To find a suitable structure of our design, basic information about cardio signal and the heart is needed. Analog sense amplifier method is the method in this thesis to detect the QRS complex (obtains from depolarization of the ventricular in the heart) and the T-wave (creates by ventricle repolarisation) of IECG (intracardiac electrogram) signal. This method consists of analog signal processing block and an A/D converter. A wavelet filter (WF) is used to design the first part. In the introduction, wavelet transform analysis, mother wavelet, the desired approximation and suitable decomposition are discussed. These are parts of the wavelet filter.

The wavelet filter is designed in discrete time domain due to its gain accuracy and low power consumption. Moreover, the switched-capacitors filters have an accurate frequency response as well as good linearity and dynamic range. The thesis discussed the design of discrete-time switched-capacitor (SC) fully differential folded cascode amplifier.

The second part of the analog sense amplifier is the A/D converter, which consists of a *sinh* transconductor and a peak detector circuit. As the WF implemented in discrete-time, the detector block should do this as well. That is why the sample and hold (SH) block is used at its input of the detector block. The binary output is expected to be seen from the QRS complex and the T-wave of the heart signal.

The whole system with an ECG signal input is built in five scales, which is needed to zoom in the different frequencies of the ECG signal. Every scale is implemented for different resolutions by using different clock frequency signals. Another way to implement the different scales is to change the ratio of the capacitors. This method is not used in this thesis, because the minimum values of the capacitors are already chosen. The system is able to detect the ECG signal with the ultra low power and small area design.

1. Introduction

In the biomedical world, one of the most important problems that the cardiologists want to solve is a better detection result of pathologies, indicated by intracardiac electrogram (IECG) morphology from a device, such as a pacemaker. In this kind of implantable medical devices, the power consumption is an important aspect due to the limited power density and the area of the portable batteries. This denotes that our design has to be optimized for very low power consumption and small area.

The electro-cardio signal (ECG) is the electrical activity of the heart, which can be monitored with a pacemaker. A heart signal consists of PQ (atria depolarisation), QRS (ventricular depolarization) and ST waves (ventricle depolarization). The two most important parts of the heart signal or ECG signal are the QRS complex and the T-wave, which will be analyzed and detected in this thesis. The QRS part, which is obtained from depolarization of the ventricular in the heart, is the biggest peak of the heart signal with duration between 0.06 and 0.1 second. The T-wave is created by ventricle depolarization. The aim of this thesis is to design a suitable system with ultra low power and small area to detect the QRS complex and T-wave to get the binary outputs for a micro-controller.

Different methods are already used to design a system to detect the ECG signal, such as digital sense amplifier and analog sense amplifier in continuous time domain. This thesis is based on the analog sense amplifier in a discrete time domain. Analog signal processing and A/D converter is needed to construct the analog sense amplifier. The wavelets filter bank technique and a sample & hold detector circuit are used to design the analog signal processing and A/D converter. The wavelet filter is built using switched-capacitor (SC) fully differential amplifier technique. The detector circuit is built using a *sinh* transconductor and a peak detector circuit. The wavelet filter technique is used by Sandro A. P. Haddad [1] in continuous time domain. Michiel Grashuis [5] also used this technique in discrete time domain for a single-scale, which is briefly presented at the end of this chapter.

Chapter one discusses the basic information about the heart, its functionality and how the system will be constructed. In chapter two, a single-scale wavelet filter is presented by using the SC fully differential folded cascode circuit. In the third chapter a *sinh* transconductor circuit and a peak detector circuit are discussed and followed by a chapter four about the whole system by using the five scales with an ECG signal as an input. At the end of our design, we expect to be able to detect the QRS complex and the T-wave of the heart signal with an ultra low-power analog integrated circuit technique in the discrete time domain.

This chapter consists of the general meaning of biomedical signals (1.1), the pumping section of the body (1.2) and its electrical activity over time (ECG signal) (1.3). The need of the wavelet transform analysis and its mother wavelet will be discussed in section 1.4 and 1.5. The approximation and the state-space description are presented in the other sections (1.6 and 1.7) to show a suitable way to construct the set of wavelet filters. This will perform the wavelet transform on an ECG input signal. Finally, the Schwarz decomposition method (1.8) is chosen to decrease the number of components.

1.1. Biomedical signals

Biomedical signals are mainly used for extracting information of a biological system under investigation [18]. Most often in biomedical application, the accuracy of the signal is not enough because of different problems, such as loss in equipments, wires or even because of patients. Thus, acquiring biomedical signals causes them to be noisy and carry unwanted information. This causes the

relevant information not to be readily extracted from the raw signal. Therefore, it is required to design better devices to extract more details about biomedical signals to get the relevant information that exists in it. For such reasons, advanced signal processing is usually required.

Another important aspect of biomedical signals is that the information of interest is often a combination of characteristics which are localized in both the time and the frequency domain. This requires the use of the wavelet transform analysis to extract information from a biomedical signal in both domains.

The cardiovascular diseases cause huge number of human deaths. The investigation in this field to decrease the overall cardiac mortality makes the cardiac signal one of the most important biomedical signals.

1.2. Pumping section (heart)

The heart is a muscular organ that is responsible for pumping blood through the body by rhythmic contractions. It is enclosed in a double-walled sac called the pericardium and it has four chambers. Two superior atria, which are the receiving chambers and two inferior ventricles, which are the discharging chambers, and they are twice the size of the atria. The atria are on top and the ventricles are below them. In this way, the heart is divided into right atrium (or auricle) (RA) and ventricle (RV) side and left atrium (LA) and ventricle (LV) side. The left ventricle is the largest and most important cardiac chamber [1]. The right and left sides of the heart are working together to pump the blood. The right side, pumps the blood to the lungs through the pulmonary artery. The left side pumps blood to the body through the aorta. In the figure below, the different parts of the human heart can be seen.

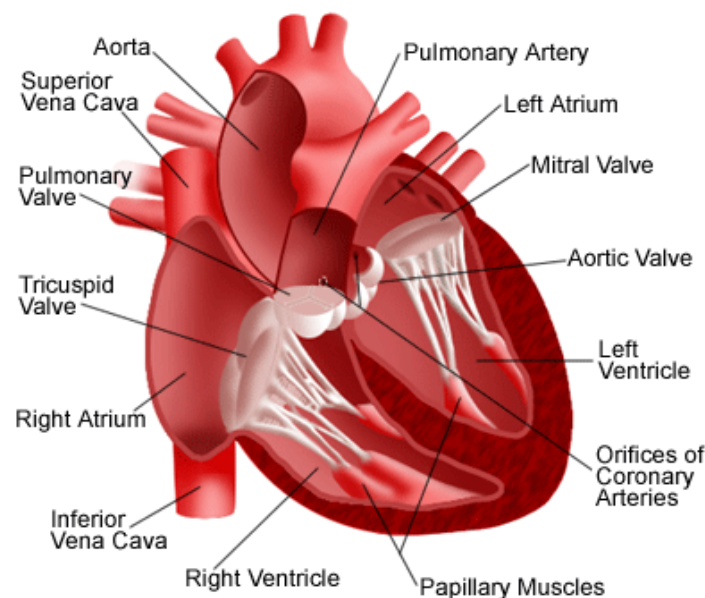


Figure 1.1: Interior view of the heart [3]

The electrical function of the heart is shortly presented here. In the heart's natural pacemaker, the SA node¹ sends out electrical impulse regularly from the top atrium and activates it to pump the blood into the bottom ventricle. Then the electrical impulse is connected to the ventricles through the AV node². The impulse propagates into the ventricles to contract the muscle to expel the blood. By monitoring this electrical activity, the ECG signal will be obtained which is discussed in the next section.

1.3. ECG signal

An electrocardiogram (ECG) is a representation of the electrical activity of the heart over time, which is recorded by an electrocardiograph. The ECG signal is perhaps the most commonly known, recognized and used biomedical signal [1]. The rhythm of the heart can be estimated by counting the waves, which are readily identifiable in terms of beats per minute (bpm). Normal (resting) heart rate is about 70 bpm [1]. The ECG signal has very low amplitude in millivolts and relatively low frequency content. The bandwidth of the signal is typically from 0.05 Hz and extends to about 150 Hz. An ECG signal is shown in Figure 1.2. This figure is an example of nominal ECG signal which consists of a P-wave, a QRS complex and a T-wave.

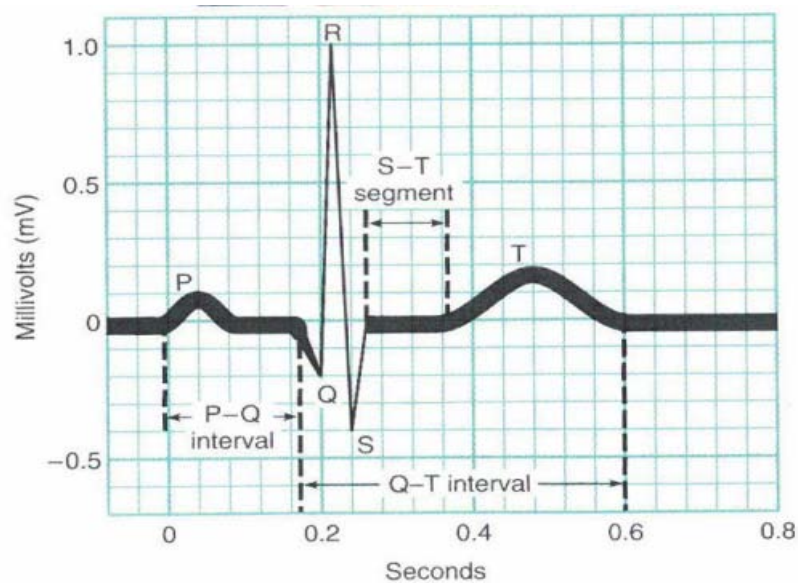


Figure 1.2: ECG signal

¹ The sinoatrial node (also commonly spelled sinuatrial node, abbreviated SA node or SAN, also called the sinus node) is the impulse-generating (pacemaker) tissue located in the right atrium of the heart, and thus the generator of sinus rhythm.

² The atrioventricular node (abbreviated AV node) is a part of electrical control system of the heart that co-ordinates heart rate. The AV node is an area of specialized tissue between the atria and the ventricles of the heart, specifically in the posteroinferior region of the interatrial septum near the opening of the coronary sinus.

The P-wave and the T-wave are created by depolarization of atria and ventricle repolarisation, respectively. Depolarization of the left and the right ventricles cause the QRS complex. The QRS complex is the dominant feature of the heart signal, which denotes activity of the heart pumping the blood around the body [5]. The duration of the QRS complex is between 0.06 to 0.1 seconds. This short duration indicates that ventricular depolarization occurs rapidly with the highest peak in a heart signal. Many coronary heart diseases have this kind of influence on the electric activity modifying the normal shape patterns. Ventricular pre-excitation³, ventricular hypertrophy⁴ and ventricular tachycardia⁵ are examples of these diseases. The QRS complex and the T-wave of the whole heart signal are the main parts on which we will focus in this thesis.

The ECG signal is a non-stationary biomedical signal of which the frequency content changes over time. This means that the extracted information from a heart signal, both in time and frequency domain analysis are needed. For such a reason, a good transform analysis must be chosen. In the next part, the Fourier transform and the wavelet transform analysis are discussed.

1.4. Wavelet transform analysis

The Fourier transform (FT) is a powerful tool for analyzing a signal in the frequency domain. A Fourier analysis performed on a time domain signal, gives the spectrum of that signal in the frequency domain. This is a very useful tool in circuit analysis, however one disadvantage of the Fourier transform during the transformation to the frequency domain, is that all the time domain information will be lost. This means that although it is possible to determine all the frequency components present in a signal, it is not possible to know when they have occurred. To overcome this problem, the wavelet analysis or wavelet transform is the most recent solution which is able to represent a signal in the time and frequency domain. The idea behind this method is to decompose the signal into different scales and analyze these scales separately. This allows the wavelet transform to preserve the time domain information of the input signal [5].

As an example, on the top row of the figures below, two different time domain signals can be seen which have different frequencies. On the left side we have the signal with two frequency components in different times and in the right side we have a signal with two different frequencies in the whole time. First the Fourier transform is done on these signals and then the wavelet transforms to show the difference between these two methods.

³ Pre-excitation syndrome is a condition where the ventricles of the heart become depolarized too early, which leads to their partial premature contraction.

⁴ Ventricular hypertrophy is the enlargement of ventricles (lower chambers) in the heart

⁵ Ventricular tachycardia (V-tach or VT) is a tachycardia, or fast heart rhythm, that originates in one of the ventricles of the heart.

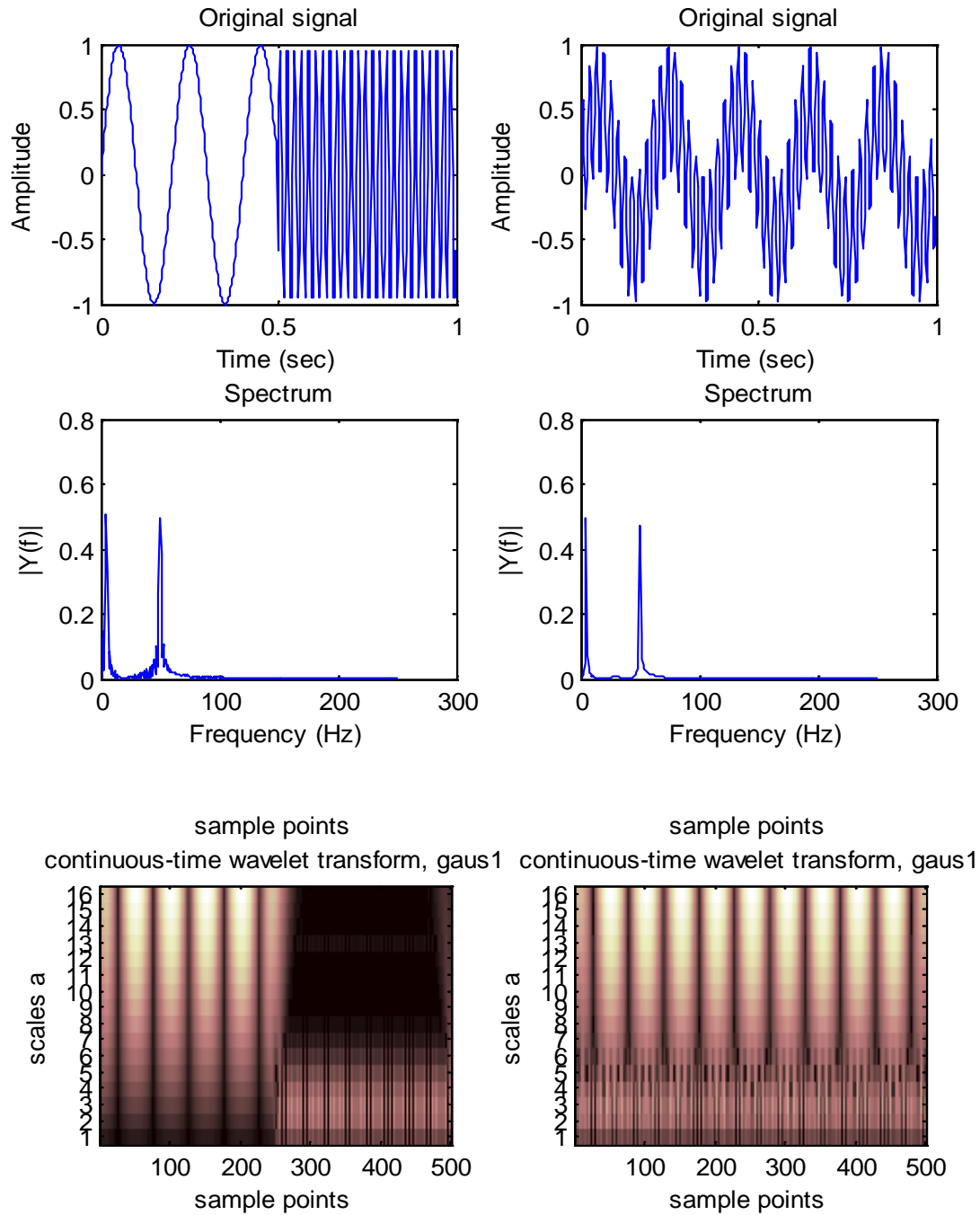


Figure 1.3: Two time domain signals and their corresponding Fourier and wavelet analysis

The second row of the figure above is the corresponding Fourier spectra of the two time domain signals. The two time domain signals are different but their Fourier spectra are almost the same. This means that the Fourier analysis only correlates the input signal with sine waves and gives the frequency components that are present in the time domain signal. Wavelet analysis however does preserve the time domain information [1]. Wavelet analysis is different from Fourier transform and it correlates the input signal with a wavelet base instead of sine waves. That is why the wavelet analysis preserves the time domain information of the signal.

On the bottom row, the corresponding wavelet analysis for different scales can be seen. In this case first derivative of Gaussian (gaus1) is used as a mother wavelet and plotted versus time (x-axis). By looking at that figure, in the wavelet transform scale, the low scale performs the higher frequency components in the signal and vice versa for a high scale. The fluctuation in the input signal is expressed as alternating dark and light colors. For a low and high scale, the high frequency components and the low frequency components of the input signal are detected, respectively. This makes the wavelet transform suitable to preserve the time domain information. This means that for a wavelet ADC, a filter bank is needed, where each filter corresponds to a wavelet scale.

1.5. Choosing the mother wavelet

The wavelet transform of a continuous time signal is written as:

$$w_f(\tau, a) = \frac{1}{\sqrt{a}} \cdot \int_{-\infty}^{\infty} f(t) \cdot \varphi^*\left(\frac{t-\tau}{a}\right) \cdot dt \quad 1.1$$

Where $f(t)$ is the input signal, $\varphi^*(t)$ is the complex conjugate of the mother wavelet or the wavelet base $\varphi(t)$, a is the scale factor of the wavelet and τ is the position parameter of the wavelet. The factor $1/\sqrt{a}$ is used for energy normalization.

The wavelet base is a small oscillatory wave or wavelet. Wavelet analysis is performed using the wavelet base, which decomposes a signal into components appearing at different scales. Hence, the WT is based on the convolution of the signal and a dilated impulse response of a filter, mapping the signal onto time and frequency domain. In addition, the main idea of the WT is to look at a signal at different windows and analyze it with different resolutions. One of the important conditions of the wavelet base is given by:

$$\int_{-\infty}^{+\infty} \varphi(t) \cdot dt = 0 \quad 1.2$$

This equation denotes that the wavelet base is oscillatory and has zero mean value. Another condition that this function needs to satisfy is the admissibility condition so that the original signal can be reconstructed by the inverse wavelet transform.

$$\int_{-\infty}^{+\infty} \frac{|\Psi(\omega)|^2}{|\omega|} \cdot d\omega = C_\Psi < \infty \quad 1.3$$

Equation 1.3 is the admissible condition which implies that the Fourier transform of the wavelet must have a finite energy. From equation 1.1, it can be seen that performing the wavelet transform is actually performing a convolution of the input signal with scaled versions of the wavelet base. So by increasing the scaling parameter, the impulse response of the wavelet filter becomes longer. It means each scale corresponds to a certain band in the frequency domain, and therefore each wavelet filter computes the wavelet transform for one scale.

In order to choose a suitable wavelet base for our design between different wavelet bases such as Gause1, Morlet and Daubechies, it is better to look at one of them that is similar to the signal. For this

season the first derivative of a Gaussian (gaus1) is chosen as a mother wavelet. The first derivative of a Gaussian wavelet can be seen in the figure bellow.

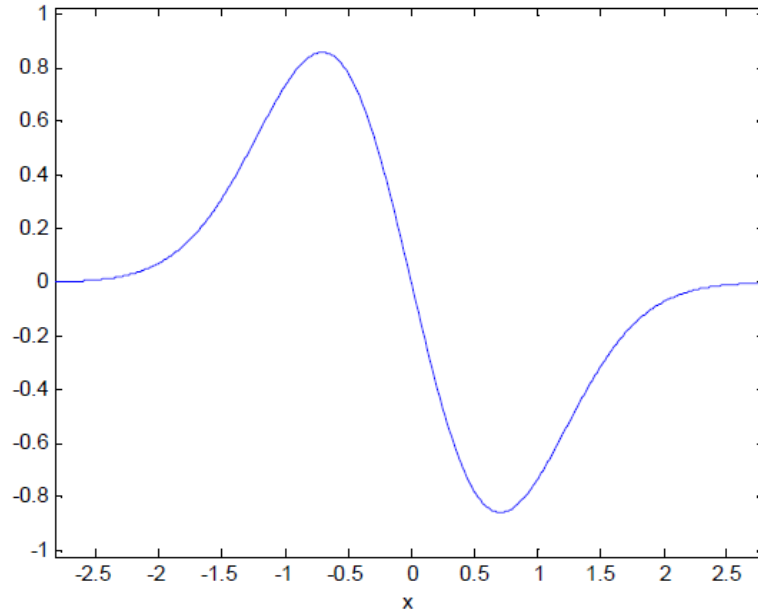


Figure 1.4: The first derivative of a Gaussian ($-2 \times \exp(-x^2)$)

1.6. Choosing the approximation

Approximation methods are necessarily to obtain the required transfer function or a wavelet impulse response. To obtain an approximation transfer function of a certain wavelet filter, there are several mathematical techniques. Three different methods of them are frequently used to find the best approximations, which are described in this section. They are the L_2 , Pade and SVD wavelet based approximations [1].

1.6.1. Pade approximation

One of the suitable methods to obtain the required transfer function is Pade approximation in the Laplace domain. It takes the time domain function as input and gives a transfer function as output.

It concentrates around one point of the function that needs to be approximated [1]. It gives a transfer function as output and the time domain function as input. Any wavelet bases in the time domain function can be used as an input, such as Morlet and Gaus1. This approximation is not used in the thesis because of its wiggle at the start point of the signal and overshoots in the peaks.

1.6.2. L_2 approximation

Another way is the L_2 approximation, which will be described briefly. The basic approach of approximation techniques are usually minimizing the certain assumed criteria of measuring the error and then minimizing that error. In L_2 approximation techniques, minimizing the least-mean-square-error is used and it works both in the time and the frequency domain. However one drawback of this method is that there is a risk that the numerical optimization ends in a local, non-global optimum [1]. It extremely depends on the starting point. By choosing a bad starting point, the iterative process of

approximation will be obtained to end up in a local optimum instead of global optimum. That was the reason to reject the use of this method in this design.

1.6.3. SVD approximation

Another approximation method is the Singular Value Decomposition (SVD), which is a new method compared to the others. This approximation is done in discrete time domain rather than continuous time domain and it has a linear relation between input and output which is defined by the transfer matrix T . SVD method uses the samples of time domain for its input and gives a state-space description as an output. SVD approximation gives much better result than the other approximation. Besides, this method yields a state-space description with the least component spread [5]. That is the reason to use this approximation in this thesis. As an example, the next figure is plotted by using a fifth order SVD approximation and the original gaus1.

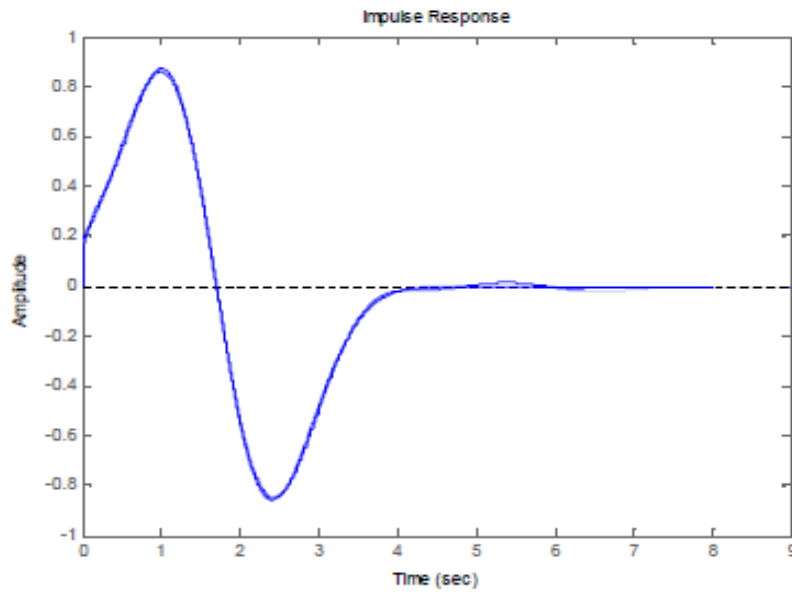


Figure 1.5: The original gaus1 overlapped with a fifth-order SVD approximation

1.7. State space description

As mentioned before, state-space descriptions allow the designer to find an implementation that fits the best to the requirement, such as maximum dynamic range, sensitivity and sparsity. State-space description can be controlled, and it describes the behavior of the internal states of the system. With different state-space descriptions, the designer has opportunities to find the best requirement such as. A state-space description can be used in the continuous time domain and in the discrete time domain. The equations and block diagram of the state-space in discrete time is implemented, because the design in the thesis is based on discrete time. In the discrete time domain, the common form of the state-space description is given by:

$$x(n+1) = A.x(n) + B.u(n) \quad 1.4$$

$$y(n) = C.x(n) + D.u(n) \quad 1.5$$

Here, $u(n)$, $y(n)$ and $x(n)$ represent the input, output and state of the system, respectively. The z-transform of equations 1.4 and 1.5 is given by following equations, and the block diagram is illustrated in Figure 1.6.

$$z.x(z) = A.x(z) + B.u(z) \quad 1.6$$

$$y(z) = C.x(z) + D.u(z) \quad 1.7$$

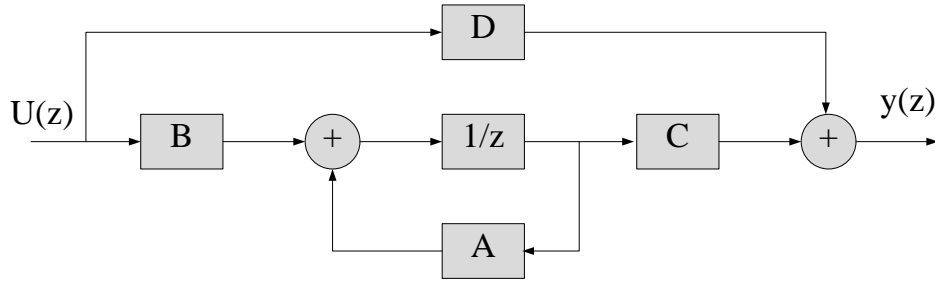


Figure 1.6: Block diagram of a discrete time state-space description

1.7.1. Dynamic range

Dynamic range of a system is determined by the maximum allowable process signal magnitude and the internally generated noise [1]. The dynamic range is defined as the ratio between the maximum signal swing (the distortion-less signal) and the minimum signal swing (the noise) that a system can handle. From the thesis of Guillen [7] and Rocha [8], it is shown that the dynamic range of a system can be expressed as:

$$DR = \frac{\left(\frac{M}{\delta(p)} \right)^2 \cdot TR(GQ)}{\max_i G_{ii}} \cdot \frac{1}{\gamma \sum_i \frac{\alpha_i}{C_i} \cdot W_{ii}} \quad 1.8$$

where,

- M is the maximum output amplitude of the integrators.
- $\delta(p)$ is a nonlinear monotonically increasing function of the fraction of time p that integrator i is allowed to clip.
- TR is the trace of a matrix, the sum of the elements on its main diagonal.
- Q is the state weighing matrix: $Q = C^T C$.
- $\gamma = \xi 2kT$ is the integrator noise figure with T is temperature in Kelvin, k is the Boltzmann's constant and $\xi \geq 1$ is a constant.
- $\alpha_i = \sum |a_{ii}|$ is the absolute sum of the elements of the i^{th} row of A .
- C_i is the i^{th} integrator capacitance.
- G_{ii} are the main diagonal element of G .
- W_{ii} are the main diagonal element of W .

In order to maximize the dynamic range of the system, the maximum distortion-less signal that the system can handle needs to be maximized and the noise needs to be minimized. The value of the dynamic range which is obtained from the equation above is:

$$DR_{before} = 140.9dB \quad 1.9$$

With the optimization of the state-space equation by using the space transform or similarity transform, the maximum dynamic range will be obtained [5] and is equal to:

$$DR_{after} = 162.7dB \quad 1.10$$

As it can be seen in these results, the improvement is about 20dB here. These calculations have been done [5] on a SVD approximation with 5th order of guas1. The disadvantage of this method is its fully dense matrices which lead to the usage of more components. To solve this problem and minimize the number of components in the system, they can be decomposed into a Schwartz form [9].

1.7.2. Schwartz

The state-space description gives A, B, C and D matrices which are fully dense matrices. This means that to implement the circuit, the number of components is a lot. To decrease this number, the Schwartz decomposition can be used. Schwarz is one of the matrix decomposition methods and by using this method, A, B, C and D matrices give the Schwarz form, which are presented below.

$$A_T = \begin{bmatrix} -a_{11} & -a_{21} & 0 & 0 & 0 \\ a_{21} & 0 & -a_{32} & 0 & 0 \\ 0 & a_{32} & 0 & -a_{43} & 0 \\ 0 & 0 & a_{43} & 0 & -a_{45} \\ 0 & 0 & 0 & a_{54} & 0 \end{bmatrix} \quad 1.11$$

$$B_T = [b_1 \quad 0 \quad 0 \quad 0 \quad 0] \quad 1.12$$

$$C_T = [c_1 \quad c_2 \quad c_3 \quad c_4 \quad c_5] \quad 1.13$$

$$D_T = [0] \quad 1.14$$

It is clear that the above matrices have a lot of zero entries as compared to the state-space description matrices. The dynamic range is calculated again and is compared to the optimum one to be sure that Schwarz decomposition does not cost a lot of dynamic range. With the same specifications of SVD approximation with 5 orders, decomposition is done into a Schwarz form and the value of the dynamic range becomes as follows [5].

$$DR_{schwarz} = 161.9dB \quad 1.15$$

This result is a little bit different from the optimum dynamic range, and this decomposition only cost about 0.8dB.

1.8. Overview of whole system

The system level can now be implemented by knowing the methods and structure of the design. The wavelet transform will be used to make a wavelet filter bank to obtain different resolutions of a heart signal. The detector part is used to make a binary output of every wavelet filter for a microcontroller. This gives us the overview about the whole system and its structure. The block diagram of a whole system can be seen in Figure 1.7.

In the next chapter, the focus of our design will be on the wavelet filter part. Because every wavelet filter design is the same, only one will be discussed. Different scales are implemented by changing the clock frequency. This will be explained in chapter two.

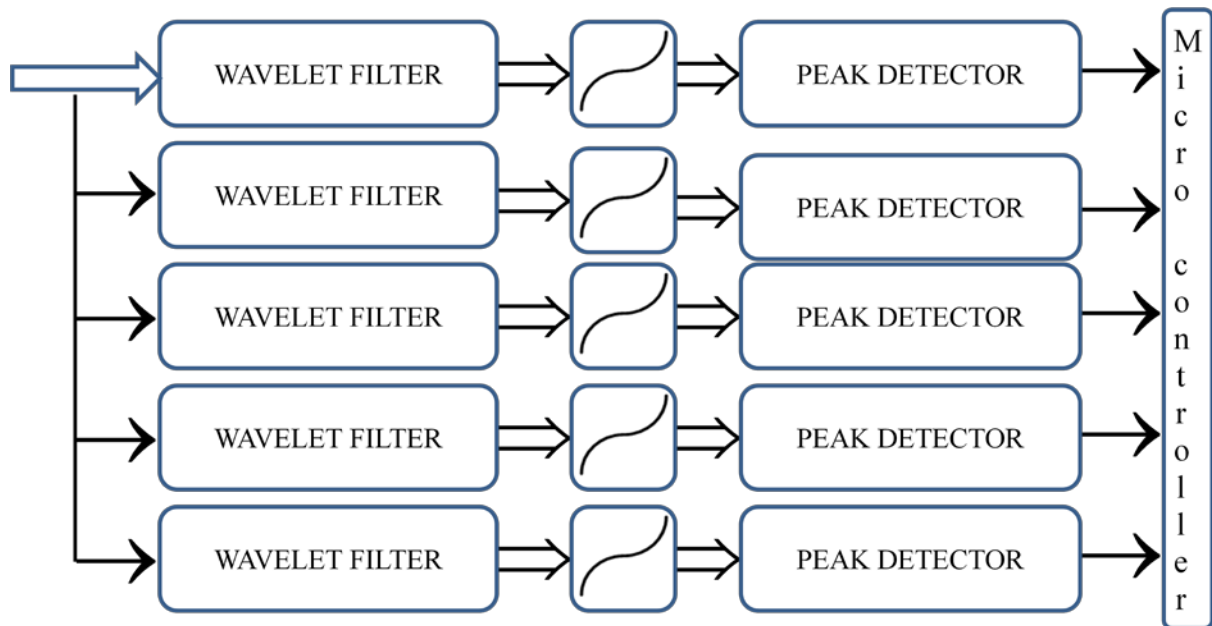


Figure 1.7: Block diagram of the whole system

1.9. Summary

In this chapter a brief overview of the biomedical signals, especially the heart signal and the functionality of the heart are presented. The QRS complex and T wave are the most important parts of the ECG signal. The QRS complex and the T wave will be detected by using a wavelet filter bank and a detector circuit.

The WT is used to construct the wavelet filter bank. This method is able to represent a signal in both the time and the frequency domain. The first derivation of a Gaussian wavelet is chosen as a mother wavelet, which looks more like a signal. The SVD approximation obtains a low-order and a good, fit transfer function of a wavelet impulse response. The state-space description is obtained from the SVD approximation that gives A, B, C and D matrices to implement the system. The Schwarz decomposition is used to increase the zero entries in all matrices, because the state-space description gives the fully dense matrices. The circuit design is based on wavelet filter in discrete time. The wavelet filter will be built by using the Schwarz structure which is the optimal state space representation. The circuit level design and building the wavelet filter for a single-scale is discussed in the next chapter.

2. One scale wavelet filter

The trend towards lower power consumption and higher frequency operation increased the interest in new design techniques for analog integrated filters. Wavelet transform analysis is a useful tool and a new way to design analog signal processing. The aim of this chapter is to focus on ultra low-power integrated discrete-time filter design, but first we will show the impulse response of the Gaus1 wavelet filter.

The whole structure of a single-scale wavelet filter is based on its state-space description. First of all, the ideal system will be constructed to get the ideal result. This ideal result will be used as a reference result to compare it with the real circuit result. In this way, we can find the difference between these results and improve the circuit to get the best result that is close to the ideal one. The ideal system means the system with ideal components, such as switches, opamp and capacitors. This system is built using Matlab Simulink. Second of all, the system will be constructed with switches, opamp and common-mode feedback circuit by using the ideal component in Cadence. Finally, the system will be built using the non-ideal components.

One suitable structure for this design is a fully differential switched-capacitor circuit with a fully differential folded cascode amplifier which has a switched-capacitor common-mode feedback structure. Michiel Grashuis [5] used this structure to construct a single-scale wavelet filter. However, there were some problems with that circuit as listed in section 2.3. In section 2.4, the problems are addressed and discussed. In section 2.5, the noise behavior of the resulting circuit is simulated and improved by further optimizing the circuit.

So, starting from the thesis results from Michiel Grashuis' [5], this thesis will go further and improve the wavelet filter circuit of one scale (this chapter), add a peak detector (chapter 3) and present a design for the whole bank of several wavelet filters and detectors (chapter 4).

2.1. System design

The wavelet filter is built up with Matlab Simulink to check the functionality of the state-space description. This structure can be seen in the Figure 2.1. In this figure, all the triangles which are labeled a, b and c, are the entries from the A, B and C matrices in equations 1.11 to 1.14, respectively.

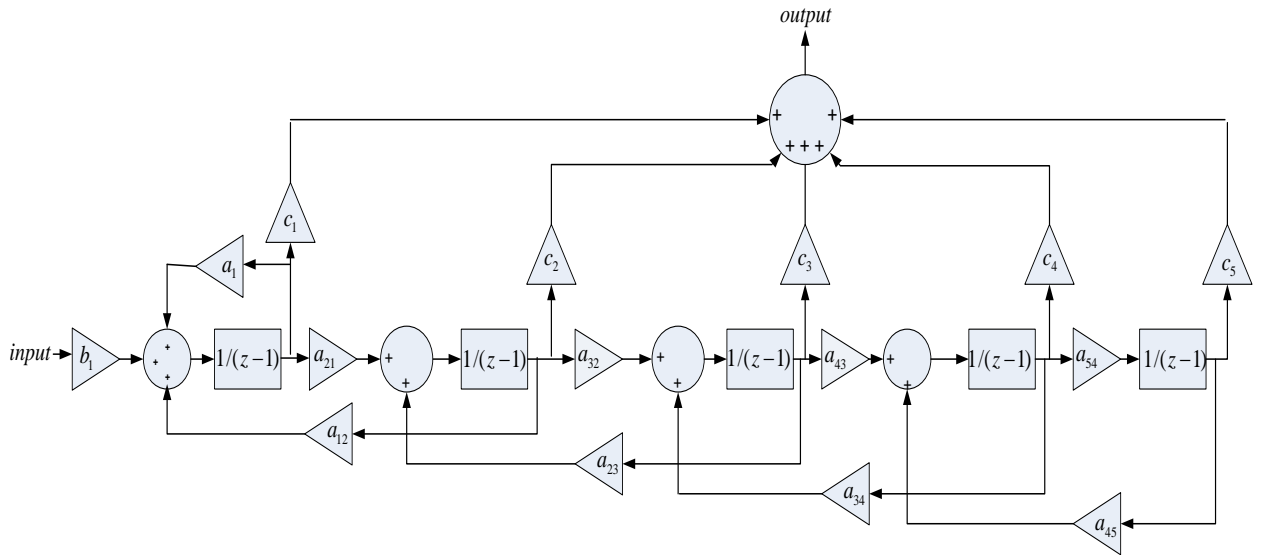


Figure 2.1: A block diagram of a fifth-orders state-space description

After running the system in Matlab with an impulse as input signal, the result in Figure 2.2 is obtained and compared with the Gaus1 wave. This figure shows that the wavelet filter in the system level works optimally and the difference between the ideal Gaus1 and the impulse response of the wavelet filter is quite small. That is because of the minimum mean-square error of the SVD approximation. This ideal impulse response is considered to the reference result, and we will strive to get almost the same result from our design in the circuit level.

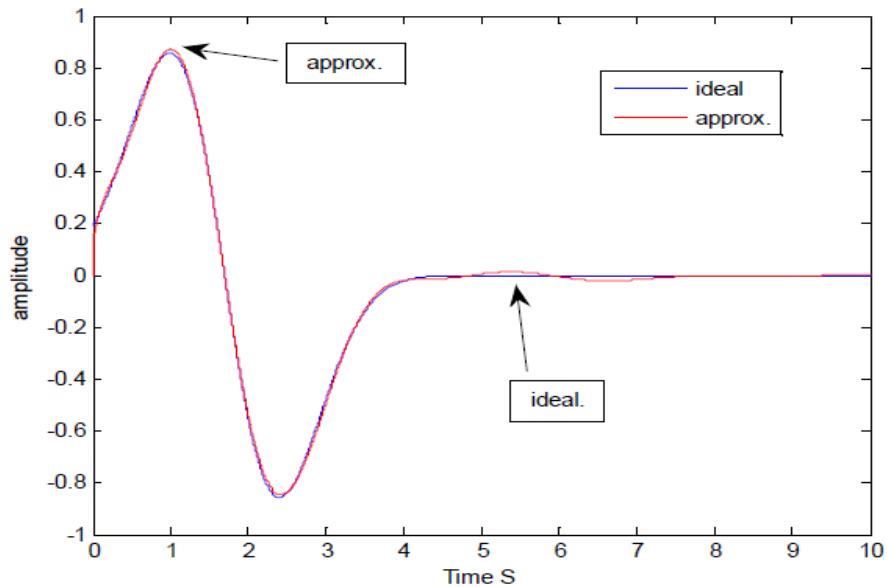


Figure 2.2: The impulse response of the state-space description

2.2. Circuit design

Integrated switched-capacitor filter is an attractive structure for many applications because of its accurate capacitors ratio to obtain a desired close loop gain. This model is used to realize the wavelet filter for our design. In this chapter, the circuit to realize this wavelet filter is discussed. The circuit consists of switched-capacitor integrators (section 2.2.1), an opamp (section 2.2.2) and common mode feedback (CMFB) (section 2.2.3). The structure of discrete time filters is implemented by using the switched-capacitor topology and the fully differential folded cascode integrator. The switches are activated with a pulse generator circuit. In the next section, the structure of the switched-capacitor integrator circuit is presented and designs of the opamp and CMFB for the opamp are discussed in section 2.2.2 and 2.2.3, respectively.

2.2.1. Switched-capacitor Integrator

A simple switched-capacitor (SC) integrator circuit is given in Figure 2.3. SC integrator consists of capacitors C_S and C_f , switches S_1 and S_2 and an opamp. The switches alternatively connect the capacitors to the input and output of the SC with a given frequency.

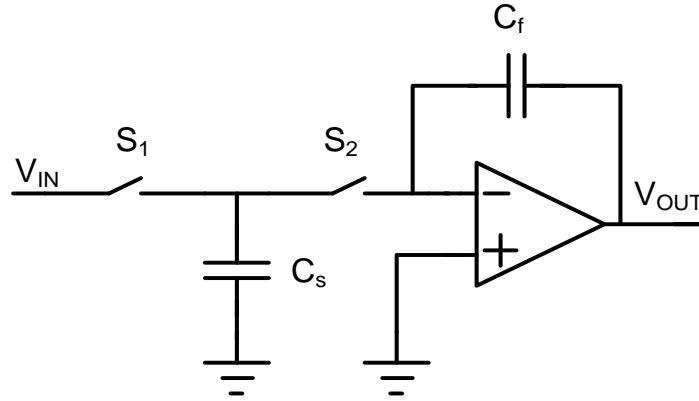


Figure 2.3: A switched-capacitor integrator

It is very important to keep in mind here that the two clock phases, which are used to drive the switches, need to be non-overlapping. Otherwise, when both switches are on and the charge will inadvertently be lost.

The relationship between the output voltage and the capacitors C_f and C_S can be found as:

$$V_{OUT}(n) = -\frac{C_S}{C_f} \sum_0^n V_{IN}(n) + V_o(0) \quad 2.1$$

The operation of the SC integrator is briefly explained here. Each switching cycle transfers a charge q at the switching frequency f from the input to the output. Therefore, capacitor C_S is charged with the input voltage when S_1 is closed and S_2 is open. In the next clock phase, when switch S_2 is closed and S_1 is open, the charge stored in C_S is transferred to C_f . The charge, which is transferred in this cycle is given by:

$$q = C_F (V_{OUT} - V_I) \quad 2.2$$

where, V_I is the voltage at the virtual ground node. Since the charge q is transferred during the sampling time T_s , the average current will be equal to:

$$I_{avg} = \frac{q}{T_s} \quad 2.3$$

By substitution equation 2.2 into 2.3, the equation of average current will be changed to:

$$I_{avg} = \frac{C_s (V_{OUT} - V_I)}{T_s} \quad 2.4$$

When we compare equation 2.4 with Ohm's law, it is easy to check that R equals T_s/C_s , where V is the voltage across C_f as $(V_{OUT} - V_I)$. As a result, the discrete time integrator functions as continuous time integrator and the relationship between the resistor and the capacitor is given by:

$$R = \frac{1}{f \cdot C_s} \quad 2.5$$

where, f is the sampling frequency with the next expression.

$$f = \frac{1}{T_s} \quad 2.6$$

The sampling frequency is needed to be twice as high as the input signal to avoid aliasing. If a lower sampling frequency is used, the original signal's information cannot be recovered from the sampled signal. In addition, because of sampling the input signal in time domain of the input signal, there will be some $\text{sinc}(t)$ distortion [5]. This is because sampling a signal in the time domain is the same as multiplying this signal with an impulse train. A rectangular baseband filter is a suitable structure to reconstruct the sampled signal. This means that the signal is multiplied with a rectangular baseband filter in the frequency domain, which in turn means convolving the signal with a $\text{sinc}(t)$ function.

The structure and the functionality of the SC integrator are described. The SC structure needs some improvement. That is because in our state-space description matrices, we have the negative and the positive entries. This requires using non-inverting and inverting SC integrators. Another improvement to remove the parasitic capacitance of the SC integrator is described in the next subsection.

2.2.1.1. (Non) inverting switched capacitor integrator

The non-inverting and the inverting integrators are two different SC integrators, which can be seen in Figure 2.4 and Figure 2.6, respectively. To show how these topologies are used in our design, a short explanation of the SC filtering is presented here. The SC integrator techniques are used for filtering, and they have become very popular tools because of their accurate frequency response, good linearity and high dynamic range. Accurate frequencies can be obtained when the coefficients of the filters are determined by capacitance ratios. The coefficients of the filters are in this case are the coefficients in the matrix of the state-space description. The capacitance ratios can be defined precisely in integrated circuits. These ratios are obtained from the feedback capacitor and the switched capacitor. In our case we have five orders system and every order needs a SC integrator to implement a single-scale WF.

The state-space description matrices have entries of the capacitance ratios. To understand the relationship between every entry in the matrices A, B, C and D and integrator's capacitance ratios, all matrix coefficients are fitted onto the integrators which can be seen as below.

$$A = \begin{bmatrix} \frac{-C_{SA1}}{C_{FA}} & \frac{-C_{SA3}}{C_{FA}} & 0 & 0 & 0 \\ \frac{C_{SB1}}{C_{FB}} & 0 & \frac{-C_{SB2}}{C_{FB}} & 0 & 0 \\ 0 & \frac{C_{SC1}}{C_{FC}} & 0 & \frac{-C_{SC2}}{C_{FC}} & 0 \\ 0 & 0 & \frac{C_{SD1}}{C_{FD}} & 0 & \frac{-C_{SD2}}{C_{FD}} \\ 0 & 0 & 0 & \frac{C_{SE1}}{C_{FE}} & 0 \end{bmatrix} \quad 2.7$$

$$B^T = \begin{bmatrix} \frac{C_{SA2}}{C_{FA}} & 0 & 0 & 0 & 0 \end{bmatrix} \quad 2.8$$

$$C = \begin{bmatrix} \frac{C_1}{C_{FF}} & \frac{C_2}{C_{FF}} & \frac{C_3}{C_{FF}} & \frac{C_4}{C_{FF}} & \frac{C_5}{C_{FF}} \end{bmatrix} \quad 2.9$$

In the above matrices, the capacitor ratios can be seen. A brief explanation gives how the entries are connected to the integrators. Every integrator is labeled with A to E and subscript S is denoted for switch in every integrator and F is denoted for feedback. To make it clearer, let's look at the second row in matrix A. It has two non-zero entries C_{SB1}/C_{FB} and $-C_{SB2}/C_{FB}$ which are on positions a_{21} and a_{23} , respectively. C_{SB1} and $-C_{SB2}$ are the switched-capacitors of integrator B. C_{FB} is the feedback capacitor of integrator B and it shows that the input signal of integrator B receives from the output of integrators A and C. The non-zero entry in matrix B is the filter's input and the entries of matrix C implement the outputs matrix.

As mentioned, the coefficients of the state-space matrices are implemented by means of capacitance ratios in the integrators. Some of these coefficients are positive and others are negative. To implement both positive and negative coefficients, it is necessary to use both non-inverting and inverting SC integrators. The non-inverting switched-capacitor integrator structure is shown in next figure. This implements the first-order transfer function as below.

$$H(Z) = \left(\frac{C_s}{C_f} \right) \cdot \frac{1}{z-1} \quad 2.10$$

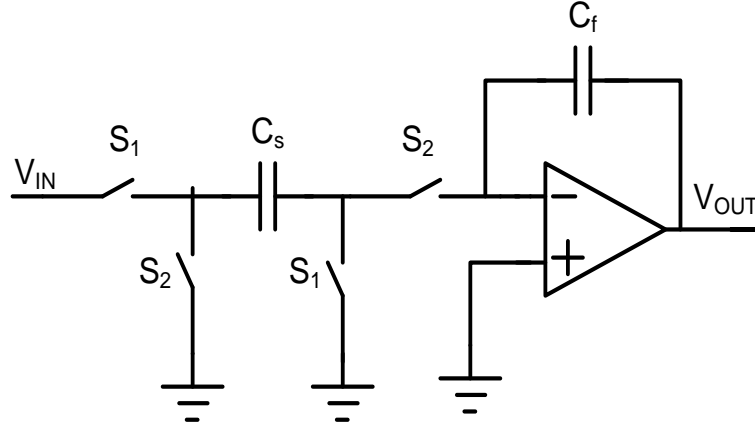


Figure 2.4: Non-inverting SC integrator

In this figure S_1 and S_2 are representing the clock phases which are non-overlapping. It is needed to prevent losing the charge. In our design the clock frequency of the highest scale which zooms in the lowest frequency of heart signal, is 300 Hz. This is because the highest frequency component of heart signal is about 150 Hz, and two times higher clock frequency makes sure that all frequency components are covered. As an example, the two non-overlapping clock signals are presented in the next figure.

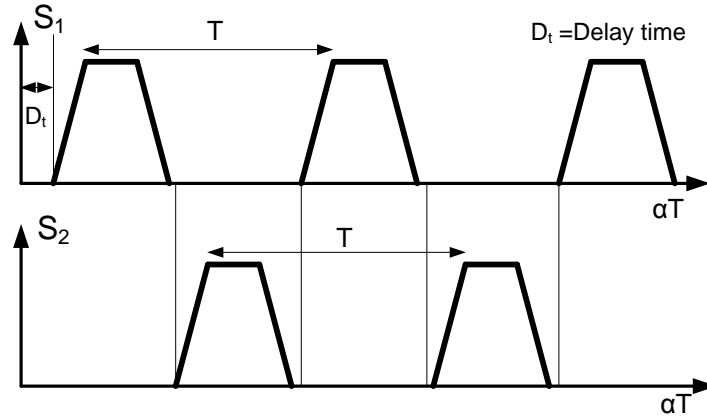


Figure 2.5: Non-overlapping clock signals

The topology of the inverting switched-capacitor integrator is shown in Figure 2.6, which implements the first-order transfer function, as shown in equation below.

$$H(Z) = -\left(\frac{C_s}{C_f}\right) \cdot \frac{1}{z-1} \quad 2.11$$

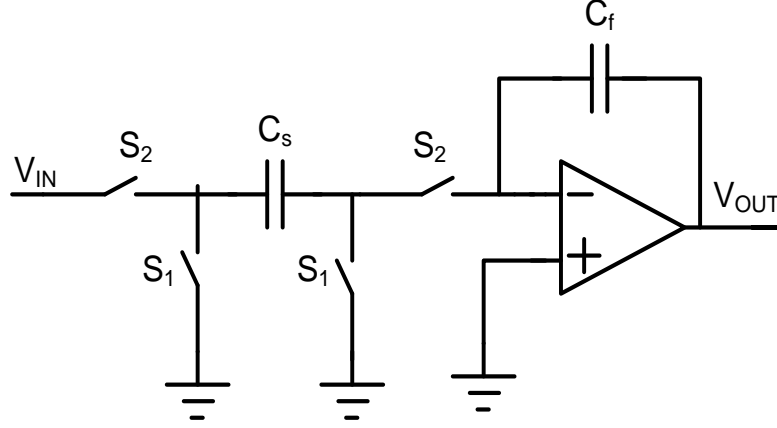


Figure 2.6: Inverting SC integrator

These two topologies of SC integrator have more switches as compared to the topology of Figure 2.3. The most important reason to use extra switches is that the switches suffer from parasitic capacitances. These parasitic capacitances affect the frequency response and degrade the performance of the filter. By using the insensitive SC integrator structure that can be seen in Figure 2.5 and 2.6, the parasitic effect will be solved.

The main building blocks of the circuit are now known, and another optimization step can be taken. This step matches the optimal capacitance distribution to the noise contribution of each individual integrator (noise scaling). In addition, the relative noise contribution of an integrator decreases when the capacitance and bias current increase. The noise scaling is done with the following equation.

$$C_i = C_{tot} \cdot \frac{\sqrt{\alpha_i \cdot W_{ii} \cdot G_{ii}}}{\sum_j \sqrt{\alpha_j \cdot W_{jj} \cdot G_{jj}}} \quad 2.12$$

where,

$$\alpha_i = \sum_j |A_{ij}| \quad 2.13$$

C_i is the feedback capacitor of i^{th} integrator and C_{tot} is the total feedback capacitance of the integrators. W and G are Observability and Controllability Gramian matrices, respectively.

By this optimization step, the dynamic range value is almost the same as the optimum dynamic range [5], which is obtained from Equation 1.8.

$$DR_{\text{schwarz-capscale}} = 162.1 \text{ dB} \quad 2.14$$

The structures of the switches are determined, and now it is possible to implement the whole system in the differential mode. This topology is now seen in the next figure.

This circuit is a macro model of the opamp with a high DC gain because of its high output resistance (R) and high g_m (ggain). This is just a model of the single ended amplifier. This circuit will be replaced by the opamp in Figure 2.7, and the wavelet filter will be constructed according to the fifth order state-space description as discussed before. In this way, the result should be the same as that of Matlab, which is obtained in Figure 2.2. Maybe it is an elegant way to fine the specifications of the opamp, but it is good to mention that we do not know how accurate the opamp should be to approximate the ideal wavelet. In this way, we can find the optimum features of the opamp.

The ideal opamp is built with the voltage controlled current source and the output resistor R (Figure 2.8). The DC voltage gain in this circuit is $g_m * R$. we chose a big value for the R and with tuning g_m we can find minimum DC gain. Now the only thing to define is g_m of the voltage controlled current source. With the high g_m , it is clear that the opamp acts as an ideal opamp, and the impulse response from the transient simulation looks like an ideal one. The minimum g_m can be found by decreasing g_m , because at one point, the impulse response starts to differ from the ideal one. This gives the minimum value of g_m . The DC voltage gain at this point which is obtained from $g_m * R$ is 38.59 dB. The allowable steady state error is about 0.01.

The other specifications that need to be determined are the gain bandwidth and the settling time of the opamp, which are obtained in a similar way. It means that by using a capacitor in parallel to the resistor, the time constant can be obtained, which sets the bandwidth of the opamp. The gain bandwidth (GBW) of the opamp can be calculated by assuming a first order behavior of opamp. The GBW that is obtained from that is 1 kHz. The Figure 2.8 is calculated using the lecture notes of Klaas Bult [19]. The maximum GBW is needed to obtain the best slew rate (SR), and the optimum DC gain is necessary for minimum settling time (ST).

The exact specifications are difficult to obtain, because currently we do not know how good the impulse response should be and what the acceptable error is. That is why the specifications obtained here are used to construct the opamp. These are 38.59 dB for the minimum DC gain and 1 kHz for the minimum gain bandwidth. The value of GBW is implemented by decreasing the gain bandwidth until the shape of impulse response is deformed compared to the ideal impulse response.

Based on these requirements, a folded-cascode opamp has been constructed as shown in the figure below.

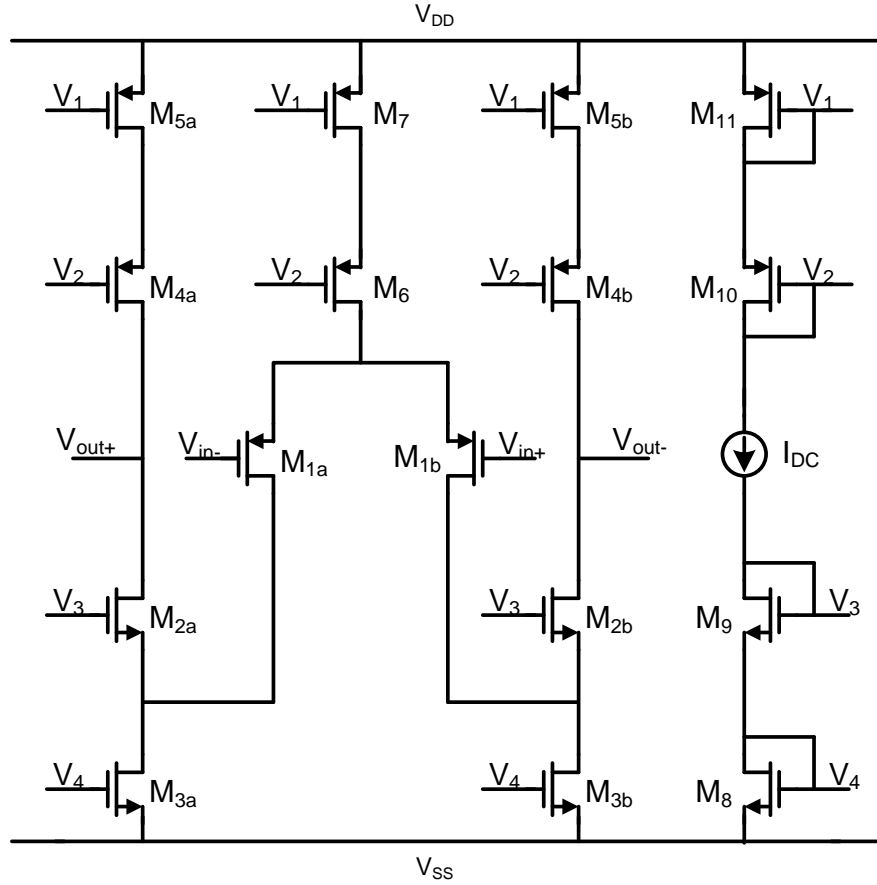


Figure 2.9: The folded cascode opamp

The right branch in Figure 2.9 is the biasing circuit and the remaining part of the figure is the opamp itself. Folded cascode architecture is chosen with PMOS input differential pair. A simple differential pair doesn't provide enough gain. In addition, the PMOS input differential pair has lower flicker noise as compared to the NMOS. This is because given n+ poly gates on N and P devices, the NMOS channel is at the surface of the Si-SiO₂ layer, while the PMOS channel is below the surface. Since many of the trap points that lead to flicker noise are at the surface, a buried channel device (PMOS) should have lower flicker noise.

The DC gain of the differential pair (M1a, M1b) is $g_m \cdot r_o$ which can be increased by adding a cascode stage. This cascode stage increases the DC gain by increasing the output resistance. The output voltage swing of the folded cascode opamp (Figure 2.9) is calculated as follows. By choosing a desired value for V_2 and V_3 , the lower end of this swing will be $V_{SD2} + V_{SD3}$ and the upper end $V_{DD} - (|V_{SD4}| + |V_{SD5}|)$. Thus, the total peak-to-peak swing on each side will be $V_{DD} - (V_{SD2} + V_{SD3} + |V_{SD4}| + |V_{SD5}|)$.

To determine the small-signal voltage gain of the opamp, one half of the circuit, as shown in Figure 2.10, will be analyzed. The equation of the small-signal voltage gain can be written as $|A_v| = G_m \cdot R_{out}$. To find the G_m in Figure 2.10, the output is grounded. The output current is almost the same as drain current of the transistor M_{1a} . That is because the output impedance ($\frac{1}{g_{mM2a}} \parallel r_{OM2a}$) is much lower

than the impedance seen by looking at the ground node through M_{3a} , which is $r_{OM1a} \parallel r_{OM3a}$. This leads to the conclusion $G_m \approx g_{mM1a}$.

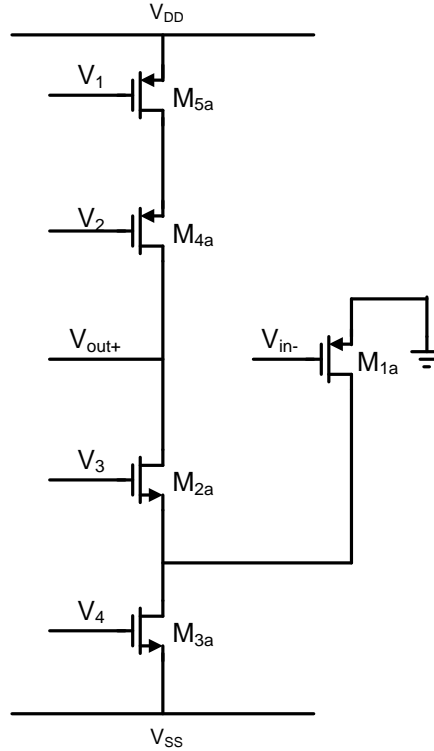


Figure 2.10: The half circuit of the folded cascode opamp

The output resistance (R_{out}) can be calculated as follows. By looking into the circuit at the output node, the impedance of transistors M_{4a} and M_{5a} , that is $g_{m4}r_{O4}r_{O5}$, is in parallel to the rest impedance, which can be seen from drain of transistor M_{3a} . This impedance is about $g_{m2}r_{O2}(r_{O1} \parallel r_{O3})$. This gives the total output impedance as in the next equation.

$$R_{out} = (g_{m4}r_{O4}r_{O5}) \parallel [g_{m2}r_{O2}(r_{O1} \parallel r_{O3})] \quad 2.15$$

The complete equation of the voltage gain for the whole circuit can be written as in the following equation by using $G_m \approx g_{mM1a}$ and Equation 2.15.

$$A_v = G_m * R_{out} = g_{m1} (g_{m4}r_{O4}r_{O5}) \parallel [g_{m2}r_{O2}(r_{O1} \parallel r_{O3})] \quad 2.16$$

As mentioned in the beginning of this chapter, this opamp is fully differential because the entire filter is built up differentially. This means that it is not needed to use two single ended opamps, which consume more power. To fix the output common mode of the opamp properly [5], another condition for the fully differential opamp is required. That is the need of common-mode feedback, which is presented in the next section.

2.2.3. CMFB

As discussed, the opamp needs a CMFB circuit. In Figure 2.9, the output voltages (V_{out+} , V_{out-}) must be fixed at the CM voltage. However, because of the load transistors ($M3a$, $M3b$) the common-mode (CM) level depends on the drain currents of these transistors. In practice, PMOS and NMOS current mirrors in this figure have mismatches, which create a finite error between the drain currents through the load transistors and $I_{SS}/2$, which is the current through $M1a$ or $M1b$. This brings the output voltages out of balance. This requires using the CMFB to set the output common mode of the opamp properly [10].

A suitable CMFB structure for the SC fully differential folded cascode is a SC common-mode feedback circuit with respect to continuous time version power consumption. The structure of a SC common-mode feedback can be seen in the next figure.

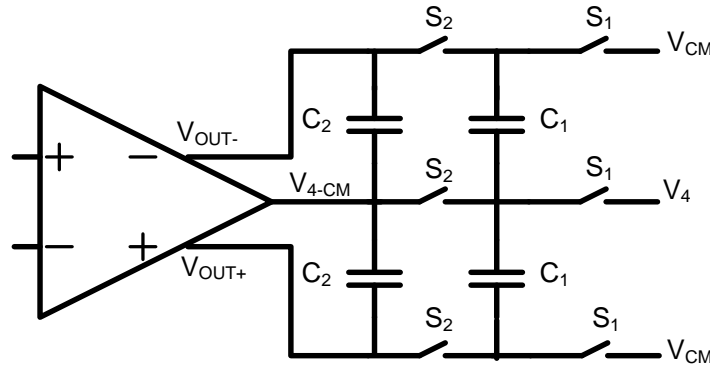


Figure 2.11: A switched-capacitor CMFB scheme

In the SC CMFB, the output voltages are sensed by capacitors and sent to the common mode voltage. In other words, the CMFB circuit that consists of the switches and capacitors in Figure 2.11 sense the common mode output voltage and subtract it from the common mode reference voltage (V_{CM}). The output voltage of the sense circuit is compared to the desired CM voltage and a bias voltage required to control the current sources of the opamp is produced. To make it clear how it works, the basic principle used in SC-CMFBs is implemented in the next figure.

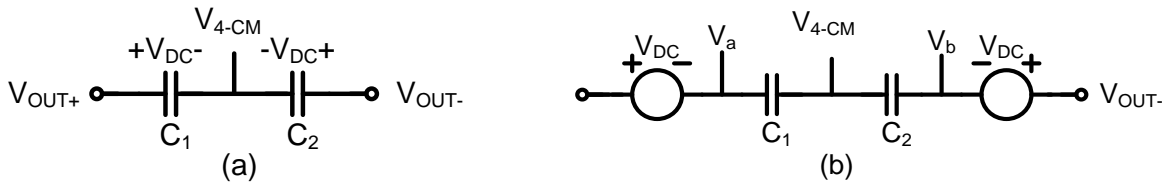


Figure 2.12: Simple CMFB with capacitors (a), DC voltage of capacitors as voltage sources (b)

Figure 2.12 (a) is a basic principle used in SC-CMFB. The two capacitors C_1 and C_2 are charged to the voltage V_{DC} with the polarity indicated. The output voltages V_{OUT-} and V_{OUT+} are level-shifted by V_{DC} and then averaged by capacitors C_1 and C_2 to produce the desired bias voltage. This DC voltage can be represented by a series voltage sources as shown in Figure 2.12 (b). This can be written in an equation using the equation of the voltage across through the C_1 and C_2 .

$$V_{4-CM} = \frac{C_1 \cdot V_a + C_2 \cdot V_b}{C_1 + C_2} \quad 2.17$$

If the next equations are used in Equation 2.17, Equation 2.19 will be obtained.

$$\begin{aligned} V_a &= V_{out-} - V_{DC} \\ V_b &= V_{out+} - V_{DC} \end{aligned} \quad 2.18$$

$$V_{4-CM} = \frac{C_1(V_{out-} - V_{DC}) + C_2(V_{out+} - V_{DC})}{C_1 + C_2} \quad 2.19$$

By rearranging Equation 2.19 and assuming that C_1 and C_2 are equal, the next equation will be obtained.

$$V_{4-CM} = \frac{V_{out-} + V_{out+}}{2} - V_{DC} = V_{CM} - V_{DC} \quad 2.20$$

where, $V_{CM} = V_{out-} + V_{out+} / 2$ is the output common-mode voltage. This result shows that the output common-mode voltage can be set by using the series connected capacitors.

The whole circuit is implemented and can be constructed for simulation. In the last design of a fully differential switched-capacitors wavelet filter of Michiel Grashuis [5], the impulse response of the wavelet filter for the lowest frequency (300 Hz) suffers from the unwanted spikes. This impulse response can be seen in the next figure. This result is obtained by means of transient analysis.

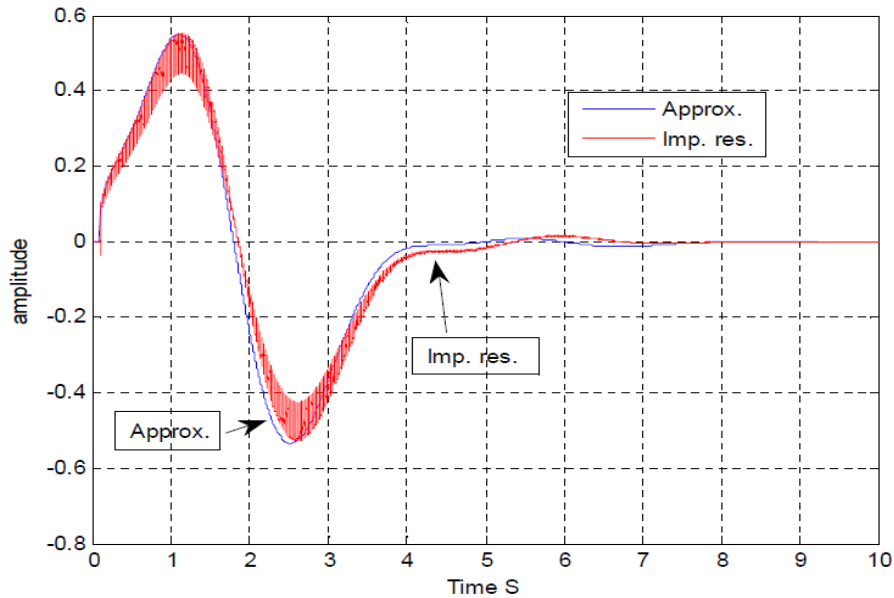


Figure 2.13: The impulse response of the first scale wavelet filter [5]

A discussion about the problems of opamp is presented in the next section.

2.3. Problems

The last result of the wavelet filter is not accurate enough to be used it for the detector circuit because of its high spikes. These spikes will affect the ECG signal as input signal and make it difficult to detect the QRS complex and T-wave. The spikes of the impulse response can have several reasons, such as charge injection, speed of the opamp and also the behavior of the CMFB circuit. Besides these problems, the SC integrator circuit has another problem, which is the clock feedthrough. These problems are briefly discussed in the next subsections.

2.3.1. Charge injection

The SC structure is built by using minimum size NMOS switches. This is because they cause the least charge injection. From the simulation this is proved to be insufficient. The charge injected by the NMOS switch connected to the opamp can be counteracted by a dummy switch driven by the opposite clock signal during the same clock phase. The dummy switch has half the size of the switch of the SC circuit. This means that the size of the all switches must be doubled. This increases the area of the circuit, but the charge injection will be cancelled. The way to connect the dummy switch can be seen in the figure below.

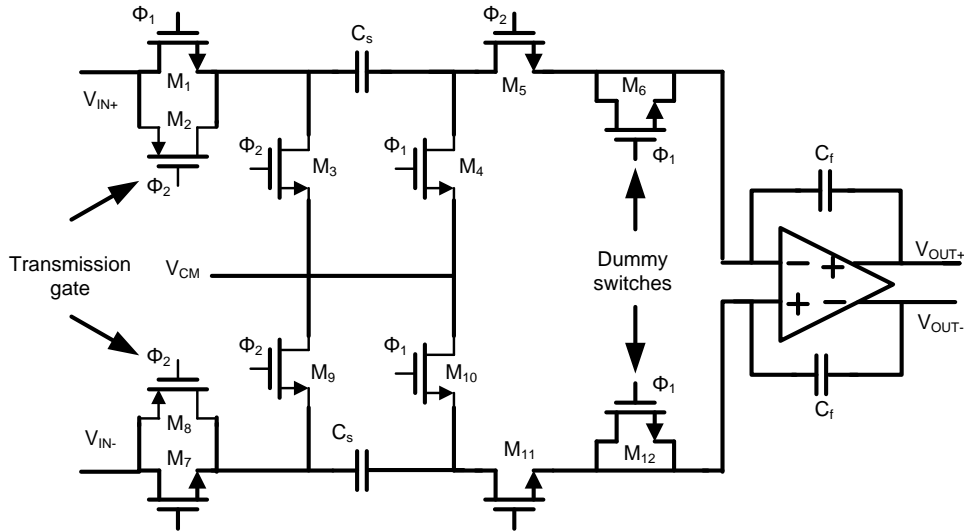


Figure 2.14: A fully differential switched capacitor block with MOS

2.3.2. CMFB behavior

Another important optimization is the ratio of the capacitors in the SC common-mode circuit. Charging and discharging of the capacitors cause the ripples in the CM voltages, which must be fixed at the CM voltage. To decrease this effect, the optimum ratio of these capacitors must be found. By trial and error techniques and checking the result of CMFB behavior with transient analysis in Cadence, an acceptable ratio (1/3) is obtained.

2.3.3. Speed of opamp

The speed of the opamp is an important aspect. The charge from the input goes, through the feedback capacitor C_f to the output during the second clock phase before the opamp turns on. This charge causes part of the spikes. To increase the speed of the opamp, it is possible to increase the settling time by increasing the DC gain. This requires higher g_m , and consequently more power consumption. The opamp is optimized to have a higher speed, but it is not possible to prevent the charge through the capacitors. That is because the capacitor starts to charge at zero time. However, the opamp cannot settle so fast.

2.3.4. Clock feedthrough

Clock feedthrough is the result of coupling between control signals on the analog switch and analog signal passing through the switch. The clock feedthrough mechanism in the charge domain occurs when the switch turns off. The accumulation of a small positive charge on the source of a MOS switch, which occurs after the switch has been turned off due to the parasitic capacitance that exists between the gate and the source of the transistor, is known as clock feedthrough. Transmission gate topology avoids this effect. The topology of the transmission gate can be seen in Figure 2.14.

Now the spikes are small enough to be neglected. However, another way to decrease them is by employing the chopping technique. This technique increases the number of components which increase the area and power consumption. That is why this method is not tested in this thesis.

2.4. Results

After optimal design, the simulation process is the next step. For the first step, the ideal components are chosen for the wavelet filter circuit. The structure of switches in an ideal version is shown in Figure 2.15. The ideal opamp is discussed in a separate section and its ideal version can be seen in Figure 2.8. The simulation is successfully done with the transient analysis in Cadence. Its result is presented in Figure 2.16.

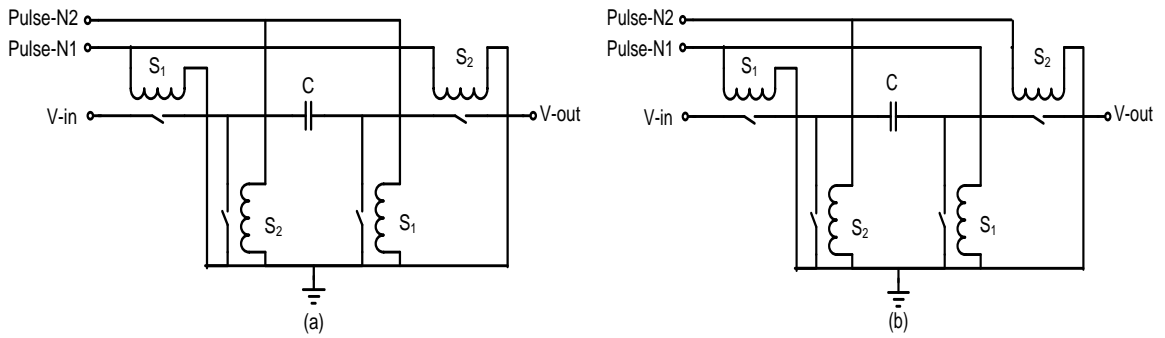


Figure 2.15: The non-inverting (a) and inverting (b) SC structure in ideal version

In the figure below the result of the transient simulation is presented. It is clear that this result is almost the same as the system level result in Figure 2.2.

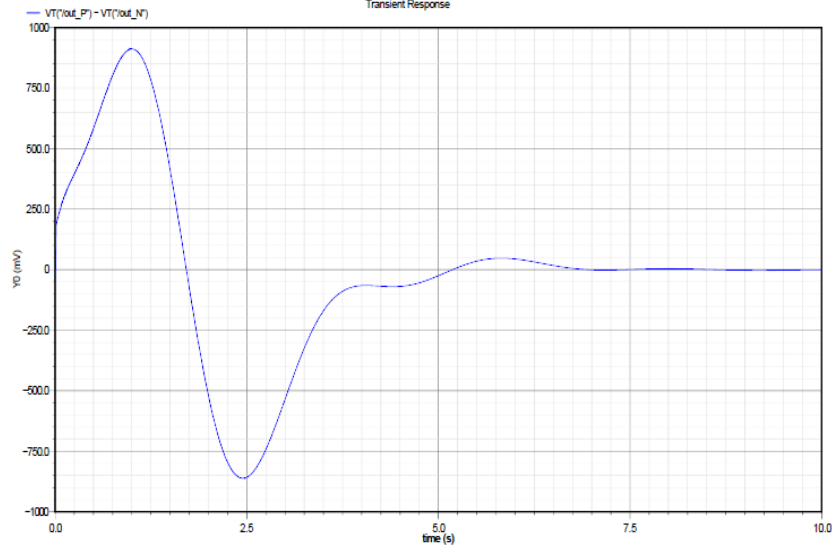


Figure 2.16: The impulse response of the ideal wavelet filter circuit

As mentioned before, by inserting the real circuit instead of the ideal one in the wavelet filter, the circuit is simulated. The result of every step of the simulation is compared to the reference result in the figure above. The starting point is to replace the SC amplifier, because it is the main circuit block of the wavelet filter, by changing the ideal switches with real NMOS transistors, as shown in Figure 2.14. That is the simulation in Cadence by using the transient analysis.

The inverting and non-inverting SC integrators use the same switches (M_4 , M_5 , M_6 , M_{10} , M_{11} and M_{12}) in the different clock phases. That is a good point to decrease the number of switches. In the next figure the structure of the real switches are presented with fewer components. This is done by using the last part of the inverting and the non-inverting structure (Figure 2.17 (b)) at the same time with multiple front parts. The total number of switches in every SC fully differential integrator is 24. 12 switches are for implementing the inverting SC integrator and 12 switches for the non-inverting SC integrator (Figure 2.14). We have five orders in every scale with the same number of switches. By using the last part of switches in the SC integrators, the numbers of switches are reduced from 24 to 18 for every SC integrator, and in total from 120 to 90 switches for every scale.

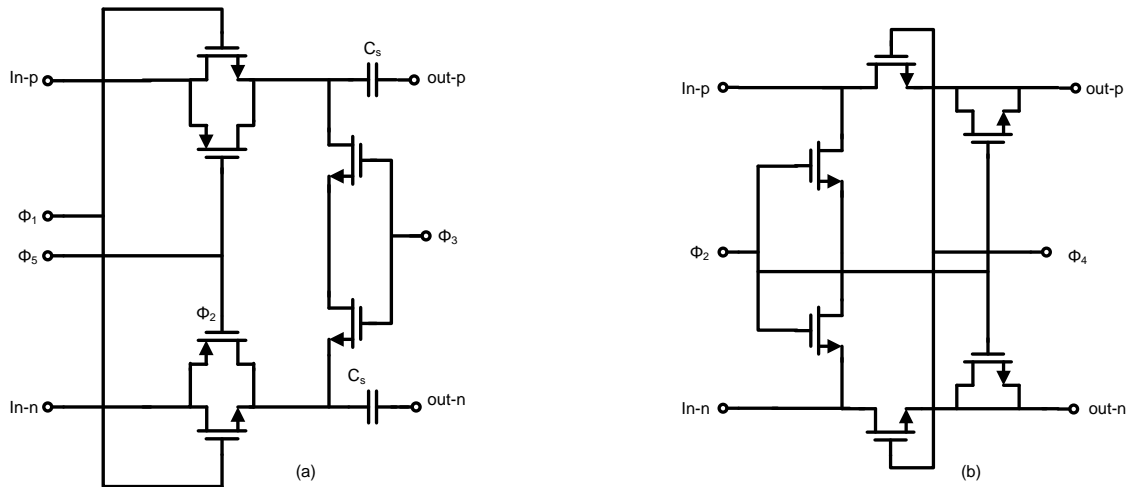


Figure 2.17: The SC structure in real form. (a) Front part and (b) End part

The front part and the end part play the role of both inverting and non-inverting SC circuits. As it can be seen in the Figure 2.17, to make the inverting and non-inverting switched-capacitor structures, it is enough to connect Q_1 , Q_2 , Q_3 , Q_4 and Q_5 to the clock pulses in a correct way. The functionality of these structures is the same as inverting SC structures if Q_1 and Q_2 are connected to pulse 1, Q_3 and Q_4 to pulse 2 and Q_5 to pulse 3, which is the invert of the pulse 1. This is clearly shown in Figure 2.17. For non-inverting SC structure, it is just needed to connect Q_1 , Q_4 to pulse2 and Q_2 , Q_3 to the pulses 1. Q_5 is connected to pulse 4, which is the invert of the pulse 2. Pulse 1 and 2 are the non overlapping pulses, as described in Figure 2.5. Pulses 3 and 4 are the same as pulses 1 and 2 with opposite value in high and low levels.

The opamp is replaced by the real one which is a fully differential folded cascode, as shown in Figure 2.9. The p_{ac} simulation is performed to get the frequency response of the circuit. This gives the values of the DC gain and the unity gain bandwidth (UGB). The result of the p_{ac} simulation is given in the figure below.

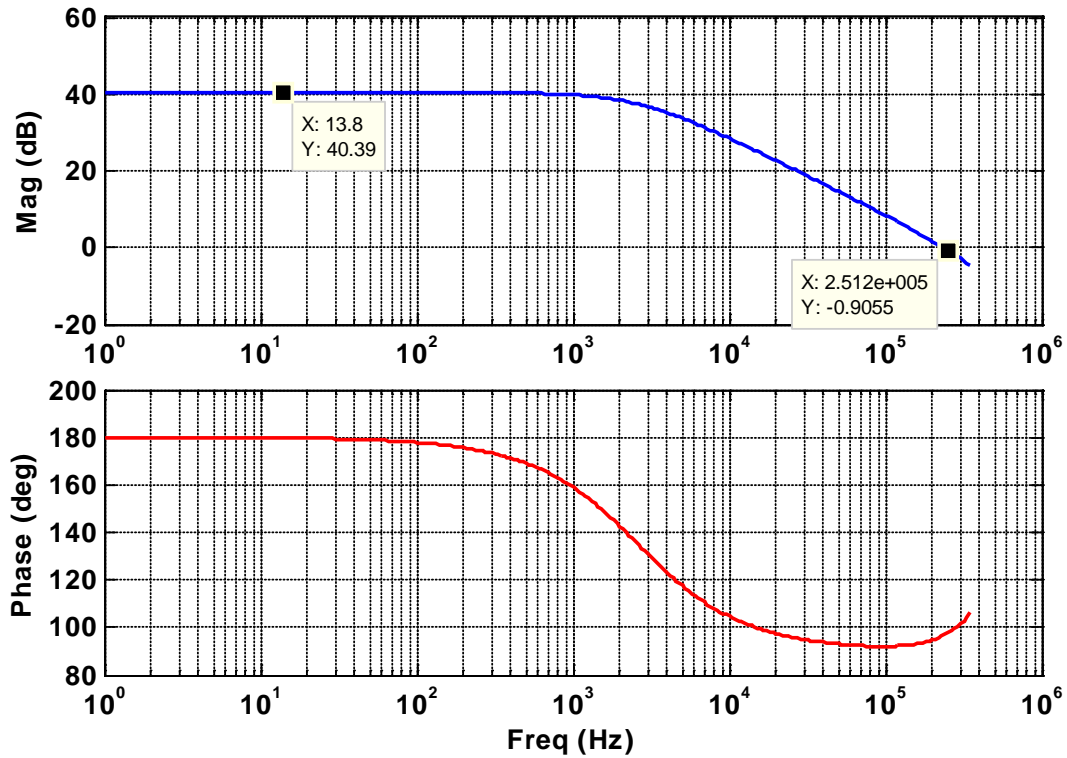


Figure 2.18: The magnitude and phase behavior of the opamp

The x-axis in both graphs in Figure 2.18 is frequency, and the y-axis is the magnitude in top and phase in bottom graph. The opamp needs the CMFB circuit to set the output DC voltage properly. The structure of CMFB is added to the opamp, as can be seen in the next figure. To verifying the functionality of the CMFB circuit, a transient analysis is performed.

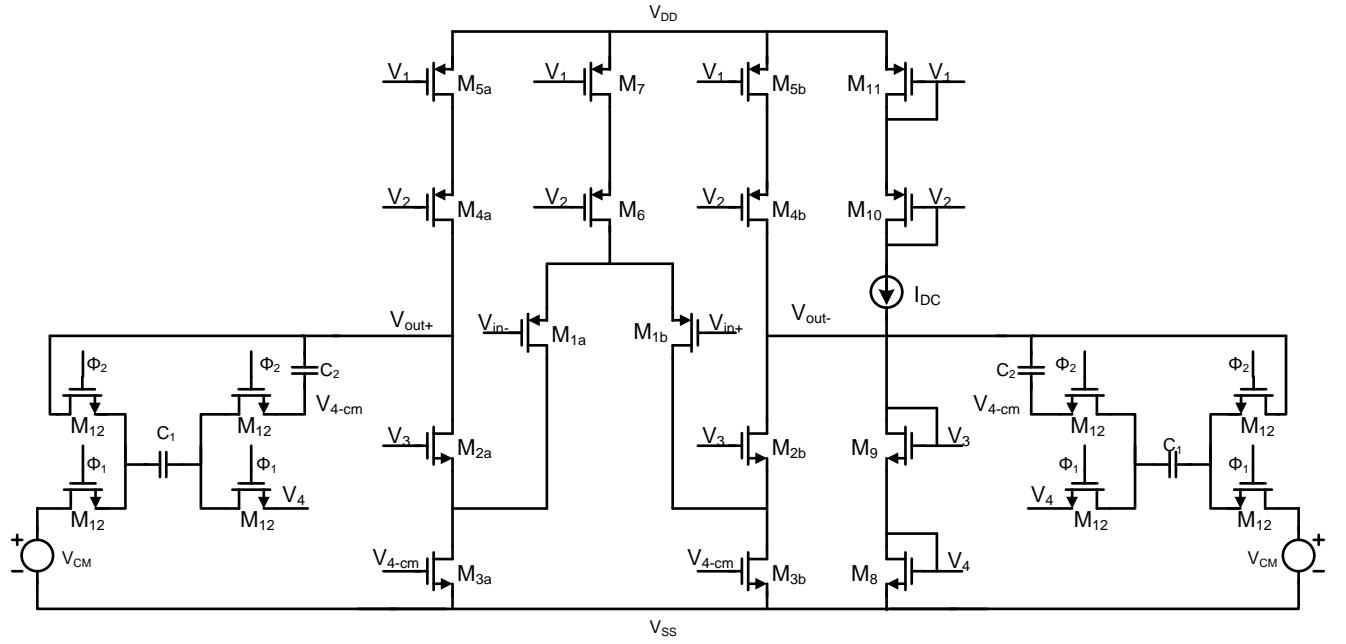


Figure 2.19: The whole structure of the opamp and the CMFB circuit

This design uses a power supply voltage of 1.2V. To get the maximum voltage swing at the output of the integrator, the common mode voltage is set to the middle of the power supply range (600 mV). Half of the power supply voltage gives the optimum dynamic range, which is obtained before. That result is obtained under the condition that signal swing is the same at the output of all integrators. The CMFB behavior is presented in Figure 2.20 using the transient analysis. The opamp is simulated in Cadence using RF specter and 0.13 μm CMOS model parameters. Transistor widths (W) and lengths (L) are given in Table 2.1.

Table 2.1: Transistor dimensions

MOSFET	M _{1a,b}	M _{2a,b}	M _{3a,b}	M _{4a,b}	M _{5a,b}	M ₆	M ₇	M ₈	M ₉	M ₁₀	M ₁₁	M ₁₂
W/L ($\mu\text{m}/\mu\text{m}$)	2/0.13	2/0.13	16/0.26	2/0.13	2/0.13	2/0.13	2/0.13	2/0.13	2/0.13	2/0.13	2/0.13	0.16/0.12
M	16	4	2	8	4	4	8	4	4	4	4	1

The power supply voltage range for correct operation is checked. V_{DD} is verified until the impulse response is deformed and the wavelet filter could not show the Gauss1 impulse response any more. V_{CM} must always be the half of the V_{DD} to get the correct power supply voltage range. The range of V_{DD} is between 0.8 V and 1.64 V.

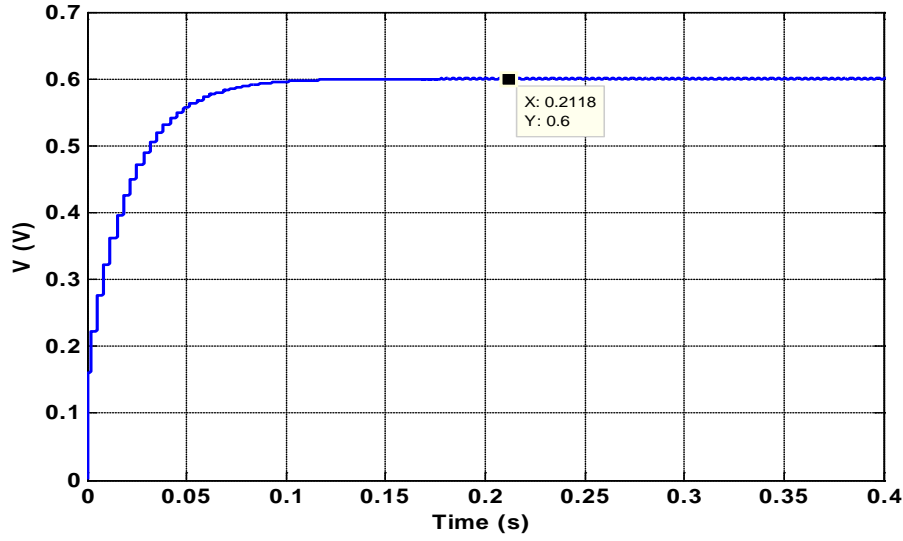


Figure 2.20: The common-mode feedback response with transient analysis

Every part of the wavelet filter is now replaced by the real one to implement the one scale wavelet filter with real components. This whole system is now ready to be simulated. . The first wavelet filter has a clock frequency of 300 Hz. This is two times higher than the heart signal frequency, which is about 150 Hz. This circuit is simulated with a transient analysis and the result is given in the next figure.

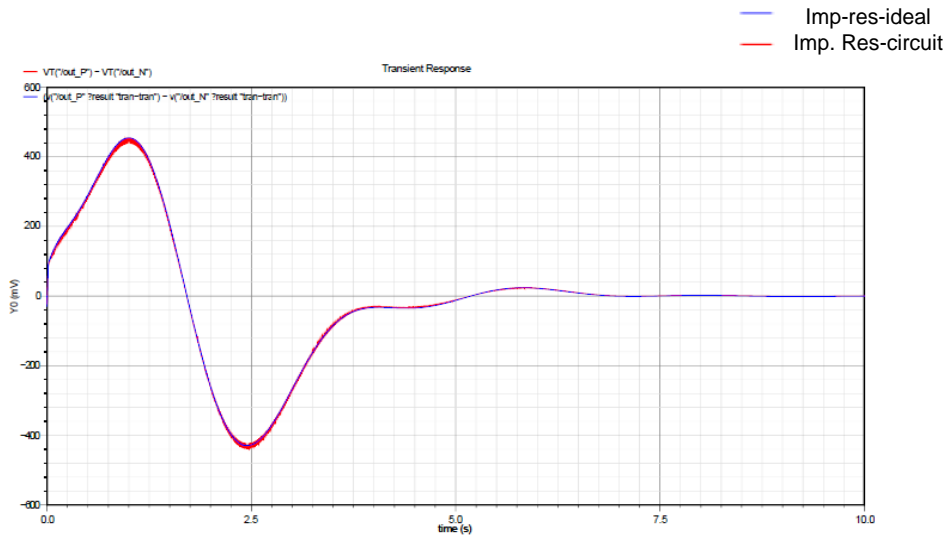


Figure 2.21: The impulse responses of the first scale wavelet filter with less spike

The amplitude of the impulse response is about 850 mV peak-to-peak. The detector will be implemented for a variation of the input signal of about 300 mV peak-to-peak. That is why the amplitude of the impulse response is decreased to 250 mV, which is a safe value for the detector. This decreasing amplitude is done by changing the value of the capacitors of the C matrix of the wavelet filter by the same ratio. The result is presented in Figure 2.22. The detector will be designed with a

sample and hold circuit at its input to take a sample of the impulse response. In this way, the spikes of the impulse response are not going through the detector, and they will be removed.

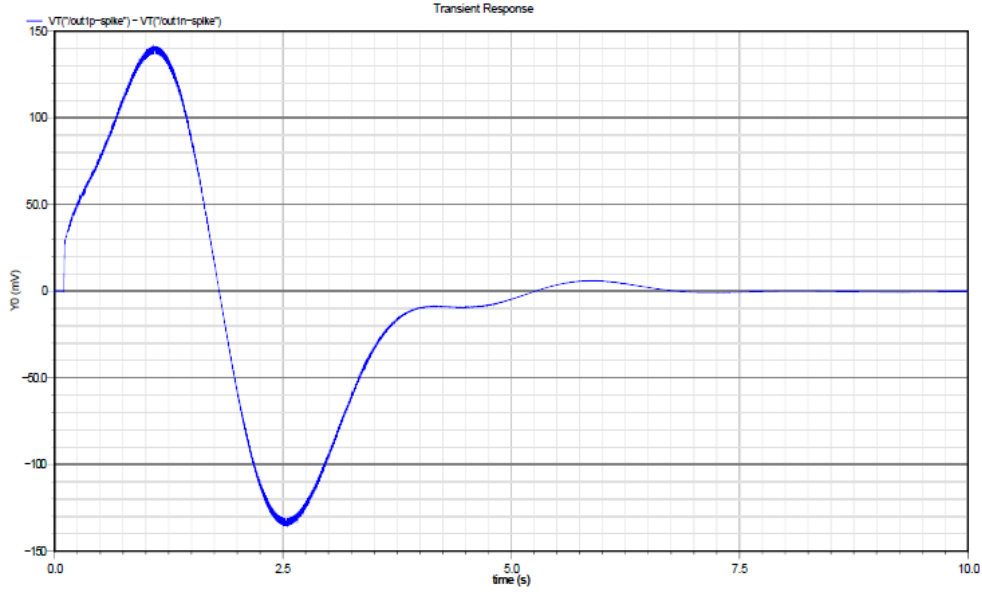


Figure 2.22: The impulse response of the first scale by matching the amplitude for detector

To see the bode plot of the whole system and check the frequency range of the filtering, *pac* and *pss* simulations are performed. The result is shown below.

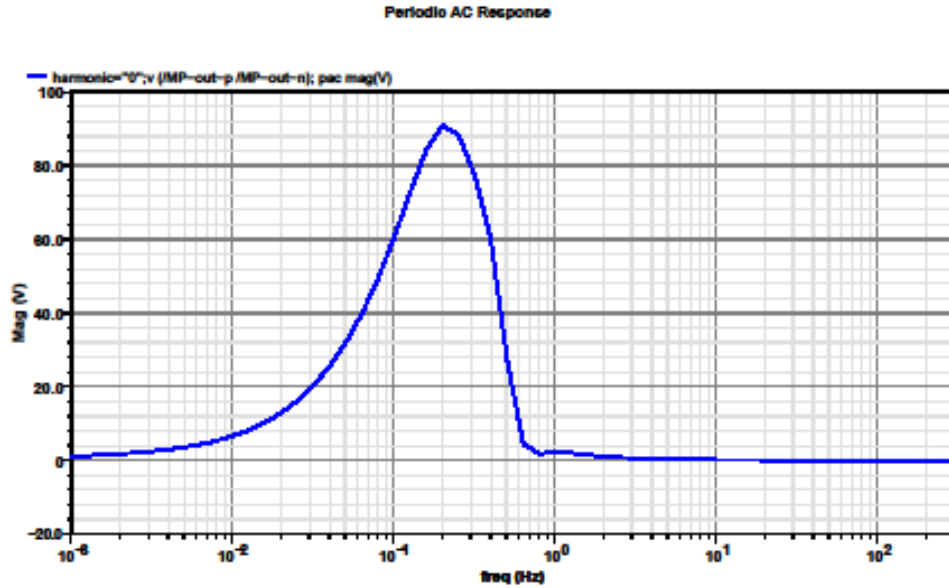


Figure 2.23: The magnitude response of the first scale wavelet filter

The total capacitance of every scale is of about 43.25 pF. This value is achieved after the optimization of the system due to the enhanced DR of WF topology and integrator. The total capacitance was about 75.89 pF before that. In the design of Haddad [1], the wavelet filter technique is used for detecting the ECG signal, which has the total capacitance of about 120 pF. In our design, this value is about three times smaller and this is one of the improvements in this thesis. This also decreases the area of one wavelet filter about three times.

2.5. Noise

The wavelet filter is constructed and its behavior is considered. In this design, the noise is another important aspect that must be considered. Different noise sources are present in our design, but the dominant source must be found. The noise sources in a transistor are thermal noise, flicker noise, gate induced noise and popcorn noise.

Since MOS's are essentially voltage-controlled resistors, they exhibit thermal noise. A MOSFET has an inverse resistive channel between the drain and the source. The gate voltage forms the channel with minority carriers. In the extreme case when the drain source voltage V_{DS} is 0, the channel can be treated as a homogeneous resistor. The noise in the channel is:

$$i_d^2 = 4.k.T.\gamma.g_m.\Delta f \quad 2.21$$

The thermal noise can be modeled by equivalent voltage source in series with the gate, as shown below.



$$V_d^2 = 4K.T.\frac{1}{g_m}.\gamma.\Delta f$$

2.22

Where, K is Boltzmann constant, T is the absolute temperature and g_m is the channel conductance at zero drain-source voltage. The factor γ is a complex function of the basic transistor parameters and bias conditions. The parameter γ has different values in different regions of the transistor: $2/3$ in saturation region, $1/2$ in weak inversion and $1 > \gamma > 2/3$ in triode region.

Thermal noise on capacitors is referred to KTC noise. Thermal noise has a white spectrum and wide band, limited only by the time constant of the switched capacitors or the bandwidth of the operational amplifiers. The total noise power can be found as:

$$v_n^2 = K.T / C \quad 2.23$$

In addition to the drain current noise, the channel also generates noise in the gate through the gate-channel capacitance $C_{ox}WL$. The fluctuating channel potential couples capacitively into the gate terminal, leading to a noisy gate current. This noise is negligible at low frequencies.

Another noise source is the popcorn noise or it is also called burst noise. The most commonly invoked cause is the random trapping and release of charge carriers at thin film interfaces in bulk semiconductor crystal. These charges can have impact on the transistor performance, and the output signal can be substantial.

According to the Carrier Number Fluctuation Theory, the flicker noise is caused by traps and de-traps of charge carriers in the material. Flicker noise, or $1/f$ noise, has been observed in all kinds of devices, from homogeneous metal film resistors and different kinds of resistors to semiconductor devices and even in chemical concentrated cells. People think that there is a fundamental physical mechanism behind $1/f$ noise, because it is well spread over the components. Till now, such a mechanism is not yet found. In the next figure, $1/f$ noise is modeled by a parallel current source.

$$I_d^2 = \frac{KI^a \Delta f}{C_{ox} WLf}$$

2.24

$1/f$ noise dominates the noise spectrum at low frequency. This means that this noise source will be the dominant noise in our design. This is because of the low frequency operation system. For this reason, the whole system is simulated using *pnoise* and transient noise functions in Cadence. By checking the noise sources in our system, the $1/f$ noise was indeed the dominant noise source. That is why the other noise sources are not analyzed anymore.

Noise simulation with *pnoise* function is done using *pac* and *pss* simulation options in Cadence. The output transistors in Figure 2.19 were found to be the main source of $1/f$ noise. The result of the noise simulation of the first scale can be seen in the next figure.

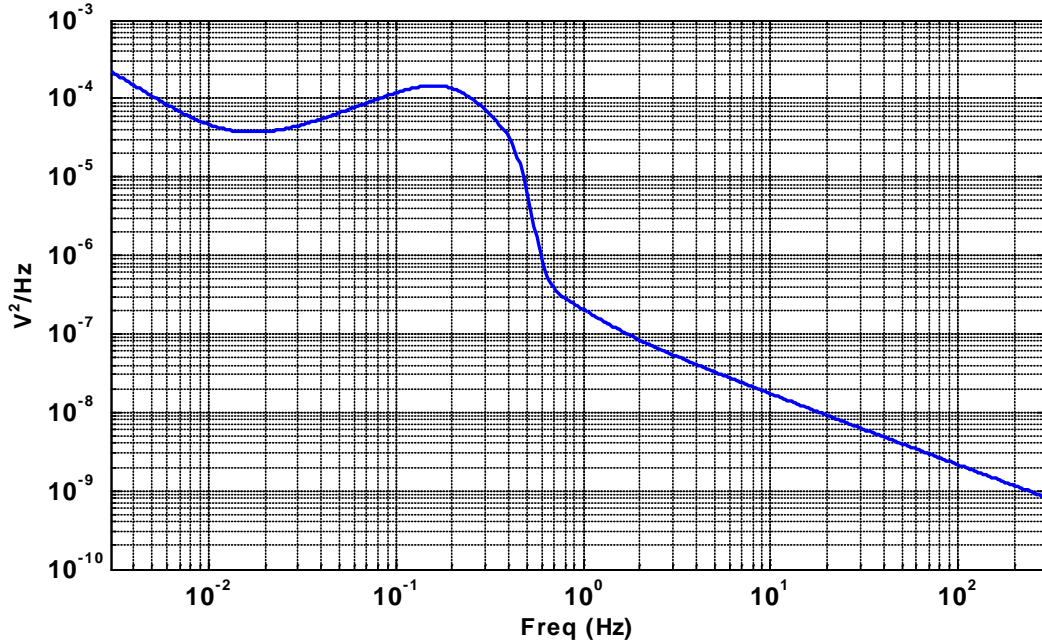


Figure 2.24: $1/f$ noise simulation for the first scale wavelet filter

The y-axis in Figure 2.24 is the power noise spectrum (V^2/Hz) and the x-axis is the frequency (Hz). It can be seen that the noise response shows the $1/f$ noise behavior. The hump in the graph of this figure is occurred at the centre frequency of the wavelet filter. The noise power value of $41.7e^{-6} V^2$ is obtained by integrating the graph in the whole frequency range (from 0 to 300 Hz). This gives a high signal to noise ratio (SNR) of about 24.31 dB, which is calculated using the next equation.

$$SNR = 10 \log_{10} \left(\frac{P_s}{P_n} \right) \quad 2.25$$

P_s is the power of the signal, which can be calculated by taking the square value of the signal's peak over two ($P_s = \frac{\hat{V}_s^2}{2}$), which is 150 mV in this case. P_n is the average power of the noise, which is obtained from Cadence.

The output transistors of the opamp are implemented by multiple transistors in parallel with the same W and L. By increasing W and L of one output transistor in the same ratio and decreasing the multiple number of that transistor, it is possible to get the same surface of the transistors. In addition, the area of one transistor will be increased, and consequently $1/f$ noise will be decreased. The result of the last simulation for the final SNR is given below in Figure 2.25.

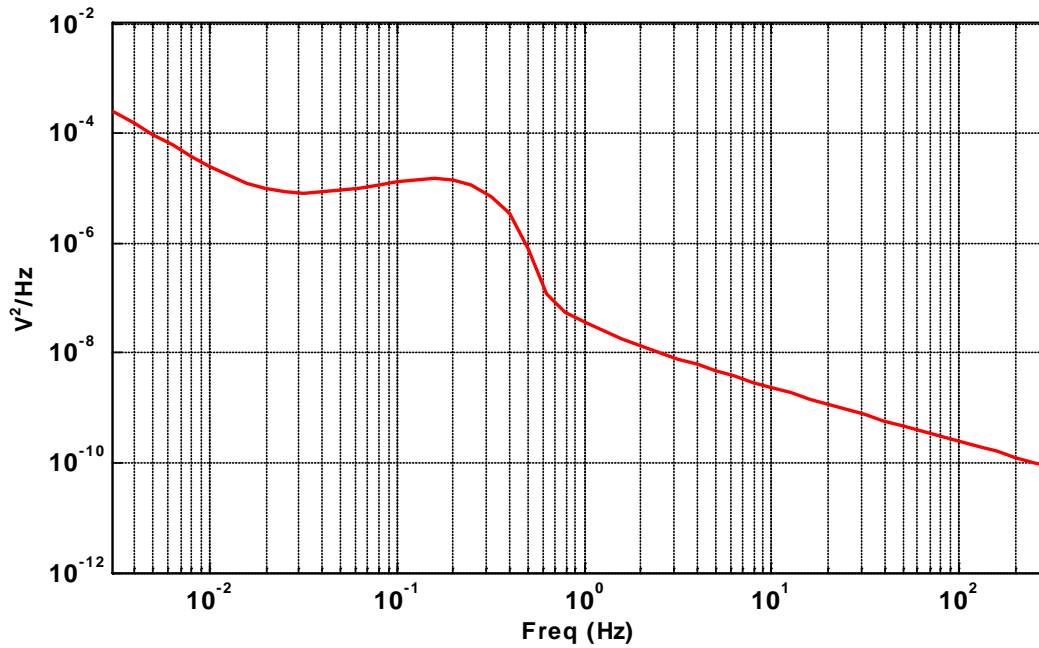


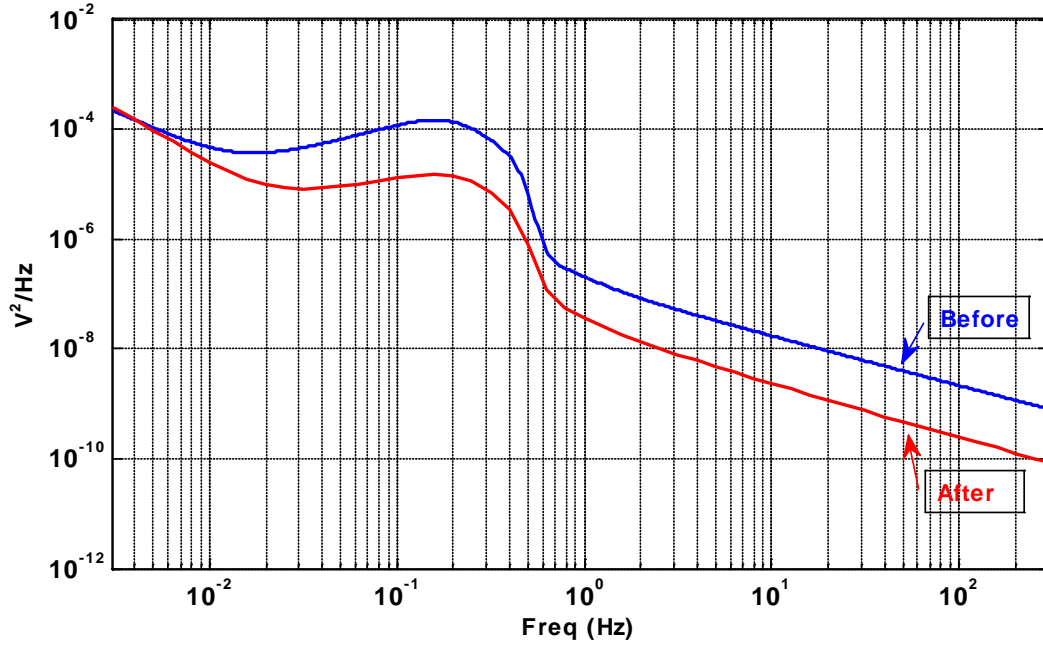
Figure 2.25: $1/f$ noise behavior for minimum noise power

The noise power value is now changed to $7.52e^{-6}V^2$, and consequently the signal to noise ratio is:

$$SNR = 31.75 dB$$

2.26

To compare the results, both simulation results are plotted in one figure as following. These results are from the scale with 250 mHz centre frequency. That is because the last design of the WF [5] is implemented in this centre frequency and our design is based on improvement of that design. In the forth chapter the different WF for all centre frequencies (6 Hz, 12 Hz, 24 Hz, 48 Hz and 96 Hz) are implemented. In that chapter, the noise simulation results and the values of the SNR are also obtained for these centre frequencies.



2.27: 1/f noise behavior for both before and after optimization

In addition, transient noise simulation is done in different value of noise to check the behavior of wavelet filter in presence of noise. These results are added to the appendix, because it was not part of this project but it is useful as a reference.

2.6. Conclusion

The wavelet filter is built by using the SC structure and fully differential folded cascode opamp. The number of switches in the inverting and non-inverting SC for one scale WF is reduced from 120 to 90. The opamp is constructed in fully differential folded cascode form because of its low power consumption and maximum output swing. This design is optimized for clock feed through, charge injection and noise. These are important aspects to reduce the spikes of the impulse response of [5] and increase the SNR. The simulation results of the first scale give a good impulse response as output of the WF when the impulse is used as its input. This means that the wavelet filter functions properly. The next chapter is dedicated to make a detector circuit with ultra low-power design.

3. QRS complex detector

In the last chapter, the wavelet filter was discussed and analyzed in discrete time. Its behavior shows that it can do its job properly by giving the proper impulse response as an output. That means that the wavelet filter is ready to used ECG signal analysis. The QRS complex is an important part of the ECG signal which must be detected and we hope to be able to detect the T-wave of the ECG signal as well. That is why the design of the suitable detector circuit is required. The power consumption and the simplicity of the circuit must be considered, because of the limitation in the area and power of a portable battery. Besides, the circuit must be able to give a binary output for microcontrollers.

3.1. Introduction

The aim of the circuit discussed in this chapter is to detect the peaks of the output signals of the wavelet filter. When the input of the WF is an impulse, the Gauss1 will be obtained. This output has a positive as well as a negative peak. An ultra low power detector circuit is constructed by using one suitable structure which is based on Senad Hiseni design [16]. He worked on “Action potential detector” with single input. As it can be seen in our block diagram (Figure 3.1), we also have differential input and S&H circuit. The block diagram of the QRS complex detector is presented in Figure 3.1.

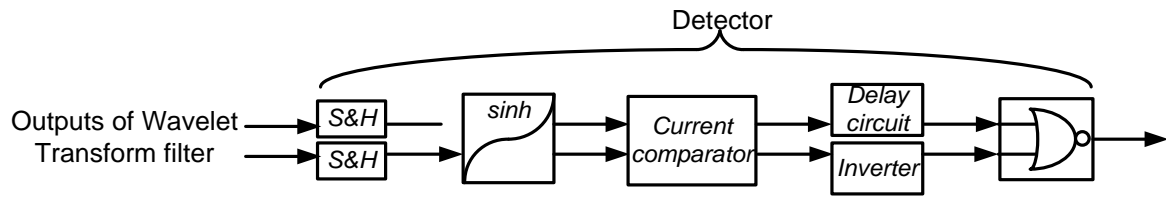


Figure 3.1: Block diagram of the detector circuit

As the WF described in Chapter 2 operates in discrete time, the detector circuit needs to be followed by either a discrete time subsequent circuit. That is why Sample & Hold circuit is used at the input of our detector circuit. The *sinh* transconductor topology is used to extract the peaks of the input signal to reduce the influence of noise, which usually is smaller than the signal (3.2). The current comparator is used to detect the outputs current peaks (3.3). A delay circuit and an inverter are used to overlap and reverse the first peak with the second peak and inverse the second peak to make a low logic peak when the first peak is low, respectively (3.4). Finally, *nor* gate circuit is used to obtain binary output (high) from its two low inputs of delay circuit and inverter (3.5).

3.2. Sinh

The ECG signal includes noise with small peaks. The influence of any small peak which will be added to the output signal must be eliminated. Based on the exponential characteristics of the weak inversion MOSFETs, *sinh* structure can be used. An expanding function (such as the *sinh* transconductor) expands the larger magnitudes of the signal and thereby suppresses the influence of noise, which usually is smaller than the signal. The exponential relationship of MOSFETs operating in weak inversion [16] for $V_{DS} > 4U_T$ (a condition to keep the devices in weak inversion) and $V_{SB} = 0$ (source and body terminals are connected), is given by:

$$I_D = I_{D0} \exp\left(\frac{V_{SG}}{nU_T}\right) \quad 3.1$$

where, I_D is the drain current, and I_{D0} is given by the equation below:

$$I_{D0} = I_s \left(\frac{W}{L}\right) \quad 3.2$$

where, I_s is the zero bias current for a unit transistor, n is the sub-threshold slope factor and U_T is the thermal voltage while W , L , V_{SD} , V_{SB} and V_{SG} have their usual meaning. By looking at the next figure and writing the KVL for the loop a , we can have:

$$V_{SG2} = V_{SG1} + V_{in} \quad 3.3$$

The next equation will be obtained by substituting (3.3) into (3.1).

$$I_x = I_o \exp\left(\frac{V_{in}}{nU_T}\right) \quad 3.4$$

Which clearly states the exponential relation between input voltage and output current depending on bias current I_o , which is set by the voltage V_o .

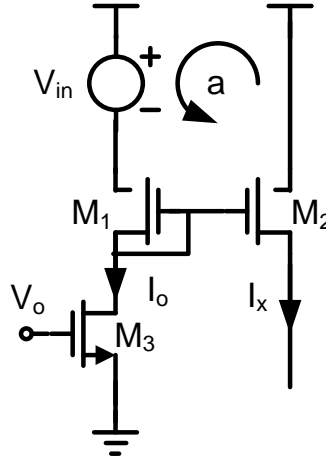


Figure 3.2: Simple pre-processor performing mathematical exponential operation

The *sinh* circuit is formed by a dual output current amplifier which is biased by a controlled current generated from a current splitter. Both the amplifier and splitter circuits can be realized from the same basic circuit block, called *Sinh* transconductor [15]. This multiplier circuit is designed in 0.13 μm CMOS technology. The voltage bias is 1 V. By using 10nA as the bias current, output currents with amplitudes of 530 nA can be applied to the circuit and a good multiplier is performed. The structure of the *sinh* transconductor is shown in next figure.

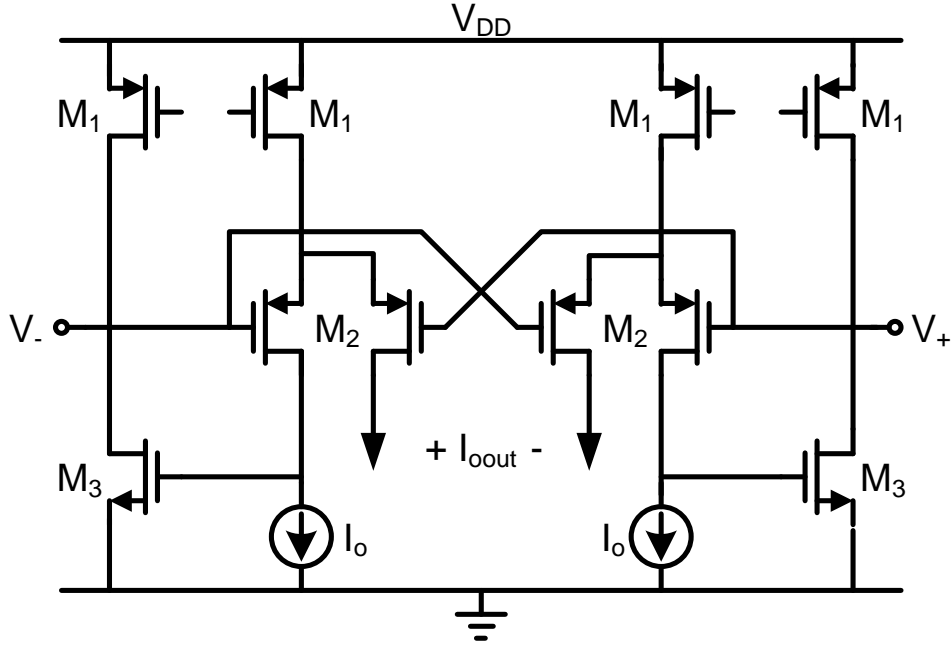


Figure 3.3: *Sinh* transconductor structure

In this figure, I_o is the biasing current and V_- and V_+ are the differential input signals. This circuit can be designed to process high input signal amplitudes while its bias current is kept low. Using the exponential relationship of MOSFETs operating in weak inversion, the input–output relation of transconductor is given as:

$$I_{out} = 2I_o \sinh\left(\frac{V_+ - V_-}{nV_T}\right) \quad 3.5$$

where n is the sub-threshold slope factor and V_T is the thermal voltage. This relationship provides *sinh* transconductor and the DC response of this circuit shows this behavior as follows:

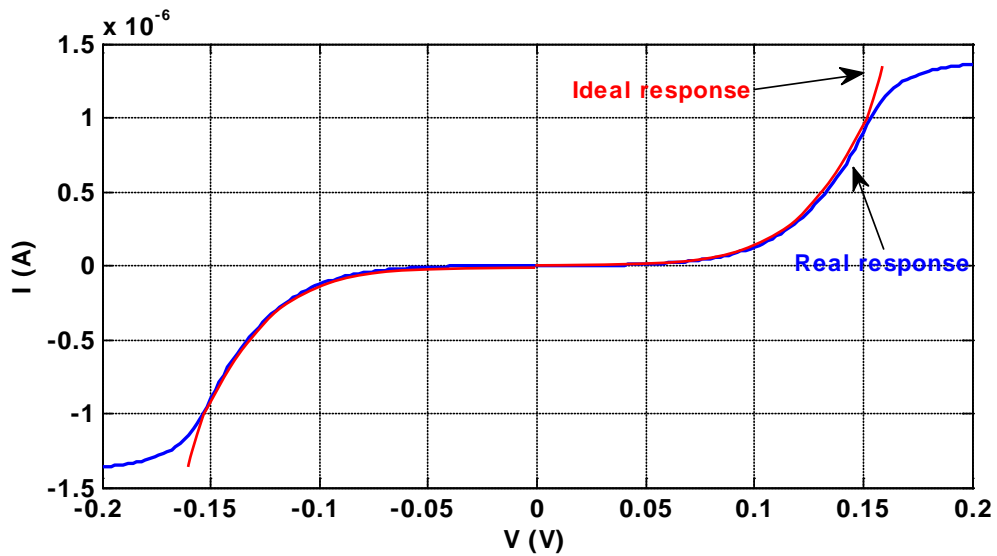


Figure 3.4: DC response of the *sinh* transconductor

The circuit response is overlapped with the ideal result in Figure 3.4. It can be seen that the circuit result is clipping at a certain current. That is because the transistors go into the saturation. The outputs current of this circuit ($\pm I_{out}$) are obtained with the transient analysis in Cadence as follows.

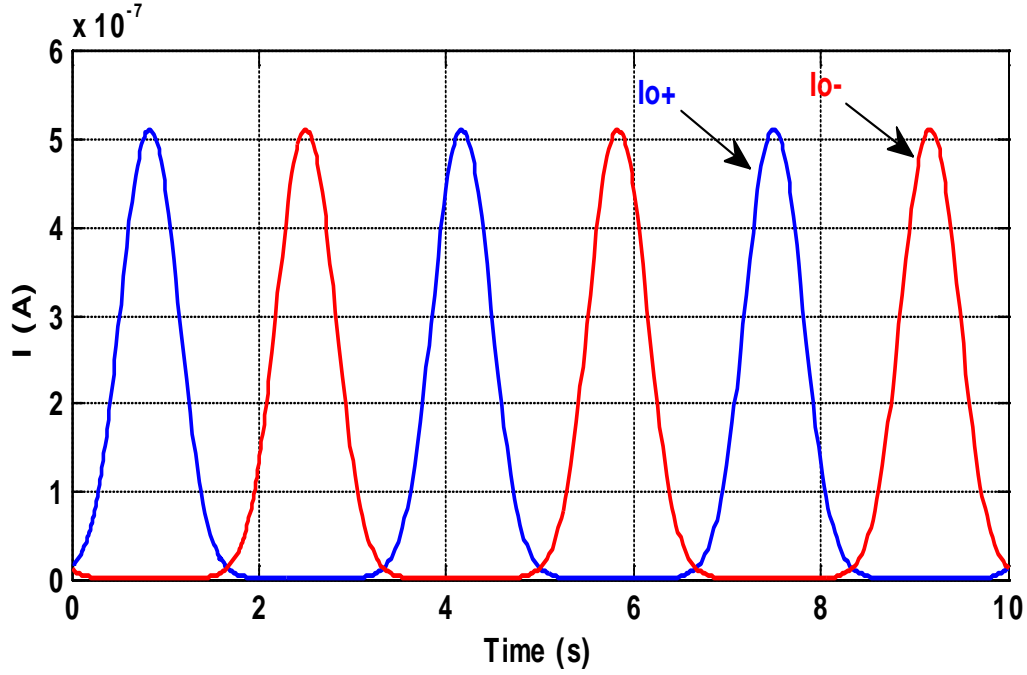


Figure 3.5: Current outputs (I_{o+}, I_{o-}) of the *sinh* transconductor

The input signal is *sin* wave with amplitude the same as the amplitude of the WF output. The frequency of the *sin* wave is 200 mHz, which is the frequency of the WF output in chapter two. This input signal is chosen because every period of this signal looks more or less like the impulse response of the WF. The peaks in Figure 3.3 can be detected by using a current mirror circuit. We can compare the output currents with a bias current of the current mirror circuit and implement V_n and V_p . This is briefly explained in the next section.

3.3. Current mirror for V_n and V_p

By adding a current mirror structure, the current comparator circuit can be made for the output currents ($\pm I_{out}$) at the points X and Y in Figure 3.4. This will detect the peaks of the outputs current. For an example we can look at point Y in this figure. When $I_{THn} > I_x$, V_n will become 0V. Otherwise it will reach the maximum voltage. In this way, we can obtain V_n and V_p . The bias current of the current mirror can be tuned to detect different peaks of the inputs signal. That is useful when we use the ECG signal as input signal of our system. Because we can define this bias current to detect smaller peaks such as the T-wave. This current mirror circuit can be seen in Figure 3.6.

3.4. Delay circuit

The delay circuit is implemented with a bias current (I_{dchrg}), capacitor C and the voltage bias V_{chrg} as shown in Figure 3.8, to overlap the first peak with the second peak. The first peak comes from the $+I_{out}$ and the second peaks comes from the $-I_{out}$. Transistor M_9 acts as a switch. If $V_n=0V$, this transistor will be ON and the discharge current will be:

$$I_{dchrg} = c \frac{dV_{nDEL}}{dt} \quad 3.6$$

By rewriting this equation, the discharging slope can be found as follow.

$$\frac{dV_{nDEL}}{dt} = \frac{I_{dchrg}}{c} \quad 3.7$$

When $V_n=V_{DD}$, transistor M_9 will be OFF and the capacitor will be charged. The charging slope equation will be:

$$\frac{dV_{nLPF}}{dt} = \frac{I_{chrg} - I_{dchrg}}{c} \quad 3.8$$

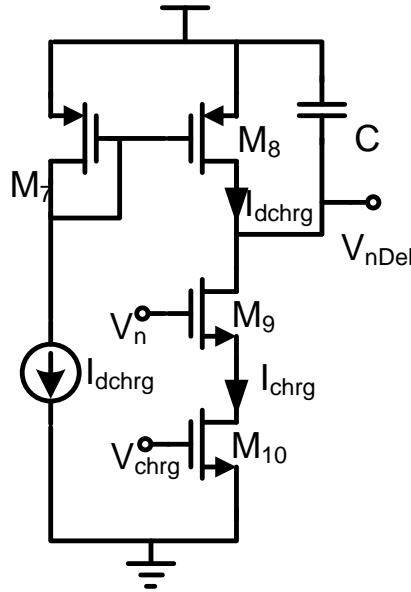


Figure 3.8: Implementation of a Delay circuit

The threshold voltage of transistor M_9 and the discharge slope determine the delay time. In the next figure, signal V_n and V_{nDel} is given. For the second peak, the inverter is added to inverse the logic output from V_p . This is necessary, because the first peak is already inversed by the delay circuit. The simple inverter circuit is implemented in Figure 3.10.

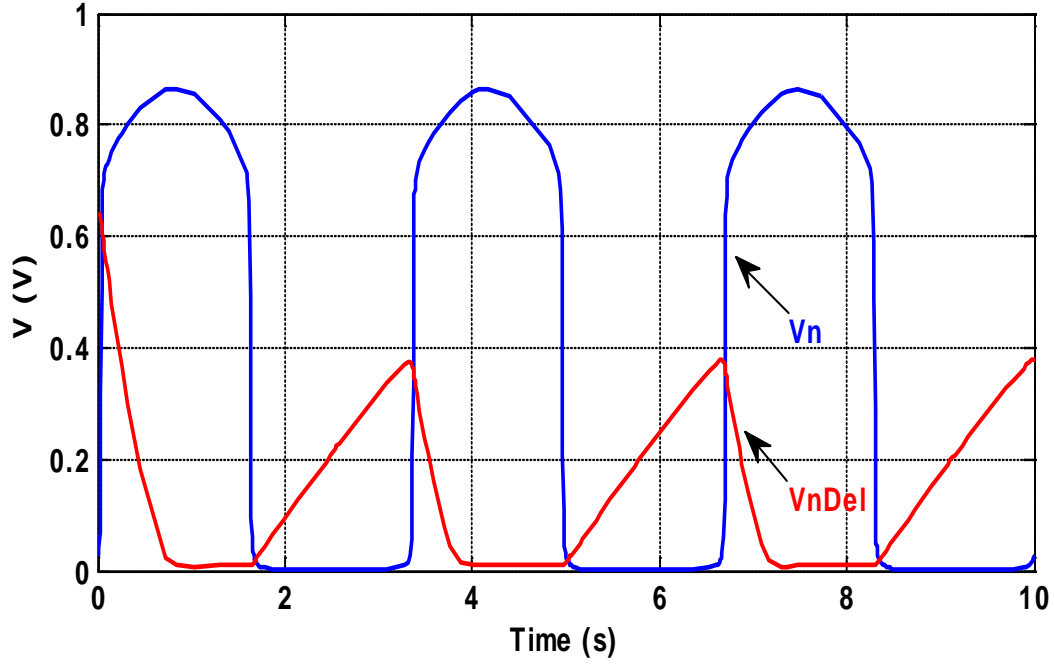


Figure 3.9: V_n and V_{nDel} signals

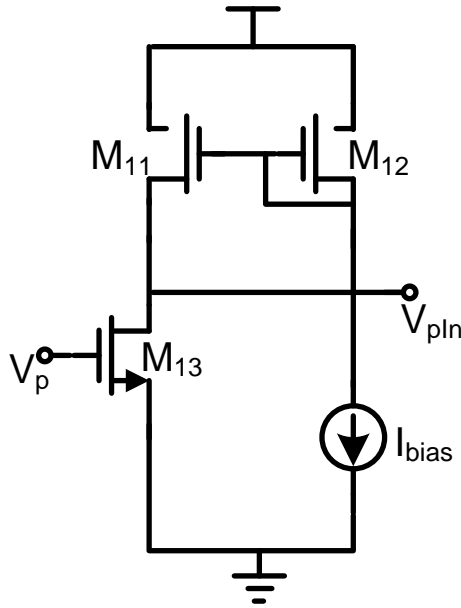


Figure 3.10: A simple inverter circuit

The outputs V_{pln} and V_{nDel} now have low logic values at the same time. This means that it can make two overlapping low logic outputs V_{pln} and V_{nDel} from the two non-overlapping high logic outputs V_n and V_p . This can be seen in next figure, which is obtained by using the transient analysis in Cadence. This is enough to use the *nor*-gate circuit as a comparator circuit.

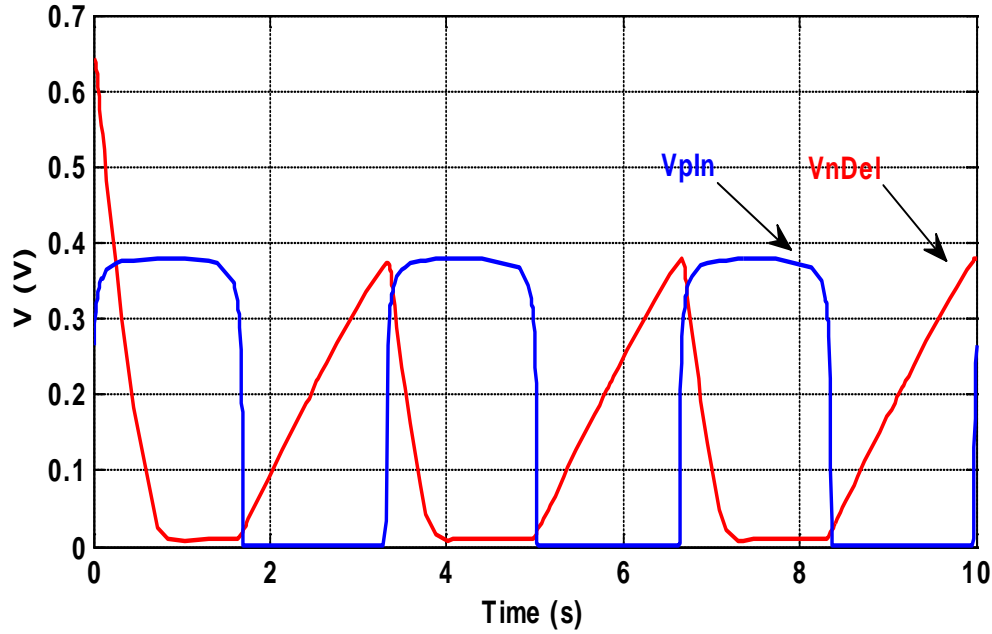


Figure 3.11: V_{pLn} and V_{nDel} signals

3.5. Nor-gate

The *nor*-gate is a binary logic gate that implements a logical NOR. It behaves according to the truth table below. A HIGH output (1) results if both the inputs to the gate are LOW (0). If one or both inputs are HIGH (1), the output will be LOW (0). This is useful for our design, because both V_{nDel} and V_{pLn} are low when the peaks of the input signals exist.

Table 3.1: Truth table of *nor*

Input		Output
A	B	$A \text{ nor } B$
0	0	1
0	1	0
1	0	0
1	1	0

By looking at the table above, we expected that *nor*-gate circuit, is able to give a binary output when the input peaks exist. A *nor*-gate structure can be seen in the Figure 3.12.

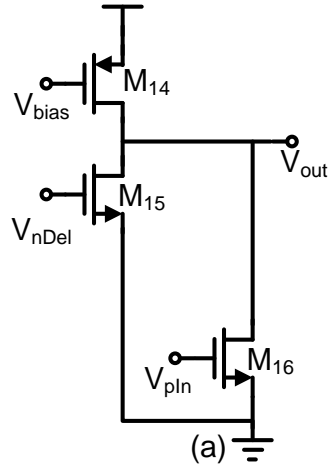


Figure 3.12: The nor-gate circuit

This structure is used, because we need a binary output for a microcontroller. Moreover, the output is high, if both V_{nDEL} and V_{pIn} are low and subsequently the transistors are off. As a result, V_{out} will be the same as V_{DD} . In this way the output of the WF will be detected. This means that with the two positive and the negative peaks of the impulse response, one binary output will be obtained. This circuit is based on the design of Senad Hiseni [16].

All pieces of the detector circuit which are discussed above are connected together as shown below to make a whole design. This circuit has another modification to follow the WF structure and prevent the unwanted spikes through the circuit. This part is a Sample and Hold circuit, which is discussed in the next section.

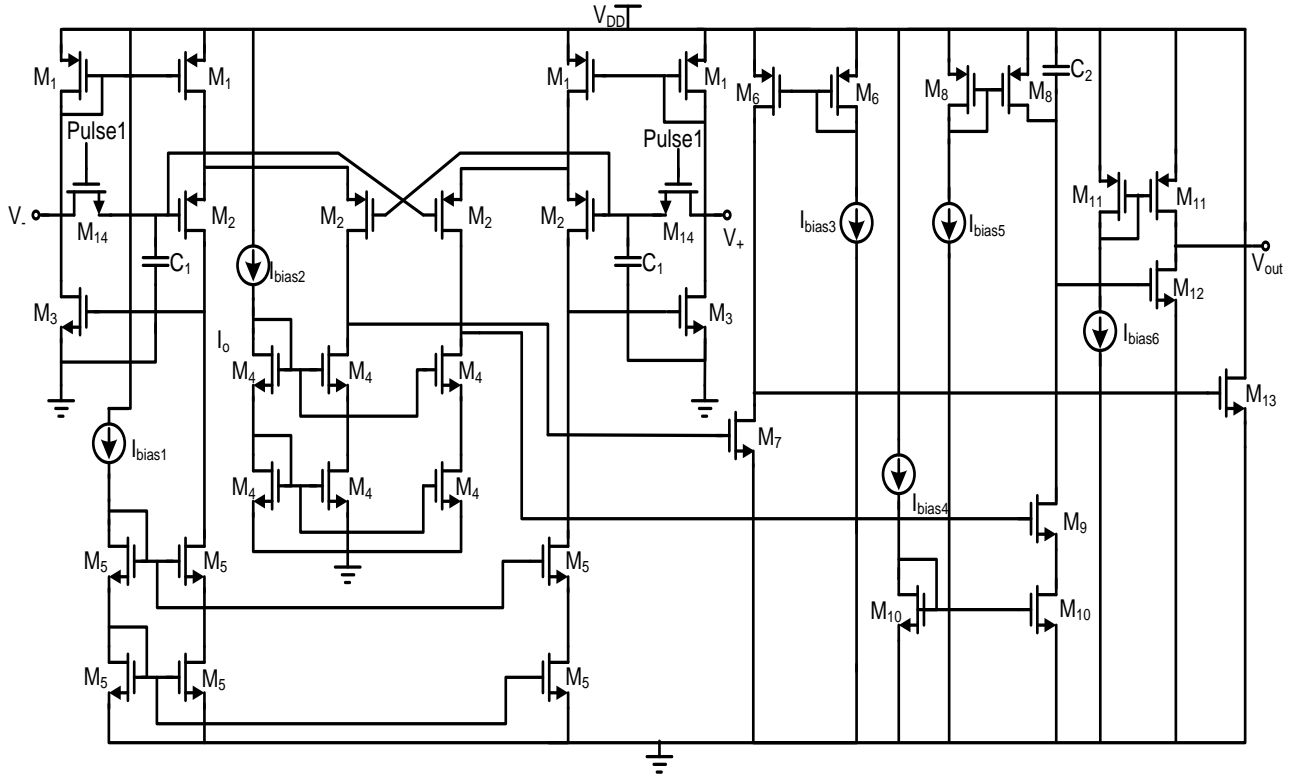


Figure 3.13: Complete detector circuit

3.6. Sample & hold

At the input of this circuit, a sample and hold circuit is used. The switches take the right samples of the inputs and the capacitors hold these values after the sample mode. In this way, we can sample parts of the input signal that does not include spikes. This means that the rest of the spikes that exist in the outputs of the WF cannot go through the detector.

The capacitor C_1 is used for hold mode and its value is obtained by trial and error. The switches drive with the same as the pulse generator of the WF. The only difference is that these pulses have no delay part at the start point. However the pulses of the WF have delay time at their start points (see Figure 2.5). That is because we can sample the input signal before any spikes occurs. This is because, as discussed in chapter two, the outputs of the WF include some spikes.

3.7. Simulation result

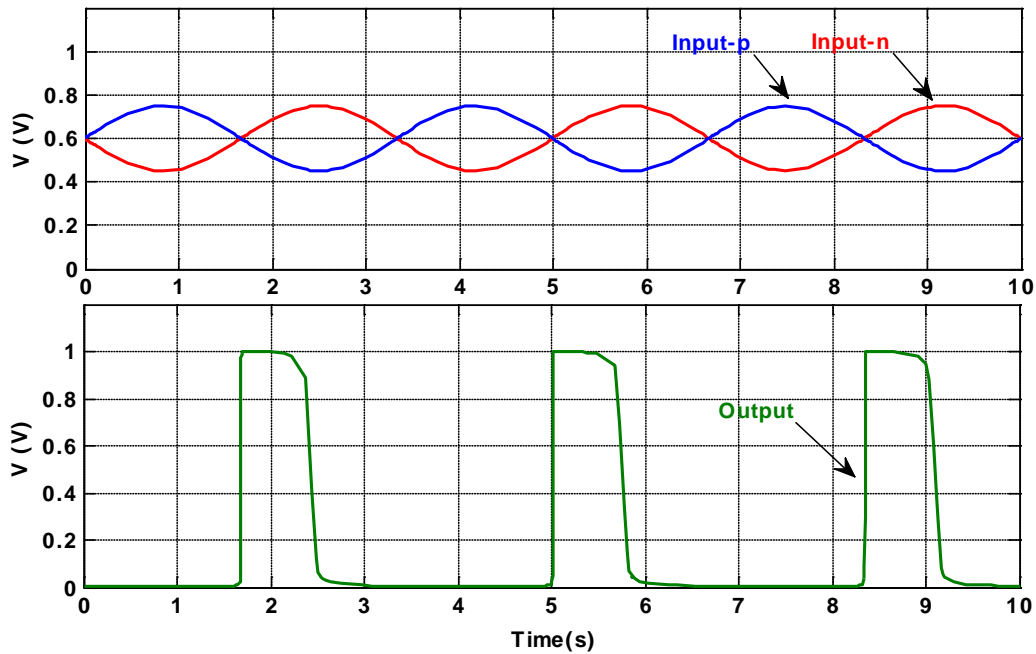
The detector is simulated in Cadence using RF spectre and 0.13 μm CMOS model parameters. Transistor widths (W) and lengths (L) are given in Table 3.2. $V_{DD}=1V$ and $I_o=10\text{ nA}$. The output of the detector must be a binary pulse. This means that the detector must give a digital output when the peaks of the WF outputs occur. The detector will give a binary output only if the negative peak is detected within a short period of time after the positive peak is detected.

Table 3.2: Transistor dimensions

MOSFET	M ₁	M ₂	M ₃	M ₄	M ₅	M ₆	M ₇	M ₈	M ₉	M ₁₀	M ₁₁	M ₁₂	M ₁₃	M ₁₄
W/L ($\mu\text{m}/\mu\text{m}$)	1/1	1/1	1/20	1/1	1/1	1/1	1/1	1/1	1/10	1/1	1/1	1/1	1/1	1/1

First, we will simulate the circuit with a *sin* wave as input, which looks more or less like an impulse response of the WF. The amplitude and the frequency of this input signal is chosen the same as the output of the WF, which is Gaus1 when its input is an impulse.

For the next circuit simulation, the sources are changed step by step with the real one, which are the current mirror structure. The complete design can be seen in Figure 3.13. The next result in Figure 3.14 is the output of the detector with *sin* waves as inputs.

**Figure 3.14:** Output result of the real detector with ideal inputs

This figure shows that the output pulse will be obtained when both the positive and negative peaks of the inputs occur. This result fulfils the expectation of our design because of the binary output from the peaks of the *sin* wave as an input. The last simulation part is to check the result when the input signals are the outputs of the WF. These outputs are Gause1 because its input is an impulse.

The simulation results by using transient analysis in Cadence are given in Figure 3.16 by implementing the complete first scale in the next figure.

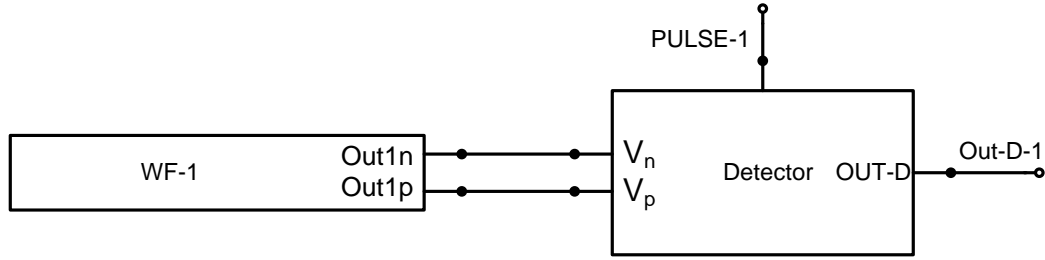


Figure 3.15: Complete first scale with wavelet filter and detector

The simulation result is obtained by using transient analysis in Cadence. To make sure that the detector can detect successive impulse responses, the transient signal is done for two impulse responses from the wavelet filter. In the next figure, the inputs and the output of the detector circuit are given.

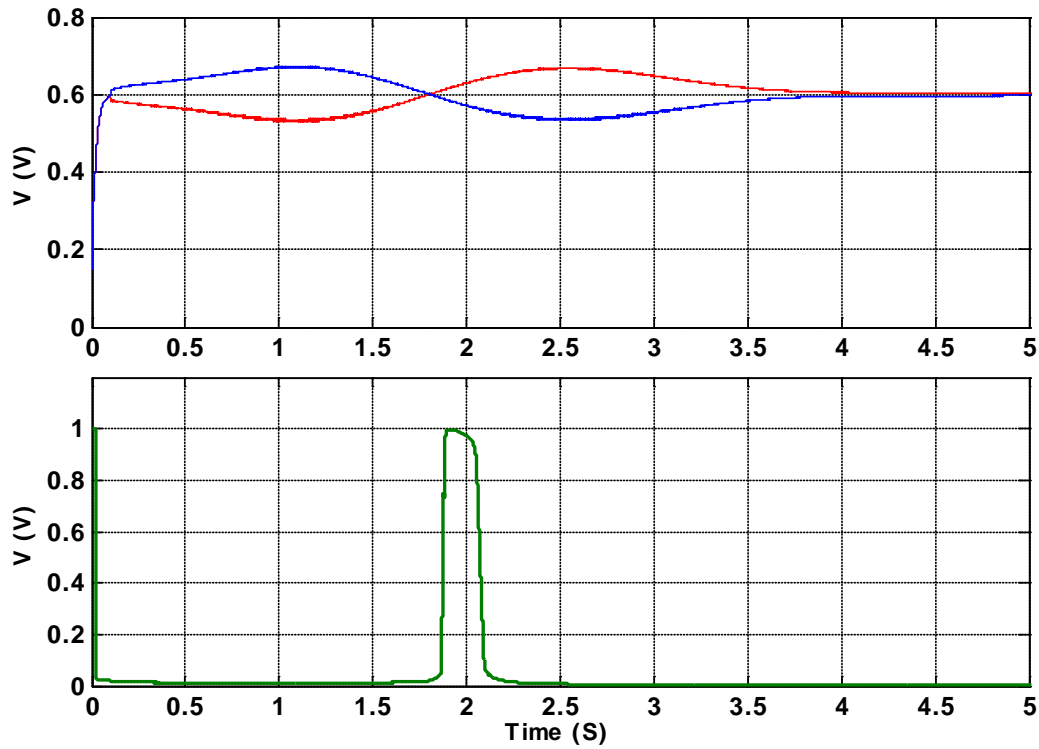


Figure 3.16: Output result of the real first scale

In this figure, the output of WF (top) is used as input of the detector and the output of the detector (below) is obtained. This result can be compared with the ideal output in Figure 3.14. It can be seen that they are almost the same and it shows that the detector works properly. The digital output is performed as expected. It means that the peaks of the impulse response can be detected in an easy way using very low power consumption circuit. The power consumption of this circuit is only 167.6nW.

3.8. Noise test

The noise analysis of the detector circuit is done by using pnoise and pss functions in Cadence. The structure of the detector circuit is the same for different scales and as mentioned before different scales are implemented with different clock frequencies. This means, that the noise behavior of one detector circuit with the lowest frequency will be enough to analyze. The lowest frequency is chosen because the higher the operating frequency is, the lower the flicker noise will be. So, the noise analysis is done for one scale. This circuit works in low frequency domain and we expect that $1/f$ noise will be a dominant noise source, as in the WF circuit.

The outputs of the WF are used as inputs of the detector circuit and the pnoise and pss analyses are used to find the noise sources. By doing the simulation and checking the dominant noise sources with “Noise summary” function, $1/f$ noise is seen to play the biggest role. In the next figure, simulation result can be seen.

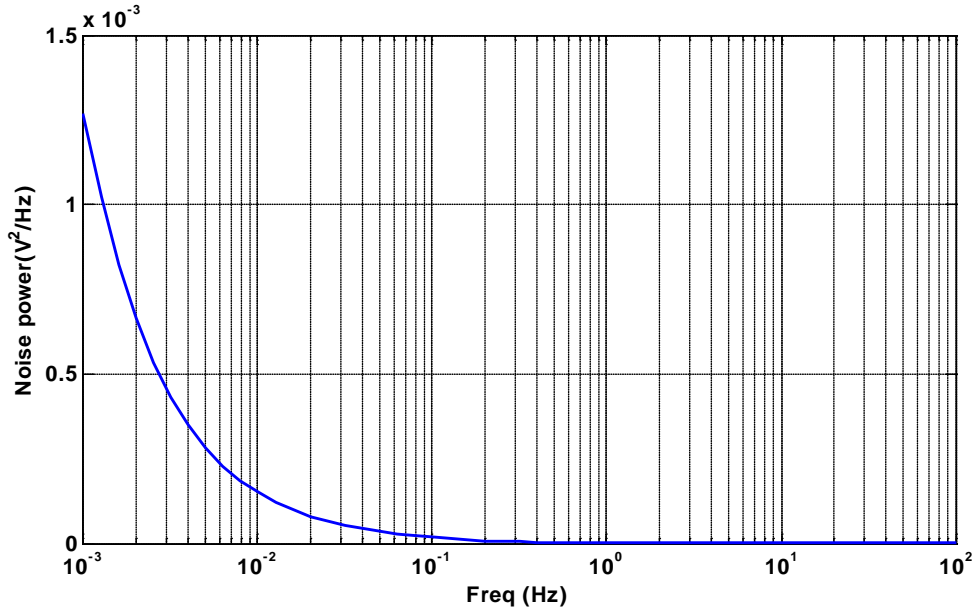


Figure 3.17: Output noise of the detector circuit

By using “intg” function in the Calculator of Cadence and integrating the graph in the figure above over whole frequency range, the value of the noise power is $1.098e^{-5} V^2$. The $1/f$ noise sources can be optimized by checking “Noise summary” function in Cadence. The transistors M10 in Figure 3.11 causes the maximum $1/f$ noise. To decrease the influence of these transistors, their area can be increased. These transistors are the load transistors and that is why they cause the $1/f$ noise in our circuit. By increasing their area, the noise power value is decrease to $0.0178e^{-5} V^2$. This value is much smaller than the noise power in the WF and it can be neglected.

3.9. Conclusion

Design of the suitable detector circuit was the aim of this chapter. The detector is based on *sinh* transconductor, current comparator, delay circuit and *nor*-gate. All these parts are implemented to detect the peaks of the impulse response of the WF. This circuit uses power consumption of about 167.6nW and also has low noise behavior. Simulation results show that the detector will give the binary output only if the negative peak is detected within a short period of time after the positive peak is detected. This circuit works properly, and to keep the simplicity of our design, this circuit will be

used for all scales in the next chapter. The whole design will be implemented and simulated in chapter 4 when the ECG signal is used as an input of WF.

4. Multiple scale wavelet QRS detector

One scale of our system is designed in the previous chapters for the lowest centre frequency of the heart signal (6Hz). The idea is now to implement the other scales for the different resolution of the heart signal looking at the different frequencies. In this way we expect to be able to extract the information about the QRS complex and T-wave as binary outputs from the ECG signal. There are several ways to do that. One of them is to use different clock frequency components and the other one is changing the capacitors C_f and C_s ratio, which are explained in the next section.

In section 4.2, the wavelet filter bank is implemented with its simulation results. The detector bank simulation results are obtained in section 4.3. An external ECG signal is used as input of the wavelet filter to get the binary code for microcontrollers at the end of this chapter.

4.1. Design of different scales

The basic block diagram of the wavelet filter bank can be seen in Figure 4.1. As described before, the wavelet filter is situated at the input of the system before the ADC. WF implements an approximation to Gaus1 wavelet transform (WT) on one scale. The complete filter is constructed by multiple scales in parallel in order to compute the WT in real time. The wavelet filter is made by using the fully differential opamp in discrete time with SC structure and SC-CMFB structure. The next part after the WF is the detector circuit which is constructed by using the *sinh* transconductor circuit, current comparator, delay circuit and the *nor*-gate circuit. The pulse generator is also used to drive the switches in wavelet filters and the detectors. The output must be a logical pulse of every single QRS complex and we will try to get information about the T-wave as well. The WT system is given by:

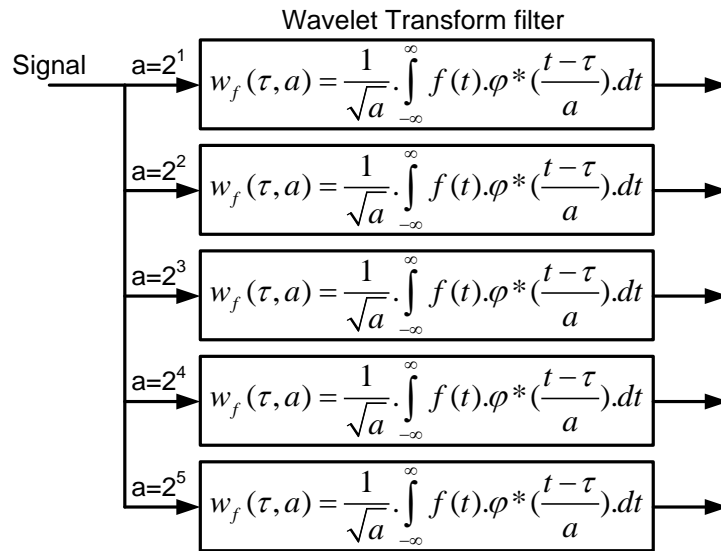


Figure 4.1: WT system with multiple scales

The wavelet filter bank has the five scales. The idea of the wavelet transform (WT) is to look at the signal in different windows and analyze it with different resolutions. By checking equation 1.1 which is the wavelet transform of a function $f(t)$ at scale a it can be seen how every scale can zoom in a specific frequency.

Different scales are represented in Figure 4.1. The first scale is the wavelet transform when $a=2^1$. This means that this scale will zoom in the highest frequency (96 Hz). The last scale has scale a equal to 2^5 and it zooms in the lowest frequency (6 Hz). These frequencies are the centre frequencies of the scales. Besides, there are several options to implement these scales. By looking at the time constant equation (4.1) of the SC integrator, it can be seen that the value of the capacitors or the clock frequency can change.

$$T = \frac{C_f}{C_s \cdot f_{clk}} \quad 4.1$$

where, C_f is the feedback capacitor, C_s is the switch capacitor and f_{clk} is the clock frequency.

In our design, minimum values of the capacitors are chosen to save the area. That is why C_f and C_s did not change. In addition, by making C_f smaller, the noise plays a bigger role. That is the challenge when choosing the capacitors values. These steps give us enough reasons to choose f_{clk} for implementing the different scales. This means that all scales have the same structure. This improves the simplicity of our design. The relationship between the scale and the clock frequency is:

$$a \propto \frac{1}{f_{clk}} \quad 4.2$$

By multiplying the clock frequency of the lowest scale with two, half of the scale (a) will be obtained. In this way every scale has 2 times higher frequency than its previous scale. This means that the 2nd ($a=4$), 3th ($a=8$), 4th ($a=16$) and 5th ($a=32$) scales have 4.8 kHz, 2.4 kHz, 1.2 kHz and 600Hz clock frequencies, respectively. The filter bank is constructed and the transient analysis will be used to get the simulation results.

4.2. Results of the wavelet filter bank

By simulating the whole system and running the transient analysis in Cadence, the different resolutions are obtained as can be seen in Figure 4.2. We are interested in different centre frequencies to cover the whole frequency range of the ECG signal (0.05 to 150 Hz). These frequencies are 6 Hz, 12 Hz, 24 Hz, 48 Hz and 96 Hz, which are the values for all five scales.

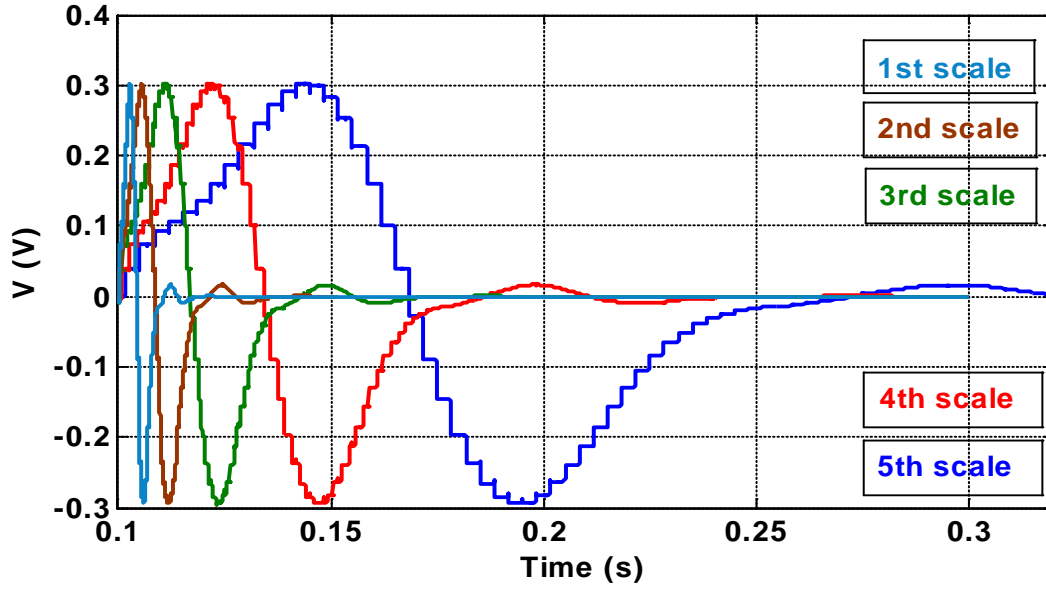


Figure 4.2: The impulse responses of the 1st, 2nd, 3rd, 4th and 5th scales for the differential outputs

In Figure 4.2, it can be seen that all outputs of the wavelet filters give very smooth impulse responses in the form of Gauss1. These results are differential outputs of all scales when an impulse is used as input of WF. The single-ended outputs are pasted in the next figure. This is, because the detector that we will use after the WF, has differential input.

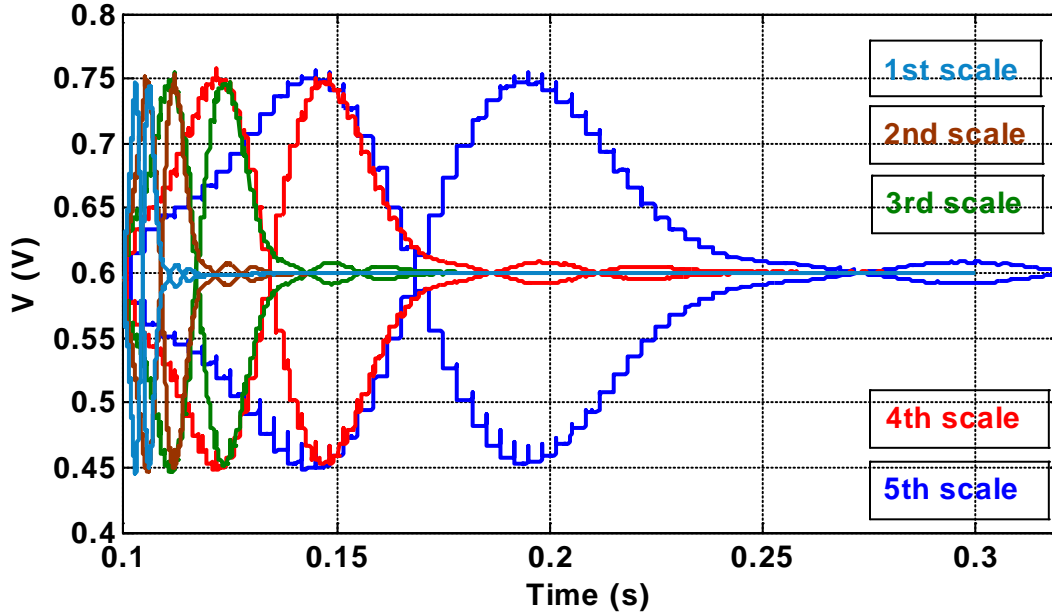


Figure 4.3: The single impulse responses of the wavelet filter bank

The *ac* responses of the every WF are obtained and plotted in one figure to check that our system is able to filter all centre frequencies. These results are implemented in Figure 4.4.

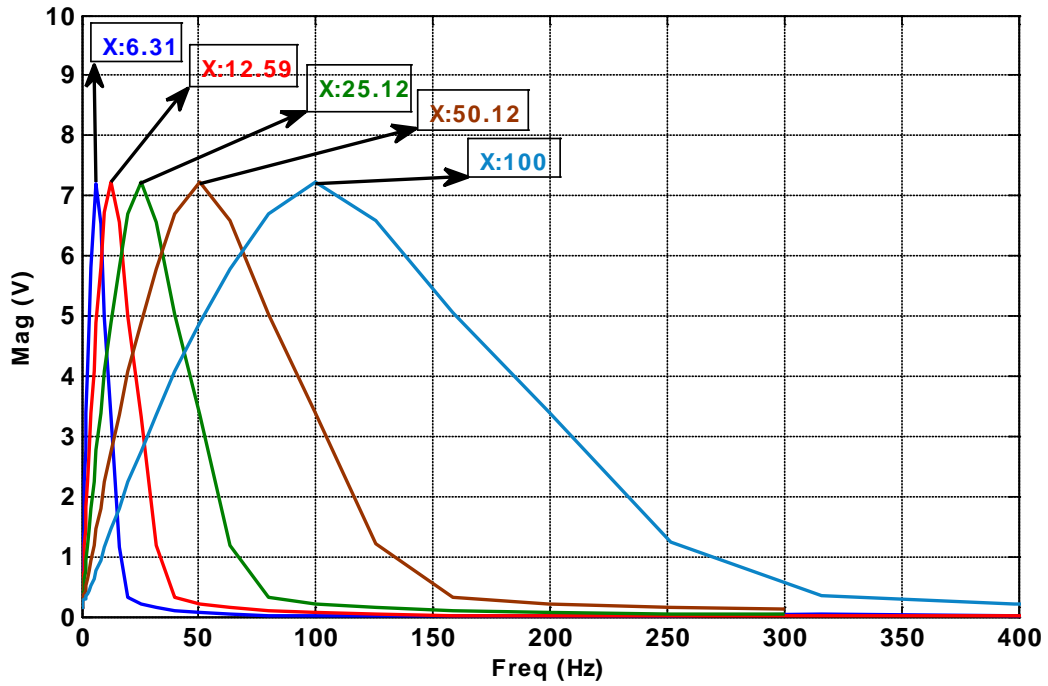


Figure 4.4: The *ac* responses of the WF bank

By checking the peaks of every graph in Figure 4.4, we can see that the WF bank is able to cover all frequency range (0.05 to 150 Hz) of the ECG signal. The simulation result gives the centre frequencies with 4% error, which comes from the parasitic capacitance. The all clock frequency components with desire centre frequencies and actual centre frequencies are given in Table 4.1.

Table 4.1: Frequency response and clock frequency value of the wavelet system

Scale	Clock frequency (KHz)	Desire Centre freq (Hz)	Actual Centre freq (Hz)
2^1	4.8	96	100
2^2	2.4	48	50.12
2^3	1.2	24	25.12
2^4	0.6	12	12.59
2^5	0.3	6	6.31

In chapter 2 and 3, we calculated the power consumption of the WF and the detector circuit. The total power consumption for the whole system will be five times the power consumption of one scale, because we have five scales. The total capacitance for the whole system is also five times the capacitance in one scale. The power consumption in one scale is 600 nW and the total capacitance is 43.25 pF. This gives the value of the total power consumption of about 3 μ W and the total capacitance of about 216.25 pF. The noise is not the same in every scale because of the frequency variation, which has influence in noise. The noise results are discussed in the next subsection.

4.2.1. Noise simulation results

For the last scale with lowest frequency, the noise simulation is performed and the value of the optimum SNR is obtained. In this part, the other scales are simulated and we expect that by increasing the frequency, $1/f$ noise will decrease. All simulation results of the 1st, 2nd, 3rd, 4th and 5th scales are presented in Figure 4.3 (a), (b), (c), (d) and (e), respectively.

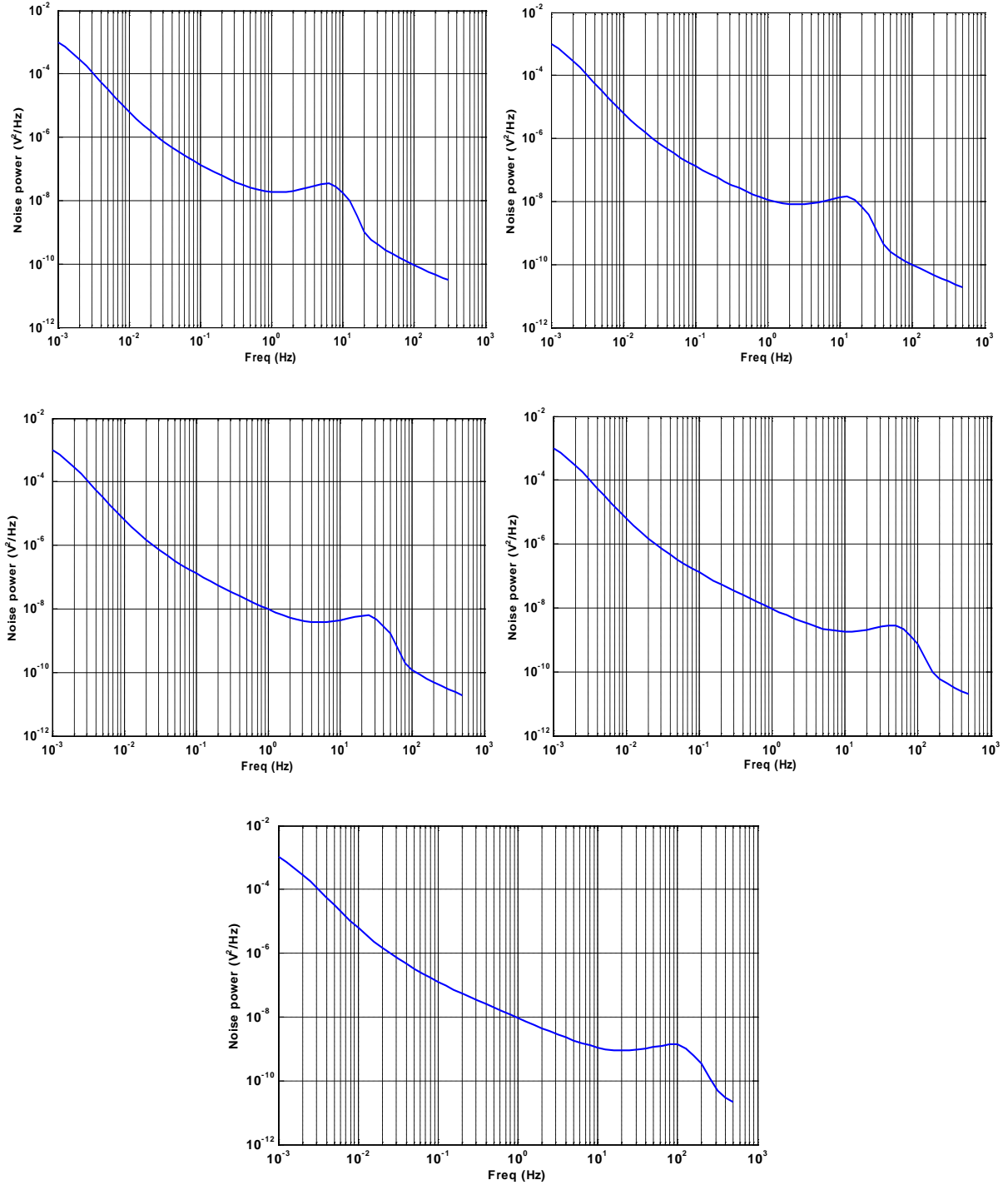


Figure 4.5: $1/f$ noise simulation for the 1st, 2nd, 3rd, 4th and 5th scales

These $1/f$ noise behavior results are obtained using pnoise and pss function in Cadence. Every graph has a hump at the centre frequency of the WF. That is because the WF is a low pass filter (LPF). For all these scales, the noise power and the SNR are calculated and presented in the next table.

Table 4.2: The power noise and the SNR for all scales

Scale	Power noise (V^2)	SNR (dB)
2^1	$2.298 \cdot 10^{-6}$	36.9
2^2	$2.318 \cdot 10^{-6}$	36.86
2^3	$2.33 \cdot 10^{-6}$	36.83
2^4	$2.366 \cdot 10^{-6}$	36.77
2^5	$2.431 \cdot 10^{-6}$	36.64

The specifications of the WF bank are obtained and the different wavelet filters are ready to use for the detector circuit. In the next step, the detector circuit will be simulated for five different WF. We expect to get binary outputs from the detectors when their inputs are the impulse responses of the wavelet filters.

4.3. Results of the detector bank

In the third chapter, the result of one detector circuit is discussed. The results of the other scales are the same, because the same circuit is used for different scales. In this section, the detector circuit will be used after the every wavelet filter to complete the whole system. The detector circuit in Figure 3.11 is connected to the wavelet filter and the whole block diagram of our design is constructed as shown in Figure 4.6.

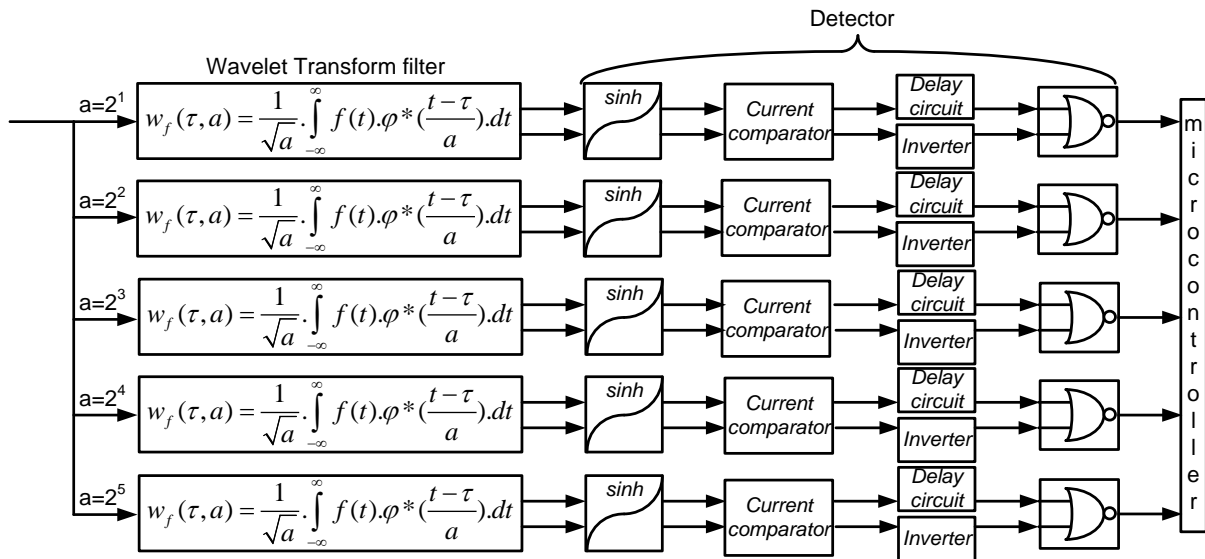


Figure 4.6: The block diagram of the whole system

The transient analysis in Cadence is used to get the results of the whole system. As mentioned before, the pulse generator is implemented for different clock frequencies. The ideal pulse generator is implemented with the voltage sources for all different phases. In the next figure, the clock pulse of every scale is plotted.

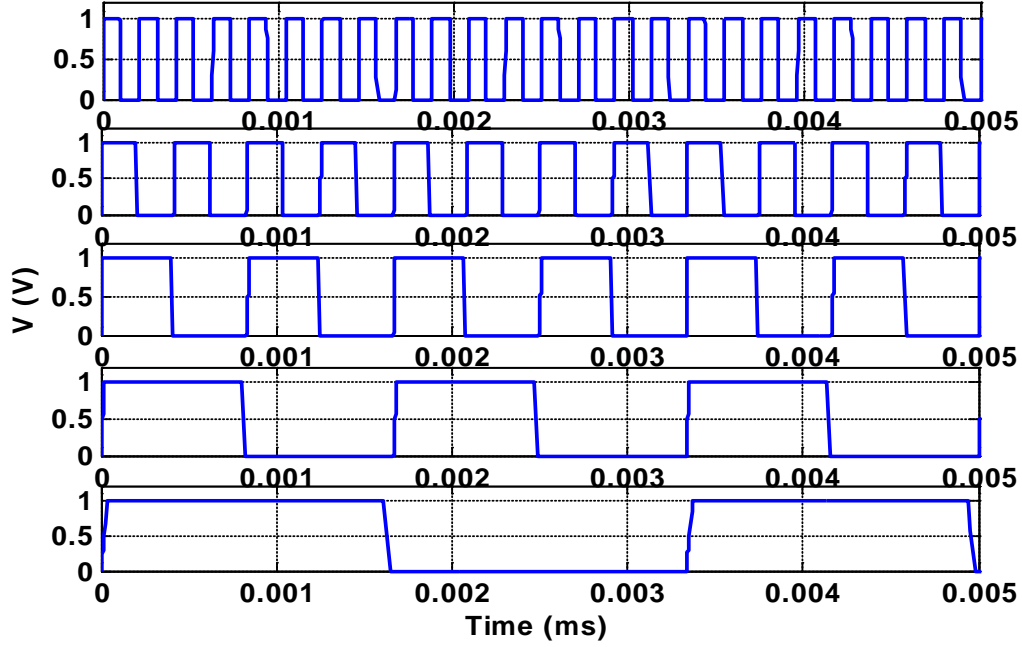


Figure 4.7: The clock pulses for 1st, 2nd, 3rd, 4th, 5th scales

By adding the pulse generator to the system, which can be seen in Figure 4.8, the transient simulation is performed. We will obtain the five binary outputs from all scales. The result of the simulation is given in Figure 4.8, which is the total result of our design.

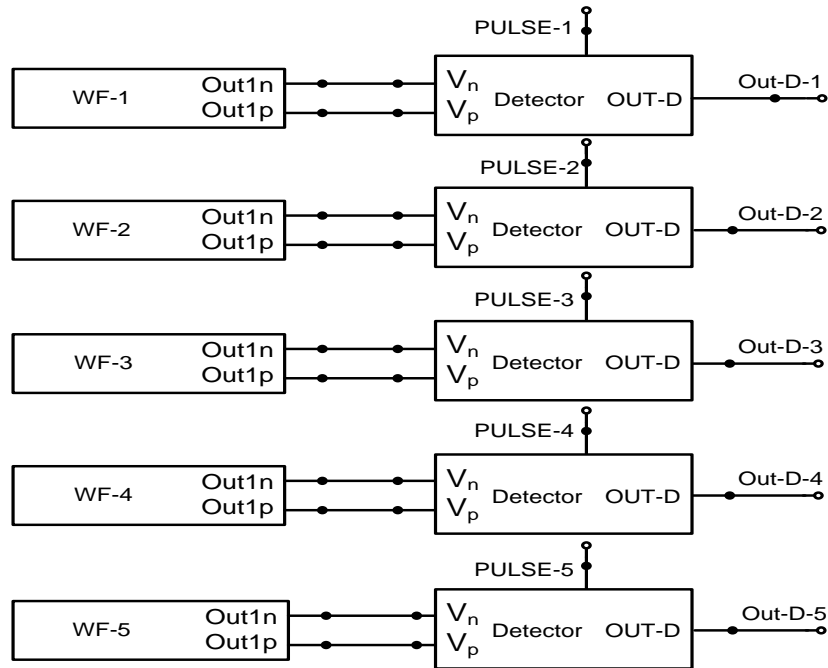


Figure 4.8: The whole system

Figure 4.9 gives the digital output of every impulse response of the wavelet filters. This means that every QRS complex of the heart signal can be detected as a binary output with different resolutions. Here, as mentioned before, the impulse response is the output of the wavelet filter when an impulse is used as its input.

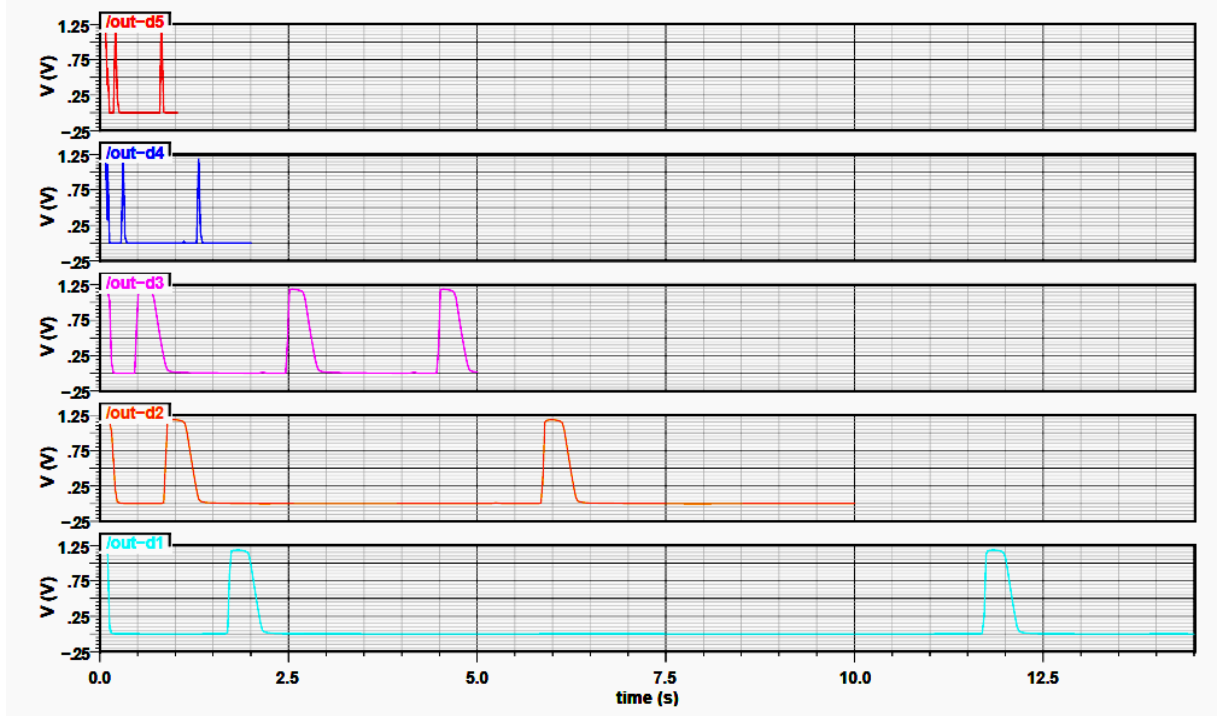


Figure 4.9: Binary outputs of 1st, 2nd, 3rd, 4th, 5th scales

The system is designed to detect the QRS complex and T-wave of the ECG signals. However, until now, the input signal was an impulse. In the previous section, the outputs of different scales are obtained for microcontrollers. As expected before, every impulse response from the input gives a binary signal in the output. In the next section, the system will be tested for the ECG signal as an input.

4.4. ECG signal as an input

In this section, the ECG signal is used as an input of our system. As the WT will reveal different morphologies, we hope to be able to detect both the QRS complex and T-wave of the heart signal. We expected to see digital pulses in the outputs of the system from the QRS complex and T-wave in different scales to be used for microcontrollers.

4.4.1. Circuit functionality

By using different scales, the WF is able to reveal different information of the ECG signal. Every scale zooms in the different frequencies and as an output of every scale, we expect to see digital pulses to make sure when QRS and T-wave are occurred. In this way, the QRS complex and T-wave, which have different frequencies, will be shown in the outputs of different scales as a digital pulse.

4.4.2. Simulation results for the ECG input

The first scale (Figure 4.10) with scale $a=s^1$ is simulated and the output of the wavelet filter and the detector can be seen in the next figures.

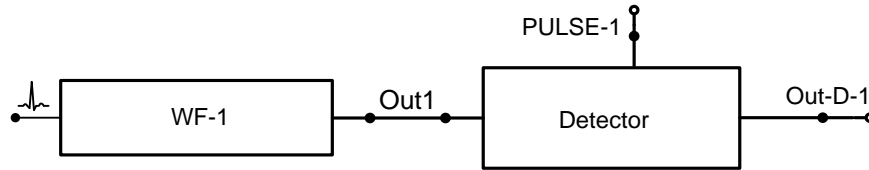


Figure 4.10: One scale with the ECG input

The ECG signal that is used as an input of our system can be seen in the next figure. This signal is an external ECG signal for a patient.

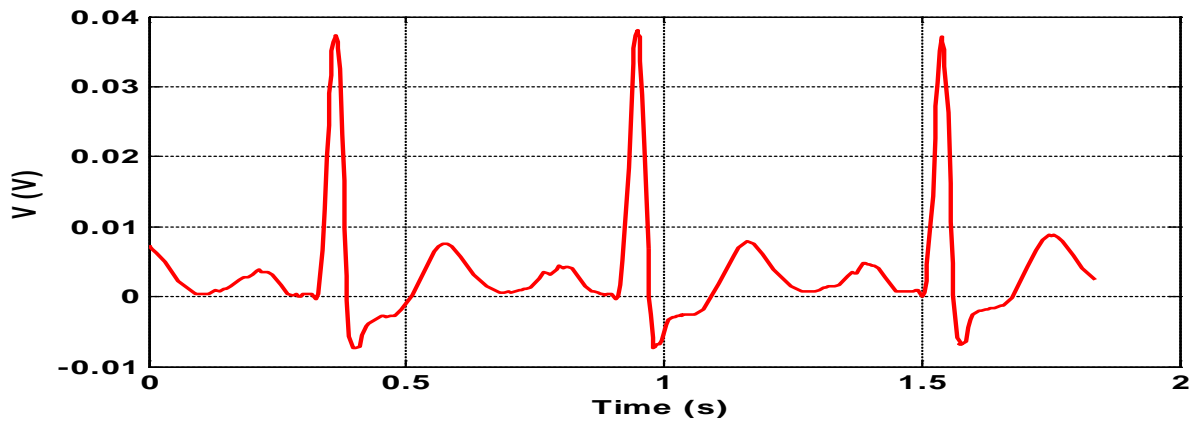


Figure 4.11: An ECG signal

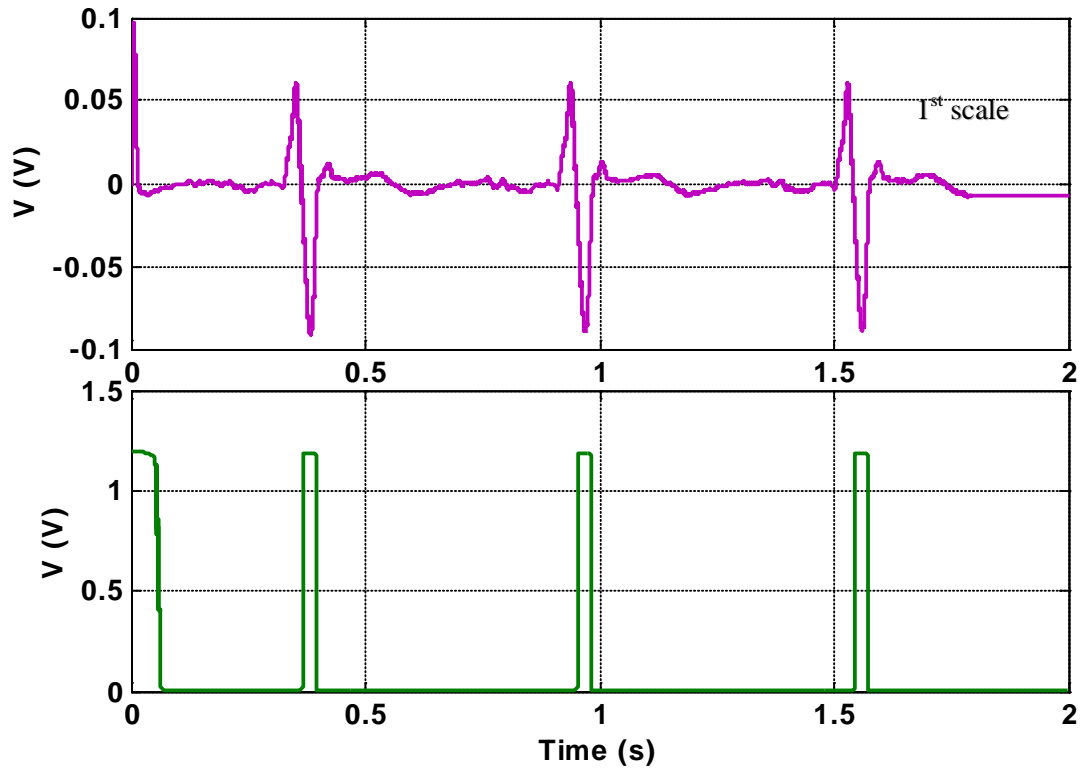


Figure 4.12: Output of the first wavelet filter (top) and the detector circuit (below)

The result shows that the system is ready to be simulated for the next scales. The block diagram of the whole system with the ECG signal as an input can be seen in the next figure.

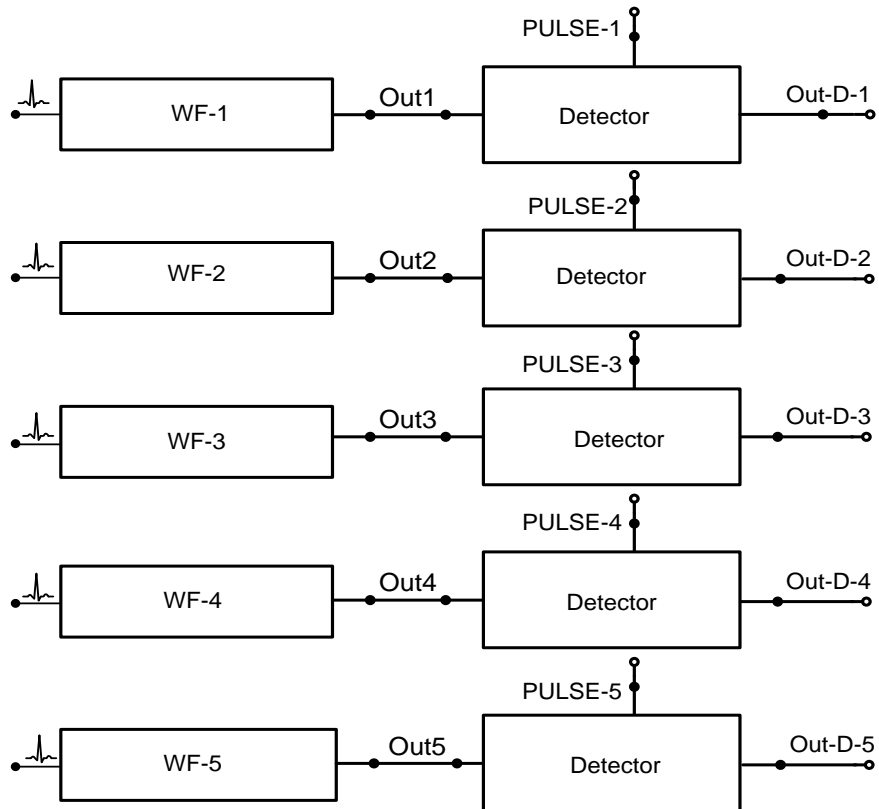


Figure 4.13: The whole system with the ECG signal as an input

This structure is simulated with the transient function in Cadence, and the result of every wavelet filter is plotted in the next figure. The outputs of the wavelet filters are given in the differential mode, and the outputs of the detectors, which are the final results in our thesis are plotted after that.

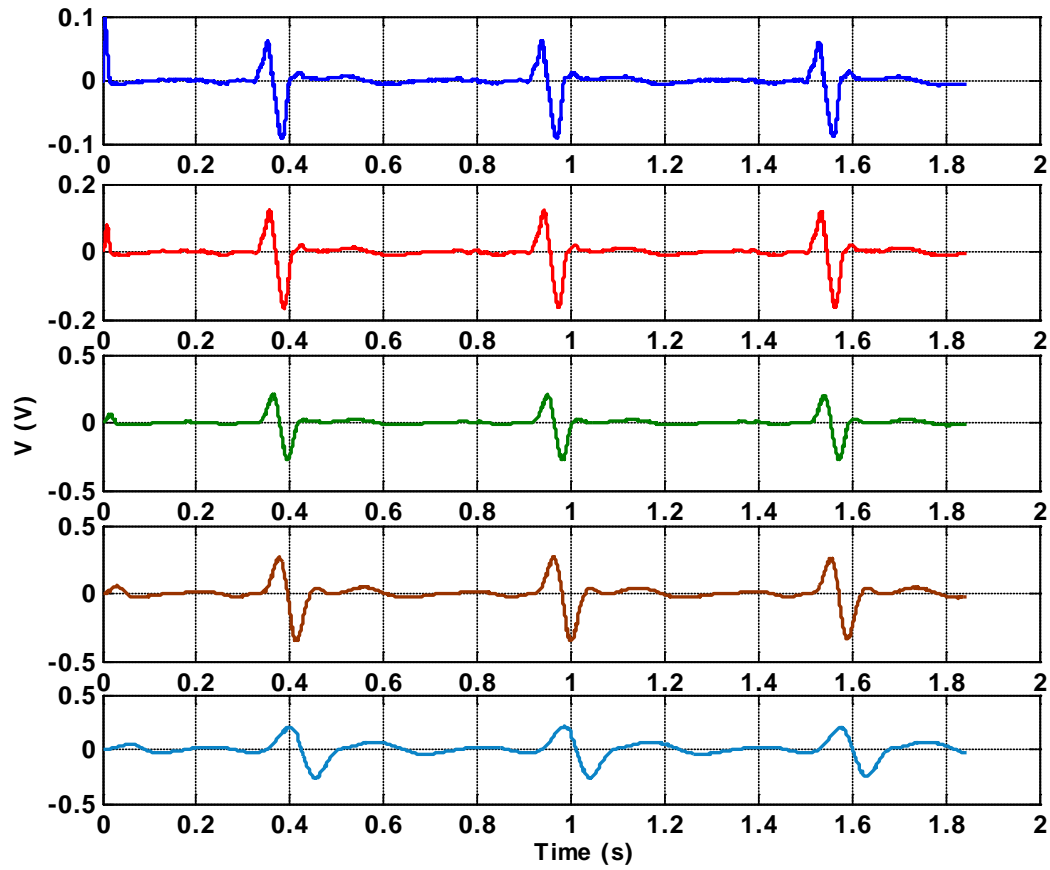


Figure 4.14: Output of the wavelet filters

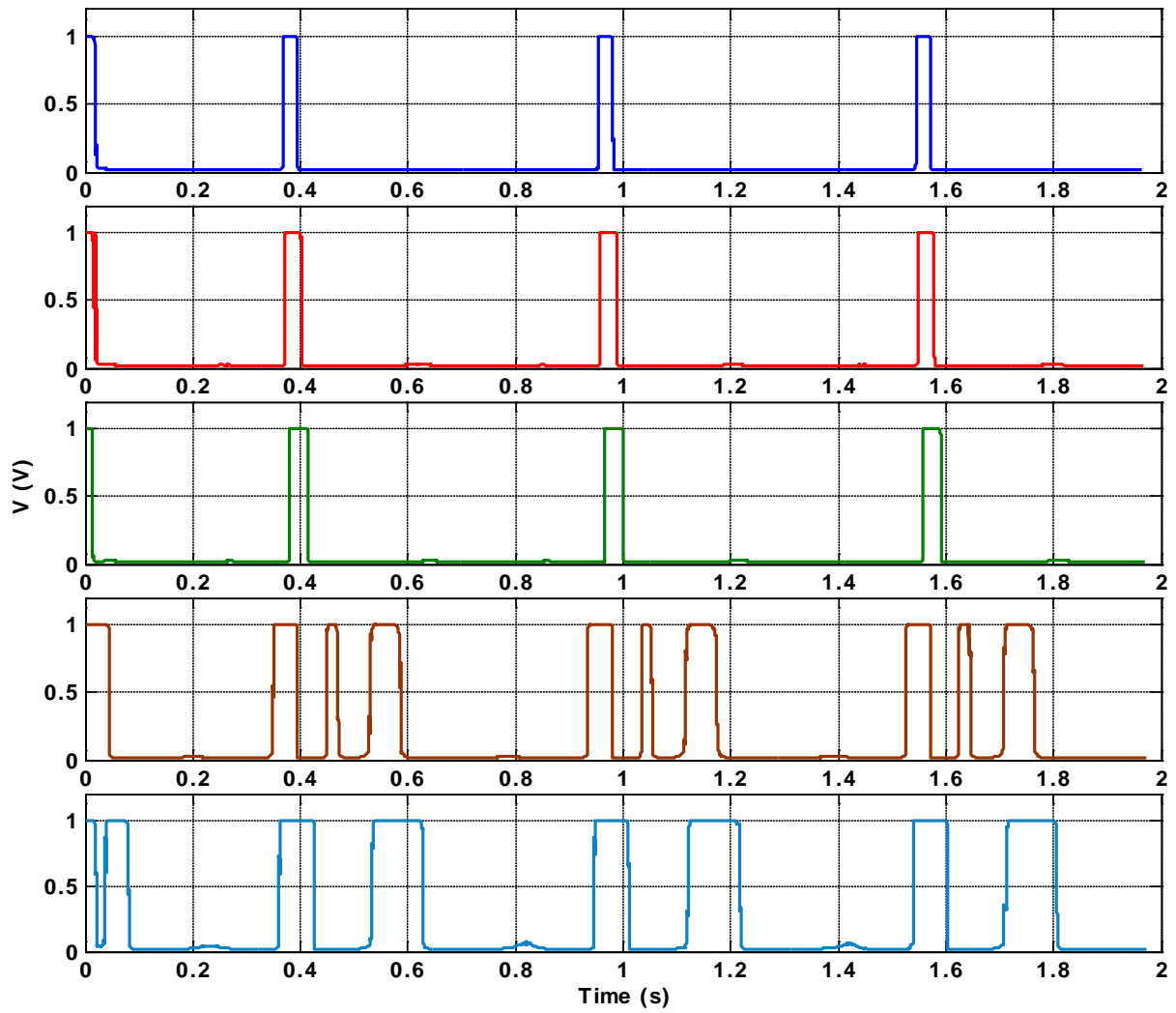


Figure 4.15: Outputs of the system

These results show that the QRS complex and the T wave of the ECG signal can be detected. In the two last scales with the lower frequencies (6.3 Hz and 12.51 Hz), the QRS complex and the T wave are detected. In the fourth scale, another peak can be seen. This is, because the ECG signal that is used in this thesis is an external ECG signal of a patient who had a heart problem. This shows that if the heart of a patient doesn't work properly and has unwanted peaks, this design is able to detect them by tuning the current comparator as an external option. All simulations and designs are performed in 37°C, which is the body temperature to make sure that the system is able to work as an implementable device.

The performance of the system is summarized in Table 4.3.

4.5. Conclusion

In this chapter, the wavelet filter bank and the detector circuit is simulated as a whole system. The simulation result of the wavelet filter bank gives the optimal impulse responses as compared to the ideal impulse response. The detector circuit is used after the wavelet filter. Then, the whole system is simulated with an impulse and the ECG signals as an input to the system. Different scales are

implemented by using different clock frequencies to keep the simplicity of our design. The results are obtained as the binary outputs that we were expected.

The QRS complex and the T-wave of an external ECG signal are detected in different scales. The system is a suitable design to detect the heart signal with some performance as following.

Table 4.3: Performance per scale

Technology	0.13 μm CMOS
Total bias current	$I=500\text{ nA}$
Supply voltage	1.2 V
Power consumption	3 μW
SNR_{MIN} WF	36.64 dB
Total capacitance	43.25 pF
Supply voltage range	0.8V – 1.65V
Temperature	37°C

In this thesis, the binary outputs are obtained from the QRS complex and the T wave in the different scales. In the last chapter the whole design is summarized and the conclusion is presented.

5. Conclusion

Since the first artificial pacemaker was introduced, much has changed and will continue to change in the future. Improvement in different areas of technology science, such as integrated circuit design and signal processing, gives the opportunity to improve the modern pacemakers. Also, due to various pathological states of the heart, morphological aspects of the cardiac signal need to be taken into account.

In implantable medical device, such as pacemakers, the power consumption and the area are critical issues, due to the limited power density and size of currently available portable battery. The Wavelet Transform (WT) has been shown to be a very efficient tool for analysis of non-stationary signals, like cardiac signals. This method can be used in a multiscale analysis technique, which offers the possibility of selective noise filtering and reliable parameter estimation, and therefore, can help the morphological analysis.

The thesis used a method for implementing the system based on WT using discrete-time analog circuitry. The methodology is based on the development of ultra low-power analog integrated circuits. The 1-bit ADC is needed for every scale of the whole system by using the analog integrated circuit design before the detector circuit. The QRS complex and T-wave are important parts of the ECG signal to be detected.

First, a brief overview of the history and development of circuit design was presented in chapter 1. Also, a comparison between frequency analysis, by means of the Fourier transform, and time-frequency representation, by means of the WT, was applied. The good time and frequency characteristic of the wavelet was revealed. In order to obtain the transfer function of certain wavelet filter, mathematical approximations techniques are required.

We indicated several methods to obtain good approximations in the time domain of the wavelet base. The Pade approximation has good performance to use. However, it has a few shortcomings. One of them is ringing at the beginning of its approximation and the other one is that it does not always gives a stable solution, especially for higher approximation orders. Another new method is the SVD approximation, which performs much better than the Pade method in this sense. It has no ringing at the beginning of its approximation, always gives a stable solution and better behavior in terms of mean square error. Due to the excellent accuracy and general applicability, the SVD approximation was chosen. We presented the state-space description for a circuit that implements a certain transfer function. This allows the designer to find a circuit that fits his specific requirements. The optimization method, which is described briefly by Haddad [1] provides an improvement in the circuit's dynamic range. This typically gives fully dense state-space descriptions. The Schwarz decomposition is the optimal state-space with respect to dynamic range, sparsity and sensitivity.

Next, in chapter 2, the theoretical structure is constructed in circuit level and it is tested by Matlab simuLink software. This gave an opportunity to drive the optimal, sparse state-space description ready for implementation with required specifications, such as wavelet, approximation order and sampling frequency. The wavelet filter is implemented by using a fully differential SC topology with common mode feedback suitable for this thesis. This topology is used, because of its high voltage swing at the output of the integrator, which spans the entire supply voltage range and therefore it has maximum dynamic range. Besides, because of its differential structure, the negative entries and the positive entries of the state-space description can be implemented.

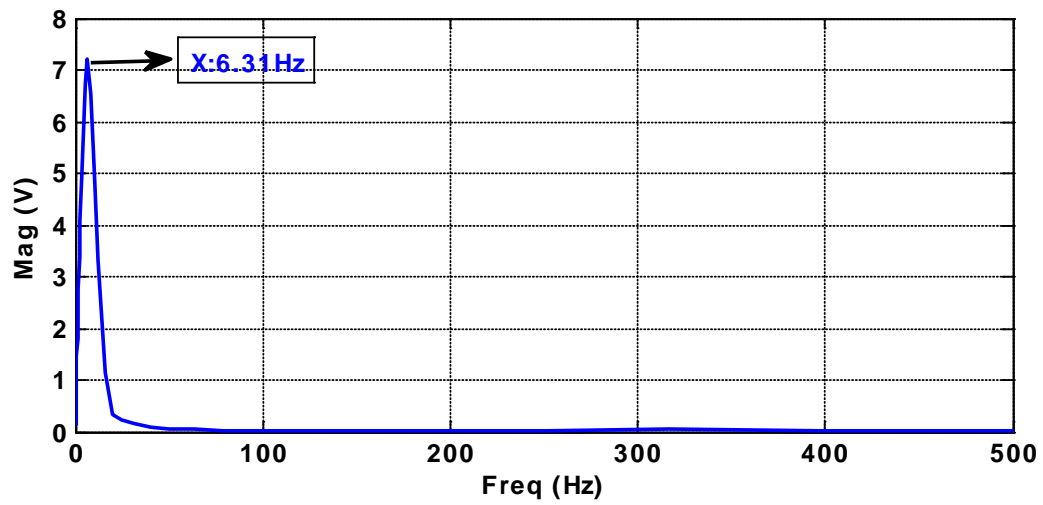
Subsequently, an approach for ultra low-power analog QRS complex detection circuit was implemented in chapter 3 to make our system design complete for one scale. This detector was consisted with *sinh* transconductor structure, current mirror, delay circuit, inverter and *nor*-gate circuit. *Sinh* is based on the exponential characteristics of the weak inversion MOSFETs. This exponential behavior expands the larger magnitude of the signal and thereby suppresses the influence of noise, which are usually smaller than the signal. By using the current mirror, the outputs current of the *sinh* transconductor were compared for a certain value to get the detected peaks of signal. Delay circuit was used to overlap and invert the first peak on other peak, and inverter circuit makes low logic output from the second peak. In this way, two low logic outputs were obtained to use as inputs of the *nor*-gate circuit. The binary output of the system was obtained because of the two low logic inputs of the *nor*-gate circuit.

Finally, the methodology presented in previous chapters was employed in the design of ultra low-power biomedical system to detect the QRS complex and T-wave of the ECG signals. Five scales were implemented in chapter 4 for different resolution with the same structure and different clock frequency components. This was done to keep the simplicity of our design, save area and minimum noise. Furthermore it is the first time that the discrete time structure is used for a wavelet filter. Moreover, a noise simulation is done for the whole system, which is also not done before. The flexibility, simplicity and stability are the advantages of this design. This gives a first step as a reference to design pacemakers in a novel way.

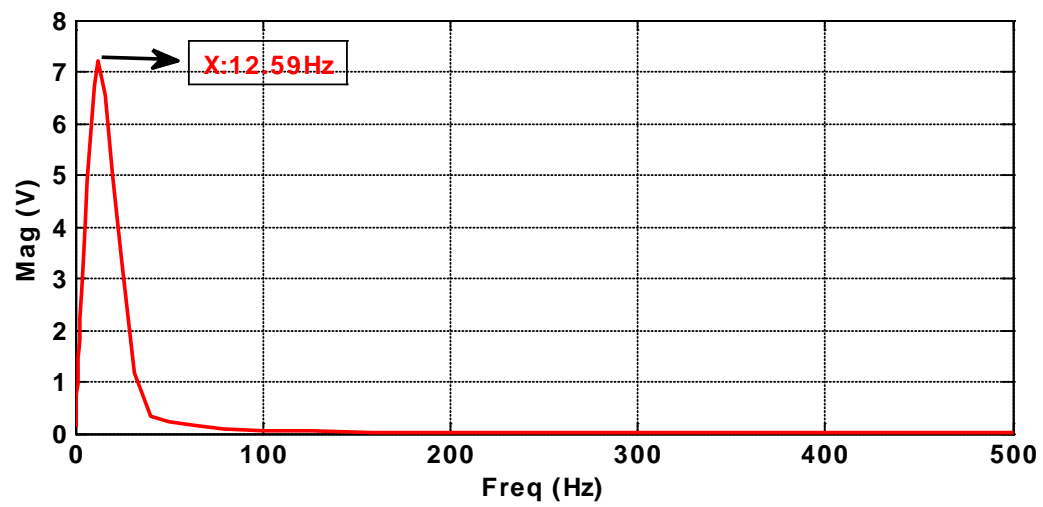
In this thesis the transient detection capability of the WT has been exploited for detection of the QRS complex. However, other important aspects in the cardiac signal, such as T-wave or P-wave can also be detected using wavelets. The next step, which has to be taken, is the IC design for implementing this circuit in currently modern pacemakers. The improvement of this design is the reduction of the power consumption and the area. A noise analysis is performed and a new detector circuit is developed. Further analysis techniques of cardiac signals are under progress and a fully integrated implementation of the analog WT circuit to be used in pacemakers is currently being investigated.

Appendix

Magnitude results of all scales in Cadence by using Pac and Pss functions.



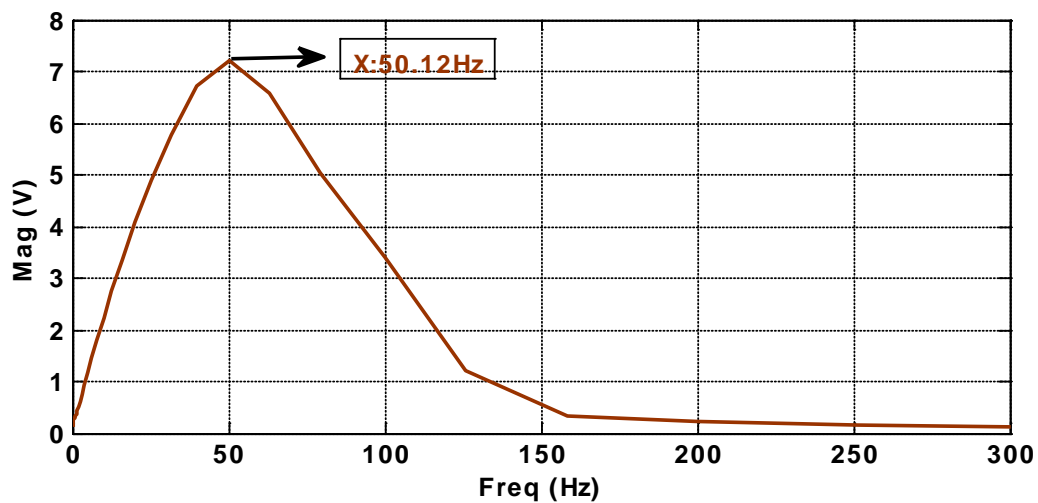
First scale



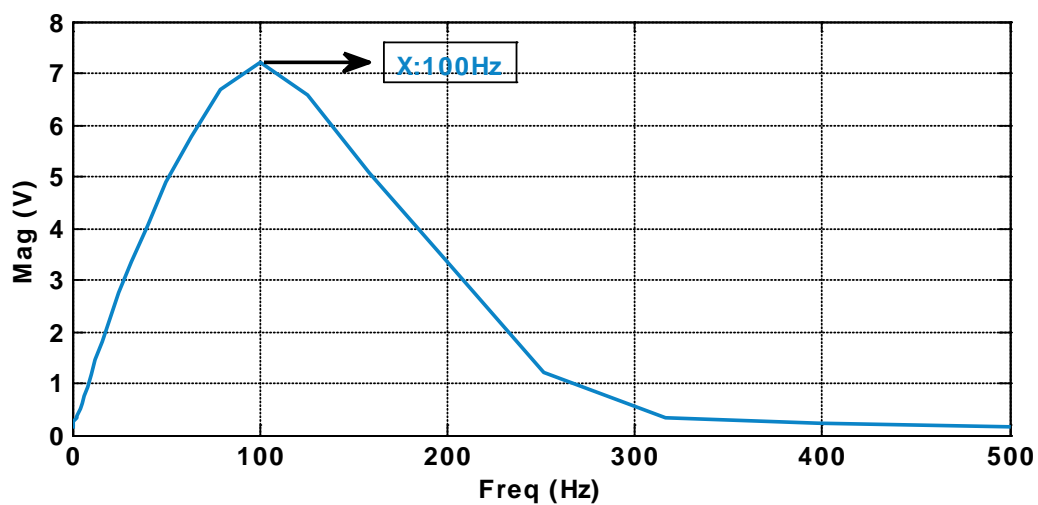
Second scale



Therd scale

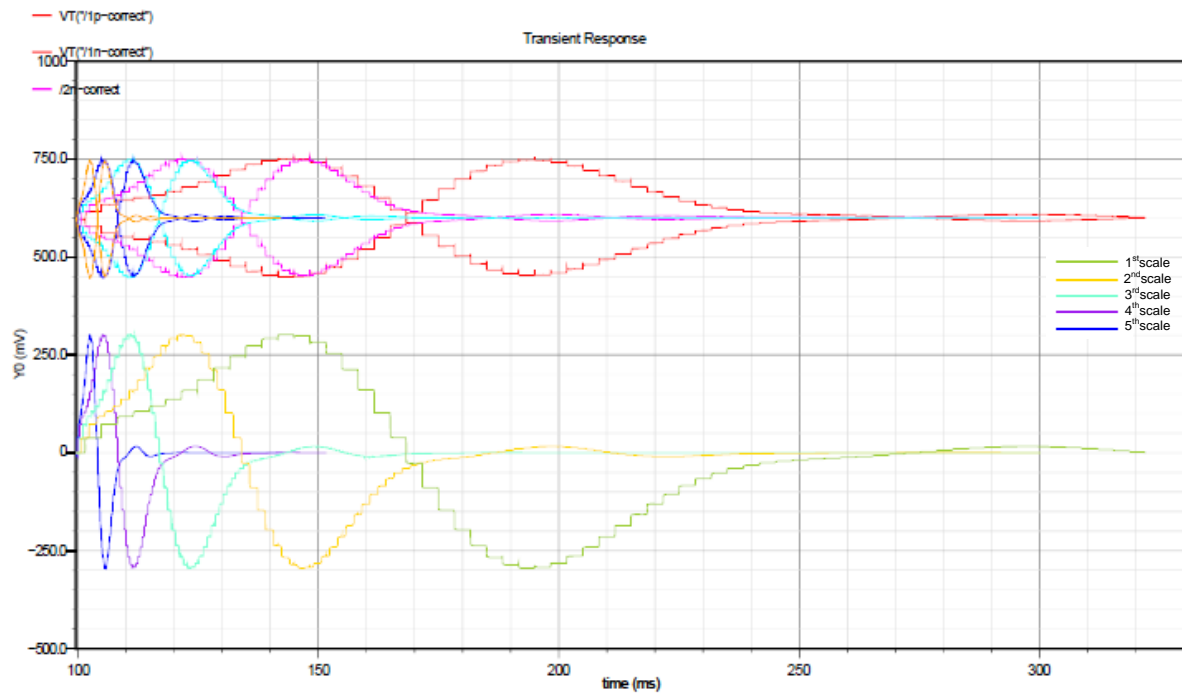


Forth scale

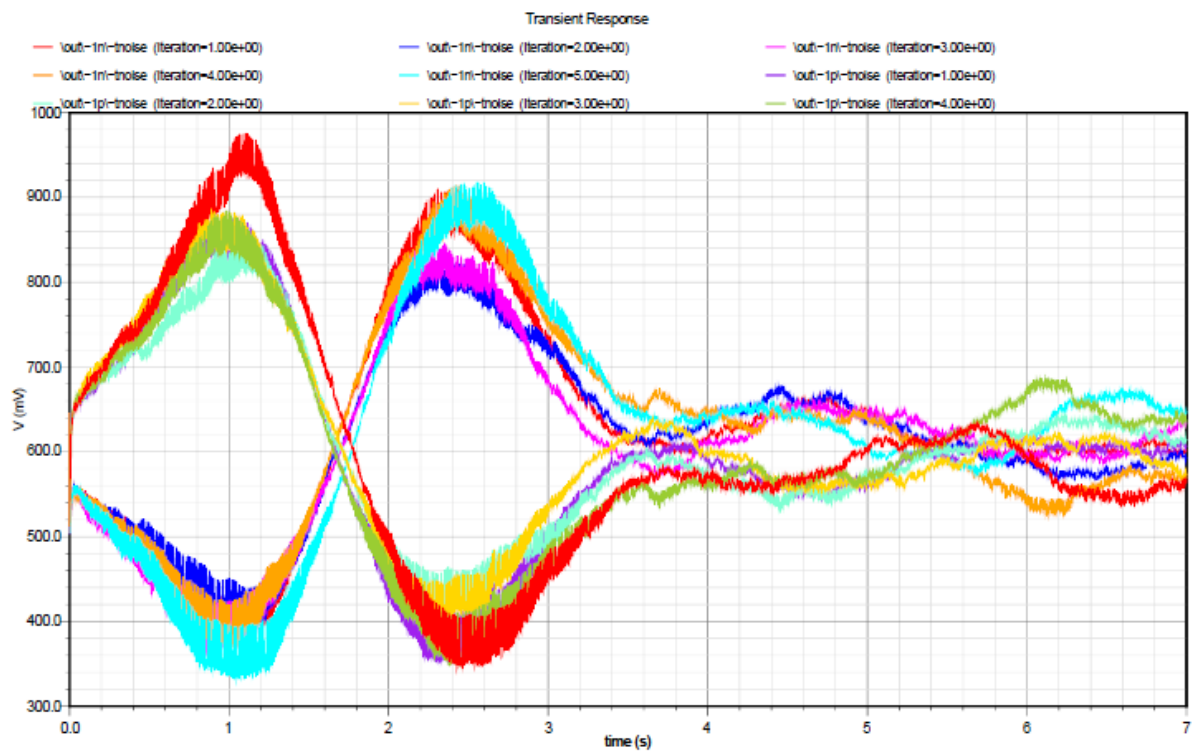


Fifth scale

Impulse response for the specific frequencies



The impulse responses of the 1st, 2nd, 3rd, 4th and 5th scales for the frequencies 6.31 Hz, 12.59 Hz, 25.12Hz, 50.12Hz and 100Hz, respectively



Transient noise simulation result



Ultra low power switched-capacitor wavelet-based ADC for ECG analyzer

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Motivation

- Ultra low power consumption is necessary for Wearable Implantable Medical Devices (WIMD) consequently to the small battery and area.
- Decrease the overall cardiac mortality which is around 40% of all human deaths by designing a device, such as artificial pacemaker.

Applications

- Analog wavelet filter before the signal enters the ADC to reduce the resolution of the ADC and consequently power consumption.
- Real time action potential (AP) detection method in discrete time to detect the QRS complex and T-wave of the ECG signal.

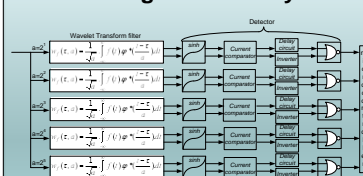
Wavelet filter and detector

- Provides local analysis of non-stationary signal.
- Performs the wavelet transform.
- By looking at the signal at various windows, analyses it with various resolution.
- Action potential of the input signal which can be included noise will be detected.
- By taking a sample of input signal, reduce the power.
- Make a digital output from the input signal.

Design

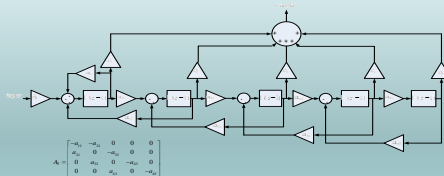
- Accuracy or the order of approximation versus power consumption.
- Discrete time solution in the wavelet filter (SC) and the detector (Switched in the real time action potential).
- Sparsity versus Dynamic range.
- Different scales by using different frequency to prevent the complicate circuit, area and noise challenging.
- Sinh* decomposition structure and current detector are implemented to detect the peaks of the input signal.
- Nor* circuit as a comparator to make a digital output.

Block diagram of the system



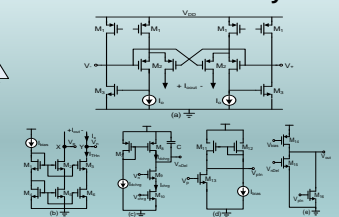
The whole block diagram is described by five scales wavelet filters, detectors and comparators, which are implemented by different clock frequency components to prevent the complicate circuit, reduce area and noise challenging.

A fifth order discrete time wavelet filter



The zero entries in the fully dense matrices of state-space description are increased by using Schwartz decomposition. As results: Minimal power consumption. Close to optimal dynamic range. Minimal sensitivity to components variations.

Detector circuitry

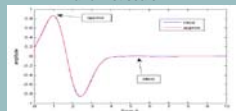


Implementation of *sinh* transconductor (a) current mirror comparator (b), delay circuit (c), inverter (d) and nor-gate (e)

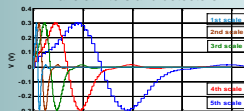
Circuit simulation with impulse

The impulse response of the state-space description and the first scale wavelet filter are provided by using Schwartz topology for the wavelet filter.

The impulse response of state-space and first scale



The five impulse responses of wavelet filters and detectors



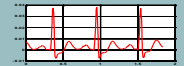
Circuit simulation with ECG signal

By using the time constant equation of the opamp, different resolutions are obtained by changing the clock frequency, f_{clk} .

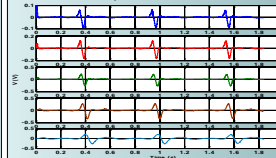
$$\tau = \frac{C_f}{C_{in} f_{clk}}$$

- Minimum size of C_f capacitor is chosen already.
- Increasing C_s costs the area.

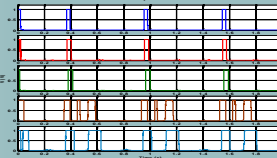
ECG signal as input signal



The five outputs of the wavelet filters



The five outputs of detectors



Conclusion

- To detect the heart beat, it is very important to make a good choice of the approximation method.
- The fully differential SC topology with SC CMFB is used, because of its high voltage swing at the output which spans entire supply voltage and therefore it has maximum dynamic range.
- By using the (non)inverting SC integrator, the negative entries as well as the positive entries of the state-space description can be implemented.
- The detector is constructed with *sinh* transconductor structure, current mirror comparator, delay circuit, inverter and *nor-gate* circuit.
- The binary outputs are obtained from QRS complex and T-wave the ECG signals.
- The ultra low-power consumption, flexibility, simplicity and stability are the advantages of this design.

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