A 16 V-Output Switched-Capacitor Sigma Converter With 180 ns Transient Response and 94% Efficiency for LiDAR Receivers

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***Abstract*—This article presents a step-up switched-capacitor (SC) sigma converter with fast transient, high efficiency, and high accuracy for light detection and ranging (LiDAR) receiver applications. The proposed sigma converter combines an unregulated SC converter in the high-voltage (HV) domain and a low-dropout (LDO) regulator in the low-voltage (LV) domain, achieving step-up voltage conversion through a series output connection. The unregulated SC converter operates in the HV domain, achieves high-efficiency power delivery, and boosts voltage in a very high density. At the same time, the LDO ensures fast transient response and accurate load regulation in the LV domain. The prototype achieves 5–16 V voltage boosting with a peak conversion efficiency of 94% at a maximum output power of 3.6 W and up to 152 mW/mm^3 power density. The LDO regulator ensures accurate load regulation of 44 μV/mA (0.063% error with full load range) and fast load transient response of 180 ns during 0–200 mA load current transition.**

***Index Terms*—Boost converter, dc–dc converter, fast transient, low dropout (LDO), sigma converter, switched-capacitor (SC) converter.**

I. Introduction

THE demand for high-density, high-efficiency, and fast dynamics power conversion has grown significantly with advancements in 3-D sensing, autonomous driving, and display technologies. A representative application is time-of-flight (ToF) sensors in light detection and ranging(LiDAR) systems.

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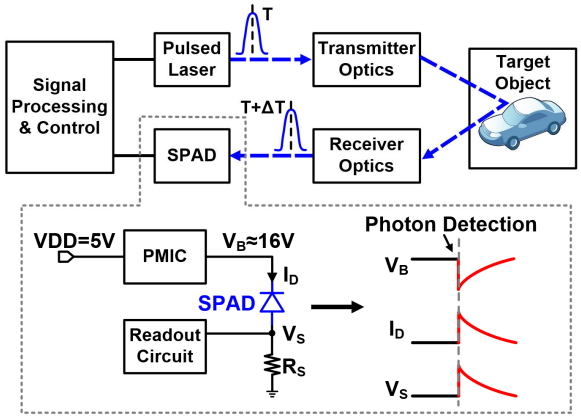

Fig. 1. Typical laser detection system and power supply for SPAD.

Fig. 1 shows a typical ToF LiDAR system. To detect the distance of a target object, a short laser pulse is emitted from the illumination unit at time T, passes through the transmitter optics, and reaches the target object [1]. The reflected laser passes through the receiver optics and is captured by a photodiode sensor at time $T + \Delta T$. The distance can be calculated by ToF (ΔT) times the speed of light. To enhance the sensitivity of the receiver, the single photon avalanche diodes (SPADs) are widely adopted, and they are usually reverse biased at a high voltage V_B (>10 V) in the avalanche breakdown region, so that only a few photons' injection can activate a large breakdown current. For the power supply, one example of the SPAD is biased at approximately 16 V, which is boosted by a power management IC (PMIC) from a 5 V general or USB power supply. Upon detecting a photon, a rapid surge of avalanche current $I_{\rm D}$ flows through the sensing resistor R_s, producing a voltage pulse V_S for the readout circuit. This configuration brings three significant challenges for the PMIC. First, it needs to generate a high biasing voltage with high efficiency to support avalanche breakdown while minimizing heat dissipation. Second, it should be capable of fast recovery from transient I_D events to minimize detection intervals. Finally, the supply voltage V_B should be accurately regulated with minimal ripple voltage to ensure the high detection accuracy of the SPAD.

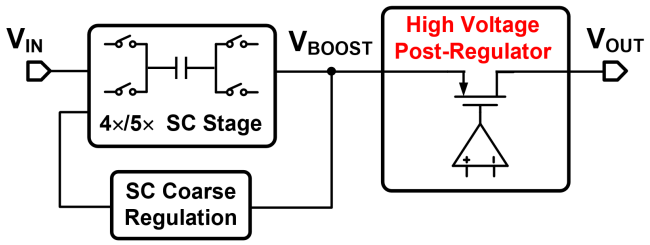

Fig. 2. Step-up SC converter cascaded with LDO as post-regulator.

Conventional boost converters (CBCs) are widely used in industrial applications. However, in high-voltage (HV) conversion applications, CBC requires a bulky power inductor to minimize current ripple [2]. Additionally, the need for HV-rated switches and the presence of a right-half-plane zero (RHPZ) limit the switching frequency of CBCs, thereby constraining their dynamic performance during the avalanche and reducing the recovery speed. Multi-layer ceramic capacitors offer energy densities that are at least two orders of magnitude higher than inductors [3], making switched-capacitor (SC) converters attractive candidates for reducing system volume. Various SC converter topologies have been explored, but open-loop SC converters suffer from topology-dependent, unregulated output voltage and low output voltage accuracy, which limits the detection accuracy of SPADs [4].

On the other hand, a closed-loop SC converter exhibits lower overall power conversion efficiency due to hard charging losses and variable switching frequencies [5]. Although fast transient response in SC converters can be achieved by increasing switching frequency, this comes at the cost of advanced processes and significant switching losses. Hybrid converters, which incorporate SC networks into CBCs, reduce voltage and current stress across the power inductor, thereby improving power density [6], [7], [8], [9]. Nevertheless, the bulky inductors and RHPZ of the hybrid boost converter are still the main factors that restrict the system volume and dynamic performance.

To achieve regulated output with high power density, SC converter cascaded with low-dropout (LDO) regulators are commonly employed in bipolar power supplies for LED displays [10], [11]. In Fig. 2 [12], a HV post-regulator LDO is cascaded with a reconfigurable step-up SC converter, where the SCC boosts the input voltage up by 4/5× to V_{BOOST}, and the LDO further regulates V_{OUT}. The LDO effectively filters out most of the noise from the SC converter and significantly improves the output accuracy. However, since the LDO operates in the floating HV domain, this architecture's overall bandwidth and output power are still constrained by the limitations of HV devices.

Fig. 3 shows the sigma converter architecture that combines the advantages of two topologies [13], [14], [15], [16]. In the step-down sigma converter configuration, the input voltage splits into two voltage domains, high-voltage HV, V_H and low-voltage (LV), V_L domains, and is handled by two in-series connected converters. The outputs of two converters are combined at the output voltage node. Typically, in the HV domain, dc transformers (DCX) with large conversion ratios or converters with high efficiency are preferred. For example, DCX were used by [13] and [16], and an open-loop SC converter was used by [14] to perform the large-ratio voltage conversions fromV_H to the output voltage (V_{OUT}). A second converter in the LV domain, such as a buck or hybrid SC converter, regulates the output voltage.

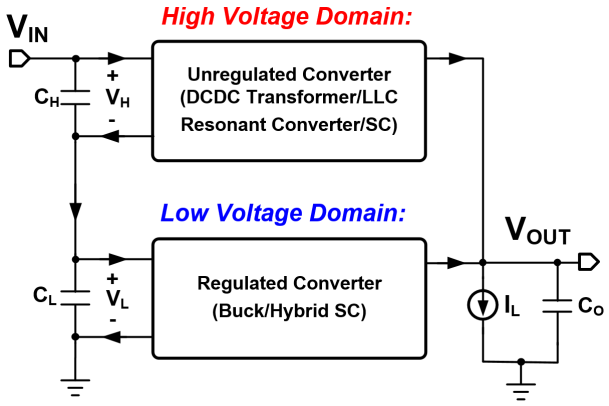

Fig. 3. Concept of step-down sigma converter architecture.

The powers of the HV and LV converters are allocated by V_L and V_H. The system efficiency η_{SIGMA} can be expressed as follows:

$$\eta_{\text{SIGMA}} = \frac{V_H}{V_{\text{IN}}}\eta_H + \frac{V_L}{V_{\text{IN}}}\eta_L. \tag{1}$$

It is noted that in the condition when V_H is significantly higher than V_L ($V_H \gg V_L$), the efficiency η_{SIGMA} is primarily determined by the HV unregulated converter. As such, the Sigma converter architecture leverages the HV converter's efficient voltage conversion and the LV converter's regulation capability.

Up to now, most of the sigma converter works are in step-down power conversions. Inspired by this architecture, we present an SC sigma converter for LiDAR applications in this work [17]. The architecture combines an efficient, compact SC converter in the HV domain with a high-accuracy, fast-transient LDO in the LV domain. The SC converter and the LDO are in a step-up sigma configuration. In the HV domain, an open-loop 3× Dickson SC converter ensures efficient power delivery with high density. In the LV domain, the high bandwidth and high gain LDO achieves less than 200 ns load transient response speed and guarantees precise voltage regulation while enabling load sensing for adaptive loop compensation. The proposed converter is inductor-less, facilitating high-density power delivery and efficient voltage boosting without the RHPZ issues typically associated with inductive converters.

The remainder of this article is organized as follows. Section II presents the architecture of the proposed step-up SC sigma converter, with a detailed discussion on efficiency and dc and ac regulation. Section III shows the detailed circuit implementation, focusing on the design and operation of the SC converter's power stage and LDO regulator. Section IV presents the measurement results, and Section V concludes this article with a summary of the findings.

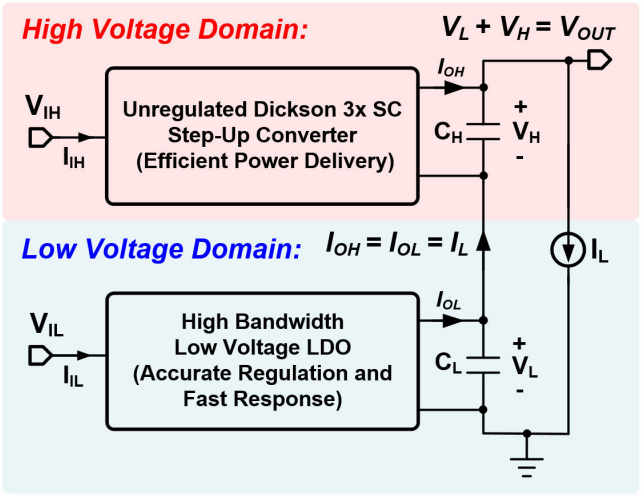

Fig. 4. Concept of proposed SC sigma converter.

II. Proposed SC Sigma Converter

Fig. 4 shows the concept of the proposed SC sigma converter. In the HV domain, an unregulated 3× step-up Dickson-type SC converter boosts the high-side input voltageV_{IH} to a floating voltage V_H. Meanwhile, an LDO regulates the low-side input voltage $V_{\rm IL}$ to V_L in the LV domain. The SC converter and LDO are connected in series at the output. Therefore, the output voltage $V_{\rm OUT}$ and load current I_L can be expressed as follows:

$$V_{\rm OUT} = V_H + V_L \tag{2}$$
$$I_L = I_{OH} = I_{OL}. \tag{3}$$

A. Voltage Dependent Efficiency and Peak Efficiency

According to (2) and (3), the overall efficiency η can be derived as follows:

$$\begin{aligned}\frac{1}{\eta} &= \frac{P_{\rm IN}}{P_{\rm OUT}} = \frac{V_{IL}I_{IL} + V_{IH}I_{IH}}{V_{\rm OUT}I_L} \\ &= \frac{V_L}{V_{\rm OUT}} \cdot \frac{V_{IL}I_{IL}}{V_L I_{OL}} + \frac{V_H}{V_{\rm OUT}} \cdot \frac{V_{IH}I_{IH}}{V_H I_{OH}} \\ &= \frac{V_L}{V_{\rm OUT}} \cdot \frac{1}{\eta_L} + \frac{V_H}{V_{\rm OUT}} \cdot \frac{1}{\eta_H}.\end{aligned} \tag{4}$$

We can obtain that

$$\eta = \frac{V_{\rm OUT}\eta_L\eta_H}{V_L\eta_H + V_H\eta_L} \tag{5}$$

where η_L and η_H are the conversion efficiencies of the low-side and high-side converter, respectively.

In the condition when V_H is much higher than V_L, (5) can be reorganized as follows:

$$\begin{aligned}\eta &= \frac{V_{\rm OUT}\eta_L\eta_H}{V_L\eta_H + V_H\eta_L} \\ &\approx \frac{V_{\rm OUT}\eta_L\eta_H}{V_{\rm OUT}\eta_L} = \eta_H \left(V_L \ll V_H \approx V_{\rm OUT}\right).\end{aligned} \tag{6}$$

In this work, V_H is designated at 15 V, which is boosted 3× from from universal or USB power supplies voltage at $V_{IH} = 5$ V, while V_L is regulated to ∼1 V from a 2 V supply. The target output voltage is 16 V to bias the SPAD device sufficiently. Since V_H is approximately equal to $V_{\rm OUT}$ and significantly larger than V_L, (5) can be simplified to (6), where η approximated equals η_H. In other words, the efficiency of the high-side SC converter is the primary determinant of the overall system efficiency when V_H constitutes a major portion of the output voltage. The highest efficiency can be achieved as long as the SC converter operates in the open-loop mode. Therefore, a highly efficient open-loop SC converter is preferred and optimal for the high-side converter.

To determine the peak efficiency, we consider the input powers($P_{\rm IH}$ and $P_{\rm IL}$) of each domain and load currents (I_L), and we can obtain

$$P_{IH} = 3V_{IH}I_L + P_{\rm SW} + P_{\rm PAR}\,(\text{HV Domain } 3\times \text{SCC}) \tag{7}$$
$$P_{IL} = V_{IL}I_L + P_Q\,(\text{LV Domain LDO}) \tag{8}$$

where $P_{\rm SW}$ and $P_{\rm PAR}$ are the switching and parasitic losses of the SC converter, and P_Q is the quiescent power of the LDO, respectively. By substituting (7) and (8) into (5), η can be rewritten as follows:

$$\begin{aligned}\eta &= \frac{P_{\rm OUT}}{P_{\rm IN}} = \frac{V_{\rm OUT}I_L}{V_{IL}I_L + V_{IH}\cdot 3I_L + P_{\rm SW} + P_{\rm PAR} + P_Q} \\ &= \frac{V_{\rm OUT}}{V_{IL} + 3V_{IH} + \left(P_{\rm SW} + P_{\rm PAR} + P_Q\right)/I_L}.\end{aligned} \tag{9}$$

Equation (9) shows that while the output voltage remains regulated, the theoretically maximum efficiency is$V_{\rm OUT}$/($V_{\rm IL}$+ $3V_{\rm IH}$) and the efficiency increases with load current. The portion of losses decreases with the load increasing, and the peak efficiency is achieved at maximum load conditions. In this design, η is theoretically maximum to be 16/17, which is verified as 94.1% in the measured efficiency.

B. R_{OUT} Compensation

Fig. 5(a) shows the equivalent model of the SC sigma converter.$V_{\rm IN5}$ and $V_{\rm IN2}$ are the inputs of the SC converter and LDO, respectively. The 3× SC converter is modeled as a 3× transformer with its output resistance $R_{\rm OUT}$ [18] and an ac voltage source ΔV_H that accounts for the switching ripple. $V_{\rm OUT}$ is fed back by $V_{\rm FB}$ to the LDO and is determined by $V_{\rm REF}$.

In the dc domain, $V_{\rm OUT}$ is expressed as follows:

$$\begin{aligned}V_{\rm OUT} &= V_L + V_H \\ &= V_L + 3V_{\rm IN5} - I_L R_{\rm OUT} \\ &= 3V_{\rm IN5} + \left(V_L - I_L R_{\rm OUT}\right).\end{aligned} \tag{10}$$

As I_L increases, V_H decreases due to $I_L R_{\rm OUT}$ drop and V_L elevates accordingly to minimize the error ($V_{\rm FB} - V_{\rm REF}$), keeping ($V_L - I_L R_{\rm OUT}$) and hence the average output constant, as shown in Fig. 5(b). Thereby, the $R_{\rm OUT}$ of the SC converter is compensated by the LDO's output voltage (V_L) as long as the regulating transistor of the LDO remains in the saturation region. The maximum V_L is

$$V_{L,\rm MAX} = V_{\rm IN2} - V_{\rm DO} \tag{11}$$

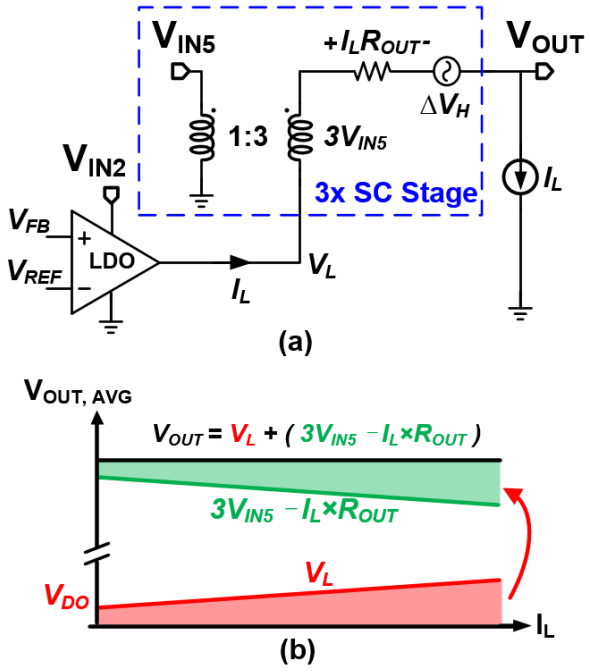

Fig. 5. (a) Equivalent circuit model of SC sigma converter. (b) DC regulation scheme.

where V_{DO} denotes the dropout voltage of LDO. After substituting (11) into (10), the maximum load current$I_{L,\mathrm{MAX}}$ for effective dc regulation can be derived as in

$$I_{L,\mathrm{MAX}} = \frac{1}{R_{\mathrm{OUT}}}\left[(3V_{\mathrm{IN5}} + V_{\mathrm{IN2}}) - (V_{\mathrm{OUT}} + V_{\mathrm{DO}})\right]. \quad (12)$$

In this design, $I_{L,\mathrm{MAX}}$ is 225 mA with a V_{DO} of 150 mV, and R_{OUT} should be smaller than 3.7 Ω. Dickson-type SC topology is employed to obtain this small R_{OUT}, which will be discussed in Section III.

C. AC Ripple Cancellation and Dynamic Performance

In terms of the output ripple ΔV_{OUT} it is mainly caused by the SC converter's switching ripple ΔV_H, which is

$$\Delta V_H = \frac{1}{2C_H f_{\mathrm{SW}}} I_L \quad (13)$$

where f_{SW} is the switching frequency of the SC converter. To mitigate the output ripple, the bandwidth of the LDO is designed to be substantially higher than f_{SW} so that the LDO can track ΔV_H and generate ΔV_L at opposite voltage to counteract the ripple of the SC converter effectively.

Fig. 6 shows the ac equivalent circuit of the SC sigma converter. The output voltage V_{OUT} is fed back by a resistor divider R_{F1} and R_{F2}, and the feedback voltage V_{FB} is connected to the positive terminal of the LDO. The error signal $(V_{\mathrm{FB}} - V_{\mathrm{REF}})$ is amplified by the transfer function $H(s)$ to V_L. There are two requirements for effective load regulation of V_{OUT} through V_L.

First, in the ac domain, it is essential that the voltage betweenV_L and V_{OUT} is strongly coupled. During load current transient, the load current i_L flowing from V_L to V_{OUT} primarily traverses the low-impedance capacitive pathway. The small signal transfer function can be expressed as follows:

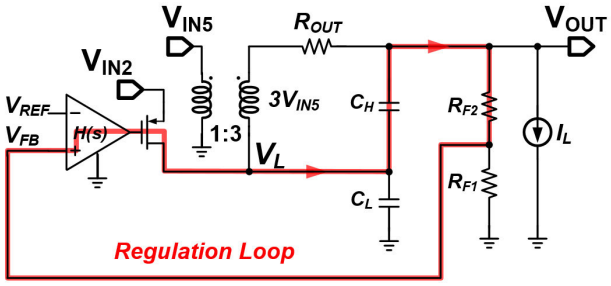

Fig. 6. Equivalent circuit model of closed-loop SC sigma converter.

$$\frac{v_{\mathrm{OUT}}(s) - v_L(s)}{\frac{1}{sC_H}} = \frac{v_L(s)}{\frac{1}{sC_L}}. \quad (14)$$

Hence,

$$v_{\mathrm{OUT}}(s) = v_L(s) \times \left(1 + \frac{sC_L}{sC_H}\right). \quad (15)$$

From (15), it can be observed that when C_H is substantially larger than C_L, $v_{\mathrm{OUT}}(s)$ is approximately equal to $v_L(s)$, the ac voltage change at node V_{OUT} will be effectively coupled to V_L. In such a case, the transient response of the converter will be mainly determined by the LDO, and the large capacitor C_H can be regarded as a low-frequency voltage source.

The second requirement is that the bandwidth of $H(s)$ should be sufficiently higher than the switching frequency of the SC converter. In this design, C_H (2 × 2.2 μF) is over∼1000 times larger than C_L (4.7 nF), and the bandwidth of the LDO is at least 70 times higher than the f_{sw} of the SC converter. The closed-loop load regulation can therefore be expressed as follows:

$$\frac{v_{\mathrm{OUT}}(s)}{v_L(s)} = -\frac{1}{\frac{R_{F1}}{R_{F1}+R_{F2}} H_{(s)}}. \quad (16)$$

Equation (16) indicates that the ac regulation is predominantly determined by the voltage divider and LDO. The accuracy of the output voltage can be ensured with a high loop gain of the LDO.

III. Circuit Implementations

Fig. 7 presents the circuit implementation of the proposed SC sigma converter. The high side SC converter operates at an adjustable frequency between 300 and 2.3 kHz. On the low side, the LDO regulates V_L by passing device M_P. Three additional blocks are implemented to optimize the sigma converter performance, including a discharge switch, a current sensor, and a dynamic compensation scheme.

A. High Side Open-Loop SCC

The high-side SC converter is based on a 3× Dickson-type SC topology and a 1× SC buffer. This design incorporates three flying capacitors C_{1-3}, two output capacitors C_H and C_L, and ten power switches S_{1-10}. Fig. 8 shows the operational scheme of the power stage. During phase 1 (φ_1), the

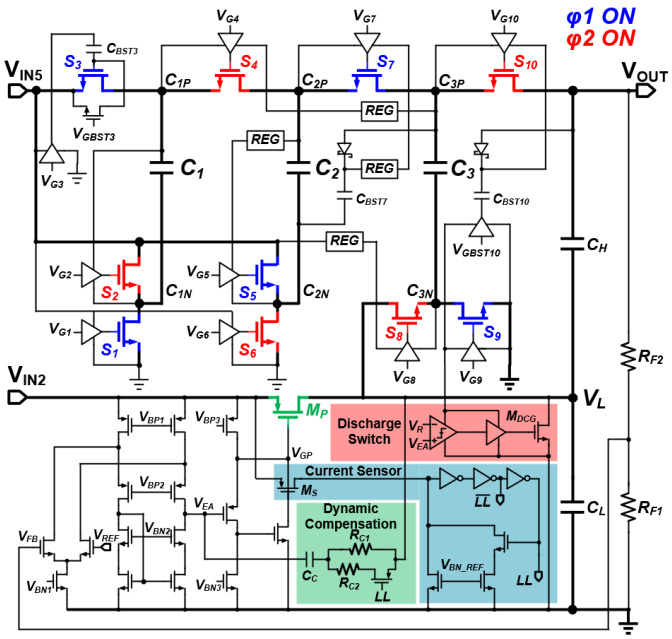

Fig. 7. Circuit implementation of the proposed SC sigma converter.

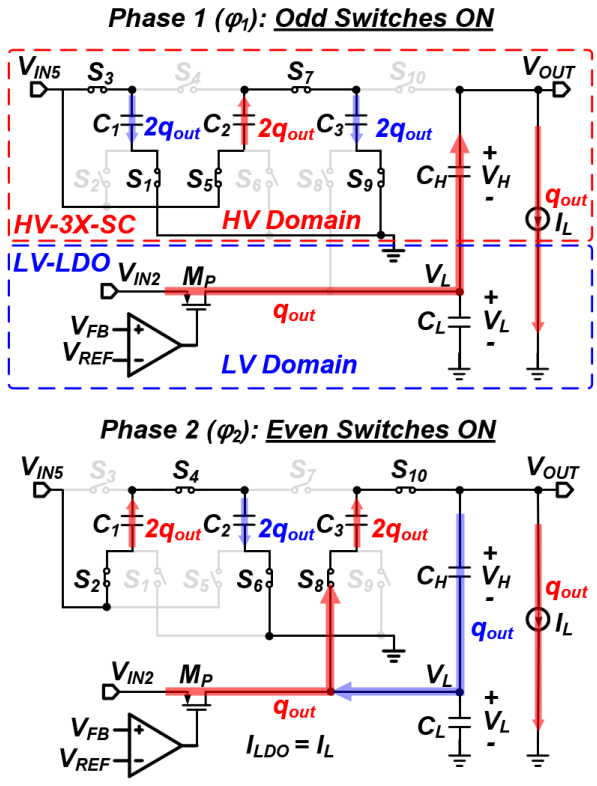

Fig. 8. Operation and charge flow of the power stage.

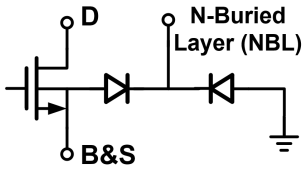

Fig. 9. Power switch isolation with junction diodes.

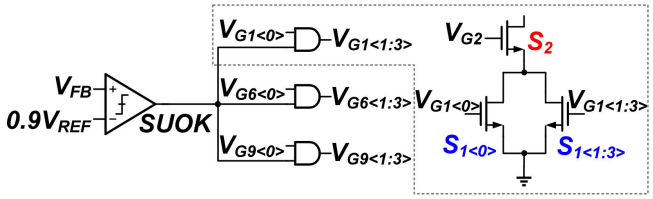

Fig. 10. Start-up design for the high side SCC.

TABLE I
VOLTAGE STRESS, SIZE AND ISOLATION CONNECTION OF SWITCHES

Switch	$V_{DS,max}$	W@L_{min}	NBL	Switch	$V_{DS,max}$	W@L_{min}	NBL
S_1	5 V	40m	-	S_6	5 V	40m	-
S_2	5 V	40m	V_{IN5}	S_7	10 V	20m	C_{2P}
S_3	5 V	15m	V_{IN5}	S_8	2 V	10m	V_{IN2}
S_4	10 V	20m	C_{1P}	S_9	2 V	10m	-
S_5	5 V	40m	V_{IN5}	S_{10}	2 V	15m	V_{OUT}

odd-numbered switches are on, C_1 is charged by V_{IN5} and C_3 is charged by V_{IN5} and C_2. C_H is discharged by load. The voltage relationship can be expressed as in

$$V_{\mathrm{IN5}} = V_{C1} \tag{17}$$

$$V_{C3} = V_{\mathrm{IN5}} + V_{C2}. \tag{18}$$

In φ_2, C_2 is charged by V_{IN5} and C_1, while C_3 is discharged by C_H and the load. The voltage relationships can be expressed as follows:

$$V_{C2} = V_{\mathrm{IN5}} + V_{C1} \tag{19}$$

$$V_H = V_{C3}. \tag{20}$$

By substituting (17)–(19) into (20), V_H and $V_{\rm OUT}$ can be derived

$$V_H = 3V_{\rm IN5} \tag{21}$$

$$V_{\rm OUT} = 3V_{\rm IN5} + V_{\rm IN2}. \tag{22}$$

All power transistors are implemented by NMOS to minimize chip size. Specifically, switches $S_{1-3,\ 5\text{-}6}$ are 5 V rated NMOS, S_{8-10} are 2 V NMOS, S_4 and S_7 are 12 V LDNMOS. The voltage isolation of this design is based on the junction diode, as shown in Fig. 9. The voltage stress and the connection of N-Buried Layer (NBL) are summarized in Table I. To optimize the efficiency of SCC, equivalent output resistance analysis [18] is performed based on the charge flow at steady state, as marked in Fig. 10. The equivalent output resistance is given as follows:

$$R_{\rm OUT} = \sqrt{R_{\rm SSL}^2 + R_{\rm FSL}^2} \tag{23}$$

where $R_{\rm SSL}$ and $R_{\rm FSL}$ are the equivalent resistance of the SC converter at the fast-switching limit and slow-switching limit, respectively. To obtain the desired$R_{\rm OUT}$ at maximum load, the sizes of the on-board capacitors C_i, switching frequency $f_{\rm SW}$, and the size of on-chip power switches are optimized according to [18]. In detail, a $R_{\rm OUT}$ smaller than 3.7 Ω is required to deliver a maximum load of 225 mA, which necessitates a suitable $R_{\rm SSL}$ and $R_{\rm FSL}$. For $R_{\rm SSL}$, a switching frequency of 300 kHz is adequate to obtain an $R_{\rm SSL}$ as small as 1 Ω, given that each flying capacitor is 10 μF. The overall $R_{\rm OUT}$ in this design is limited by $R_{\rm FSL}$. The sizes of each power switch are primarily determined by the charge delivered by the switches, as shown in Table I, and an $R_{\rm FSL}$ of 3.2 Ω is obtained. The sizes of grounded switches are preferably enlarged, as no area penalty is associated with the bootstrap capacitor. As a result, the overall $R_{\rm OUT}$ at 3.4 Ω is obtained with $C_{1\text{-}3}$ of 10 μF and $f_{\rm SW}$ of 300 kHz. A light-load (LL) mode is also implemented in the SCC driver. When the load sensing circuit detects a light load (LL) situation, $f_{\rm sw}$ is reduced to 1/128× to minimize switching loss and enhance efficiency under LL conditions.

The detailed driver circuit of the SC converter is also shown in Fig. 7. The control signals of power switches$V_{\rm G1-10}$ are generated from the same clock signal. A fixed delay is inserted in the local clock buffer to generate non-overlapping control signals with sufficient deadtime. The drivers of $S_{1,}$ S_6, and S_9 are directly powered by the input voltage $V_{\rm IN5}$ and $V_{\rm IN2}$, respectively. Driver of S_2 is powered by C_{1P}. The supply voltages of V_{G3} and V_{G10} are generated from the driver-based charge pumps with $C_{\rm BST3}$ and $C_{\rm BST10}$, respectively. S_4 and S_7 are driven by regulators that generate the desired voltage levels from C_{3P}. Similarly, the drivers for S_5 and S_8 are regulated from C_{2P} and $V_{\rm IN5}$, respectively.

During the start-up process, a large inrush current can occur due to the smallON-resistance and the substantial voltage difference across power switches to charge the loading and flying capacitor. A current-limiting start-up scheme is used, as illustrated in Fig. 10. The switchesS_1, S_6, and S_9 are equally divided into four cells, for example, $S_{1<0:3>}$. The start-up signal SUOK is low during start-up, turning on $S_{1<0>}$ (25% of the full switch) while keeping $S_{1<1:3>}$ off. This configuration effectively quadruples the ON-resistance of S_1, thereby reducing the inrush current. Once $V_{\rm OUT}$ reaches 90% of the desired value, SUOK turns high, and the SC converter will operate normally.

B. LV Side LDO Regulator Design

Fig. 11 shows the circuit implementation of the LDO regulator in the LV domain. It consists of the power transistorM_P, the error amplifier (EA), the super source follower (SSF), the dynamic compensation, the load-current sensing circuit, and the discharge switch.

The power transistor M_P is implemented by a 2 V PMOS transistor and sized by the maximum load current $I_{L,\rm MAX}$, and the overdrive voltage at the edge of the saturation region, as given by

$$\frac{W}{L} \geq \frac{2I_{L,\rm MAX}}{\left(V_{\rm GS} - V_{\rm TH}\right)^2 \mu_p C_{\rm ox}}. \tag{24}$$

To minimize output error, the folded cascode EA is adopted for its high dc gain. The output impedance $r_{\rm o,EA}$ of the EA is high, forming a low-frequency pole with the gate capacitance$C_{\rm GP}$ of the pass device. To achieve high bandwidth, an SSF is introduced between the EA and the pass device, effectively reducing the output impedance seen by $C_{\rm GP}$.

Three major poles and two zeros are labeled in Fig. 11. In this design, the load current of LDO ranges from 0 to 225 mA, significantly affecting the output pole p_1. To ensure the stability of the system, the dominant pole is placed at the output end of EA and labeled as p_0. Two other poles, p_1 and p_2, are located at the output of EA and LDO, respectively. Two zeros, z_1 andz_2, are implemented to compensate for the secondary poles. The frequency of the dominant pole p_0 is given as follows:

$$f_{p_0} \approx \frac{1}{2\pi} \cdot \frac{1}{r_{o,\rm EA} C_{\rm EA} + \left(1 + g_{MP} r_{\rm out}\right) r_{o,\rm EA} C_{C1}} \tag{25}$$

where $g_{\rm MP}$ is the transconductance of M_P. The output resistance $r_{\rm out}$ of can be approximated as follows:

$$r_{\rm out} \approx r_{o,\rm MP} \| R_L \parallel \left(R_{F1} + R_{F2}\right) \tag{26}$$

where $r_{\rm o,MP}$ is the output resistance of M_P, and R_L is the load resistance. The frequency of secondary pole p_1 is approximated as follows:

$$f_{p_1} \approx \frac{1}{2\pi} \cdot \frac{C_{\rm EA} + \left(1 + g_{\rm MP} r_{\rm out}\right) C_{C1}}{r_{\rm out}\left[C_{\rm EA}\left(C_{C1} + C_L\right) + C_L C_{C1}\right]}. \tag{27}$$

The compensating capacitor C_{C1} pushes p_0 to a lower frequency and p_1 to a higher frequency. Two nulling resistors, R_{C1} and R_{C2}, are incorporated to introduce a left-half-plane zero z_1, compensating for the near-bandwidth phase reduction caused byp_1. The frequency of z_1 is given by

$$f_{z_1} \approx \frac{1}{2\pi} \cdot \frac{g_{\rm MP}}{2\pi\left(1 - g_{\rm MP} R_C\right) C_{C1}} \tag{28}$$

where R_C is the compensation resistor, two resistors (R_{C1} and R_{C2}) are designed for large and LL conditions.

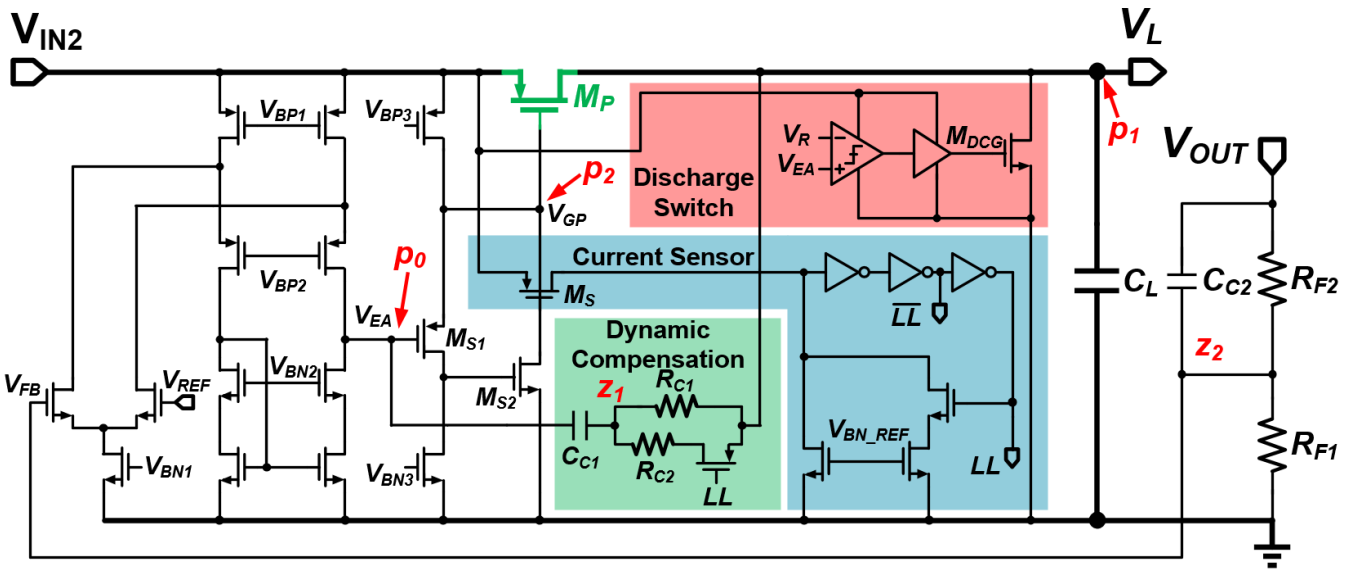

Fig. 11. Circuit implementation of LV LDO regulator.

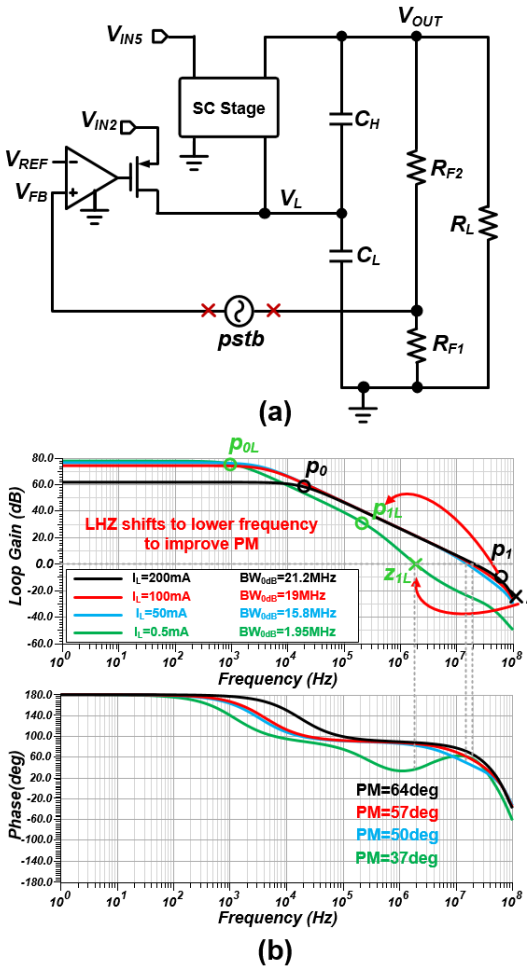

Fig. 12. (a) Modeling and (b) stability simulations of the proposed converter.

Fig. 12(a) shows the small signal model, and Fig. 12(b) plots the simulated Bode plot of the proposed sigma converter.

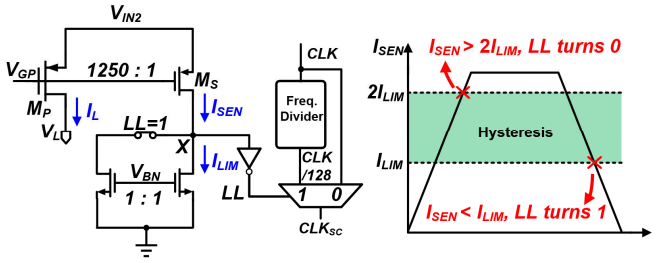

Fig. 13. Load current sensing and LL signal generation.

In this design, the loop bandwidth at maximum load is approximately 21 MHz, which is around 70 times higher than the switching frequency of the SC converter at 300 kHz. Although p_1 is pushed outside the unit-gain frequency (UGF) during heavy load and compensated by z_1, it shifts to a lower frequency p_{1L} at LL, which may reduce phase margin. A dynamic compensation scheme is implemented to adjust R_C and prevent instability actively. As illustrated in Fig. 13, when the load current falls below a preset boundary, the LL signal turns high, and R_{C2} is removed from R_C, and z_1 is shifted to a lower frequency z_{1L} alongside p_{1L}.

Another secondary pole p_2, is located at the gate of M_P and is given as follows:

$$f_{p_2} \approx \frac{1}{2\pi} \cdot \frac{1}{r_{o,\mathrm{SSF}}\left(g_{\mathrm{MP}} r_{\mathrm{out}} C_{\mathrm{GD,MP}} + C_{\mathrm{GS,MP}}\right)} \tag{29}$$

where $r_{\mathrm{o,SSF}}$ is the output resistance of SSF. The frequency of p_2 is approximately 50 MHz, which is compensated by the zero z_2 consisting of the feedback resistor R_{F2} and compensating capacitor C_{C2}, in the feedback network. The transfer function from output V_{OUT} to V_{FB} can be derived as follows:

$$\frac{v_{\mathrm{FB}}}{v_{\mathrm{OUT}}}(s) = \frac{1 + sR_{F2}C_{C2}}{1 + s\left(R_{F1} \parallel R_{F2}\right)C_{C2}}. \tag{30}$$

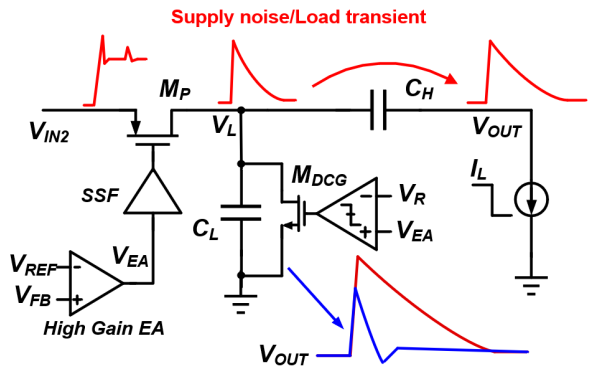

Fig. 14. Active discharge scheme at node V_L.

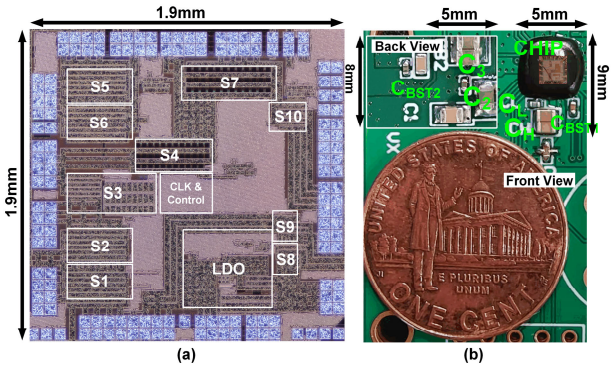

Fig. 15. (a) Chip micrograph and (b) PCB photograph of the proposed converter.

The feedback coefficient is 0.1 in this design. Therefore, pole p_3 in (30) is far beyondz_2. As a result, this configuration has minimal impact on the overall stability of the system.

A load current sensing circuit, as presented in Fig. 13, is implemented to improve LL efficiency by switching frequency modulation and to ensure the stability of the proposed converter by dynamic compensation. The circuit features a sensing transistorM_S that mirrors the load current from the pass device M_P at a ratio of 1:1250 to a sensing current I_{SEN}. I_{SEN} is therefore equal to I_L/1250 and competes with a preset current I_{LIM} at node X. When I_{SEN} is smaller than I_{LIM}, indicating that the converter is operating at LL mode, node X is pulled down, and LL turns high to "1." Subsequently, LL turns the output of a selector CLK_{SC} from the original 300 kHz to a 1/128$\times$ frequency divided from cascaded D-type flip-flops. To prevent mis-triggering, a hysteresis is introduced by an additional branch that mirrors the current at a 1:1 ratio. In LL mode, node X is pulled down by $2I_{\text{LIM}}$ so that I_L needs to exceed $2500I_{\text{LIM}}$ to turn LL low.

The power device is a PMOS transistor, which is not capable of sinking excessive current at node V_L. Voltage overshoots at V_L, caused by heavy-to-LL transients or supply noise coupled through M_P, may lead to overvoltage issues. To address this issue, an active discharge transistor M_{DCG} is implemented. As shown in Fig. 14, the voltage overshoot of V_L will be coupled to V_{OUT}, which is subsequently fed back to the EA of LDO.V_{EA} will saturate and be compared with a reference voltage V_R, and M_{DCG} will be turned on. Eventually, V_L and V_{OUT} can be pulled down at a much faster speed than passive discharge.

IV. Measurement Results

The proposed converter was fabricated by a 0.18 μm BCD process with all power switches, drivers, control circuits, and LDO integrated on-chip. Fig. 15 presents the chip micrograph and PCB photograph of the proposed converter. The total chip area of the proposed converter is 1.9 $\times$ 1.9 mm^2 with an active area of 2.31 mm^2. Three flying capacitors C_{1-3}, two output capacitors C_H and C_L, and three bootstrap capacitors $C_{\text{BST1}-3}$ are mounted on the PCB. The total system area is around 5 $\times$ 9 mm.

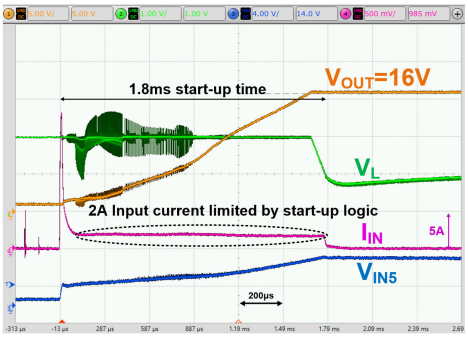

Fig. 16. Measured start-up waveforms of the proposed converter.

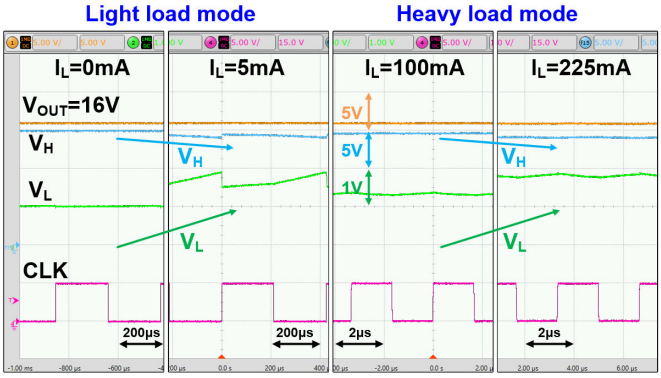

Fig. 17. Measured dc waveforms of the proposed converter at different load currents.

Fig. 16 presents the start-up waveforms of the proposed converter. With start-up design, the input currentI_{IN} is limited to approximately 2 A within a start-up time of 1.8 ms. During start-up, theR_{OUT} of SC is large, and the output of LDO (V_L, green) has to reach its maximum to minimize the error between V_{FB} and V_{REF}. After V_{OUT} (orange) reaches a preset voltage level (90% V_{OUT}), SUOK turns high. Subsequently, S_1, S_6, and S_9 are switching at their full capacity, as shown in Fig. 10. The $I_L R_{\text{OUT}}$ drop of SC decreases; therefore, V_L returns to a lower level as measured. The prototype converts a 5 V input into a regulated output of 16 V for the load current I_L from 0 to 225 mA. Fig. 17 presents the measured dc waveforms of V_H, V_L, and V_{OUT} at I_L of 0, 5, 100, and 225 mA,

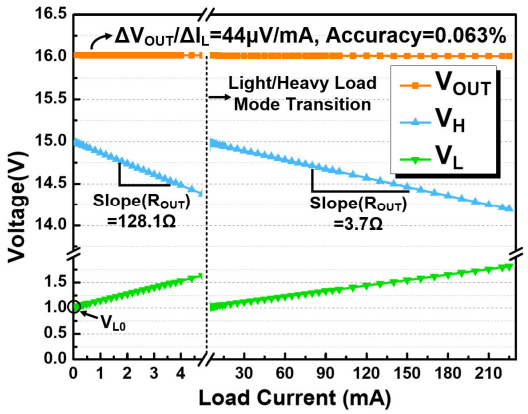

Fig. 18. Summary of measured dc voltages against load currents.

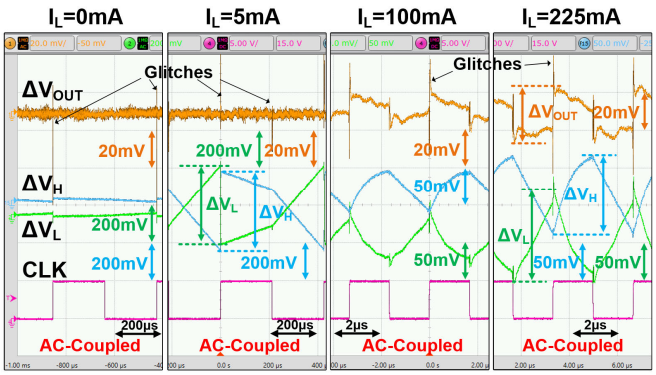

Fig. 19. Measured ac coupled waveforms of the proposed converter at different load currents.

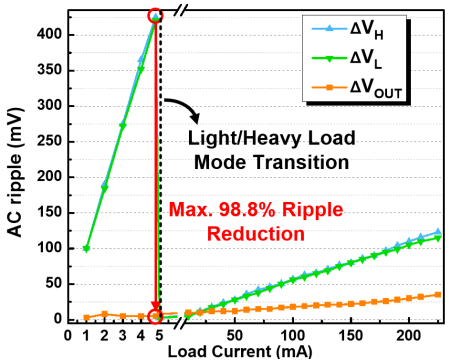

Fig. 20. Summary of measured ac ripples versus load currents.

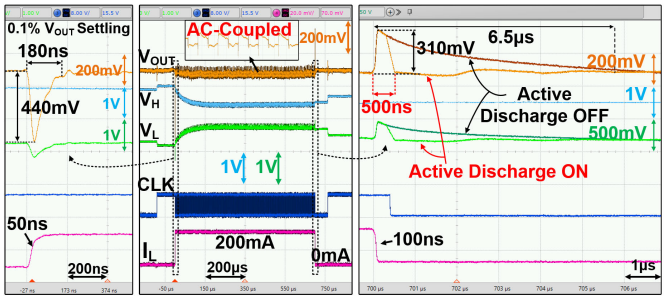

Fig. 21. Measured load transient response.

respectively. In both LL and heavy-load modes, V_H decreases as I_L increases due to the $I_L R_{\mathrm{OUT}}$ drop of the high-side SC converter, and V_L increases in the reverse to compensate for the voltage drop, thereby maintaining a constant V_{OUT}. The clock signal CLK verifies that the switching frequency changes from 2.3 kHz in LL mode (LL = 1) to 300 kHz in heavy-load mode (LL = 0). The dc voltage measurements are summarized in Fig. 18. Across the load current range of 0–225 mA, V_L effectively compensates for the impedance of the SC converter, ensuring an accurate regulation of V_{OUT} with a load regulation of 44 μV/mA. The maximum dc error of the converter is approximately 10 mV, which corresponds to 0.063% of V_{OUT}, attributed to the high gain of the LDO. The slope of the V_H curve with respect to I_L indicates that the R_{OUT} of the SC converter in LL mode and heavy load mode is 128.1 and 3.7 Ω, respectively.

Fig. 19 shows the ac-coupled voltage ripple waveforms of ΔV_H, ΔV_L, and ΔV_{OUT}. Similar to the dc waveforms, ΔV_H increases as I_L increases, while ΔV_L mitigates the output ripple ΔV_{OUT} by counteracting ΔV_H. It can be observed that ΔV_L is always in the opposite direction of ΔV_H, so that the output ripple voltage $\Delta V_{\mathrm{OUT}} = \Delta V_H + \Delta V_L$ was much canceled. In a result, output voltage ripple with less than 5 mV ripple in LL and 30 mV at heavy load was achieved, respectively. Fig. 20 summarizes the voltage ripple with respect to I_L. The LDO demonstrates effective mitigation of ΔV_H across the entire load range, which verifies that the bandwidth of the LV LDO is sufficient to track variation in ΔV_H. The ripple in LL mode is significantly larger than that in heavy-load mode due to 1/128 $\times$ lower switching frequency, as shown in Fig. 13. In heavy-load mode, the output ripple slightly increases as the load current increases due to the limited minimum dropout voltage of LDO$V_{\mathrm{DO,MIN}}$. The maximum measured ripple reduction ratio is 98.8% in LL mode.

Fig. 21 shows the measured load transient response of the proposed sigma SC converter. In a 0–200 mA I_L transition with a rising edge of 50 ns, the response time for a 0.1% V_{OUT} settling is 180 ns, and the voltage undershoot is 440 mV. In a 200–0 mA I_L transition with a falling edge of 100 ns, as shown on the right side of Fig. 21, the response time is 500 ns with an overshoot of 310 mV. Thanks to the active discharge circuit in the LDO, the converter's response time is significantly shortened from the original 6.5 μs (without active discharge) to 500 ns.

The measured efficiency of the proposed SC sigma converter is summarized in Fig. 22. In general, the efficiency increases with increasing load current. In the LL region ($I_L < 6$ mA), a comparison of conversion efficiency with and without LL mode is presented. With LL mode enabled, the efficiency increases by a maximum of 27%. The converter achieved a broad operational range with over 80% efficiency from 0.5 to 225 mA.

Fig. 23 presents the conversion efficiency of the SC sigma converter with different V_{OUT}. A peak efficiency of 94% is obtained at the maximum load I_L of 225 mA when V_{OUT} is 16 V, resulting in an output power of 3.6 W. Fig. 24 illustrates

TABLE II
COMPARISON OF THE STATE-OF-THE-ART WORKS

Works		CICC 2025[19]	JSSC 2021[6]	ISSCC 2023[8]	JSSC 2023[12]	ADM 8839 [4]	ISSCC 2014[5]	This Work
Process		180nm BCD	350nm CMOS	180nm BCD	180nm BCD	N/A	160nm	**180nm BCD**
Topology		Step-Up SC + Post HV LDO	Step-Up Hybrid	Step-Up Hybrid	Step-Up SC + Post HV LDO	Step-Up SC	Step-Up SC	**Step-Up SC + LV LDO Sigma**
V_{IN}		2.8-5 V	2-4.4V	2-6V	3.35-4.5V	2.7-4.2V	3.3V	**5V/2V**
V_{OUT}		10-15.5 V	9-20V	5-32V	±15.2V	±15V	16V	**15-16.8V**
Voltage Conversion Ratio (VCR)		4, 5, 6	2/(1-D)	1/D-2/D	3×, 4×, 5×	5×	6×	**3-3.36×**
I_O		3mA	10-250mA	5-50mA	0-20mA	0.01-0.15mA	0.1-7mA	**0-225mA**
P_{MAX}		58.7mW	5W	8W	0.6W	2.25mW	0.158W	**3.6W**
F_{SW}		Not reported	2MHz	1MHz	1.7-30kHz	60-140kHz	6.7MHz	**300kHz/2.3kHz**
Inductors		None	2×3.3µH	10µH	None	None	None	**None**
C_{OUT}		100nF	10µF	10µF	2×4.7µF	2×0.22µF	1µF	**2×22µF+4.7nF**
C_{FLY}		100nF	2×0.47µF	4.7µF	10µF+4×4.7µF	3×0.22µF	1µF+0.22µF	**3×10µF**
Peak Efficiency (η_{PEAK}) @ Power		91.5% @47mW	93.5% @1.89W	95.3% @1.5W	90.5% @120mW	87% @1.5mW	70.8% @60.8mW	**94.4% @3.6W**
Ripple Voltage @ Maximum I_L		50mV*	15mV @100mA	N. R.	28.7µV_{RMS} @20mA	180mV @0.15mA	160mV @7mA	**35mV @225mA**
Load Transient Response	Up Settling Time @I_O Step (Edge)	N. R.	400µs @230mA(1µs)	32µs @400mA	5µs @0.15mA(1µs)	4.2µs @20mA(50ns)	18µs @7mA(N/A)	**180ns @200mA(50ns)**
	Down Settling Time @I_O Step (Edge)	N. R.	400µs @230mA(1µs)	N. R.	4µs @0.15mA(1µs)	16.5µs @20mA(50ns)	22µs @7mA(N/A)	**500ns @200mA(100ns)**
Load Regulation $\Delta V_{OUT}/\Delta I_O$		N. R.	N. R.	N. R.	N. R.	3000mV/mA	40mV/mA	**0.044mV/mA**
Voltage Error @ Maximum I_O		N. R.	N. R.	N. R.	N. R.	3.98%	2.47%	**0.063%**
Active Chip Area		3mm²*	0.86mm²	5.5 mm²	8.74mm²	N/A	1.5mm²	**1.79mm²**
Power Density (Active Area) @ η_{PEAK}		0.02W/mm²*	2.19W/mm²	0.27W/mm²	0.014W/mm²	N/A	0.04W/mm²	**2.01W/mm²**
Power Density (System) @ η_{PEAK}		N. R.	90mW/mm³*	25mW/mm³*	4.8mW/mm³*	0.08mW/mm³	55mW/mm³*	**152mW/mm³**

* Estimated from papers. Total system volume is calculated with total component footprint multiplied by maximum component height.

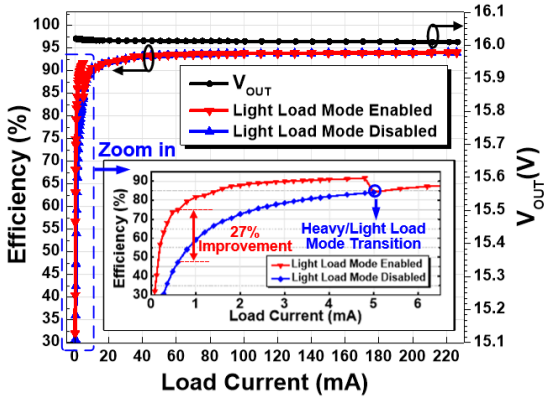

Fig. 22. Measured converter efficiency with respect to load current.

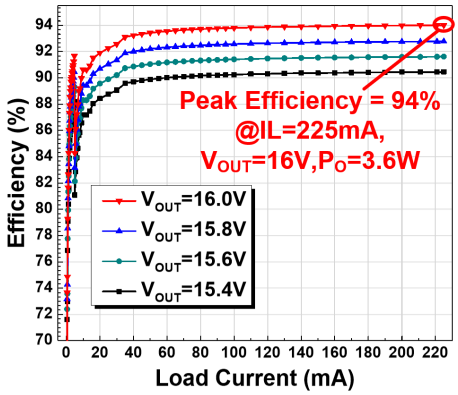

Fig. 23. Measured converter efficiencies of different V_{OUT}.

the power loss breakdown at 225 mA. The dominant loss is caused by the SC's R_{OUT}, which accounts for nearly 60% of the total loss.

Table II compares this work with state-of-the-art boost converters. This work achieves a maximum output power of 3.6 W and a peak efficiency of 94% at the peak output power. The LV LDO ensures a small voltage ripple of 35 mV, a fast load transient response time of 180 ns, and a high load regulation accuracy of 0.044 mV/mA. The power density at peak efficiency based on active chip area is 2.01 W/mm$_2$, while the power density relative to system volume is 152 mW/mm$_3$. Compared to previous works, this work is the only one to achieve sub-1 μs transient response time. Compared to the inductive designs [5], [8], the proposed converter achieves higher power density and faster transient speed. When compared with SC converter designs [3], [4], this work achieves much higher output power, resulting in at least a 2× enhancement in power density. Additionally, the load regulation accuracy is improved, compared to the post-LDO regulator in [11], while achieving faster transient response time by using LV LDO.

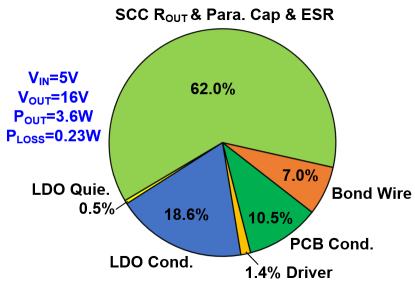

Fig. 24. Simulated power loss breakdown.

V. Conclusion

In summary, this work proposes an SC sigma boost converter, which incorporates an LV LDO regulator into the HV SC converter with input parallel and output series connection. The high-side SC converter achieves efficient and high-density power delivery, and the low-side LDO ensures accurate and fast load regulation. A load sensing circuit is incorporated for the dynamic compensation of the LDO and optimization of the SC converter's switching frequency, enhancing both LL efficiency and stability. An active discharge scheme is proposed to significantly reduce the load transient response and protect the LV LDO from overvoltage conditions. The prototype boosts a 5 V input to a 16 V output, delivering a maximum load current of 225 mA with a peak efficiency of 94.4%. The LDO compensates for the impedance of the SC converter, contributing to the high load regulation accuracy of 44 μV/mA. The high-bandwidth LV LDO ensures a small output voltage ripple of less than 35 mV and facilitates fast load transients of 180 and 500 ns during up and down 200 mA load current transitions, respectively. The inductor-less design further enhances the power density of 152 mW/mm$_3$.

References

[1] D. Bronzi, F. Villa, S. Tisa, A. Tosi, and F. Zappa, "SPAD figures of merit for photon-counting, photon-timing, and imaging applications: A review," *IEEE Sensors J.*, vol. 16, no. 1, pp. 3–12, Jan. 2016.

[2] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up DC–DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9143–9178, Dec. 2017.

[3] S. R. Sanders, E. Alon, H.-P. Le, M. D. Seeman, M. John, and V. W. Ng, "The road to fully integrated DC–DC conversion via the switched-capacitor approach," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4146–4155, Sep. 2013.

[4] *ADM8839 Datasheet and Product Info — Analog Devices*. Accessed: Aug. 13, 2024. [Online]. Available: https://www.analog.com/en/products/adm8839.html#part-details

[5] R. Karadi and G. V. Pique, "4.8 3-phase 6/1 switched-capacitor DC–DC boost converter providing 16V at 7 mA and 70.3% efficiency in 1.1 mm3," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 92–93.

[6] M. Huang, Y. Lu, T. Hu, and R. P. Martins, "A hybrid boost converter with cross-connected flying capacitors," *IEEE J. Solid-State Circuits*, vol. 56, no. 7, pp. 2102–2112, Jul. 2021.

[7] W. C. Liu, P. H. Ng, and R. Pilawa-Podgurski, "A three-level boost converter with full-range auto-capacitor-compensation pulse frequency modulation," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 744–755, Mar. 2020.

[8] M. Kim et al., "8.9 A 96.5% peak efficiency duty-independent DC–DC step-up converter with low input-level voltage stress and mode-adaptive inductor current reduction," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 160–162.

[9] S.-J. Lee et al., "30.5 A 95.3% 5V-to-32V wide range 3-level current mode boost converter with fully state-based phase selection achieving simultaneous high-speed V_{CF}balancing and smooth transition," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 446–448.

[10] *LM27761 Data Sheet, Product Information and Support*. Accessed: Aug. 16, 2024. [Online]. Available: https://www.ti.com.cn/cn/lit/ds/symlink/lm27761.pdf?ts=1726740378607

[11] *LTC1550/LTC1551—Low Noise, Switched Capacitor-Regulated Voltage Inverters*. Accessed: Aug. 14, 2024. [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/15501fa.pdfmymargin

[12] M.-W. Ko, H. Han, and H.-S. Kim, "A bipolar-output switched-capacitor DC–DC boost converter with residual-energy-recycling regulation and low dropout post-filtering techniques," *IEEE J. Solid-State Circuits*, vol. 58, no. 5, pp. 1400–1413, May 2023.

[13] J. Sun, M. Xu, D. Reusch, and F. C. Lee, "High efficiency quasi-parallel voltage regulators," in *Proc. 23rd Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2008, pp. 811–817.

[14] X. Yang et al., "A high-efficiency wide output range reconfigurable capacitive-sigma DC–DC converter," *IEEE J. Solid-State Circuits*, vol. 59, no. 5, pp. 1532–1542, May 2023.

[15] X. Yang et al., "A 5V input 98.4% peak efficiency reconfigurable capacitive-sigma converter with greater than 90% peak efficiency for the entire 0.4 1.2V output range," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 65, Feb. 2022, pp. 108–110.

[16] M. Ursino, R. Rizzolatti, G. Deboy, S. Saggini, and K. Zufferli, "Sigma converter family with common ground for the 48 V data center," *IEEE Trans. Power Electron.*, vol. 38, no. 9, pp. 10997–11009, Sep. 2023.

[17] C. Hu, X. Huang, X. Liu, S. Du, X. Liu, and J. Jiang, "31.7 A 3.6W 16V-output 180ns-response-time 94%-efficiency SC sigma converter with output impedance compensation and ripple mitigation for LiDAR driver applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 508–510.

[18] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[19] W. Zhu, X. Sun, X. Zhang, and C. Huang, "A multi-level power management architecture for battery-powered SPAD drivers with supply intrinsic quenching and 10-ns dead time," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2025, pp. 1–3.

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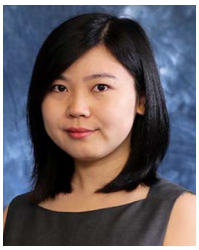

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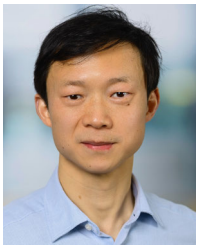

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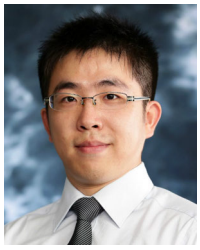

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