A β-Compensated NPN-Based Temperature Sensor With ±0.1 °C (3σ) Inaccuracy From -55 °C to 125 °C and 200fJ · K² Resolution FoM

Toth, Nandor G.; Makinwa, Kofi A.A.

DOI
10.1109/JSSC.2024.3440071

Publication date
2024

Document Version
Final published version

Published in
IEEE Journal of Solid-State Circuits

A β-Compensated NPN-Based Temperature Sensor With ± 0.1 °C (3σ) Inaccuracy From -55 °C to 125 °C and 200fJ $\cdot$ K^2 Resolution FoM

Nandor G. Toth, *Graduate Student Member, IEEE*, and Kofi A. A. Makinwa, *Fellow, IEEE*

***Abstract*— This article presents a CMOS temperature sensor that achieves both state-of-the-art energy efficiency and accuracy. An NPN-based front end uses two resistors to efficiently generate a PTAT and CTAT current, whose ratio is then digitized by a continuous-time (CT) $\Delta\Sigma$-modulator. A β-compensation technique is used to mitigate base current errors associated with the NPN's finite β. Component mismatch and $1/f$ noise are mitigated by applying chopping and dynamic element matching (DEM), while the spread in V_{BE} and the ratio of the two resistors are digitally trimmed at room temperature (RT). Fabricated in a 0.18-μm CMOS process, the sensor draws 2.5 μA from a supply voltage ranging from 1.4 to 2.2 V. Measurements on 40 samples show that it achieves an inaccuracy of ± 0.1 °C (3σ) from -55 °C to 125 °C. Furthermore, it is both highly energy efficient, with a resolution figure of merit (FoM) of 200fJ $\cdot$ K^2, as well as very compact, occupying only 0.07 mm^2.**

***Index Terms*— β-compensation, continuous-time (CT) $\Delta\Sigma$-modulator, current-mode readout, NPN-based temperature sensor, resistor ratio calibration.**

I. Introduction

OVER the last two decades, BJT-based temperature sensors have consistently demonstrated their ability to achieve high accuracy [less than ± 0.2 °C (3σ) error from -55 °C to 125 °C] after a single room temperature (RT) trim [1]. In integrated frequency references, such high-accuracy temperature sensors are used to compensate for the temperature dependence of their analog subblocks [2], [3], [4]. Since the temperature sensor's noise will then manifest itself as phase noise, such sensors must also achieve high resolution in an energy-efficient manner.

To achieve high accuracy, BJT-based sensors have typically combined switched-capacitor (SC) $\Delta\Sigma$-modulators [5], [6], [7] with precision techniques, such as chopping and dynamic element matching (DEM). In this manner, inaccuracies as low as ± 0.06 °C (3σ) from -55 °C to 125 °C have been achieved [8]. However, their resolution is then dominated by kT/C noise, which typically limits their energy efficiency, as expressed by the resolution figure of merit (FoM) [9], to several pJ $\cdot$ K^2 [1].

More recently, continuous-time (CT) current-mode readout circuits have been proposed [10], [11]. These convert the temperature-dependent voltages generated by a BJT-based front end into currents, which can then be digitized by a CT $\Delta\Sigma$-modulator without introducing kT/C noise. In this manner, an NPN-based design achieved a state-of-the-art resolution FoM of 190 fJ $\cdot$ K^2 [12]. Unfortunately, its inaccuracy was not specified. In previous work, we reported a PNP-based current mode design that achieved an inaccuracy of ± 0.1 °C (3σ) from -55 °C to 125 °C, as well as a resolution FoM of 850 fJ $\cdot$ K^2 [11]. The goal of this work is to design a current-mode temperature sensor, whose inaccuracy is similar to that of [11], while also achieving an energy efficiency similar to that of [12].

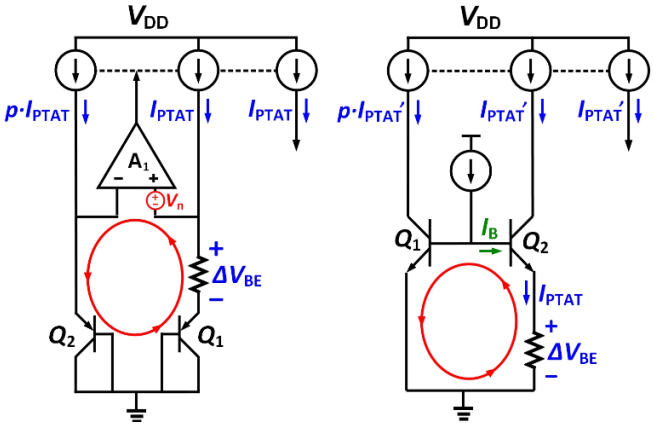


Fig. 1. Simplified circuit diagram of a current-mode PNP-based front end (left) and NPN-based front end (right).

Fig. 1 (left) shows a simplified circuit diagram of the PNP-based front end used in [11]. Two PNPs are biased at a current ratio p to generate ΔV_{BE}. The virtual ground of opamp A_1 closes a voltage loop comprising two base–emitter voltages and the voltage drop across a resistor, thus establishing $I_{PTAT} = \Delta V_{BE}/R$. This current can then be accurately mirrored to the input of a $\Delta\Sigma$-modulator. However, the input-referred noise V_n of A_1 will then be added to ΔV_{BE}. Since this noise will impact the sensor's resolution, a significant amount of power must be dissipated in A_1, which reduces the sensor's energy efficiency.

A simplified circuit diagram of an NPN-based front end is shown in Fig. 1 (right). Since the collectors of the NPNs

Manuscript received 12 May 2024; revised 1 July 2024; accepted 31 July 2024. Date of publication 26 August 2024; date of current version 25 November 2024. This article was approved by Associate Editor Drew Hall. This work was supported by Analog Devices Inc., (ADI). *(Corresponding author: Nandor G. Toth.)*

The authors are with the Electronic Instrumentation Laboratory, Microelectronics Department, Faculty of Electrical Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: N.G.Toth@tudelft.nl).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2024.3440071.

Digital Object Identifier 10.1109/JSSC.2024.3440071

are not tied to the substrate, a similar voltage loop can be made without a noisy opamp. This reduces both the sensor's power consumption and noise [12]. However, due to the finite current gain (β) of the NPNs, their collector current is only approximately equal to I_{PTAT}. As a result, simply mirroring this current to the input of the $\Delta\Sigma$-modulator, as in [12], will incur significant β-dependent errors. In addition, the vertical NPNs available in the target 0.18-μm process are more stress-sensitive than their PNP counterparts [13]. Furthermore, the leakage of the reverse-biased junction formed by their deep n-well collectors and the substrate can cause significant collector current errors at high temperatures [14].

This article, an extended version of [15], presents a current-mode NPN-based front end that uses a β-compensation technique to mitigate β-dependent errors and thus achieves both excellent energy efficiency and accuracy. DEM is applied to mitigate current mirror and BJT mismatch, while resistor-ratio mismatch is mitigated by a low-cost calibration scheme. The resulting sensor achieves a resolution FoM of 200fJ $\cdot$ K^2 and an inaccuracy of ± 0.1 °C (3σ) from -55 °C to 125 °C after an RT trim, both of which represent the state-of-the-art performance.

The rest of this article is organized as follows. Section II discusses various ways of dealing with β-dependent errors in current-mode front ends. Section III describes the design of the proposed sensor and its error-reduction techniques in detail. Its circuit implementation is discussed in Section IV. Section V presents the measurement results and compares them to the state of the art. This article ends with conclusions.

II. β-Compensation for NPN-Based Front Ends

The current-mode BJT-based temperature sensors typically use a $\Delta\Sigma$-modulator to determine the temperature-dependent ratio of a PTAT current (I_{PTAT}) and a CTAT current (I_{CTAT}) [11], [12]. Since the sensitivity of ΔV_{BE} is an order of magnitude lower than that of V_{BE} (-1.9 mV/K), the accuracy of I_{PTAT} usually determines the overall accuracy of such sensors.

In Fig. 2, two NPNs with an emitter area ratio of r are biased at a unit current ratio p via their collectors to generate the following signals:

$$V_{\mathrm{BE}} = n_e \frac{kT}{q} \ln\left(\frac{I_{\mathrm{C}}}{I_{\mathrm{S}}}\right) \tag{1}$$

$$\Delta V_{\mathrm{BE}} = V_{\mathrm{BE2}} - V_{\mathrm{BE1}} = n_e \frac{kT}{q} \ln(pr) \tag{2}$$

where n_e is the BJT's nonideality factor, k is the Boltzmann constant, q is the unit electron charge, and I_{C} and I_{S} are the BJT's collector and saturation current, respectively. Resistor R_1 then sets the emitter current of Q_1 to $I_{\mathrm{PTAT}} = \Delta V_{\mathrm{BE}}/R_1$. The base current of the two NPNs ($I_{\mathrm{B1}} + I_{\mathrm{B2}}$) is supplied by a buffer to avoid disturbing the collector currents.

However, in a current-mode temperature sensor, the signal of interest is the current that is mirrored to the ADC (I_{ADC}), which is proportional to I_{C}. Due to the finite β of Q_1 ($\sim$20 at RT), its base current (I_{B1}) will result in a β-dependent error

$$I_{\mathrm{ADC}} = \frac{\Delta V_{\mathrm{BE}}}{R_1} - I_{\mathrm{B1}} = I_{\mathrm{PTAT}} \frac{\beta}{\beta + 1}. \tag{3}$$

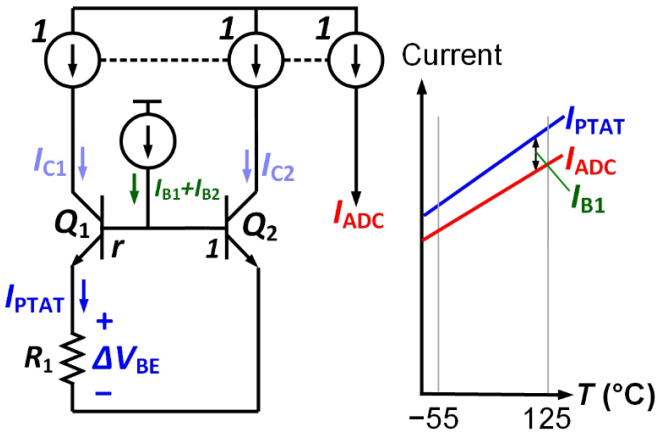


Fig. 2. Circuit diagram of a current-mode NPN-based front end.

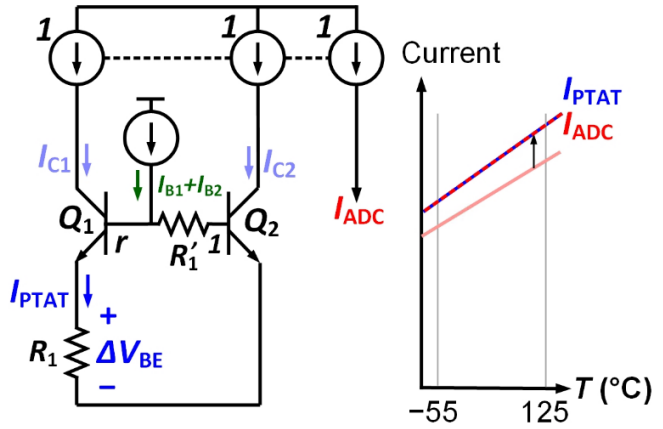


Fig. 3. Circuit diagram of a current-mode NPN-based front end with R-based β compensation.

Unfortunately, this error is non-PTAT and so will only be partially mitigated by the PTAT trim that is generally used to correct for V_{BE} spread. In the target 0.18-μm CMOS process, simulations show that this β-dependent error will result in a worst case temperature error of ± 0.65 °C from -55 °C to 125 °C after an RT PTAT trim.

One way of compensating such β-dependent errors is to place a second resistor R_1' in series with the base of Q_2 [16], as shown in Fig. 3. This adds an I_{B2} component to the voltage across R_1, which compensates for the I_{B1} component that is effectively subtracted by Q_1, resulting in the following expression:

$$I_{\mathrm{ADC}} = \frac{\Delta V_{\mathrm{BE}} + I_{\mathrm{B2}} R_1'}{R_1} - I_{\mathrm{B1}} \approx I_{\mathrm{PTAT}}\left(1 - \frac{\Delta\beta}{\beta^2}\right). \tag{4}$$

However, as shown in Fig. 4, an NPN's β also depends on its collector current density (J_{c}). Since the NPNs must be biased at a certain J_{C} ratio to generate ΔV_{BE}, this means that there will always be a difference ($\Delta\beta$) in the βs of Q_1 and Q_2. Since $\Delta\beta$ varies over temperature and process corners, the resulting error in I_{ADC} still cannot be removed by a PTAT trim and results in a worst case corner spread of ± 0.2 °C ($r = 7$).

In this work, a β-compensation technique is proposed that uses an I_{B}-current mirror to compensate for the missing base current. As shown in Fig. 5, a copy of the average of I_{B1}

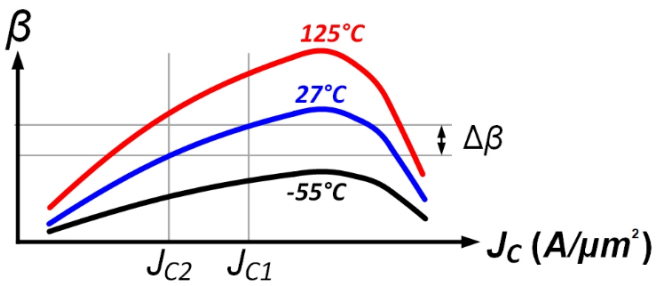


Fig. 4. NPN's β versus its collector current density at different temperatures.

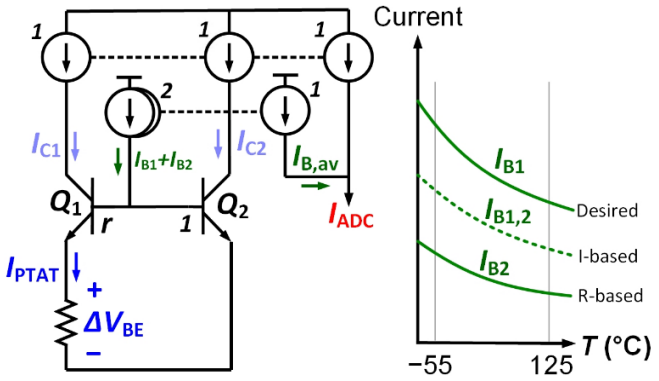


Fig. 5. Circuit diagram of the front end with I-based β compensation (left) and a comparison of the β-compensation current for I- and R-based β compensation.

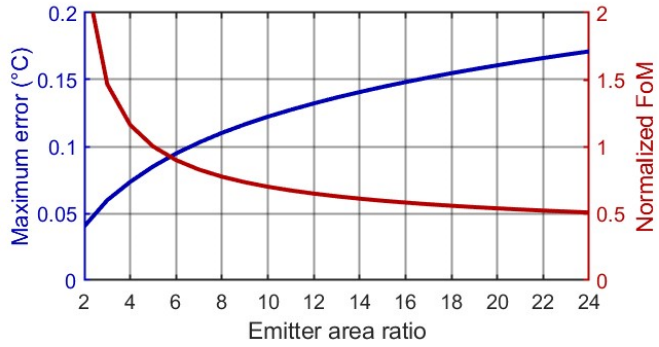


Fig. 6. Maximum temperature error after trimming and normalized resolution FoM versus emitter area ratio.

and I_{B2} ($I_{B,av}$) can be obtained by supplying the NPN's base currents via a 2:1 current mirror. I_{ADC} can then be expressed as follows:

$$I_{ADC} = \frac{\Delta V_{BE}}{R_1} - I_{B1} + \frac{I_{B1} + I_{B2}}{2} \approx I_{PTAT}\left(1 - \frac{\Delta\beta}{2\beta^2}\right). \quad (5)$$

It can be observed that this results in a $\Delta\beta$ error that is only half that of the R-based compensation circuit shown in Fig. 3.

According to (2), maximizing r increases ΔV_{BE}, which, in turn, improves energy efficiency. However, it also increases the J_C ratio, resulting in a larger $\Delta\beta$ error and worse accuracy (Fig. 4). Fig. 6 illustrates the simulated tradeoff between inaccuracy (after an RT PTAT trim) and resolution FoM (normalized at $r = 5$). For the proposed sensor, $r = 7$ was chosen as a good compromise, resulting in a worst case trimmed inaccuracy of ± 0.1 °C from -55 °C to 125 °C.

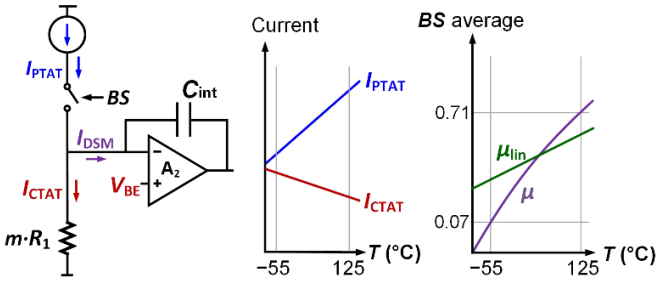


Fig. 7. Simplified circuit diagram of the single-level DAC and the current signals and bitstream average versus temperature.

III. Proposed Sensor Topology and Techniques

As in [11], a digital representation of temperature is obtained by balancing a fixed I_{CTAT} with the variable output of an I_{PTAT} DAC, which is controlled by the bitstream of a $\Delta\Sigma$-modulator. As discussed in Section II, an accurate I_{PTAT} is generated by an NPN-based front end with the help of the proposed β-compensation technique, while, as shown in Fig. 7, an accurate I_{CTAT} is generated by using the modulator's 1st integrator to force V_{BE} over a resistor $R_2 = mR_1$ [17].

A. DAC and Current Scaling

As shown in Fig. 7, the sensor employs a 1-bit DAC that switches between 0 and I_{PTAT}. Compared to the DAC used in [11], which switches between I_{PTAT} and $4I_{PTAT}$, this reduces the peak DAC current by 4×. It also reduces the integrator's input current (I_{DSM}) proportionally and thus the power dissipation of its opamp A_2, which must be designed to source/sink this current. With the chosen topology, a bitstream is generated, whose average μ can be expressed as follows:

$$\mu = 1 - \frac{1}{m} \cdot \frac{V_{BE}}{\Delta V_{BE}} = 1 - \frac{X}{m} \quad (6)$$

where $X = V_{BE}/\Delta V_{BE}$. To ensure that I_{PTAT} and I_{CTAT} are balanced properly over the targeted temperature range (Fig. 7, middle), the coefficient m is set to 24, so that μ ranges from 0.07 to 0.71 over the military temperature range (Fig. 7, right). Compared to [11], where μ ranges from 0.08 to 0.9, the OSR of the 2nd order $\Delta\Sigma$-modulator must be increased by ~10% to maintain the same SQNR, which is acceptable considering the achieved reduction in DAC complexity and power. As explained in [8], μ can be linearized by applying the following formula:

$$\mu_{lin} = \frac{\alpha}{\alpha + X} = \frac{\alpha}{\alpha + 24(1 - \mu)} \quad (7)$$

where α is a digital constant.

B. Dynamic Error Reduction

Fig. 8 shows a block diagram of the proposed sensor. To achieve high accuracy, various dynamic error correction techniques are applied. As in [3], the integrator's opamp A_2 is chopped at f_s to remove both its offset and $1/f$ noise. Furthermore, the mismatch of the I_C- and I_B-current mirrors is again mitigated by bitstream-controlled (BSC) DEM at f_s [18].

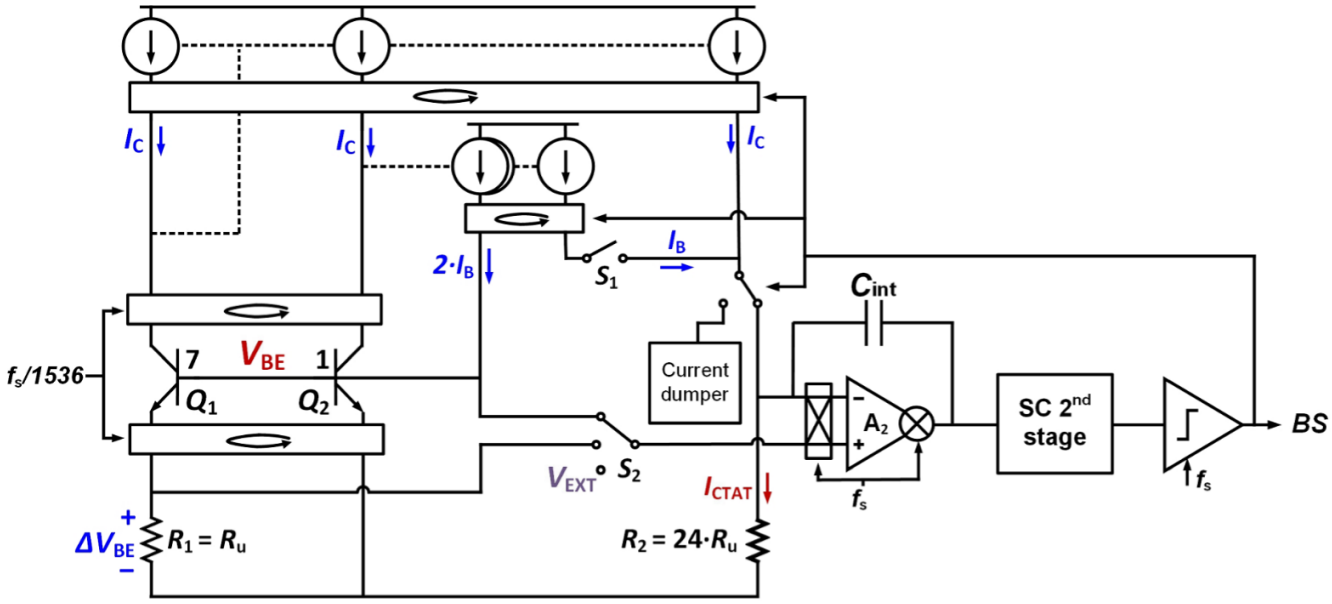


Fig. 8. Block diagram of the full sensor.

Since $p = 1$ and $I_{DAC} = I_{PTAT}$, only three I_C- and I_B-current sources require DEM, which simplifies the digital logic and ensures a small residual error. A current dumper is added to reduce DAC-related switching transients [11].

NPN mismatch is mitigated by applying barrel-shifting DEM. Since the NPNs have a shared base connection, this is implemented by switches placed at the collector and emitter of each unit NPN ($2 \times 2\ \mu$m). A full DEM cycle, which consists of eight states, then takes place at $f_s/1536$, thus ensuring that the full conversion of 3072 cycles ($2 \cdot 1536$) is not limited by quantization noise. The choice of such a low DEM frequency results in negligible quantization noise folding.

C. Resistor Calibration

In [11], the resistor ratio m is calibrated by reconfiguring the $\Delta\Sigma$-modulator to extract the resistor ratio, after which the mismatch is compensated in the digital domain. This requires two conversions, during which the ambient temperature must be stable to avoid readout errors. In this work, this foreground calibration is implemented by connecting the integrator to ΔV_{BE} via the multiplexer S_2 (Fig. 8). The current flowing through R_2 will then be I_{PTAT}/m, where m is the resistor ratio. It follows that the modulator now balances I_{PTAT} against I_{PTAT}/m, resulting in the following expression for the bitstream average:

$$\mu_{RCAL} = 1 - \frac{I_{PTAT}/m}{I_{PTAT}} = 1 - \frac{1}{m} \approx 0.96 \tag{8}$$

from which m can be extracted. The total integrated thermal noise is sufficiently low ($<0.005\%$) after a 0.1-s conversion. Note that a second-order $\Delta\Sigma$-modulator is still stable for dc signals close to full scale. Any deviations in m can then be compensated by applying the following formula in the digital domain:

$$\mu_{\text{calibrated}} = \frac{\mu - 1}{24 \cdot (1 - \mu_{RCAL})} + 1. \tag{9}$$

Since temperature variations affect I_{PTAT} and I_{PTAT}/m in a similar manner, ambient temperature drift does not cause errors, greatly relaxing the requirements on temperature stability during calibration. Furthermore, the calibration can be performed in about 0.1 s, making it a low-cost operation.

D. Voltage Calibration

Voltage calibration [19] is also implemented as a low-cost alternative to RT calibration. It involves connecting (via S_2) a known external reference voltage V_{EXT} to the integrator instead of V_{BE}. This allows ΔV_{BE}, and therefore the die temperature, to be extracted using (2), after which any errors can be digitally trimmed. The accuracy of the estimated die temperature is limited by the spread in the NPN's nonideality factor n_e and by the $\Delta\beta$-dependent error in (4). However, voltage calibration is a fast and low-cost alternative to a traditional temperature calibration since it requires no external temperature reference and no additional time to allow it to achieve thermal equilibrium with the die [11].

IV. Circuit Implementation

A. Front End

Fig. 9 shows a more detailed circuit diagram of the proposed front end. The three I_C-current mirrors are implemented as cascoded pMOS transistors biased in strong inversion ($g_m/I_D = 2.5$). This ensures good matching, large r_{out} ($>250\ \mathrm{G}\Omega$ over PVT), as well as a low noise contribution. As a result, their noise contribution to μ is only 25% at RT, so that R_1 and the NPNs dominate the noise, contributing 50% and 25%, respectively. As discussed in the previous section, DEM is applied to further improve their matching. Since the virtual ground of the ADC is at ΔV_{BE} during resistor calibration, placing the DEM switches at the drains of the cascodes would cause large switching transients during DEM transitions. For this reason, the DEM switches are placed between the current

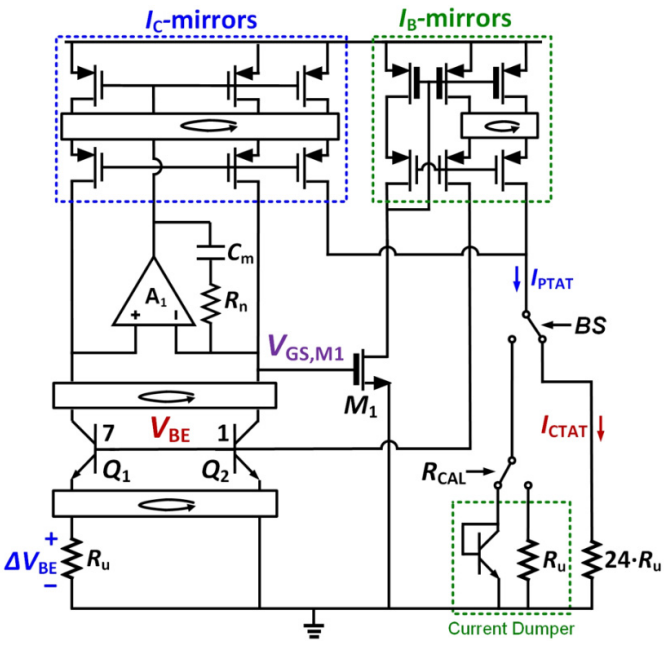


Fig. 9. Circuit diagram of the front end and the DAC.

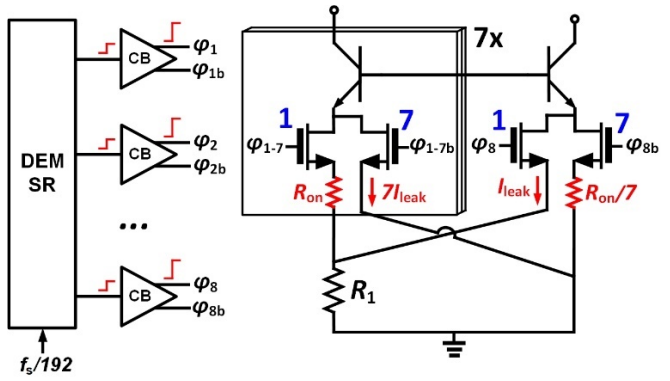


Fig. 10. Circuit diagram of the NPN-DEM switches and their signal generation.

sources and the cascodes [12]. This ensures that the voltages around the DEM switches are identical irrespective of the ADC's virtual ground.

The I_C-current mirrors are biased by opamp A_1. Since the biasing loop does not directly affect I_{PTAT}, its noise and error contribution is negligible. Therefore, it is designed as a simple and low-power five-transistor OTA. It realizes a loop-gain bandwidth of ~120 kHz at RT, resulting in switching transients that contribute less than 10-mK error. A Miller capacitor (C_m = 800 fF) and a nulling resistor (R_n = 450 kΩ) are added to stabilize the loop. A_1 also ensures that the NPN's collector voltages are identical, which reduces static errors in the collector current ratio related to the NPN's early effect ($V_A \approx 45$ V at RT) and the pMOS's finite r_{out}. Due to its small error and noise contribution, there is no need to chop A_1.

As discussed in Section II, the NPN's base current I_B is added to I_C to obtain an accurate copy of I_{PTAT}. Like the I_C-current mirrors, this is achieved by using cascoded PMOS current sources biased in strong inversion. The same BSC-DEM signals are used to control the cascoded DEM switches. As shown in Fig. 9, the I_B-current mirrors are biased using an additional I_B branch, which sets the collector voltages to V_{GS} of an HV_t NMOS ($V_{GS,M1}$). This voltage tracks V_{BE} and ensures that V_{CE} is large enough (>300 mV at 125 °C) to keep the NPNs saturated over the temperature range. Since the bias current of M_1 has a negligible effect on I_{PTAT}, the corresponding current source is not incorporated in the DEM cycle. Unlike the design in [7], this biasing circuit does not need an additional opamp. Furthermore, it requires a voltage headroom of only $V_{BE} + V_{DS}$, which allows the current sources to be biased further into strong inversion.

Since the NPN DEM switches at the emitters are in series with R_1, their IR drop directly affects ΔV_{BE}, thus requiring a low R_{ON}. Additionally, insufficient R_{OFF} at high temperatures would cause large leakage currents (I_{leak}), resulting in errors in the generated I_{PTAT}. A combination of high R_{OFF} and low R_{ON} is achieved by using I/O switches controlled by clock-boosted (CB) signals, which are generated by a DEM shift register (SR) (Fig. 10). As a result, the worst case R_{ON} and R_{OFF} (at 125 °C, V_{DD} = 1.4 V) are 5 kΩ and 75 GΩ, respectively. To cancel the effect of their R_{ON} to the 1st order, the switches are sized at a 1:7 ratio corresponding to the currents they conduct. This results in an absolute error of 80 mK, which will be further reduced by resistor calibration.

B. Delta-Sigma Modulator

The current signals are digitized by a 1-bit, 2nd-order, CIFF ΔΣ-modulator with a CT 1st integrator. It operates at a clock frequency of 80 kHz and an OSR of 3072, resulting in a conversion time of 38.4 ms.

As in [11], the 1st integrator is designed as a two-stage opamp with a single-ended common-source 2nd stage. The integrator's input common-mode voltage can be V_{BE} (normal operation) as well as ΔV_{BE} (resistor calibration). For this reason, the 1st stage of the opamp is designed as a PMOS-input folded-cascode, which can operate over a large input voltage range. A Miller capacitor (230 fF) and nulling resistor (200 kΩ) are used for stability. The opamp has a dc gain of 110 dB, resulting in a gain error much less than 0.01% as is required during resistor calibration. A GBW of 350 kHz ensures that the error resulting from switching transients is below 30 mK during normal operation and less than 0.01% required during resistor calibration. Since the DAC currents are reduced by 4× compared to [11], C_{int} (15 pF) could be reduced proportionally, resulting in significant area savings. The DAC switches are implemented with I/O devices, which exhibit negligible leakage at high temperatures. As in [11], the 2nd integrator is implemented as an area-efficient SC integrator using 3.5× less power and 8× less area than the 1st integrator.

The DAC current dumper generates a copy of the virtual ground from the unused DAC current. Under normal operation, V_{BE} is generated using a unit-NPN load, while during resistor calibration, a unit resistor is used to generate ΔV_{BE} (Fig. 8).

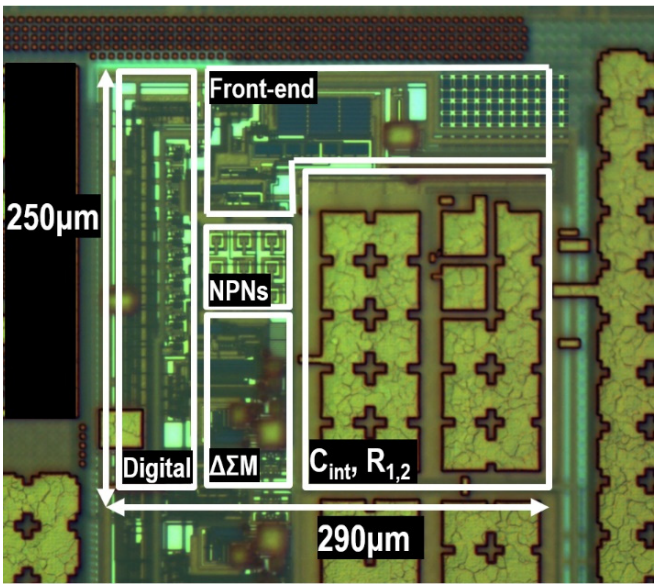


Fig. 11. Micrograph of a single sensor.

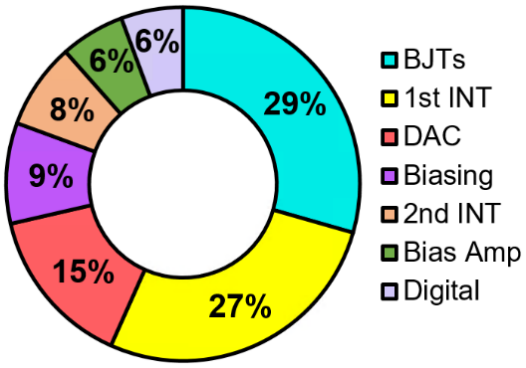


Fig. 12. Power breakdown of the sensor.

V. Measurement Results

The proposed temperature sensor was fabricated in a standard 0.18-μm CMOS process. The die photograph is shown in Fig. 11. Each die contains two sensors, so that differential measurements can be performed to cancel ambient temperature drift [20]. All digital control signals are generated by a digital controller clocked at 320 kHz. For flexibility, the nonlinearity removal and decimation filter were implemented off-chip.

A. Area and Power Consumption

A single sensor draws 2.5 μA from a 1.4-V supply at RT. Fig. 12 shows a detailed power distribution of the proposed sensor, which is dominated by the power dissipation of the BJTs and the 1st integrator. Since the bias amplifier A_1 has relaxed noise requirements, its power dissipation is negligible.

The proposed sensor occupies only 0.07 mm^2. Fig. 13 shows that this area is dominated by resistors (R_1 and R_2) and capacitors (C_{int1} and charge pump). As shown in [11], the addition of a decimation filter, polynomial engine, and an SPI interface would not significantly increase the sensor's area and power consumption.

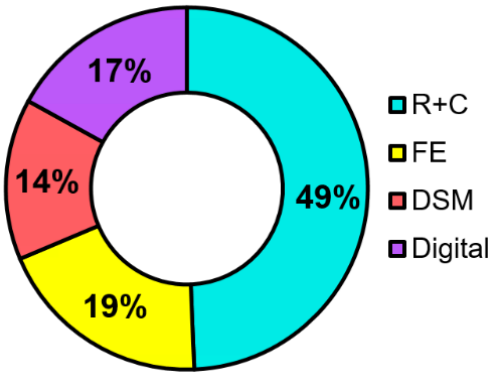


Fig. 13. Area breakdown of the sensor.

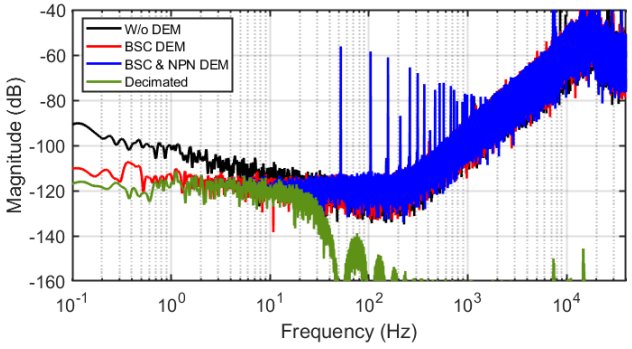


Fig. 14. FFT of the bitstream.

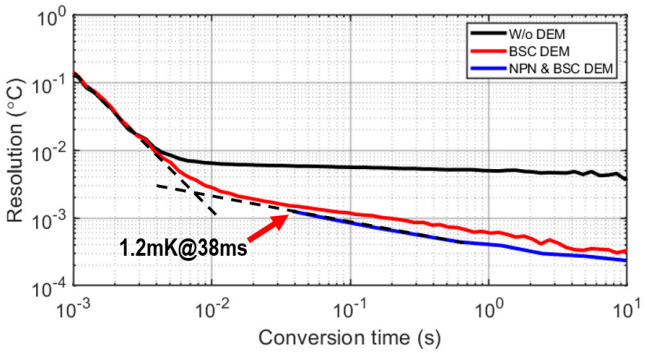


Fig. 15. Temperature resolution plotted versus conversion time.

B. FFT and Resolution

Fig. 14 shows a fast Fourier transform (FFT) of the bitstream when the modulator is operating in the free-running mode. It can be seen that most of the $1/f$ noise comes from the PMOS current mirrors, followed by the NPNs. After applying DEM to both, a $1/f$ noise corner well below 100 MHz along with a quantization noise corner of 200 Hz was achieved. The remaining tones are related to the low-frequency NPN DEM and are suppressed by the notches of the sinc^2 decimation filter. As shown in Fig. 15, after applying both types of DEM, the sensor achieves a thermal-noise limited resolution of 1.2 mK (σ) in 38 ms, which results in a resolution FoM of 200 fJ $\cdot$ K^2.

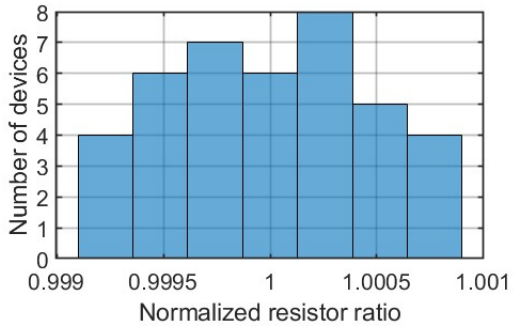


Fig. 16. Histogram of the normalized resistor ratios extracted from 40 sensors.

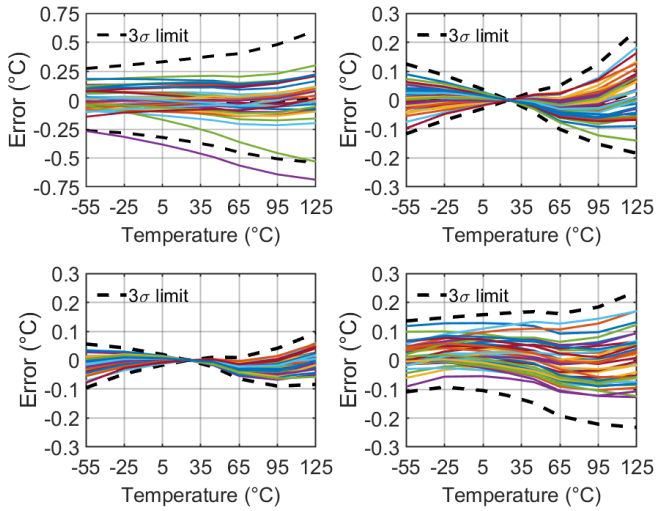


Fig. 17. Measured temperature spread of 40 sensors before trimming (top left), with RT trim (top right), with RT trim and resistor-ratio calibration (bottom left), and with voltage- and resistor-ratio calibration (bottom right).

TABLE I
ACCURACY-IMPROVEMENT TECHNIQUES

BJT DEM	CHOP	I_C-CM DEM	I_B-CM DEM	R-CAL	Trimmed Inacc. (3σ)
OFF	ON	ON	ON	ON	±1.5°C
ON	**OFF**	ON	ON	ON	±1.2°C
ON	ON	**OFF**	OFF	ON	±1.0°C
ON	ON	ON	**OFF**	ON	±0.2°C
ON	ON	ON	ON	**OFF**	±0.2°C
ON	ON	ON	ON	ON	±0.1°C

C. Extracted Resistor Ratios

Using resistor calibration, the on-chip resistor ratio can be extracted. Fig. 16 shows a histogram of the normalized resistor ratios of all measured samples. Even though very different resistor ratios are used, it shows a standard deviation (0.046%) that is similar to [11]. Achieving sub-0.01% matching would have required a resistor area larger than 2 mm^2, emphasizing the need for resistor calibration in low-cost designs.

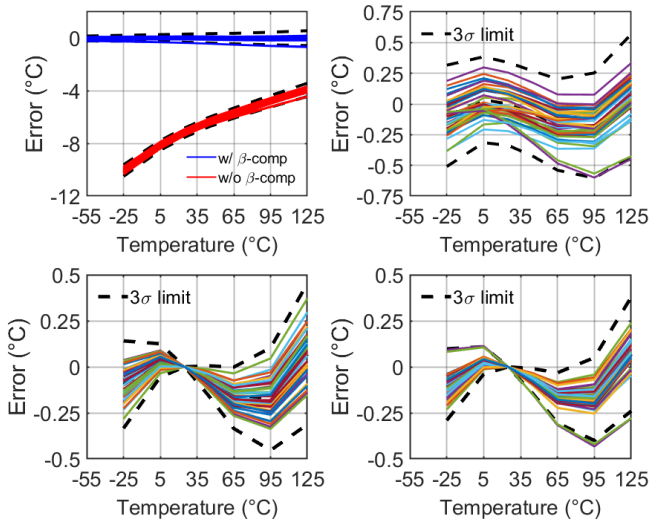


Fig. 18. Non-β-compensated temperature spread before batch calibration (top left), after batch calibration (top right), with resistor-ratio calibration a PTAT RT trim (bottom left), and an offset RT trim (bottom right).

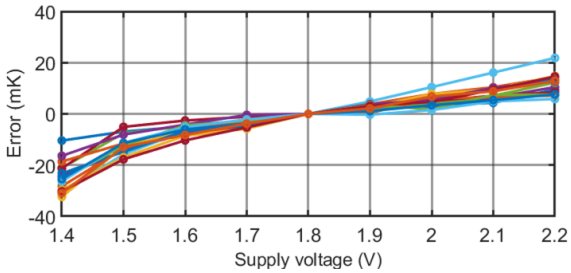


Fig. 19. Power supply sensitivity of 16 samples.

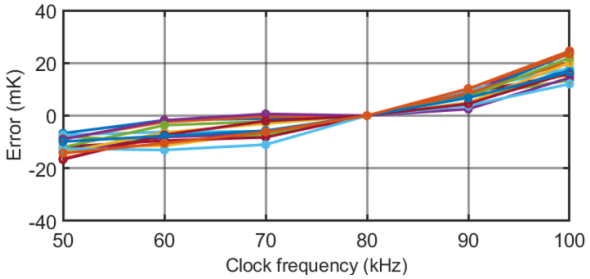


Fig. 20. Clock frequency sensitivity of 16 samples.

D. Accuracy

To determine the sensor's accuracy, 40 sensors on 20 dies were characterized in a temperature-controlled oven, with the samples mounted in close thermal contact with a calibrated pt-100 thermistor. The batch-calibrated inaccuracy is ±0.6 °C (3σ) (Fig. 17, top left), with a residual nonlinearity of ±0.02 °C (α = 12.1). This improves to ±0.2 °C (3σ) after an RT trim (Fig. 17, top right). After applying resistor-ratio calibration, the target inaccuracy of ±0.1 °C (3σ) is achieved (Fig. 17, bottom left). Replacing the temperature trim with a low-cost voltage calibration increases the inaccuracy to ±0.25 °C (3σ) (Fig. 17, bottom right), which is sufficient for most applications. Table I presents the effectiveness of each accuracy-improvement technique. Chopping, BJT-DEM, and I_C-CM DEM contribute the largest accuracy improvements,

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE OF THE ART

	ISSCC'22 [21]	TCAS'21 [23]	JSSC'17 [8]	ASSCC'19 [16]	ISSCC'20 [12]	JSSC'23 [22]	JSSC'23 [11]	This work
Sensor type	PNP	PNP	PNP	NPN	NPN	PNP	PNP	**NPN**
Architecture	DTΔΣM	DCM	DTΔΣM	CTΔΣM	CTΔΣM	DTΔΣM	CTΔΣM	**CTΔΣM**
Technology	0.18µm	0.13µm	0.16µm	0.18µm	0.11µm	0.18µm	0.18µm	**0.18µm**
Chip area [mm²]	0.42	0.086	0.16	0.35	0.2	0.25	0.12	**0.07**
Supply current [µA]	2.5	33	4.6	5.6	550	0.81	9.5	**2.5**
Supply voltage [V]	1.5 to 2	1.2	1.5 to 2	1.6 to 2.2	1.125	0.95 to 1.4	1.7 to 2.2	**1.4 to 2.2**
Supply sensitivity [°C/V]	0.44	-	0.01	0.01	-	0.2	0.01	**0.04**
Temperature range	-50°C to 180°C	-40°C to 125°C	-55°C to 125°C	-40°C to 125°C	-35°C to 95°C	-55°C to 125°C	-55°C to 125°C	**-55°C to 125°C**
3σ inaccuracy [°C] after a 1-pt trim	±0.45	±0.54	±0.06[2]	±0.13[2]	-	±0.15	±0.1	**±0.1**
Relative inaccuracy [%]	0.39	0.65	0.07	0.16	-	0.17	0.11	**0.11**
Resolution [mK]	17.6	60	15	1.67	0.65	1.8	1.1	**1.22**
Conversion time [ms]	8.3	1.3	5	213	0.72	128	40	**38.4**
Resolution FoM[1] [pJK²]	9700	51600	7800	5400	190	340	850	**200**

[1] FoM = Energy / Conversion x (Resolution)² [2]After systematic non-linearity removal

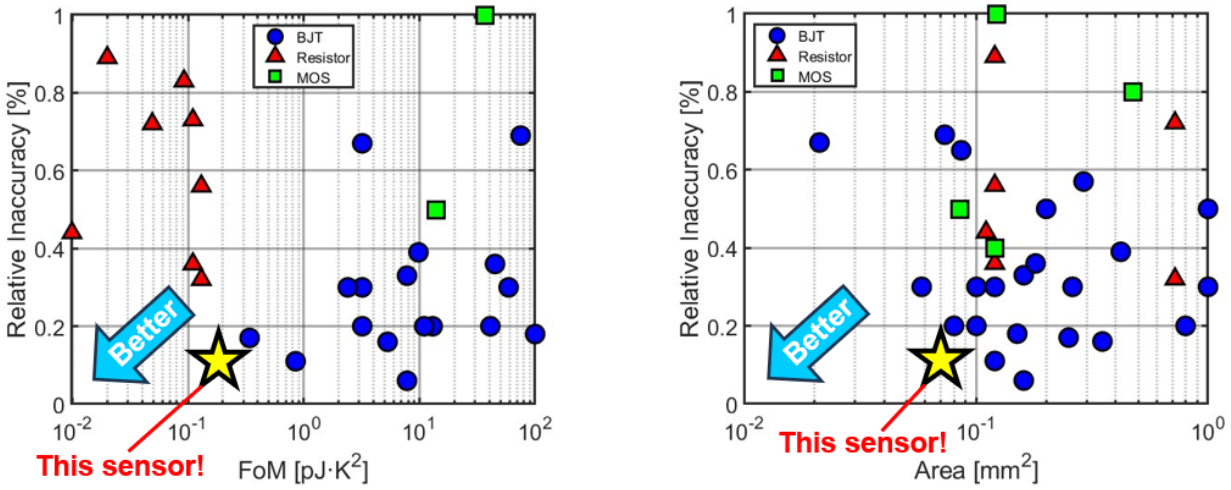


Fig. 21. FoM and area versus RIA after a one-pt trim for the state-of-the-art CMOS temperature sensors.

while I_B-CM DEM and resistor calibration contribute smaller, but still significant accuracy improvements.

Similar measurements were performed, where β compensation was turned off by opening switch S_1 (Fig. 8). Fig. 18 (top left) shows the absolute error caused by removing β compensation. This error exceeds 10 °C at low temperatures, where it causes the $\Delta\Sigma$-modulator to clip. Recalculating the batch-calibration coefficients ($\alpha = 11$) results in a similar nontrimmed spread of $\pm$0.6 °C (3σ); however, the residual nonlinearity increases to $\pm$0.2 °C (Fig. 18, top right). Applying a PTAT-trim at RT results in an inaccuracy of $\pm$0.45 °C (3σ) (Fig. 18, bottom left), which improves to 0.35 °C (3σ) (Fig. 18, bottom right) when replacing this with an offset-trim instead. Clearly, removing β compensation adds a 2nd error on top of the spread in V_{BE}, so that high accuracy cannot be achieved with just a single trim. This illustrates the need for β compensation in current-mode NPN-based front ends.

E. Power Supply and Clock Frequency Sensitivity

Fig. 19 shows the power supply sensitivity at RT of 16 samples as V_{DD} is varied from 1.4 to 2.2 V. It shows a PSS of 0.04 °C/V down to 1.4 V, demonstrating the ability of the sensor to operate over a large supply range.

Fig. 20 shows the sensor's sensitivity at RT to changes in clock frequency. As the clock frequency increases from 50 to 100 kHz, its sensitivity to switching transients increases. An average clock frequency sensitivity of 0.7 mK/kHz is found, which indicates that errors related to switching transients were successfully minimized.

F. Comparison to the State of the Art

Table II summarizes the performance of the proposed sensor and compares it with that of other state-of-the-art BJT-based temperature sensors, which achieve similar accuracy and/or energy efficiency [1]. The proposed sensor demonstrates excellent all-around performance, achieving both high accuracy and energy efficiency while occupying only a small area. This favorable tradeoff is illustrated in Fig. 21, which shows the performance of several one-pt trimmed CMOS sensors [1]. Among high-accuracy temperature sensors (RIA $<$ 0.2%), the proposed temperature sensor is 2$\times$ more efficient and occupies 2$\times$ less area than the state of the art.

VI. Conclusion

This work presents an NPN-based temperature sensor implemented in 0.18-μm CMOS that achieves both state-of-the-art one-point trimmed accuracy and energy efficiency while occupying a small area. A compact NPN-based front end is proposed along with an efficient circuit implementation to remove β errors introduced by the NPNs. Applying techniques, such as DEM, chopping, and resistor ratio calibration, along with a PTAT trim results in an accuracy of ± 0.1 °C (3σ) from -55 °C to 125 °C. Furthermore, the sensor achieves 200fJ $\cdot$ K^2 resolution FoM while occupying only 0.07 mm^2.

Acknowledgment

The authors would like to thank Zu-Yao Chang for his help with the measurements.

References

[1] K. A. A. Makinwa. *Smart Temperature Sensor Survey*. Accessed: Aug. 2023. [Online]. Available: http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls

[2] C. Gurleyuk, S. Pan, and K. A. A. Makinwa, "A 16 MHz CMOS RC frequency reference with ±90 ppm inaccuracy from -45 °C to 85 °C," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2429–2437, Aug. 2022.

[3] S. Zaliasl et al., "A 3 ppm 1.5 × 0.8 mm^2 1.0 μA 32.768 kHz MEMS-based oscillator," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 291–302, Jan. 2015.

[4] H. Lee, A. Partridge, and F. Assaderaghi, "Low jitter and temperature stable MEMS oscillators," in *Proc. IEEE Int. Freq. Control Symp.*, May 2012, pp. 1–5.

[5] K. Souri, Y. Chae, and K. A. A. Makinwa, "A CMOS temperature sensor with a voltage-calibrated inaccuracy of ±0.15°C (3σ) from –55°C to 125°C," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 292–301, Jan. 2013.

[6] M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ±0.1°C from -55°C to 125°C," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 292–301, Jan. 2013.

[7] F. Sebastiano, L. J. Breems, K. A. A. Makinwa, S. Drago, D. M. W. Leenaerts, and B. Nauta, "A 1.2-V 10-μ W NPN-based temperature sensor in 65-nm CMOS with an inaccuracy of 0.2°C (3σ) from –70°C to 125°C," *J. Solid-State Circuits*, vol. 12, no. 45, pp. 2591–2601, Feb. 2010.

[8] B. Yousefzadeh, S. H. Shalmany and K. A. A. Makinwa, "A BJT-based temperature-to-digital converter with ±60mK (3σ) inaccuracy from –55°C to +125°C in 0.16-±m CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 1044–1052, Apr. 2017.

[9] K. A. A. Makinwa, "Smart temperature sensors in standard CMOS," *Proc. Eng.*, vol. 5, pp. 930–939, Jan. 2010.

[10] A. Heidari, G. Wang, K. A. A. Makinwa, and G. Meijer, "A BJT-based CMOS temperature sensor with a 3.6pJ·K2-resolution FoM," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jun. 2014, pp. 224–225.

[11] N. G. Toth, Z. Tang, T. Someya, S. Pan, and K. A. A. Makinwa, "A PNP-based temperature sensor with continuous-time readout and ±0.1 °C (3σ) inaccuracy from -55°C to 125°C," *IEEE J. Solid-State Circuits*, early access, Jun. 3, 2024, doi: 10.1109/JSSC.2024.3402131.

[12] S. H. Shalmany et al., "3.7 A 620μW BJT-based temperature-to-digital converter with 0.65mK resolution and FoM of 190fJ·K2," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 70–72.

[13] J. F. Creemer, F. Fruett, G. C. M. Meijer, and P. J. French, "The piezojunction effect in silicon sensors and circuits and its relation to piezoresistance," *IEEE Sensors J.*, vol. 1, no. 2, p. 98, Jan. 2001.

[14] T. Someya, V. van Hoek, J. Angevare, S. Pan, and K. Makinwa, "A 210 nW NPN-based temperature sensor with an inaccuracy of ±0.15 °C (3s) from -15 °C to 85 °C utilizing dual-mode frontend," *IEEE Solid-State Circuits Lett.*, vol. 5, pp. 272–275, 2022.

[15] N. G. Toth and K. A. A. Makinwa, "3.7 A β-compensated NPN-based temperature sensor with ±0.1°C (3σ) inaccuracy from -55°C to 125°C and a 200fJ·K2 resolution FoM," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 66–68.

[16] R. K. Kumar, H. Jiang, and K. A. A. Makinwa, "An energy-efficient BJT-based temperature-to-digital converter with ±0.13°C (3s) inaccuracy from -40 to 125°C," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2019, pp. 107–108.

[17] M. Eberlein and H. Pretl, "A current-mode temperature sensor with a ±1.56 °C raw error and duty-cycle output in 16nm FinFET," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2021, pp. 1–5.

[18] M. A. Pertijs and J. H. Huijsing, "A sigma-delta modulator with bitstream-controlled dynamic element matching," in *Proc. 30th Eur. Solid-State Circuits Conf.*, Jan. 2004, pp. 187–190.

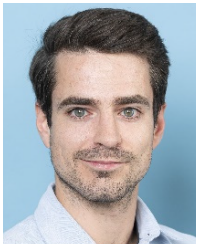
[19] M. A. P. Pertijs, A. L. Aita, K. A. A. Makinwa, and J. H. Huijsing, "Voltage calibration of smart temperature sensors," in *Proc. IEEE Sensors*, Oct. 2008, pp. 756–759.

[20] S. Pan and K. A. A. Makinwa, "A 0.25 mm^2-resistor-based temperature sensor with an inaccuracy of 0.12 °C (3 σ) from -55 °C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3347–3355, Dec. 2018.

[21] B. Wang and M.-K. Law, "Subranging BJT-based CMOS temperature sensor with a ±0.45 °C inaccuracy (3σ) from –50 °C to 180 °C and a resolution-FoM of 7.2 pJ·K^2 at 150 °C," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3693–3703, Dec. 2022.

[22] Z. Tang, S. Pan, M. Grubor, and K. A. A. Makinwa, "A sub-1 V capacitively biased BJT-based temperature sensor with an inaccuracy of ±0.15°C (3σ) from -55°C to 125°C," *IEEE J. Solid-State Circuits*, vol. 58, no. 12, pp. 3433–3441, Sep. 2023.

[23] Z. Huang, Z. Tang, X.-P. Yu, Z. Shi, L. Lin, and N. N. Tan, "A BJT-based CMOS temperature sensor with duty-cycle-modulated output and ±0.5°C (3s) inaccuracy from -40 °C to 125 °C," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 8, pp. 2780–2784, Aug. 2021.



Nandor G. Toth (Graduate Student Member, IEEE) was born in Delft, The Netherlands, in 1997. He received the B.Sc. and M.Sc. degrees in electrical engineering from Delft University of Technology, Delft, in 2018 and 2021, respectively, where he is currently pursuing the Ph.D. degree.

His research interests include mixed-signal design and smart sensors.

Kofi A. A. Makinwa (Fellow, IEEE) received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Ife, Nigeria, in 1985 and 1988, respectively, the M.E.E. degree from the Philips International Institute, Eindhoven, The Netherlands, in 1989, and the Ph.D. degree from Delft University of Technology, Delft, The Netherlands, in 2004.

From 1989 to 1999, he was a Research Scientist with Philips Research Laboratories, Eindhoven, The Netherlands. Since 1999, he has been at Delft University of Technology, where he is an Antoni van Leeuwenhoek Professor and the Head of the Microelectronics Department. His research interests include the design of mixed-signal circuits, sensor interfaces and smart sensors. This has led to 20+ books, 350+ technical papers, and 30+ patents.

Dr. Makinwa was the Analog Subcom chair of ISSCC from 2018 to 2021, and has served on the program committees of several other IEEE conferences. He has also been a distinguished lecturer of the Solid-State Circuits Society and an elected member of its Adcom. He is currently a member of the executive committee of the VLSI symposium and a co-chair of the Advances in Analog Circuit Design (AACD) workshop and the IEEE Sensor Interfaces Meeting (SIM). Dr. Makinwa is the co-recipient of 18 best paper awards, from the JSSC, ISSCC and VLSI symposium, among others. In 2023, at the 70th anniversary of ISSCC, he was recognized as its top contributing author. He is a member of the Royal Netherlands Academy of Arts and Sciences.