Chapter 10
An Outlook on Power Electronics Reliability and Reliability Monitoring

Henry A. Martin, Edsger C. P. Smits, R. H. Poelma, Willem D. van Driel, and G. Q. Zhang

10.1 Introduction

Reliability is an essential performance metric in power electronics for developing high-efficiency and high-power-density devices. In today's rapidly evolving technological landscape, meeting reliability requirements presents several challenges. These include catering to field-critical applications, enduring harsh environmental conditions, adhering to rigorous testing and safety regulations, accommodating the need for higher power density, complex integration, uncertainties related to new materials, and resource constraints [1]. Besides, reliability qualification has undergone a transformative shift. The evolution of reliability qualification is distinct into four stages, as illustrated in Fig. 10.1 [2–5]. In the past, micro- and power electronic devices underwent various stress tests (temperature cycling, thermal shock, humidity testing, electrical overstress, and vibration testing), irrespective of

H. A. Martin (✉)
Delft University of Technology, Department of Microelectronics, Delft, The Netherlands
Chip Integration Technology Center (CITC), Nijmegen, The Netherlands
e-mail: henry.martin@citc.org; h.a.martin@tudelft.nl

E. C. P. Smits
Chip Integration Technology Center (CITC), Nijmegen, The Netherlands

R. H. Poelma
Delft University of Technology, Department of Microelectronics, Delft, The Netherlands
Nexperia B.V., Nijmegen, The Netherlands

W. D. van Driel
Delft University of Technology, Department of Microelectronics, Delft, The Netherlands
Signify N.V., Eindhoven, The Netherlands

G. Q. Zhang
Delft University of Technology, Department of Microelectronics, Delft, The Netherlands

W. D. van Driel et al. (eds.), *Recent Advances in Microelectronics Reliability*,
https://doi.org/10.1007/978-3-031-59361-1_10

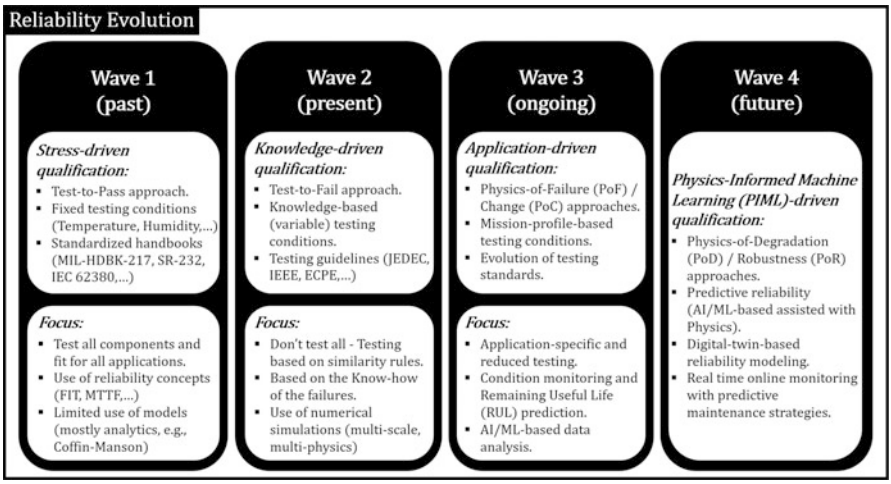


Fig. 10.1 The evolution of reliability summarized as wave 1 (past), wave 2 (present), wave 3 (ongoing), and wave 4 (future). Each stage highlights the driving aspect of reliability research and its vital focus elements [*Adapted from iREL4.0 newsletter (with permission)*]

their application. The component failure rates were further documented in empirical military handbooks MIL-HDBK-217, technical handbook SR-232 from Telcordia, technical report IEC 62380, and Siemens SN29500 standards. This approach was primarily reactive, focusing on identifying and resolving issues after they occurred. A proactive knowledge-driven approach later emerged, emphasizing reliability physics and understanding failure mechanisms. Esteemed bodies like JEDEC, IEEE, and ECPE have instituted predefined testing standards and guidelines for electronic components. These span across integrated circuits, discrete semiconductors, electronic modules, and passive components, categorized based on their designated applications. This proactive paradigm reflects preemptive issue mitigation rather than reactive troubleshooting.

A noticeable trend has recently emerged, focusing attention on application-driven qualifications. This approach emphasizes mission-profile-based testing, active condition monitoring, and an intricate grasp of two complementary approaches in reliability engineering: the physics of failure (PoF) and the physics of change (PoC). The PoF approach analyzes root-cause failure mechanisms, considering materials, defects, and stresses, while the PoC approach seeks to understand physical alterations resulting from failure. In the evolving landscape of reliability, traditional metrics like failure in time (FIT) and mean time to failure (MTTF) are being superseded by remaining useful life (RUL) prediction with a shift in focus from understanding failure mechanisms to degradation mechanisms and device robustness [6, 7]. Physics-informed computational techniques, including machine learning (ML) and artificial intelligence (AI), are expected to play a crucial role in early fault prediction and performance decline. Reliability modeling based on digital-twin and real-time online monitoring are anticipated to be pivotal for

high-value applications. These coordinated approaches are essential in developing reliable power semiconductor devices, ensuring seamless operation, and promoting a sustainable environment.

In order to support the evolving reliability qualification methods, several measurement strategies have been devised to streamline the process of reliability monitoring. Monitoring reliability entails assessing the device condition continuously throughout its lifetime. In this context, three fundamental conceptions of implementing condition monitoring are elucidated below [8, 9]:

1. Measuring the device's intrinsic parameters as an indication of the device performance degradation
2. Add-on (or) embedded sensors to measure the device's robustness against performance degradation
3. Reliability modeling approach to compare the device's performance against a computational model

Reliability modeling at the component level, system level, and software reliability has the highest percentage of research publications [10]. Therefore, reliability modeling is excluded from the scope of this chapter. Recent publications on lifetime modeling are presented in [11, 12]. The primary objective of this chapter is to present a comprehensive overview of various relevant measurement techniques, particularly thermal measurements, commonly used in industry and academia that can support reliability monitoring (both online and offline). An ideal strategy for device performance monitoring would avoid additional sensors to measure temperature, humidity, and mechanical stresses. An increment in those stressors might not directly relate to the device's electrical performance characteristics. Besides, additional sensors might introduce additional failure modes. Hence, measuring the device's intrinsic electrical performance parameters is preferable. However, the limitation in understanding the relationship between various stressors and the device performance degradation requires embedded sensors for reliability monitoring.

This chapter discusses the current state of power electronics reliability and several noteworthy reliability measurement methodologies. Section 10.2 explores the power electronics market and survey reports from literatures on power device failure rates. Section 10.3 focuses on selected chip-level and package-level degradation mechanisms. Section 10.4 provides a detailed review of various reliability measurement methodologies. Section 10.5 summarizes the discussed methods, highlighting their advantages and disadvantages. The chapter concludes with an emphasis on the need for online reliability monitoring for a sustainable future.

10.2 Power Electronics Market and Failure Statistics from Field Experiences

Concerns about device efficiency and reliability surfaced due to the increasing demand for high power. The recent transition towards wide-bandgap (WBG)

semiconductors further amplified reliability concerns. While silicon has traditionally been the preferred material for semiconductors, its energy gap decreases from ∼1.12eV at room temperature (25°C) to around ∼1eV at 300°C, resulting in reduced power transistor efficiency at high operating temperatures [13, 14]. Consequently, semiconductor materials with bandgap energy exceeding 2eV at 25°C have gained significant interest, enabling the development of power transistors with higher breakdown voltage and higher operating temperature, thereby generating market demand. The increasing demand is reflected in the current market projections: As of 2021, the global power electronics industry was valued at around ∼$17B, and it is expected to grow at a compound annual growth rate (CAGR) of 6.9% by 2026 [15]. This growth is primarily driven by three segments: **(a)** consumer electronics, **(b)** automotive electric vehicle (EV) systems, and **(c)** industrial applications.

(a) Silicon metal oxide semiconductor field effect transistors (MOSFETs) have traditionally dominated consumer applications. However, in recent times, gallium nitride (GaN) technology is replacing silicon in fast-charging consumer electronics.

(b) The automotive inverter technology market has conventionally relied on integrated gate bipolar transistor (IGBT) modules based on silicon. The adoption of SiC technology in automotive inverters has experienced significant growth since Tesla implemented silicon carbide (SiC) MOSFETs. In 2020, BYD semiconductors and LUCID Motors also adopted SiC MOSFETs in their automotive inverters [16].

(c) Silicon IGBT modules dominate high-power industrial applications, including photovoltaic (PV), wind energy, and battery energy storage systems (BESS). SiC IGBTs demonstrate higher efficiency than Si IGBTS for controllers used in aircraft ground power units (AGPUs) [17].

A survey conducted on the reliability of power converters across various applications revealed that power semiconductor devices are particularly susceptible to failures [18]. Figure 10.2 illustrates the failure rates of power semiconductor devices in four highly demanding industrial applications. In wind energy systems, a survey conducted over a span of 15 years on 1500 wind turbines indicated that approximately 23% of the reported malfunctions (34,582) were attributed to electrical system failures, with wind energy power converters exhibiting the highest failure rate distribution [19] (Fig. 10.2a). Similarly, in utility-scale-grid-connected photovoltaic (PV) systems, a survey revealed that 37% of unscheduled maintenance events between 2001 and 2006 accounted for 59% of the overall maintenance cost. Among these events (Fig. 10.2b), power inverters were responsible for the majority of repairs [20, 21]. In electric railway traction chain (ERTC) systems, power semiconductor devices play a vital role. A survey conducted from 2009 to 2013 reported that the traction power converter contributed to 34% of the total failures in the traction drive systems [22] (Fig. 10.2c). Furthermore, as the aerospace industry moves towards electrified aircraft, the demand for high-power converters in hybrid electric propulsion systems is increasing. A survey on the failure rate of

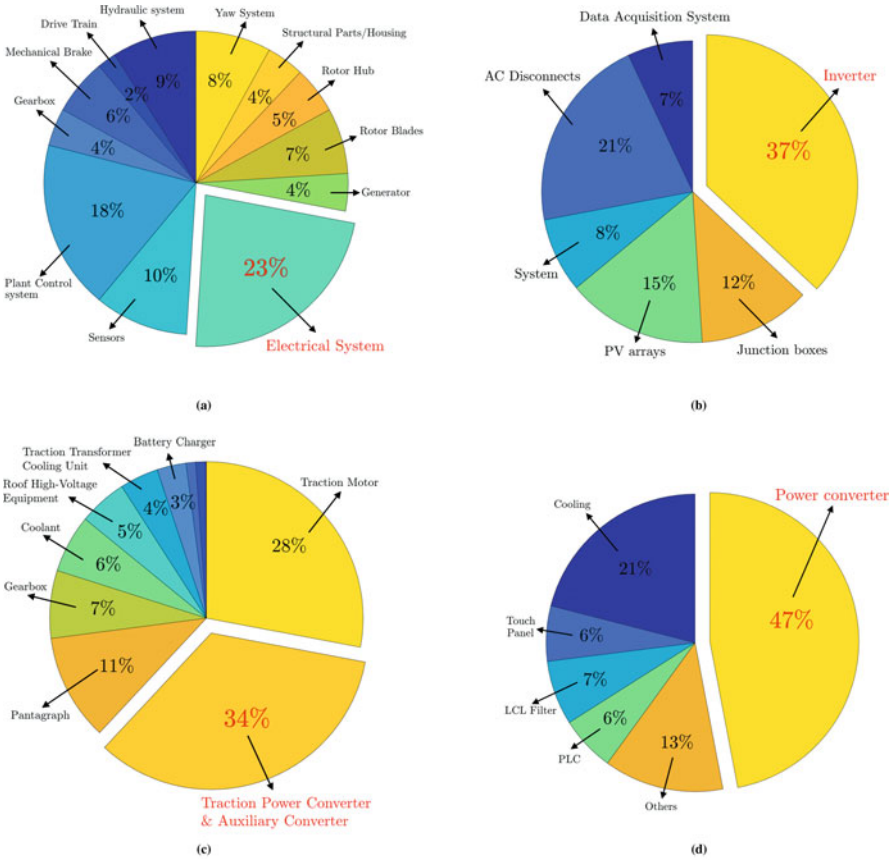


Fig. 10.2 The percentage failure rate of power devices against other components was compiled based on the survey reports in high-power demanding industrial applications. **(a)** In wind energy systems, power converters have the highest distribution of the failure rate [19]. **(b)** The power inverter malfunction in PV systems accounted for 37% unscheduled maintenance [20, 21]. **(c)** The traction power converter led to 34% of the total failures in electric train traction systems [22]. **(d)** The power converter failure rate in aircraft electric-drive systems was reported to be 47% of the total system failure [23]. (**a**) Wind energy systems. (**b**) Photovoltaic (PV) systems. (**c**) Electric railway traction chain (ERTC) Systems. (**c**) Electric drive panel systems in aerospace [*The graphical data shown are adapted from the literatures that are cited*]

electric-drive panel systems revealed that power converters accounted for 47% of the total system failures [23] (Fig. 10.2d).

The survey findings reported in the literature provide compelling evidence that despite the extensive history of power electronics, its reliability remains a significant concern, particularly due to its impact on real-life applications resulting in increased downtime and costs. While power electronics play a crucial role in automotive applications, comprehensive statistical data on the failure rate of power devices in electric vehicles (EVs) is rarely available to the public. However, it is

worth noting that power MOSFETs used for battery connect/disconnect switches in automobiles exhibit a failure rate of a few per million [24]. The failure statistics depicted in Fig. 10.2 have significant implications attributed to factors such as electrical overstress and environmental conditions like temperature and humidity. Consequently, it is imperative to explore and understand the key chip-related and package-related degradation mechanisms that contribute to these failures.

10.3 Power Electronics Degradation Mechanisms

Material degradation is an inevitable natural phenomenon that significantly affects power electronics' device reliability, performance, and lifespan. Power devices experience degradation caused by multiple factors, including operating temperature, power input, switching stresses (electrical transients), humidity, mechanical stresses, and aging. Figure 10.3 illustrates a schematic of a typical power module and provides a classification of chip-related and package-related degradation, which will be discussed further in detail.

10.3.1 Chip-Related Degradation Mechanisms

Chip-related degradations primarily involve intrinsic mechanisms, where the device's internal operation deteriorates, primarily as a result of electrical overstress and temperature. Among these mechanisms, two dominant wear-out mechanisms at

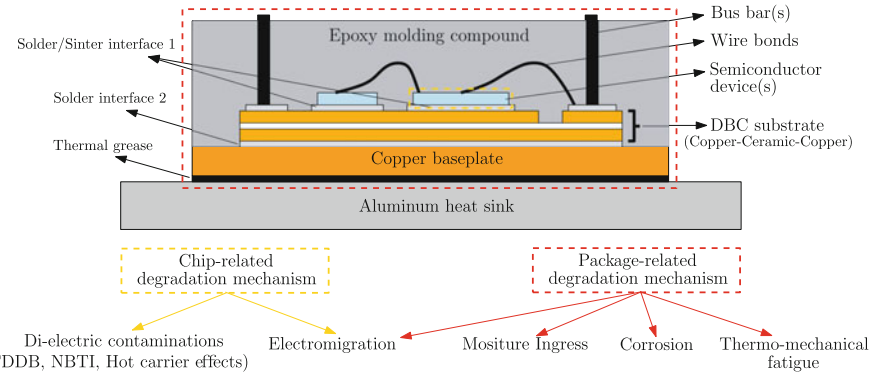


Fig. 10.3 A schematic of a typical power module is shown with layer stacks of different materials enclosed in a plastic housing. Some dominant degradation mechanisms in power electronics are classified into chip-related and package-related. The time-dependent dielectric breakdown (TDDB), negative bias temperature instability (NBTI), and hot carrier injections are categorized as dielectric contamination. Though the mechanisms are differentiated as chip- and package-related, they overlap in reality

the chip level are electromigration and dielectric contamination. Electromigration on the chip level refers to the movement of ions in the circuit interconnects, leading to their degradation over time. On the other hand, dielectric contamination involves the entrapment of ions in the dielectric material. Both of these mechanisms contribute to degraded performance and eventual failure of the chip. The impact of temperature on the electromigration process and gate-oxide contamination accelerates the rate of deterioration. Higher temperatures exacerbate these wear-out mechanisms, intensifying the degradation of the chip and shortening its overall lifespan.

10.3.1.1 Electromigration

Metal interconnects on semiconductors are susceptible to electromigration at high current densities (10^5 A/cm^2) [25]. Electromigration is a material transport phenomenon that occurs when electrons flowing through the conductors transfer their momentum. This leads to either the depletion or accumulation of material, resulting in open-circuit or short-circuit conditions, respectively [26, 27]. The process of ions electromigrating is thermally activated, which is shown in Black's equation for electromigration (Eq. (10.1)). The MTTF_{EM} is inversely proportional to the current density j, the effective length L_{eff} over which the current density is applied, and an Arrhenius behavior of thermal activation. Here E_a represents the activation energy for migration, T is the temperature in Kelvin, and k is the Boltzmann constant. The constant n in the equation is specific to the material and influences the overall behavior of the electromigration process [27–29]:

$$\mathrm{MTTF_{EM}} \propto \frac{1}{j^n \times L_{eff}} \exp\left(\frac{E_a}{k\boldsymbol{T}}\right) \tag{10.1}$$

The degradation caused by electromigration experiences exponential growth with increasing temperature. It is also possible for electromigration to occur at the package level, affecting components such as wire bonds and interconnects. Apart from temperature, the presence of intermetallic compounds significantly influences the rate of electromigration. Intermetallics such as copper-tin (Cu-Sn), silver-copper (Ag-Cu), nickel-tin (Ni-Sn), or gold-aluminum (Au-Al) at interface joints or wire bonds can accelerate the migration rate.

10.3.1.2 Dielectric Contamination

In metal oxide semiconductor (MOS) devices, the dielectric serves as an insulating oxide layer between the gate and the conductive channel. Contamination of the dielectric, i.e., ions getting entrapped, can lead to transistor performance degradation. Applying a sufficiently high electric field across the dielectric layer can cause dielectric breakdown, which is a time-dependent (TDDB) failure. This

failure occurs due to processes such as electron tunneling or ion entrapment in the oxide layer over time [27, 29–32]. The lifetime of the dielectric is heavily influenced by various factors, including the quality and thickness of the oxide layer, the applied electric field, and the operating temperature of the device. However, conflicting experimental observations have been reported, particularly for ultrathin dielectrics, leading to controversies in the equations that define TDDB [31–33]. Based on experiments conducted in reference [33], an empirical model for mean time to failure (MTTF) due to TDDB has been derived from [27, 29]. In Eq. (10.2), t_{ox} represents the gate oxide thickness, A_{ox} denotes the oxide area over which a voltage V is applied, and T is the temperature in Kelvin. The parameters a, b, X, Y, and Z are fitting parameters used in the model.

$$\mathrm{MTTF}_{\mathrm{TDDB}} \propto 10^{t_{ox}} \times \frac{A_{ox}}{V^{(a-b\boldsymbol{T})}} \times \exp\left(\frac{X + Y\boldsymbol{T}^{-1} + Z\boldsymbol{T}}{k\boldsymbol{T}}\right) \tag{10.2}$$

Contamination of the dielectric can also occur through other means. At extremely high operating temperatures (beyond the lattice temperature), some ionic charge carriers flowing through the conductive channel are entrapped (diffused) in the gate oxide layer. This phenomenon is referred to as ionic contamination or hot carrier injection [8, 30]. Like TDDB, another effect of dielectric contamination is the negative bias temperature instability (NBTI), a commonly observed phenomenon in PMOS devices. It arises due to the presence of gate-oxide interface traps (positive charges) that neutralize the negative gate voltages [30]. NBTI happens also in NMOS devices operated under negative bias.

The chip-level degradation mechanisms mentioned above primarily result in reduced efficiency and electrical performance, which can be observed by a shift in the device threshold voltage and higher leakage currents. These mechanisms do not immediately impact transistor operation but instead cause cumulative damage over time. However, the degradation process can be accelerated under extremely harsh environmental conditions. For instance, the power semiconductor devices used in avionics and space applications have reported single-event burnout failure. This occurs due to the transfer of kinetic energy from charged particles in the Earth's magnetic field and exposure to cosmic radiations like high-energy neutrons [8, 34, 35].

10.3.2 Package-Related Degradation Mechanisms

Chip-related degradation mechanisms are primarily driven by intrinsic stresses, whereas electronic packages are susceptible to both intrinsic and extrinsic environmental conditions. At the package level, dominant wear-out mechanisms include moisture ingress, corrosion, and thermomechanical fatigue. Similar to chip-related degradation, the operating temperature has a significant influence on the rate of deterioration in package-related mechanisms.

10.3.2.1 Moisture Ingress

Epoxy-based molding compound (EMC) is a commonly used encapsulant for electronic devices, providing protection against temperature, humidity, and dust. However, being hygroscopic, EMC is susceptible to oxidation when exposed to high temperatures and highly humid conditions. In [36], the moisture diffusion characteristics of an epoxy-based molding compound (90.6wt% silica filler and 2.04 g/cm^3 density) were analyzed using a dynamic sorption analyzer at temperatures 20°C to 85°C with 0–85% relative humidity. Moisture ingress, in turn, leads to device degradation through electrochemical migration and corrosion. A review on moisture ingress in photovoltaic modules has reported that the moisture content in the thermoplastic polymer encapsulant led to corrosion on the metal grids [37]. The aging process of the epoxy compound due to moisture ingress is accelerated at higher temperatures due to increased moisture absorption and diffusion within the EMC material. An experimental study [38, 39] demonstrated that pristine EMC undergoes rapid oxidation within 24 hours when exposed to elevated temperatures. The oxidation significantly alters the mechanical properties of the molding compound, including changes in the elastic modulus, thermal expansion coefficient, and glass transition temperature. The mean time to failure (MTTF) due to moisture ingress follows an inverse relationship with relative humidity (RH) and exhibits an Arrhenius behavior characterized by an exponential decay (Eq. (10.3)). The constant n in the equation depends on the specific epoxy compound being used.

$$\mathrm{MTTF_{MI}} \propto \frac{1}{RH^n} \exp\left(\frac{E_a}{k\boldsymbol{T}}\right) \tag{10.3}$$

The oxidation of the molding compound further impacts the reliability of the package solder joints. The correlation between the oxidation of the molding compound and solder-joint thermal fatigue was investigated in [40]. It provides insights into the effects of oxidation on the lifetime and durability of solder joints.

10.3.2.2 Corrosion

Corrosion is a well-studied phenomenon, but its significance in electronics packaging requires further attention. An overview of failure mechanisms associated with corrosion in control electronics (ECU), sensor electronics, and power electronics is provided in [41]. Water treeing is a corrosion mechanism that degrades the packaging molding compound in high-power electronic devices operating in the kV range. High voltages generate electric fields that ionize the moisture content in the molding compound, resulting in the formation of microchannels. Based on an electrochemical corrosion process called anodic migration, dendrite structures start growing within the microchannels. An experimental study was conducted in [41] to analyze the dendrite structures due to anodic migration phenomenon (AMP) in

polymer compounds, and temperature plays a significant role. The mobility of metal ions increases with temperature, thereby accelerating the rate of dendrite growth through the polymer to form conductive paths.

In recent times, considerable research efforts have been focused on investigating inorganic encapsulation materials with high thermal conductivity as potential replacements for epoxy molding compounds in high-power devices [42]. In power electronics, cement-based encapsulants were proposed in [43] for their potential usage. However, corrosion remains a primary concern when utilizing cement-based materials. The mean time to failure (MTTF) due to corrosion can be described by an inverse relationship with relative humidity and applied electric field ($E = V/d$) and an exponential relationship with temperature, as expressed in Eq. (10.4). It is worth noting that other forms of material migration, including anodic corrosion, cathodic corrosion, and purple plagues, may also occur in packaging materials.

$$\mathrm{MTTF_{AMP}} \propto \left(\frac{1}{RH^n} + \frac{d^m}{V}\right) \exp\left(\frac{E_a}{k\boldsymbol{T}}\right) \tag{10.4}$$

10.3.2.3 Thermomechanical Fatigue

Thermomechanical fatigue (TMF) occurs due to repeated cyclic loading caused by temperature fluctuations, temperature gradients within the device, and mechanical stressors like vibrations or shocks. A power module consists of layer stacks of materials with distinct properties housed within a plastic enclosure. The thermal expansion coefficient (CTE) of pure copper (∼16.5 ppm/°C) is roughly four to five times higher than that of silicon (∼3 ppm/°C) or SiC (∼4 ppm/°C). This discrepancy induces thermomechanical stresses at the interface, as depicted in Fig. 10.4. Therefore, selecting the interconnect material between the semiconductor die and the copper substrate plays a crucial role.

Thermomechanical fatigue occurring at the interface material is a cumulative damage process. The impact of thermomechanical fatigue conditions on automotive

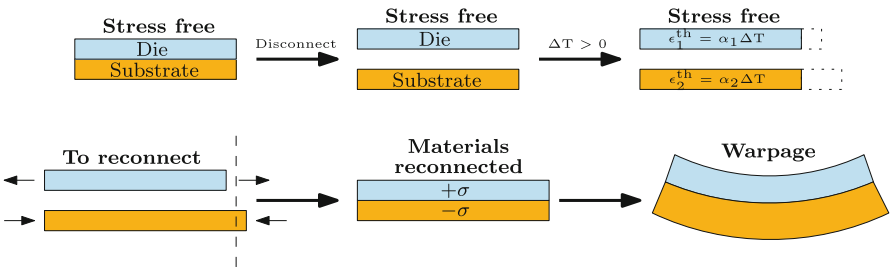


Fig. 10.4 A schematic illustration of thermomechanical stresses induced due to thermal expansion coefficient α mismatch. In a stress-free situation, the strain ϵ will result in independent expansion when $\Delta T > 0$. However, if the dissimilar materials remain connected, the thermomechanical stresses σ will lead to material warpage

power modules has been extensively investigated in [44]. One resulting behavior of repeated thermomechanical loading conditions is stress migration. Stress migration refers to material migration due to thermomechanical stresses. Interestingly, the phenomenon of stress migration in silver is also utilized as a die-attachment bonding process [45, 46]. An empirical relationship is provided in Eq. (10.5) correlating the number of cycles to failure, the temperature swing (ΔT), and the maximum temperature (T_{max}) [47, 48].

$$\text{MTTF}_{\text{TMF}} \propto \Delta \boldsymbol{T}^{n} \exp\left(\frac{E_a}{k \boldsymbol{T}_{max}}\right) \tag{10.5}$$

The T_{max} is an arbitrary temperature established from the empirical model, suggesting that the material lifetime will be longer if it stayed below the maximum temperature. The equation expresses a power law dependence of MTTF on the temperature swing and exhibits an Arrhenius behavior of thermal activation between MTTF and T_{max}.

To summarize:

1. The mean time to failure (MTTF) metric serves as a measure to estimate the expected time until a material fails due to degradation. Many prevalent chip-related and package-related degradation mechanisms demonstrate an Arrhenius relationship with temperature. However, it is important to note that these empirical models may not be universally accurate and necessitate thorough experimental validation. It is also essential to consider complex relationships with material properties, testing conditions, and microstructures, which require comprehensive experimental validation.
2. This suggests that traditional reliability concepts such as failure in time (FIT) and mean time to failure (MTTF) are undergoing a transition. The failure rate documented by empirical handbooks is no longer sufficient to address the uncertainties associated with field-critical applications. As a result, the future calls for the adoption of real-time online reliability monitoring supported by advanced computational techniques for seamless, non-interruptive system operation. This transition aims to embrace predictive reliability qualification and effectively address the evolving challenges in ensuring reliable performance.

10.4 Power Electronics Reliability Monitoring

Reliability, as the highest level of robustness assurance, is essential in ensuring the system's resilience and performance [49]. *Reliability monitoring* can be defined as "*a process of continuously assessing the device's performance throughout its lifetime to detect early signs of anomalies and implement predictive maintenance strategies to reduce system downtime.*" Power semiconductor devices are particularly vulnerable to failures due to factors such as high electric fields, high currents,

and high temperatures [18]. Field experiences, as illustrated in Fig. 10.2, indicated the impact of power component failure and its aftermath, leading to unforeseen system downtime and additional repair costs. Such unexpected maintenance could have been mitigated through early fault detection based on real-time online monitoring. Hence, in this section, we delve into various measurement methods that can support online or offline reliability monitoring.

Monitoring the power device's reliability involves measuring its key performance metric. Particularly in automotive and high-power industrial applications operating in harsh environments, device failure caused by thermal breakdowns outweighs the impact of vibrations and humidity [50, 51]. To address the importance of reliability monitoring, this section summarizes various measurement methodologies, mostly tailored towards thermal methods, as depicted in Fig. 10.5. These tailored measurement methods effectively monitor the device's condition to reduce the risks associated with unexpected system interruption during operation. In Fig. 10.5, several reliability measurement methods are classified into contact and contactless approaches. In the past, measuring the device junction temperature involved directly probing thermocouples on the device's active surface. However, this method presented various limitations such as low resolution, contact inaccuracies, and the invasive nature of physical probing [47, 49]. To overcome these challenges, contactless techniques were introduced, which are further subdivided into thermal and nonthermal methods. Among the nonthermal methods, two notable approaches are measuring the device's electrical parameters and using acoustic microscopy. These methods are widespread and commonly used measurement techniques in various industries.

The on-state resistance $R_{DS}(on)$ is a critical electrical parameter that characterizes the resistance experienced by the current flowing through the channel of a device when it is in its conducting state. In most packages, the drain terminal of the device is electrically connected to the package substrate. As a result, the on-state resistance includes the resistance contributions from the die, the die-attach material, and the package substrate. Having a lower $R_{DS}(on)$ is crucial for ensuring optimal device performance with minimal power losses and maximum efficiency. Changes in the on-state resistance directly correspond to performance degradation in the package, particularly in the electrical and thermal interconnects that are more susceptible to failures. Therefore, monitoring the device's on-state resistance over its lifetime allows for identifying potential issues with the device's electrical performance. However, localized failures or thermal hotspots may not directly reflect in the device's electrical resistance $R_{DS}(on)$.

On the other hand, scanning acoustic microscopy (SAM) is a powerful, non-destructive method to identify packaging defects. SAM consists of a piezoelectric transducer that generates ultrasonic pulses transmitted to the sample through a water medium. SAM uses water as a coupling medium due to its excellent ultrasonic conductivity and relatively low acoustic impedance. As the ultrasonic waves interact with material interfaces, they undergo reflection and scattering, producing an echo signal that is converted into an electrical output. An image processor then digitizes this signal. The raster scanning motion of the acoustic transducer generates

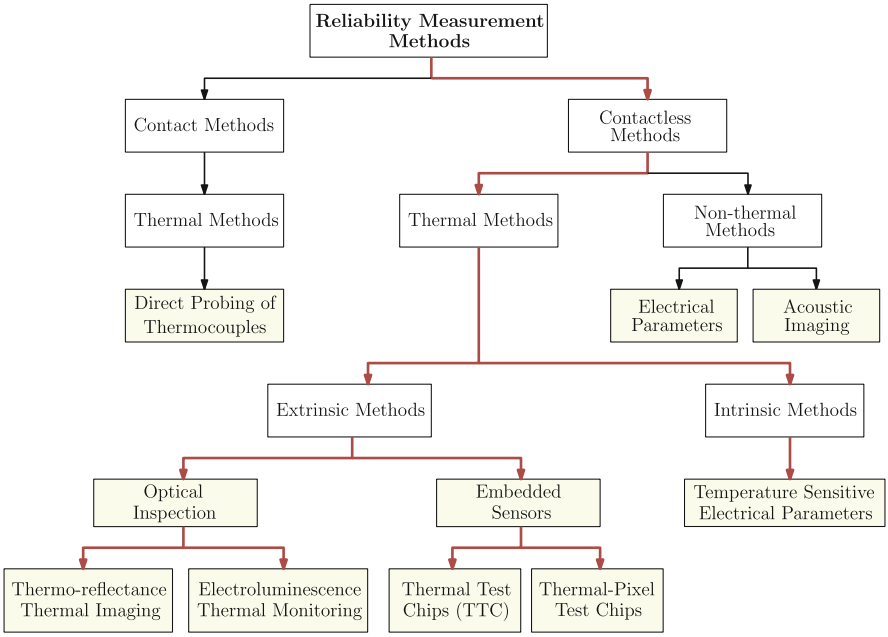


Fig. 10.5 Measurement methodologies mostly tailored towards thermal measurements were identified from the literature and shown. Probing a thermocouple to identify the junction temperature was used in early times, which sooner got replaced by contactless techniques, which are further subdivided into thermal and nonthermal methods. Measuring the device's electrical parameters and acoustic imaging are the most commonly used methods to monitor the device's reliability performance. Thermal methods are further divided into extrinsic and intrinsic methods. Extrinsic methods include optical inspection and embedded sensors. Though several optical techniques exist for thermal measurements, thermoreflectance-based thermal imaging and electroluminescence-based temperature estimation are studied in depth in this section. Likewise, temperature-sensitive electrical parameters (TSEP) are discussed under the intrinsic methods. The listed methods are commonly used measurement/characterization techniques employed in academia and industries. The relevance of the abovementioned methods for online monitoring requires careful consideration and implementation, which are further explained in Sect. 10.5

ultrasonic pulses at high frequencies that are reflected from the sample, thereby capturing the depth information [52]. It is important to acknowledge that SAM, like any imaging technique, has its limitations. The penetration depth of acoustic waves typically ranges from approximately 1 to 2 mm for most materials, and image quality is highly dependent on the properties of the sample being imaged. Encapsulation of semiconductor devices with epoxy molding compounds attenuates acoustic signals, while laminates and PCBs introduce significant reflection and scattering of ultrasonic pulses due to their complex layered structures with different materials. Consequently, an effective strategy for scanning encapsulated packages is to perform through-acoustic scan, before mounting on PCBs. During lifetime testing, power electronic packages are micrographed at intermittent life cycles to identify physical damages resulting from fatigue [53, 54].

The severity of thermal breakdowns has led to the development of various thermal measurement/characterization methods, categorized as extrinsic methods in Fig. 10.5. Likewise, semiconductor devices controlling the flow of electrons possess electrical properties that are highly sensitive to temperatures. These temperature-sensitive electrical parameters (TSEP) represent an intrinsic approach that enables direct translation of electrical measurements into device temperature readouts. In the following subsections, each of these contactless thermal measurement methods will be thoroughly reviewed by explaining its underlying physics.

10.4.1 Optical Thermal Inspection

Emissivity, a fundamental material property, plays a crucial role in optical thermal inspection. It refers to a material's ability to emit electromagnetic and infrared (IR) radiation. In an ideal scenario, a perfect emitter would absorb all incident radiation and emit thermal radiation across all wavelengths, and a perfect reflector would reflect all incoming radiation. However, in reality, no material is a perfect emitter or reflector. IR thermography, one of the earliest techniques used in electronics, utilizes IR radiation to detect thermal hot spots and gradients. As all materials above absolute zero emit IR radiation to some extent, IR-sensitive photodiode arrays and microbolometers can measure the emitted infrared energy as a function of temperature. A comprehensive review of IR thermography for nondestructive testing can be found in [55]. Steady-state IR thermography has also been employed to determine in-plane thermal conductance properties of materials [56].

In recent years, fiber-optic thermal sensors have gained significant interest due to their advantages, including high sensitivity, wide operating temperature range, rapid response time, immunity to electromagnetic interference, and suitability for use in hazardous environments. These fiber-optic high-temperature sensing systems utilize optical fiber transducers based on various principles such as black body radiation, fluorescence-based techniques, interferometry, or fiber Bragg grating (FBG) [57]. For instance, Khatir et al. [58] integrated fluorescence-based optic fibers into a multichip power electronic module to measure the junction temperature and characterize thermal impedance. Other thermal characterization techniques, such as Raman thermometry and liquid crystal thermography, have also been utilized in [59, 60]. While these optical thermal inspection methods have been extensively reviewed in the past, this section specifically focuses on reflectance-based thermal imaging and electroluminescence-based thermal monitoring methods, providing detailed discussions of their principles and applications.

10.4.1.1 Thermoreflectance-Based Thermal Imaging

The reflective properties are specific to each material and can be influenced by the interaction with electromagnetic radiation. The energy associated with the

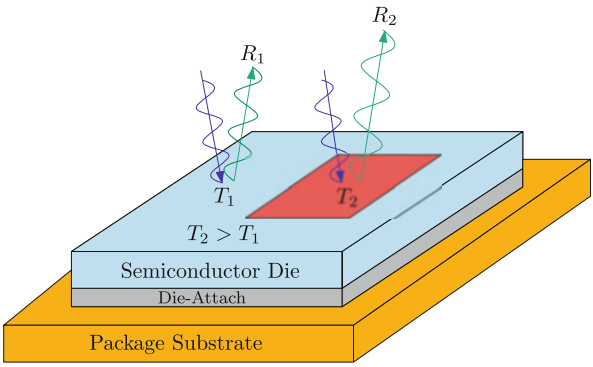


Fig. 10.6 The temperature-dependent surface reflectivity resulting in a change in amplitude and phase shift are schematically shown

reflected or scattered light beam exhibits a strong dependence on temperature. Thermoreflectance-based thermal imaging relies on the temperature-dependent surface reflectivity of materials, where thermoreflectance is inversely proportional to the material's thermal conductivity. Consequently, thermoreflectance-based measurements are commonly used to characterize the thermal conductivity of materials in both steady-state and transient-state techniques [61]. In optical thermal imaging systems employing thermoreflectance, transient techniques are employed, incorporating detectors with raster scanning capabilities. These detectors comprise arrays of photodiode sensors that detect the amplitude and phase shift of the reflected signals, as illustrated schematically in Fig. 10.6. The rate of change in surface reflectivity with respect to surface temperature change is governed by the thermoreflectance coefficient β, as shown in Eq. (10.6). A higher value of β corresponds to a lower noise level in the measurement signal. For example, the thermoreflectance coefficient of aluminum is approximately 2.55×10^{-5}, K^{-1}, while for silicon, it is approximately 1.5×10^{-4}, K^{-1} [62–64].

$$\frac{\Delta R(T(t))}{R} = \left(\frac{1}{R}\frac{\partial R}{\partial T}\right)\Delta T(t) = \beta \Delta T \tag{10.6}$$

The thermoreflectance coefficient is influenced by the wavelength of the probing medium and the surface roughness. By tuning the illumination wavelength, certain encapsulant materials can become transparent, allowing for noninvasive identification of the device junction temperature. For instance, a thermoreflectance-based thermal mapping of an IGBT power module encapsulated with silicone gel demonstrated that the silicone gel becomes transparent to visible white light, with green light exhibiting the highest thermoreflectance coefficient [65]. Similar thermal mapping using thermoreflectance thermography has been conducted on the surface of power devices, as documented in [64]. A thermoreflectance thermography

setup with a 488-nm Ar-Ion laser system at 50-MHz frequency was used to capture thermal transients in [66]. This method enables submicron spatial resolution, making it highly effective for detecting hot spots and obtaining precise thermal readings. Thermoreflectance-based thermal imaging is currently the only known method that can capture submicron thermal information.

10.4.1.2 Electroluminescence-Based Thermal Monitoring

Electroluminescence is a well-established concept, referring to the emission of electromagnetic radiation when a material absorbs energy, typically through an electric current or electric field. It is driven by radiative recombination, where a free electron combines with a positively charged ion (exciton), resulting in the emission of a photon. This phenomenon occurs in direct bandgap semiconductors, such as amorphous silicon and silicon carbide (SiC), where there is no change in momentum during the transition of an electron from the valence band to the conduction band. Consequently, SiC exhibits strong electroluminescence due to radiative recombination. The intensity of electroluminescence in semiconductor devices is influenced by the material's bandgap and doping concentration. Higher impurity concentrations lead to increased electron-hole recombination events and, consequently, higher luminescence intensity. Compound semiconductors like gallium nitride (GaN) and indium gallium nitride (InGaN) are renowned for their high electroluminescence efficiency and find applications in light-emitting diodes (LEDs) and laser diodes. The intensity of electroluminescence is also temperature-dependent, as well as wavelength-dependent. By calibrating the spectral density of the emitted light at a specific wavelength, it is possible to determine the junction temperature. The relationship between the electroluminescence spectrum and the junction temperature of LEDs has been studied in previous research [67, 68].

Electroluminescence-based junction temperature estimation is being successfully implemented in wide-direct bandgap devices, such as SiC MOSFETs. The MOSFET devices have an inherent structure that allows for the formation of a PN junction between the source and drain terminals, known as the body diode. Figure 10.7 illustrates the schematic representation of the body diode in a vertical MOSFET construction, accompanied by photon emission resulting from the radiation recombination mechanism. By operating the SiC MOSFET in reverse bias through the body diode, the junction temperature can be determined. The intrinsic body diode of SiC MOSFETs emits visible blue light, which is dependent on the device's current and junction temperature [69, 70]. In a study by Luo et al. [71], a simultaneous extraction method for junction temperature and drain current was demonstrated for SiC MOSFETs based on the device's electroluminescence effect. Two spectral peaks were observed: at a wavelength of 390 nm, the luminescence intensity increases with temperature, while an inverse relationship was observed at a wavelength of 510 nm. Another study [72] measured SiC light emission by retrofitting a silicon PiN photodiode into a SiC module. Numerous researchers have successfully estimated the junction temperature of SiC MOSFETs using the

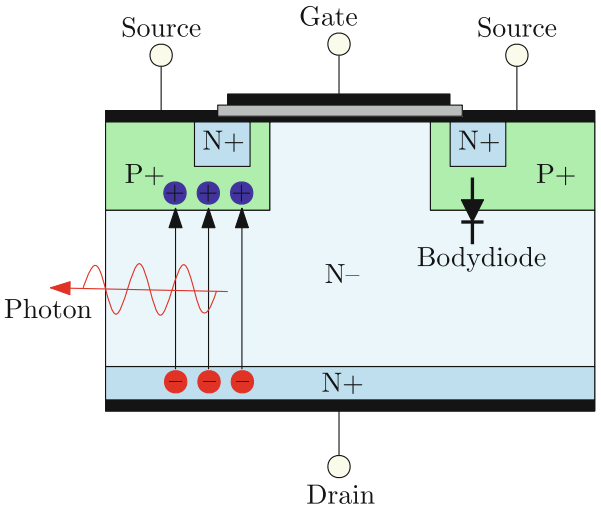


Fig. 10.7 Radiative recombination mechanism emitting photons on a SiC vertical MOSFET operating under reverse conduction is schematically shown as a symmetric structure

electroluminescence effect, making it a promising and noninvasive method for temperature monitoring [73, 74]. Likewise, porous SiC has been reported to yield temperature-dependent photoluminescence properties [75].

10.4.2 Thermal Test Chips

Thermal test chips (TTCs) are specialized devices fabricated using the same process technology as semiconductor devices. These chips are equipped with built-in heating and temperature sensing elements, enabling engineers to characterize the thermal behavior of interconnect materials, optimize package thermal performance, and evaluate the effectiveness of thermal interface materials (TIMs). Test chips from Thermal Engineering Associates (TEA) [76] contain two metal film resistors, covering approximately 86% of the active surface area, and strategically placed diodes for temperature sensing. Another example is the TTC designed and fabricated by Sattari et al. [77], which contains three resistance-based temperature detectors (RTDs) and six heaters distributed across a 4 mm $\times$ 4 mm area. Metal RTDs offer several advantages over diodes due to their higher sensitivity to temperature. However, the resistance sensitivity of an RTD relies on the temperature coefficient of resistance (TCR) of the base material. In a study conducted by Sattari et al. [78], TTCs were utilized to characterize nano metallic silver and copper sinter joints.

The fabrication of thermal test chips (TTCs) is relatively straightforward and can be performed on various semiconductor substrates. The process begins with depositing an oxide (or) a nitride passivation layer using either chemical vapor deposition

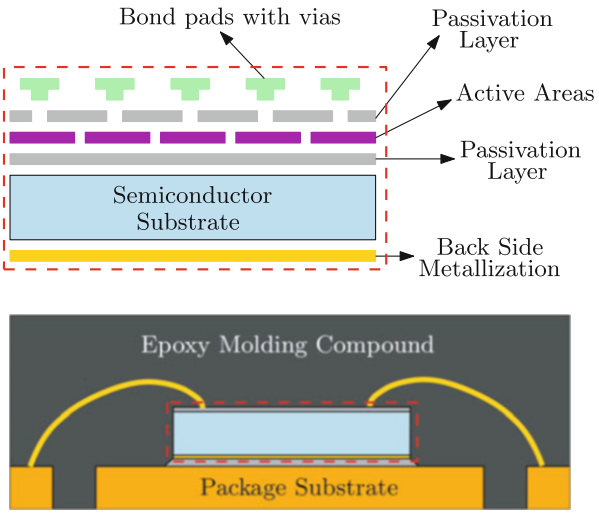


Fig. 10.8 A schematic illustration of fabricating a relatively simple thermal test chip with active areas (heating and sensing) is shown. The realized TTCs are assembled into packages to optimize the package's thermal performance

(CVD) or plasma-enhanced CVD (PECVD). Subsequently, the active areas, which include the heating and sensing elements, are defined through lithography. Another passivation layer is then applied over the active areas, with vertical vias spacing provided for electrical interconnects. Additionally, a bond pad is created for wire bonding or solder bumps. To enhance adhesion with the die-attach material, the backside of the semiconductor substrate is metalized. Finally, the wafer is cut into individual dies, which are assembled into packages for characterization. The steps involved in this process are depicted schematically in Fig. 10.8. The fabrication of TTCs follows similar processes as semiconductor devices, and their design can be customized to meet specific requirements. Consequently, TTCs offer an appealing solution for package thermal optimization.

The integration of thermal test chips (TTCs) into functional power quad flat no-lead (PQFN) surface-mount packages for package reliability analysis has been demonstrated in [79]. Furthermore, TTCs have been utilized for characterizing diamond heat spreaders in advanced packaging solutions [80]. Diamond is renowned for its exceptional thermal conductivity but relatively low thermal capacity, making it an ideal material for heat-spreading applications. To validate the heat-spreading effects across an active device surface, TTCs are particularly well-suited due to their multiple temperature-sensing elements. Numerous researchers have explored the integration of on-chip temperature sensors in electronic modules to analyze the device's thermal performance [81, 82].

10.4.3 Thermal-Pixel Test Chips

Thermal-pixel test chips, similar to TTCs, have been developed as a nondestructive method for detecting interface delaminations. These test chips, as demonstrated in [83–87], incorporate thermoelectrical transducers known as "thixels" that operate based on the 3-omega (3ω) principle. The 3ω method is widely recognized for its precise measurement of the thermal conductivity of thin films. By applying an electrical current (I) at an angular frequency of 1ω, joule heating ($Q = I^2R$) occurs at a higher frequency of 2ω. The amplitude and phase of temperature fluctuations depend on the material's thermal properties. This perturbation in the heating element's electrical resistance at 2ω is amplified by the driving current at 1ω, resulting in a small voltage signal across the heating element at a frequency of 3ω [88].

Wunderle et al. [83–85] employed the same process technology used for semiconductor devices to fabricate thermal-pixel test chips, which featured an array of 3ω structures patterned on a glass wafer. Each 3ω transceiver on the test chip emitted a thermal wave into the surrounding materials, and the wave was reflected upon interaction with an interface. The thermal wavelength depended on the material and the frequency of the AC signal. When a crack or delamination was present near a 3ω transceiver, the reflected signal caused an increase in the 3ω voltage. By analyzing the reflected signals, packaging defects in the vicinity of the transceiver could be identified. Recent advancements have focused on fabricating thermal pixels on a silicon substrate using flip-chip technology, allowing for higher thixel density and enabling the detection of on-chip interface delaminations and thermal inhomogeneities [86, 87].

10.4.4 Temperature-Sensitive Electrical Parameters

Monitoring the device junction temperature by measuring the temperature-sensitive electrical parameters (TSEPs) of semiconductor devices is an effective method for reliability monitoring. Temperature has a profound influence on the properties of materials at the atomic and molecular levels. Atoms vibrate more vigorously with increasing temperature, affecting the kinetic energy and leading to changes in the electrical, magnetic, and mechanical properties of materials. In metals, elevated temperatures intensify atomic collisions, impeding the flow of electrons and causing an increase in electrical resistance. Similarly, temperature variations impact the conductivity and carrier mobility of semiconductors. Various temperature-dependent factors, such as charge carrier mobility, doping concentration, and bandgap energy, determine the performance of semiconductor devices [49]. Consequently, electrical measurements can be correlated to device temperature. For a comprehensive understanding of the temperature dependence of semiconductor bandgaps and the underlying principles of power semiconductor devices, refer to [89, 90].

All previously mentioned thermal measurement methods require physical or visual access to the semiconductor device. In contrast, measuring the device TSEP enables estimating the device junction temperature without the need for direct chip access. However, the TSEP assumes a uniform temperature over the complete device, which may not hold true in reality due to surface thermal gradients. Additionally, the TSEP method may not be applicable when the device's electrical parameters exhibit high nonlinearity with temperature. A study on various temperature-sensitive electrical parameters of Si, SiC, and GaN power transistors is provided in [91, 92]. In this subsection, we present the temperature dependence of two such parameters of a through-hole (TO)-packaged N-channel silicon power MOSFET device: the forward bias on-state resistance $R_{DS}(on)$ and the reverse conduction source-drain voltage V_{SD}. It is essential to realize that the TSEP may vary depending on the type of device (e.g., bipolar junction transistor, field-effect transistor, diode) and the semiconductor material.

10.4.4.1 On-State Resistance R_{DS}*(on)*

Among the various electrical parameters, the on-state resistance $R_{DS}(on)$ is a critical parameter. It represents the resistance measured across the drain-source terminals of a MOSFET device under forward bias conditions. In a vertical MOSFET configuration, the drain terminal is located at the bottom of the die and is electrically connected to the die pad of the package. Therefore, the measured $R_{DS}(on)$ includes the resistance contributions from multiple components. It is the sum of the semiconductor device resistance under on-state conditions (R_{Die}), the die-attach resistance (R_{DA}), and the package substrate (leadframe) resistance (R_{LF}). The semiconductor device resistance under on-state conditions (R_{Die}) depends on the device structures (trench or lateral). The R_{Die} comprises of the channel resistance (R_{CH}), drift region resistance (R_{drift}), and substrate resistance (R_{sub}). The wire bond resistances R_{wire} can be neglected assuming 4-point Kelvin contacts. All other contact resistances are denoted as R_C. Therefore, the expression for the drain-source on-state resistance $R_{DS}(on)$ of a packaged device can be defined as follows:

$$R_{DS}(ON) \approx R_{CH} + R_{drift} + R_{sub} + R_{DA} + R_{LF} + R_C \tag{10.7}$$

The $R_{DS}(on)$ parameter varies for different devices depending on the semiconductor material and the package assembly processes. Furthermore, the $R_{DS}(on)$ is temperature-dependent, and the temperature coefficient(s) of $R_{DS}(on)$ is dependent on its operating characteristics. For instance, when a MOSFET device is turned on, there are two effects that determine the device's behavior with temperature. With increasing temperature, the device threshold voltage reduces, which allows more current to flow through the device than at lower temperatures. In contrast, with increasing temperature, the thermal resistance property of silicon also increases, thereby reducing the flow of current. The resultant effect leads to a critical current limit (at zero temperature coefficient [ZTC]), below which the temperature

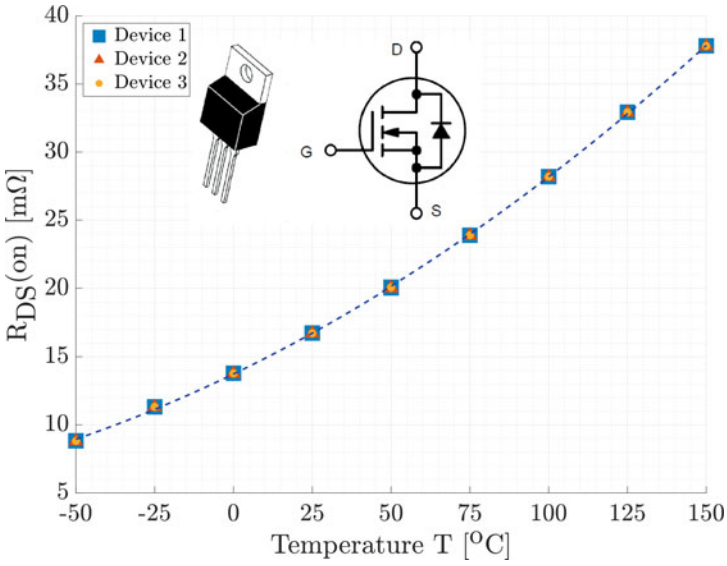


Fig. 10.9 $R_{DS}(on)$ of multiple N-Channel Silicon Power MOSFETs assembled in Through-Hole (TO) packages were measured inside a climate-controlled oven at nine different temperatures between −50°C to +150°C. A Gate-Source voltage V_{GS} of 10 V is applied with a drain current I_D of 1 A

coefficient experiences a change in sign (negative to positive), and the device experiences a risk of thermal runaway. Therefore, it is essential to understand the device characteristics and it is crucial to calibrate every device to establish the relationship between the electrical on-state resistance $R_{DS}(on)$ parameter and the device temperature.

To exemplify, multiple commercially available N-channel silicon power MOSFETs in through-hole (TO) packages were measured in a climate-controlled oven at temperatures from −50°C to +150°C (see Fig. 10.9). The device was operated in forward bias with a gate-source voltage V_{GS} of 10 V and a drain current I_D of 1 A. The resulting voltage difference across the drain-source terminal V_{DS} was measured at different temperatures. Thereby, a relationship between the device's on-state resistance and temperature was established. Consequently, the device's junction temperature during operation can be extracted by measuring its on-state resistance. Similar temperature-dependent $R_{DS}(on)$ measurements on SiC devices have been demonstrated in [93]. Moreover, other parameters such as turn-on saturation current and threshold voltage also have strong temperature dependence (when the device is fully open $R_{CH} << R_{DS}(on)$) that is used to estimate the junction temperature of SiC power MOSFETs in [94].

10.4.4.2 Source-Drain Voltage V_{SD} *Under Reverse Bias (Body Diode)*

As previously mentioned, silicon and SiC MOSFETs possess a PN junction between their source and drain terminals, known as the body diode. This body diode enables conduction in the reverse direction when the gate is off. In power electronics applications, the body diode plays a crucial role in dissipating inductive energy and protecting the MOSFET and circuits from voltage spikes. Tiwari et al. [95] demonstrated that the body diode of SiC FETs can safely dissipate inductive energy. Furthermore, a comprehensive analysis of the switching performance and robustness of power MOSFETs' body diodes is provided in [96]. During reverse conduction, the resistance across the various layers in a packaged device remains relatively the same. However, the current direction is reversed, flowing through the body diode, resulting in a voltage drop across the source-drain terminals denoted as V_{SD}.

The N-channel silicon power MOSFETs in TO packages were measured by applying a gate-source voltage V_{GS} of 0 V, and a negative potential difference was applied between the drain-source terminal ($-V_{DS} = +V_{SD}$) with a source current I_S of 1 A. The voltage difference between the source-drain terminals (V_{SD}) was measured inside a climate-controlled oven at nine different temperatures from -50°C to $+150$°C. The relationship between the source-drain voltage (V_{SD}) and temperature is illustrated in Fig. 10.10. A similar experimental investigation of

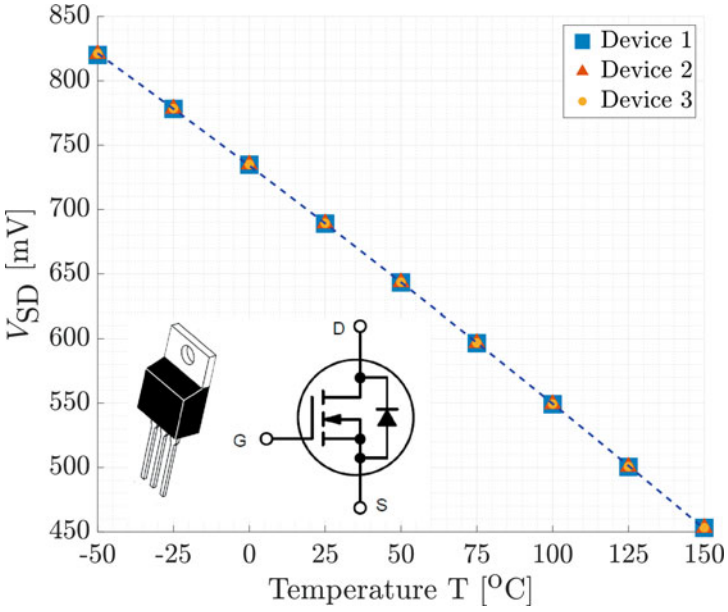


Fig. 10.10 The V_{SD} of multiple N-channel silicon power MOSFETs assembled in TO packages were measured inside a climate-controlled oven at nine different temperatures between -50°C and $+150$°C. A gate-to-source continuous voltage V_{GS} of 0 V is applied with a source current I_S of 1 A

the source-drain voltage (V_{SD}) for temperature estimation during power cycling tests was conducted in [97]. With the increasing demand for SiC MOSFETs in automotive inverter technology, recent research publications indicate the usage of the intrinsic body diode of SiC devices for junction temperature estimation. The body diode of SiC MOSFETs experiences interface traps when the gate-source terminal is set to zero volts ($V_{GS} = 0$). To mitigate this issue, an alternative approach is to set the gate-source terminal to negative voltages ($V_{GS} < 0V$) on SiC devices [98]. The body diode, also called a parasitic diode, proves to be a valuable component for accurately estimating the device junction temperature without needing external sensing elements. In [99, 100], the junction temperature measurements obtained using the TSEP method were compared with measurements from an IR camera to assess its accuracy.

10.5 Comparison of the Different Measurement Methods for Reliability Monitoring

A summary of the measurement methods discussed in the previous section is presented in Table 10.1, providing an overview of their merits and limitations. Directly probing a thermocouple on the active device surface is a cost-effective approach. Still, it necessitates physical access and relies on the accuracy of surface contact, making it less desirable despite its affordability. Optical inspection offers a contactless and noninvasive means of temperature determination. Infrared (IR) thermography is widely employed for temperature distribution analysis, but the working environment can influence their effectiveness. Fiber-optic thermal sensors, on the other hand, offer immunity to electromagnetic radiation, making them suitable for harsh and hazardous conditions. However, both IR and fiber-optic sensors are limited to surface measurements. Thermoreflectance-based thermography stands out as the method capable of detecting surface temperatures at submicron resolution, enabling the identification of microthermal hot spots. The transparency of certain materials can be achieved by tuning the illumination wavelength, although this requires complex processes and meticulous calibrations. With the increasing use of SiC MOSFETs, the electroluminescent property of wide-direct bandgap materials emitting visible blue light during reverse conduction has gained attention. Extracting device temperature by calibrating the spectral intensity at a specific wavelength poses a significant challenge. Despite optical methods' nonintrusive and noninvasive nature, visual access to the device is typically required.

Thermal test chips (TTCs) can be designed for application requirements, allowing engineers to optimize the package's thermal performance. The TTCs consist of embedded temperature-sensitive heating and sensing elements, offering a noninvasive alternate solution to probing a thermocouple onto the device's surface. Recent developments focus on incorporating mechanical strain sensors into the TTCs. However, test chips require additional input/output readout in real-life applications. A recent advancement is the thermal-pixel (thixel) test chip, which

Table 10.1 A comparative summary of the various measurement methodologies are listed with each of its working principle, measurement parameters, advantages, and limitations. To visually represent the strengths and weaknesses of each measurement method, we have ranked them into five categories: cost, complexity, online monitoring capability, accuracy, and intrusiveness. The ranking system ranges from 1 to 5, i.e., the most positive (green-shaded area) to the most negative (red-shaded area) outcome

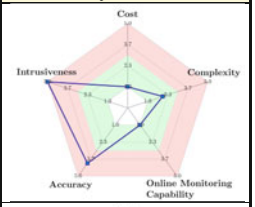
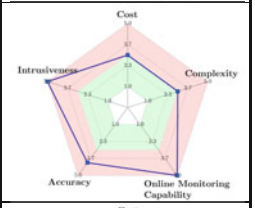
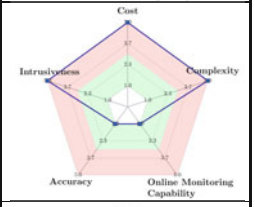
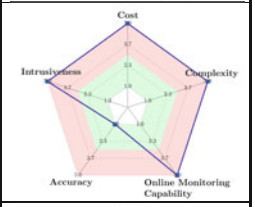
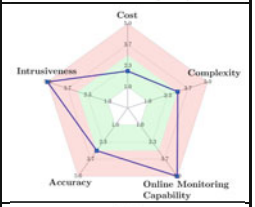
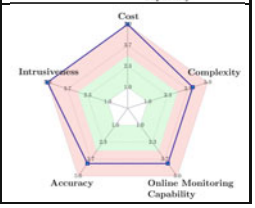
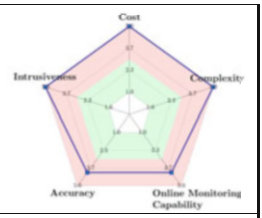
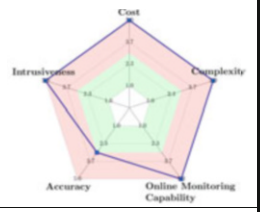
Measurement Method	Working Principle	Measurement Parameter	Advantages	Disadvantages	Graphical Representation
Direct Contact (Thermocouples)	Physical Probing (Seebeck effect)	Voltage / Temperature	1. Low cost. 2. Easy to Implement 3. Suitable for online monitoring.	1. Low Resolution. 2. Contact inaccuracies. 3. Needs physical access to the chip.	
IR Thermography (Optical)	IR Radiation Detection	IR radiation / Temperature	1. Contactless and non-destructive method. 2. Wide temperature range (up to 2000^{o}C). 3. High Resolution. 4. Rapid detection technique.	1. Surface measurement only. 2. Sensitive to emissivity. 3. Accuracy can be biased by its working ambient. 4. Low to High Cost. 5. Requires visual access to the chip.	
Fiber Optic Thermal Sensors (Optical)	Radiation / Fluorescence / Interferometric / Fiber Bragg Grating	Temperature	1. Small size, contactless, and non-destructive. 2. Highly temperature sensitive 3. Immune to EM radiation. 4. Wide temperature range (-200^{o}C to 1000^{o}C). 5. Fast response time.	1. Surface measurement only. 2. Difficult to calibrate. 3. Complex installation and needs visual access. 4. High cost and Fragile components.	
Thermo-reflectance (Optical)	Temperature-dependent Surface Reflectivity	Reflectivity / Temperature	1. Sub-micron spatial resolution. 2. Contactless and non-destructive method. 3. Transparency. 4. Wide temperature range 5. Highly temperature sensitive. 6. Fast response time.	1. Requires reflective surface (material dependent). 3. Difficult to calibrate. 4. Complex installation and need visual access. 5. High cost and requires dedicated setup.	
Electro-luminescence (Optical)	Radiative Recombination	Spectral Intensity / Temperature	1. Contactless and non-destructive method. 2. Low cost - Suitable to measure with optical cameras. 3. Sensitivity and response time depends on the detectors.	1. Surface measurement only. 2. Radiative recombination works only on SiC and amorphous Silicon 3. Difficult to calibrate. 4. Need visual access to the chip.	
Thermal Test Chips (TTC)	Electrical	Resistance / Voltage / Temperature	1. Package optimization, and interface characterization. 2. Same process technology as semiconductor devices. 3. Design to requirements. 4. Small and compact.	1. High Cost. 2. Limited spatial resolution. 3. Limited flexibility. 4. Requires specific electrical layout and direct access.	

Table 10.1 (continued)

Thermal-Pixel Test Chips	3ω	Voltage	1. Ideal alternative for acoustic imaging to detect delaminations. 2. Same process technology as semiconductor devices. 3. Small and compact. 4. Suitable to integrate on real functional power devices.	1. Expensive and under development. 2. High computational power (Depending on thixel density). 3. Resolution is proportional to thixel density. 4. Complex integration. 5. Requires specific electrical layout and direct access.	
Acoustic Imaging	Reflection of Ultrasound	Acoustic Impedance	1. Contactless (Non-invasive). 2. Non-destructive method. 3. High resolution and accurate. 4. Various scanning methods (Lateral and through scan with single and sequential steps).	1. High Cost and complex. 2. Ultrasound attenuation depending on materials. 3. Misinterpretation. 4. Direct access and water as a medium.	
Temperature-Sensitive Electrical Parameters (TSEP)	Electrical	Resistance / Voltage / Temperature	1. Non-invasive, non-destructive. 2. Real-time monitoring. 3. High-temperature sensitivity 4. No external sensors 5. Wide temperature range. 6. No visual access is needed. 7. fast time-transients.	1. Assumes uniform temperature distribution. 2. Complex semiconductor device phenomenon can lead to a high non-linearity. 3. High signal-to-noise ratio.	

utilizes transceivers to emit and receive thermal signals for detecting packaging defects. This approach presents an appealing alternative to acoustic imaging. However, it is important to note that acoustic microscopy offers a unique advantage over other monitoring methods. It enables nondestructive imaging of samples with buried interfaces, providing spatial and depth information. Nonetheless, acoustic imaging requires a dedicated setup and water as a coupling medium.

The temperature-sensitive electrical parameter (TSEP) is a promising methodology for real-time online condition monitoring, as it eliminates the need for external temperature sensing devices. Unlike other methodologies that require direct chip access, the TSEP allows for the extraction of device junction temperature based on its inherent property. The device's on-state resistance $R_{DS}(on)$, which exhibits a strong temperature dependence, serves as a key performance indicator for MOSFETs. Monitoring the on-state resistance over the device's lifetime provides valuable insights into its electrical and thermal performance. However, it is essential to acknowledge that this method assumes a uniform temperature distribution across the device, which may not reflect the actual temperature gradients. This could lead to an underestimation of the device's temperature. Furthermore, the signal-to-noise ratio is influenced by the transient measurement time. Therefore, each method has its own advantages and limitations, making it necessary to carefully choose the measurement method based on the application.

10.6 Conclusion

As global concerns over environmental sustainability and energy conservation intensify, there is an increasing demand for renewable energy generation, energy-efficient systems, industrial carbon-neutral commitments, and electric vehicle transportation. At the core of such transitional technologies lies power electronic devices, which are pivotal in elevating these systems to higher levels of efficiency and performance. However, ensuring the reliability of power semiconductor devices is paramount to ensure the long-term viability and widespread adoption of energy-efficient technologies. This chapter has presented a comprehensive outlook on the current state of power electronics, emphasizing its reliability concerns in field-critical applications, elucidating dominant degradation mechanisms encompassing both chip-related and package-related aspects, and exploring advanced measurement methodologies for reliability monitoring.

Diverse sectors, including low-power consumer electronics, high-value automotive electric vehicles, and high-power industrial applications, drive the global demand for power electronic devices. However, such field-critical applications have been surveyed to suffer from more than 20% of unscheduled maintenance and repairs. The growing concerns on power device reliability and increasing environmental awareness have prompted the establishment of stringent reliability requirements (e.g., *Automotive AEC-Q100/101—2000 thermal cycles* $-55°C/+150°C$ *for highest Grade 0*) and safety regulations (e.g., *lead [Pb] solder replacement and poly-fluoroalkyl [PFA]-free substances*) for semiconductor device manufacturers. The pursuit of higher efficiency and higher reliability has also led to a transition in reliability metrics. The empirical-model-based failure in time (FIT) and mean time to failure (MTTF) approaches are being superseded by remaining useful life (RUL) prediction. The semiconductor industry and academia have invested considerable efforts in developing new measurement methods for reliability/condition monitoring to facilitate reliability prediction. This chapter has provided a comprehensive overview of various measurement methods, including their underlying physical principles. Based on a thorough review of these techniques, a summary that highlights their respective advantages and limitations was further presented. A multivariate radar chart has been included to interpret the comparison visually. This chart plots the measurement techniques based on five key categories: cost, complexity, online monitoring capability, accuracy, and intrusiveness. The radar chart clearly and concisely depicts the strengths and weaknesses of each measurement method, enabling readers to make informed decisions.

Investigating failure and degradation mechanisms is crucial for developing high-efficiency and highly reliable power devices. However, reliability monitoring methods are required for seamless, non-interruptive system operation. Monitoring the device condition makes early detection of faults possible, leading to efficient maintenance strategies and minimizing costly downtime. The integration of reliability monitoring methods, coupled with a deeper understanding of degradation mechanisms, provides a comprehensive and proactive approach to enhancing the reliability of power electronics. Such efforts are crucial in building a sustainable

future where energy-efficient and reliable power systems are pivotal in advancing technology, industry, and society.

References

1. Wang, H. et al. (2014). Transitioning to physics-of-failure as a reliability driver in power electronics. *IEEE Journal of Emerging and Selected Topics in Power Electronics, 2*(1), 97–114. https://doi.org/10.1109/JESTPE.2013.2290282.
2. Modarres, M. (2012). The evolution and history of reliability engineering: Rise of mechanistic reliability modeling. *International Journal of Performability Engineering, 8*, 35.
3. Wang, H., & Blaabjerg, F. (2020). Power electronics reliability: State of the art and outlook. *IEEE Journal of Emerging and Selected Topics in Power Electronics, 9*(6), 6476–6493. https://doi.org/10.1109/JESTPE.2020.3037161.
4. (2018). *Rongen, r. on the evolution of qualification methods and standards for microelectronics in automotive applications beyond aec-qxx. in plot conference*. veldhoven.
5. (2022). *Newsletter m24, volume 3, intelligent reliability 4.0 (irel40)*.
6. Wang, H., Ma, K., & Blaabjerg, F. (2012). Design for reliability of power electronic systems. In: *IECON 2012—38th annual conference on IEEE industrial electronics society* (pp. 33–44). https://doi.org/10.1109/IECON.2012.6388833.
7. Olivares, C., Rahman, R., Stankus, C., Hampton, J., Zedwick, A., & Ahmed, M. (2021). *Predicting power electronics device reliability under extreme conditions with machine learning algorithms*. arXiv: 2107.10292 [cs.LG].
8. Yang, S., Xiang, D., Bryant, A., Mawby, P., Ran, L., & Tavner, P. (2010). Condition monitoring for device reliability in power electronic converters: A review. *IEEE Transactions on Power Electronics, 25*, 2734–2752. https://doi.org/10.1109/TPEL.2010.2049377.
9. Baker, N., Liserre, M., Dupont, L., & Avenas, Y. (2014). Improved reliability of power modules: A review of online junction temperature measurement methods. *IEEE Industrial Electronics Magazine, 8*(3), 17–27. https://doi.org/10.1109/MIE.2014.2312427.
10. Ni, Z., Lyu, X., Yadav, O. P., Singh, B. N., Zheng, S., & Cao, D. (2020). Overview of real-time lifetime prediction and extension for sic power converters. *IEEE Transactions on Power Electronics, 35*(8), 7765–7794. https://doi.org/10.1109/TPEL.2019.2962503.
11. Ciappa, M., Carbognani, F., & Fichtner, W. (2003). Lifetime modeling of thermomechanics-related failure mechanisms in high power IGBT modules for traction applications. In *Proceedings of the 2003 IEEE 15th international symposium on power semiconductor devices and ICs, 2003 (ISPSD '03)* (pp. 295–298). https://doi.org/10.1109/ISPSD.2003.1225286.
12. Ceccarelli, L., Kotecha, R. M., Bahman, A. S., Iannuzzo, F., & Mantooth, H. A. (2019). Mission-profile-based lifetime prediction for a SiC mosfet power module using a multi-step condition-mapping simulation strategy. *IEEE Transactions on Power Electronics, 34*(10), 9698–9708. https://doi.org/10.1109/TPEL.2019.2893636.
13. Bludau, W., Onton, A., & Heinke, W. (2003). Temperature dependence of the band gap of silicon. *Journal of Applied Physics, 45*(4), 1846–1848. ISSN: 0021-8979. https://doi.org/10.1063/1.1663501. eprint: https://pubs.aip.org/aip/jap/article-pdf/45/4/1846/7952763/1846\T1\textbackslash_1\T1\textbackslash_online.pdf.
14. Rahmani, M., et al. (2017). Reversible thermal tuning of all-dielectric metasurfaces. *Advanced Functional Materials, 27*, 1700580. https://doi.org/10.1002/adfm.201700580.
15. (2021) *Status of the power electronics industry 2021 (market & technology report). yole developpement*.
16. Robles, E., Pérez, A., Fernández, M., Aretxabaleta Astoreka, I., Andreu Larrañaga, J., Fernández Zubizarreta, M., & Martín González, J. L. (2022). The role of power device technology in the electric vehicle powertrain. *International Journal of Energy Research, 46*(15). https://doi.org/10.1002/er.8581.

17. Abdalgader, I. A. S., Kivrak, S., & Özer, T. (2022). Power performance comparison of SiC-IGBT and Si-IGBT switches in a three-phase inverter for aircraft applications. *Micromachines, 13*(2). ISSN: 2072-666X. https://doi.org/10.3390/mi13020313. https://www.mdpi.com/2072-666X/13/2/313.
18. Yang, S., Bryant, A., Mawby, P., Xiang, D., Ran, L., & Tavner, P. (2011). An industry-based survey of reliability in power electronic converters. *IEEE Transactions on Industry Applications, 47*(3), 1441–1451. https://doi.org/10.1109/TIA.2011.2124436.
19. Hahn, B., Durstewitz, M., & Rohrig, K. (2006). Reliability of wind turbines: Experiences of 15 years with 1500 wts. In: *Fraunhofer IWES*.
20. Chai, Q., Zhang, C., Dong, Z., & Xu, Y. (2021). Operational reliability assessment of photovoltaic inverters considering voltage/var control function. *Electric Power Systems Research, 190*, 106706. https://doi.org/10.1016/j.epsr.2020.106706.
21. Moore, L., & Post, H. (2008). Five years of operating experience at a large, utility-scale photovoltaic generating plant. *Progress in Photovoltaics: Research and Applications, 16*, 249–259. https://doi.org/10.1002/pip.800.
22. Hu, K., Liu, Z., Yang, Y., Iannuzzo, F., & Blaabjerg, F. (2020). Ensuring a reliable operation of two-level IGBT-based power converters: A review of monitoring and fault-tolerant approaches. *IEEE Access, 8*, 89988–90022. https://doi.org/10.1109/ACCESS.2020.2994368.
23. Sathik, M. H. M., Prasanth, S., Sasongko, F., & Pou, J. (2018). Lifetime estimation of off-the-shelf aerospace power converters. *IEEE Aerospace and Electronic Systems Magazine, 33*(12), 26–38. https://doi.org/10.1109/MAES.2018.180030.
24. *Vishay siliconix, "power mosfet failures in automotive applications," application note 910.*
25. Bernstein, J., Gurfinkel, M., Li, X., Walters, J., Shapira, Y., & Talmor, M. (2006). Electronic circuit reliability modeling. *Microelectronics Reliability, 46*, 1957–1979. https://doi.org/10.1016/j.microrel.2005.12.004.
26. Young, D., & Christou, A. (1994). Failure mechanism models for electromigration. *IEEE Transactions on Reliability, 43*(2), 186–192. https://doi.org/10.1109/24.294986.
27. Mangalagiri, P., Bae, S., Krishnan, R., Xie, Y., & Narayanan, V. (2008). Thermal-aware reliability analysis for platform FPGAS. In *2008 IEEE/ACM international conference on computer-aided design* (pp. 722–727). https://doi.org/10.1109/ICCAD.2008.4681656.
28. Lacerda de Orio, R. (2010). Electromigration modeling and simulation. In *Dissertation, Technische Universität Wien*. https://resolver.obvsg.at/urn:nbn:at:at-ubtuw:1-33806.
29. Srinivasan, J., Adve, S., Bose, P., & Rivers, J. (2004). The impact of technology scaling on lifetime reliability. In *International conference on dependable systems and networks, 2004* (pp. 177–186). https://doi.org/10.1109/DSN.2004.1311888.
30. Groeseneken, G., Degraeve, R., Nigam, T., Van den bosch, G., & Maes, H. (1999). Hot carrier degradation and time-dependent dielectric breakdown in oxides. Microelectronic Engineering, 49(1), 27–40. Reliability in VLSI Circuits: Operation, Manufacturing and Design, ISSN: 0167-9317. https://doi.org/10.1016/S0167-9317(99)00427-X. https://www.sciencedirect.com/science/article/pii/S016793179900427X.
31. *Seyab, msk., haron, nzb., & hamdioui, s. (2008). cmos scaling impacts on reliability, what do we understand? in s.n. (ed.), 19th annual workshop on circuits, systems and signal processing* (pp. 260-266). stw.
32. Suehle, J. (2002). Ultrathin gate oxide reliability: Physical models, statistics, and characterization. *IEEE Transactions on Electron Devices, 49*(6), 958–971. https://doi.org/10.1109/TED.2002.1003712.
33. Wu, E. et al. (2002). Interplay of voltage and temperature acceleration of oxide breakdown for ultra-thin gate oxides. *Solid-State Electronics, 46*, 1787–1798. https://doi.org/10.1016/S0038-1101(02)00151-X.
34. Oberg, D., Wert, J., Normand, E., Majewski, P., & Wender, S. (1996). First observations of power MOSFET burnout with high energy neutrons. *IEEE Transactions on Nuclear Science, 43*(6), 2913–2920. https://doi.org/10.1109/23.556885.
35. Hands, A., et al. (2011). Single event effects in power MOSFETs due to atmospheric and thermal neutrons. *IEEE Transactions on Nuclear Science, 58*(6), 2687–2694. https://doi.org/10.1109/TNS.2011.2168540.

36. Jansen, K., Zhang, M., Ernst, L., Vu, D.-K., & Weiss, L. (2020). Effect of temperature and humidity on moisture diffusion in an epoxy moulding compound material. *Microelectronics Reliability, 107*, 113596. ISSN: 0026-2714. https://doi.org/10.1016/j.microrel.2020.113596. https://www.sciencedirect.com/science/article/pii/S0026271419311771.
37. Segbefia, O. K., Imenes, A. G., & Sætre, T. O. (2021). Moisture ingress in photovoltaic modules: A review. *Solar Energy, 224*, 889–906. ISSN: 0038-092X. https://doi.org/10.1016/j.solener.2021.06.055. https://www.sciencedirect.com/science/article/pii/S0038092X21005375.
38. Inamdar, A., Yang, Y. H., Prisacaru, A., Gromala, P., & Han, B. (2021). High temperature aging of epoxy-based molding compound and its effect on mechanical behavior of molded electronic package. English, *Polymer Degradation and Stability, 188*. ISSN: 0141-3910. https://doi.org/10.1016/j.polymdegradstab.2021.109572.
39. Inamdar, A. et al., Study of thermal aging behavior of epoxy molding compound for applications in harsh environments. In *2019 IEEE 69th Electronic components and technology conference (ECTC)* (2019), pp. 811–818. https://doi.org/10.1109/ECTC.2019.00128.
40. Inamdar, A., Gromala, P. J., Prisacaru, A., Kabakchiev, A., Yang, Y. H., & Han, B. (2022). EMC oxidation under high temperature aging. In W. D. van Driel & M. Y. Mehr (Eds.). *Reliability of organic compounds in microelectronics and optoelectronics* (1st ed., pp. 53–80). Springer. ISBN: 978-3-030-81575-2. https://doi.org/10.1007/978-3-030-81576-9_3.
41. Meier, M. R., & Schweigart, H. (2022). Corrosion in power electronics. In *CIPS 2022; 12th International Conference on Integrated Power Electronics Systems* (pp. 1–5).
42. Behrendt, S. (2022). Investigation of inorganic encapsulated power modules with enhanced cooling possibilities. In *2022 IEEE 9th electronics system-integration technology conference (ESTC)* (pp. 446–451). https://doi.org/10.1109/ESTC55720.2022.9939500.
43. Naumann, F., Boettge, B., Behrendt, S., Eisele, R., & Klengel, S. (2020). Numerical material design for reliable power electronics with cement-based encapsulation. In *CIPS 2020; 11th international conference on integrated power electronics systems* (pp. 1–6).
44. Bouarroudj Berkani, M. (2008). *Study of thermomechanical fatigue of power electronic modules under high environemental temperatures for automotive applications*.
45. Noh, S., Zhang, H., Yeom, J., Chen, C., Li, C., & Suganuma, K. (2018). Large-area die-attachment by silver stress migration bonding for power device applications. *Microelectronics Reliability, 88–90*, 701–706. 29th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2018). ISSN: 0026-2714. https://doi.org/10.1016/j.microrel.2018.07.131. https://www.sciencedirect.com/science/article/pii/S0026271418307121.
46. Oh, C., Nagao, S., & Suganuma, K. (2015). Silver stress migration bonding driven by thermomechanical stress with various substrates. *Journal of Materials Science: Materials in Electronics, 26*, 2525–2530. https://doi.org/10.1007/s10854-015-2717-9.
47. Hanif, A., Yu, Y., DeVoto, D., & Khan, F. (2019). A comprehensive review toward the state-of-the-art in failure and lifetime predictions of power electronic devices. *IEEE Transactions on Power Electronics, 34*(5), 4729–4746. https://doi.org/10.1109/TPEL.2018.2860587.
48. Held, M., Jacob, P., Nicoletti, G., Scacco, P., & Poech, M.-H. (1997). Fast power cycling test of IGBT modules in traction application. In *Proceedings of second international conference on power electronics and drive systems* (vol. 1), pp. 425–430. ISBN: 0-7803-3773-5. https://doi.org/10.1109/PEDS.1997.618742.
49. Susinni, G., Rizzo, S. A., & Iannuzzo, F. (2021). Two decades of condition monitoring methods for power devices. *Electronics, 10*(6), 683.
50. Sundaram, A., & Velraj, R. (2008). Thermal management of electronics: A review of literature. *Thermal Science—THERM SCI, 12*, 5–26. https://doi.org/10.2298/TSCI0802005A.
51. Blaabjerg, F., Wang, H., Vernica, I., Liu, B., & Davari, P. (2021). Reliability of power electronic systems for EV/HEV applications. *Proceedings of the IEEE, 109*(6), 1060–1076. https://doi.org/10.1109/JPROC.2020.3031041.
52. Yu, H. (2020). Scanning acoustic microscopy for material evaluation. *Applied Microscopy, 50*, 25. https://doi.org/10.1186/s42649-020-00045-4.

53. Bertocci, F., Grandoni, A., & Djuric-Rissner, T. (2019). Scanning acoustic microscopy (SAM): A robust method for defect detection during the manufacturing process of ultrasound probes for medical imaging. *Sensors, 19*, 4868. https://doi.org/10.3390/s19224868.
54. Levikari, S., Kärkkäinen, T. J., Andersson, C., Tammminen, J., & Silventoinen, P. (2019). Acoustic detection of cracks and delamination in multilayer ceramic capacitors. *IEEE Transactions on Industry Applications, 55*(2), 1787–1794. https://doi.org/10.1109/TIA.2018.2873989.
55. Usamentiaga, R., Pablo, V., Guerediaga, J., Vega, L., Molleda, J., & Bulnes, F. (2014). Infrared thermography for temperature measurement and non-destructive testing. *Sensors (Basel, Switzerland), 14*, 12305–12348. https://doi.org/10.3390/s140712305.
56. Greppmair, A. et al. (2016). Measurement of the in-plane thermal conductivity by steady-state infrared thermography. *The Review of Scientific Instruments, 88*(4), 044903.
57. Ma, S. et al. (2022). Optical fiber sensors for high-temperature monitoring: A review. *Sensors, 22*(15). ISSN: 1424–8220. https://www.mdpi.com/1424-8220/22/15/5722.
58. Khatir, Z., Carubelli, S., & Lecoq, F. (2004). Real-time computation of thermal constraints in multichip power electronic devices. *IEEE Transactions on Components and Packaging Technologies, 27*(2), 337–344. https://doi.org/10.1109/TCAPT.2004.828563.
59. Stoib, B. et al. (2014). Spatially resolved determination of thermal conductivity by raman spectroscopy. *Semiconductor Science and Technology, 29*(12), 124 005. https://doi.org/10.1088/0268-1242/29/12/124005.
60. Kumar, D., Choudhury, R., & Layek, A. (2022). Application of liquid crystal thermography for temperature measurement of the absorber plate of solar air heater. *Materials Today: Proceedings, 59*, 605–611. Third International Conference on Recent Advances in Materials and Manufacturing 2021, ISSN: 2214-7853. https://doi.org/10.1016/j.matpr.2021.12.091. https://www.sciencedirect.com/science/article/pii/S2214785321077634.
61. Braun, J. L., Olson, D. H., Gaskins, J. T., & Hopkins, P. E. (2019). A steady-state thermoreflectance method to measure thermal conductivity. *The Review of Scientific Instruments, 90*(2), 024905.
62. Wilson, R. B., Apgar, B. A., Martin, L. W., & Cahill, D. G. (2012). Thermoreflectance of metal transducers for optical pump-probe studies of thermal properties. *Optics Express, 20*(27), 28829–28838. https://doi.org/10.1364/OE.20.028829. https://opg.optica.org/oe/abstract.cfm?URI=oe-20-27-28829.
63. Wang, Y., Park, J., Koh, Y., & Cahill, D. (2010). Thermoreflectance of metal transducers for time-domain thermoreflectance. *Journal of Applied Physics, 108*, 043507–043507. https://doi.org/10.1063/1.3457151.
64. Rossi, L., Breglio, G., Irace, A., & Spirito, P. (2006). Thermal mapping of power devices with a completely automated thermoreflectance measurement system. In *2006 Ph.D. Research in Microelectronics and Electronics* (pp. 41–44). https://doi.org/10.1109/RME.2006.1689891.
65. Metayrek, Y., Kociniewski, T., & Khatir, Z. (2020). Thermal mapping at the cell level of chips in power modules through the silicone gel using thermoreflectance. *Microelectronics Reliability, 105*, 113563. ISSN: 0026-2714. https://doi.org/10.1016/j.microrel.2019.113563. https://www.sciencedirect.com/science/article/pii/S0026271419309904.
66. Komarov, P., Burzo, M., & Raad, P. (2006). A thermoreflectance thermography system for measuring the transient surface temperature field of activated electronic devices. In *Twenty-Second annual IEEE semiconductor thermal measurement and management symposium* (vol. 2006, pp. 199–203). ISBN: 1-4244-0153-4. https://doi.org/10.1109/STHERM.2006.1625228.
67. Vaskuri, A. et al. (2018). Relationships between junction temperature, electroluminescence spectrum and ageing of light-emitting diodes. *Metrologia, 55*(2), S86. https://doi.org/10.1088/1681-7575/aaaed2.
68. Cengiz, C., Azarifar, M., & Arik, M. (2022). A critical review on the junction temperature measurement of light emitting diodes. *Micromachines, 13*, 1615. https://doi.org/10.3390/mi13101615.
69. Winkler, J., Homoth, J., & Kallfass, I. (2018). Utilization of parasitic luminescence from power semiconductor devices for current sensing. In *PCIM Europe 2018; International*

Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (pp. 1–8).
70. Ruppert, L., Kalker, S., Van der Broeck, C., & De Doncker, R. (2021). Analyzing spectral electroluminescence sensitivities of SiC MOSFETs and their impact on power device monitoring.
71. Luo, H., Mao, J., Li, C., Iannuzzo, F., Li, W., & He, X. (2022). Online junction temperature and current simultaneous extraction for SiC MOSFETs with electroluminescence effect. *IEEE Transactions on Power Electronics, 37*(1), 21–25. https://doi.org/10.1109/TPEL.2021.3094924.
72. Ceccarelli, L., Luo, H., & Iannuzzo, F. (2018). Investigating SiC MOSFET body diode's light emission as temperature-sensitive electrical parameter. *Microelectronics Reliability, 88*, 627–630. https://doi.org/10.1016/j.microrel.2018.07.027.
73. Li, C., Lu, Z., Wu, H., Li, W., He, X., & Li, S. (2019). Junction temperature measurement based on electroluminescence effect in body diode of SiC power MOSFET. In *2019 IEEE applied power electronics conference and exposition (APEC)* (pp. 338–343). https://doi.org/10.1109/APEC.2019.8722249.
74. (2020). A non-invasive SiC MOSFET junction temperature estimation method based on the transient light emission from the intrinsic body diode. *Microelectronics Reliability, 114*, 113845. 31st European Symposium on Reliability of Electron Devices, Failure Physics and Analysis, ESREF 2020, ISSN: 0026-2714. https://doi.org/10.1016/j.microrel.2020.113845. https://www.sciencedirect.com/science/article/pii/S0026271420306168.
75. Lu, W., Tarekegne, A., Ou, Y., Kamiyama, S., & Ou, H. (2019). Temperature-dependent photoluminescence properties of porous fluorescent SiC. *Scientific Reports, 9*, 16333. https://doi.org/10.1038/s41598-019-52871-6.
76. Siegal, B., & Galloway, J. (2008). Thermal test chip design and performance considerations. In *2008 Twenty-fourth annual IEEE semiconductor thermal measurement and management symposium* (pp. 59–62). https://doi.org/10.1109/STHERM.2008.4509367.
77. Sattari, R., van Zeijl, H., & Zhang, G. (2021). Design and fabrication of a multi-functional programmable thermal test chip. In *2021 23rd European microelectronics and packaging conference exhibition (EMPC)* (pp. 1–7). https://doi.org/10.23919/EMPC53418.2021.9584984.
78. Sattari, R., Hu, D., Liu, X., van Zeijl, H., Vollebregt, S., & Zhang, G. (2023). Transient thermal measurement on nano-metallic sintered die-attach joints using a thermal test chip. *Applied Thermal Engineering, 221*, 119503. ISSN: 1359-4311. https://doi.org/10.1016/j.applthermaleng.2022.119503. https://www.sciencedirect.com/science/article/pii/S1359431122014338.
79. Martin, H. A., Sattari, R., Smits, E. C. P., van Zeijl, H. W., van Driel, W. D., & Zhang, G. Q. (2022). In-situ reliability monitoring of power packages using a thermal test chip. In *2022 23rd International conference on thermal, mechanical and multi-physics simulation and experiments in microelectronics and microsystems (EuroSimE)* (pp. 1–10). https://doi.org/10.1109/EuroSimE54907.2022.9758913.
80. Martin, H., et al. (2023). Heterogeneous integration of diamond heat spreaders for power electronics application. In *2023 IEEE 73rd electronic components and technology conference (ECTC)*. https://doi.org/10.1109/ECTC51909.2023.00029.
81. Motto, E. R., & Donlon, J. F. (2012). IGBT module with user accessible on-chip current and temperature sensors. In *2012 Twenty- Seventh annual IEEE applied power electronics conference and exposition (APEC)* (pp. 176–181). https://doi.org/10.1109/APEC.2012.6165816.
82. Zhou, Y., et al. (2017). Dynamic junction temperature estimation via built-in negative thermal coefficient (NTC) thermistor in high power IGBT modules. In *2017 IEEE applied power electronics conference and exposition (APEC)* (pp. 772–775). https://doi.org/10.1109/APEC.2017.7930782.
83. Wunderle, B., May, D., Ras, M. A., & Keller, J. (2017). Non-destructive in-situ monitoring of delamination of buried interfaces by a thermal pixel (Thixel) chip. In *2017 16th IEEE intersociety conference on thermal and thermomechanical phenomena in electronic systems (ITherm)* (pp. 1238–1246). https://doi.org/10.1109/ITHERM.2017.7992626.

84. Wunderle, B., et al. (2018). Spatially resolved, non-destructive in-situ detection of interface degradation by remote electrical readout of an on-chip thermal pixel (Thixel) matrix. In *2018 7th Electronic system-integration technology conference (ESTC)* (pp. 1–7). https://doi.org/10.1109/ESTC.2018.8546437.
85. Wunderle, B., et al. (2016). In-situ monitoring of interface delamination by local thermal transducers exemplified for a flip-chip package. In *2016 22nd International workshop on thermal investigations of ICs and systems (THERMINIC)* (pp. 230–235). https://doi.org/10.1109/THERMINIC.2016.7749057.
86. Kumar, A., et al. (2019). Latest advancements towards delamination detection in a FCOB assembly using thermal pixel (Thixel) array. In *2019 25th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)* (pp. 1–7). https://doi.org/10.1109/THERMINIC.2019.8923388.
87. Kumar, A., et al. (2018). Delamination detection in an electronic package by means of a newly developed delamination chip based on thermal pixel (Thixel) array. In *2018 7th Electronic System-Integration Technology Conference (ESTC)* (pp. 1–7).
88. Dames, C. (2013). *Chapter 2 measuring the thermal conductivity of thin films: 3 omega and related electrothermal*.
89. O'Donnell, K., & Chen, X. (1991). Temperature dependence of semiconductor band gaps. *Applied Physics Letters, 58*, 2924–2926. https://doi.org/10.1063/1.104723.
90. Baliga, B. (2010). *Fundamentals of power semiconductor devices*. Springer. ISBN: 9780387473147. https://books.google.nl/books?id=UiqrUWrYZXkC.
91. Zhang, L., Liu, P., Guo, S., & Huang, A. Q. (2016). Comparative study of temperature sensitive electrical parameters (TSEP) of Si, SiC and GaN power devices. In *2016 IEEE 4th workshop on wide bandgap power devices and applications (WiPDA)* (pp. 302–307). https://doi.org/10.1109/WiPDA.2016.7799957.
92. Zhu, S., Fayyaz, A., & Castellazzi, A. (2018). *Static and dynamic TSEPS of SiC and GaN transistors*.
93. Guo, H., Guo, C., Wei, L., & Liu, Y. (2021). Junction temperature measurement method for thermal resistance testing of SiC MOSFET module. *Journal of Physics: Conference Series, 1907*, 012012. https://doi.org/10.1088/1742-6596/1907/1/012012.
94. Yang, H.-C., Simanjorang, R., & See, K. (2019). A method of junction temperature estimation for SiC power MOSFETs via turn-on saturation current measurement. *IEEJ Journal of Industry Applications, 8*, 306–313. https://doi.org/10.1541/ieejjia.8.306.
95. Tiwari, S., Abuishmais, I., Langelid, J. K., Lund, R., Midtgård, O., & Undeland, T. M. (2018). Characterization of body diodes in the-state-of-the-art SiC FETS-are they good enough as freewheeling diodes?. In *2018 20th European conference on power electronics and applications (EPE'18 ECCE Europe)* (pp. P.1–P.10).
96. Jahdi, S., et al. (2015). An analysis of the switching performance and robustness of power MOSFETs body diodes: A technology evaluation. *IEEE Transactions on Power Electronics, 30*(5), 2383–2394. https://doi.org/10.1109/TPEL.2014.2338792.
97. Hoffmann, F., & Kaminski, N. (2019). Evaluation of the V_{SD}-method for temperature estimation during power cycling of SIC-MOSFETs. *IET Power Electronics, 12*(15), 3903–3909. https://doi.org/10.1049/iet-pel.2018.6369.
98. Nguyen, Q., Tounsi, P., Fradin, J.-P., & Reynes, J.-M. (2020). *Investigation on the use of the MOSFET SiC body diode for junction temperature measurement*.
99. Dupont, L., Avenas, Y., & Jeannin, P.-O. (2012). Comparison of junction temperature evaluations in a power IGBT module using an IR camera and three thermo-sensitive electrical parameters. In *2012 Twenty-Seventh annual IEEE applied power electronics conference and exposition (APEC)* (pp. 182–189). https://doi.org/10.1109/APEC.2012.6165817.
100. Dupont, L., Avenas, Y., & Jeannin, P.-O. (2013). Comparison of junction temperature evaluations in a power IGBT module using an ir camera and three thermosensitive electrical parameters. *IEEE Transactions on Industry Applications, 49*(4), 1599–1608. https://doi.org/10.1109/TIA.2013.2255852.