A 40.68-MHz Dual-Output Wireless Power Transfer System for Millimeter-Scale Biomedical Implants

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***Abstract*—This article presents a single-link, dual-output wireless power transfer (WPT) system operating at 40.68 MHz for miniature, high-power biomedical implants. The elevated carrier frequency enables a millimeter-scale receiver (RX) coil while maintaining link efficiency and output power comparable to low-frequency WPT designs. End-to-end (E2E) efficiency is optimized through global power modulation using a dynamic OFF-time (DOT) algorithm in conjunction with a fully integrated load-shift-keying (LSK) uplink. At the RX, a single-stage dual-output resonant-current-mode (DORCM) rectifier with single-mode zero-crossing-based control achieves zero-voltage switching (ZVS) and robust adaptability over varying coupling conditions. At the transmitter (TX), an adaptive-ZVS (AZVS) class-D power amplifier (PA) minimizes switching losses and electromagnetic interference (EMI). Both the TX and RX chips are fabricated in a 180-nm BCD process. Measurement results demonstrate dual-output voltage regulation at 1.2 and 2 V under DOT control (DOT Ctrl), with smooth switching behaviors observed at both the TX and RX. The DORCM RX supports seamless cold-start-up operation and achieves a peak power conversion efficiency (PCE) of 90.3% at 90.4-mW output power. The peak E2E efficiency is 51.2% at a coupling factor of $k = 0.2$. Enabling DOT modulation improves E2E efficiency by up to 18.2%, corresponding to a 2.2× reduction in TX input power. The system delivers up to 149.7-mW output power with a TX input voltage of 5 V.**

***Index Terms*—40.68 MHz, dual-output, dynamic OFF-time (DOT), global power modulation, load shift keying, miniature biomedical implant, resonant current-mode rectifier, wireless power transfer (WPT), zero-voltage switching (ZVS).**

I. Introduction

WIRELESS power transfer (WPT) is a promising non-invasive technology for powering implantable medical devices (IMDs), such as neural interfaces, retinal implants, and pacemakers [1], [2]. These IMDs demand compact and power-efficient system designs due to stringent anatomical, thermal, surgical, and biocompatibility constraints. Specifically, the implantation site around or within the human eye offers only millimeter-scale space. Despite this, retinal implants support complex functionality, including neural stimulation, data telemetry, and image processing, which typically requires tens of milliwatts of power supply [1], [2]. This introduces critical challenges for the WPT system design, as illustrated in Fig. 1. The receiver (RX) must be both highly efficient and miniaturized. The overall end-to-end (E2E) efficiency must be optimized to ensure sufficient power delivery and long-life operation of the wearable transmitter (TX). Additionally, adaptability to varying coupling conditions is essential for maintaining reliable power flow under varying alignment and loading scenarios.

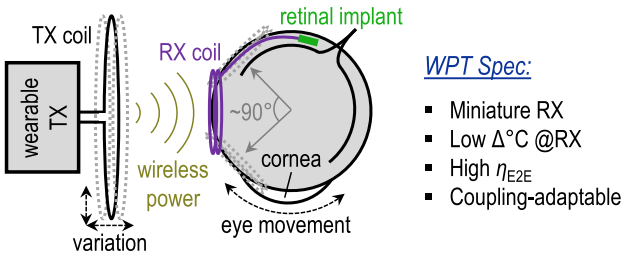

Fig. 1. WPT for retinal implants.

Several techniques have been proposed to address the aforementioned challenges. At the RX, active diodes and adaptive delay compensation techniques eliminate diode conduction losses and enable soft switching [3], [4], [5], [6]. In addition, single-stage regulating rectifiers have been proposed to replace the conventional two-stage architecture consisting of a rectifier and a dc–dc converter [7], [8], [9], [10], [11], [12], [13]. These designs directly modulate the rectifier operation to regulate the output voltage, enabling higher power conversion efficiency (PCE) and a more compact form factor. At the TX, power modulation dynamically aligns the TX drive with the RX load to improve E2E efficiency [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24]. Rather than conventional methods that adjust the TX supply via a dc–dc converter [15], recent single-stage TX architectures regulate power using pulse-modulation techniques such as pulse-duty control [17], [18], [21], [22], [23] and pulse-skipping control [14], [19], [24]. These approaches eliminate cascaded conversion losses and reduce component count. Since TX power modulation requires RX feedback, a backward data link is essential. While traditional systems employ separate data links, recent work demonstrates fully integrated through-power-link backscatter communication using load-shift-keying (LSK) techniques [19], [20], [22], [23], [24], further minimizing the number of components and enabling more compact, cost-effective implementations.

Though the aforementioned techniques enable high-performance biomedical WPT systems, most reported designs employ large-inductance RX coils with centimeter-scale

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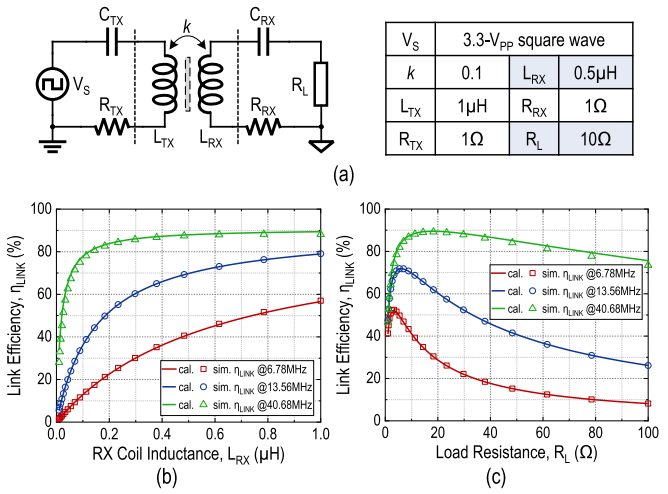


V_S	3.3-V_{PP} square wave		
k	0.1	L_{RX}	0.5μH
L_{TX}	1μH	R_{RX}	1Ω
R_{TX}	1Ω	R_L	10Ω

Fig. 2. WPT link efficiency analysis. (a) WPT link configuration. (b) η_{LINK} versus L_{RX}. (c) η_{LINK} versus R_L.

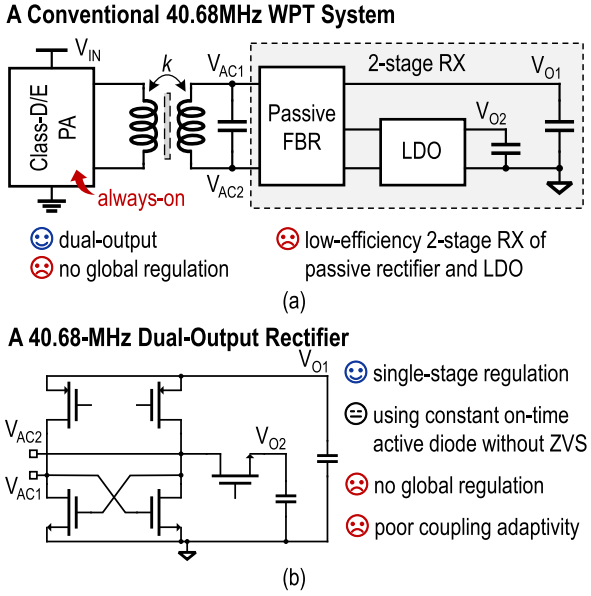


Fig. 3. Reported WPT designs at 40.68 MHz. (a) System design [27]. (b) Rectifier design [9].

dimensions, as they operate at relatively low industrial, scientific, and medical (ISM) frequency bands of 6.78 or 13.56 MHz. This design constraint can be understood by examining the relationship among link efficiency η_{LINK}, RX coil inductance L_{RX}, and carrier frequency f_C. Fig. 2(a) shows a WPT link model with series resonances at both the TX and RX, where R_{TX} and R_{RX} are the loop resistances in the respective L–C tanks. Based on electromagnetic theory and Kirchhoff's current law applied to both TX and RX sides [25], [26], the link efficiency, η_{LINK}, defined as the ratio of the power delivered to the load resistance R_L over the power drawn from the voltage source V_S, is given by

$$\eta_{LINK} = \frac{R_L}{R_{RX}+R_L} \cdot \frac{1}{1+\dfrac{R_{TX}(R_{RX}+R_L)}{k^2\omega^2 L_{TX}L_{RX}}} \tag{1}$$

where k is the coupling factor and $\omega = 2\pi f_C$. From (1), η_{LINK} increases with f_C for a given coil set, implying that higher carrier frequencies allow smaller coils without degrading efficiency. This trend is verified in Fig. 2(b), which plots η_{LINK} versus L_{RX} at $R_L = 10\ \Omega$. The solid curves represent analytical predictions from (1), and the discrete points are Cadence Virtuoso simulation results using identical parameters. The calculated and simulated results show close agreement. They confirm that achieving the same η_{LINK} at lower operating frequencies, such as 6.78 and 13.56 MHz, requires significantly larger L_{RX}, which implies physically larger RX coils if R_{RX} remains constant. Fig. 2(c) further explores the dependence of η_{LINK} on R_L at $L_{RX} = 0.5\ \mu H$. Except under extremely heavy load conditions, which are uncommon in biomedical applications, a higher f_C consistently yields higher η_{LINK}. Hence, prior WPT systems rely on centimetric coils to sustain adequate link efficiency and thus sufficient output power; however, this design choice limits their practical applicability in highly miniaturized biomedical implants.

Driven by practical application needs, 40.68-MHz WPT solutions have been investigated in advanced biomedical systems [27], [28]. Fig. 3(a) presents a WPT system used for a neural interface, reported in 2024 [27]. To support diverse bioelectronic functions, the system provides dual output voltages in different domains. However, the TX operates continuously without global power modulation, reducing the E2E efficiency under light-load conditions. In addition, the RX design employs a conventional two-stage architecture with passive diode conduction followed by a linear regulator, resulting in poor PCE and potential thermal safety concerns. Recent power management research at this frequency has primarily focused on improving RX performance [9], [29], [30]. For example, dedicated switching control, instead of delay compensation, has been developed for open-loop active rectifiers to mitigate substantial switching delays relative to the short resonant period (< 25 ns) at 40.68 MHz [30]. In 2023, the first regulating rectifier at this frequency was reported, which achieves single-stage dual-output regulation, as shown in Fig. 3(b) [9]. This design uses constant-on-time (5 ns) active diodes to simplify switching control, but incurs reverse currents and hard switching when coupling or load conditions vary. Moreover, it still omits global power modulation, and its full-bridge rectifier (FBR) topology yields a low voltage conversion ratio (VCR), making it unsuitable for loose-coupling scenarios with small RX coils.

State-of-the-art WPT systems integrate various technological advances to improve efficiency, output power, and compactness. However, most still require impractically large RX coils, and many techniques are not readily extendable to 40.68-MHz operation. While existing 40.68-MHz designs address specific application needs, they lack several key circuit innovations, leaving a gap between application requirements and practical implementation. This work presents a 40.68-MHz WPT system that achieves a millimeter-scale RX coil while delivering state-of-the-art power and efficiency [31]. The system incorporates: 1) global power modulation via a dynamic OFF-time (DOT) algorithm with an in-band LSK uplink; 2) a single-stage, dual-output resonant-current-mode

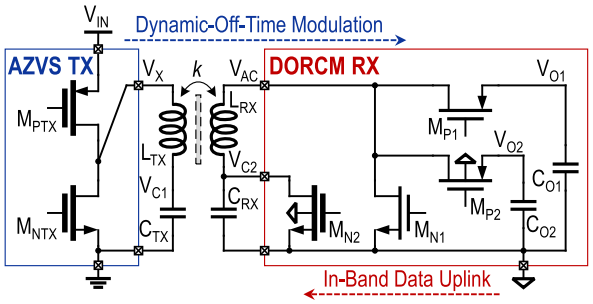


Fig. 4. Proposed 40.68-MHz WPT system topology.

(RCM) rectifier at the RX that achieves soft switching and robust adaptability to varying coupling; and 3) an adaptive zero-voltage-switching (AZVS) class-D PA at the TX that minimizes switching losses and electromagnetic interference (EMI). The remainder of this article is organized as follows. Section II introduces the proposed system topology and operation principle. Section III details the system and circuit implementations. Section IV shows the measurement results, and conclusions are drawn in Section V.

II. Proposed 40.68-MHz WPT System

The proposed WPT system topology is shown in Fig. 4, comprising three main stages: an AZVS TX, a dual-output RCM (DORCM) RX, and a wireless link. The AZVS TX employs a class-D power amplifier (PA), composed of M_{PTX} and M_{NTX}, to drive a series-resonant $\mathrm{L_{TX}}$–$\mathrm{C_{TX}}$ tank. The DORCM RX consists of four power transistors, M_{P1}, M_{P2}, M_{N1}, and M_{N2}, and two output capacitors, $\mathrm{C_{O1}}$ and $\mathrm{C_{O2}}$. M_{P2} and M_{N2} employ dynamic body biasing to prevent unintentional conduction under high V_{ac} or negative V_{C2} conditions. Considering applied voltage stress, M_{PTX}, M_{NTX}, and M_{N2} are implemented by 5-V MOSFET devices, while M_{P1}, M_{P2}, and M_{N1} are 2-V devices. The system adopts DOT-based power modulation, leveraging RX feedback from an in-band LSK uplink. To regulate the two dc output voltages and trigger the uplink signal, the RX operates in three distinct modes that collectively involve four operation phases, as detailed in Section II-A. The DOT-based modulation will be elaborated in Section II-B, and the system-level operation waveforms are presented in Section II-C.

A. DORCM Rectifier

A smaller RX coil weakens the wireless link and increases its sensitivity to misalignment and separation distance variations, thereby requiring a high-VCR RX. Voltage-mode (VM) rectifiers, such as the FBR and voltage doubler, offer limited VCRs and cannot adapt to varying coupling conditions, thus narrowing the operable range of a WPT system [32], [33]. Voltage-/current-mode (V/CM) rectifiers reported in [23] and [33] improve input sensitivity by entering RCM with a "resonance and charging" operation [34], [35]. However, their voltage-doubler-based structures essentially benefit only the VM operation rather than the RCM operation. As a result,

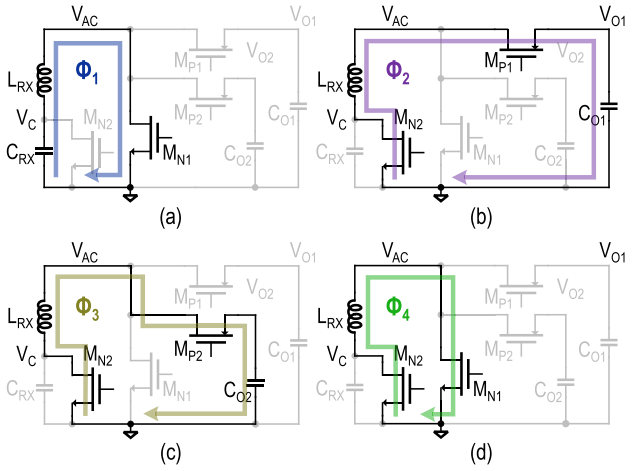


Fig. 5. Operation phases of the DORCM RX. (a) Resonance phase Φ_1. (b) V_{O1}-charging phase Φ_2. (c) V_{O2}-charging phase Φ_3. (d) Freewheeling phase Φ_4.

TABLE I
RX Mode-Phase Mapping

Mode @RX	MD_1	MD_2	MD_{LSK}
Phase operation	$\Phi_1 \leftrightarrow \Phi_2$	$\Phi_1 \leftrightarrow \Phi_3$	Φ_4

V/CM rectifiers are most effective when operated predominantly in VM. In contrast, given the weak and varying link in the proposed system, this work employs a dedicated RCM topology at the RX, achieving a high VCR while eliminating the need for complex control units.

The RX operates in four distinct phases: the resonance phase (Φ_1), V_{O1}-charging phase (Φ_2), V_{O2}-charging phase (Φ_3), and the freewheeling phase (Φ_4), as shown in Fig. 5(a)–(d), respectively. In Φ_1, only M_{N1} is turned on, allowing the $\mathrm{L_{RX}}$–$\mathrm{C_{RX}}$ tank to freely resonate and accumulate energy. In Φ_2, M_{P1} and M_{N2} are turned on, enabling $\mathrm{L_{RX}}$, as a current source, to deliver the accumulated charge to $\mathrm{C_{O1}}$. In Φ_3, M_{P2}, instead of M_{P1}, is turned on to direct charge to $\mathrm{C_{O2}}$ in a similar fashion. In Φ_4, M_{N1} and M_{N2} are turned on, shorting $\mathrm{L_{RX}}$ and thus interrupting the $\mathrm{L_{RX}}$-$\mathrm{C_{RX}}$ resonance.

Notably, the RX enables charging phases (Φ_2 and Φ_3) when I_{LRX} peaks, and M_{N2} bypasses $\mathrm{C_{RX}}$ in the charging phases, both actions ensuring residual-free charging [35]. In addition, series-LC RCM rectifiers can also achieve residual-free charging by enabling charging phases before I_{LRX} peaks and using both $\mathrm{L_{RX}}$ and $\mathrm{C_{RX}}$ as energy sources [36], [37]. However, such rectifiers require feedback control to detect the phase-switching point, making them unsuitable for coupling-varying operations. Therefore, this work adopts the proposed RX structure for its simple and robust control as well as high reliability.

Based on the four phases, the RX operates in three distinct modes to fulfill its functionality: V_{O1}-charging mode ($\mathrm{MD_1}$), V_{O2}-charging mode ($\mathrm{MD_2}$), and power-data uplink mode using LSK ($\mathrm{MD_{LSK}}$). The mapping between RX modes and phases is summarized in Table I. In $\mathrm{MD_1}$, the RX alternates between Φ_1 and Φ_2 to charge V_{O1}, while in $\mathrm{MD_2}$, it alternates between Φ_1

and Φ_3 to charge V_{O2}. In MD_{LSK}, the RX enters Φ_4, during which it presents a distinct reflected impedance at the TX than the normal charging modes MD_1 and MD_2. The reflected impedance, Z_{REF}, in both cases is expressed as

$$Z_{REF} = \begin{cases} \dfrac{\omega^2 k^2 L_{TX} L_{RX}}{R_{RX} + R_{ON}} \lambda, & (\text{in } MD_1, MD_2) \\ \dfrac{\omega^2 k^2 L_{TX} L_{RX}}{R_{RX} + j\omega L_{RX} + R_{ON}}, & (\text{in } MD_{LSK}) \end{cases} \quad (2)$$

where R_{RX} is the loop resistance in the L_{RX}-C_{RX} tank, R_{ON} denotes the ON-resistance of a power transistor, and λ is a near-unity factor representing the time-averaged impedance transformation of the RCM operation [33]. From (2), Z_{REF} is largely reduced in MD_{LSK}, resulting in an increased current amplitude in the L_{TX}–C_{TX} tank. This change enables the in-band data backscattering.

B. Global DOT Modulation

Global power modulation is an effective approach to improve E2E efficiency by adapting the TX power to varying RX load conditions. In [16], constant-OFF-time (COT) modulation was proposed, which disables the TX power stage for a fixed duration once the RX output voltage reaches its target level. This enables fully on/off TX operation and provides a wide power adjustment range. However, it suffers from poor load regulation and can induce large output voltage ripples under heavy-load conditions. Hysteresis control (Hyst), proposed in [19], maintains the RX output voltage in a hysteresis window, resulting in nearly load-independent output ripples. Nonetheless, it requires the TX to remain in a power-leaking standby mode, while the RX is off to detect the lower-threshold trigger, thereby narrowing the TX power adjustment range and reducing E2E efficiency under light-load conditions. Pulsewidth modulation (PWM) has been introduced to balance the tradeoff between output voltage ripple and E2E efficiency by adjusting TX's on/off duty ratio while keeping the total modulation period constant. PWM can be implemented using phase-locked-loop (PLL)-based analog methods [18], [22] or look-up table (LUT)-based digital methods [23], [38]. The analog approach offers tight voltage regulation but suffers from slow transient responses, whereas the digital method responds quickly to load transients but requires complex, area-consuming hardware implementations. In addition, the LUT size in [23] and [38] increases rapidly if the total modulation period is lengthened.

To overcome the limitations of prior approaches, DOT modulation is proposed. As shown in Fig. 6(a), the proposed DOT algorithm regulates the total modulation period (T_{TOT}), comprising a TX-on period (T_{ON}) and a TX-off period (T_{OFF}), within a hysteresis window centered at $m \times T_{RE}$ and bounded by a width of $2n \times T_{RE}$, where $T_{RE} = 1/f_C$ is the resonant period. When T_{TOT} exceeds the hysteresis boundaries (#1 → #2 or #4 → #5), the TX adjusts T_{OFF} stepwise (#2 → #3 → #4 or #5 → #6). To avoid oscillatory toggling in T_{TOT}, the adjustment step α should be set smaller than the hysteresis window width, which is given by

$$\frac{T_{OFF,i}}{T_{OFF,i\pm1}} = \frac{T_{TOT,i}}{T_{TOT,i\pm1}} = \alpha < \frac{m+n}{m-n} \quad (3)$$

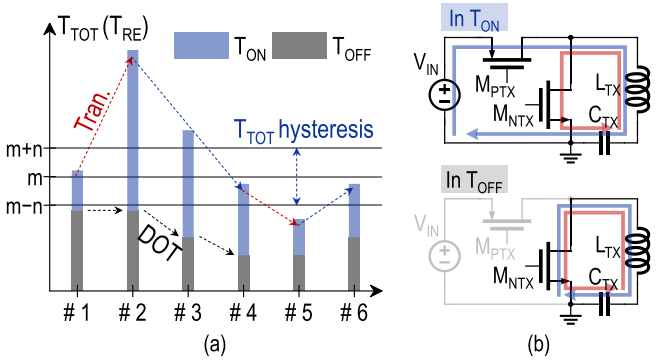


Fig. 6. DOT modulation. (a) Operation principle. (b) Corresponding TX operation phases.

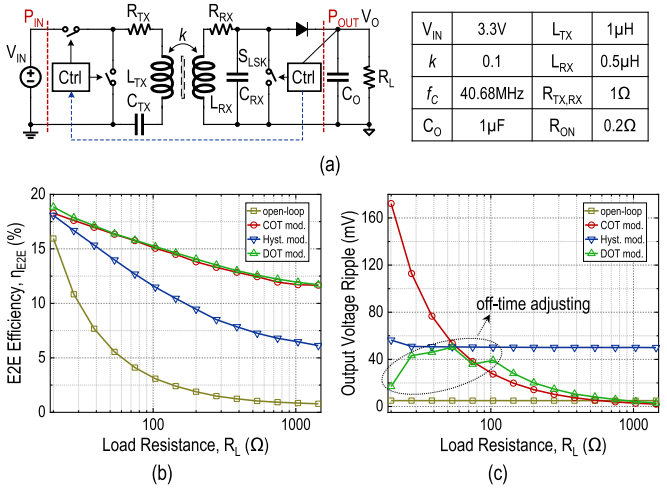
where the ± sign accounts for both increasing and decreasing T_{OFF} cases. Fig. 6(b) illustrates the two operation phases of the class-D PA TX: during T_{ON}, the class-D PA drives the L_{TX}–C_{TX} tank with symmetric pulsing (active state); during T_{OFF}, only M_{NTX} remains closed, allowing the L_{TX}–C_{TX} tank to freewheel without drawing power from V_{IN} (idle state).

From (3), a larger α yields a wider hysteresis window. A wide window can degrade load regulation (as in constant-ON-time control), whereas a small adjustment step can slow the transient response (as in analog PWM). In practice, α should be chosen to balance regulation accuracy and response speed based on application requirements. In this prototype, $m = 128 \times T_{RE}$ and $n = 32 \times T_{RE}$ are selected, resulting in $\alpha = 1.5$. The corresponding available T_{OFF} values are 0, 8, 12, 18, 27, 40, 60, and 90 ($\times T_{RE}$), where the value "0" is intentionally included to support extremely heavy-load conditions.

It is worth noting that the proposed global modulation method exhibits integral-like behavior without derivative action, which can result in slower load regulation. An additional local regulator can be used at the RX if faster output regulation is required. In addition, the DOT modulation operates as a discrete-time digital feedback loop. Though the uplink latency can introduce extra loop delay, stability is ensured by (1), the hysteresis window that bounds T_{TOT}, and (2), the fixed adjustment step $\alpha = 1.5$ that limits loop gain.

Compared to prior methods, the proposed DOT modulation enables fully on/off TX operation under regulation for improved E2E efficiency than Hyst, while achieving a smaller ripple by adjusting T_{OFF} than COT. Unlike analog PWM methods, the proposed scheme allows faster load transients without complex compensation. Compared to digital PWM methods, it offers slightly slower regulation but greatly simplifies the digital implementation by eliminating large LUTs and permits longer T_{TOT} settings to flexibly balance ripple and efficiency for different applications.

The proposed DOT method is further quantitatively compared against COT, Hyst, and open-loop control, as shown in Fig. 7. A class-D PA is adopted at the TX, and a half-bridge rectifier (HBR) is used at the RX [Fig. 7(a)]. When the RX output voltage V_O reaches 1.8 V, the backscattering switch S_{LSK} turns on, idling the HBR and switching the TX to the



V_{IN}	3.3V	L_{TX}	1μH
k	0.1	L_{RX}	0.5μH
f_C	40.68MHz	$R_{TX,RX}$	1Ω
C_O	1μF	R_{ON}	0.2Ω

Fig. 7. Comparison of global modulation methods. (a) WPT system implementation. (b) η_{E2E} versus R_L. (c) Output voltage ripple versus R_L.

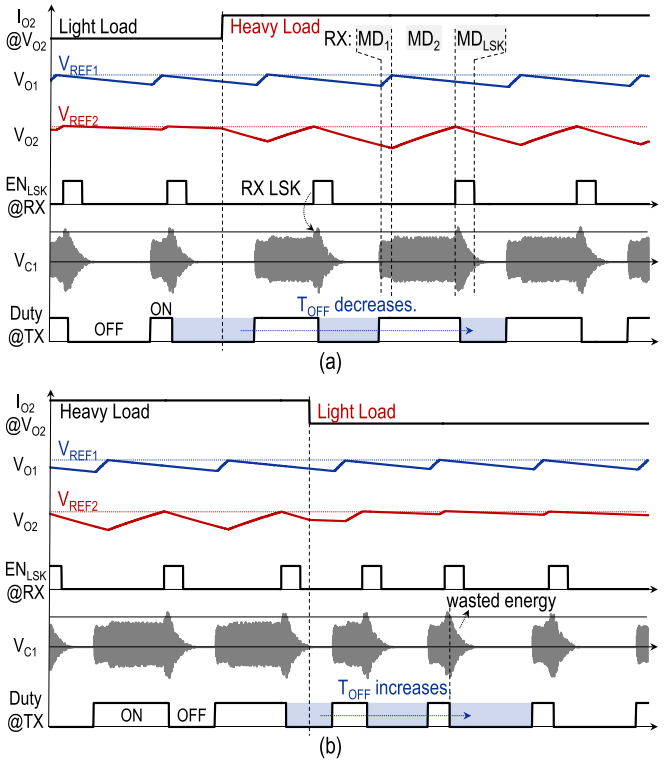


Fig. 8. System-level operation waveforms. (a) During a light-to-heavy load transient. (b) During a heavy-to-light load transient.

"OFF" state. For DOT and COT, the TX in the "OFF" state is fully disabled, as shown in Fig. 6(b). The DOT method employs the $\alpha = 1.5$ configuration, while COT applies a fixed TX-OFF period of 64 $\times$ T_{RE}. For Hyst, the TX in the "OFF" state periodically skips three positive drive pulses, resulting in 1/4 $\times$ output power. It resumes "ON" state when V_O drops below 1.75 V. For the open-loop method, the TX remains on, as shown in Fig. 6(a). All switches and the HBR diode are assumed to have identical ON-resistance, R_{ON}. The E2E efficiency, η_{E2E}, is defined as the ratio of P_{OUT} to P_{IN}.

Fig. 7(b) and (c) shows η_{E2E} and output voltage ripple, respectively, as functions of load resistance R_L ranging from 20 Ω to 1.5 kΩ. The DOT method presents a rough ripple profile because of the 1.5 $\times$ T_{OFF} adjustment step. The results confirm that DOT and COT modulation achieve high η_{E2E}, thanks to fully on/off TX operation. Meanwhile, DOT and Hyst exhibit small output voltage ripples, owing to their adjustable TX-OFF periods.

C. System-Level Operation

Fig. 8 presents the system-level operation waveforms. During a light-to-heavy load transition at V_{O2}, as shown in Fig. 8(a), T_{TOT} can exceed the upper hysteresis bound, and the DOT algorithm correspondingly shortens T_{OFF}, thereby suppressing the ripple on V_{O2}. Since T_{TOT} remains within the hysteresis window both before and after the transient, the charging/discharging duty ratio of V_{O1} may vary only slightly or remain unchanged, resulting in negligible ripple variation on V_{O1} across the transient. Notably, cross-regulation (undershoots) at V_{O1} may still occur during transients due to the temporarily extended T_{OFF}.

During each T_{ON}, the RX follows the sequence $MD_1 \Rightarrow MD_2 \Rightarrow MD_{LSK}$. Upon detecting the RX LSK, the TX evaluates whether T_{TOT} exceeds the hysteresis bounds and adjusts T_{OFF} accordingly.

Fig. 8(b) shows the waveforms during a heavy-to-light load transient at V_{O2}. In this case, T_{OFF} is increased if T_{TOT} falls below the lower hysteresis bound. Owing to instantaneous mode switching at the RX, no overshoots are observed at either V_{O2} or V_{O1}. In principle, when the RX is in MD_{LSK}, it stops receiving power from the TX, and the residual resonant energy in the L_{TX}–C_{TX} tank is likely wasted during T_{OFF}. Unlike COT, DOT modulation can extend T_{OFF} under light-load conditions, mitigating this negative impact on E2E efficiency.

III. System and Circuit Implementations

Fig. 9 shows the proposed WPT system architecture. At the TX, a 40.68-MHz clock signal, clk, drives the class-D PA and establishes the dead time between the gate driving signals V_{GP} and V_{GN}. Zero-voltage switching (ZVS) at node V_X is enabled by the AZVS control block (AZVS Ctrl), which is detailed in Section III-B. The uplink demodulation block (Uplink Dem) monitors the voltage amplitude across C_{TX} to detect the uplink signal from the RX [23]. Upon receiving an uplink pulse, the output of Uplink Dem, DE_{TX}, asserts high to initiate T_{TOT} hysteresis evaluation and pull down the latched signal V_{DUTY} within the DOT control (DOT Ctrl) block. This transitions the class-D PA into the idle state via the driving control (Driving Ctrl) block. If T_{TOT} exceeds its hysteresis window [96 $\times$ T_{RE}, 160 $\times$ T_{RE}], the DOT Ctrl block updates the multiplexer selection to modify the subsequent T_{OFF}. When T_{OFF} ends, a logic-high output from the T_{OFF} counter sets V_{DUTY} high again, triggering the class-D PA back to the active state.

At the RX, M_{N2} is driven by an adaptive gate driver that can clamp its gate voltage to the lower of V_{C2} and ground, ensuring reliable turn-off during the resonance phase (Φ_1) [11],

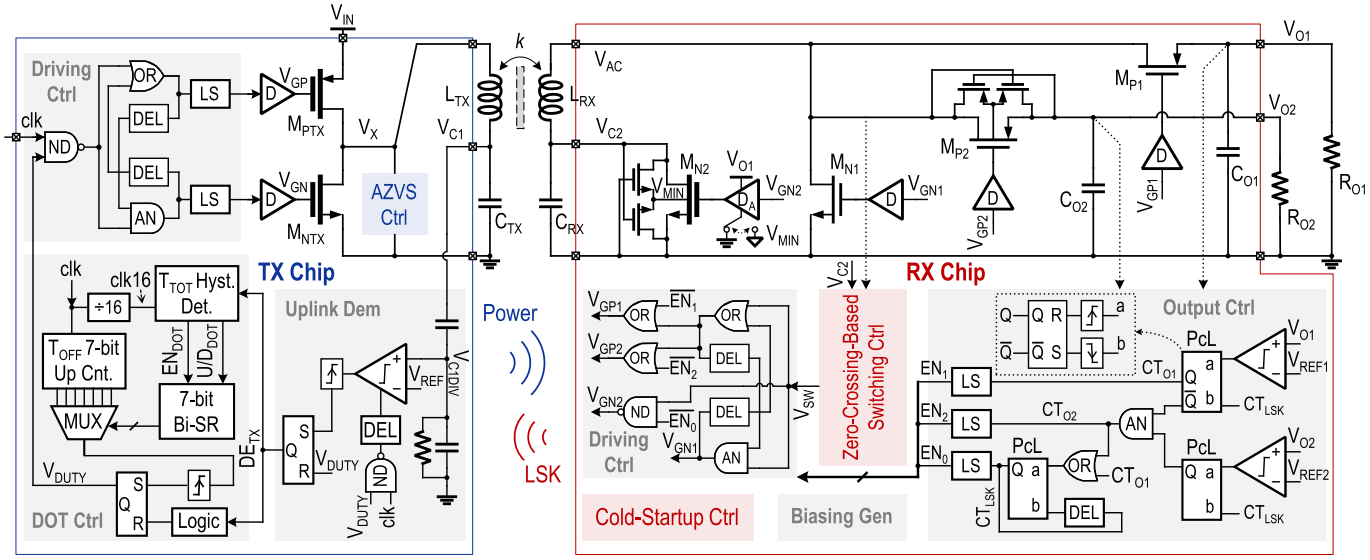


Fig. 9. System architecture of the proposed 40.68-MHz single-link dual-output WPT system.

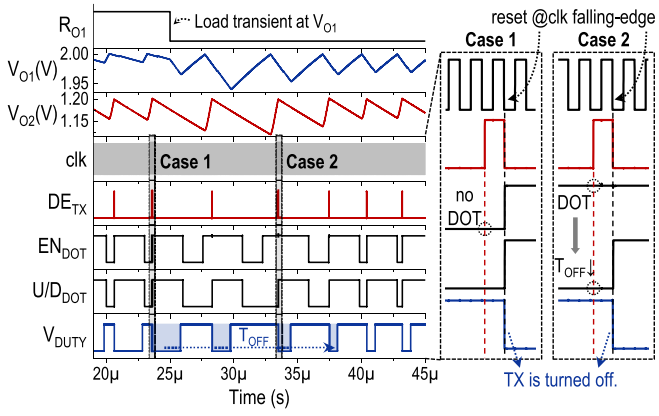
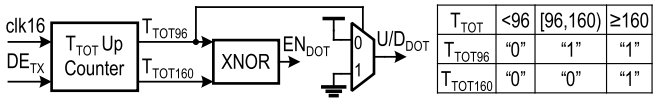


Fig. 10. Simulated waveform of the DOT Ctrl block.



T_{TOT}	<96	[96,160)	≥160
T_{TOT96}	"0"	"1"	"1"
T_{TOT160}	"0"	"0"	"1"

Fig. 11. Circuit implementation of T_{TOT} hysteresis detector.

[35]. The dc output voltages V_{O1} and V_{O2} are compared with reference voltages V_{REF1} and V_{REF2}, respectively, within the output control (Output Ctrl) block. The comparison results are latched by pulse-controlled latches (PcLs) to generate three time-multiplexed enable signals, EN_1, EN_2, and EN_0, only one of which is asserted high at any given time to indicate the RX operation mode. The RX switching behavior is governed by the zero-crossing-based switching control block (Switching Ctrl), which outputs the control signal V_{SW} to the Driving Ctrl block; Driving Ctrl then generates the gate-driving signals V_{GP1}, V_{GP2}, V_{GN1}, and V_{GN2}, conditioned upon the state of the enable signals. The implementation details of Switching Ctrl are provided in Section III-A. In addition, the RX supports cold-start-up, as will be discussed in Section III-C.

Fig. 10 shows the simulated waveform of the DOT Ctrl block with detailed logic timing. Case 1 represents steady-state operation. At the rising edge of DE_{TX}, EN_{DOT} remains low, indicating that T_{TOT} stays within the hysteresis window; therefore, T_{OFF} remains constant. At the next falling edge of clk, DOT Ctrl will lower V_{DUTY} to turn off the TX power stage and reset the logic. Case 2 represents a load-transient condition. At the rising edge of DE_{TX}, EN_{DOT} is already high, meaning T_{TOT} exceeds the hysteresis bounds. DOT Ctrl then checks U/D_{DOT}: if it is logic low, the next T_{OFF} will be decreased. At the next falling edge of clk, DOT Ctrl lowers V_{DUTY} to turn off the TX power stage, reset the logic, and start counting the new T_{OFF}, whose duration is set according to the updated T_{OFF} option. Fig. 11 shows the circuit implementation of T_{TOT} hysteresis detector (T_{TOT} Hyst. Det.), explaining the generation of EN_{DOT} and U/D_{DOT}.

Fig. 12 shows the detailed simulated waveform of the DORCM RX. Notably, after the RX switches from MD_{LSK} to MD_1, it can still enable a few additional charging phases to V_{O1} even after the TX has turned off its power stage. This occurs because the L_{TX}–C_{TX} tank retains residual resonant energy (see Fig. 8). This residual reception helps reduce TX energy waste during T_{OFF}. In addition, V_{GN2} follows V_{C2} during resonance phases when V_{C2} is lower than ground, allowing L_{RX}–C_{RX} resonance without interference from M_{N2}.

A. RX Zero-Crossing-Based Switching Control

Interfacing a variable link, the RCM rectifier can stay in the resonance phase (Φ_1) for either a single resonant period (T_{RE}), referred to as single-period Φ_1 (SP-Φ_1) case, or multiple periods, referred to as multi-period Φ_1 (MP-Φ_1) case. This requires the RX to detect the resonance energy level during each T_{RE}. If sufficient energy is detected, the RX transitions from Φ_1 to Φ_2, or Φ_3, to deliver energy to the outputs. Prior RCM designs operating at 6.78 or 13.56 MHz

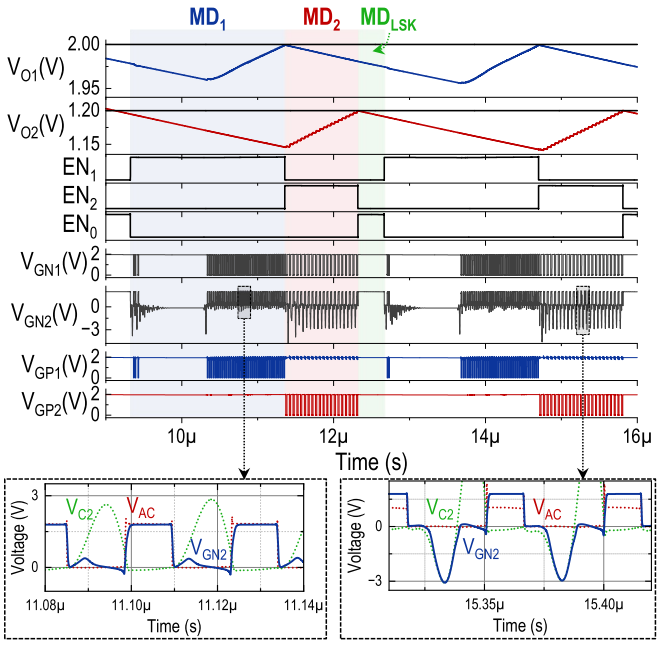


Fig. 12. Simulated waveform of the DORCM RX.

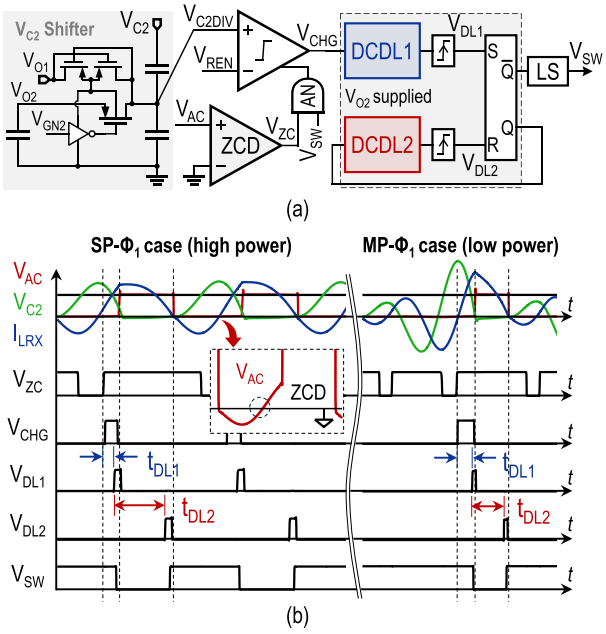


Fig. 13. RX zero-crossing-based switching controller. (a) Circuit implementation. (b) Operation waveform.

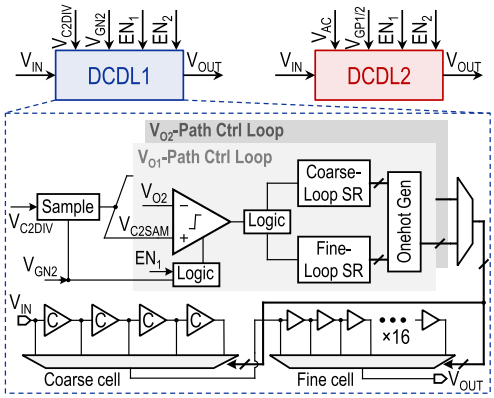


Fig. 14. Circuit implementation of the DCDL in the RX switching controller.

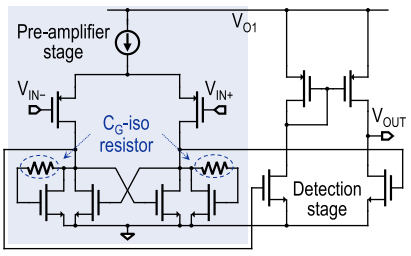


Fig. 15. Circuit implementation of the ZCD in the RX switching controller.

typically employ continuous-time comparators to detect peak resonance voltage across C_{RX}, while using delay-compensation techniques in comparators for accurate phase switching control [35], [36], [37]. However, these approaches do not scale well to 40.68 MHz: continuous-time comparators may fail to capture sharp voltage peaks due to limited bandwidth, and comparator-based delay-compensation schemes demand impractically large voltage offsets as T_{RE} shortens at 40.68 MHz. This further requires comparators with a wide dynamic range and sufficient input voltage swing. Though increasing bias current can ease these requirements, it sharply increases power consumption. Some designs mitigate the switching-control challenges by performing resonance energy detection and phase switching over two adjacent resonance periods, such as [36]. Nonetheless, it precludes SP-Φ_1 operation, compromising system performance under high-power conditions.

Fig. 13 shows the proposed single-mode zero-crossing-based switching controller, which seamlessly supports both SP-Φ_1 and MP-Φ_1 operations. In the resonant L_{RX}–C_{RX} tank, a zero-crossing of V_{ac} coincides with a peak in V_{C2}. Hence, to detect the energy level during Φ_1, a zero-crossing detector (ZCD) is used to identify the V_{ac}-zero events, which, in turn, trigger a clocked comparator. This comparator evaluates a dc-shifted, scaled version of V_{C2} (V_{C2DIV}), generated by the V_{C2} shifter block, against a reference voltage V_{REN}. Unlike continuous-time comparators, this combination of a ZCD and a clocked comparator outputs the "resonance-good" signal V_{CHG} (on its rising edge) with a well-defined delay, mainly from the ZCD. To trigger the RX transition from Φ_1 to Φ_2 (or Φ_3), an additional delay, t_{DL1}, is introduced from V_{CHG} by digital-controlled delay line 1 (DCDL1) to align with the I_{LRX} peak, which corresponds to the V_{C2} zero. DCDL2 subsequently determines the charging duration (t_{DL2}) and initiates the RX transition back to Φ_1 when I_{LRX} reaches zero. Notably, the resonance detection with a properly set V_{REN} also protects M_{N2} from overvoltage stress by triggering the charging phase before V_{C2} approaches the device breakdown limit. In addition, V_{REN} influences the RX power capability by defining the resonance phase duration [39]. In this work, V_{REN} is externally set and held constant during operation to meet only the safe-operation requirement.

Fig. 14 shows the circuit implementation of DCDL1, while DCDL2 employs a similar structure. DCDL1 samples V_{C2DIV} at the rising edge of V_{GN2} and then compares the sampled value V_{C2SAM} with the dc component of V_{C2DIV} and V_{O2}. Under ideal ZVS of M_{N2} and V_{C2} is grounded, making V_{C2DIV} equal to V_{O2}. If a switching error presents, DCDL1 adjusts its delay line stepwise, guided by the comparison result. The delay line includes a 2-bit coarse cell and a 4-bit fine cell, offering a practical balance between tuning range, resolution, and hardware consumption. The unit delays of the coarse and fine cells are 3.1 ns and 290 ps, respectively. DCDL2 achieves zero-voltage turn-off of M_{P1} (or M_{P2}) at the end of Φ_2 (or Φ_3) by monitoring V_{ac} at the rising edge of V_{GP1} (or V_{GP2}). Both DCDL integrate two separate control loops for the V_{O1}-charging mode (MD_1) and the V_{O2}-charging mode (MD_2), enabling seamless mode transitions from MD_1 to MD_2. To ensure accurate peak-V_{C2} detection, the ZCD adopts a continuous-time two-stage structure that provides low offset and high speed, as shown in Fig. 15 [40]. It has a typical power consumption of 38 μW.

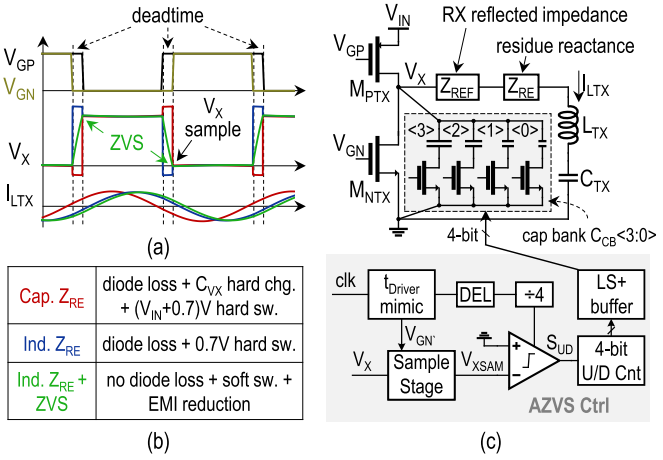
It is worth noting that the proposed ZCD + DCDL method differs from conventional comparator-based delay-compensation methods by directly adjusting delay elements to compensate for the control loop delay, thereby avoiding voltage-to-time conversion in comparators. As a result, it eliminates the tradeoff among dynamic range, input swing, and power consumption inherent in conventional methods.

B. TX AZVS Control

In high-milliwatt-class biomedical WPT systems, class-D PAs are widely adopted due to their high theoretical efficiency and robust performance against load variations [41]. To prevent shoot-through currents between the supply and ground, a dead time is usually inserted between the conduction periods of the high-side and low-side switches. However, beyond inherent gate-driving and conduction losses, load conditions and parasitics at the mid-node can introduce additional power loss during this interval. This issue becomes more pronounced at 40.68 MHz, where the dead time occupies a larger fraction of the switching cycle.

In practical WPT scenarios, the class-D PA may experience either inductive or capacitive loading due to the residual reactance of the L_{TX}–C_{TX} tank (Z_{RE}) and the reflected impedance from the RX (Z_{REF}). Under ideal resonance at the RX, Z_{REF} is mostly real, and the nature of Z_{RE} determines whether the PA exhibits capacitive or inductive switching behavior, each associated with different power loss characteristics, as shown in Fig. 16(a) and (b). Prior works have favored inductive Z_{RE} to alleviate hard switch turn-on and mitigate the charging/discharging of the parasitic capacitance at V_X (C_{VX}) [41]. However, body–diode conduction and hard switching persist.

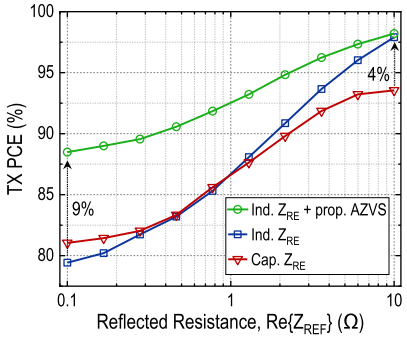
To address the abovementioned issues, this work applies an AZVS strategy, as shown in Fig. 16(c). It introduces programmable capacitance at V_X to compensate for the lagging current (I_{LTX}) under inductive Z_{RE}, enabling zero-voltage switch turn-on at the end of the dead time and eliminating diode losses. In addition, the softened V_X waveform helps reduce EMI. A 4-bit capacitor bank connected to V_X with



Cap. Z_{RE}	diode loss + C_{VX} hard chg. + (V_{IN}+0.7)V hard sw.
Ind. Z_{RE}	diode loss + 0.7V hard sw.
Ind. Z_{RE} + ZVS	no diode loss + soft sw. + EMI reduction

(b)

Fig. 16. (a) Switching waveforms and (b) loss characteristics of a class-D PA under different load impedance conditions. (c) TX AZVS class-D PA implementation.

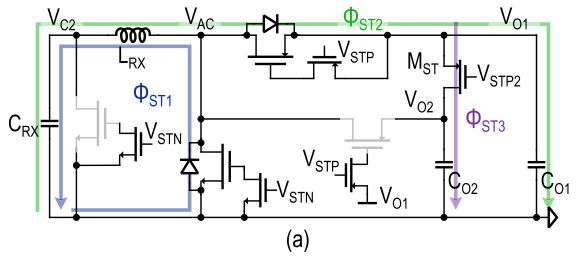


f_C	40.68MHz
L_{TX}	510nH
C_{TX}	29pF/31pF (ideal 30pF)
C_{VX}	A few pF
$C_{CB<3:0>}$	40, 20, 10, 5pF
R_{LTX}	1Ω
R_{ONTX}	0.2Ω
R_{ONCB}	0.05Ω
t_{DDT}	1ns

Fig. 17. Simulated TX PCE under different C_{TX} and ZVS conditions.

binary-weighted capacitance values, $C_{CB<3:0>}$, is controlled by an AZVS control block (AZVS Ctrl). At each rising edge of V_{GN}, V_X is sampled as V_{XSAM}. V_{XSAM} is then compared with the TX ground once every four periods. The lower adjustment speed helps ensure a stable loop. If V_X drops below ground when M_{NTX} turns on, AZVS Ctrl increases the total capacitance at V_X to reduce its slew rate; otherwise, it decreases C_{VX}, as indicated by signal S_{UD}. Notably, charging or discharging the added capacitance does not incur charge-sharing losses, as I_{LTX} is regulated by L_{TX}. It is worth mentioning that the proposed AZVS method operates only when Z_{RE} in the L_{TX}–C_{TX} loop is inductive. This can be intentionally achieved by slightly increasing either L_{TX} or C_{TX} at the TX. If a capacitive Z_{RE} arises due to coil shape distortion, aging effects, or other factors, the AZVS method can only disable the entire capacitor bank to minimize hard-switching loss, but cannot maintain ZVS. Achieving ZVS with a capacitive Z_{RE} requires impedance matching techniques [42].

Fig. 17 shows simulated TX PCE under various C_{TX} and ZVS conditions. The purely real Z_{REF} is swept from 0.1 to 10 Ω, and simulation parameters are listed on the right. In simulation, C_{TX} is set to either 29 or 31 pF, corresponding to capacitive or inductive Z_{RE} conditions, respectively; perfect resonance occurs near C_{TX} = 30 pF. A few picofarads of



	State 1	State 2
Φ_{ST}	1+2+3	1+2
V_{STP}	gnd	gnd
V_{STN}	V_{O1}	V_{O1}
V_{STP2}	gnd	V_{O1}

(b)

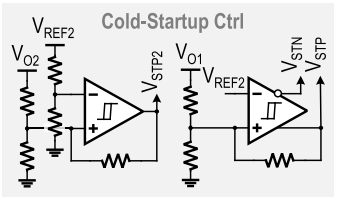


Fig. 18. RX cold-start-up setting. (a) Topology configuration. (b) Operation state table. (c) Circuit implementation of the cold-start-up controller.

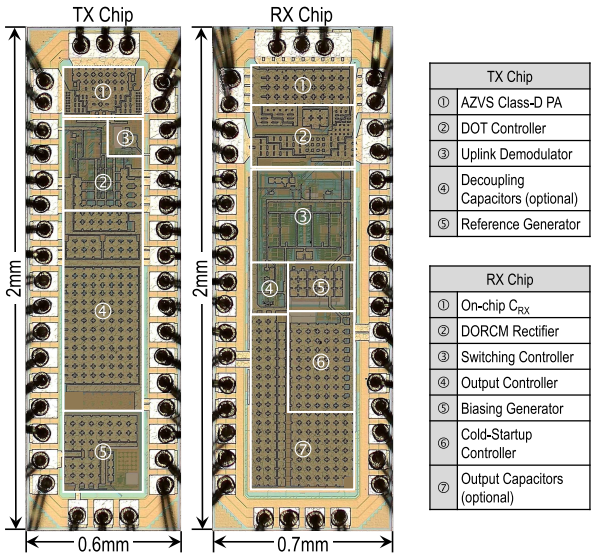


Fig. 19. Chip micrographs.

parasitic capacitance are assumed at V_X, attributed to M_{PTX}, M_{NTX}, and off-chip interconnections. The ON-resistances of M_{PTX}/M_{NTX} and the capacitor bank switches are denoted as R_{ONTX} and R_{ONCB}, respectively. The dead time is fixed at 1 ns, matching the near-1 ns slew rates of V_{GP} and V_{GN}. Simulation results confirm that the proposed AZVS control enhances TX PCE across the entire load range, with improvements of up to 9% over either inductive or capacitive Z_{RE} cases.

It is important to note that the capacitance values in the capacitor bank should be designed by simultaneously considering several parameters: 1) the residual inductance in the L_{TX}–C_{TX} tank; 2) the load resistance range of the class-D PA; and 3) the switching deadtime of the class-D PA. The first two parameters influence the current phase and amplitude in the L_{TX}–C_{TX} loop, respectively, and the third determines the voltage integration time across the capacitance at node V_X. In addition, though the added capacitance from the capacitor bank always connects to V_X, it only affects the slew rate of V_X during deadtime and does not impact the L_{TX}–C_{TX} resonance and normal conducting phases of the class-D PA. For example, when M_{PTX} is on, the added capacitance is effectively merged with the input voltage source, whereas when M_{NTX} is on, it is shorted by the low ON-resistance of M_{NTX}.

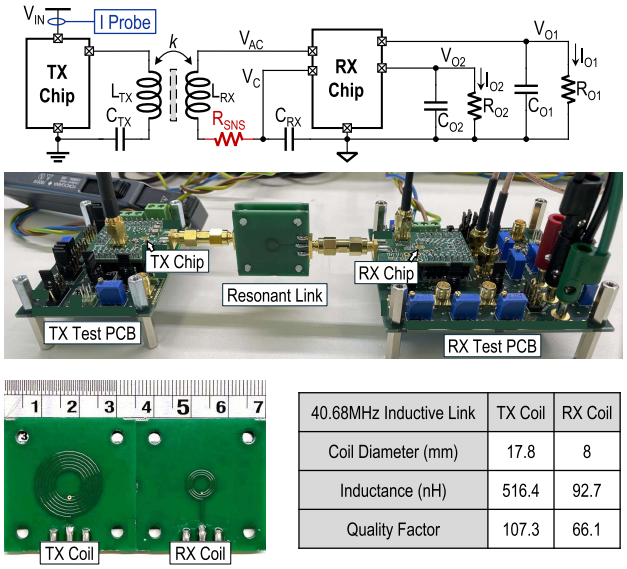
C. RX Cold-Start-up Configuration

As the supply for an implanted device, the RX must be capable of starting up from the cold state. Fig. 18 shows the proposed RX start-up configuration. In the cold state, the RX cannot operate in the active RCM mode and instead relies solely on passive body diodes. Therefore, M_{P2} and M_{N2} are not usable due to their dynamic body biasing. On the other hand, the body diodes of M_{P1} and M_{N1} form a half-bridge rectifier (HBR), enabling V_{O1} to charge up. To charge V_{O2}, a P-type start-up switch, M_{ST}, connects V_{O1} and V_{O2}. To ensure its robust turn-off in normal operation, the body of M_{ST} is tied to the higher potential V_{O1}. At the beginning of the start-up, its gate (V_{STP2}) is grounded. As a result, M_{ST} turns on when V_{O1} exceeds the PMOS threshold, allowing V_{O2} to charge. This phase is referred to as State 1. Once V_{O2} reaches a sufficient level while V_{O1} is only higher by the conduction drop across M_{ST}, M_{ST} will be turned off by pulling V_{STP2} up to V_{O1}. Thereafter, the HBR continues charging V_{O1} until it reaches its target level. This phase is defined as State 2.

During start-up, all four power transistors are switched off via control signals V_{STP} and V_{STN}. The cold-start-up controller (Cold-Start-up Ctrl) generates the three control signals V_{STP}, V_{STN}, and V_{STP2}, as shown in Fig. 18(c). At the beginning of cold start-up, circuit blocks are inoperable due to the low supply voltage; however, V_{STP} and V_{STP2} are pulled low through resistive paths to ground. Once the supply voltage V_{O1} rises sufficiently, the comparators begin to function and produce the appropriate outputs. Specifically, V_{STP2} transitions high when the divided V_{O2} exceeds the divided V_{REF2}, while V_{STP} and V_{STN} swap polarities once the divided V_{O1} surpasses V_{REF2}, indicating the completion of cold start-up. The resistor divider ratios are designed to match the target levels of V_{O1}, V_{O2}, and the reference V_{REF2}. To enable correct operation, a self-start-up reference generator is required to ensure V_{REF2} settles before any polarity transitions of the control signals occur.

IV. Measurement Results

The proposed TX and RX chips are fabricated in a 180-nm BCD technology, occupying silicon areas of 1.2 and 1.4 mm^2, respectively, as shown in Fig. 19. The measurement setup is illustrated in Fig. 20. The spiral RX coil (L_{RX}) is realized using a single-layer PCB with an 8-mm diameter and an inductance of 92.7 nH. Its dimension is possible to be designed further smaller with the same inductance; however, that will result in a smaller k under the same coil separation condition. The output capacitors C_{O1} and C_{O2} are mainly implemented off-chip, each with a capacitance of 100 nF. The coaxial coil separation distance D_{COIL} is adjustable to emulate varying coupling conditions in practical applications. For efficiency measurements, a current probe is used to sample the TX input



40.68MHz Inductive Link	TX Coil	RX Coil
Coil Diameter (mm)	17.8	8
Inductance (nH)	516.4	92.7
Quality Factor	107.3	66.1

Fig. 20. Measurement setup.

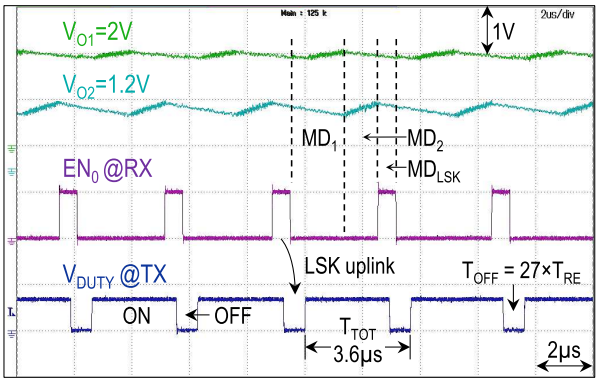


Fig. 21. Measured steady-state waveform at I_{O1} = 8 mA, I_{O2} = 12 mA, V_{IN} = 3.3 V, and D_{COIL} = 5.2 mm.

power with minimal disturbance to the high-energy power path. Meanwhile, the RX input power is measured via a shunt-based method combining R_{SNS} with a high-bandwidth differential probe.

Fig. 21 shows the measured steady-state waveform under RX load currents I_{O1} = 8 mA and I_{O2} = 12 mA, with a TX supply voltage of V_{IN} = 3.3 V. D_{COIL} is set at 5.2 mm, approximately corresponding to a coupling factor of k = 0.1. The output voltages V_{O1} and V_{O2} are regulated at 2 V and 1.2 V, respectively. The RX alternates between the V_{O1}-charging mode (MD_1), V_{O2}-charging mode (MD_2), and LSK uplink mode (MD_{LSK}). Upon demodulating each LSK uplink, the TX transitions from the active ("ON") state to the idle ("OFF") state, establishing a stable on/off duty ratio over each complete DOT modulation period (T_{TOT}). The measured result confirms that T_{TOT} stabilizes around 3.6 μs, with the TX-off period (T_{OFF}) equal to 27 × T_{RE}.

Fig. 22 shows the measured steady-state waveform of the V_{ac} signal, which verifies mode transitions at the RX. Notably, immediately after exiting MD_{LSK} and entering MD_1, the RX enables a few additional charging phases to transfer the

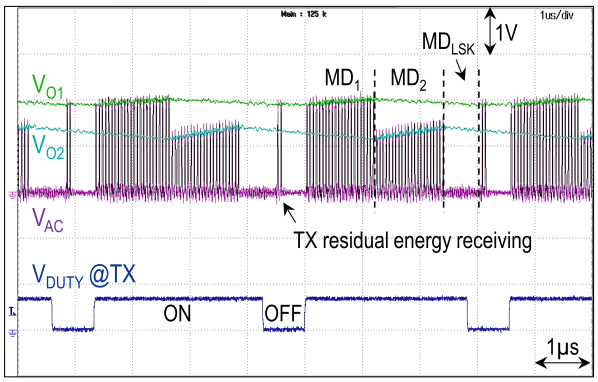


Fig. 22. Measured steady-state V_{ac} waveform at I_{O1} = 8 mA, I_{O2} = 12 mA, V_{IN} = 3.3 V, and D_{COIL} = 5.2 mm.

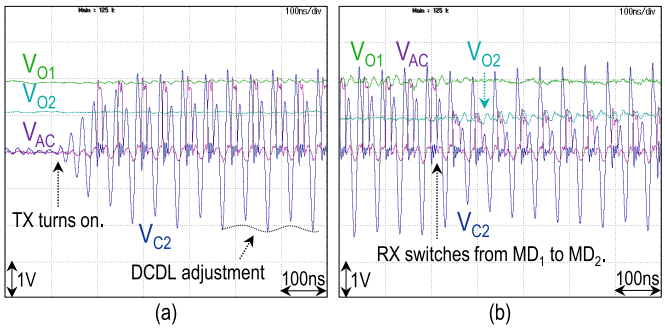


Fig. 23. Measured steady-state waveforms at the RX. (a) In MD_1. (b) Switching from MD_1 to MD_2.

residual resonant energy in the L_{TX}–C_{TX} tank to V_{O1}, even after the TX has turned off.

Fig. 23 shows the measured RX steady-state waveform with all key voltage signals in the power path. As shown in Fig. 23(a), the RX exhibits smooth switching behavior when the TX turns on, owing to the RCM nature in which charging phases occur only when the resonant energy reaches a certain threshold. Fig. 23(b) further confirms a seamless RX mode transition from MD_1 to MD_2, enabled by the separated V_{O1}-path and V_{O2}-path control loops in the DCDLs. The small ripples on the V_{C2} amplitudes indicate that the DCDLs are dynamically adjusting to track the optimal switching timing.

Fig. 24(a) and (b) presents the measured zoom-in steady-state waveforms during V_{O1} and V_{O2} charging, respectively, at D_{COIL} = 5.2 mm, where the RX operates in the MP-Φ_1 mode. Fig. 24(c) and (d) shows corresponding measurements at D_{COIL} = 2.5 mm (approximately k = 0.2), where the RX operates in the SP-Φ_1 mode. In both MP-Φ_1 and SP-Φ_1 scenarios, the phase transition from Φ_1 to Φ_2 (or Φ_3) occurs when V_{C2} is near zero, indicating near zero-voltage turn-on of M_{N2}. Likewise, V_{ac} exhibits only minor voltage surges during the Φ_2 (or Φ_3) to Φ_1 transition, demonstrating near zero-voltage turn-off of M_{P1} (or M_{P2}), thanks to the proposed switching control strategy.

Fig. 25 shows the measured load-transient waveform at V_{O1} with I_{O2} = 8 mA, V_{IN} = 3.3 V, and D_{COIL} = 5.2 mm. When I_{O1} transitions from 2 mA to 15 mA (a 7.5× step), the ripple on V_{O1} increases due to the heavier load. T_{OFF}

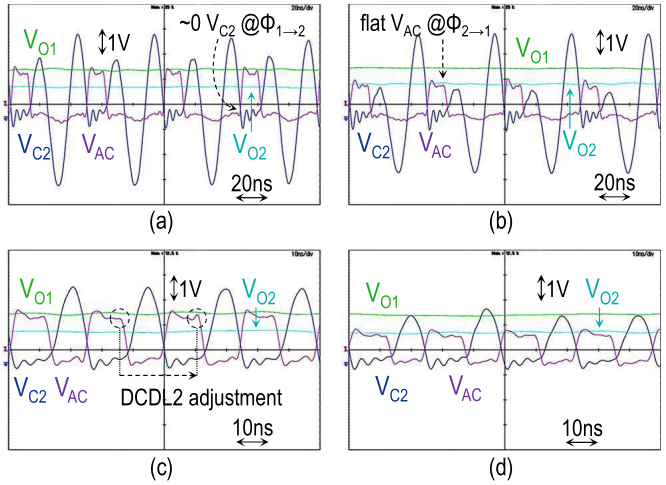


Fig. 24. Measured zoom-in steady-state waveforms at the RX. (a) MP-Φ_1 case in MD_1. (b) MP-Φ_1 case in MD_2. (c) SP-Φ_1 case in MD_1. (d) SP-Φ_1 case in MD_2.

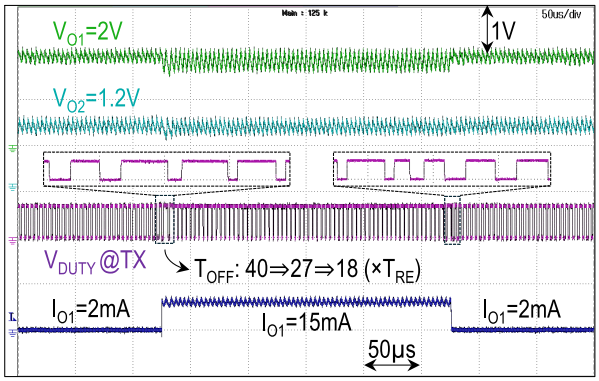


Fig. 25. Measured load-transient waveform at I_{O2} = 8 mA, V_{IN} = 3.3 V, and D_{COIL} = 5.2 mm.

decreases from 40 × T_{RE} to 18 × T_{RE} to maintain a constant T_{TOT} and mitigate the load regulation performance. Larger output capacitors can be used to further suppress the voltage ripple. Though V_{O2} shows a slight undershoot caused by the momentarily prolonged T_{TOT} during the transient, it maintains nearly constant ripple before and after the event, owing to the relatively constant T_{TOT} enabled by the DOT modulation. Upon a heavy-to-light load transition, T_{OFF} increases back from 18 × T_{RE} to 40 × T_{RE}. Due to immediate mode switching at the RX, cross-regulation on V_{O2} is unnoticeable. The load-transient behavior observed at V_{O2} is similarly well-regulated.

Fig. 26 shows the measured LSK uplink modem waveform at D_{COIL} = 5.2 mm. When the RX enters MD_{LSK}, the TX observes an increase in the amplitude of V_{C1} as well as V_{C1DIV}, enabling successful demodulation of the uplink signal.

The measured TX switching waveforms with the capacitor bank and the AZVS controller disabled and enabled are shown in Fig. 27(a) and (b), respectively. When the capacitor bank and the AZVS controller are enabled, the capacitance at node V_X is finely tuned, enabling nearly ZVS of both M_{PTX} and M_{NTX} without noticeable body-diode conduction and voltage spikes.

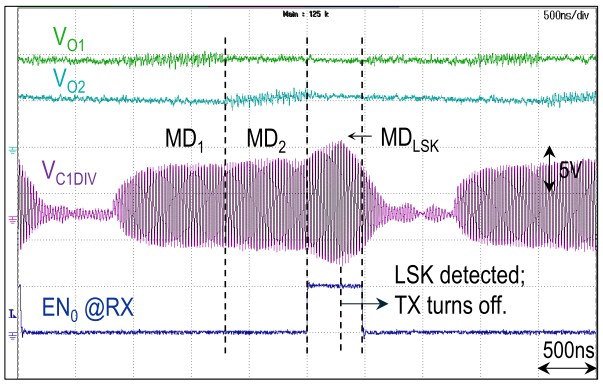


Fig. 26. Measured LSK modem waveform at D_{COIL} = 5.2 mm.

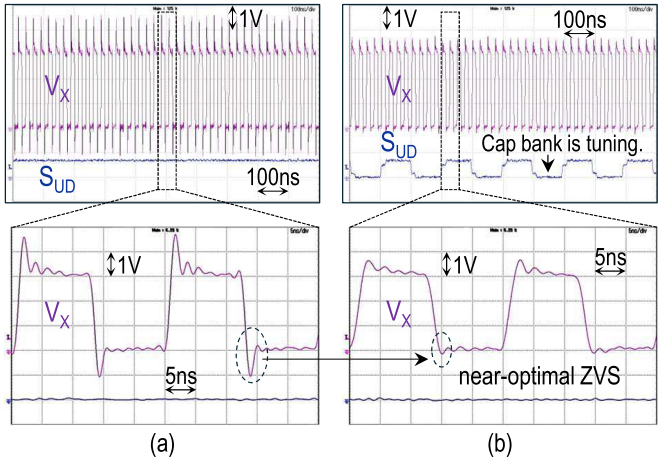


Fig. 27. Measured TX switching waveforms with the capacitor bank and the AZVS controller. (a) Disabled. (b) Enabled.

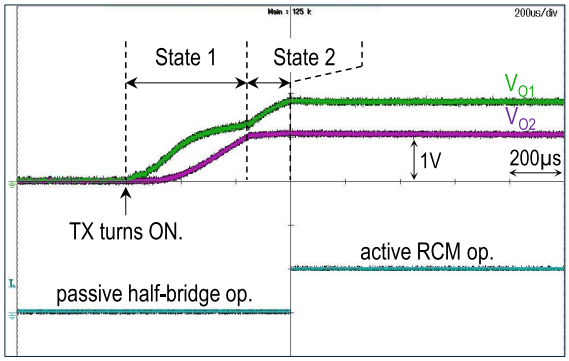


Fig. 28. Measured RX cold-start-up waveform.

Fig. 28 shows the measured RX cold-start-up waveform. During the half-bridge operation based on body diodes, the two subsequent states are observed. Once State 2 concludes, the RX transitions into active RCM operation.

Fig. 29 shows the measured PCE at the RX, with D_{COIL} = 5.2 mm and V_{IN} = 5 V. The RX input power was measured using the shunt resistor R_{SNS} with a resistance of 3.5 Ω. A 2-GHz bandwidth differential probe (PBD2000) monitors the voltage across R_{SNS} using a 4-wire Kelvin connection on the test PCB. In both I_{O1} = 5 mA and I_{O2} = 5 mA cases, the RX demonstrates similar PCE profiles, confirming soft-switching

TABLE II
COMPARISON WITH STATE-OF-THE-ART BIOMEDICAL WPT SYSTEM DESIGNS

	JSSC'18[16]	JSSC'22[19]	TCAS-I'23[20]	JSSC'24[21]	JSSC'24[23]	JSSC'24[9]	ISSCC'24[27]	**This work**
Carrier Frequency	13.56MHz	6.78MHz	6.78MHz	13.56MHz	13.56MHz	40.68MHz	40.68MHz	**40.68MHz**
Coil Diameter	RX 20mm TX 25.2mm	RX 25mm TX 32mm	RX 23mm TX 41mm	RX 30mm TX 35mm	RX 20mm TX 30mm	RX 4mm TX 16.5mm	RX 24mm TX 32mm	**RX 8mm TX 17.8mm**
Chip Integration	TX & RX	TX & RX	TX & RX	TX & RX	TX & RX	RX only	RX only	**TX & RX**
Technology	65nm CMOS	180nm CMOS	180nm CMOS	65nm CMOS	180nm CMOS	65nm CMOS	180nm BCD	**180nm BCD**
Chip Area	RX 1.44mm^2 TX 1.44mm^2	RX 1.3mm^2 TX 0.98mm^2	RX 2.7mm^2 TX 0.98mm^2	RX 0.15mm$^{2\#}$ TX 0.15mm$^{2\#}$	RX 1.65mm^2 TX 1.53mm^2	RX 0.74mm^2 TX external	RX 1.6mm^2 TX external	**RX 1.4mm^2 TX 1.2mm^2**
Off-Chip Components	C_O (1μF), and a LSK sensing coil	C_O (8μF)	2 C_O	C_{O1} (1μF), C_{O2} (1μF), a LSK coil and a detector	2 C_O (330nF each)	C_{O1} (220nF), C_{O2} (470nF)	C_{O1} (1μF), C_{O2} (1μF)	**C_{O1} (100nF), C_{O2} (100nF)**
TX Topology	Class-D PA	Class-D PA	Class-D PA	Reconfigurable Class-D PA	Reconfigurable Class-D PA	OPA 2677	Class-E PA	**Adaptive-ZVS Class-D PA**
RX Topology	Full-Bridge Regulating Rectifier	Full-Bridge Regulating Rectifier	DO RCM Regulating Rectifier	DO Full-Bridge Regulating Rectifier	VM/RCM Regulating Rectifier	DO Full-Bridge Regulating Rectifier	Full-Bridge Rectifiers + LDOs	**DO RCM Regulating Rectifier**
Global Regulation	Constant Off-Time Control	Hysteretic Control	"Record & Replay" Control	PWM Control	Digital PWM Control	No	No	**Dynamic Off-Time Control**
TX Input Voltage	2.5V	1.8V	1.8V	1.2V	1.8V	N/R	N/R	**3.3V~5V**
RX Output Voltages (# of outputs)	1.2~2.5V (1)	1.2~1.8V (1)	3V; 1.8V (2)	2.5V; 1.2V (2)	1.8V (1)	2.2V; 1.1V (2)	4V; 2V (2)	**2V; 1.2V (2)**
Output Voltage Ripple (I_{LOAD})	50mV (10mA)	75mV (hysteretic)	50mV@V_{O1}(1mA); 50mV@V_{O2}(1mA)	N/R	100mV (30mA)	190mV@V_{O1}(25mA); 90mV@V_{O2}(5mA)	N/R	**58mV@V_{O1}(8mA); 160mV@V_{O2}(12mA)**
RX Cold-Startup	No	No	Yes	Yes	No	Yes	Yes	**Yes**
Coil Separation Distance (D)	0.2~1.1cm	0.65cm	1~2cm	0.6~1.5cm	0.5~7cm	0.2cm	1.2cm (k=0.115)	**0.25~1cm (k=0.04~0.2)**
Peak E2E Efficiency	70.6% (@D=0.6cm)	61.9% (@D=0.65cm)	31.3% (@D=1cm)	62.7% (@D=0.6cm)	72.3% (@D=0.5cm)	N/R	31.4% (@D=1.2cm)	**51.2% (@D=0.25cm)**
Peak RX PCE	N/R	N/R	85.1%	88%	92.7%	90.1%	87.4%**	**90.3%**
Maximum P_{OUT}	49.4mW	32mW	7mW	20mW	80.5mW	60.5mW	110mW	**149.7mW**

N/R: Not reported; #area excluding pads; **simulation result.

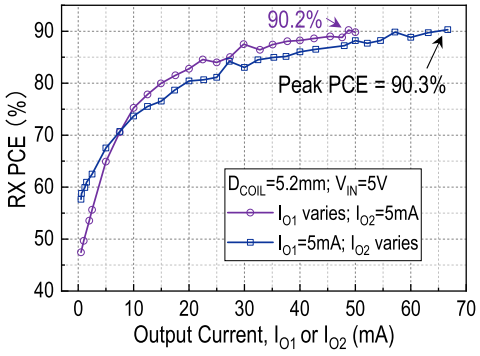


Fig. 29. Measured PCE at the RX.

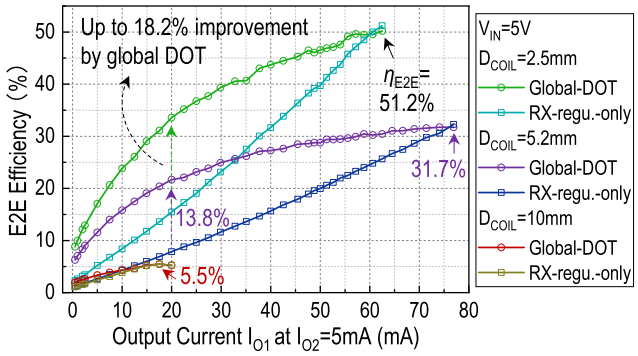


Fig. 30. Measured E2E power efficiency.

behavior in both the V_{O1} and V_{O2} charging paths. A peak PCE of 90.3% is achieved at I_{O1} = 5 mA and I_{O2} = 67 mA, corresponding to a total output power of 90.4 mW.

Fig. 30 presents the measured E2E power efficiency from the TX input to the RX outputs, in which R_{SNS} is short-circuited. To reflect practical coupling scenarios in biomedical implants, the E2E efficiency was measured under three representative D_{COIL}: 2.5, 5.2, and 10 mm, corresponding to k of 0.2, 0.1, and 0.04, respectively. Measurements are performed under two operating modes: global-DOT-modulation mode and RX-regulation-only mode. The global-DOT-modulation mode represents the normal operation where the TX is dynamically modulated based on feedback. In contrast, the RX-regulation-only mode keeps the TX continuously on, with the RX periodically entering MD_{LSK} to regulate V_{O1} and V_{O2}.

In the D_{COIL} = 10 mm case, the peak E2E efficiency is limited to 5.5%, and the maximum output power reaches only 46 mW due to the low link efficiency. As D_{COIL} decreases to 5.2 mm, the operable load range significantly expands, and the system achieves a peak PCE of 31.7% at a maximum output power of 149.7 mW. Under this condition, enabling global DOT modulation yields up to a 13.8% improvement in E2E

efficiency. When D_{COIL} becomes 2.5 mm, the system achieves a peak E2E efficiency of 51.2% at 130 mW output power. With global DOT modulation, the E2E efficiency improves by up to 18.2%, which, at $I_{\mathrm{O1}} = 20$ mA, translates to a 2.2× reduction in TX input power.

It is worth noting that the power results were measured ex vivo using PCB-based coils in air. For practical in vivo applications, compliance with applicable specific absorption rate (SAR) limits must be ensured. Standardized tissue-equivalent measurements are recommended to validate the power results before deployment. In addition, angular misalignment between the TX and RX coils has a similar impact on the coupling coefficient as increasing coil separation.

Table II benchmarks this work against state-of-the-art biomedical WPT system designs. By operating at a power carrier frequency of 40.68 MHz, the proposed system achieves an 8-mm-diameter RX coil without significantly sacrificing output power and RX PCE. The higher maximum output power in this work is attributed to two factors: 1) the TX is driven with a relatively higher input voltage and 2) the RCM rectifier at the RX, when configured to operate the charging phase in every resonant period, can deliver power comparable to that of FBR and VD rectifiers under strong coupling [43]. Though small-output capacitors are used, the proposed global DOT modulation regulates the output voltage ripple. Increasing the output capacitance can further reduce the ripple. Compared to low-frequency designs, the proposed system exhibits a lower peak E2E efficiency due to: 1) the smaller coupling factor at which the peak was measured, dictated by the small RX coil; 2) increased TX and RX coil losses from the skin effect at higher switching frequencies; and 3) additional losses from the power switches in the class-D PA. Compared to other 40.68-MHz designs, though [9] employs a smaller 4-mm-diameter RX coil, its coil separation is limited to 2 mm; in contrast, the proposed system demonstrates strong coupling adaptability, enabled by the RX RCM topology. The proposed system also optimizes switching operations at both the TX and RX. Furthermore, it achieves a high level of integration, with global power modulation realized through a fully integrated data uplink channel.

V. Conclusion

This article presents a highly integrated WPT system operating at 40.68 MHz for high-milliwatt-class miniature biomedical implantable devices. By incorporating global DOT power modulation, a DORCM rectifier at the RX, and an AZVS class-D TX, the system achieves a millimeter-scale RX coil while delivering state-of-the-art output power and efficiency, along with high coupling adaptability.

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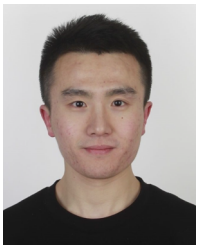

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