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DOI
10.23919/EuCAP48036.2020.9135726

Publication date
2020

Document Version
Submitted manuscript

Published in
14th European Conference on Antennas and Propagation (EuCAP 2020)

Effect of Element Number Reduction on Inter-User Interference and Chip Temperatures in Passively-Cooled Integrated Antenna Arrays for 5G

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***Abstract*—The impact of reducing the total number of elements in passively-cooled, chip-integrated and space-tapered 5G base station antenna arrays on inter-beam interferences and chip temperatures is investigated for multi-user space-division-multiple-access applications. A convex element position optimization algorithm is used to synthesize the array layouts with minimized side lobes within a pre-defined cell sector. The multi-beam radiation patterns are computed to study the average trend of the maximum side lobe level with the element number. Thermal simulations are also performed by considering the same EIRP for all the arrays. The results indicate that, after an optimal number of elements, adding more elements to an array does not help reduce the inter-user interference further or provide significant advantage on decreasing the chip temperatures.**

***Index Terms*—antenna synthesis, base station antennas, fifth generation (5G), irregular arrays, passive cooling, sparse arrays.**

I. Introduction and Motivation

High throughput expectations from 5G systems require sufficient simultaneous frequency re-use at the base station (BS) through formation of multiple beams with low interference and thus with low side lobe levels (SLLs) [1]. Besides, optimal use of the total available power via uniform-amplitude arrays is a key requirement in a 5G link, especially at mm-waves, due to low power amplifier efficiencies [2]. To resolve the issues with the inter-beam interference while achieving the optimum power efficiency, space-tapered arrays with optimized element locations were recently proposed to be used in 5G systems [3] and their advantages in terms of the quality-of-service (QoS) over the regular counterparts were presented in detail [4].

Thermal management is yet another issue that should be considered when designing 5G BS antennas at mm-waves. It is worthy of note that the 5G transceiver chips that are currenly used by the industry are highly inefficient, which leads to extremely large heat generation [5]. This excess heat has to be removed from the BS preferably passively via natural convection. To realize such a cooling mechanism, fanless CPU coolers were used effectively with an antenna printed on a double-sided PCB as shown in Fig. 1 and it was shown that the heat that is concentrated on the baseplate of the cooler (where the chips are thermally connected) can be efficiently transferred to the metallic fins via the use of heat pipes and dissipated to the surrounding air [6].

In the past few years, the number of publications that joinly consider the antenna and cooling system design challenges has increased remarkably (see, for example, [6]–[8]). Thermal simulations and experiments of chip-integrated arrays with CPU coolers were performed in [9]. Thermal and electromagnetic performance of several existing sparse array layouts were investigated in [6]. Later, in [10], a smart iterative convex element position optimization technique was introduced to synthesize uniform-amplitude linear arrays with minimized side lobes for a beam scanned freely inside a given cell. In [3], the technique was extended to passively-cooled planar arrays. The optimization in [3] was performed using a 64-element array for comparison with the 8x8 regular half-wavelength spaced arrays existing in the industry (see the antennas from NXP [9], Ericsson [11], IBM [12]) and the QoS performances of the two were compared in [13].

To the best of the authors' knowledge, there is no prior work that jointly investigates the effect of the number of BS antenna elements on the array temperature and inter-beam interferences in a typical 5G cell deployment scenario. However, due to the limitations in system cost and power consumption, there is still a need to find out the lowest number of elements (transceiver chips or RF chains in the case of digital beamforming) at the BS antenna which can sufficiently suppress the inter-user interference and work at a reliable temperature.

In this paper, taking into account the thermal integration with the CPU cooler used in [9], we use the technique in [3] to synthesize optimal multibeam antenna layouts with minimized SLLs within the communication sector for different number of total array elements and different initial array topologies.

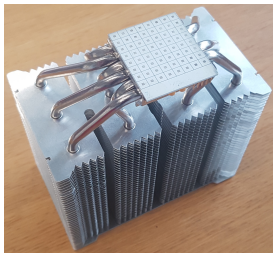


Fig. 1. State-of-the-art fabricated chip-integrated array with the Mugen MAX fanless CPU heatsink [14] (picture taken from [9]).

We also perform temperature simulations and search for the "best" array layout with the smallest number of elements that can achieve sufficiently low SLLs and chip temperatures. The rest of the paper is organized as follows. Section II presents the simulation settings both in electromagnetic and thermal aspects. The simulations results are shown and discussed in Section III. Finally, the conclusions are given in Section IV.

II. Simulation Settings

A. Electromagnetic Aspects

We consider the 5G cell sector used in [11] which is defined by a ± 15 degree range in elevation and a ± 60 degree range in azimuth as visualized in Fig. 2. The number of elements in the BS antenna is varied from 16 to 64. The minimum element spacing is set to 0.5λ. As explained before, the positions of the elements are to be optimized using the Convex Optimization algorithm introduced in [3] with the aim of minimizing the maximum SLL for a beam that is scanned freely inside the sector. Here, differently from [3], we minimize the SLL within the cell sector only and also investigate the effect of the choice of different initial array layouts on the outcome. Assuming a center operating frequency of 38 GHz (λ = 7.9 mm), the aperture size is made restricted to $\pm 2.5\lambda$, which defines the approximate baseplate dimensions of the commercially available CPU coolers. It is worthy of note that in practice, the baseplate of the cooler in [9] can be made larger with a post-fabrication treatment. However, in that case, as seen in [9], the elements (chips) that are further from the heat pipes will be cooled less and will create a problem. Therefore, while designing the integrated antennas, it is better to stick to the dimensions dictated by the optimally designed CPU coolers. Otherwise, more expensive and customer-specific cooler designs will be needed which are not directly available in the market. In this paper, we use the limited aperture size, but we also discuss (in Section III) the impact of unrestricted aperture size on the maximum SLL for different number of elements in order to show the trade-off between the QoS and complexity of thermal management.

B. Thermal Aspects

We consider that the chip integrated antennas are passively cooled using the fanless CPU heatsink Mugen MAX [14]. On the double-sided PCB, the chips are glued to the baseplate of the cooler on one side, while the radiators (patches) are facing the opposite side. Two-resistor thermal model validated in [9] is used in CST MPS solver to compute the chip temperatures. The common parameters of the thermal model are summarized in Table I. We further assume that the heat generated by a chip is directly proportional to the RF power produced by the chip. Therefore, the heat dissipated per chip (P_h) is computed depending on the number of elements such that the EIRP is kept the same both for sparse and densely populated arrays. In other words, P_h in the sparser arrays will be higher than that of the relatively dense ones due to their lower gain, which should be compensated with a larger output power.

TABLE I
Thermal Model Parameters

IC junction-to-case resistance	10 W/K
IC junction-to-board resistance	14 W/K
Heat transfer coefficient at the air interfaces	10 W/m^{2}K
Total board dimensions (length x width x height)	45 x 45 x 1.4 mm
Effective board thermal conductivity (length x width x height)	12 x 12 x 3 W/mK
Surface emissivity	0.9
Ambient temperature	25^{o}C

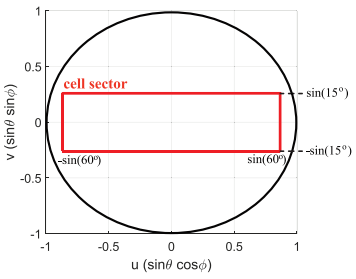
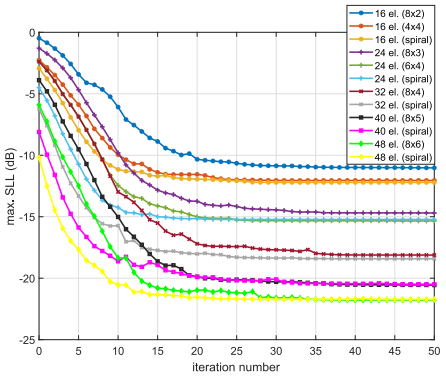
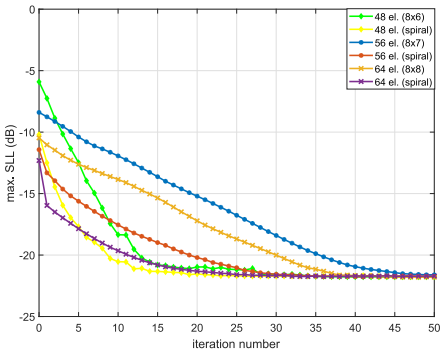


Fig. 2. A typical 5G cell sector in the uv-plane with ± 15 degree range in elevation and ± 60 degree range in azimuth.

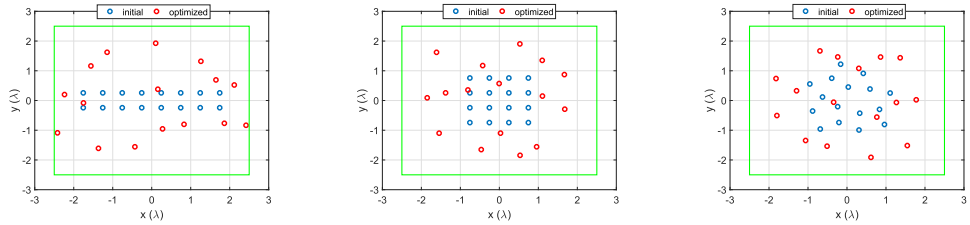


(a)



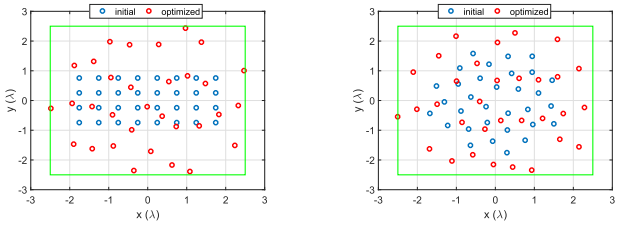
(b)

Fig. 3. Algorithm convergence in peak SLL for different number of total array elements and initial layouts in a 5G cell sector defined by ± 15 degree range in elevation and ± 60 degree range in azimuth: (a) from 16 to 48 elements, (b) from 48 to 64 elements.



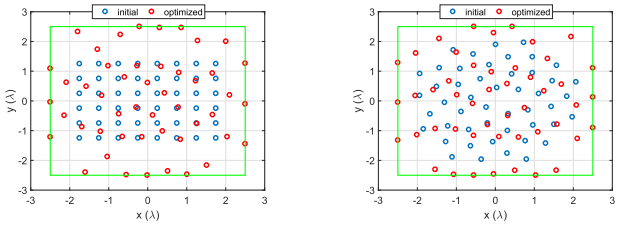
(a) (b) (c)

Fig. 4. Optimized element positions for the 16-element array using the initial layout of (a) 8 x 2 - rectangular, (b) 4 x 4 - square, (c) 16-element sunflower.



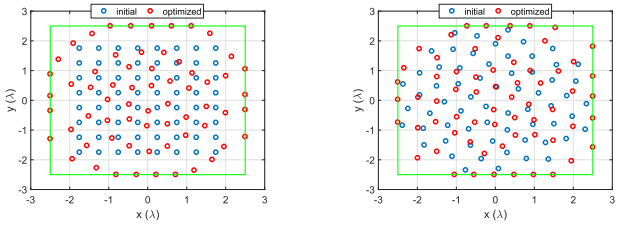
(a) (b)

Fig. 5. Optimized element positions for the 32-element array using the initial layout of (a) 8 x 4 - rectangular, (b) 32-element sunflower.



(a) (b)

Fig. 6. Optimized element positions for the 48-element array using the initial layout of (a) 8 x 6 - rectangular, (b) 48-element sunflower.



(a) (b)

Fig. 7. Optimized element positions for the 64-element array using the initial layout of (a) 8 x 8 - square, (b) 64-element sunflower.

III. Simulation Results and Discussion

In this section, first, we present the maximum SLL and radiation pattern results for different total BS antenna element numbers. Fig. 3 shows the convergence of the maximum SLL within the sector in Fig. 2 for different initial layouts (square, rectangular, spiral) and varying element number. From Fig. 3(a), it can be seen that using a spiral (sunflower) array layout at the algorithm input generally provides the best result in terms of the SLL and for the maximum aperture edge length of 5λ, the maximum SLL can be reduced from -12.2 dB for 16 elements to -18.4 dB for 32 elements and to -21.7 dB for 48 elements. The effect of increasing the element number more (until a maximum of 64 elements) is given in Fig. 3(b). One can observe that after 48 elements, increasing the element number does not help suppressing the SLL further. This is due to the limitation in the aperture size that is enforced by the characteristics of the cooler. Yet, for completeness, we also performed the simulations with no limitation on the aperture size. In that case, for 32, 48 and 64 elements, maximum SLL become -18.4 dB, -22 dB and -25.2 dB, respectively. It can be seen that although there is no change for 32 and 48 element arrays, maximum SLL in the 64 element array can be reduced by 3.5 dB more. This comes at the expense of increased aperture size with an edge length of 6.1λ, which will require a costly, design-specific cooler for reliable operation. Therefore, as mentioned in Section II-A, in this paper we present the results using a restricted aperture.

The initial and optimized layouts for 16 to 64 element BS arrays are plotted in Fig. 4 to Fig. 7, respectively. Next, the multibeam radiation patterns (scanned towards the four sector corners) of the optimized 16, 32, 48 and 64 element arrays are given in Fig. 10 to Fig 13, respectively. These radiation patterns help visualizing the maximum SLL values reported in Fig. 3. It is again seen that 48 and 64 element arrays are able to effectively and equally suppress the side lobes within the sector, while the out-of-sector pollution is smaller in the 64-element array.

Next, the optimized (using a sunflower initial layout) 16, 32, 48 and 64 element arrays are simulated in CST MWS to compute the array directivities. The patch element shown in Fig. 8 is used as the unit cell. The simulated broadside radiation patterns are shown in Fig. 9. It is seen that the gain of 32, 48 and 64 element arrays are 2, 2.7 and 3.6 times more than the gain of the 16 element array. This means that, if we assume per chip output power of P_o and heat generation P_h in the 64-element array, to achieve the same EIRP, P_o

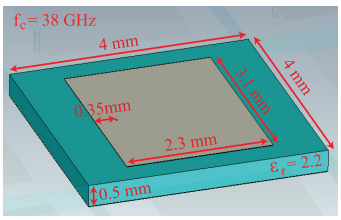


Fig. 8. Pin-fed patch antenna dimensions used in the full-wave simulations.

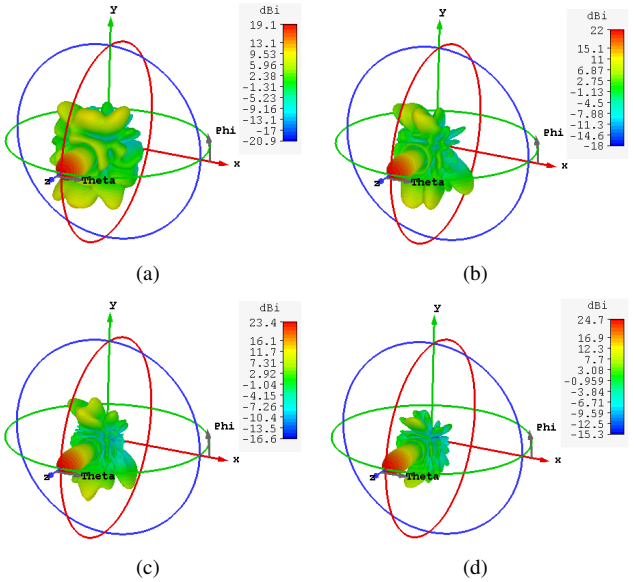


Fig. 9. Array directivity (in dBi) for the broadside beam using the optimized array layouts with (a) 16, (b) 32, (c) 48, (d) 64 elements.

(and thus P_h) for the 48, 32 and 16 element arrays will be approximately 1.8, 3.6 and 14.4 times more, respectively. For thermal simulations, we assume that P_h for 64 element array is 0.5 W (which results in P_h equal to 0.9 W, 1.8 W and 7.2 W for 48, 32 and 16 element arrays, respectively) and the chip dimensions are 0.7 x 0.7 x 0.5 mm. Taking into account the output power needed, we also modify the chip size accordingly such that the 48, 32 and 16 element arrays have chips (per element) with dimensions of 1.4 x 0.7 x 0.5 mm, 1.4 x 1.4 x 0.5 mm and 2.8 x 2.8 x 0.5 mm.

The thermal simulation results are given in Fig. 14. It can be seen that the temperature is the highest and not allowable in the 16 element array due to high per-chip heat generation, i.e.

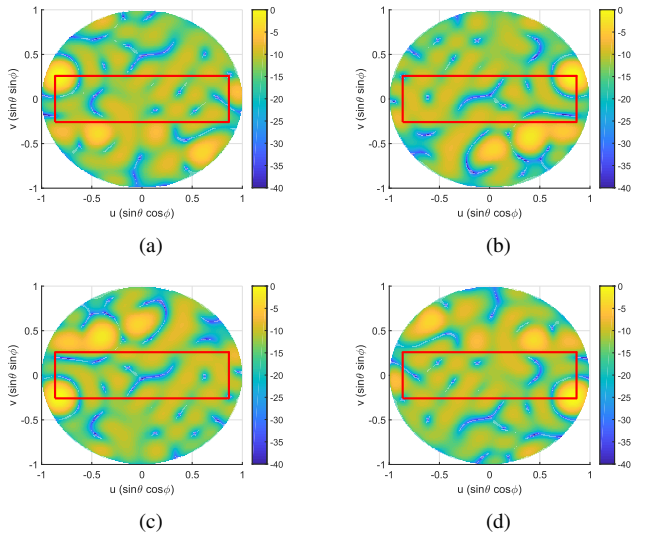


Fig. 10. Multi-beam radiation patterns (in dB, normalized) of the optimized 16-element array for a beam scanned towards (a) $u = -\sin(\pi/3)$, $v = \sin(\pi/12)$, (b) $u = \sin(\pi/3)$, $v = \sin(\pi/12)$, (c) $u = -\sin(\pi/3)$, $v = -\sin(\pi/12)$, (d) $u = \sin(\pi/3)$, $v = -\sin(\pi/12)$.

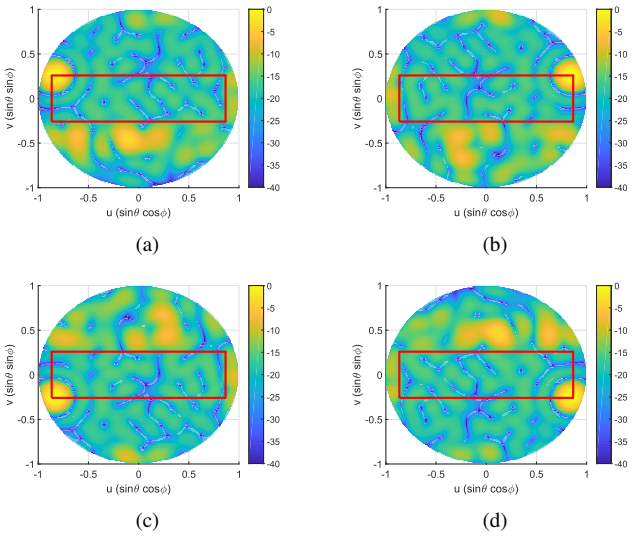


Fig. 11. Multi-beam radiation patterns (in dB, normalized) of the optimized 32-element array for a beam scanned towards (a) $u = -\sin(\pi/3)$, $v = \sin(\pi/12)$, (b) $u = \sin(\pi/3)$, $v = \sin(\pi/12)$, (c) $u = -\sin(\pi/3)$, $v = -\sin(\pi/12)$, (d) $u = \sin(\pi/3)$, $v = -\sin(\pi/12)$.

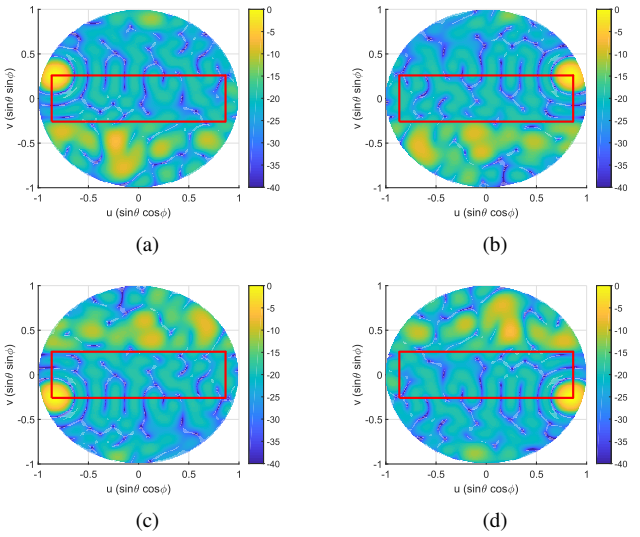


Fig. 12. Multi-beam radiation patterns (in dB, normalized) of the optimized 48-element array for a beam scanned towards (a) $u = -\sin(\pi/3)$, $v = \sin(\pi/12)$, (b) $u = \sin(\pi/3)$, $v = \sin(\pi/12)$, (c) $u = -\sin(\pi/3)$, $v = -\sin(\pi/12)$, (d) $u = \sin(\pi/3)$, $v = -\sin(\pi/12)$.

P_h. When the element number is increased, P_h goes down as well as the chip temperatures. For the 32, 48 and 64 element arrays, the maximum temperature become 85^{o}C, 66^{o}C and 54^{o}C, respectively. Here, we see that the thermal performances of the 48 and 64 element arrays (which provide the same EIRP) are close to each other and both can guarantee a safe and reliable device operation for a long time. Taking into account the radiation pattern results too, we can conclude that for our case with the commercially available passive CPU coolers, using the 48 element array with the optimized layout is the optimal design solution at the 5G BS.

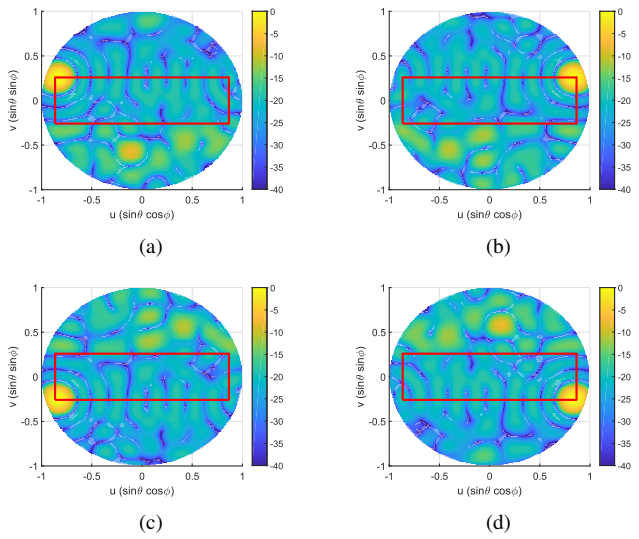


Fig. 13. Multi-beam radiation patterns (in dB, normalized) of the optimized 64-element array for a beam scanned towards (a) $u = -\sin(\pi/3)$, $v = \sin(\pi/12)$, (b) $u = \sin(\pi/3)$, $v = \sin(\pi/12)$, (c) $u = -\sin(\pi/3)$, $v = -\sin(\pi/12)$, (d) $u = \sin(\pi/3)$, $v = -\sin(\pi/12)$.

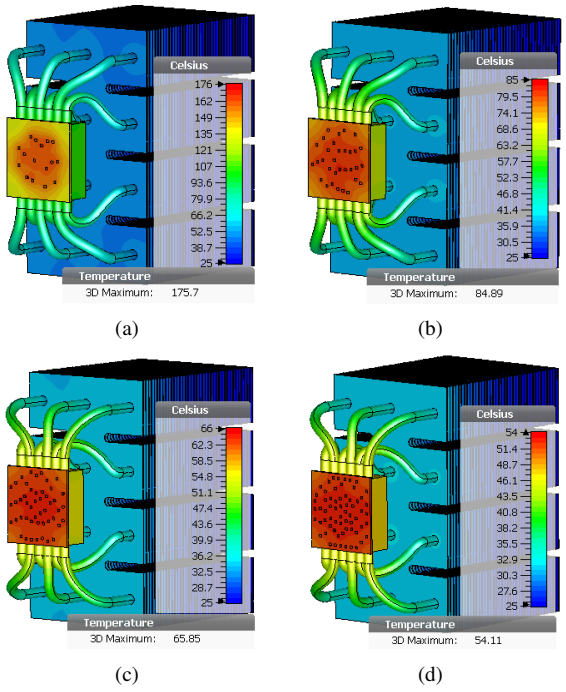


Fig. 14. Chip temperature distributions across the passively-cooled active integrated antenna arrays with (a) 16 elements - P_h = 7.2 W, (b) 32 elements - P_h = 1.8 W, (c) 48 elements - P_h = 0.9 W, (d) 64 elements - P_h = 0.5 W.

IV. Conclusion

The effect of varying the total element number in passively-cooled, chip-integrated and space-tapered antenna arrays for 5G on inter-user interference and chip temperatures has been studied. The convex optimization algorithm in [3] has been used to optimize the positions of the elements with the aim of minimizing the maximum SLL within the coverage sector for a beam scanned freely inside that sector. The element number is specified at the input of the algorithm and is gradually reduced to create the sparser arrays. The array aperture has been restricted to the baseplate dimensions of the commercially available CPU heatsinks for direct and low-cost cooling.

It has been observed that the maximum SLL reduces as the element number increases. This trend continues until an optimal element number, after which adding more elements does not help reduce the SLL further because of the limited aperture size. Thermal simulations have also been performed by taking into account the EIRP equalization and it has been seen that increasing the element number decreases the maximum temperature in the array and brings it to a safe level since the heat generated per-element (or per-chip) is reduced.

Overall, this study points out the trade-offs between the electromagnetic/thermal performance and the number of array elements (thus cost, design/fabrication/processing complexity). Note that the idea presented here can also be applied to different study cases employing different sector definitions, cooling strategies, chip/board characteristics etc. straightforwardly.

Acknowledgment

This research was conducted as part of the NWO-NXP Partnership Program on Advanced 5G Solutions within the project titled “Antenna Topologies and Front-end Configurations for Multiple Beam Generation". More information: www.nwo.nl.

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