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Au-based and Au-free Ohmic Contacts to AlGaN/GaN Structures on Silicon or Sapphire Substrates

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Abstract

Ohmic contacts to AlGaN/GaN with different metal stacks on Si or Sapphire substrate are fabricated and compared in this paper. For Au-capped ohmic contacts, the lowest contact resistances of $0.7 \Omega \cdot \text{mm}$ and $1.3 \Omega \cdot \text{mm}$ are achieved by Ti/Al/Ti/Au (20/110/40/50 nm) and Ti/Al/Ni/Au (20/110/40/50 nm) stacks, respectively. It also shows that the substrate material and epitaxial structure play an important role in ohmic contact engineering. For CMOS compatible Au-free structures, the Ti/Al/W (20/100/30 nm), Ti/Al/Ni/W (20/100/20/10 nm) and (20/100/10/20 nm) are demonstrated with the minimum contact resistance values of 0.45, 1.3, and $1.6 \Omega \cdot \text{mm}$, respectively. The three metal stacks of Au-free ohmic contact are compared and obtained results are explained.

1. Introduction

Nowadays, GaN based electronic devices are believed to be promising for high-efficiency power devices due to superior material properties such as high breakdown voltage, high thermal stability, high electron saturation velocity and high mobility realized by two-dimensional electron gas (2DEG) channel at the AlGaN/GaN heterojunction [1, 2]. One of the most important devices is the high electron mobility transistor (HEMT).

Typical AlGaN/GaN HEMTs utilize Au-based multi-layer metal stacks based on Ti/Al/X/Au for ohmic contacts. In these structures, Ti and Al react with GaN to form ohmic contact [3]. X is inserted to limit Au diffusion [4] with numerous metals e.g. Ti [5, 6], Ni [4], Mo [7, 8], Ta [9] previously reported. The role of Au in this structure is forming Ga vacancies in the semiconductor [10] and preventing the oxidation of the metal surface.

However, Au can slowly diffuse into the lower metal layers causing degradation [10]. Furthermore, Au is a contaminant in CMOS compatible micro-fabrication.

Therefore, Au-free ohmic contacts are of critical importance for adopting GaN technology in existing CMOS process lines.

Numerous attempts to form Au-free ohmic contacts have been previously reported, however no widely adopted common structure has been developed thus far. The low contact resistance of $0.22 \Omega \cdot \text{mm}$ was obtained by a complicated multi-layer stack consisting of Ta/Si/Ti/Al/Ni/Ta [11]. Another structure that achieved low contact resistance of approximately $0.5 \Omega \cdot \text{mm}$ is Ti/Al/W combined with barrier recess etching [10, 12]. While, low annealing temperature of 550°C was achieved by IMEC with acceptable contact resistance of $1.25 \Omega \cdot \text{mm}$, using barrier recess and Ti/Al/Ti/TiN stack [13].

In this paper, we fabricated and tested Au-based and Au-free metal stacks with and without recess in order to obtain low contact resistance for AlGaN/GaN heterostructure. The lowest contact resistance of $0.45 \Omega \cdot \text{mm}$ was achieved with recessed Ti/Al/W stack annealed at 820°C .

2. Experimental Procedure

The epitaxial structure for experiments was purchased from commercial vendors, the material was grown by MOCVD on C-plane sapphire and Si (111) wafers. For sapphire, the material stack, starting from the substrate, consisted of a proprietary nucleation layer, a 1.8 μm GaN buffer, a 1 nm AlN interlayer, followed by an undoped 21 nm $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ barrier and 1 nm GaN cap layer. On silicon, the stack consisted of a buffer layer, for lattice mismatch compensation, an intrinsic GaN layer,

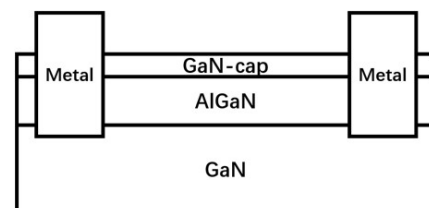


Fig. 1 The cross-sectional schematic view of Au-free ohmic contact structure.

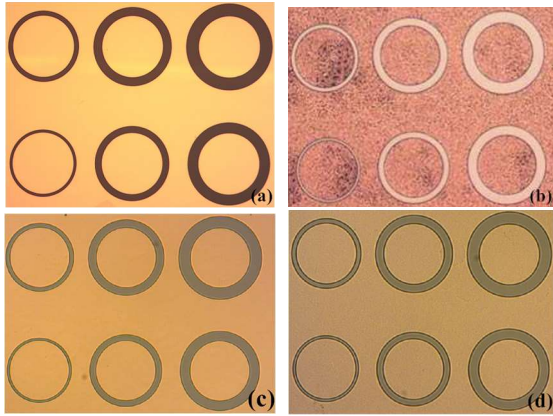


Fig. 2. The test pattern of CLTM. These pictures are different surface of: (a) gold-based surface before annealing; (b) gold-based surface after annealing; (c) gold-free surface before annealing; (d) gold-free surface after annealing.

followed by an undoped 24.7 nm AlGa_N barrier and 2.9 nm Ga_N cap layer.

The samples were first cleaned with chemical solutions of acetone, and isopropyl alcohol, and then rinsed with deionized water, and immediately blow dried with N₂. The dual-layers photoresist was coated on samples and patterned for metal lift-off. Prior Au-based ohmic contact deposition, samples were treated by HCl:H₂O (1:4) solution for 1 minute to remove the natural oxidation of Ga_N directly. For Au-free ohmic contact, the barrier recess was done by inductively coupled plasma (ICP) with BCl₃/Cl₂ chemistry prior to metal deposition. After an approximate 31 nm recess etching, the Au-free samples were also treated by HCl solution. Then, electron beam evaporation was used to deposit metal stacks immediately. For Au-based ohmic contact, on silicon and sapphire substrate, the thickness of Ti, Al, Ni/Ti, and Au layers were 20, 110, 40, and 50 nm, respectively. For Au-

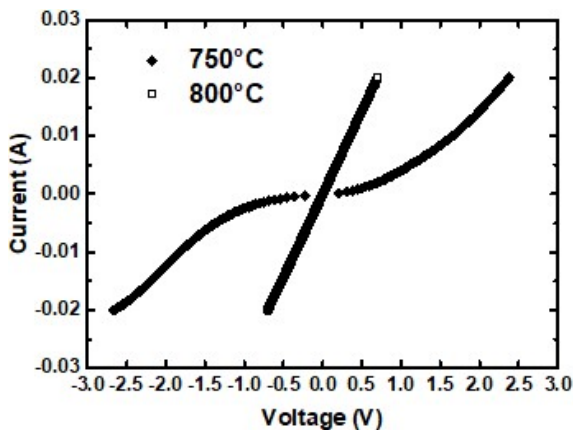


Fig. 3. I-V curves of Ti/Al/Ni/W (60/100/20/10 nm) ohmic contacts annealed at different temperatures. The measured at the gap spacing was 30 μ m. Lower temperature resulted in a rectifying contact.

free ohmic contact, three kinds of metal stacks: Ti/Al/W (60/100/30 nm), Ti/Al/Ni/W (60/100/10/20) and (60/100/20/10 nm) were deposited on separate pieces of the silicon substrate. After metal by lift-off the samples were annealed at different temperatures in N₂ ambient using rapid thermal annealing equipment. Au-based samples were annealed for 45 s, and Au-free samples were annealed for 30 s. The cross-section schematic view of Au-free structure is shown in Fig. 1. The circular transmission line method (CTLM) pattern, as shown in Fig. 2, was used for contact resistance characterization. A Keithley 4200 semiconductor characterization system was used to measure the electrical data of CTLM structure using 4-point probe method.

3. Results and Discussion

Fig. 3 illustrates the impact of annealing temperature. It is clear that contacts annealed at 750 $^{\circ}$ C show rectifying behavior, while increasing the temperature to 800 $^{\circ}$ C resulted in ohmic conduction. Only results of ohmic conduction are presented in the following sections.

Fig. 4 shows the resistance versus CTLM gap spacing measurements for Au-based and Au-free structures. Correction factors (c) were calculated and applied to measured resistance values R/c to account for CTLM geometry [14]. Linear fit of Au-free samples has the highest slope, lowest Y intercept and longer error bars. It is evident that Au-free results are less stable than Au-based results. The Au-free fit line has a higher slope and maximum X intercept, which suggests higher sheet resistance and lower transfer length [14] due to application of recess etching in these structures.

Fig. 5 (a) depicts the contact resistance of different

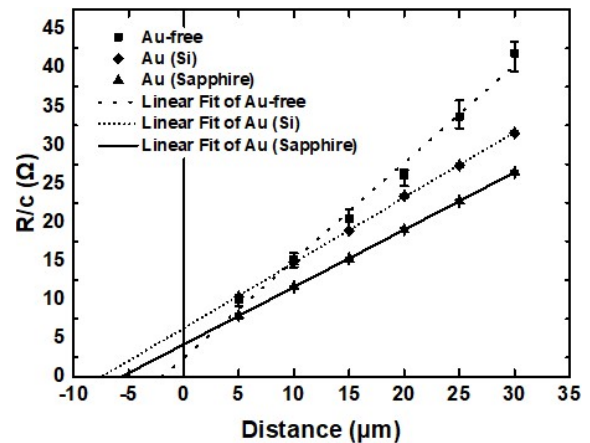


Fig. 4. Corrected resistance (R/c) versus CTLM gap spacing measurements. Au-free samples were annealed for 30 s at 800 $^{\circ}$ C. Both Au-based samples were annealed for 45 s at 830 $^{\circ}$ C. Each point is the mean value of 4 samples. The error bars indicate maximum and minimum measured values.

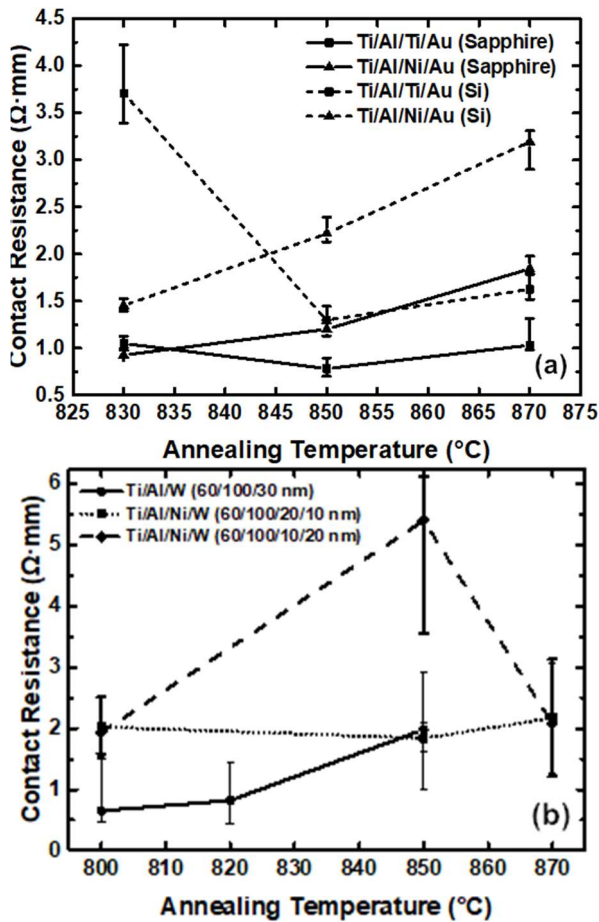


Fig. 5. (a) The Au-based contact resistance on Silicon and sapphire substrates. All samples were annealed for 45 s. (b) The Au-free contact resistance at different annealing temperatures. All samples were annealed for 30 s. The points are medians of the data. The error bars represent maximum and minimum measured values.

structures on two studied substrates. The best result on sapphire substrate is $0.7 \Omega \cdot \text{mm}$ at 850°C using Ti/Al/Ti/Au stack. The Ti/Al/Ni/Au stack on sapphire has the minimum value of $0.9 \Omega \cdot \text{mm}$. For silicon substrate, the best results were obtained as 1.3 and $1.5 \Omega \cdot \text{mm}$ at 830 and 850°C for Ti/Al/Ni/Au and Ti/Al/Ti/Au, respectively. Ti-barrier and Ni-barrier stacks have the lowest values at 850 and 830°C . These different trends of metal stacks are similar to those previously reported [9, 15]. **Fig. 5 (b)** shows the contact resistance dependence on annealing temperature for the studied Au-free metal stacks on silicon substrate. For Ti/Al/W (60/100/30) metal stack, the temperature for comparison are 800, 820, and 850°C . The results show that the ohmic contact is quite unstable but contact resistance is 0.65 and $0.83 \Omega \cdot \text{mm}$ in average for 800 and 820°C , respectively. For Ti/Al/Ni/W (60/100/20/10 nm) stack, the minimum value of $1.27 \Omega \cdot \text{mm}$ was obtained at 870°C . But the results at 850°C were more stable. For Ti/Al/Ni/W (60/100/10/20 nm) stack, the results of 850°C are higher than $3 \Omega \cdot \text{mm}$ and

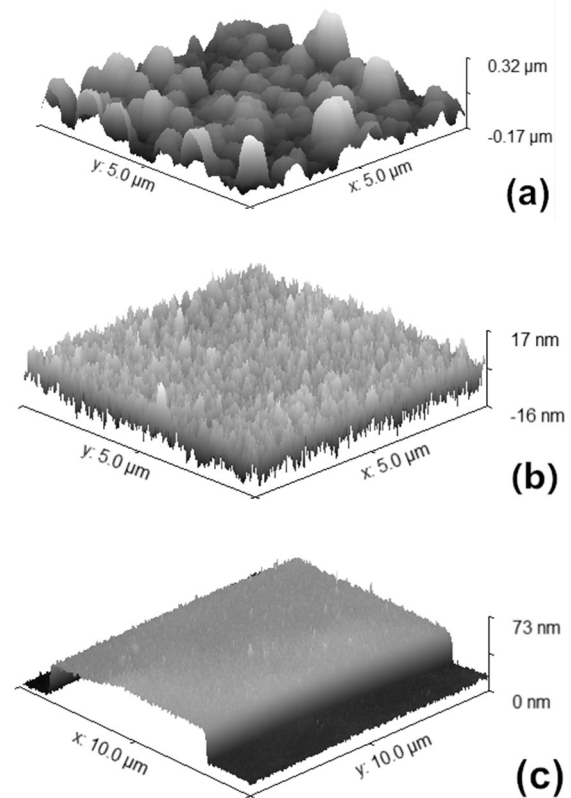


Fig. 6. The measurement of atomic force microscope. The 3-d view of (a) Au surface after annealing, (b) W surface after annealing, and (c) Au-free etched step.

all samples have longer error bars. The lowest contact resistances for metal stacks with Ni are higher than $1 \Omega \cdot \text{mm}$. As shown in the error bar, the stability is better than samples without Ni. Whether Ni can improve the stability of contact resistance need more experimental investigation to validate. Comparing with Au-based ohmic contacts, the instability in Au-free ohmic contact is possibly due to difficulty in controlling the AlGaN barrier recess process.

Besides, the benefit of CMOS compatibility for Au-free ohmic contacts, as shown in **Fig. 2** the Ti/Al/(Ni)/W metal stacks result in smoother surface after annealing and especially more acute edge morphology. **Fig. 6** is the atomic force microscope (AFM) scan result. The RMS is 4.867 nm and 72.5 nm for Au-free and Au-capped surface respectively on $5 \times 5 \mu\text{m}$. This is highly beneficial for the power/RF device down-scaling [12].

4. Conclusions

In summary, we have fabricated AlGaN/GaN ohmic contacts using both Au-based and Au-free metal stacks on two different epitaxial structures on Si or sapphire. The conventional Au-based (Ti/Al/X/Au) ohmic contact process is under superior control. For Au-free ohmic contact, our results indicate that Ti/Al/Ni/W (60/100/20/10 nm) metal stack with 850°C annealing

makes an acceptable ohmic contact with improved stability and surface morphology. The contact resistance can be further improved by controlling the etching depth uniformity and annealing conditions.

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