PROJECT RETINA

A new scalable driving and
counting system for SNSPDs

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SINGLE QUANTUM

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A new scalable driving and counting system for SNSPDs

by

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to obtain the degree of Master of Science
at the Delft University of Technology,
to be defended publicly on friday August 21, 2020 at 2:00 PM.

Student number:	1314491	
Project duration:	August 13, 2019 – August 21, 2020	
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This thesis is confidential and cannot be made public until August 20, 2022.

An electronic version of this thesis is available at `http://repository.tudelft.nl/`.

TU Delft

Abstract

The driving and counting electronics for the *Superconducting Nanowire Single Photon Detector*s (SNSPDs) fabricated and commercialized by *Single Quantum* (SQ) is currently designed to interface with at most 8 SNSPD channels. Single Quantum is already selling 24 channel systems and the trend is generally towards more channels. In those systems, multiple 8 channel drivers have been used in parallel. However, a redesign of the electronics is needed to allow such system to interface with an arbitrary number of channels, hence enabling new application areas, such as biomedical imaging.

Currently, each channel uses up to 5 W of power, which hinders a larger densely packed system. In addition, the current implementation has a counting dead-time of about 20 ms, which gives a significant slow down in characterizing the SNSPD. And last, the SNSPD might occasionally latch into resistive state and needs to be actively quenched back into superconducting state but the current system is not always able to perform such operation.

This project addresses those issues by making the system scalable in $n \times 12$ channels, reducing the high power consumption on each channel to 2.9 W, proposing a new counting mechanism such that the characterization of an SNSPD is sped up and all photon detections are counted, and proposing a new way to actively quench all types of SNSPD implementations.

The functionality for a 12 channel system is split in *Channel Unit*s and a *Main Control Unit*. The channel units count, bias and control a single SNSPD and communicate with the main control unit through a CAN-FD bus. The main control unit communicates all data from the channel units to the *Graphical User Interface* (GUI) through ethernet and vice versa translate the control commands from the Graphical User Interface to the channel units. All units are based on the LPC54618 microcontroller by NXP.

The newly designed system has been tested to work for up to 12 channels, and can be housed in a 19 inch rack mountable enclosure. Using an ethernet switch allows for interfacing with $n \times 12$ channel systems.

This system design paves the way towards the bias and readout of, for instance, a 10×10 SNSPD array such that detailed spatial information may be added at the single photon level.

Acknowledgements

I would like to thank the following people and authorities that have made it possible for me to follow this path of becoming a Master in Computer Engineering.

Andreas Fognini, my supervisor at Single Quantum. For your advice and feedback throughout the past year and for the opportunity to do my Master's-thesis at your company.

Fabio Sebastiano, my supervisor at TU Delft. Your advice and feedback, both technical and non-technical, has helped me give structure to the thesis.

My former colleague and friend Remco de Wit, for your help in hardware debugging, i.e., as a substitute "rubber duck" [3].

My dear friend Laurens de Vos, for making the front page illustration [14].

My employer, Rotterdam University of Applied Sciences, for giving me time off for my studies. And all my colleagues who had to adjust their agenda due to my overloaded agenda in the last 6 years.

And finally my spouse Digna for being the cornerstone in my life. Thank you for your support during the 9 years that it took me to finish my studies and to help me fulfill this goal.

ing. T.J.W. (Tijmen) van Eijk
Delft, August 2020

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Acronyms

ADC Analog to Digital-Converter

AWG Arbitrary Waveform Generator

CML Current-Mode Logic

CU Channel Unit

DAC Digital to Analog-Converter

DMA Direct Memory Access

DNL Differential Non-Linearity

ECL Emitter-Coupled Logic

EEPROM Electrically Erasable Programmable Read Only Memory

EMC ElectroMagnetic Compatibility

ENBW Equivalent Noise BandWidth

FF Flip-Flop

FWHM Full Width at Half Maximum

GPIO General Purpose Input-Output

GUI Graphical User Interface

IC Integrated Circuit

IDE Integrated Development Environment

INAMP Instrumentation Amplifier

JSON JavaScript Object Notation

LDO Linear Drop-Out

LVDS Low-Voltage Differential Signaling

MCU Main Control Unit

MII Media-Independent Interface

PCB Printed Circuit Board

PCIe Peripheral Component Interconnect Express

PLL Phase-Locked Loop

POE Power Over Ethernet

PSU Power Supply Unit

RMII Reduced Media-Independent Interface

RMS Root Mean Squared

RT-Amp Room-Temperature Amplifier board

Sa/S Samples Per Second

SEM Scanning Electron Microscope

SMA Sub-Miniature A connector

SMP Sub-Miniature Push-on

SNR Signal to Noise Ratio

SNSPD Superconducting Nanowire Single Photon Detector

SPI Serial Peripheral Interface

SQ Single Quantum

TDC Time to Digital Conversion

TTL Transistor-Transistor Logic

UART Universal Asynchronous Receiver-Transmitter

Nomenclature

channel SNSPD with counting, bias and amplification electronics

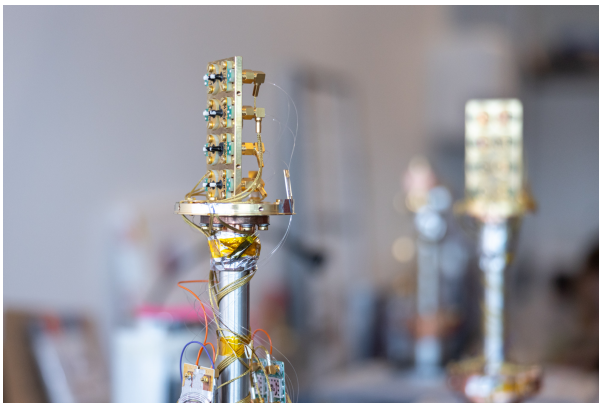
system 12-channel system

1 Introduction

Single Quantum (SQ) produces the world's most sensitive single photon measurement device using Superconducting Nanowire Single Photon Detectors (SNSPDs). These detectors combine high detection efficiency (≥90 %) with low dark count rates (< 1 Hz) and low timing jitter (< 15 ps) [12, 16, 25].

The detectors are mounted on a cold head (shown in fig. 1.1b) in a cryostat and cooled down to 2.5 K. The detectors are single-mode fibre coupled to the optical input terminals. An analog electrical output terminal is provided for each detector that carries the voltage pulses indicating single photon detections. A complete cryostat is shown in fig. 1.1a.

(a) A 24-channel cryostat.



(b) 8 detectors mounted on a cold head.

Figure 1.1: A complete cryostat in fig. 1.1a and a cold head in fig. 1.1b.

The existing commercial system (in this thesis referred to as the "old system") that drives and counts the photon detections (depicted in fig. 1.2a) amplifies the voltage pulses such that they can be used by, for instance, time-tagging devices connected to the analog output. A block diagram for 1 channel is shown in fig. 1.2b. The comparator receives the amplified voltage pulses and translates them to discrete levels which are used as the input to the counting circuitry.

The old system uses a *Printed Circuit Board* (PCB) (the Data and Aquisition (DAQ)-card) which houses 4 channel counting circuits and a microcontroller. The microcontroller has the following functions:

- It controls and reads the counting circuitry.
- It sets the trigger level for the comparators.
- It measures the voltages over the detectors.
- It sets bias currents for the detectors.

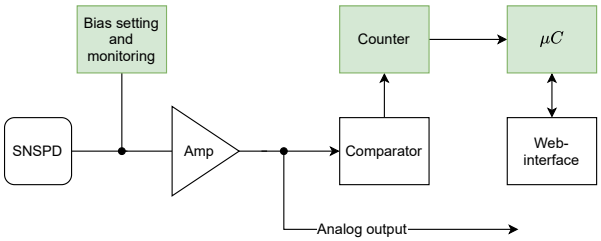
The microcontroller in the old system lets the counting circuitry count photon detections for a certain set interval (10 ms up to 1 min), reads this count data and sends it to a webserver that hosts a web-interface. During the read and send time the counting circuitry is idle. This introduces the so-called "dead-time" in the counting mechanism (up to 20 ms per integration interval) and leads to uncounted photon detection events.

The web-interface in incorporated the old system and enables:

- Finegrained control settings for all channels.
- Detector characterization.
- Channel count rates.

Up to 2 DAQ-cards (8 channels) can be connected to the web-interface hardware.

(a) 2 old systems, each has 8 detector drive and counting circuits



(b) Current implementation of a single channel.

Figure 1.2: Old system front and single channel architecture

A typical commercial measurement system currently contains up to 24 detectors. To interface with 24 detectors, several 8 channel drivers have to be used in parallel. SQ's current customers asks for more channels and possible new application area's need more channels, therefore SQ wishes to create a system in which the number of channels can be added virtually without limit, with at least 60 channels envisioned in the near future. This introduces scalability issues with the current implementation since the counting circuitry by itself draws up to 4 W per channel, the web-interface can not control and readout more than 2 DAQ-cards and the deadtime-time is an unwanted effect.

This thesis will develop the first prototype for "Project Retina", named after the light-sensitive part of the human eye, as it will open the way for driving and readout of SNSPD arrays, allowing precise 2D-imaging at the single photon level.

1.1. Motivation

Currently, the system is mostly used in quantum information processing, such as quantum cryptography and quantum communication [20]. It also finds applications in metrology, for instance in characterizing single photon emitters using the HBT protocol [19] and in meteorology, for example measuring the wind profile [24]. SQ wants to broaden the application area of its systems to the colored area's shown in fig. 1.3 (red is area where systems from SQ are currently used). Each of the areas need different specifications for the detectors and its subsequent system with drive and readout electronics in order to fit the specific application. For instance, astrophysics needs detectors with a large detection area that can be coupled to multimode fibers [23], while medical imaging and bio-luminescence needs a detector array resulting in added spatial information to the measurement [17, 22]. A general redesign of the system such that it can accommodate for varying demands from application areas is therefore paramount.

1.2. Goals

The following goals (**G#**) have been formulated at the start of the thesis and are prioritized by the MoSCoW method: Must have (M), Should have (S), Could have (C) and Wont have (W).
By the end of this project:

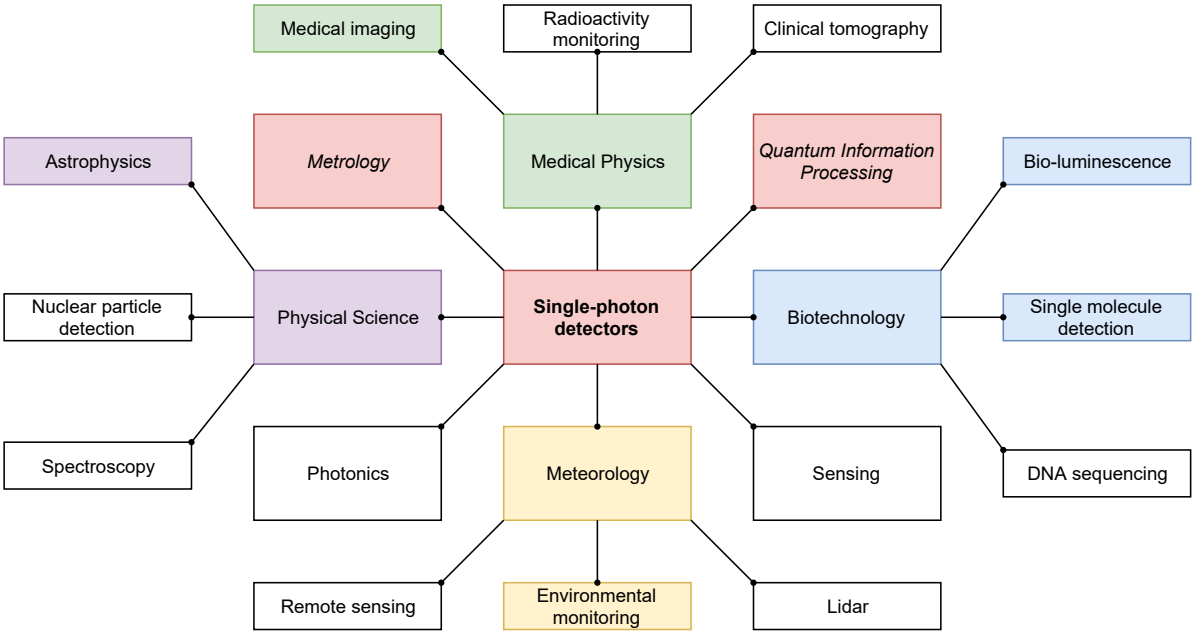


Figure 1.3: Single photon detection application areas, partially redrawn from [13].

G1 (M) A system is designed that can be scaled up to 60 channels, meaning that without re-configuring the software or redesigning the hardware of the system, channels can be added.

G2 (M) The amount of channels n, can be added one by one up to $n = 60$.

G3 (M) The scalable system is verified to work for up to 12 channels.

G4 (S) The system has a digitized detection output for each channel.

1.3. Scope

The scope of this thesis is redesigning the system architecture such that it becomes scalable, including the counting, bias setting, measurement and communicating with a webserver. It does not include a possible redesign of the amplifier stages and comparator circuit and will not include a redesign of the webserver. For a single channel, the scope is colored in green in fig. 1.2b.

1.4. Outline

Chapter 2 introduces the concept of SNSPDs, its technical specifications and a comparison between different commercial SNSPD systems. Their technical specifications are compared to the current state of the art system from SQ. The analysis of the old system and its shortcomings are elaborated on in chapter 3. This chapter also contains the functional decomposition of the new design using the structured analysis method by [26], which results in the system requirements. In addition, a prediction will be made on the possible improvements that this thesis will implement. Chapter 4 elaborates on the proposed architecture and the interfaces between subsystems. In chapter 5, the process of getting to a fully functional prototype of the system will be explained, which contains the justification of the software and hardware designs. The test procedures and results will be presented in chapter 6. To conclude, in chapter 7, the results will be compared to the old system, improvements will be stated and future work will be proposed.

2

The Detector

The core component of the single photon measurement system produced by SQ is the SNSPD. An image of a bonded SNSPD is shown in fig. 2.2a. Combining good timing resolution (low jitter), high detection efficiency, low dark counts at wavelengths surpassing 1550 nm are key performance characteristics of a SNSPD. The photon detection rate is a limiting factor due to the "click" working principle (The detector either "clicks" at a photon detection or it does not) versus the "linear" working principle of a photodiode.

In the following chapter the working principle of a SNSPD will be explained and its characteristics will be described.

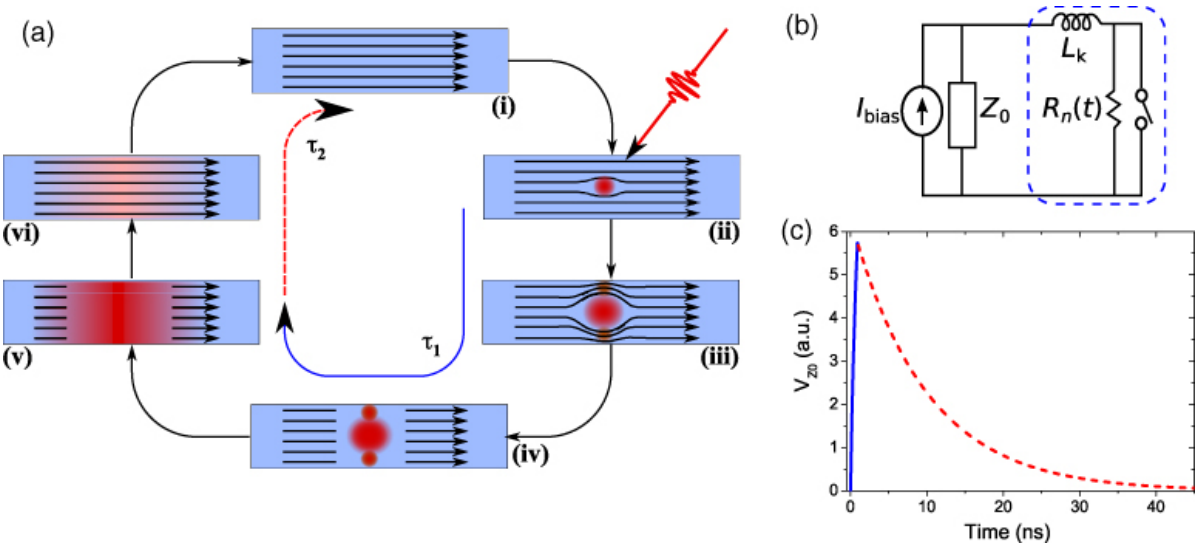


Figure 2.1: Basic operation principle of an SNSPD, reprinted from [21].

2.1. Concept

Figure 2.1a shows the detection cycle of a SNSPD:

(i) The superconducting nanowire, maintained well below the critical temperature, is DC-biased below its critical current (see section 3.1.1). (The critical temperature is the temperature below which a superconducting state of the wire can be maintained, while the critical current is the maximum current through the SNSPD for which the superconducting state can be maintained.)

(ii) When a photon is absorbed by the nanowire a small resistive hotspot is created.

(iii) The supercurrent is forced to flow along the periphery of the hotspot. Since the NbTiN nanowires are narrow, the local current density around the hotspot increases, exceeding the superconducting critical current density.

(iv) This in turn leads to the formation of a resistive barrier across the width of the nanowire.

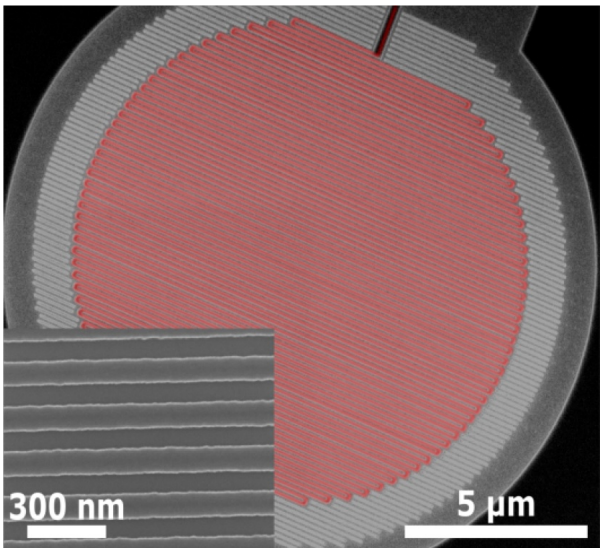
(v) Joule heating (via the DC bias) aids the growth of resistive region along the axis of the nanowire until the current flow is blocked and the bias current is shunted by the external (read-out) circuit.

(vi) This allows the resistive region to cool down and the wire becomes fully superconducting again. The bias current through the nanowire returns to the original value (i) [21].

An electrical equivalent model of the bias circuit and SNSPD is shown in fig. 2.1b. The elements in the dashed rectangle comprise a model of the SNSPD. The switch is normally closed (superconducting state). When a photon hits, the switch opens creating a resistive path. This resistive path is orders of magnitude more resistive than the impedance of the readout circuit, pushing the bias current to this circuit such that it can be read out. The inductance L_k is due to the kinetic inductance of the nanowire caused by the high mobility of the charge carriers in a superconductor. Counter-intuitively, the inductance due to the meandering pattern of an SNSPD as shown in fig. 2.2b is several orders of magnitude smaller and can therefore be neglected.

The voltage pulses seen by the readout circuit have a shape as shown in fig. 2.1c. It shows the rise time τ_1 at a photon detection and the time τ_2 needed to get back to superconducting state, enabling another photon detection. In this period $\tau_1 + \tau_2$ the detector is "blind" to photons hitting its surface. This limits the detection rate of the SNSPD.

(a) 4 bonded detectors.



(b) Scanning Electron Microscope image of an SNSPD, reprinted from [18].

Figure 2.2: Physical view of a SNSPD.

2.2. Characteristics

SNSPDs have detection limitations. These are due to the characteristics of the SNSPD and will be explained in the following sections.

2.2.1. Detection Efficiency

The efficiency of detecting single photons is an important characteristic of a SNSPD, as it describes the probability that when a photon is sent to the SNSPD it will result in an electrical pulse at the output. This characteristic can be factored in 3 different components [15]:

1. The probability of an electrical pulse generation due to an absorbed photon.
2. The photon absorption efficiency of the superconducting nanowire.
3. The optical coupling efficiency between the incident light and the active area of the detector.

State-of-the-art detection efficiency is around 92 % [16].

2.2.2. Dead time
As stated before, the time for the SNSPD to return to the superconducting state after absorbing a photon is finite and typically in the order of 10 ns. This limits the detection rate of the detector. Single Quantum regularly produces detectors with 100 MHz count rates and experimental detectors with even higher rates. Currently, the highest detection rate is above 1.5 GHz [27].

2.2.3. Timing jitter
Timing jitter is another valuable characteristic of an SNSPD. It describes the difference in arrival times of the amplified voltage pulses at the analog output of the system with respect to a reference. This is expressed in *Full Width at Half Maximum* (FWHM). Timing jitter is measured using a pulsed laser input with an electrical interface. This interface can be used to trigger an oscilloscope every time the laser is pulsed. The amplified voltage pulses are measured by a high-speed oscilloscope (typically with 40 G*Samples Per Second* (Sa/S)) and the time difference between trigger and arrival of the pulse is measured and plotted in a histogram. The timing jitter is highly influenced by the noise caused by the readout circuitry, since the voltage pulses coming from the SNSPD are small (in the order of 100 µV) before getting amplified.

The timing jitter of the system created by SQ can be below 15 ps FWHM.

2.2.4. Dark counts
Dark counts are electrical pulses occurring while no photons are sent deliberately to the detector. These dark counts are mainly due to black body radiation. The detection of black body radiation occurs since the detectors have some detection efficiency at wavelengths other than what they are designed for.They are false counts and should be taken into account during measurements. Typical dark count rates for the detectors are in the order of 100 counts per second (cps) but can be as low as 0.01 cps for detectors designed for 800nm.

2.3. Read-out options
Either one or both of the circuits as shown in the blue and red dashed boxes in fig. 2.3 can be connected to the detector to improve the readout characteristics of the detector before the pulse exits the cryostat. The output of the circuit is the input for the amplifier board which is described in section 3.3.4. The following sections will explain why each of these circuits have been designed.

Table 2.1: Values for fig. 2.3.

R_n	L_k	R_{bs}	R_{bp}	R_c
$\approx 1\,\mathrm{M\Omega}$	$\approx 500\mathrm{nH}$	$20\,\Omega \leq R_{bs} \leq 200\,\Omega$	$20\,\Omega \leq R_{bp} \leq 200\,\Omega$	$\approx 70\,\mathrm{k\Omega}$

2.3.1. Bridge
The bridge (dashed blue box) consists of 2 resistors R_{bs} and R_{bp}. These resistors help reducing the deadtime, hereby increasing the count rate. This is due to demagnetizing the magnetic field in the inductance L_k faster such that τ_2 becomes shorter. If we take the demagnetization current $i(t) = K \cdot \mathrm{e}^{-\frac{R}{L_k} \cdot t}$, some constant K and R the series resistance $R_n + R_{bs} + R_{bp}$, increasing R would result in a steeper negative exponential resulting in a faster return to superconducting state. R can not be made infinitely large since then the detector would stay in resistive state. Fine-tuning of the bridge resistors is quite time consuming since they are chosen based on the SNSPDs measured characteristics. If the high count rate is not a requirement, the bridge resistors are left out.

2.3.2. Cryogenic Amplifier
The cryogenic amplifier (dashed red box) consists of a capacitively-coupled high-frequency amplifier that amplifies the signal before leaving the cryostat and a bypass resistor R_c that allows the DC bias current to be injected from the signal line. The amplifier reduces the timing jitter since the *Signal to Noise Ratio* (SNR) at low temperature is much better (for instance the Johnson-noise $v_n = \sqrt{4kTR}$ is reduced by a factor of ≈ 12).

The bypass resistor allows the SNSPD to be biased by a DC current through a DC offset on the RF-line. This reduces the amount of cabling that needs to go into the cryostat. Two additional cryogenic cables would otherwise be needed to bias the system and monitor the voltage over the SNSPD. These cables transmit some heat, putting pressure on the cryostat cooling power, are expensive and quite complex to solder. Adding

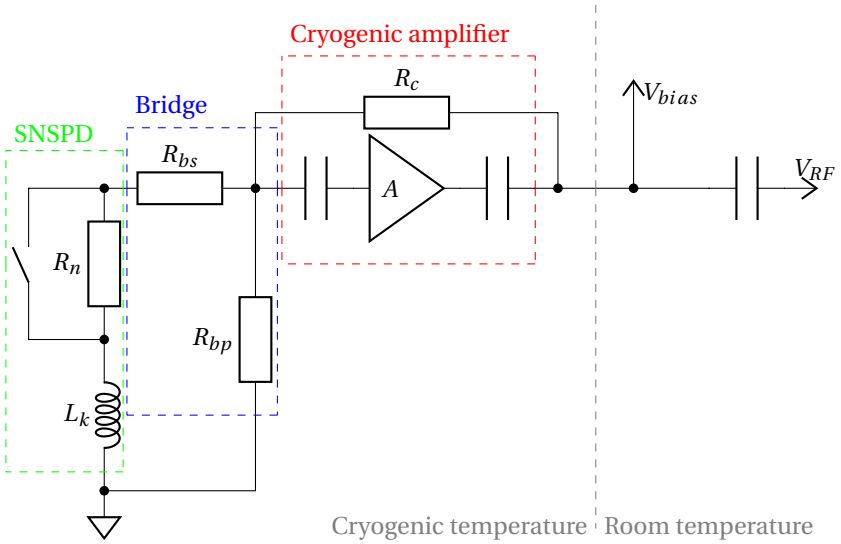


Figure 2.3: Bridge and/or Cryogenic amplifier additions to the SNSPD.

a cryogenic amplifier to the system is straightforward, and reduces the gain and noise requirements of the amplifier stage at room temperature. It increases the total system cost but reduces the jitter of the system.

2.4. Comparison with competitors

There are a couple of other companies that sell SNSPD systems. However, they all differ on some or multiple aspects of the complete system. To give a quick overview, table 2.2 has been compiled and shows the similarities and differences.

Table 2.2: Comparison of SNSPDs systems.

λ : 800 nm/1550 nm	SQ[10]	Quantum Opus[8]	Photon Spot[7]	Scontel[9]	IDQ[6]
Efficiency	90 %/85 %	90 %/80 %	85 %	85 %/80 %	90 %
Dark Counts	≤ 1 Hz/ ≤ 300 Hz	≤ 1 Hz/ ≈ 100 Hz	≤ 100 Hz	≈ 10 Hz	≤ 1 Hz
Timing Jitter	< 15 ps/ < 50 ps	< 80 ps/ < 100 ps	≈ 70 ps	≈ 45 ps	≈ 20 ps
Dead time	≈ 10 ns	≈ 50 ns	≈ 50 ns	≈ 10 ns	≈ 5 ns
Operating Temp	≈ 2.5 K	≈ 2.5 K	≈ 0.8 K	≈ 2.5 K	≈ 0.8 K
Cool down time	≈ 5 h	≈ 5 h	≈ 12 h	≈ 5 h	≈ 12 h
Cont. operation	Yes	Yes	No	Yes	No
Hold time	10000 h	10000 h	36 h	10000 h	40 h
PC controlled	Yes	No	No	No	Yes
Active quenching	Yes	No	No	No	Yes
Photon counting	Yes	No	No	No	Yes
# Channels/system	24	16	?	8	16

The table shows an advantage of using a detector that works at 2.5 K. It can be cooled by a closed cycle cryostat which allows for continuous operation. Photon Spot and ID Quantique (IDQ) use a cryostat that can not be used continuously. An autonomous system that shows the photon count data, can actively quench the detector when it is latched (more on that in section 3.1.1), and can characterize the detectors is only made by one competitor in the field: ID Quantique.

2.5. Conclusion

A SNSPD is a so called “binary”, or “click” detector. It either detects a photon or it does not. This allows for very precise photon measurement devices. The devices come with some limitations such as limited detection rates and timing jitter. These limitations are improved by some readout-options. In the following chapter, it will become evident that these readout-options directly have an influence on the subsequent amplification stages and how the SNSPD is monitored to be in superconducting state.

3

Analysis

This chapter explains the limitations of the old system, describes the company requirements, sketches the context of the new system, and shows its functional decomposition based on the structured analysis method by Yourdon [26]. Following from the limitations, the new system context or the structured analysis, the requirements will be presented directly in the following way:

G-REQ 1 ...

All requirements are summed up in appendix A.

3.1. Old system

As can be seen in fig. 3.1, the old system architecture is constructed in a tree-like fashion: The web-interface, 2 DAQ (Data and AcQuisition)-cards and electronics for each channel (C.x).

A single channel circuit was shown in chapter 1 and is reprinted in fig. 3.2. The 4 counters, the microcontroller (μC) and the bias setting and measuring functions are placed on the DAQ-card. The amplification stage and comparator are placed on a separate PCB for each channel on (C.x). This PCB is called the *Room-Temperature Amplifier board* (RT-Amp) and will be described in section 3.3.4.

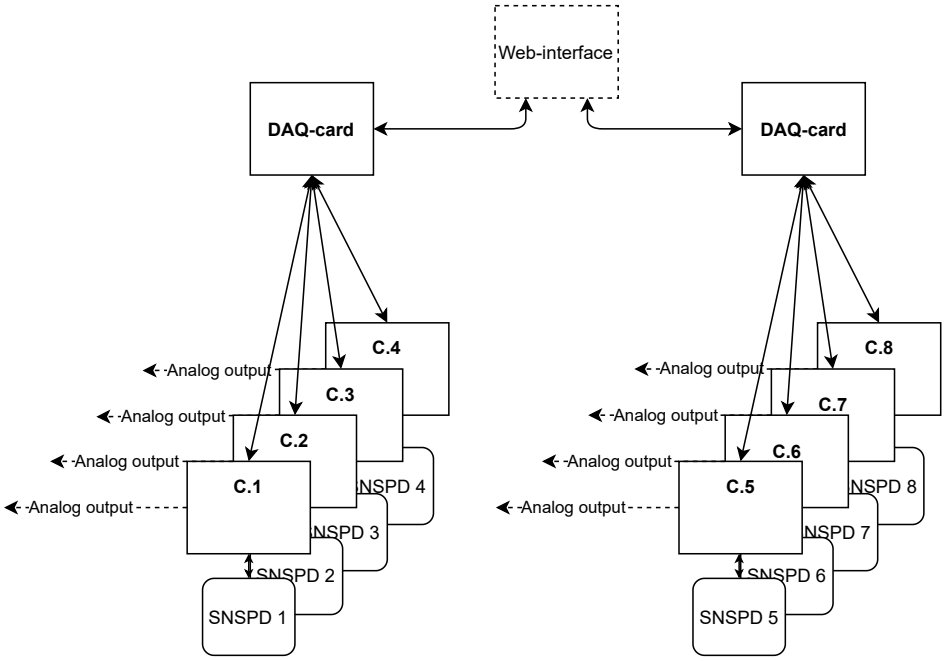


Figure 3.1: Old system architecture.

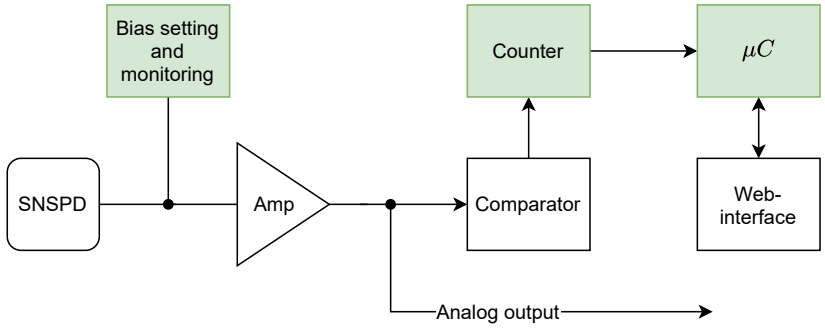


Figure 3.2: Current implementation of a single channel.

The following sections will explain the functionality and the limitations of each unit in the old system.

3.1.1. Bias setting and monitoring

The bias setting and monitoring circuit of the old system is depicted in fig. 3.3. Biasing of the SNSPD is done using a 16 bit dual supply DAC with a range between $-10\,\text{V} \leq V_{dac} \leq 10\,\text{V}$. It supplies the current I_{bias} to the SNSPD on the RF-line through R_x,R_y and R_z resulting in a bias current ranging from $-66\,\mu\text{A} \leq I_{bias} \leq 66\,\mu\text{A}$. The company requires the precision of the bias current to be set within 100 nA which results in the accuracy of the DAC to be at least 15 mV. V_{RF} is the signal containing the photon detection pulses which is connected to the "Amp" in fig. 3.2. The C's are in place to construct a low pass filter structure with $f_c \approx 212\,\text{Hz}$ such that the high frequency pulses do not interfere with the bias source .

Table 3.1: Values for fig. 3.3.

R_1	R_2	R_3	R_x	R_y	R_z	C
100 kΩ	100 kΩ	100 kΩ	50 kΩ	50 kΩ	50 kΩ	15 nF

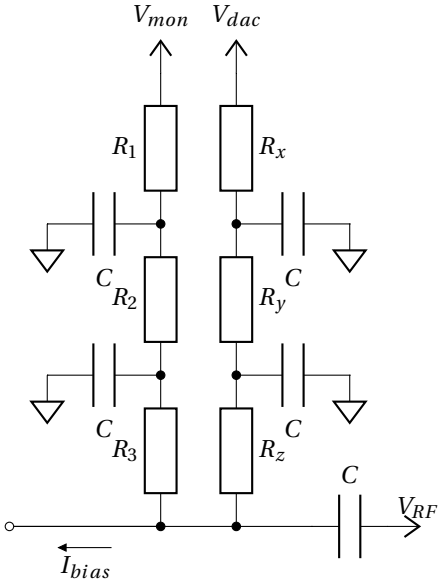


Figure 3.3: Current latch detection and bias current injection

When a SNSPD is biased close to its critical current (the current at which the SNSPD transitions from superconducting state to resistive state), it can happen that it remains in a resistive state with a value R_n of about 1 MΩ due to an excess of Joule heating. This is called a *latch* event. To undo a latched detector, the current through the SNSPD must be actively brought back to 0 such that the SNSPD can return to superconducting state. This is called *active quenching*.

A latched detector is currently being detected by monitoring the DC voltage (V_{mon}) on the RF-line. When the DC voltage jumps from approximately 0 V to a value distinguishable by the ADC connected to V_{mon}, the bias voltage is switched off for 1 s (t_{latch}). This relatively long period is due to the RC time imposed by the bias current injection circuit.

Currently, the system is not able to detect and actively quench the SNSPD when both the Bridge and the Cryogenic Amplifier are in place, see fig. 2.3. This is due to the combination of the bridge resistors R_{bs}, R_{bp}, and the bypass resistor R_c. The change in voltage when both are placed, $\Delta V_{mon} = V_{mon,latched} - V_{mon,unlatched}$, when the SNSPD latches from 0 Ω to 1 MΩ (R_n) can not be distinguished by the12 bit ADC that samples V_{mon}.

For example when V_{dac} is constant, $R_{bs} = R_{bp} = 100\,\Omega$ and $R_c = 70\,\text{k}\Omega$ results in a voltage change on V_{mon} at a latching event:

$$\frac{V_{mon,unlatched}}{V_{dac}} = \frac{R_c + R_{bs} /\!/ R_{bp}}{R_x + R_y + R_z + R_c + R_{bs} /\!/ R_{bp}} = \frac{70\,\text{k}\Omega + 100\,\Omega /\!/ 100\,\Omega}{220\,\text{k}\Omega + 100\,\Omega /\!/ 100\,\Omega} = \frac{467}{1467} \tag{3.1}$$

$$\frac{V_{mon,latched}}{V_{dac}} = \frac{R_c + (R_{bs} + R_n) /\!/ R_{bp}}{R_x + R_y + R_z + R_c + (R_{bs} + R_n) /\!/ R_{bp}} = \frac{70\,\text{k}\Omega + (100\,\Omega + 1\,\text{M}\Omega) /\!/ 100\,\Omega}{220\,\text{k}\Omega + (100\,\Omega + 1\,\text{M}\Omega) /\!/ 100\,\Omega} \approx \frac{701}{2201} \tag{3.2}$$

$$\Delta V_{mon} \approx 155 \cdot 10^{-6} \cdot V_{dac} \tag{3.3}$$

As V_{dac} is set somewhere in the range:

$$-10\,\text{V} \leq V_{dac} \leq 10\,\text{V} \tag{3.4}$$

This results in ΔV_{mon}:

$$-1.55\,\text{mV} \leq \Delta V_{mon} \leq 1.55\,\text{mV} \tag{3.5}$$

The absolute value of V_{mon} that has to be sampled by the ADC ranges from:

$$-\frac{467}{1467} \cdot 10\,\text{V} \leq V_{mon} \leq \frac{467}{1467} \cdot 10\,\text{V} \Rightarrow -3.18\,\text{V} \leq V_{mon} \leq -3.18\,\text{V} \tag{3.6}$$

If the ADC would be referred to exactly this voltage range, the theoretical minimal LSB step would be:

$$\frac{6.36\,\text{V}}{2^{12}} \approx 1.55\,\text{mV} \tag{3.7}$$

Therefore, the latch detection and active quenching circuit has to be redesigned.

Another type of latching is due to an impedance mismatch with the subsequent readout circuit. It might occur that the detector starts oscillating at some point in time due to an unwanted $\frac{L}{C}$ resonance in the RF-circuit. This is called *frequency latching* and is detected by the counter exceeding some upper frequency bound f_u. It is corrected in the same fashion as DC-latching, interrupting the bias current for 1 s. As a redundant functionality, there is also a lower frequency bound f_l that can be set (e.g. 0.0001 Hz) which helps in detecting a DC-latch for if no counts at all occur (not even dark counts) the detector must be latched. Based on the above, the following requirements were set:

G-REQ 1 The system shall be able to supply a bias voltage at least between −10 V and 10 V with steps of 1 mV over the bias circuit for each detector, the accuracy must be ±1 mV.
G-REQ 2 The system shall monitor the voltage over the SNSPDs every 10 ms.
G-REQ 3 The system shall be able to automatically unlatch the SNSPDs including those that are equipped with a bridge and/or a cryogenic amplifier circuit.
G-REQ 4 The system shall be able to unlatch the SNSPDs due to frequency latching.

3.1.2. Comparator

After careful filtering and amplification of about 60 dB, the signal is routed to a *Sub-Miniature A connector* (SMA) for direct analog output and tapped off to a comparator (ADCMP572) circuit. This comparator receives an external trigger level between 0 V to 2.25 V. This trigger level is filtered and buffered reducing noise and interference before being supplied to the comparator. The accuracy constraints for the DAC supplying the level are not tight since the photon detection pulses are amplified to ~100 mV. Therefore an inexpensive

12 bit DAC can be used. The comparator output is *Current-Mode Logic* (CML) with a specified minimal output pulse-width of 100 ps.

As stated in section 2.2.2, SQ regularly produces detectors with detection rates of 100 MHz and experimental detectors with even higher detection rates. It is observed that, in research facilities, SNSPDs have been manufactured that exceed the 1 GHz detection rate threshold [27]. Therefore, the system must at least be able to count up to 1 GHz.

The accuracy is limited for high detection rates to ±20 counts since they are negligible on count rates exceeding $\geq 50 \cdot 10^6$. For detection rates below 50 MHz the accuracy becomes relevant since dark count rates, as explained in section 2.2.4, can be as low as 0.01 Hz.

G-REQ 5 The system shall be able to count from 0 Hz to 1 GHz pulses coming from a comparator CML/ECL output with a minimum pulsewidth of 100 ps. The accuracy in the range ≤ 50 MHz is ±1 count. The accuracy for counts between 50 MHz and 1 GHz is ±20.
G-REQ 6 The system shall be able to adjust the trigger level of the comparators between 0 V and 2.25 V with at least 12 bit resolution.

3.1.3. Counter

The counter setup is as follows: Directly connected to the comparator is a MC100E137, an 8 bit ripple counter. The 8 *Emitter-Coupled Logic* (ECL) outputs connected via an ECL to TTL translator to a SN74HC165 8 bit shift register that serially clocks the data into the microcontroller.

The MC100E137 ripple counter is obsolete. This imposes a supply chain problem. Next to that, ECL is very power hungry, as each counter circuit in the old system by itself has been measured to draw as much as 4 W per channel. This must be reduced, otherwise the power supply might become the limiting factor in the new scalable system. Therefore a requirement on the power needs for each added channel is set:

G-REQ 7 Each added channel (SNSPD with counting, bias and amplification electronics) will require at most an additional 3 W.

3.1.4. Microcontroller

The microcontroller is a dSPIC33 and next to digitally interfacing with the ADCs and DACs it requests counts every set count interval and receives counts from 4 shift registers into 1 data input port. Each integration interval, the web-interface requests count data from the microcontroller. This data request/send is done through RS-232. During this send time possible photon detections are not counted. This can be up to 20 ms for each send operation.

G-REQ 9 The system shall be able to count and send count datapackets without dead-time.

3.1.5. Web-interface

The web-interface communicates through an RS-232 connection with the microcontroller on the DAQ-card asking for counts each set integration interval. The system user can access the web-interface through an internet browser. The section 3.3.1 will elaborate on the relevant commands and received data for the web-interface in more detail.

3.2. Company Requirements

Multiple discussions have been performed with the representatives of the following teams within SQ: Sales, production, development, and testing. These discussions had the goal to do requirements trawling such that the new system complies with the customers' (possible future) requirements but also the requirements that allow for fast production and easy testing of the system and detectors. These requirements could be split in 3 categories: housing, flexibility and power supply. The next sections will explain these categories and state their requirements.

3.2.1. Housing

The old system is housed in a custom designed enclosure for either 2, 4 or 8 channels as seen in fig. 1.2a. This is not a nice solution for systems that must house more channels. Therefore, a more regular design must be thought of. The decision was made that the new system will be housed in 19 inch rack mountable enclosures. The height of the RT-Amp (see section 3.3.4) is about 47 mm and must be able to fit into the housing. Therefore the smallest height of the enclosure must be 2U (about 89 mm).

G-REQ 16 The system will be mounted in a 19 inch rack using 2U height casings.

3.2.2. Flexibility

Based on the housing requirement **G-REQ 16** another requirement has to be addressed: the connection from all enclosures to the webserver. One of these enclosures needs to contain the webserver that establishes the web-interface through ethernet. Therefore a regular ethernet connection with a dedicated ethernet switch to connect all enclosures to, creates the highest flexibility regarding placement of the webserver in one of the enclosures. In addition, it allows for a single robust design of the housing that can be used for either the system that holds the webserver or the other systems that have to connect to it.

G-REQ 8 The system shall have an ethernet connection with the web-interface.

The customers or institutions to which SQ sells its system have different needs in number of detectors and might have new needs as research in these institutions progresses. Therefore adding or replacing channels without the need to reconfigure the software and hardware that the channel interfaces with, is a wanted requirement for the new system.

G-REQ 17 The system shall be able to scale up to at least 60 channels.
G-REQ 18 The system shall be able to add channels one by one without reconfiguring the software or the interfacing hardware.

The functionality on the RT-Amp board (explained in section 3.3.4) and the functionality that needs to be implemented by the new system will be kept on separate boards such that the development of these functions can be done in parallel. This also increases the flexibility of the new system. In this way, the new system can interface with different implementations of the RT-Amp boards. For instance, there are already 2 different types of RT-Amp boards, they have different gain dependent on the presence of a cryogenic amplification stage.

3.2.3. Power supply

The system will be designed to be scalable to at least 60 or more channels, therefore considering the way the system will be powered is relevant. The old system uses an off-the-shelf power adapter converting 230 VAC to 18 VDC. To house 60 channels or more, multiple 2U enclosures will be placed on a 19 inch rack which all need individual connections to a power source. Using multiple power adapters for each 2U enclosure would result in a rather messy setup.

Since the system will have a web-interface that can be connected to through ethernet, the idea arose to use *Power Over Ethernet* (POE). This would reduce the number of cabling and components for power supply significantly.

G-REQ 19 The system shall be powered using Power Over Ethernet (POE) that has an output of 52 V and can supply 60 W for each ethernet connection.

3.3. New System Context

This section explains the context of the new system such that it complies with the set goals in section 1.2 and can replace the current design. The data context diagram for the new system is shown in fig. 3.4. The new system (green circle) has to interface with multiple terminators (colored rectangles) that might receive and/or transmit data from/to the new system. The following terminators have been identified that the new

system has to interface with:

1. Web-interface
2. User
3. Cryostat
4. Room-Temperature Amplifier board

The following sections describe these terminators and the requirements they impose on the new system.

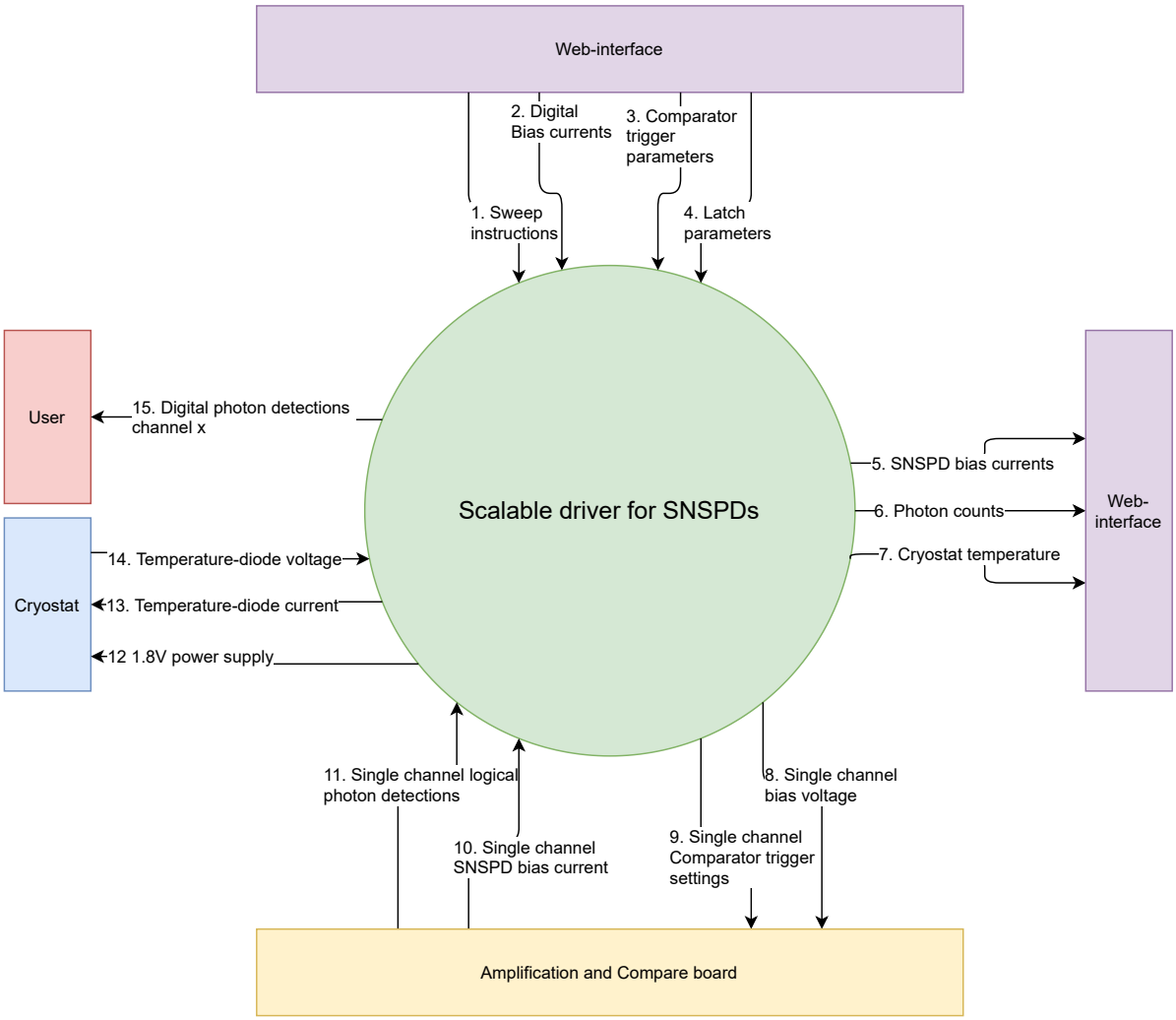
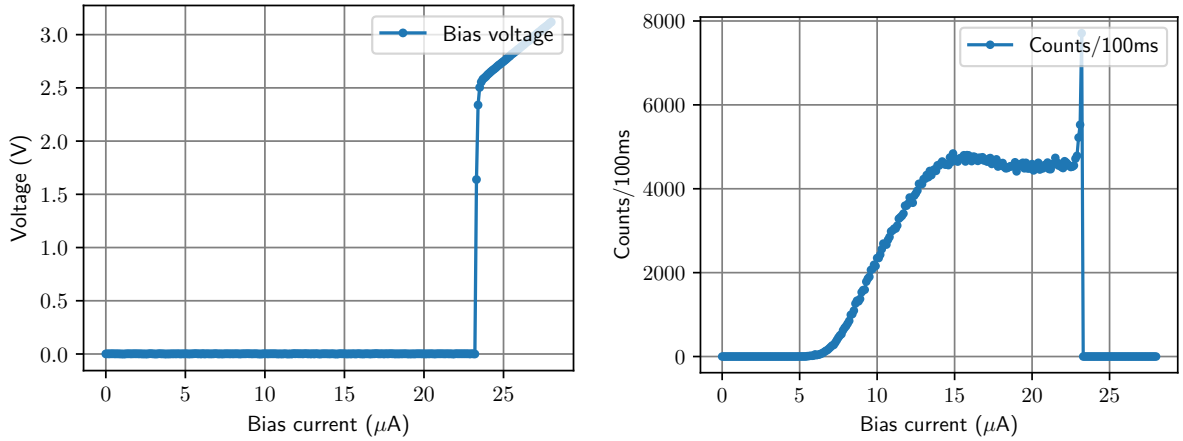


Figure 3.4: Data context diagram.

3.3.1. Web-interface

The “Web-interface” houses the following functionality:

- **SNSPD visualization:**
  Plotting the real-time count rates for all SNSPDs synchronously.
- **SNSPD configuration:**
  The configuration options in the web-interface allows the user to manipulate the bias current, the comparator trigger level and the latch detection parameters for each channel.



(a) (b)

Figure 3.5: I/V and I/Count curve example.

- **SNSPD characterization:**
  Characterization of the SNSPD through the web-interface focuses on two aspects of the detector.
  Firstly, it shows the I/V curve as in fig. 3.5a, showing the critical current before latching from superconducting to resistive state.
  Secondly, the I/Count curve as in fig. 3.5b, showing the bias current to achieve the maximum count rate. This also shows a different aspect of the detector: there is a range in bias currents in which the count rate does not change dramatically. This so-called count-plateau is needed for stable detection efficiency.

G-REQ 10 The system shall be able to synchronize the integration interval and start of the counting for all channels.
G-REQ 11 The system shall be able to configure the channels: setting the bias current, comparator trigger level and latch parameters.
G-REQ 12 The system shall be able to characterize the detectors, sweeping the bias current and measuring the voltage and count rate.

3.3.2. User

The "User" will be able to use to the digitized photon detections. A digitized photon detection interface uses *Low-Voltage Differential Signaling* (LVDS), a photon detection is encoded in the rising and falling edge of the signal. More on this subject in section 5.2.1. This is a feature that opens the possibilities to do for instance combinatorial signal processing of multiple SNSPDs on an FPGA or *Time to Digital Conversion* (TDC). This feature is requested by multiple institutions, one of which is the European Space Association (ESA).

G-REQ 13 The system shall output digitized photon detections based on the LVDS physical interface.

3.3.3. Cryostat

The terminator "Cryostat" holds the SNSPDs and possibly the other circuits as explained in section 2.3 (bridge and/or cryogenic amplifier). Next to that it also contains a temperature diode to verify the temperature of the SNSPDs inside the cryostat. The system must be able to provide a bias current to the temperature diode and read out the voltage over the diode. It must also supply the 1.8 V needed for the optional cryogenic amplification stage. Since the circuit used in the old system works, it does not need any alteration for the new system.

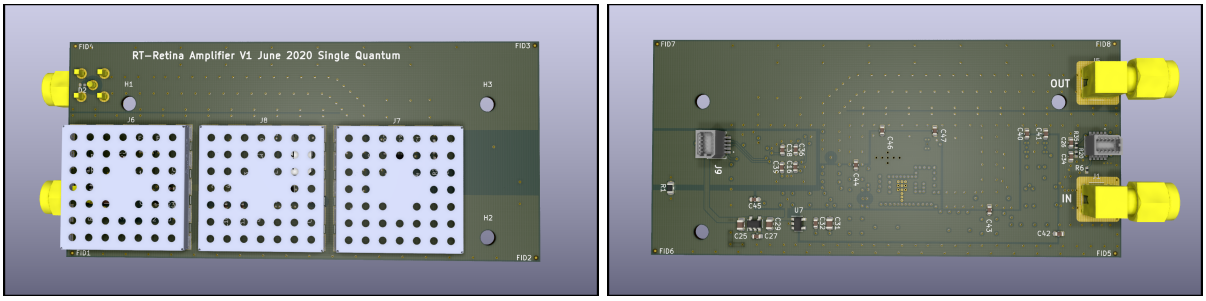
G-REQ 14 The system shall be able to supply the current of the temperature-diode which monitors the temperature in the cryostat with a constant current of 10µA. The design of this circuit will be identical to the circuit currently implemented.
G-REQ 15 The system shall be able to read the temperature-diode voltage and send this to the web-interface.

3.3.4. Room-Temperature Amplifier board

Each detector has a dedicated RT-Amp as shown in figs. 3.6a and 3.6b. This is an analog board has the following functionality:

- It amplifies the SNSPD pulses on the RF-line input, connected to via a SMA connector.
- It supplies the amplified SNSPD pulses on an analog output, connected to via a SMA connector.
- It receives the bias voltage from the system to bias the SNSPD.
- It allows for monitoring the DC-voltage on the RF-line input.
- It receives the comparator trigger level and supplies the comparator output.

This is the implementation for the “Amp” and “Comparator” symbols, and the analog output in fig. 3.2. It needs about 1 W.



(a) Front (b) Bottom

Figure 3.6: Render of the Room-Temperature Amplifier board

Since the system must be able to add channels one by one as stated in **G-REQ 18** and explained in section 3.2.2, the part that must interface with this board is connected to through 2 board-to-board connectors, the grey connectors shown fig. 3.6b.

3.4. Functional Decomposition

This section dissects the new system in separate functions. Dataflow diagram 0 (fig. 3.7) shows which dataflows from/to terminators shown in the Data Context Diagram of fig. 3.4 connect to what functional block. As seen in fig. 3.7 the first functional decomposition step is separating a MCU from the CUs functionality. This is imposed by the requirement on scalability: **G-REQ 18**, allowing the system to add channels at will without depending on hardware and software already in place.

The dataflows with running nummer # are structured as follows:

- #: A flow on the data context diagram level flowing to/from the system to/from the terminators (external flows).
- 1.# or 2.#: A flow on the data flow diagram level that is internal in function 1 (the MCU) or specifically from a function in block 1 to another functional block (internal flows). Likewise flows with 2.# are internal or flow specifically from function 2 (the CU).

The MCU is the intermediary between the web-interface and the CUs, receiving the control commands and sending out the counts for all channels to the web-interface. It supplies the synchronize and clock signals such that all CUs have a synchronized timestamp and their count interval is equal and does not drift with

respect to other CUs. Next to that, it measures the temperature of the cryostat using a temperature diode circuit and also supplies power for the optional cryogenic amplifiers.

The CUs are the direct connection to the RT-Amp terminator. They hold the functionality counting the comparator pulses, supplying the bias current and monitoring the voltage on the RF-line. It sends the needed information to the MCU and receives control signals from the MCU.

Since the CUs interface directly with the RT-Amp, the maximum amount of CUs in each 2U enclosure is limited. The maximum inner width of such an enclosure is about 400 mm, the RT-Amp has a thickness (including RF-cage and components) of about 12 mm and the thickness of the added CU board will be around 10 mm. Therefore, placing a channel every 25 mm and leaving some space for the MCU and possible other connections results in a maximum of 12 channels in each enclosure.

G-REQ 20 Each 2U casing can connect to at most 12 detectors.

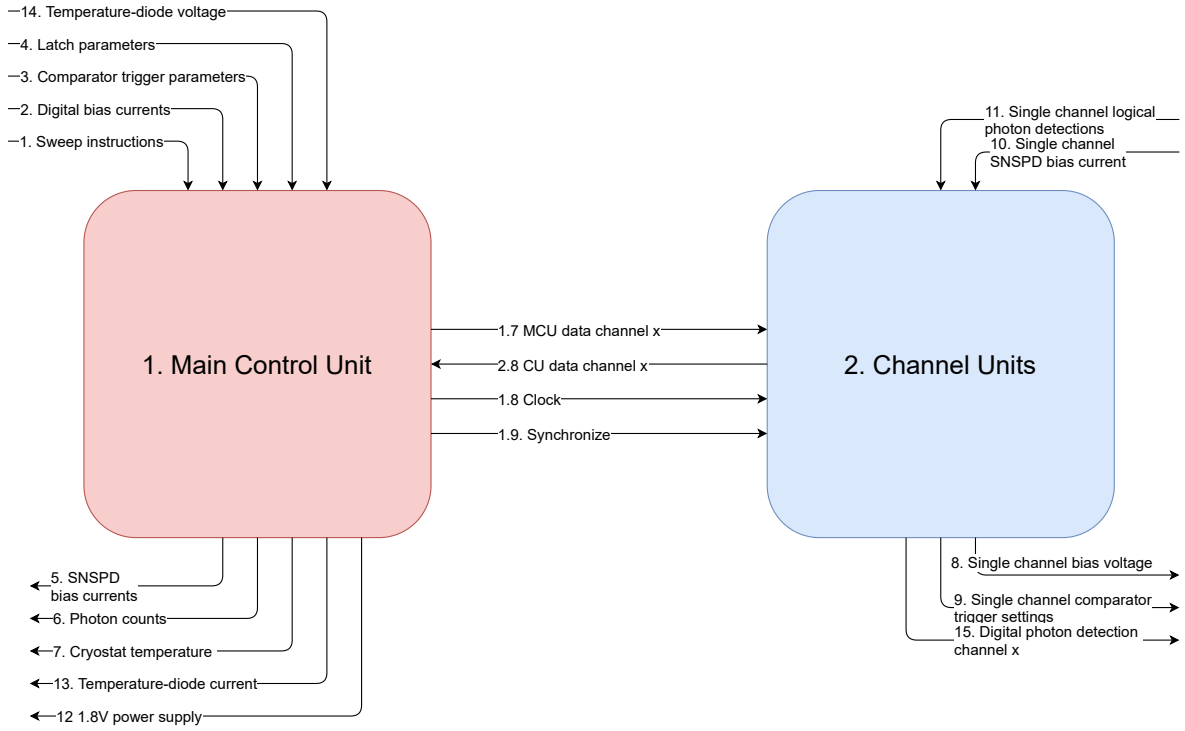


Figure 3.7: Data flow diagram 0.

The following subsections will explain what the functions for both MCU and CUs are and what data flows are used or generated.

3.4.1. Main Control Unit (MCU)

The needed functionality of the MCU are depicted in fig. 3.8. It must be able to execute the following functions:

1.1 **Execute Sweep:** It sends a sweep command to specific CUs. The CU sweeps the bias current over a certain range, incrementing the bias every set integration interval. It sends back the count and monitored voltage on the RF-line at that bias current setting.

1.2 **Determine channels:** Based on control parameters coming from the web-interface the MCU creates a command to update the configuration of a specific CU.

1.3 **Translate cryostat temperature:** This function translates the voltage from the temperature diode to a data package that is sent to the web-interface. It also supplies the current to the temperature diode such that it functions properly.

1.4 **Receive CU data:** This function translates the received data from the CUs to data that can be sent and interpreted by the web-interface.

1.5 **Generate/buffer Clock and Synchronize:** This function supplies the synchronize and clock signals such that all CUs are synchronized, their count interval is equal and does not drift.

1.6 **Generate power for cryogenic amplifier:** This function supplies power to the optional cryogenic amplifiers.

1.7 **Transmit MCU data:** This function translates the control packets from the MCU to the selected CUs.

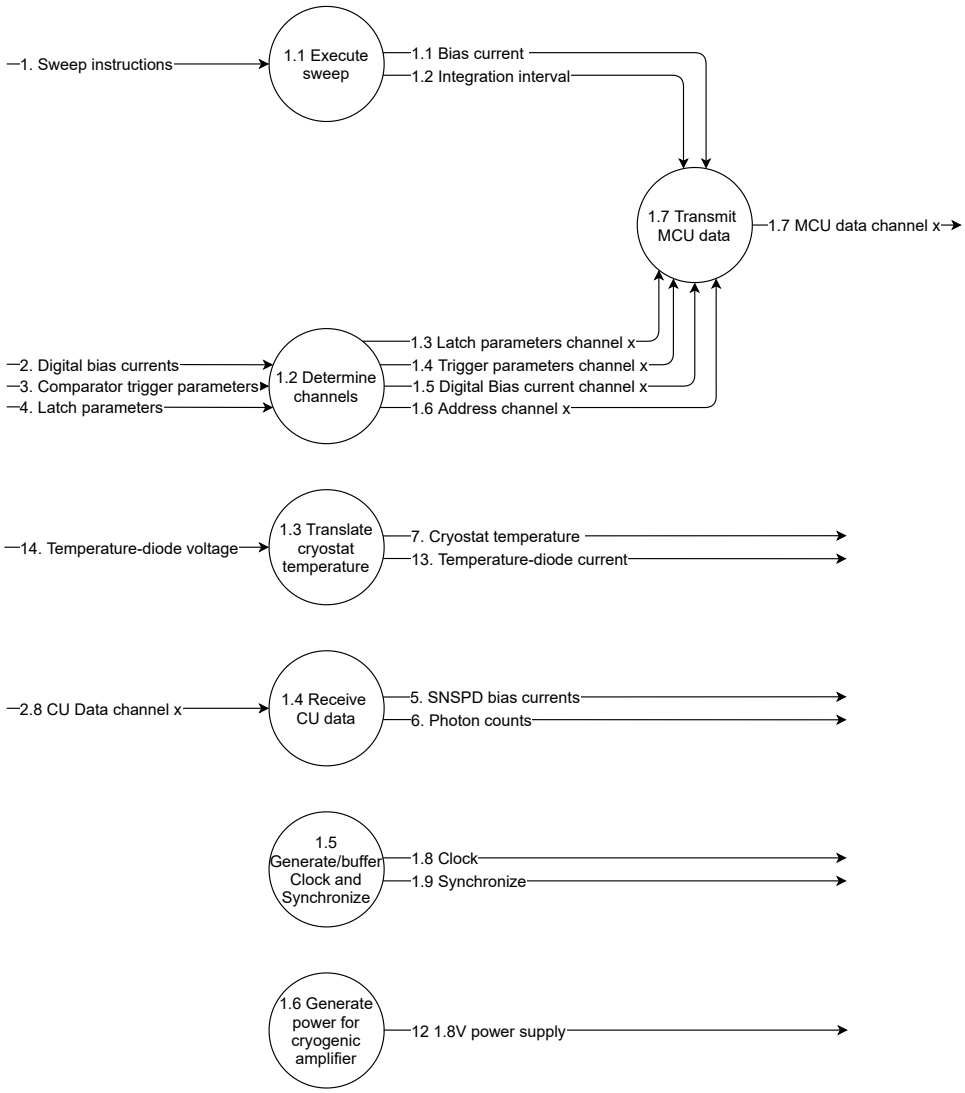


Figure 3.8: Data flow diagram 1.

3.4.2. Channel Unit (CU)

The needed functionality of the CUs are depicted in fig. 3.9. It must be able to execute the following functions:

2.1 **Receive MCU data:** Translates control packets from MCU to instructions for the CU.

2.2 **Adjust comparator settings:** Adjusts the trigger level of the comparator.

2.3 **Adjust SNSPD bias current:** Adjusts the bias current through the detector.

2.4 **Measure SNSPD voltage:** Measures the voltage on the RF-line such that it can detect latching and perform the I/V sweep.

2.5 **Count logical photon detections:** Increments a counter based on the comparator pulses and store the count based on the clock and synchronize signal.

2.6 **Digitize detections:** Converts comparator pulses into digital pulses.

2.7 **Transmit CU data:** Translates the gathered information to data packets that are sent to the MCU.

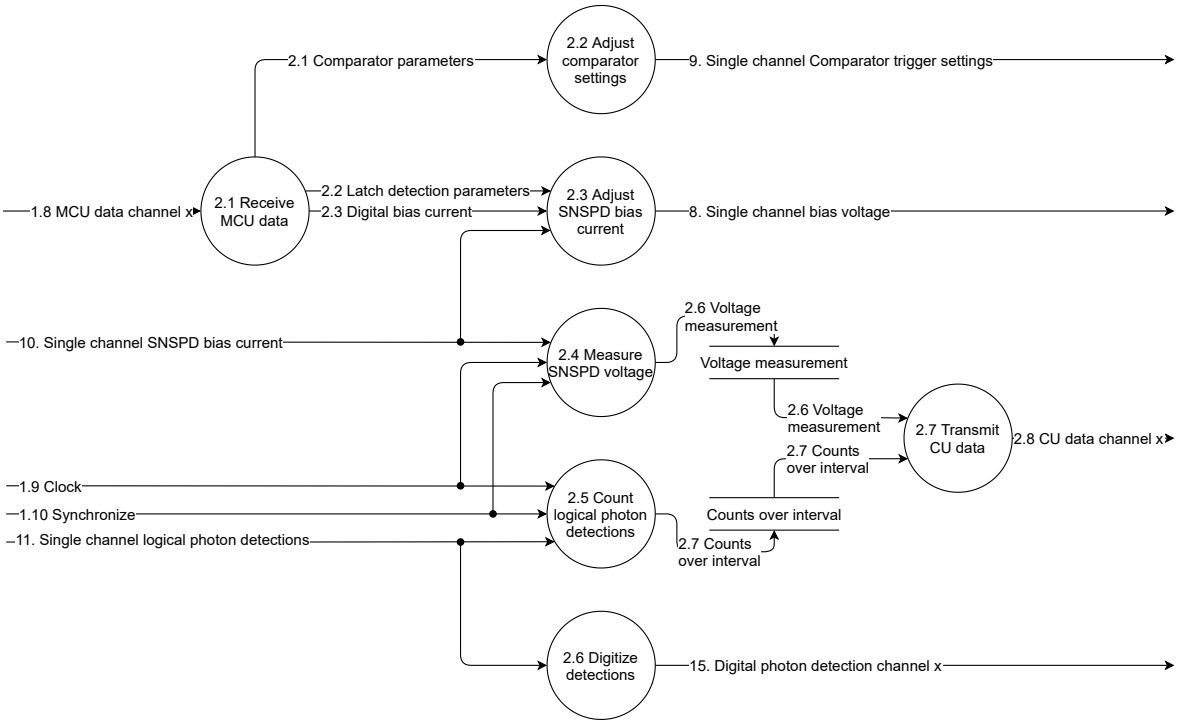


Figure 3.9: Data flow diagram 2.

3.5. Conclusion

The executed analysis has shown that the old system has some limitations and shortcomings that will have to be addressed in the new system design. The system requirements have been drawn up and are summed up in appendix A. These requirements are the foundation for the new design and the design will be verified on these requirements after it has been created.

The key improvements for the new system are compared to the old system in table 3.2.

Table 3.2: Comparison

		Old system	New system
1.	Power consumption per channel	5 W	≤ 3 W
2.	Active quenching	Partially	Yes, with all cryogenic blocks installed
3.	Scalability without reconfiguring HW	×	✓
4.	No dead-time	×	✓
5.	LVDS output of photon detections	×	✓

Based on the functional decomposition, an architecture for the new system will be distilled in the following chapter in which the functionality will be mapped on actual hardware or software. This architecture will be designed in multiple layers of abstraction. For each layer, interfaces connecting the units in that layer will be presented and justified.

4

Architecture

This chapter presents the architecture and gives a technical justification of the interfaces between units that are following from the analysis phase. The architecture is split in three levels. For convenience the three levels are labelled respectively “Super-system”, “12-channel systems” and “Sub-systems”. First, the Super-system is described, which incorporates the scalability to $n \times 12$ channels. It is followed by the explanation of a 12-*channel system*. The Sub-systems in a 12-channel system will be elaborated on in the following chapter.

4.1. Super-system

The Super-system architecture is depicted in fig. 4.1. This figure shows how the scalability of $n \times 12$ channels is created. Depending on the amount of ethernet ports in the POE switch, the amount of channels can be scaled. POE switches, for instance the NETGEAR GS710TUP, holds 8 POE ports that can supply up to 60 W on each port.

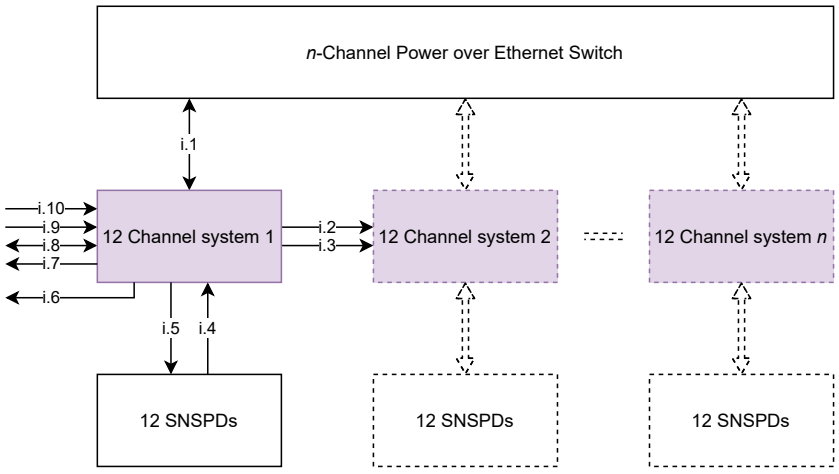


Figure 4.1: Super-system architecture. See fig. 4.2 for the architecture of a 12-channel system.

4.1.1. 12-Channel Systems

A 12-channel system holds all the functionality to control and readout 12 SNSPDs. It can generate or buffer externally supplied clock and synchronization signals. It has 2 outputs for each of the 12 channels which hold their amplified photon detections and digitized photon detections. It can bias and readout the temperature diode in the cryostat.

When 12 or less channels are required, a single system will be connected to a POE switch such that the outside world can connect to the webserver which hosts a web-interface, and the system is powered.

When more than 12 channels are required, the first 12-channel system will become the “master” system which holds the webserver and generates the clock and synchronization signals on interfaces **i.2** and **i.3**.

Additional 12-channel systems are connected to the switch but do not house a webserver or supply/readout the temperature diode. They daisychain interfaces **i.2** and **i.3**. These 12-channel systems are the "slaves" in the super-system.

4.1.2. Interfaces

The interfaces are labeled with a running number #, dependent on the abstraction layer in the architecture:

- **i.#** for the Super-system interfaces. Described below.
- **iG.#** for the internal interfaces of a 12-channel system. Described in section 4.2.4.
- **iM.#** for the internal interfaces of Sub-system: MCU. Described in section 5.1.7.
- **iC.#** for the internal interfaces of Sub-system: CU. Described in section 5.2.7.

i.1 Power Over Ethernet:
This interface is based on company requirement **G-REQ 19**.

- **Functionality:** Supplies 52 V at a maximum of 60 W and dataconnection to the webserver.
- **Physical connection:** CAT-6 cable and RJ45 sockets.

i.2 Clock out and **i.10** Clock in:
These interfaces, together with interfaces **i.3** and **i.9** are the implementation for requirement **G-REQ 10**, synchronizing the integration interval for all systems.

- **Functionality:** A 10 MHz single ended 3.3 V output/input that connects clock interfaces of subsequent 12-channel systems.
- **Physical connection:** 50 Ω coaxial cable and SMA connector.

This implementation for a distributed clock and synchronize function was favored over for example the Precision Time Protocol (IEEE 1588-2008) that is ran over Ethernet.

It is favored because of its simplicity. The requirement for the system is that it needs to be sure that the integration interval is equal for all channels, eliminating clock drift. Clock skew is not an issue just as long as the clock is phase locked in each subsequent 12-channel system and the propagation delay of **i.3** is shorter than one clock period. Propagation time of a pulse through a copper wire is about 200 000 km/s, resulting in a propagation time over a 3 meter wire of 15 ns which is $\frac{3}{20}$ of the clock period. 3 meter is a rough estimation for total length of cable needed to connect to a 2 meter height 19 inch rack full of 12-channel systems.

Either an external 10 MHz oscillator can be attached to the input of the first 12-channel system such that the integration interval is accurately set to 10 ms or the first 12-channel system can generate the 10 MHz when a lower accuracy is allowed.

i.3 Sync out and **i.9** Sync in:
These interfaces, together with interfaces **i.2** and **i.10** are the implementation for requirement **G-REQ 10**, synchronizing the integration interval for all systems.

- **Functionality:** A synchronization pulse that is normally high, 3.3 V, and low, 0 V, for 100 ms when a synchronization for all channels is initiated by the master 12-channel system.
- **Physical connection:** 50 Ω coaxial cable and SMA connector.

It eliminates the need to add actual timestamps to the count data. Asserting this interface (active low) resets a sequence counter (which increments each integration interval with wrap around the maximum) on all channels. This way the webserver can easily construct a congruent plot for all channels based on its sequence number.

This signal is also used at initialization time of the complete system. When a master and multiple slaves are connected, each subsequent slave toggles its sync output of this signal once more with respect to the amount of toggles it detected on the sync input. This way each slave can fix its hardware address based on the position in the daisychain.

i.4 Photon detections:

- **Functionality:** Voltage pulses coming from the biased SNSPDs.
- **Physical connection:** 50 Ω coaxial cable and SMA connector.

This is a fixed interface by SQ.

i.5 Bias currents:

- **Functionality:** Direct current, biasing individual SNSPDs such that voltage pulses can occur when a photon hits the nanowire. The currents can be either positive or negative and range between 5 µA and 100 µA.
- **Physical connection:** Shares the same physical interface as **i.4**.

i.6 Amplified photon detections:

- **Functionality:** After amplification, the photon detections are directly routed to an output.
- **Physical connection:** 50 Ω coaxial cable and SMA connector.

This is a fixed interface by SQ.

i.7 Digital photon detections:

- **Functionality:** Up to 12 LVDS interfaces, photon detections are encoded in both rising and falling edge of this signal. This is explained in section 5.2.1.
- **Physical connection:** A *Peripheral Component Interconnect Express* (PCIe) x1 connector.

The LVDS protocol was chosen since it is requested by SQ customers, stated in **G-REQ 13** and because: "it is the most common differential signaling interface. The low power consumption, minimal EMI, and excellent noise immunity are the features that have made LVDS an interface of choice for many applications. In addition, the LVDS wide-input common mode makes LVDS devices easy to interoperate with other differential signaling technologies."[5].

i.8 Temperature diode current and voltage readout:

- **Functionality:** The temperature diode in the cryostat is biased at 10 µA its voltage read out by the master 12-channel system.
- **Physical connection:** 4 pins on a 48-pin connector.

This is a fixed interface by SQ.

4.2. 12-Channel System

The 12-channel system architecture is depicted in fig. 4.2. This figure shows how the scalability of 1 to 12 channels is created. It comprises the Sub-systems Main Control Unit, the Backplane, 1 to 12 Channel Units and Room-Temperature Amplifier boards and their interconnections. If it is the only 12-channel system or if it is the "master" system, it also contains the webserver. The following sections will briefly explain the functionality for each Sub-system, it will state the design decisions and describes the internal interfaces labeled **iG.#**. A more thorough explanation of each Sub-system can be found in chapter 5.

4.2.1. Main Control Unit

The MCU incorporates the functions described in section 3.4.1. It is mainly a translator between the ethernet connection and the bus interface connecting the 12 CUs. It also acts as a buffer or generator for the clock and sync signals. This depends whether it is the the MCU in the master system or in a slave system.

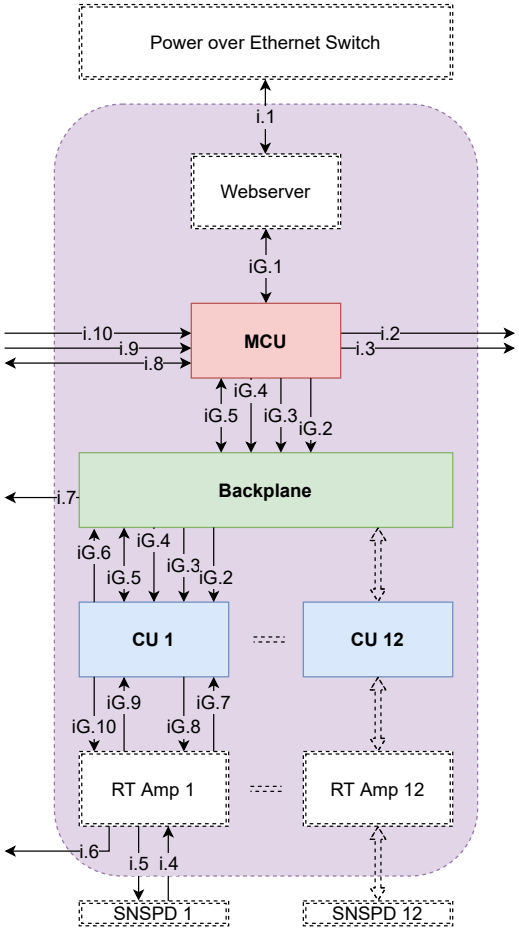


Figure 4.2: The 12-channel system architecture, part of super system shown in fig. 4.1.

4.2.2. Backplane

The backplane is the passive interconnection subsystem that allows connecting 12 CUs to the MCU and also provides the power distribution as shown in fig. 4.3. The physical interface between the backplane and either MCU or CU will be a PCIe x1 connector. This connector was chosen since:

- It is designed for 50 Ω high-frequency signal lines such as the bus interface and **i.7**.
- It reduces the amount of connectors needed, since the CU and MCU will have PCB fingers.
- It allows for easy 90° physical angle stacking of PCBs.

4.2.3. Channel Units

The CU incorporates the functions described in section 3.4.2. The design decisions for the CU architecture are stated below:

- **Integration Interval:** The distributed 10 MHz clock, described at item **iG.4** is used by the CUs to generate an interrupt every 10 ms that triggers the photon counter to store its count and reset its counter to 0. This way all CUs integrate their photon detections over 10 ms creating a regular data stream coming from all CUs. If a different integration interval is requested by the user of the system, in x-multiples of 10 ms, the webserver sums the counts from x messages from that CU with successive sequence numbers before plotting the countrate.
- **Data rate:** The requirement **G-REQ 5** states that each channel must be able to count up to a rate of 1 GHz, therefore:

– The count of photon detections over 10 ms is maximally 10^7. This means that to store each count we need at most:

$$\log_2\left(10^7\right) \approx 23.25 \Rightarrow 24\,\text{bit} \tag{4.1}$$

Since the webserver needs to know what the sequence of count data is, a 16 bit sequence number is added to each count. The data packet containing a count from a specific channel must contain the unique identifier, or address, from this channel. Stated in **G-REQ 17** up to 12 channels may be added to a single system so at least 4 bit must be reserved for this identifier.
To give the MCU some additional information about the received data we've assumed an 8 bit state parameter field which indicates what state of the CU.

$$24 + 16 + 4 + 8 = 52\,\text{bit} \tag{4.2}$$

– The CUs shall send their settings to the MCU each integration interval. This allows the MCU to update the webserver's information on each CUs.

– The datasize for the monitored voltage on the RF-line will be at most 24 bit.

– The datasize to set the bias current will be at most 24 bit.

– The datasize to set the comparator trigger level will be at most 16 bit.

– Based on **G-REQ 3**, **G-REQ 4** and **G-REQ 11** multiple parameters must be able to be set such that the CU knows when it has to quench the SNSPD. These parameters are:

◇ V_{latch} : 16 bit: A voltage which helps the active quenching functionality to detect a latched SNSPD.

◇ t_{latch} : 16 bit: The time that the bias current should be actively set to 0 such that the SNSPD can return to superconducting state. In multiples of 10 ms

◇ f_{lower} : 16 bit: A lower frequency bound, as a redundancy for the resistive state latch event. Most often set at a value ~ 0.01 Hz or lower.

◇ f_{upper} : 16 bit: An upper frequency bound that detects a detector in oscillation.

◇ R_{bs} : 16 bit: The series bridge resistor. $20\,\Omega \leq R_{bs} \leq 200\,\Omega$.

◇ R_{bp} : 16 bit: The parallel bridge resistor. $20\,\Omega \leq R_{bp} \leq 200\,\Omega$.

◇ R_c : 16 bit: The bypass resistor on the cryogenic amplifier. $\approx 70\,\text{k}\Omega$.

– The previous summed up data will be sent to the MCU every 10 ms such that the MCU, and subsequently the webserver, continuously knows the settings on each CU. For a data packet from each CU we need:

$$52 + 24 + 24 + 16 + 96 = 212\,\text{bit} \approx 27\,\text{B} \tag{4.3}$$

Sending a datapacket each 10 ms results in a minimal data-rate requirement for the bus connecting the CUs to the MCU of 21.2 kbit/s. When all channels 12 are connected to the same bus the data rate becomes 254.4 kbit/s.

4.2.4. Interfaces

The internal interfaces **iG.#** for a 12-channel system are explained below. They are depicted in fig. 4.2. The **i.#** interfaces are described in section 4.1.2.

iG.1 Ethernet:

- **Functionality:** The data connection to the webserver or POE switch. The data packets are formatted in JSON. See appendix B.1 for the specification of the JSON datapacket.
- **Physical connection:** CAT-6 cable and RJ45 sockets.

This is a direct implementation of the requirement **G-REQ 8**. The JSON dataformat was chosen since the format is easily generated and parsed by a microcontroller and Python which is used for the webserver.

iG.2 Reset:

- **Functionality:** Hardwired reset that resets the software of the CUs. Normally high 3.3 V and low 0 V for 100 ms to do a reset.
- **Physical connection:** 1 pin on PCIe x1 connectors for all CUs and the MCU.

iG.3 Sync:

- **Functionality:** A synchronization pulse that is normally high: 3.3 V, and asserted low: 0 V, for 100 ms when a synchronization for all channels is initiated by the MCU in the master 12-channel system. Distributed to all CUs, buffered by the MCUs in slave systems.
- **Physical connection:** 1 pin on PCIe x1 connectors for all CUs and the MCU.

iG.4 Distributed Clock:

- **Functionality:** A 10 MHz single ended 3.3 V clock. Distributed to all CUs buffered by the MCU.
- **Physical connection:** 1 pin on PCIe x1 connectors for all CUs and the MCU.

iG.5 CAN-FD:

- **Functionality:** A two wire CAN-FD bus interface that handles all the datapackets coming from the CUs and the control packets coming from the MCU.
- **Physical connection:** 2 pins on PCIe x1 connectors for all CUs and the MCU.

The bus interface was chosen early in the design process. At that moment it was not clear in what way and how many CUs would be connected to the MCU.

Several bus oriented protocols have been considered that would accomodate the datarate requirement stated in section 4.2.3 and would allow 12 CUs to connect to it through daisychaining instead of a peer-to-peer bus. This way the hardware demands on the MCU would be less strict. Such bus interfaces are: *Serial Peripheral Interface* (SPI) was an option but was discarded since the arbitration for reading out

Table 4.1: Bus specifications

Type	Data rate	Bus application
Serial Peripheral Interface (SPI)	up to 10 Mbit/s	On PCB, general peripheral interface
CAN	up to 1 Mbit/s	Cabled or on PCB, automotive
CAN-FD	up to 5 Mbit/s	Cabled or on PCB, automotive
FireWire	up to 3200 Mbit/s	Cabled, general computing

all the CUs would have to be manually programmed on the MCU: selecting/deselecting the slave-select pins as the data from the CUs would become available and be on time to readout all CUs before the next 10 ms integration interval had passed. In addition the slave select wires would have to be connected in a tree like fashion from the MCU to all CUs, removing ability to daisychain.

Firewire was considered but also discarded since its specified datarate is way above what is needed. In addition it seems industry is has moved away from this interface, according to [11], creating the possibility that compatible components become less and less available in the future.

Therefore the preferred interface was CAN or CAN-FD (Flexible Data-rate). The connection could be either cabled or through a PCB and the data rate could accommodate for more than 12 CUs. Arbitration is done by a dedicated CAN-FD control-peripheral on each node. CAN-FD allows for sending up to 64 bytes of data in each message at a higher rate than classical CAN which can only send 8 byte each message. Since the messages that have to be sent by each CU contain around 27 byte, the flexibility of sending all information in 1 message is preferred. Therefore, CAN-FD has been chosen as the bus interface connecting the 12 CUs to the MCU.

All nodes on the CAN-FD bus receive all CAN-FD messages but filters can be configured in the peripheral that filter the messages based on the CAN-ID field in the message. This ID field can be either 11 bit (normal) or 29 bit (extended ID). Since the MCU must be able to broadcast commands to all CUs but also send commands to individual CUs, 1 bit is needed to address each CU, summing up to 12 bit. Another 4 bit in the CAN-ID field is required such that the MCU can configure its filter such that it only

Table 4.2: CAN-ID specification

CU#	From MCU to CU#	From CU# to MCU
0	$0x0001$	$0x1000$
1	$0x0002$	$0x2000$
2	$0x0004$	$0x3000$
3	$0x0008$	$0x4000$
4	$0x0010$	$0x5000$
5	$0x0020$	$0x6000$
6	$0x0040$	$0x7000$
7	$0x0080$	$0x8000$
8	$0x0100$	$0x9000$
9	$0x0200$	$0xA000$
10	$0x0400$	$0xB000$
11	$0x0800$	$0xC000$
All	$0x0FFF$	–

accepts the CAN-FD messages from the CUs. Therefore, the extended CAN-ID field is used. The addressing/filtering as shown in table 4.2 is implemented in the system. As can be seen in table 4.2 the CAN-ID for each CU uses a separate bit position. This means each CU can initiate its message filters based on its own address (0-11) and will reject (mask) all messages except when a 1 is written on bit position "address". For the MCU, it is straightforward to create a specific message for the designated CUs (setting bits to 1 on their respective position) or broadcast a message to all CUs (set bits $11-0$ to 1).

Filtering for the MCU is also straightforward since it rejects all CAN-ID's for bit position 0 through 11 and allows the messages in bit positions 12 through 15 which are the messages from the CUs.

iG.6 Digital photon detections:

- **Functionality:** A LVDS interface that holds the photon detection information in both its rising and falling edge.
- **Physical connection:** From 2 pins on a PCIe x1 connectors on each of the CUs to a single PCIe x1 connector on the backplane.

iG.7 Comparator output:

- **Functionality:** The comparator output uses CML. When high, it means a photon detection has occured.
- **Physical connection:** 2 pins on a 10-pin Molex board to board connector connecting the RT-Amp to the CU.

iG.8 Comparator trigger level:

- **Functionality:** A voltage between 0 V and 2.25 V that sets the trigger level of the comparator.
- **Physical connection:** 1 pin on a 10-pin Molex board to board connector connecting the RT-Amp to the CU.

iG.9 Monitor voltage:

- **Functionality:** Measured voltage over the bias circuit in the RT-Amp used to determine the state of the SNSPD (latched/unlatched).
- **Physical connection:** 2 pins on a 10-pin Molex board to board connector connecting the RT-Amp to the CU.

iG.10 Bias current:

- **Functionality:** Direct current, biasing individual SNSPDs such that voltage pulses can occur when a photon hits the nanowire. The currents can be either positive or negative and range between 5 µA and 100 µA.

- **Physical connection:** 2 pins on a 10-pin Molex board to board connector connecting the RT-Amp to the CU.

4.3. Power Supply Unit

The *Power Supply Unit* (PSU) architecture is shown in fig. 4.3. Power is supplied over the ethernet cable and is specified to supply at most 60 W at 52 V. The PSU will be designed to handle this power. For this thesis a POE splitter has been bought that splits the power from data and converts the voltage to 24 V. This is used as an input to the PSU.

The RT-Amp needs about 1 W and needs a supply voltage of both 6.5 V for the amplification stages and 3.3 V for the comparator. The 6.5 V is converted to 5 V on the RT-Amp PCB.

The power budget for each CU has been specified at 2 W. The CUs need a bipolar supply of ±15 V, since they need to supply the bias currents conform to **G-REQ 1**. Since the RT-Amp converts its 6.5 V input voltage (which is routed through the CU) to 5 V it would be convenient that the CU converts this 6.5 V to 5 V on the CU board to supply the CAN-FD transceiver and possibly other *Integrated Circuit*s (ICs). This way reducing the amount of supply lines coming from the PSU by 1. 3.3 V is required for all other ICs, such as the microcontroller and counter circuits.

The MCU must be able to supply 1.8 V such that optional cryogenic amplifiers can be powered. The MCU like the CU needs both 6.5 V to be converted to 5 V used for the CAN-FD transceiver and 3.3 V for all other ICs. The PSU connects its power rails to the backplane using a 6-pin Molex connector. The MCU and CUs connect

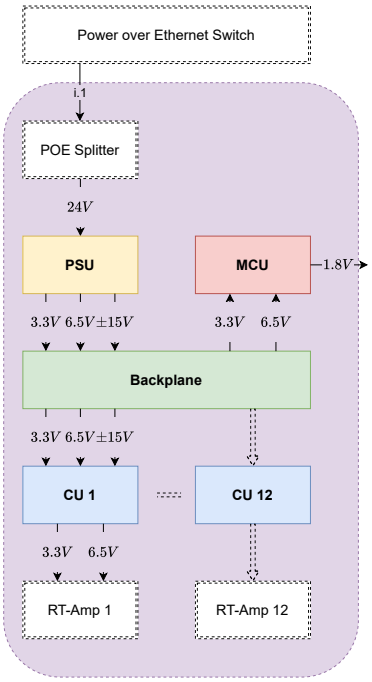


Figure 4.3: PSU Architecture.

to their supply voltages via pins on the PCIe x1 connector. The RT-Amp connects to its supply voltages via the 10-pin Molex board to board connectors.

4.4. Conclusion

The architecture for both the Super-system and 12-channel system has been designed. This architecture allows the system to be scalable, virtually without limit. As a by-product, it will probably reduce assembly time since all connections within a 12-channel system are done through a backplane PCB.

This architecture paves the way for the next chapter in which detailed designs for all Sub-systems are described.

5

Design and implementation

This chapter describes the design decisions on the individual units.

One main decision will be explained directly since it is core for both the MCU and the CU, i.e. the choice of the microcontroller. It has to be a microcontroller that can handle the following functions:

- Ethernet MAC peripheral.
- CAN-FD controller.
- 3 counters or more that can count both rising and falling edges at a frequency of at least 50 MHz.
- Handle 2 or more SPI peripherals simultaneously such that at least 2 ICs with different SPI configurations may be addressed without continuously reconfiguring the peripheral.
- SysTick such that a FreeRTOS [2] can be used. This might be useful when a baremetal firmware approach with interrupts does not fulfill its functionality. As will be seen further on in the chapter, this functionality was not needed.

All the main microcontroller manufacturers, such as TI, STM, NXP, and Microchip, have a microcontroller that complies with above-mentioned specifications and are all within the same price range of about €6.5. Since this is the case, we can get more picky on the manufacturer's global position such that the supply chain of this component is not hampered by politics or regional conflicts. SQ sees a risk in integrating components coming from the USA to their products since it is becoming more and more a protectionist country. This is why TI and Microchip were out of scope. STM is a Swiss company and NXP a Dutch company at it roots. Since SQ is a Dutch company it was found suitable to buy ICs from a Dutch-originated company such as NXP. So the NXP microcontroller was chosen: LPC54618.

This microcontroller has a development board: the OM13094 with a CAN-FD shield such that fast testing of the bus interface could be executed. For both the MCU and the CU, the LPC54618 will be used. This reduces the development time, since the developer only needs to fully understand one microcontroller to program a piece of software and configure its peripherals. Furthermore, this might reduce costs since the microcontroller can be bought in bulk capacity.

5.1. Main Control Unit

The design for the MCU is shown in fig. 5.1. It was decided that this part can be implemented on the development board to prove the functionality of the prototype of the new system. This because the main functionality of the MCU is in the software domain and the development board can accommodate the needed hardware. In the following sections, each of the functional blocks in fig. 5.1 will be explained. The running number in the section headers correspond to the numbers in the functional blocks.

5.1.1. Ethernet

The development board OM13094 incorporates a 10/100 Mbit/s PHY interface and has a RJ45 connector such that it can communicate with the webserver.

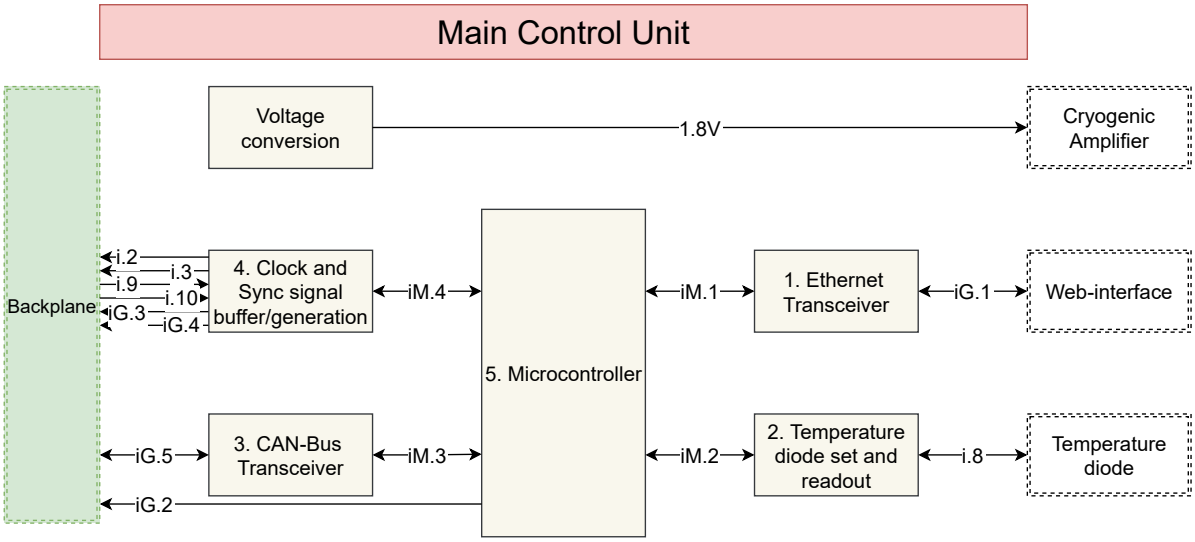


Figure 5.1: Main Control Unit architecture.

5.1.2. Temperature diode set and readout

As described in **G-REQ 14**, the circuit that implements the setting and readout of the temperature diode will be copied from the old system since it works properly and does not need adjustment. For this thesis it is not implemented since the MCU is implemented on the development board. The circuit as implemented in the old system is shown in fig. 5.2. Two instrumentation amplifiers are used. One as a feedback loop for the current supplied to the diode from the DAC and one that functions as a readout circuit for the voltage over the diode, which is proportional to the temperature. In future work, a custom PCB will be designed for the MCU which will house this circuit.

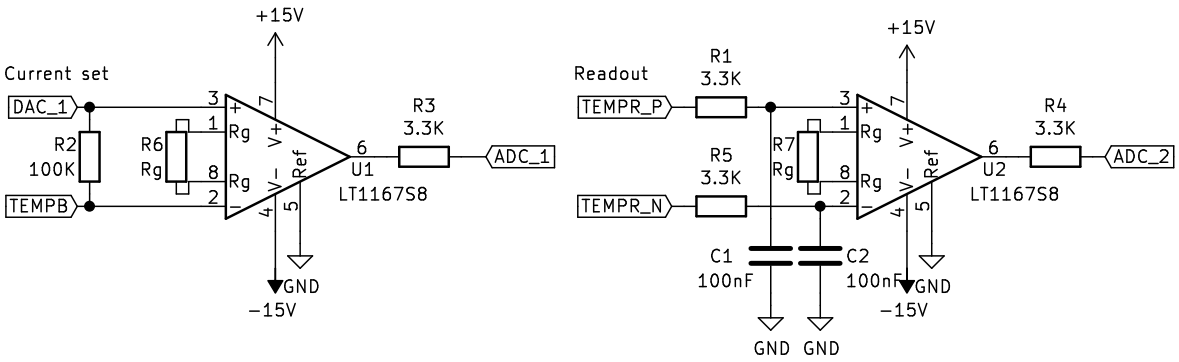


Figure 5.2: Temperature diode set and readout circuit. The left *Instrumentation Amplifier* circuit measures the voltage induced over a 100 kΩ resistor by the DAC (DAC_1) which supplies the bias current for the diode on pin TEMPB. The right *Instrumentation Amplifier* measures the voltage over the diode which is proportional to the temperature at pins TEMPR_P and TEMPR_N. The resistor R_g is to set the gain for the amplifiers.

5.1.3. CAN-bus Transceiver

The shield that came with the OM13094 development board incorporates the CAN-FD transceiver circuit featuring a TJA1057 IC and has a D-SUB9 connector that can be used to communicate with the backplane CAN-FD lines.

5.1.4. Clock and sync signal buffer/generation

The super-system interfaces that are connected to this functional block: **i.2, i.3, i.9** and **i.10** are either input or output for the synchronize signal or the distributed clock signal. Either an external 10 MHz oscillator can be attached to the input of the "master" 12-channel system such that the integration interval for all CU is accurately set to 10 ms or the "master" 12-channel system can generate the 10 MHz when a lower accuracy is allowed.

In either case, a buffer that supplies this signal to all CUs through **iG.4** is required such that the 12 CUs sampling the clock do not directly draw current from the clock source. This prevents a possible issue when multiple systems are connected to the same clock source. It might be necessary to add a *Phase-Locked Loop* (PLL) to this circuit such that any delay introduced by the buffer is mitigated.

For now, the circuit for clock synchronization and the sync buffer have not been designed, as these would become necessary only when multiple 12-channel systems are integrated. Integration of multiple 12-channel systems is out of scope for this thesis.

The generation of the clock will be done with a counter on the MCU. The sync signal will be a *General Purpose Input-Output* (GPIO) pin that is toggled if synchronization is sent as a command by the web-interface.

5.1.5. Microcontroller

As stated at the beginning of this chapter, the LPC54618 microcontroller is used on its development board OM13094. The software will be explained in section 5.2.8.

5.1.6. Software

The global flow diagram for the MCU is shown in fig. 5.3. Each initialized CU sends a CAN-FD message every 10 ms. The contents of the CAN messages coming from the CUs is shown in fig. B.3. The MCU aggregates these messages into a *JavaScript Object Notation* (JSON) formatted ethernet packet which is sent to the webserver. See appendix B.1 for the specification of the JSON datapackets that are sent to the web-interface.

Occasionally the web-interface could sent a JSON datapacket to the MCU requesting for instance an adjustment in bias currents on specific CUs or sending a "sweep" command.

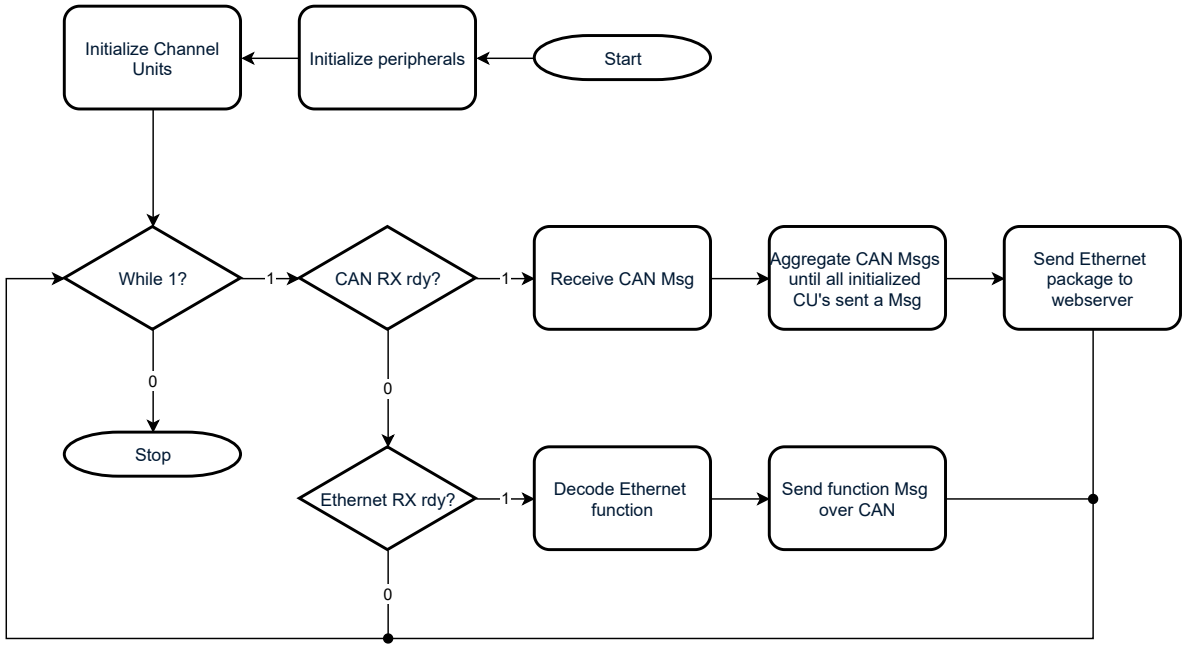


Figure 5.3: Main Control Unit Software design.

5.1.7. Interfaces

The internal MCU interfaces are specified with **iM.#**. The interfaces (**i.#** and **iG.#**) are explained in respectively sections 4.1.2 and 4.2.4.

iM.1 This is the RMII (*Reduced Media-Independent Interface*) or MII (*Media-Independent Interface*) between the PHY chip and the MAC layer peripheral in the microcontroller.

iM.2 SPI for the communication between the functions: 2. “Set comparator trigger level” and 3. “Set bias current and latch detection”.

iM.3 This is the interface between the CAN-FD transceiver and CAN-FD controller on the microcontroller.

iM.4 This interface is used by the master 12-channel system that pushes its 10 MHz clock and sync signal to slave 12-channel systems. Its description can be found in 5.1.4.

5.2. Channel Unit

The design for the CU is shown in fig. 5.4. In the following sections, each of the functional blocks in fig. 5.4 will be elaborated on. The resulting PCB is shown in fig. 5.5. A larger image is depicted in figs. D.1 and D.2. The schematics for the final design of the CU are shown in appendix C.1.

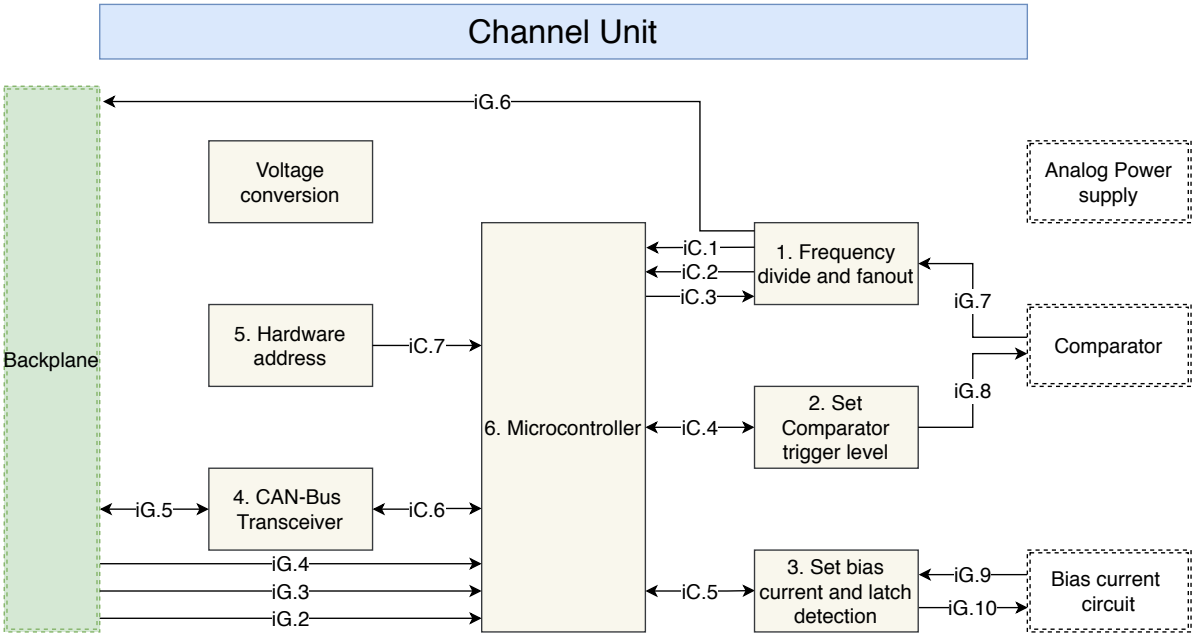
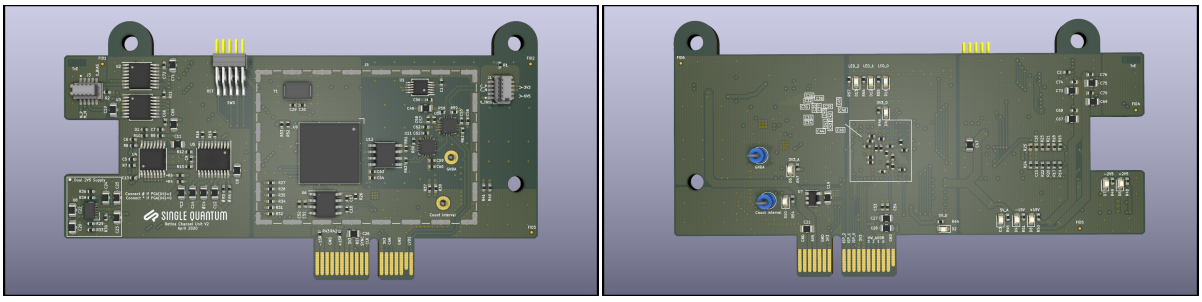


Figure 5.4: Channel Unit architecture.



(a) Front (b) Back

Figure 5.5: Channel Unit PCB render.

5.2.1. Frequency divider and fanout

The output from the comparator is routed to this functional block through **iG.7**. In the worst case scenario, the signal coming from this comparator has a frequency of 1 GHz with a minimal pulse width of 100 ps, as stated in **G-REQ 5**. To be able to count at this detection rate without dead-time and to keep the power demand within bounds, 2 options were considered that would implement **G-REQ 5**, **G-REQ 9** and **G-REQ 7**.

1. The first option is to find a dedicated IC that can convert this frequency and pulse width to a digital format, without dead-time and at a lower power usage than the currently used IC. A thorough browse through the well-known chip manufacturers showed that multiple high frequency counters are available, but all very power hungry and none with integrated digital electronics to overcome the dead-time.

2. The second option is to shape the comparator output pulse to a frequency and pulse width that can be counted by the internal counters in the LPC54618 microcontroller. These internal counters can count both rising and falling edge transitions at a maximum input frequency of f_{clk} since they sample the counter input every rising edge of the clock. The LPC54618 has a maximum f_{clk} of 180 MHz resulting in a theoretical maximum counting frequency of 180 MHz. A frequency division circuit has to be designed that can at least divide the frequency by 6 to accomodate the maximum 1 GHz count rate.

   There are two problems to solve with this approach:

   (a) The system must be able to count precisely with an error of ± 1 count for up to 50 MHz detection rate. Once the frequency division ratio r is set, its precision is automatically reduced to $\pm r$.

   (b) When r is at a fixed value and the photon detection frequency at the input of the counter exceeds the maximum 180 MHz, software cannot verify if the counted detections is equal to the actual detections. Since the input of the counter is switched too fast to count all detections, the counted data is invalid.

   Luckily the LPC54618 microcontroller has multiple counters that can count both rising and falling edge at a rate of maximally 180 MHz. Using a fanout circuit that feeds 2 counters on the LPC54618, one with the comparator output divided by 2 such that all detections are counted, and one that receives the comparator output with a higher division ratio r, such that high frequency counting (higher than 180 MHz) is accounted for but with a lowered precision. The software decides which of the 2 counts will be sent to the MCU.

   Lastly, the "Could have" requirement **G-REQ 13** requires that all photon detections are digitized in LVDS format. This can be implemented by fanning out a divide-by-2 version of the comparator output.

A way to shape the comparator output pulse is by using JK-*Flip-Flop*s (FFs) with its J and K inputs set high and its clock input connected to the comparator output such that it toggles its output: ($Q_n = \overline{Q_{n-1}}$), every time the comparator signals a detection. This way the frequency is divided by 2^x in which x is the amount of cascaded FFs, lengthening the pulse-width such that it can be counted by the microcontroller.

An example showing the steps from amplified voltage pulses to a divide-by-4 comparator output is shown in fig. 5.6. The following enumeration describes each subplot, 1 being the top graph, 4 being the bottom graph. Time is an arbitrary value in this example. The amplitude is normalized.

1. Shows amplified photon detections as voltage pulses coming from a SNSPD and the trigger level at which the comparator switches its output.

2. Shows the comparator output and in red the counter clock. This graph shows that none of these pulses will be counted since the hold time of the pulses is shorter than a clock-period.

3. Shows the comparator output divided by 2 and in red again the counter clock. This graph shows that the first 2 photon detections will not be counted since again this pulse is shorter than a clock-period. The other photon detections are counted properly.

4. Shows the comparator output divided by 4 and now in green the counter clock since it can count all photon detections.

An integrated circuit that has a selectable division ratio and a fanout to 3 outputs is the SY89873L. Its block diagram shown in fig. 5.7 is reprinted from its datasheet. It has the following specifications:

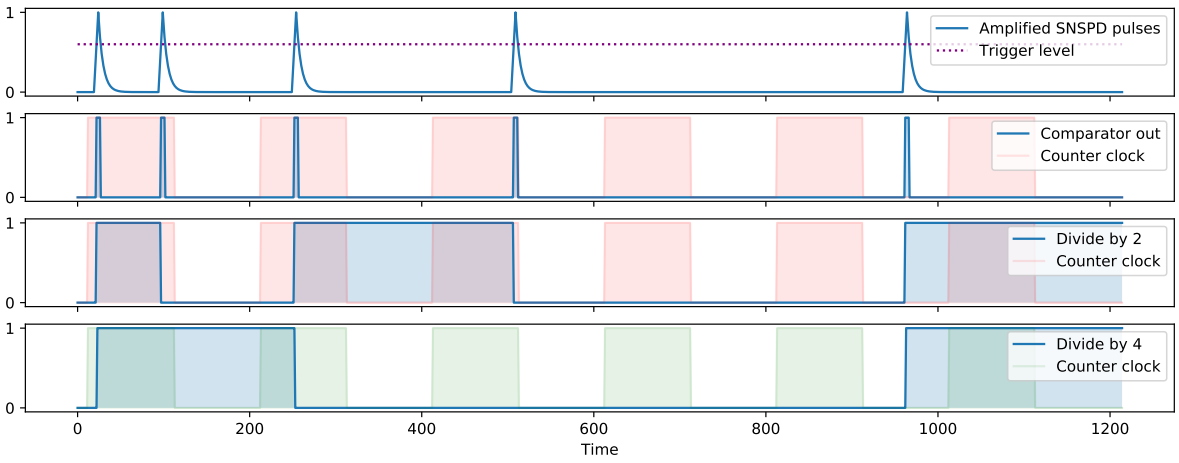


Figure 5.6: Frequency Division.

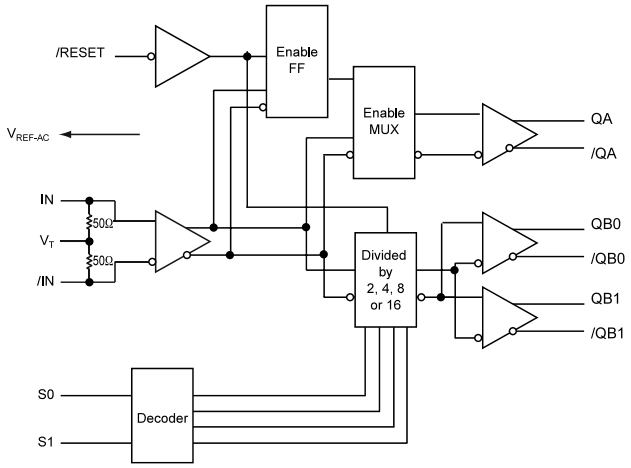


Figure 5.7: SY89873L Block Diagram.

- It accepts CML input from the comparator
- In experiments it has been shown that it can properly divide frequencies up to at least 1.4 GHz coming from the comparator.
- It can divide the input frequency by 2, 4, 8, or 16 times.
- It has fanout capabilities, one straight through input to output (QA), and 2 copies of the divided input ($QB0$ and $QB1$). All outputs are matched in delay.
- Its outputs are LVDS, reducing the power demands with respect to CML or ECL outputs.

The final design is shown in fig. 5.8. Two SY89873L are cascaded, for the first IC both $QB0$ and $QB1$ outputs are used and its division ratio is fixed to 2. One output is routed directly to the PCIe x1 connector on the backplane in compliance with **G-REQ 13**, the other output is connected to the input of the second IC. Two counters on the microcontroller which are configured to count both rising and falling edges are connected to either QA or $QB0$ outputs from the second IC. This way the division ratio on the $QB0$ output can be adjusted without adjusting the QA division ratio. The 10 MHz clock from the MCU is routed to a third counter on the microcontroller that is setup to generate a pin interrupt every 10 ms, which is used by counters 1 and 0 to store their count and clear the counter. The last part is done in software in which the 2 counts are compared using eq. (5.1).

C_{out}, the sent out countdata, depends on whether the counts on C_0 (the counter with the higher division ratio, as seen in fig. 5.8) is above the theoretical maximum count for the microcontroller. Which is $1800 \cdot 10^3$ for a period of 10 ms. However, experiments show that for countrates higher than $1700 \cdot 10^3$ things get distorted. Therefore a safety margin for the count of C_1 is set to $1690 \cdot 10^3$.

$$C_{out} = \begin{cases} C_1 \text{ when } 16 \cdot C_o \leq 1690 \cdot 10^3 \\ C_0 \text{ when } 16 \cdot C_o > 1690 \cdot 10^3 \end{cases} \tag{5.1}$$

The 10 ms match interrupt generated by Counter 2 also executes a routine on the microcontroller that increments the sequence number (timestamp) and sets the flag to transmit a CAN-FD message after comparison of C_1 and C_0.

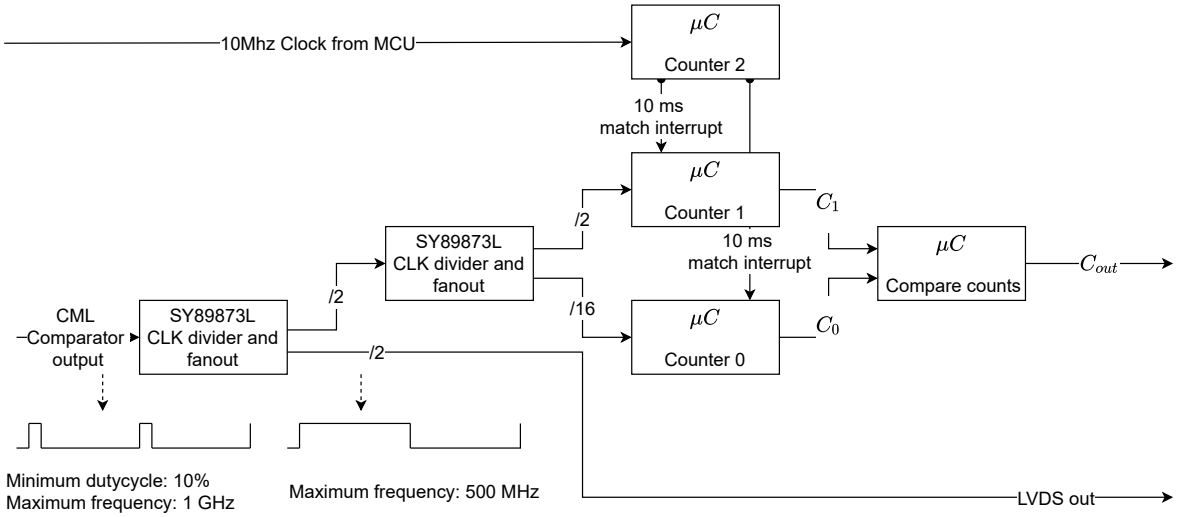


Figure 5.8: Counting circuit.

When the "LVDS out" signal in fig. 5.8 would be used by a time-tagger, timing-jitter as explained in section 2.2.3 becomes a relevant specification of the signal. As shown in fig. 3.2, the analog output is connected to the input of the comparator. The jitter introduced by the ADCMP572 comparator and the SY89873L clock division IC must therefore be considered. The best possible FWHM jitter currently measured on the analog amplified output was 15 ps (see table 2.2). This value is based on a Gaussian distribution which implies that the FWHM jitter (j_{FWHM}) is related to the *Root Mean Squared* (RMS) jitter (j_{RMS}) as in eq. (5.2)[4].

$$j_{\text{FWHM}} = 2\sqrt{2\ln 2} \cdot j_{\text{RMS}} \tag{5.2}$$

The jitter for the comparator is specified in the datasheet as 10 ps deterministic jitter and 200 fs random jitter, it is assumed these are RMS values. The clock division IC is specified at 1 ps RMS cycle to cycle jitter.

n uncorrelated jitter sources may be summed up quadratically resulting in the total RMS jitter j_{tot} being:

$$j_{tot} = \sqrt{j_1^2 + j_2^2 + ... + ... + j_n^2} \tag{5.3}$$

If we plug in the value for analog jitter, together with the comparator jitter and the clock divider jitter the total FWHM jitter (j_{tot}) would then be:

$$j_{tot} = \sqrt{\left(15 \cdot 10^{-12}\right)^2 + \left(2\sqrt{2\ln 2} \cdot 10 \cdot 10^{-12}\right)^2 + \left(2\sqrt{2\ln 2} \cdot 200 \cdot 10^{-15}\right)^2 + \left(2\sqrt{2\ln 2} \cdot 10^{-12}\right)^2} \approx 28\,\text{ps} \tag{5.4}$$

Further research would have experimentally verify this value and conclude whether this total jitter would be an acceptable value for a time-tagger. This research has not been performed since the LVDS out signal was a "Could Have" goal for this thesis.

5.2.2. Set comparator trigger level

This component must match **G-REQ 6** with the output ranging between 0 V and 2.25 V with at least 12 bit resolution. The MCP48CVB21 by Microchip has been used in the first proof of concept design and fulfilled its functionality. It is an inexpensive 12 bit DAC that has an internal band-gap reference such that the output can be set between 0 V and 2.428 V without supplying it with an external reference.

5.2.3. Set bias current and latch detection

This circuit must be able to supply a positive or negative DC-bias current as stated by **G-REQ 1**. Next to that, it must be able to monitor the voltage over the SNSPD (**G-REQ 2**) such that the CU can perform an I/V and I/Count sweep (**G-REQ 12**, fig. 3.5a and fig. 3.5b) and can actively quench the SNSPD when latched into resistive state (**G-REQ 3**). The DC-biasing of the SNSPD is done through a second-order low-pass filter comprising of R_x, R_y, R_z and C's connecting to the RF-line, as shown in fig. 5.9. This reduces the RF signal interfering with the bias source and reversely creating an impedance mismatch with the 50 Ω RF-line. Since the SNSPD can have 2 blocks connected to it inside the cryostat (also shown in fig. 5.9), the latch detection must become very sensitive (as explained in section 3.1.1). Especially for the cases where both the bridge resistors and the cryogenic amplifier are connected.

In essence, a latched SNSPD changes the current through its bias circuit by altering the total resistance of the circuit. There are multiple ways to detect a latched SNSPD. A couple of options have been considered and were found to not be applicable within the set system requirements:

- Current mirror: Using a current mirror to copy the bias current would decouple the current used by the measurement circuit from the bias current through the SNSPD. In addition, an IC using for instance trans-linear techniques allow direct amplification of the mirrored current such that the requirements for subsequent readout circuitry can be less demanding. However, since the SNSPD must be able to have bipolar biasing (**G-REQ 1**), this option is not applicable.

- Phase change detection: The SNSPD has a defined kinetic inductance. Therefore, the impedance at a given frequency due to a latched SNSPD will change and can be detected. Superimposing a sine wave with a certain frequency on the DC-bias current would allow for measuring the AC impedance and hence the phase change due to a latched detector. However, since the inductance is in the order of 500 nH and the latched resistance is in the order of 1 MΩ, the required frequency to measure a proper phase change due to a latched detector is in the order of 100 MHz or even higher. The signal amplifier has roughly a 60 dB of gain in the range of 5 MHz up to 2 GHz, so superimposing a frequency within this range with a very small amplitude (e.g. 100 µV range) will cause saturation of the amplifier.

A more promising method is using the voltage difference on the bias circuit imposed by the latched SNSPD. The following calculations will show the degree of freedom that can be used to optimize the identification of a latched detector.

Referring to fig. 5.9, R is defined as the total Ohmic resistance between V_{dac} and ground at the time the SNSPD is in superconducting state. If we define ΔR as the change in total resistance due to a latched SNSPD then:

$$\Delta V_a = V_a(\Delta R \neq 0) - V_a(\Delta R = 0) \tag{5.5}$$

$$\frac{\Delta V_a}{V_{dac}} = \left(\frac{R + \Delta R - R_x}{R + \Delta R} - \frac{R - R_x}{R}\right) = \underbrace{\frac{\Delta R}{R}}_{fixed} \cdot \underbrace{\frac{R_x}{R + \Delta R}}_{free} \tag{5.6}$$

$\frac{\Delta R}{R}$ ratio is fixed at the moment the bias resistor values (R_x, R_y, R_z) are chosen. By practical measurements it was shown that R_z must be at least 10 kΩ to keep proper impedance mismatch with the RF-line and prevent any significant noise to be added to the signal. Next to that, to be able to supply the bias current in the μA range at a precision of ~ 10 nA using a 16 bit DAC in the range of ±10 V, $R_x + R_y + R_z \geq 30\,\text{k}\Omega$.

$\frac{R_x}{R+\Delta R}$ ratio is free, implying that to get a decent voltage difference when the SNSPD is latched, R_x must be chosen large with respect to $R + \Delta R$

Table 5.1: Typical values for fig. 5.9.

R_x	R_y	R_z	C	R_c	R_{bs}	R_{bp}	R_n	L_k
50 kΩ	50 kΩ	50 kΩ	15 nF	70 kΩ	100 Ω	100 Ω	1 MΩ	500 nH

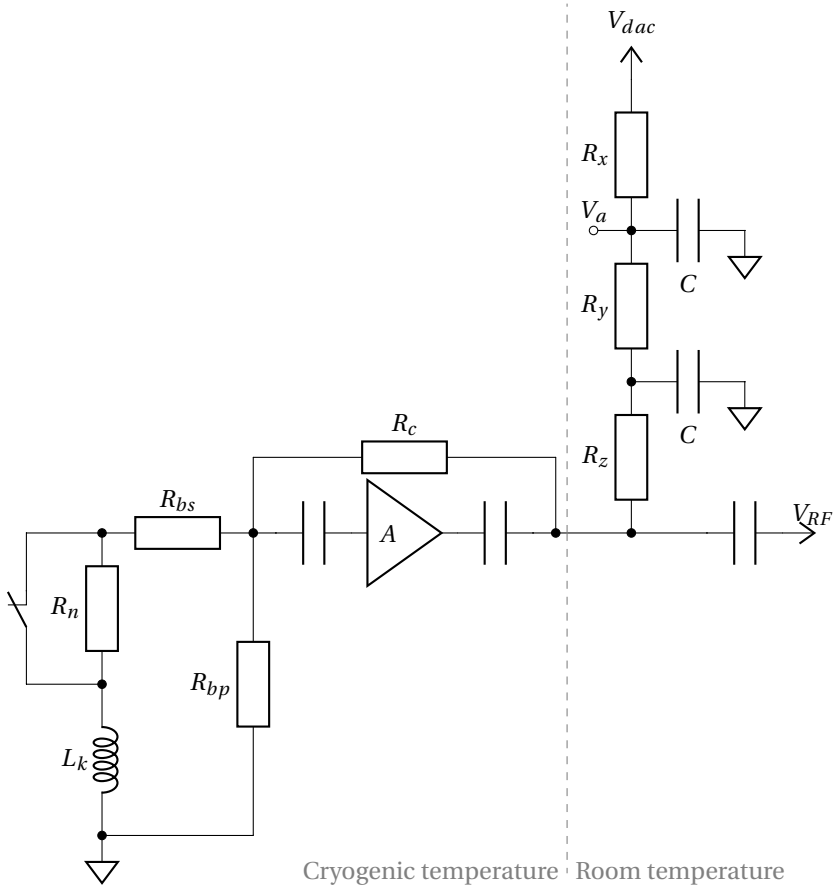


Figure 5.9: Complete biasing circuit. Values are shown in table 5.1.

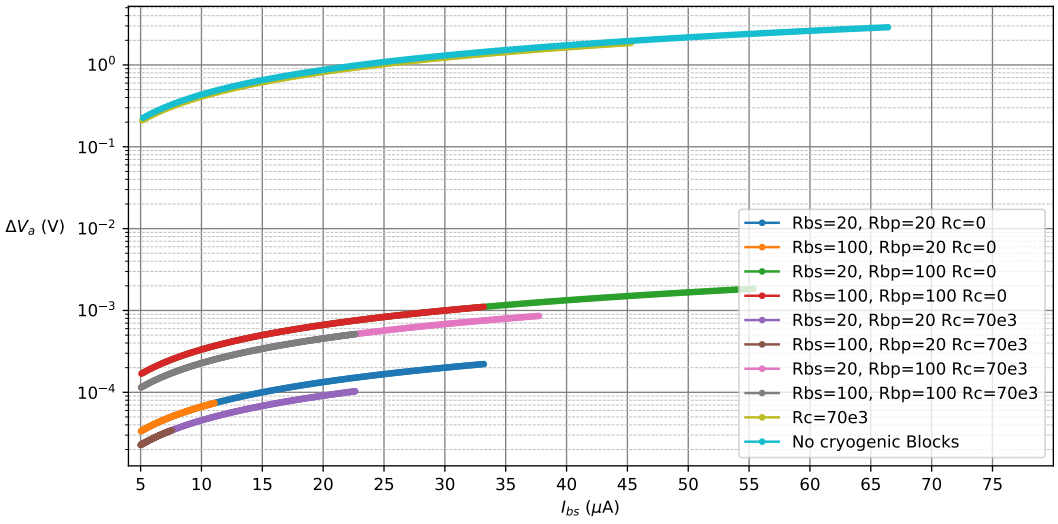


Figure 5.10: Voltage change on V_a at a latching event of the SNSPD with respect to the (unlatched) bias current through the SNSPD.

The simulation results in fig. 5.10 are based on the typical values in table 5.1. It shows results of ΔV_a for bias voltage range between $40\,\text{mV} \leq V_{dac} \leq 10\,\text{V}$ with all variations of the cryogenic blocks:

1. **NONE:** No cryogenic blocks.

2. **RC:** Just the cryogenic amplifier's bypass resistor R_c.

3. **RB**: Just the bridge resistors R_{bs} and R_{bp}, values varied from 20 Ω to 100 Ω.

4. **RC+RB:** Combining the cryogenic amplifier's bypass resistor R_c with the bridge resistors R_{bs} and R_{bp}.

The resulting bias current ranges between $5\,\mu A \leq I_b \leq 70\,\mu A$. The bias current is limited due to the maximum bias voltage of 10 V, this way some simulations have reduced bias current range due to a higher total resistance.

The range of ΔV_a is between $22\,\mu V \leq \Delta V_a \leq 3\,V$.

If we now adjust the parameters as shown in table 5.2, such that R_x is larger with respect to $R + \Delta R$ while maintaining a proper impedance mismatch for the 50 Ω RF-line. The simulation results in fig. 5.11 show that there is an increase in voltage change over the complete range.

Table 5.2: New values for fig. 5.9 used for the simulation results shown in fig. 5.11.

R_x	R_y	R_z
50 kΩ	10 kΩ	10 kΩ

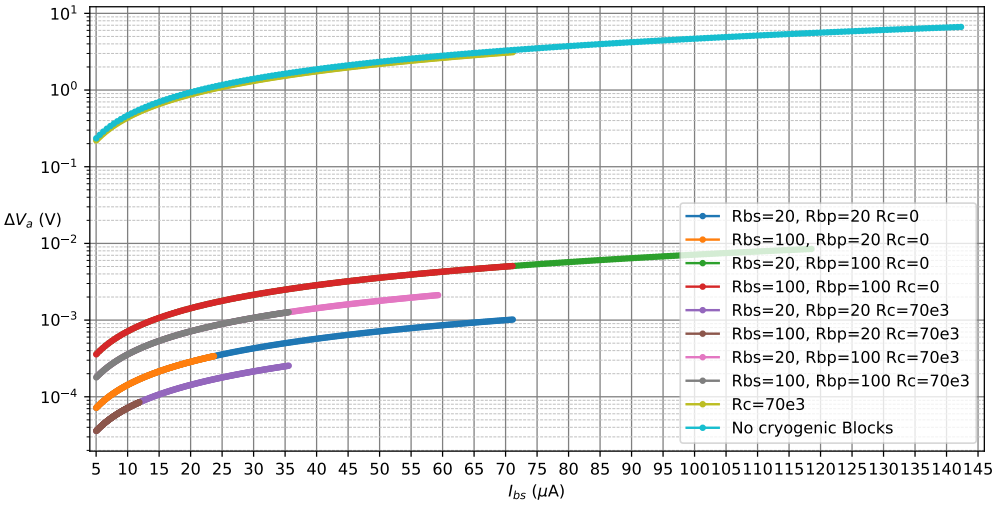


Figure 5.11: Voltage change on V_a at a latching event of the SNSPD with respect to the (unlatched) bias current through the SNSPD, optimized resistors.

The simulations give a rough estimation on the requirements imposed on the readout circuit. The detectable range of ΔV_a is now:

$$38\,\mu V \leq \Delta V_a \leq 7\,V \tag{5.7}$$

This range is relevant especially for the bias currents as low as 5 µA with bridge resistors and a cryogenic amplifier stage in place and still allow the system to actively quench the SNSPD. To make sure the latch detection and active quenching is not influenced by noise, the following requirements must be taken into account for the readout circuit: The peak to peak noise $v_{n,pp}$ within $6\sigma = 99.999\,66\,\%$ (σ being the RMS noise) is at least a factor $\sqrt{10}$ times smaller then the smallest detectable voltage change $\Delta V_a = 38\,\mu V$. This results in a maximum peak to peak noise requirement of: $v_{n,pp} \leq 12\,\mu V$. Making the occurence of a false latch detection due to noise negligible. This imposes the following SNR requirement:

$$\mathrm{SNR}_{min} = 20 \cdot \log\left(\frac{38}{12}\right) = 10\,\mathrm{dB} \tag{5.8}$$

The capacitor C connected to the bias line at V_a creates an approximate first order low pass filter with:

$$f_c \approx \frac{1}{2\pi R_x /\!/ (R_y + R_z) C} \approx 742\,\text{Hz} \tag{5.9}$$

The actual bandwidth, limiting the noise, will be smaller since the bias circuit is actually a second order low pass filter. To be on the safe side, the first order approximation is used.

R_c, R_{bs} and R_{bp} are not taken into account for the noise-calculation since they are at temperatures of 20 K or less and using them in the bandwidth-calculation would only further diminish the bandwidth. In addition the resistance of R_{bs} and R_{bp} are 3 orders of magnitude lower than the resistors in the bias circuit.

The *Equivalent Noise BandWidth* (ENBW) for a first order approximation of this bias circuit is:

$$\text{ENBW} \approx f_c \cdot \frac{\pi}{2} \approx 1167\,\text{Hz} \tag{5.10}$$

This results in a RMS thermal noise of approximately:

$$v_{n,rms} \approx \sqrt{4kTR_x /\!/ (R_y + R_z) \cdot \text{ENBW}} \approx 525\,\text{nV} \tag{5.11}$$

The maximum peak to peak noise budget that may be injected by the readout circuitry ($v_{n,ic,pp}$) is therefore:

$$v_{n,ic,pp} \leq \sqrt{\left(12 \cdot 10^{-6}\right)^2 - \left(6 \cdot 525 \cdot 10^{-9}\right)^2} \leq 11.57\,\mu\text{V} \tag{5.12}$$

There are a couple of problems with measuring ΔV_a single ended in the μV range that might wrongly trigger the latch detection:

1. Adjusting the bias current: this will also impose a ΔV_a since the overall voltage changes. This can be solved by a software subtraction of the previous voltage measured.

2. An uncontrolled voltage spike or dip in the supply by V_{dac}.

3. The absolute voltage range on V_a: this voltage can range between about ± 9.5 V even with ΔV_a in the μV range. This eliminates the possibility to amplify ΔV_a before readout.

These problems are solved by using a balanced bridge (a Wheatstone bridge) approach as shown in fig. 5.12.

At initialization of the CU, the SNSPD is biased with a current at which it is certainly superconducting (e.g. 1 µA to 5 µA). In this state, the bridge is actively balanced by adjusting the value of R_{pot} such that $V_{ab} = V_a - V_b \approx 0$ V.

An adjustment to the bias current or voltage spike/dip imposes a different voltage at V_a but this voltage change also occurs at V_b such that V_{ab} remains approximately 0 V, solving problem 1 and 2. Next to that, this approach allows for a subsequent *Instrumentation Amplifier* (INAMP) with a high gain, solving problem 3. When the bridge becomes unbalanced by a latched SNSPD, it will be detected by $V_{ab} \neq 0$ V. V_{ab} is used as an input for the circuit in fig. 5.13.

Now the thermal noise due to the right half of the Wheatstone bridge has to be taken into account as well. The passive components on this half will be equal to the components on the left half effectively increasing the noise by $\sqrt{2}$. This results in a new maximum peak to peak noise budget that may be injected by the readout circuitry ($v_{n,ic,pp}$):

$$v_{n,ic,pp} \leq \sqrt{\left(12 \cdot 10^{-6}\right)^2 - 2 \cdot \left(6 \cdot 525 \cdot 10^{-9}\right)^2} \leq 11.14\,\mu\text{V} \tag{5.13}$$

We still have to define the requirements for the amplification stage, the potentiometer and ADC, such that the voltage change can be detected.

Requirements for the INAMP are:

1. **Low drift in offset and gain:** a drifting INAMP could falsely trigger the active quenching.

2. **Low noise:** can not be higher than 11.14 µV from 0 Hz $\leq f_n \leq$ 10 Hz

3. **Common-mode input voltage:** range must be ± 15 V since that is the supply voltage for the bias current DAC.

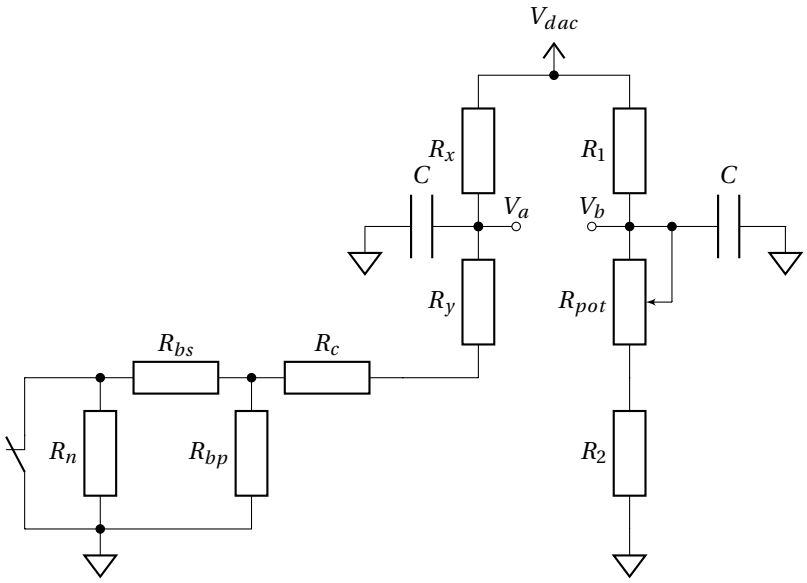


Figure 5.12: Simplified circuit of a balanced bridge with bypass resistor from the cryogenic amplifier, bridge and model of an SNSPD

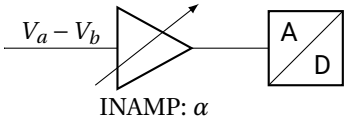


Figure 5.13: Amplification and readout.

4. **Tunable gain:** as the range of detectable voltages is $38\,\mu V \leq \Delta V_a \leq 7\,V$ the gain must be adjustable based on the SNSPD and bias circuit configuration. At least a gain factor α between $0.25 \leq \alpha \leq 100$.

Due to the rather stringent requirements, only a single suitable INAMP has been found: the PGA281 .

Table 5.3: Relevant parameters for the PGA281 Instrumentation Amplifier.

Parameter	Value
α	$\frac{1}{8} \leq \alpha \leq 176$
Gain Drift	0.5 ppm/°C
Voltage Drift	0.05 µV/°C
$v_{n,pp}$	420 nV in range 0.1 Hz $\leq f \leq$ 10 Hz at $\alpha = 128$.
Differential output voltage v_{out}	$0\,V \leq v_{\text{out}} \leq 5\,V$

In the worst case scenario, the PGA281 is set to its maximum gain $\alpha = 176$ at which the minimum voltage difference 38 µV is amplified to 6.688 mV. This would result in a minimal bit resolution requirement for the ADC of

$$\log_2\left(\frac{5}{6.688 \cdot 10^{-3}}\right) \approx 10\,\text{bit} \tag{5.14}$$

However, for cost effectiveness and research purposes it would be beneficial to test if the balanced bridge could be read out by an ADC without a PGA281 in between. Therefore the minimal requirement on the resolution is:

$$\log_2\left(\frac{5}{38 \cdot 10^{-6}}\right) \approx 18\,\text{bit} \tag{5.15}$$

Noise requirements on the ADC are not very stringent since the added noise is small with respect to the amplified input voltage. The requirements for the subsequent ADC are:

1. **Minimal sample rate:** 100 Sa/S such that every integration interval of 10 ms the voltage can be sampled.
2. **Minimal resolution:** 18 bit
3. **Input voltage range:** must be in $0\,\text{V} \leq v_{\text{in}} \leq 5\,\text{V}$.

This INAMP is built to be used in combination with a specific ADC: the 24bit 14kSa/S with Low-Drift Reference: ADS1259. The low drift reference can be used as the common-mode signal that the PGA281 needs for its output to distinguish between positive and negative differential input signals. It has the following specifications:

Table 5.4: Relevant parameters for the ADS1259 Analog to Digital-Converter.

Parameter	Value
Sample rate f_s	$10\,\text{Hz} \leq f_s \leq 14\,400\,\text{Hz}$
Resolution	24 bit
Noise free bits at 400Sa/S	19 bit
Input voltage range v_{in}	$0\,\text{V} \leq v_{\text{in}} \leq 5\,\text{V}$

5.2.4. CAN-bus Transceiver

The CAN-FD transceiver one recommended by NXP: the TJA1057, which includes a logic level shifter from the 3.3 V logic levels used by the microcontroller to the 5 V used by the CAN-FD physical interface.

5.2.5. Hardware Address

Each of the 12 CUs needs an unique address such that the MCU can distinguish count data from all the CU.

A straightforward approach is implementing a circuit that can be fixed to a certain value between 0 and 11 and readout by the microcontroller during initialization. There are various ways to implement this, from a simple DIP-switch for each CU up to dedicated unique ID ICs. However, all these options add costs and take up PCB space on the system. There is a more straightforward implementation that does not need any component costs, assembly time (adjusting the DIP-switches based on the required address) or added initialization complexity (programming/readout of the EEPROM on the unique ID IC and communicating the ID to the MCU). This approach is fixing 4 GPIO lines to (3.3 volt) or (0 V) via the PCIe x1 connector on the backplane, based on the position of the PCIe x1 connector, such that CU-0 is 0000 up to CU-11 is 1011 in binary notation. This way no added component costs, assembly time or complex initialization schemes are required to fix the hardware address for each CU.

5.2.6. Microcontroller

As stated at the beginning of this chapter, the LPC54618 is used. The software will be explained in section 5.2.8.

5.2.7. Interfaces

This section describes the internal Channel Unit interfaces as shown in fig. 5.4, specified with **iC.#**. The interfaces (**i.#** and **iG.#**) are explained in respectively sections 4.1.2 and 4.2.4.

iC.1 A TTL interface that signals photon detections in both its rising and falling edge.

iC.2 A TTL interface that signals photon detections in both its rising and falling edge at a selectable division ratio.

iC.3 Multiple GPIO lines that set the division ratio.

iC.4 SPI interfacing with the comparator trigger level DAC.

iC.5 SPI interfacing with the bias and latch detection peripherals.

iC.6 CAN RX/TX interface

iC.7 4 GPIO lines that are hardwired to either “1” (3.3 V) or “0” (0 V) for setting an unique CU hardware address.

5.2.8. Software

The software has been written in C/C++, compiled by "gnu++14" and follows the hierarchical flow diagrams shown in figs. 5.14 to 5.17.

The *Integrated Development Environment* (IDE) used for debugging and compiling is MCUXpresso by NXP which is an Eclipse based IDE.

Figure 5.14 shows the global flow of the CU software. The transmission of a CAN message is dictated by the high priority interrupt generated by the integration interval. This way a steady stream of CAN messages is generated. Every 10 ms each CU sends a 64 byte message to the MCU. The contents of the message is shown in appendix B fig. B.3.

Occasionally the MCU might send a CAN message to the selected CU. When this happens a lower priority interrupt is triggered at the arrival of the message and the message is handled in the CU state machine in the time between CAN transmissions from the CU. The state machine shown in fig. 5.15 shows that after initial-

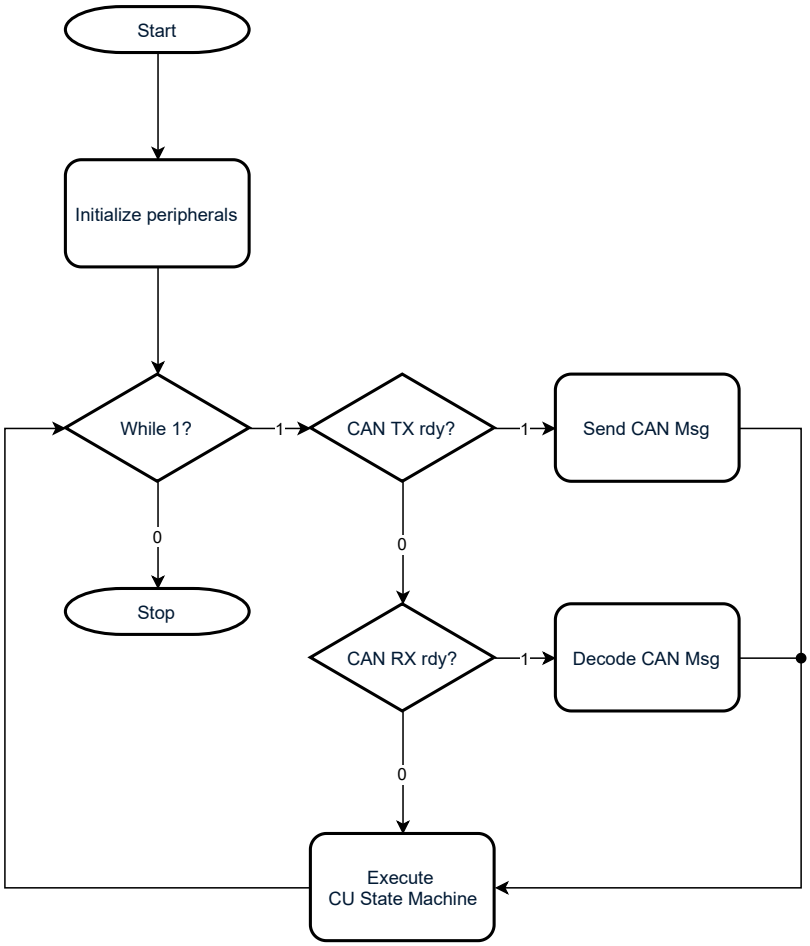


Figure 5.14: Channel Unit global flowdiagram.

ization only 2 states can occur. Normal and Sweep. Normal state incorporates the flow diagram as shown in fig. 5.16 and handles all CAN function messages from the MCU that can be executed. The message contents are depicted in appendix B fig. B.2. At every iteration of the Normal state flow diagram, the latch detection (and possible active quenching) of the SNSPD is executed. Whenever an adjustment on parameters or other settings has been executed by the CU, these adjustments will be looped back to the MCU by updating the CAN message.

Normal state allows switching to Sweep state when a Sweep function is requested by the MCU. Before switching to the Sweep state, the sweep parameters are set: The start bias current I_a, end bias current I_b, current increment I_c and integration time t_i (the time between each current increment). Also the present bias current setting is stored such that after the sweep the normal bias current can be reset. In the Sweep state flow

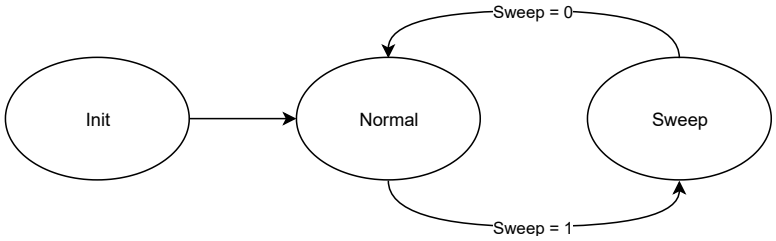


Figure 5.15: Channel Unit state machine.

diagram depicted in fig. 5.17, the only CAN function message from the MCU that is allowed to be processed is the “abort sweep” function. All other functions requested by the MCU are ignored. The integration time for the sweep function can be adjusted in multiples of the fixed 10 ms integration interval. Every time the integration time has passed, the monitor voltage is sampled and the bias current is incremented by I_c. Subsequently, the information in the CAN message is updated. Lastly, the bias current setting is tested against the end bias current I_b. When the sweep is completed, the normal bias current is reset and the state returns to “Normal”.

5.3. Backplane

The backplane incorporates only passive components and traces that allow the interfaces between the CUs and the MCU to be connected. It also transports the various power lines to the CUs and MCU. Its length is rather large: 38 cm. Therefore, care has been taken such that the signal lines for **iG.4** and **iG.3** are of equal length (within 1 mm) for all CUs. This reduces the signal skew such that all CUs reset their sequence number at the same time and that the clock signal is arriving at the same time. The signal lines for the clock are routed at the bottom layer as shown in figs. D.3 to D.5.

5.4. PSU

Since the power budget is 60 W, we have to determine which of the supply voltages get what share in this budget. The power requirements for each CU are shown in table 5.5.

Table 5.5: Power Supply Unit requirements for each CU.

Supply voltage	3.3 V		5 V		±15 V
LPC54618	200 mA	TJA1057	70 mA	AD5761R	12 mA
SY89873L	2 · 95 mA	RT-amp power	50 mA		
MCP48CVB21	120 mA				
PGA281	0.13 mA	PGA281	25 mA	PGA281	6 mA
MAX9171	15 mA				
ADS1259	0.70 mA	ADS1259	3.8 mA		
AD5293BRUZ-100	0.01 mA			AD5293BRUZ-100	0.03 mA
ADCMP572	50 mA				
Total ≈	510 mA		150 mA		18 mA

6.5 V is supplied by the PSU and is converted on each CU to 5 V by means of a NCP718 *Linear Drop-Out* (LDO) regulator, dissipating up to 0.25 W each at an output current of 150 mA. This results in at most $12 \cdot 0.25\,\text{W} = 3\,\text{W}$ extra power demand to the power budget assigned to the 6.5 V line.

The power supply demand on the 3.3 V line for 12 CUs is ≈ 21 W, 5 V at ≈ 9 W and ±15 V at ≈ 7 W. The MCU will demand power in both the 3.3 V and 5 V domain. For this we reserve an additional 1 W at 3.3 V and 1 W at 5 V. Accepting about 10 % losses due to voltage conversion and allowing some resistive losses in power transportation results in the final PSU output power demands shown in table 5.6. For this thesis, it has been decided to keep the PSU board as simple as possible since the focus of the thesis is not to produce a power supply board. Using integrated electronics by Tracopower will convert the 24 V output from the POE splitter to 3.3 V using the TEN30-2410, to 6.5 V using the TSR2-2465 and to ±15 V using the THD12-2423. Reference designs, also taking into account *ElectroMagnetic Compatibility* (EMC), that have been supplied

Table 5.6: Power Supply Unit requirements.

3.3 V	6.5 V	±15 V
30 W	13 W	8 W

by the manufacturer have been carefully redrawn on the PCB as shown in fig. D.6. It is a 2 layer board with 70 µm copper thickness such that the high current draw will not be hampered by the resistance in the copper foil. It also helps with the power dissipation from the converters.

5.5. Conclusion

This chapter described the various design decisions that had to be made in order to meet the set requirements.

The complexity of the work was in designing the frequency divider and fanout circuit (5.2.1), the set bias current and latch detection circuit (5.2.3) for the CU due to their stringent requirements, the software such that the microcontrollers would be configured and running properly and not in the least the physical design for both the CU and the backplane allowing a systems to really become a “plug and play” system.

A traceability table has been drawn to verify that each requirement is implemented in at least one of the subsystems in table 5.7. The schematics for all designs are added in appendix C and a reprint of all PCB designs are shown in appendix D. With the PCBs for the CU and backplane ready, the following chapter will explain the procedures and results for the tests such that the requirements may be verified.

Table 5.7: Requirements Traceability

Requirement	MCU	CU	PSU
G-REQ 1		✓	
G-REQ 2		✓	
G-REQ 3		✓	
G-REQ 4		✓	
G-REQ 5	✓	✓	
G-REQ 6		✓	
G-REQ 7		✓	
G-REQ 8	✓		
G-REQ 9	✓	✓	
G-REQ 10	✓	✓	
G-REQ 11	✓	✓	
G-REQ 12	✓	✓	
G-REQ 13		✓	
G-REQ 14	✓		
G-REQ 15	✓		
G-REQ 16	✓	✓	
G-REQ 17	✓	✓	
G-REQ 18	✓	✓	
G-REQ 19			✓
G-REQ 20	✓	✓	

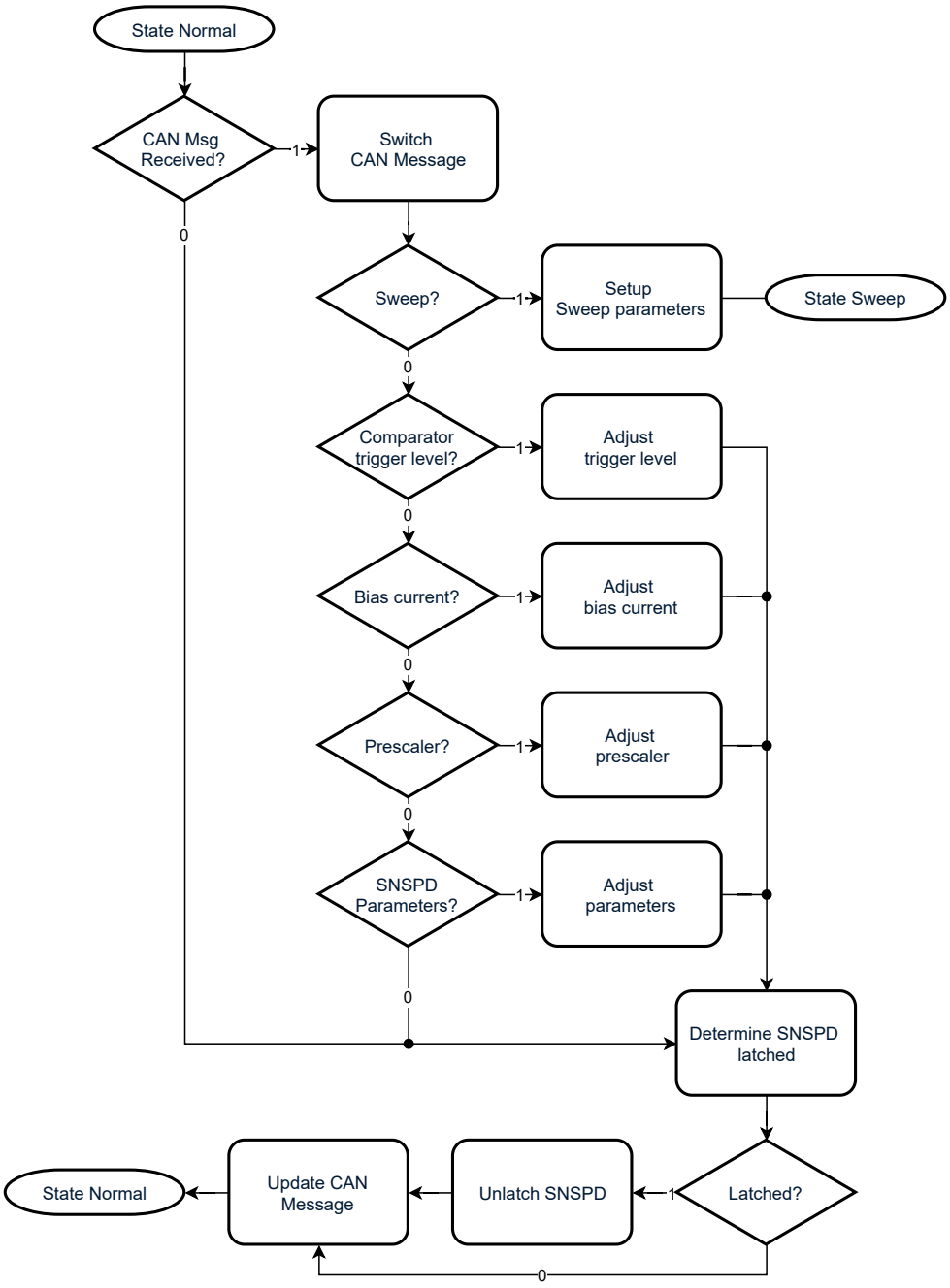


Figure 5.16: Channel Unit state: normal.

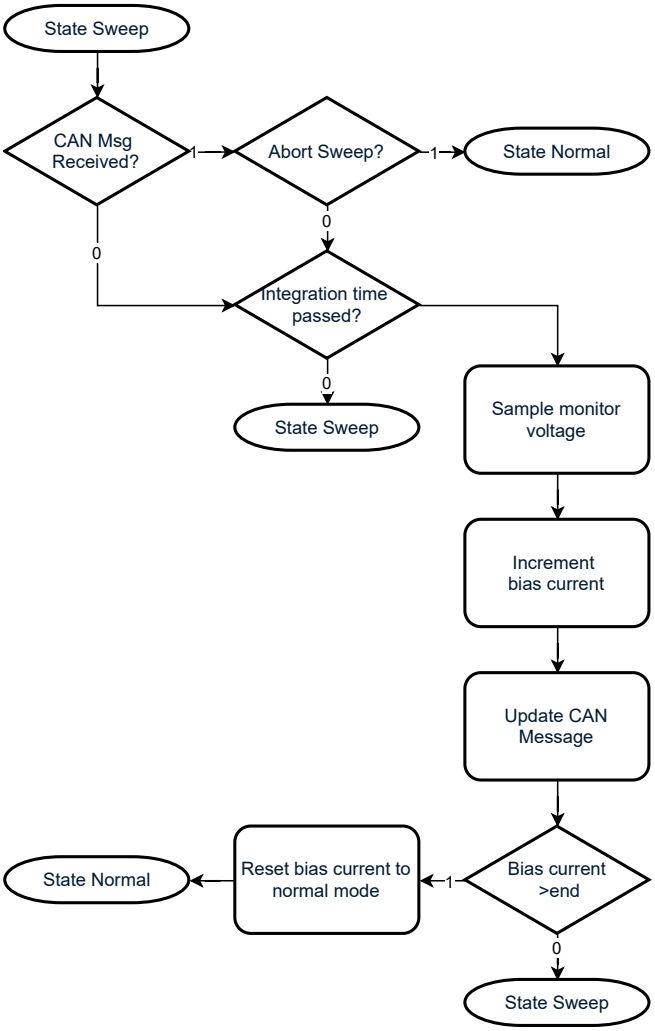


Figure 5.17: Channel Unit state: sweep.

6

Testing and Results

The following chapter explains the test procedures and the results for the requirements stated in appendix A. Some requirements are specifically implemented by one of the subsystems and can therefore be tested through a unit-test. Others require the testing of the interfaces that have been decided on in section 4.2.4 through an integration test and finally the requirements that comprise the complete system are tested in the acceptance test. The requirements are reprinted in a blue box, and are followed by a short explanation of the test procedure and lastly the test results are shown.

6.1. Unit tests

The next subsections will describe tests that have been performed solely on the individual units.

6.1.1. CU-Active Quenching

G-REQ 3 The system shall be able to automatically unlatch the SNSPDs including those that are equipped with a bridge and/or a cryogenic amplifier circuit.

For these requirements a separate test PCB has been designed which comprises of passive circuits that simulate the 4 possible SNSPD configurations as shown in fig. 6.1.

The configurations are:

1. **None:** No cryogenic blocks connected to the SNSPD.
2. **RB:** Bridge resistors connected to the SNSPD.
3. **RC:** The bypass resistor from the cryogenic amplifier is connected to the SNSPD.
4. **RC+RB:** Both the bridge and bypass resistors are connected to the SNSPD.

The testboard holds two 4-DIP switches. One decides the SNSPD configuration and the other emulates a latched SNSPD. It connects to the CU through the same board to board connectors as the RT-Amp (10-pin Molex).

Procedure:

Upon initialization of the CU, it first balances the Wheatstone bridge using proportional (P)-controller software that reduces V_{ab} to approximately 0 by adjusting the value of R_{pot}, see fig. 6.4. When the most optimal value for R_{pot} is found, it determines the slope r in ($\Delta V_{ab}/\Delta V_{dac}$) of V_{ab} imposed by the imperfect Wheatstone circuit (R_{pot} increments its resistance with steps of $\frac{100\,\mathrm{k}\Omega}{1024} \approx 97.66\,\Omega$). This is done using the following equation:

$$r = \frac{V_{ab}(I_{bias}) - V_{ab}(-I_{bias})}{V_{dac}(I_{bias}) - V_{dac}(-I_{bias})} = \Delta V_{ab}/\Delta V_{dac} \tag{6.1}$$

In words, the slope is the change in V_{ab} with respect to the change in V_{dac} (the bias voltage in fig. 6.1 V_{bias}). As explained in section 5.2.3, the SNSPDs are always biased above 5 µA (or below -5 µA) which implies it can not be latched between ±5µA, therefore we set $I_{bias} = \pm 5\,\mu\mathrm{A}$.

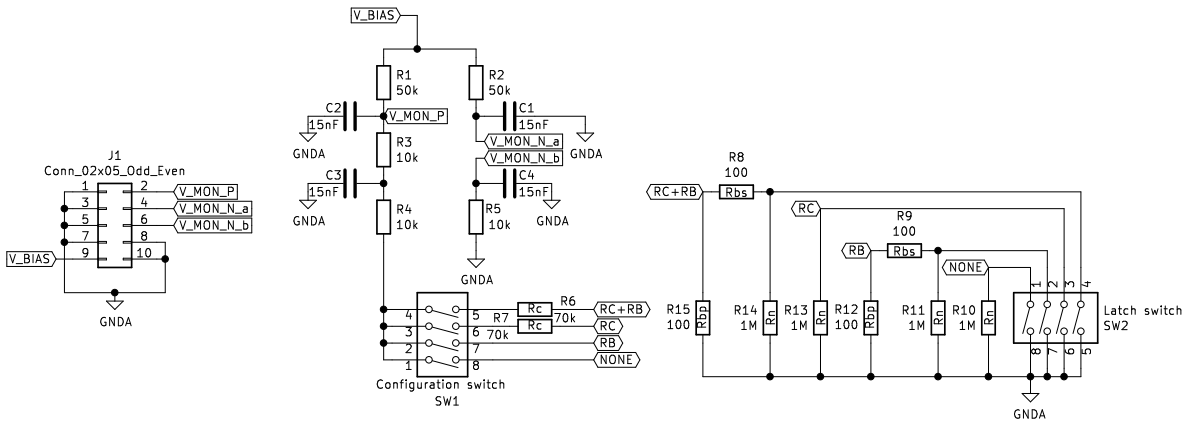


Figure 6.1: Testboard circuits. On the left is the 10-pin Molex connector, connecting the testboard signals to the CU. The middle part is the biasing and balancing circuit (potentiometer on the CU) and the configuration can be chosen by SW1. On the right, the latch switch that is normally closed (superconducting state) and opened when a latched SNSPD is emulated.

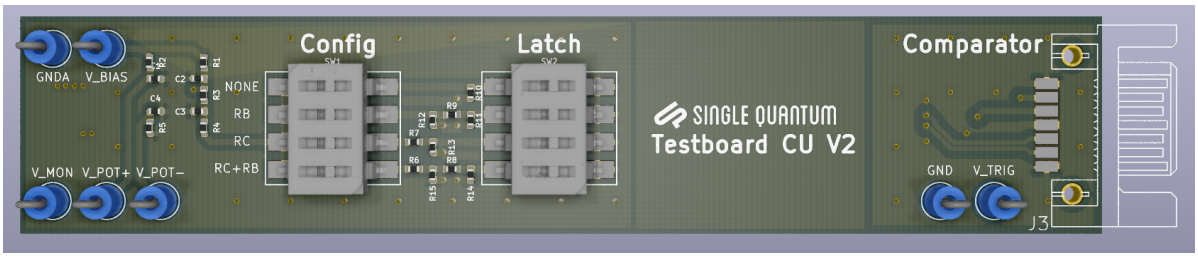


Figure 6.2: Testboard Front.

The approach to determine the slope r in eq. (6.1) assumes the complete circuit to be purely resistive (linear) at DC with the SNSPD in superconducting state. The only possible nonlinearity is in R_{pot} which is ±1 LSB. This is a non-issue since once the bridge is balanced, the value for R_{pot} is not changed or used in the calculation. Therefore, it is fair to assume that the circuit is linear. The slope can be either positive or negative. This depends on in the Wheatstone bridge being balanced slightly below or above the equivalent resistance of the bias circuit.

Two latch event types may occur, and only the second type needs to know the slope, r_0, of an unlatched SNSPD.

1. The first type of latch event is at a fixed bias current close to the critical current. This is detected by sampling V_{ab} every 10 ms and compare the previous sample with the current sample. When it is out of bounds, the SNSPD is latched and the bias current is switched off for 1 s.

2. The second event is a latch that follows directly after an increase in bias current. This happens when the user of the system adjusts the bias current to a new steady state value which could also latch the detector into resistive state. Due to the not perfect balancing of the Wheatstone bridge it is necessary to compare the slope of this adjustment in bias current with respect to the non-latched slope r_0. If the slope is out of bounds of the slope of an unlatched detector, the detector must be latched and the bias current is switched off for 1 s.

The bounds for these two types of latch events are variable since they depend on the gain of the INAMP and the inaccurracy of R_{pot} mirroring the bias circuit. These bounds have been experimentally set in software. The first latch type can be properly shown by the testboard, using the latch-switch to emulate a latched SNSPD. The second needs a real SNSPD to test its functionality.

Results:

A latched SNSPD can be detected and is actively quenched for all four configurations, for both events. However, due to a hardware failure in the CU PCB, graphs showing these events have not yet been drawn. It is

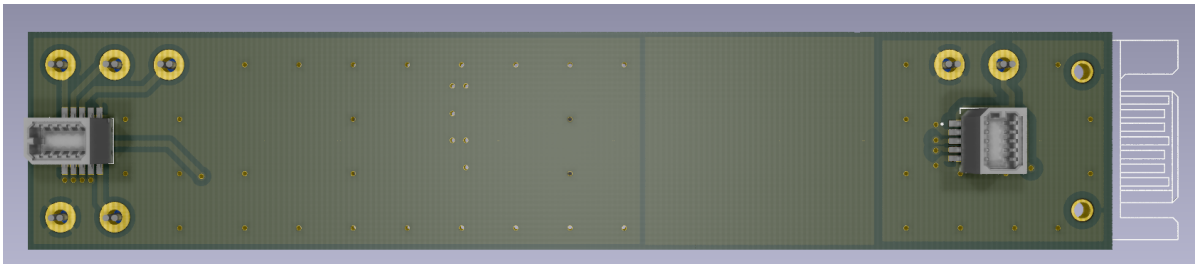


Figure 6.3: Testboard Back.

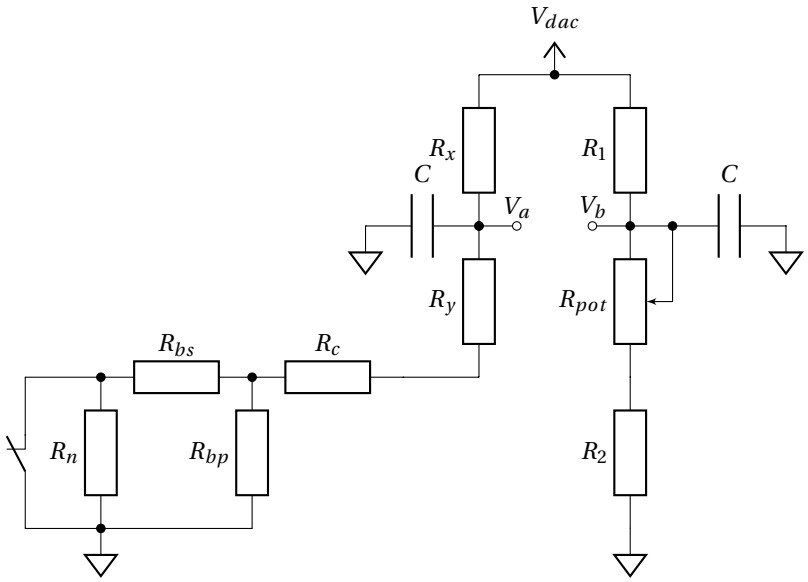


Figure 6.4: Balanced bridge with bypass resistor from the cryogenic amplifier, bridge and simplified model of an SNSPD

assumed that at the thesis defense, graphs showing these events will be available.

Frequency Latching:

G-REQ 4 The system shall be able to unlatch the SNSPDs due to frequency latching.

Frequency latching is implemented by continuously comparing the countrate to a set of values (f_l, the lower count-frequency bound, and f_u, the upper count-frequency bound). If the countrate is out of these bounds, the bias current is switched off for 1 s.

Procedure:

A pulsed laser will be connected to the SNSPD with its repetition rate adjustable to above the set f_u upper count-frequency. When the frequency is above f_u, the counts should return to 0 for 1 s since the bias current is switched off. The result is shown in figure X. The lower count-frequency bound is tested in the following way: when a 50 Ω termination is applied to the input of the RT-Amp (resulting in 0 pulses), the following 1 s should give a monitor voltage of 0 V.

Results:

A frequency-latched SNSPD can be detected and is actively quenched when the counts are out of the count-frequency bounds. However, due to a hardware failure in the CU PCB, graphs have not yet been drawn. It is assumed that at the thesis defense, graphs will be available.

6.1.2. CU-Bias current

G-REQ 1 The system shall be able to supply a bias voltage at least between −10 V and 10 V with steps of 1 mV over the bias circuit for each detector, the accuracy must be ±1 mV.

The DAC that was chosen for the bias current supply: AD5761R can increment its voltage with a precision of 16 bit in theoretical steps of 305 µV at a maximum *Differential Non-Linearity* (DNL) of ±1 LSB as specified by the manufacturer. This results in a theoretical maximum voltage change due to incrementing the DAC by 1 LSB of 610 µV.
Procedure:

1. Design software that increments the bias DAC with a LSB every 100 ms starting from -10 V up to 10 V.
2. Measure the voltage supplied by the DAC with a digital multimeter (Keithley) and save the trace.
3. Compare the voltage change between each incremented LSB with the theoretical value.

Results:
Due to time constraints this test has not been executed. For now we rely on the manufacturers specifications which comply with the requirements.

6.1.3. CU-Monitor voltage

G-REQ 2 The system shall monitor the voltage over the SNSPDs every 10 ms.

By design, each 10 ms integration interval, the monitor voltage is sampled and added to the data package sent over CAN.

6.1.4. CU-Comparator trigger level

G-REQ 6 The system shall be able to adjust the trigger level of the comparators between 0 V and 2.25 V with at least 12 bit resolution.

The MCP48CVB21 comparator trigger DAC has a 12 bit resolution at a set output voltage range of 0 V up to 2.428 V results in a minimum step size of 593 µV.
Procedure:

1. Design software that increments the comparator trigger DAC with a LSB every 100 ms starting from 0 V up to 2.25 V.
2. Measure the voltage supplied by the DAC with a digital multimeter (Keithley) and save the trace.
3. Compare the voltage change between each incremented LSB with the theoretical value.

Results:
Due to time constraints this test has not been executed. For now we rely on the manufacturers specifications which comply with the requirements.

6.1.5. CU-Power

G-REQ 7 Each added channel (SNSPD with counting, bias and amplification electronics) will require at most an additional 3 W.

A single channel including the analog amplification, frequency dividers, microcontroller and bias circuit has been measured to require 2.9 W in normal operation.

6.1.6. MCU-Ethernet

Table 5.7 in chapter 5 shows that **G-REQ 8**, **G-REQ 14** and **G-REQ 15** are implemented solely by the MCU subsystem. For convenience they are reprinted below:

G-REQ 8 The system shall have an ethernet connection with the web-interface.

The MCU is, as stated before, implemented on the development board OM13094 for this thesis. It has a 10/100 Mbit/s PHY interface and a RJ45 connector. Currently the ethernet connection to the web-interface has not been implemented yet. A *Universal Asynchronous Receiver-Transmitter* (UART) connection has been set up which connects with a Python based GUI on a PC. This connection facilitates the control of the 12-channel system and shows the data sent from the MCU. A figure showing the GUI is added to fig. E.1.

G-REQ 14 The system shall be able to supply the current of the temperature-diode which monitors the temperature in the cryostat with a constant current of 10 µA. The design of this circuit will be identical to the circuit currently implemented.
G-REQ 15 The system shall be able to read the temperature-diode voltage and send this to the web-interface.

G-REQ 14 and **G-REQ 15** would implement an already designed circuit which would not add any complexity to this design. Due to this fact and due to time constraints, it has been kept out of the scope for this thesis.

6.1.7. PSU

The PSU has been designed to work for a 60 W input total. Table 6.1 shows the current that can be drawn from each supply voltage.

Table 6.1: Output rating

Voltage	Current
3.3 V	8 A
6.5 V	2 A
±15 V	400 mA

Procedure:
An endurance test has been performed. For this test, 3 DC-loads have been setup to draw the maximum specified current from each supply voltage for 2 h at room temperature without added passive or active cooling on the PSU. After the 2 h have passed, the results as shown in table 6.2 were noted.
Results:
The input voltage was 28 V and average input current 2.179 A making the input power 61.012 W. This results

Table 6.2: Testresults PSU

Output voltage	Actual voltage	Current	Power	Converter Temperature
3.3 V	3.09 V	8.00 A	24.72 W	91 °C
6.5 V	6.27 V	2.00 A	12.54 W	84 °C
±15 V	± 14.29 V	363.6 mA	10.39 W	71 °C

in an efficiency of $\eta = 78\,\%$. It is assumed that the efficiency will go up when the converters get a heatsink.

6.2. Integration

The system integration tests validaties the interfaces between Sub-systems: CU, MCU and the Backplane. These interfaces have been explained in section 4.2.4 and a figure showing their connections is shown in fig. 4.2.

The following sections explain the test procedures and their results.

6.2.1. Interface iG.1: Ethernet connection

The ethernet connection will be tested the moment it is implemented on the MCU. Most likely this will not happen within the thesis period.

6.2.2. Interface iG.2: Reset

The reset interface is hardwired to the microcontroller's reset pins on all CUs and MCU and has been tested to reset the microcontrollers.

6.2.3. Interface iG.3: Synchronize

The synchronize signal will be tested to work in section 6.3.3.

6.2.4. Interface iG.4: Distributed Clock

The distributed clock will be tested to work in section 6.3.3.

6.2.5. Interface iG.5: CAN-bus

The CAN-bus is occupied by 12 Channel Units and 1 MCU and is rated to 5 Mbit/s. In the current implementation, each CU sends out 58.6 kbit/s (64 byte plus CAN-FD message overhead every 10 ms), resulting in a total of 703.2 kbit/s for the 12 CUs. Since the commands from the MCU are occasional, those can not be quantified to the total bitrate. Due to a time shortage it was not possible to assemble a full 12 Channel Units. For testing purposes, 3 additional CU PCBs have been fitted with just the microcontroller circuit and the CAN-transceiver. They act as "dummy" CUs which push out random data on the CAN-bus.
Procedure:

1. Configure the "dummy" CUs such that it pushes out data every integration interval.
2. Use the GUI to save the received data from the MCU to a file.
3. Save the data for 1 min and verify that all packets have been received based on the sequence number.
4. Decrement the integration interval by a factor of 2 to 5 ms such that the data rate is doubled. Repeat step 2 and 3. Repeat this step until step 3 shows that not all packets have been received.

Results:
The integration interval has been decreased to 2.5 ms. 4 CU were connected and sent out their 64 byte data every 2.5 ms to the MCU. This results in a total bitrate of 937.6 kbit/s. This is above the maximum bitrate for 12 CUs at an integration interval of 10 ms. The MCU translates it to UART data. This data is saved on the PC and has been verified to contain all sent information from the CU. Pushing the data rate further showed that not all data is sent over the UART connection. This is due to the limiting speed of the UART.

6.2.6. Interface iG.6: LVDS digitized photon detections

G-REQ 13 The system shall output digitized photon detections based on the LVDS physical interface.

The digitized photon detections are routed from the CU to a dedicated PCIe connector on the backplane. The testing of this interface is straightforward:
Procedure:

1. A sinewave is applied to the input of a specific CU.
2. The trigger level for the comparator is adjusted such that the comparator triggers its output every positive half-wave.
3. The input frequency is varied from 1 Hz up to 1 GHz in decades.
4. The LVDS pins on the PCIe dedicated for the specific CU are measured differentially by 2 channels on an oscilloscope.
5. A comparison with the input frequency is made: Each rising ánd falling edge on the LVDS line correspond to the detection of a positive half-wave of the input frequency. Therefore, the frequency of the LVDS signal must always be half of the input frequency.

Results:
Due to a hardware failure in the CU PCB, graphs have not yet been drawn. It is assumed that at the thesis defense, graphs will be available.

6.2.7. Interface iG.7: Comparator output
The comparator output will be tested to work in section 6.3.1.

6.2.8. Interface iG.8: Comparator trigger level
The comparator trigger level is tested to work in section 6.1.4.

6.2.9. Interface iG.9: Monitor voltage
The monitor voltage is tested to work in section 6.1.1.

6.2.10. Interface iG.10: Bias current
The bias current will be tested to work in section 6.3.5.

6.3. Acceptance
The following sections describe test procedures and -results on requirements that need the complete system to be functional.

6.3.1. Count rate and precision
G-REQ 5 The system shall be able to count from 0 Hz to 1 GHz pulses coming from a comparator CML/ECL output with a minimum pulsewidth of 100 ps. The accuracy in the range ≤ 50 MHz is ±1 count. The accuracy for counts between 50 MHz and 1 GHz is ±20.

As explained in section 5.2.1, the detection pulses coming from the comparator are fed into 2 separate counter circuits which get the pulses divided by different ratios. This way a distinction can be made between low and high detection rates (below/above 169 MHz) with higher absolute precision at low detection rates.
Procedure:
The following three elements in the requirement will be tested:

1. Countrate-bandwidth.
2. Precision.
3. Minimal pulse width.

The following procedure will test the count rate bandwidth and precision:

1. Connect the GUI to the system in which at least 1 CU is initialized.
2. Connect an *Arbitrary Waveform Generator* (AWG) to the SMA input connector.
3. Configure the AWG such that it sweeps over a sinusoidal frequency ranging from 1 Hz up to 1 GHz with a logarithmic incrementation and a timestep of 100 ms.
4. Store the count and sequence number on the GUI.
5. A plot showing the countdata, with respect to their input frequencies such that it may be verified that for each frequency the countdata is correct.
6. A second plot showing the countdata modulo 16 (the division ratio for high detection rates) with respect to the input frequency. This should show some random data between 0 and 15 for frequencies up to 169 MHz. Above this frequency the countdata modulo 16 should show only 0's, verifying that the high detection rate counter is used.

The following procedure will test the minimal pulse width requirement:

1. Connect the GUI to the system in which at least 1 CU is initialized.

2. Connect an AWG to the SMA input connector.
3. Configure the AWG such that it sends out a sinusoidal frequency of 1.4 GHz continuously.
4. Adjust the comparator trigger level V_{trig} such that the comparator output pulse is reduced to 100 ps.
5. Store the counts and sequence numbers through the GUI.
6. Verify that the counts still match the input frequency.

Results:
The CUs can count within the set precision up to 1.65 GHz. Figure 6.5 shows the count-rate for an integration interval of 10 ms in blue and the count-rate modulo 16 in red over time (sequence number in multiples of 10 ms). For count-rates below 170 MHz random values occur in the red plot and above 170 MHz they are all 0 confirming that the functionality of switching to the "divide by 16" counter works.

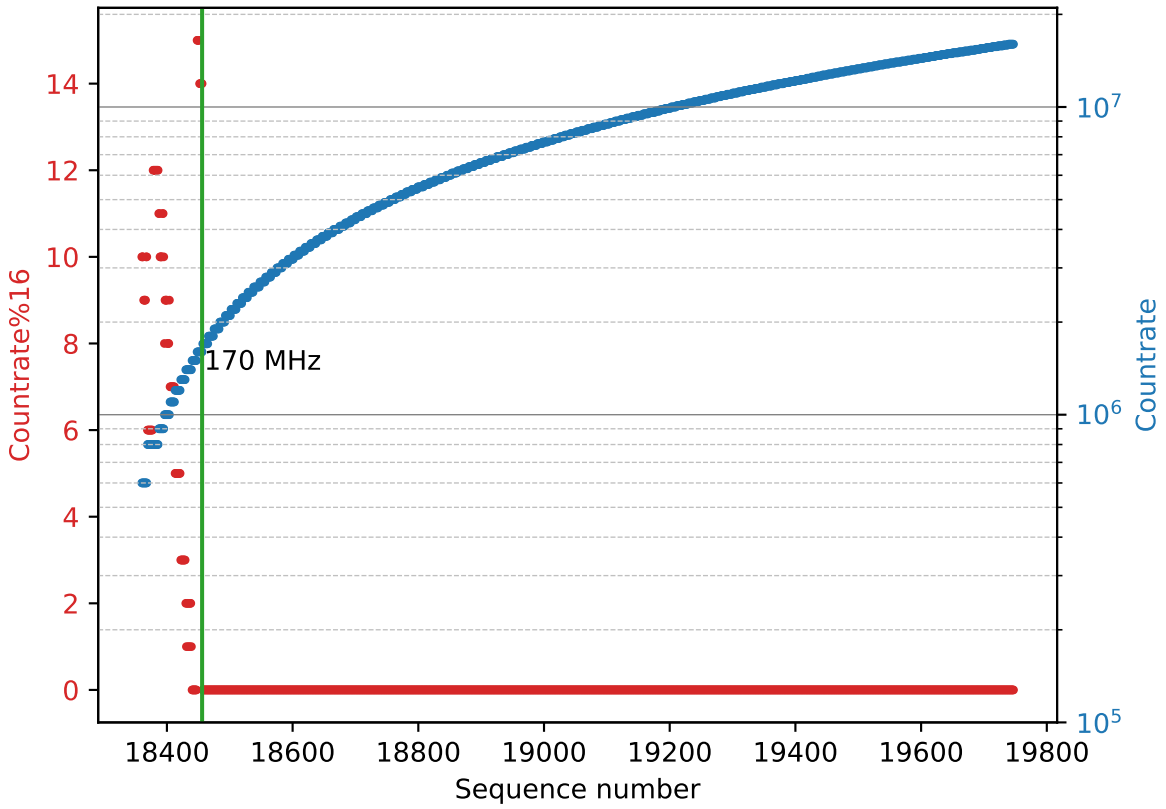


Figure 6.5: Countrate versus sequence number.

To get the pulse of the comparator to its minimal specified output width of 100 ps is quite tough and can not be experimentally shown to work due to the lack of equipment that is needed to measure if the pulses coming from the comparator are actually 100 ps. The pulsewidth of the comparator at an input of 1.65 GHz is maximally 303 ps if the comparator trigger level is precisely in the middle of the sinewave. The counts at this frequency has been verified to be correct.

6.3.2. Count Dead-time

G-REQ 9 The system shall be able to count and send count datapackets without dead-time.

By design, the counters incorporated in the LPC54618 microcontroller must be programmed such that:

1. The two counters increment their values on both rising and falling edge of a signal on one of their input capture pins. This signal is one of the outputs from the frequency division circuit as explained in section 5.2.1 and its design shown in fig. 5.8.
2. On the rising edge of another capture input for both counters, a snapshot of the counter values are stored in registers and the counter values are cleared. This input is connected to the 10 ms integration interval signal and also generates an interrupt.
3. The interrupt routine has to:
   (a) Readout both registers before they are overwritten with the next counts.
   (b) Do a comparison such that the correct count is selected (when the detection rate exceeds 169 MHz).
   (c) Increment a sequence number.
   (d) Send this data over the CAN-bus.

The only possible lost counts might occur at the clearing of the counter during the snapshot event. Since it is unclear from the datasheet how many clock cycles are needed to copy the snapshot of the counter to a register and clear the counter, only an estimation could be given. The estimation for the inner workings of the counters in the LPC54618 is: at the moment a snapshot has to be taken from the counter value, the 32 bit value is copied to a register in 1 clock cycle. Another clock cycle is needed to clear the counter.
Results:
The above mentioned assumption would result in $\frac{2}{180\,\text{MHz}} \approx 11.11\,\text{ns}$ of deadtime. Paraphrasing from the LPC54618 datasheet: "*Since two successive rising edges of the bus clock are used to identify only one edge on the selected capture input, the frequency of the capture input cannot exceed one half of the bus clock.*". This results in missing a maximum of 1 edge of the signal.

For detection rates ranging from 0 Hz up to 169 MHz, a maximum of 1 missed photon detection for each 10 ms. For detection rates ranging from 169 MHz up to 1 GHz, a maximum of 16 photon detections could be missed at a division ratio of 16 for each 10 ms.

6.3.3. Synchronization and integration interval

G-REQ 10 The system shall be able to synchronize the integration interval and start of the counting for all channels.

This requirement has been implemented using 2 distributed signals:

1. A 10 MHz clock that is used by each CU to derive the 10 ms integration interval. Since all CUs derive this from the same clock, the precision and drift of the 10 MHz clock is not critical.
2. A synchronization signal is sampled by the photon counters each interrupt routine. When the signal is asserted (active low), all CUs reset their sequence number.

Procedure:

1. Connect a logic level 10 MHz square wave generator to the backplane clock via the dedicated connector.
2. Initialize at least 2 CUs and measure the integration interval on them with an oscilloscope.
3. Measure the period-difference, Δt, in integration interval signals.
4. Connect the GUI to the MCU such that the data coming from the 2 CUs is shown.
5. Send the synchronize command to the MCU.
6. Verify that the sequence numbers are reset to 0.

Results:
As can be seen in fig. 6.6 a delay in the integration interval between CUs is present of about 45.31 µs. This is due to the fact that the initialization time needed to start each CU might be a bit different hence the integration interval counter starts at a different time. The period difference of the integration interval: Δt has a

standard deviation $\sigma \approx 2.3\,\text{ns}$. If we assume 6σ to be the maximum period difference, this would account for an inaccuracy of 1.4 ppm on a integration interval of 10 ms.

A solution to the delay in the two integration intervals is to connect the synchronize signal to the counter that dictates the integration interval. At assertion of this signal, the counter is cleared. The sequence numbers

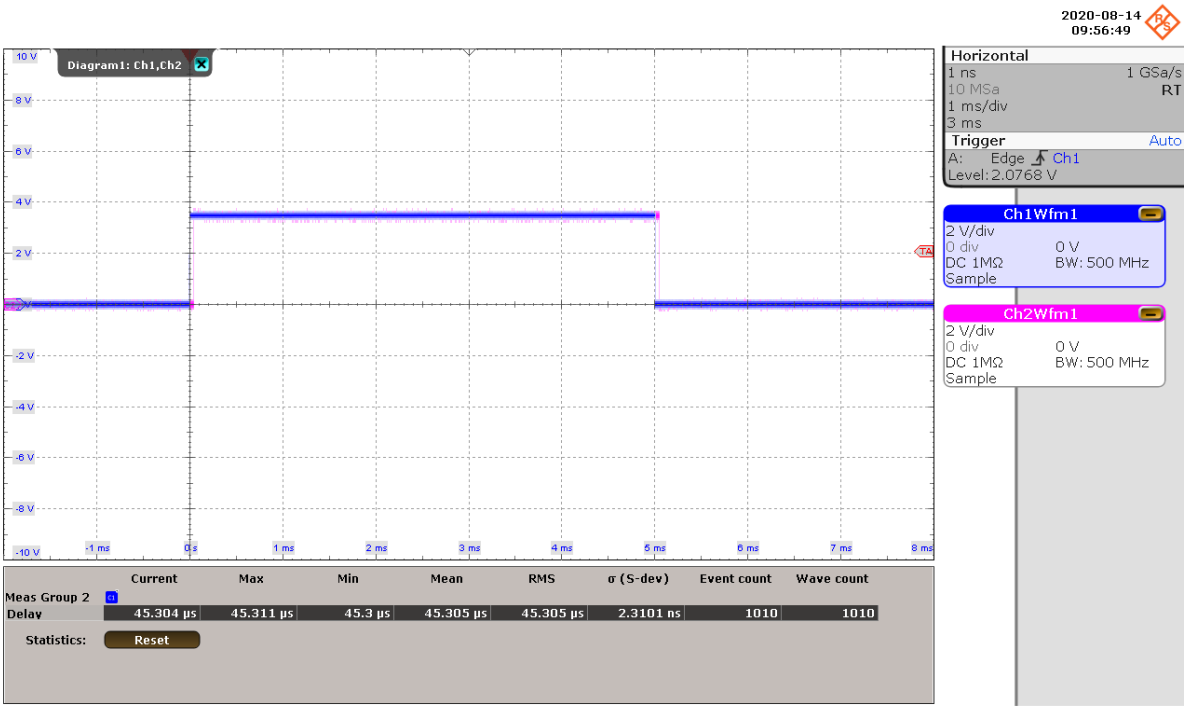


Figure 6.6: Measurement of Δt, the time difference of integration intervals between CUs.

have been verified to be reset to 0 at the assertion of the synchronization signal.

6.3.4. SNSPD Configuration

G-REQ 11 The system shall be able to configure the channels: setting the bias current, comparator trigger level and latch parameters.

Configuration for the following parameters is implemented by commands that can be sent from the GUI to the designated CU:

1. t_{latch}: The time the current is actively brought to 0 at a latch event.
2. f_u: The upper latch frequency, above which the SNSPD is assumed to be latched in oscillation.
3. f_l: The lower latch frequency, below which the SNSPD is assumed to be latched to resistive state.
4. I_{bias}: The bias current.
5. R_{bs} and R_{bp}: The optional bridge resistors. If R_{bp} is set to 0, the software assumes no bridge is in place.
6. R_c: The bypass resistor over the cryogenic amplifier. If R_c is set to 0, the software assumes no cryogenic amplifier is in place.
7. V_{trig}: The comparator trigger level.
8. X_{presc}: The clock prescaler division ratio.

Results:
These commands are defined in appendix B.2, they are all properly interpreted by the CU.

6.3.5. SNSPD Characterization

G-REQ 12 The system shall be able to characterize the detectors, sweeping the bias current and measuring the voltage and count rate.

The sweep functionality is described in section 5.2.8 with its flow diagram in fig. 5.17. The following test procedure is followed to verify this requirement:
Procedure:
First the biascurrent data that is sent back to the GUI must be verified:

1. Setup the system and make sure the GUI can send commands to the CUs.
2. Connect a digital multimeter (Keithley) that can measure in the μA range to the RF-input of the CU that will sweep its bias current.
3. Send the sweep command to the CU and store the sweep-data that is sent back to the GUI, make sure the sweep integration time is set to 2 seconds such that the multimeter can be read out properly.
4. Note the actual measured current in the multimeter for each current incrementation.
5. Compare the measured current with the current sent to the GUI. These currents should differ by at most $\pm 1\mu$A for the test to be a success.

Once this test has been completed, connect an actual SNSPD that has been characterized by the old system and perform the following test:

1. Setup a laser that shines onto the SNSPD with an estimated amount of photons per second of about 200 kCounts/s.
2. Send the sweep command to the CU and store the sweepdata that is sent back to the GUI.
3. Compare the sweep data received in the GUI with the data that was retrieved from the old system. The current at which the SNSPD is assumed to be latch must be equal within $\pm 1\mu$A. The I/count curve should follow the same curve as the old system's curve for this test to be a success.

Results: The CUs are able to perform a sweep based on a command coming from the GUI. However, due to a hardware failure in the CU PCB, graphs have not yet been drawn. It is assumed that at the thesis defense, graphs will be available.

6.3.6. Scalability Global

G-REQ 17 The system shall be able to scale up to at least 60 channels.

Each 12-channel system will act as a server to which the webserver connects to through ethernet as client. Therefore 12-channel systems can be added up to the maximum amount of ethernet ports that is supported by the ethernet switch.
Results:
At the current state of the system, the data connection has not been implemented over ethernet yet. This due to a shortage of time. However, the concept of client-server is a rather well worked out concept in the internet protocol. In addition, the ethernet controller embedded in the LPC54618 microcontroller can handle 100 Mbit/s which allows the sending of all CAN-data (703.2 kbit/s) with ease. We can therefore safely assume that, by design, this scalability requirement will be met in the near future.

6.3.7. Scalability Local

G-REQ 18 The system shall be able to add channels one by one without reconfiguring the software or the interfacing hardware.

The system has been designed in such a way that during initialization, the MCU in each 12-channel system will detect the Channel Units that are connected to its backplane. The Channel Units are requested to

send out one initialization message over CAN with their hardware address encoded in the CAN-ID. The web-interface initializes the 12-channel systems.

When a master 12-channel system and multiple slave 12-channel systems are connected, each subsequent slave toggles its sync output of this signal once more with respect to the amount of toggles it detected on its sync input. This way each slave can fix its IP-address based on the position in the daisychain.

Results:
The CUs add their hardware address properly and are detected by the MCU. Since only a single 12-channel system has been tested, no real validation on the sync toggle could be executed. It would need multiple MCUs to test this feature.

6.3.8. Power distribution

G-REQ 19 The system shall be powered using Power Over Ethernet (POE) that has an output of 52 V and can supply 60 W for each ethernet connection.

Results:
A POE splitter has been used for this thesis. It splits the data from the power supply and converts the 52 V to 24 V. This voltage is used as an input to the PSU. The PSU has been designed to draw at most 60 W and is tested in section 6.1.7.

6.3.9. Housing

G-REQ 16 The system will be mounted in a 19 inch rack using 2U height casings.
G-REQ 20 Each 2U casing can connect to at most 12 detectors.

The Sub-systems as explained in chapter 5 have been carefully designed on PCBs within a set form factor such that they would comply with the requirements **G-REQ 16** and **G-REQ 20**.

Results:
In table 6.3 the height of each part in the complete system is shown. The space left to the top plate is approximately 29 mm which leaves ample space for possible mechanical connections. A frontal picture of the system with 1 complete channel installed is shown in fig. 6.7. The backplane with its 38 cm fits tightly into a 19 inch enclosure which has an inner width of about 40 cm.

Table 6.3: Height of the complete system

Spacers bottom plate	Backplane thickness	PCIe connector	Channel Unit	Space to top plate
10 mm	1.6 mm	8 mm	58 mm	29 mm

The number of CU that can fit into each enclosure is limited by the width of each channel and is therefore at most 12.

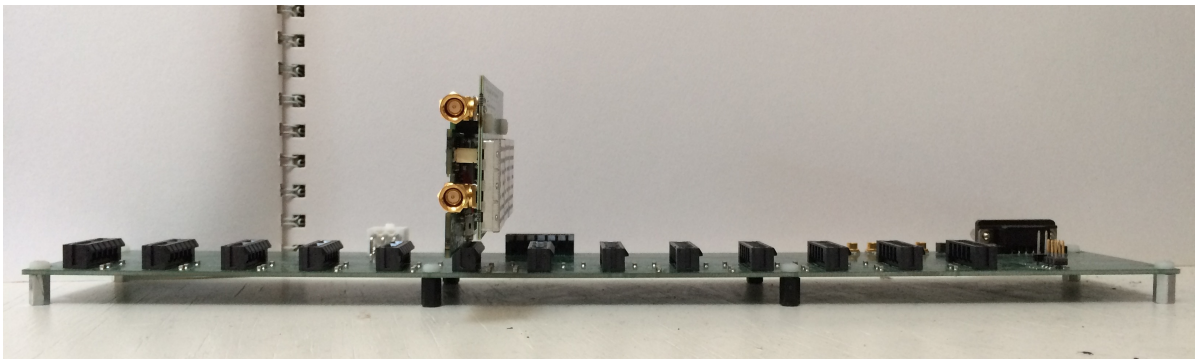


Figure 6.7: Front view of a system

6.4. Final Results

Table 6.4 gives an overview which requirements have been verified.

Table 6.4: Final Results

Requirement	Passed?
G-REQ 1	✓
G-REQ 2	✓
G-REQ 3	✓
G-REQ 4	✓
G-REQ 5	✓
G-REQ 6	✓
G-REQ 7	✓
G-REQ 8	✗
G-REQ 9	✓
G-REQ 10	✓
G-REQ 11	✓
G-REQ 12	✓
G-REQ 13	✓
G-REQ 14	✗
G-REQ 15	✗
G-REQ 16	✓
G-REQ 17	✓
G-REQ 18	✓
G-REQ 19	✓
G-REQ 20	✓

7

Conclusions and Future Work

This chapter will draw conclusions, will propose some possible improvements and will describe future work suggestions.

7.1. Conclusions

Single Quantum produces the worlds most sensitive Superconducting Nanowire Single Photon Detectors and has designed a system that can drive and readout these detectors (the old system). This system has limitations:

1. Its poor scalability due the architecture of the system and due to the high power demand from the old counter circuit.
2. 20 ms of uncounted photon detections each integration interval. This severely limits the speed of characterizing a SNSPDs and the precision of the system.
3. Inability to detect a latched SNSPD in the case where a cryogenic amplifier and a bridge are connected to the SNSPD such that the system is unable to actively quench the SNSPD back to superconducting state.
4. Some components used in the old system have become obsolete.

This thesis has solved the old system's limitations. Thorough analysis of the old system, and creating a functional decomposition based on company requirements, resulted in a new system architecture proposal. This architecture allows for a high flexibility in both the micro- and macro scale.

On the macro scale: dependent on the customer requirements, the amount of detectors can be added virtually without limit. The limiting factors would become:

- Space in routing of the SMA cables from the cryostat to the 12-channel systems and placement of 19 inch cabinets.
- The maximum datarate of the ethernet interface.
- The speed of the webserver to decode and visualize all this data.

On the micro scale: the analog board (RT-Amp) and digital board of a Channel Unit (CU) have a standardized interface such that the individual parts can be developed atomical, i.e., without affecting the design of the other. For instance when a different amplifier design has to be implemented due to a change in the SNSPD configuration, it can simply interface with the already developed digital board without having to adjust the digital board in both hardware or software. Next to that, when a CU turns out to be broken during operation, a new CU can just sent to the customer since installing a CU has become almost as simple as connecting a power plug in a wall socket.

From this architecture, detailed designs have been created such that all set requirements were met. Finally, these designs have been implemented on PCBs and tested. The following results have been measured for the new system:

- **Count rate:** Each channel can count up to 1.65 GHz photon detection rates with a precision of ±1 count below 169 MHz and a precision of ±16 counts above.

- **Integration interval:** A precise 10 MHz external oscillator (for example the OSC10-8101 [1]) that dictates the 10 ms integration interval for all CUs can be connected to the system. This example oscillator has a precision of 10 MHz ± 1 Hz, resulting in an inaccuracy on the integration interval of 10 ppm i.e. ±1 n sec. Introducing a maximum inaccuracy on the maximum 1.65 GHz photon detection rate of ±1.65 counts.

- **Active Quenching:** Each channel can actively quench the SNSPD when latched. This includes configurations in which all cryogenic blocks are installed.

- **Power reduction:** Each added channel requires just 2.9 W from the power budget.

- **Deadtime:** The deadtime is reduced by a factor of 1.800.000 to 11.11 ns, resulting in at most one detection missed every 10 ms.

- **Assembly time:** The assembly time for a 12-channel system is estimated to be about 4 h, 0.33 h per channel. The old 8 channel system is assembled in 14 h, 1.75 h per channel. This reduces the assembly time by a factor of 5.25 per channel, thus resulting in a reduced cost. The costs for a single channel in the an 8 channel old system is estimated at € 430. The cost for a single channel in the new 12-channel system is estimated at € 240, cutting the cost to drive and count SNSPDs by almost half.

The table in section 3.5 is reprinted in table 7.1 containing updated and extended results.

Table 7.1: Comparison based on results

		Old system	New system
1.	Power consumption per channel	5 W	≈ 2.9 W
2.	Active quenching	Partially	Yes
3.	Scalability without reconfiguring HW	×	✓
4.	No dead-time	×	✓
5.	LVDS output of photon detections	×	✓
6.	System cost per channel	€ 430	€ 240

7.2. Improvements

Looking at the resulting system. The following improvements should be implemented:

- **Ethernet:** The ethernet connection to the MCU is the first thing that should be configured such that the throughput of all CAN datapackets for 12 CUs can be tested.

- **Synchronize clock interrupt:** Use the synchronize signal also at a capture input for the 10 ms integration interval counter on each CU. Configure the counter in such a way that when the synchronization signal is asserted, the counter is reset to 0. This way it is ensured that for all CUs, the counters generate the 10 ms interrupt at the same time.

- **Buffer circuit:** The design of a buffer stage that connects the clock signal for the integration interval is required such that the 12 CUs on each 12-channel system sampling the clock do not directly draw current from the clock source. This prevents a possible issue when multiple systems are connected to the same clock source. It might be necessary to add a PLL to this circuit such that any delay introduced by the buffer is mitigated.

- **PSU Cooling:** Apply extra passive cooling for the PSU such that the conversion efficiency could go up.

- **Error Messages:** Implement CU error messages over the CAN-bus to the web-interface.

7.3. Future Work

Some future work is recommended and will be discussed in this section.

- **Housing:** In the future it might be physically possible to add more channels to a single 2U enclosure since the depth of the enclosure has not been completely filled with electronics. A possible "zig-zag" formation of CUs might allow for up to 24 channels in each enclosure. The CAN-interface with the MCU should be able to handle this amount of channels without a problem. The issue would be the power supply. Since each CU needs about 3 W, the MCU needs approximately 2 W and the output of the PSU is now maximally $0.8 \cdot 60\,\text{W} = 48\,\text{W}$ would result in a maximum of 15 channels in each system. POE development is also reaching for higher power supply specifications in the near future, with 100 W already specified in IEEE 802.3bt.

- **Firmware updates:** It would be a great addition for both assembly time reduction and customer service to be able to update firmware on the CUs through the CAN-bus. It would reduce assembly time since after physically installing the CUs to the backplane, a single command from the web-interface to the MCU would start the programming of the firmware to all CUs. This instead of having to connect each of the digital boards of the CU to a programming device.

- **Usage of EEPROM:** Some customers use the system in a so called "free running" mode. In this mode the CUs must be configured just once, according to the SNSPD they interface with. After this, only the analog amplified photon detection outputs are used with a separate time-tagger. The web-interface, and MCU for that matter, are not used. It would be preferable that in this mode of operation, each CU would store its configuration on something like *Electrically Erasable Programmable Read Only Memory* (EEPROM). This way, when the system is power cycled (due to for instance a power outage or maintenance), the CUs would not need to be reconfigured again. Especially, when the number of channels starts to get bigger, this would become a tedious process.

- **Scale:** In more distant future it is required to scale the system to 1000+ channels. For this number of channels it would not be feasible to route out 1000 SMA cables from the cryostat to multiple 19 inch cabinets that contain the systems. These number of channels would probably require that the complete analog amplification, bias and latch detection, and probably some of the digital part of the system is in the cryostat such that only digitized photon detections are sent out of the cryostat. This imposes some heavy requirements on the maximum heat generation of these circuits since cryostat cooling power is limited.

A

Requirements

A.1. General

G-REQ 1 The system shall be able to supply a bias voltage at least between −10 V and 10 V with steps of 1 mV over the bias circuit for each detector, the accuracy must be ±1 mV.

G-REQ 2 The system shall monitor the voltage over the SNSPDs every 10 ms.

G-REQ 3 The system shall be able to automatically unlatch the SNSPDs including those that are equipped with a bridge and/or a cryogenic amplifier circuit.

G-REQ 4 The system shall be able to unlatch the SNSPDs due to frequency latching.

G-REQ 5 The system shall be able to count from 0 Hz to 1 GHz pulses coming from a comparator CML/ECL output with a minimum pulsewidth of 100 ps. The accuracy in the range ≤ 50 MHz is ±1 count. The accuracy for counts between 50 MHz and 1 GHz is ±20.

G-REQ 6 The system shall be able to adjust the trigger level of the comparators between 0 V and 2.25 V with at least 12 bit resolution.

G-REQ 7 Each added channel (SNSPD with counting, bias and amplification electronics) will require at most an additional 3 W.

G-REQ 8 The system shall have an ethernet connection with the web-interface.

G-REQ 9 The system shall be able to count and send count datapackets without dead-time.

G-REQ 10 The system shall be able to synchronize the integration interval and start of the counting for all channels.

G-REQ 11 The system shall be able to configure the channels: setting the bias current, comparator trigger level and latch parameters.

G-REQ 12 The system shall be able to characterize the detectors, sweeping the bias current and measuring the voltage and count rate.

G-REQ 13 The system shall output digitized photon detections based on the LVDS physical interface.

G-REQ 14 The system shall be able to supply the current of the temperature-diode which monitors the temperature in the cryostat with a constant current of 10 μA. The design of this circuit will be identical to the circuit currently implemented.

G-REQ 15 The system shall be able to read the temperature-diode voltage and send this to the web-interface.

G-REQ 16 The system will be mounted in a 19 inch rack using 2U height casings.

G-REQ 17 The system shall be able to scale up to at least 60 channels.

G-REQ 18 The system shall be able to add channels one by one without reconfiguring the software or the interfacing hardware.

G-REQ 19 The system shall be powered using Power Over Ethernet (POE) that has an output of 52 V and can supply 60 W for each ethernet connection.

G-REQ 20 Each 2U casing can connect to at most 12 detectors.

B

Data Packages

B.1. MCU to Web-interface

JSON Format

```
{
"sequenceNumber"  : [x0,x1,x2,x3,x4,x5,x6,x7,x8,x9,x10,x11],
"countValue"      : [cnt0,cnt1,cnt2,cnt3,cnt4,cnt5,cnt6,cnt7,cnt8,cnt9,cnt10,cnt11],
"biasCurrent"     : [bias0,bias1,bias2,bias3,bias4,bias5,bias6,bias7,bias8,bias9,bias10,bias11],
"monitorVoltage"  : [mon0,mon1,mon2,mon3,mon4,mon5,mon6,mon7,mon8,mon9,mon10,mon11],
"triggerLvl"      : [trg0,trg1,trg2,trg3,trg4,trg5,trg6,trg7,trg8,trg9,trg10,trg11],
"unlatchTime"     : [t_l0,t_l1,t_l2,t_l3,t_l4,t_l5,t_l6,t_l7,t_l8,t_l9,t_l10,t_l11],
"freqLowerLatch"  : [f_l0,f_l1,f_l2,f_l3,f_l4,f_l5,f_l6,f_l7,f_l8,f_l9,f_l10,f_l11],
"freqUpperLatch"  : [f_u0,f_u1,f_u2,f_u3,f_u4,f_u5,f_u6,f_u7,f_u8,f_u9,f_u10,f_u11],
"Rc"              : [Rc0,Rc1,Rc2,Rc3,Rc4,Rc5,Rc6,Rc7,Rc8,Rc9,Rc10,Rc11],
"Rbs"             : [Rbs0,Rbs1,Rbs2,Rbs3,Rbs4,Rbs5,Rbs6,Rbs7,Rbs8,Rbs9,Rbs10,Rbs11],
"Rbp"             : [Rbp0,Rbp1,Rbp2,Rbp3,Rbp4,Rbp5,Rbp6,Rbp7,Rbp8,Rbp9,Rbp10,Rbp11],
"prescaleSetting" : [prsc0,prsc1,prsc2,prsc3,prsc4,prsc5,prsc6,prsc7,prsc8,prsc9,prsc10,prsc11],
"channelAddress"  : [0,1,2,3,4,5,6,7,8,9,10,11],
"driveNumber"     : y
}

x:
- unsigned 16 bit integer ranging from 0-65536 with wrap to 0

cnt:
- unsigned 24 bit integer ranging from 0 - 10^7

bias:
- The set bias current through the SNSPD in signed 16 bit integer ranging from
  100 uA < bias < 100 uA in fixed point notation: Q6.9

mon:
- The calculated voltage over the SNSPD in signed 16 bit integer ranging from
  -10 V < mon < 10 V in fixed point notation: Q4.11

trg:
- The set trigger level in unsigned 16 bit integer ranging from
  0V < trigger < 2.5 V in fixed point notation: Q2.13

t_l:
- The unlatch time in unsigned 16 bit integer ranging from
  (0s < t_l < 1000)*10ms (steps of 10 ms).

f_l:
- The lower frequency latching parameter in unsigned 16 bit integer ranging from
  (0 counts < f_l < 65536)*160 counts. (0 to 10^7 counts)

f_u:
- The upper frequency latching parameter in unsigned 16 bit integer ranging from
  (0 counts < f_l < 65536)*1600 counts. (0 to 10^9 counts)
```

```
Rc:
- The bypass resistor value over the cryogenic amplifier unsigned 16 bit integer ranging from
  (0 Ohm < Rc < 65536 Ohm)*10 (steps of 10 Ohm)

Rbs:
- The resistor value in series with the SNSPD unsigned 16 bit integer ranging from
  (0 Ohm < Rbs < 65536 Ohm)

Rbp:
- The resistor value in parallel with the SNSPD unsigned 16 bit integer ranging from
  (0 Ohm < Rbp < 65536 Ohm)

prsc:
- The prescaler setting in unsigned 8 bit integer ranging from
  (0 < prsc < 255) (can be either 2, 4, 8, 16, 32, 64 or 128)

address:
- unsigned 4 bit value ranging from 0 to 12 holding the channel address

y:
- The MCU number for multiple drivers of 12 channels in 4 bit.
  0 if only 1 driver is connected.
```

B.2. MCU to CU

Function field value:	Description:
0x00	*Update Comparator Trigger level*
0x01	*Update Bias current*
0x02	*Update Prescaler settings*
0x03	*Sweep*
0x04	*Abort Sweep*
0x05	*Update SNSPD latching parameters*
0x06	*Update Cryogenic and/or Bridge resistor values*

Figure B.1: Function field specification.

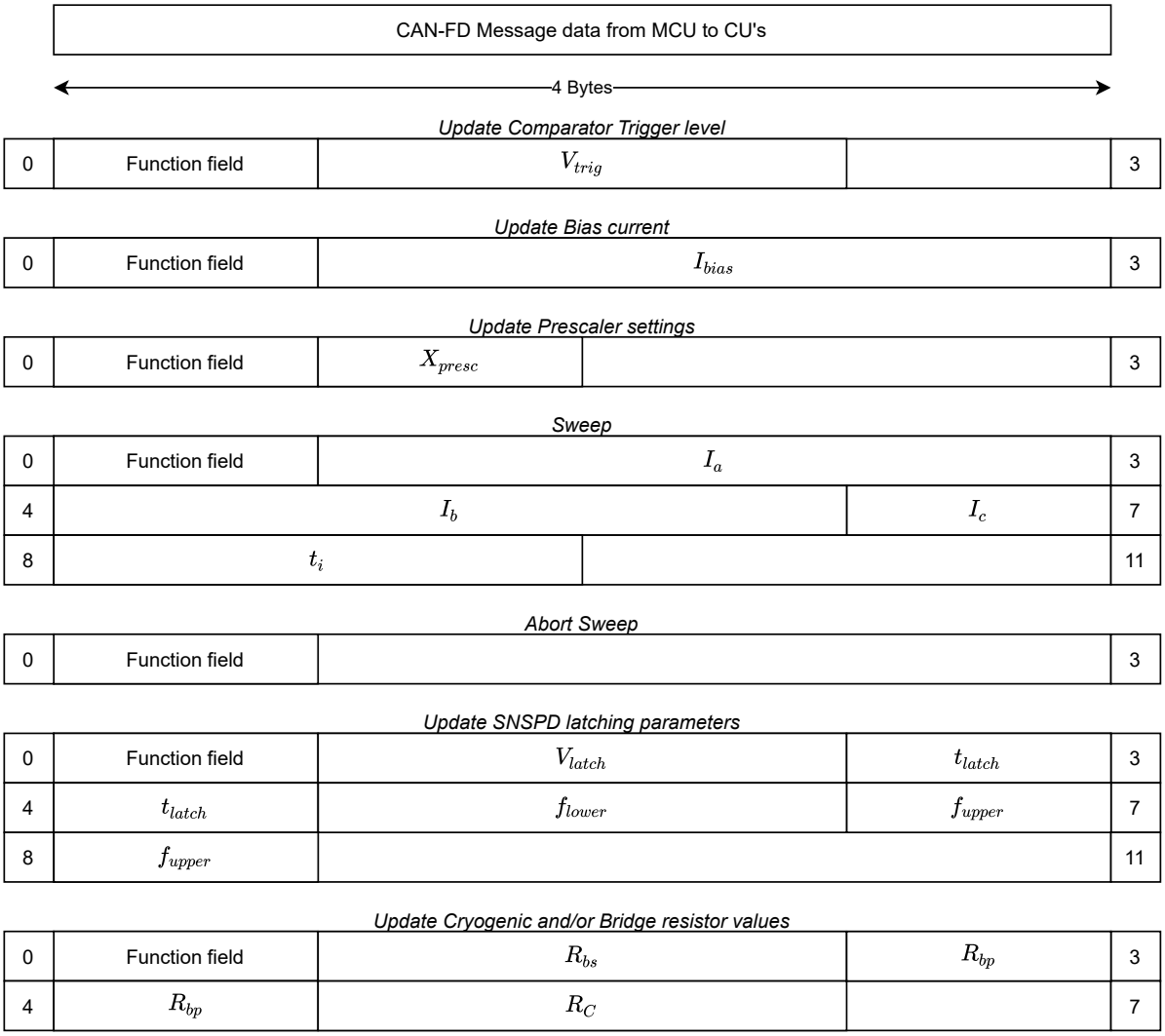


Figure B.2: Data package from MCU to CU.

B.3. CU to MCU

CAN-FD Message data from CU's to MCU

4 Bytes

0	Count		Sequence number	3
4	Sequence number	V_{mon}		7
8	I_{bias}		V_{trig}	11
12	V_{trig}	V_{latch}	t_{latch}	15
16	t_{latch}	f_{lower}	f_{upper}	19
20	f_{upper}	R_{bs}	R_{bp}	23
24	R_{bp}	R_C		27
28	X_{presc}	State		31
32				35
36				39
40				43
44				47
48				51
52				55
56				59
60				53

Figure B.3: Data package from CU to MCU.

- Count: The 24 bit count rate in 10 ms
- Sequence number: The time stamp such that the web-interface can plot the counts for all CUs at the same time. Also such that the web-interface can sum over multiple counts to elongate the integration interval.
- V_{mon}: The monitored voltage over the SNSPD
- I_{bias}: The bias current through the SNSPD
- V_{trig}: The comparator trigger level
- V_{latch}: The voltage setting that helps the detection of a latched detector.
- t_{latch}: The time needed to set the current to 0 at a latched detector event.
- f_{lower}: The lower frequency bound, if the count is below this value, the CU assumes the SNSPD is latched.
- f_{upper}: The upper frequency bound, if the count is above this value, the CU assumes the SNSPD is latched.
- R_{bs}: The series resistance in the optional bridge.

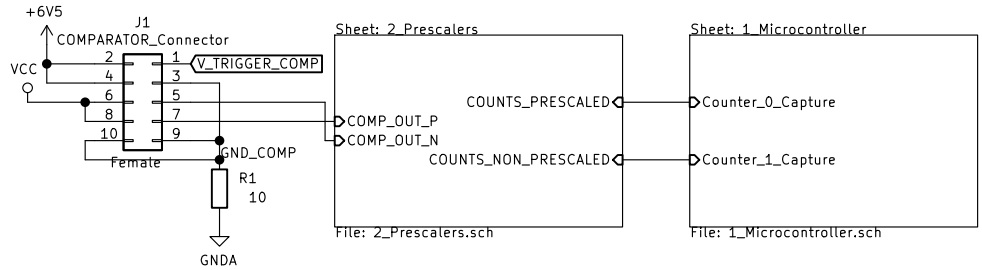
- R_{bp}: The parallel resistance in the optional bridge.
- R_c: The bypass resistor in the optional cryogenic amplifier.
- X_{presc}: The prescaler/division ratio.
- State: The state of the CU. May be Init 0, Normal 1, or Sweep 2.

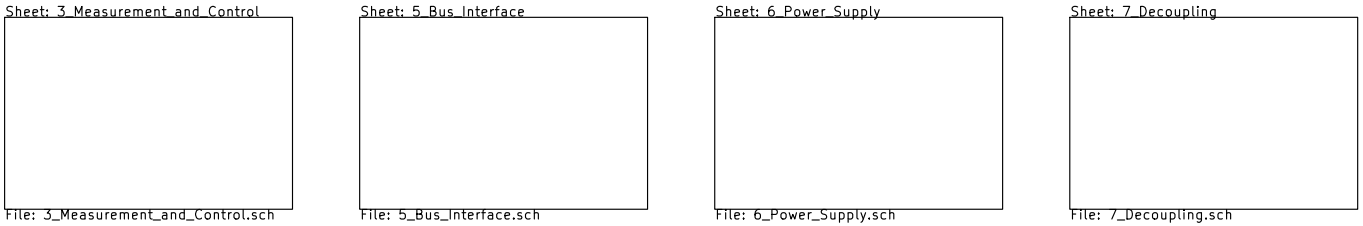
C

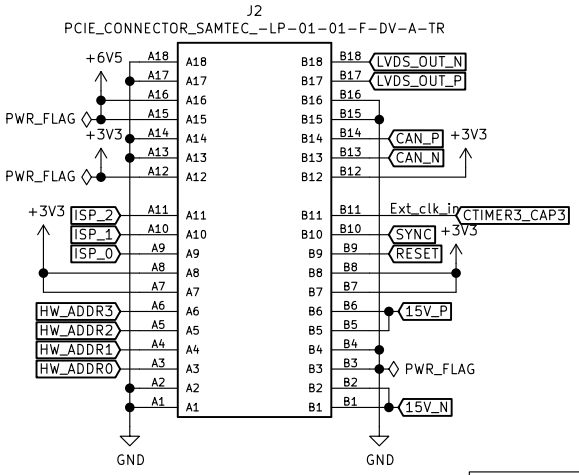
Schematics

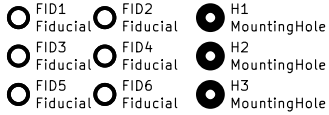
This appendix will hold all schematics that have been drawn during this thesis.

C.1. Channel Unit







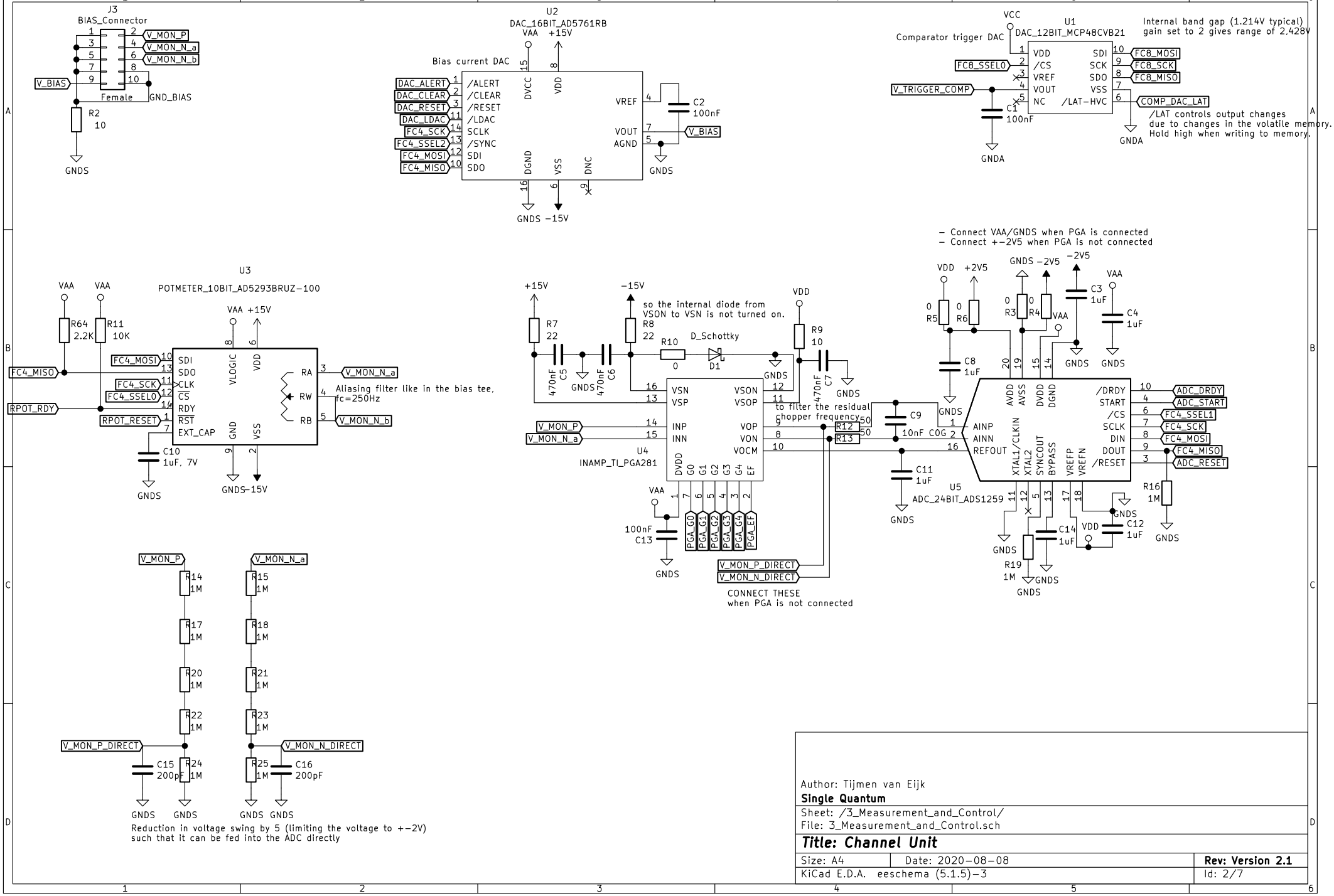


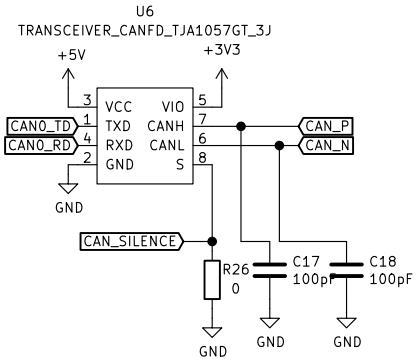
Author: Tijmen van Eijk
Single Quantum

Sheet: /
File: SNSPD_Driver.sch

Title: Channel Unit

Size: A4	Date: 2020-08-08	**Rev: Version 2.1**
KiCad E.D.A. eeschema (5.1.5)-3		Id: 1/7


J3
BIAS_Connector
V_MON_P
V_MON_N_a
V_MON_N_b
V_BIAS
GND_BIAS
Female
R2
10
GNDS
U2
DAC_16BIT_AD5761RB
VAA +15V
Bias current DAC
DAC_ALERT
DAC_CLEAR
DAC_RESET
DAC_LDAC
FC4_SCK
FC4_SSEL2
FC4_MOSI
FC4_MISO
/ALERT
/CLEAR
/RESET
/LDAC
SCLK
/SYNC
SDI
SDO
DVCC
VDD
DGND
VSS
DNC
VREF
VOUT
AGND
C2
100nF
GNDS −15V
VCC
U1
DAC_12BIT_MCP48CVB21
Comparator trigger DAC
Internal band gap (1.214V typical)
gain set to 2 gives range of 2.428V
FC8_SSEL0
V_TRIGGER_COMP
C1
100nF
GNDA
VDD
/CS
VREF
VOUT
NC
/LAT−HVC
SDI
SCK
SDO
VSS
FC8_MOSI
FC8_SCK
FC8_MISO
COMP_DAC_LAT
/LAT controls output changes
due to changes in the volatile memory.
Hold high when writing to memory.
U3
POTMETER_10BIT_AD5293BRUZ−100
VAA
R64
2.2K
R11
10K
FC4_MISO
FC4_MOSI
FC4_SCK
FC4_SSEL0
RPOT_RDY
RPOT_RESET
SDI
SDO
CLK
CS
RDY
RST
EXT_CAP
VLOGIC
VDD
GND
VSS
RA
RW
RB
V_MON_N_a
V_MON_N_b
Aliasing filter like in the bias tee,
fc=250Hz
C10
1uF, 7V
GNDS
GNDS −15V
+15V
−15V
R7
22
R8
22
R10
0
D_Schottky
D1
so the internal diode from
VSON to VSN is not turned on.
470nF
C5
C6
R9
10
C7
to filter the residual
chopper frequency
U4
INAMP_TI_PGA281
VSN
VSP
INP
INN
VSON
VSOP
VOP
VON
VOCM
DVDD
G0
G1
G2
G3
G4
EF
PGA_G0
PGA_G1
PGA_G2
PGA_G3
PGA_G4
PGA_EF
C13
100nF
V_MON_P_DIRECT
V_MON_N_DIRECT
CONNECT THESE
when PGA is not connected
− Connect VAA/GNDS when PGA is connected
− Connect +−2V5 when PGA is not connected
VDD
+2V5
GNDS −2V5
−2V5
R5
R6
R3
R4
C3
1uF
C4
1uF
C8
1uF
C9
10nF COG
C11
1uF
U5
ADC_24BIT_ADS1259
AINP
AINN
REFOUT
AVDD
AVSS
DVDD
DGND
XTAL1/CLKIN
XTAL2
SYNCOUT
BYPASS
VREFP
VREFN
/DRDY
START
/CS
SCLK
DIN
DOUT
/RESET
ADC_DRDY
ADC_START
FC4_SSEL1
FC4_SCK
FC4_MOSI
FC4_MISO
ADC_RESET
R16
1M
C14
1uF
C12
1uF
R19
1M
V_MON_P
V_MON_N_a
R14
1M
R15
1M
R17
1M
R18
1M
R20
1M
R21
1M
R22
1M
R23
1M
V_MON_P_DIRECT
V_MON_N_DIRECT
C15
200pF
R24
1M
R25
1M
C16
200pF
GNDS
Reduction in voltage swing by 5 (limiting the voltage to +−2V)
such that it can be fed into the ADC directly
Author: Tijmen van Eijk
Single Quantum
Sheet: /3_Measurement_and_Control/
File: 3_Measurement_and_Control.sch
Title: Channel Unit
Size: A4
Date: 2020−08−08
Rev: Version 2.1
KiCad E.D.A. eeschema (5.1.5)−3
Id: 2/7

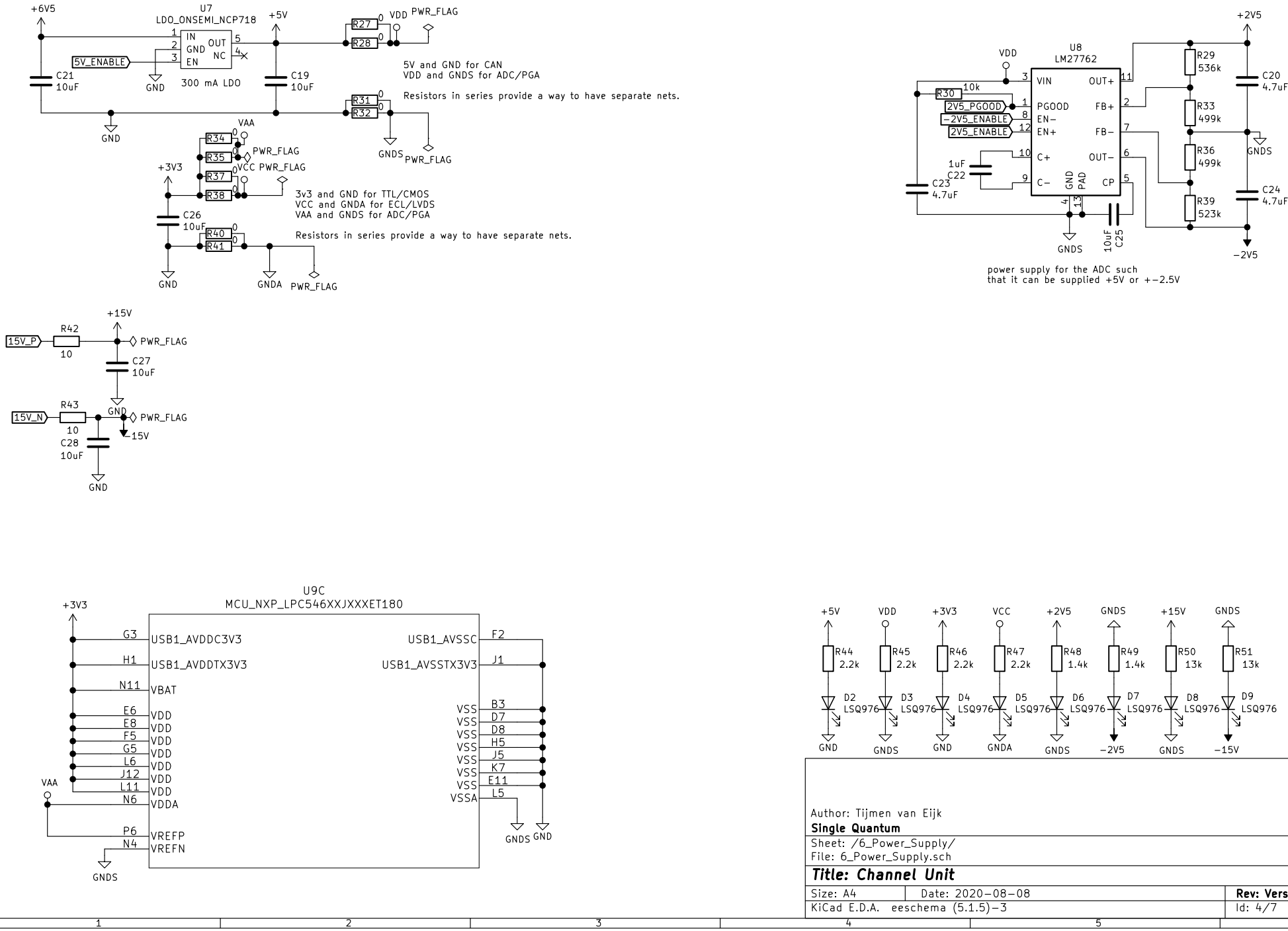


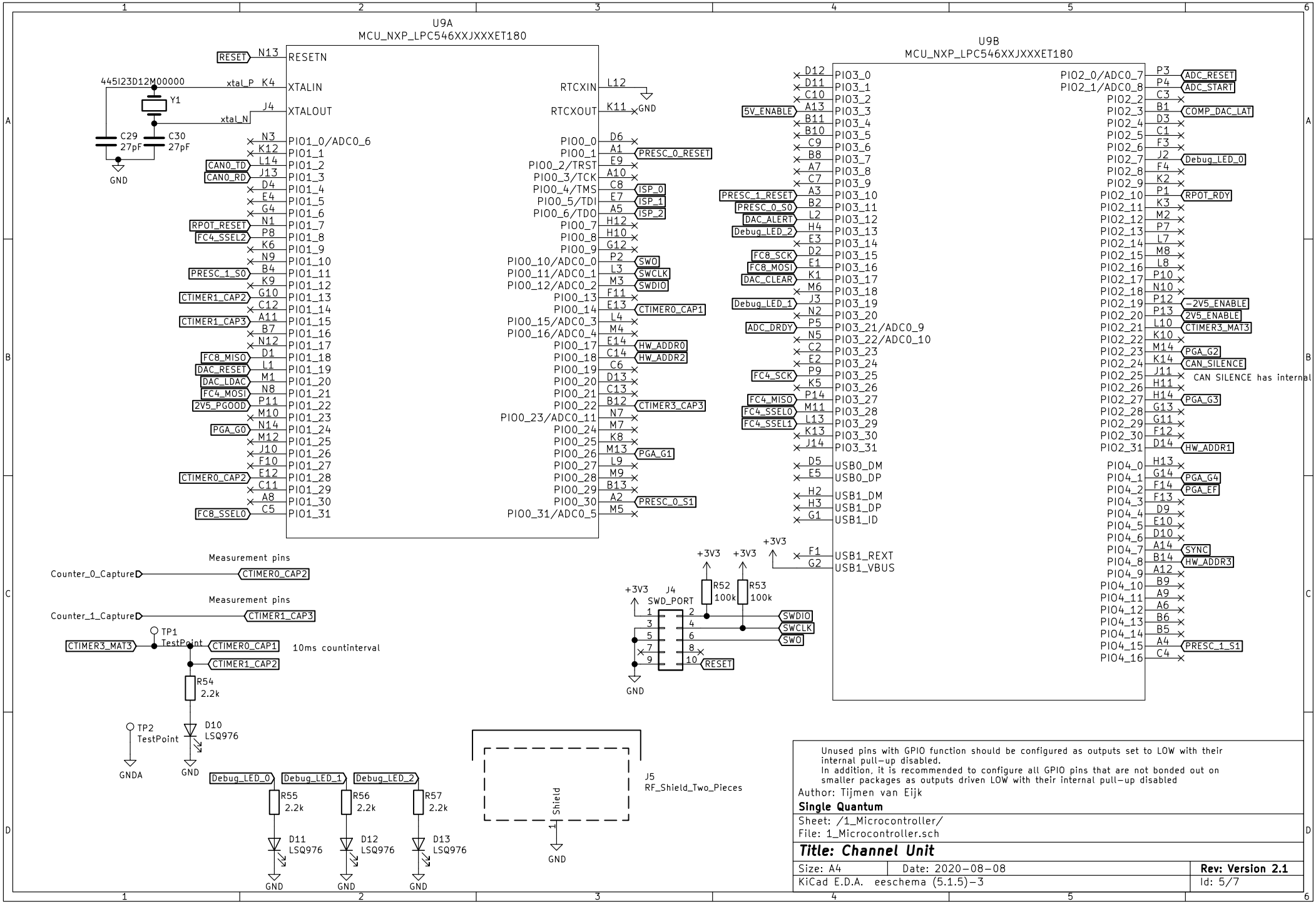
Author: Tijmen van Eijk
Single Quantum

Sheet: /5_Bus_Interface/
File: 5_Bus_Interface.sch

Title: Channel Unit

Size: A4	Date: 2020-08-08	**Rev: Version 2.1**
KiCad E.D.A. eeschema (5.1.5)-3		Id: 3/7


+6V5
U7
LDO_ONSEMI_NCP718
IN
GND
EN
OUT
NC
5V_ENABLE
GND
300 mA LDO
+5V
C21
10uF
C19
10uF
R27
R28
VDD
PWR_FLAG
5V and GND for CAN
VDD and GNDS for ADC/PGA
R31
R32
Resistors in series provide a way to have separate nets.
GNDS
PWR_FLAG
VAA
R34
R35
PWR_FLAG
+3V3
R37
VCC PWR_FLAG
R38
3v3 and GND for TTL/CMOS
VCC and GNDA for ECL/LVDS
VAA and GNDS for ADC/PGA
C26
10uF
R40
R41
Resistors in series provide a way to have separate nets.
GND
GNDA
PWR_FLAG
+2V5
U8
LM27762
VDD
VIN
OUT+
R30
10k
2V5_PGOOD
PGOOD
FB+
−2V5_ENABLE
EN−
FB−
2V5_ENABLE
EN+
C+
OUT−
1uF
C22
C23
4.7uF
C−
GND
PAD
CP
R29
536k
C20
4.7uF
R33
499k
R36
499k
GNDS
C24
4.7uF
R39
523k
GNDS
10uF
C25
−2V5
power supply for the ADC such
that it can be supplied +5V or +−2.5V
+15V
15V_P
R42
10
PWR_FLAG
C27
10uF
GND
15V_N
R43
10
PWR_FLAG
−15V
C28
10uF
GND
U9C
MCU_NXP_LPC546XXJXXXET180
+3V3
G3
USB1_AVDDC3V3
H1
USB1_AVDDTX3V3
N11
VBAT
E6
E8
F5
G5
L6
J12
L11
VDD
N6
VDDA
VAA
P6
VREFP
N4
VREFN
GNDS
USB1_AVSSC
F2
USB1_AVSSTX3V3
J1
VSS
B3
D7
D8
H5
J5
K7
E11
L5
VSSA
GNDS
GND
+5V
VDD
+3V3
VCC
+2V5
GNDS
+15V
GNDS
R44
2.2k
R45
2.2k
R46
2.2k
R47
2.2k
R48
1.4k
R49
1.4k
R50
13k
R51
13k
D2
LSQ976
D3
LSQ976
D4
LSQ976
D5
LSQ976
D6
LSQ976
D7
LSQ976
D8
LSQ976
D9
LSQ976
GND
GNDS
GND
GNDA
GNDS
−2V5
GNDS
−15V
Author: Tijmen van Eijk
Single Quantum
Sheet: /6_Power_Supply/
File: 6_Power_Supply.sch
Title: Channel Unit
Size: A4
Date: 2020−08−08
Rev: Version 2.1
KiCad E.D.A. eeschema (5.1.5)−3
Id: 4/7



Unused pins with GPIO function should be configured as outputs set to LOW with their internal pull-up disabled.
In addition, it is recommended to configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled

Author: Tijmen van Eijk

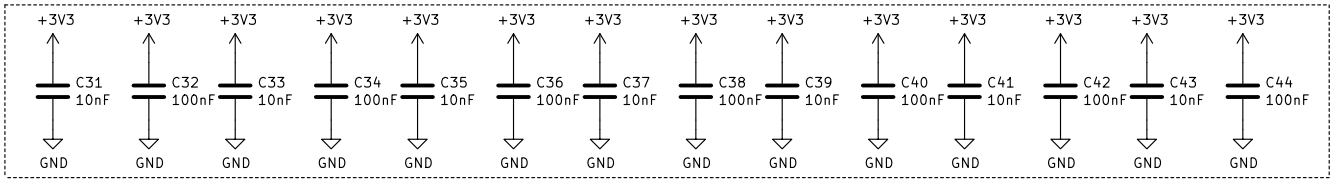
Single Quantum

Sheet: /1_Microcontroller/
File: 1_Microcontroller.sch

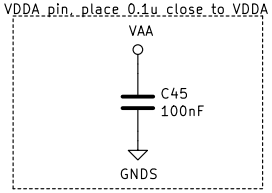
Title: Channel Unit

Size: A4	Date: 2020-08-08	**Rev: Version 2.1**
KiCad E.D.A. eeschema (5.1.5)-3		Id: 5/7

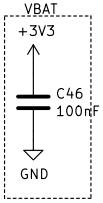
VDD Pins uC



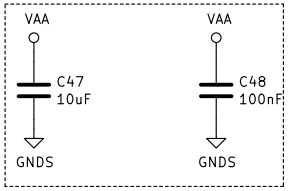
VDDA pin, place 0.1u close to VDDA



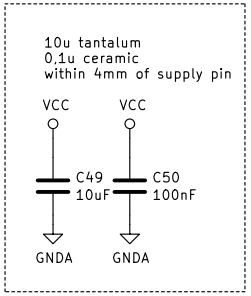
VBAT



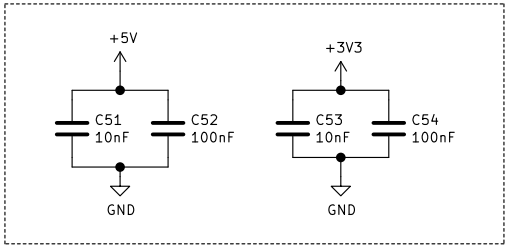
VREFP PIN, PLACE 0.1U close to VREFN



DAC: Comparator trigger level

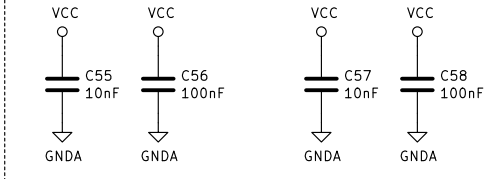


CAN Interface

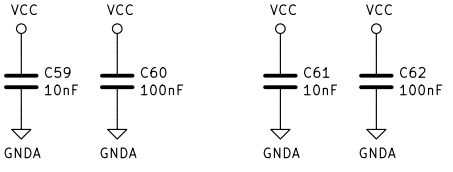


PRESCALER 0

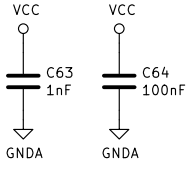
SY89873L Ceramic decouple caps, Smallest C closest to VCC pin.
Exposed pad connected to GND



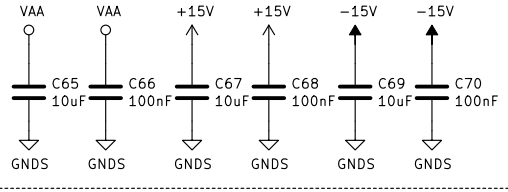
PRESCALER 1



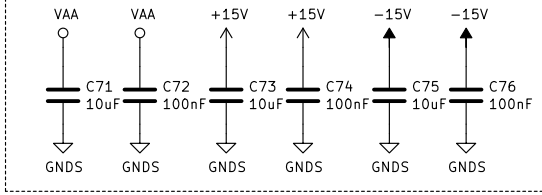
LVDS to CMOS translator Ceramic caps,
Smallest C closest to VCC pin.



Potentio meter: AD5293BRUZ-100



DAC 16Bit: AD5761RB

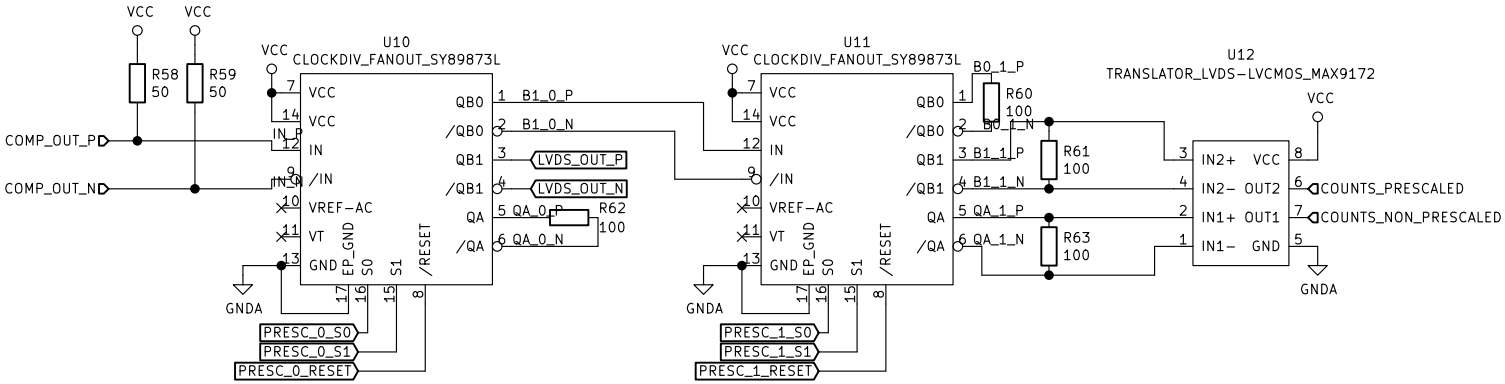


Author: Tijmen van Eijk
Single Quantum

Sheet: /7_Decoupling/
File: 7_Decoupling.sch

Title: Channel Unit

Size: A4	Date: 2020-08-08	**Rev: Version 2.1**
KiCad E.D.A. eeschema (5.1.5)-3		Id: 6/7



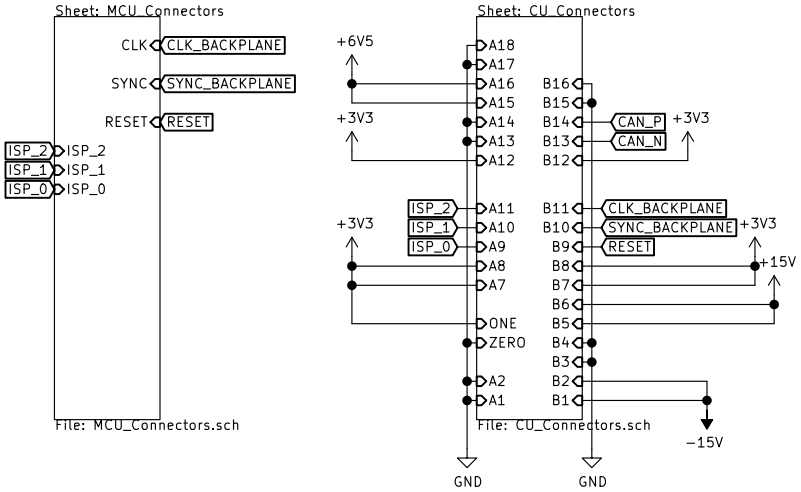
Author: Tijmen van Eijk
Single Quantum

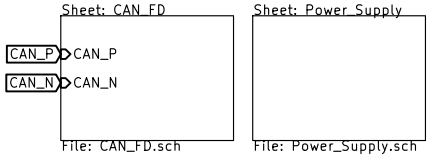
Sheet: /2_Prescalers/
File: 2_Prescalers.sch

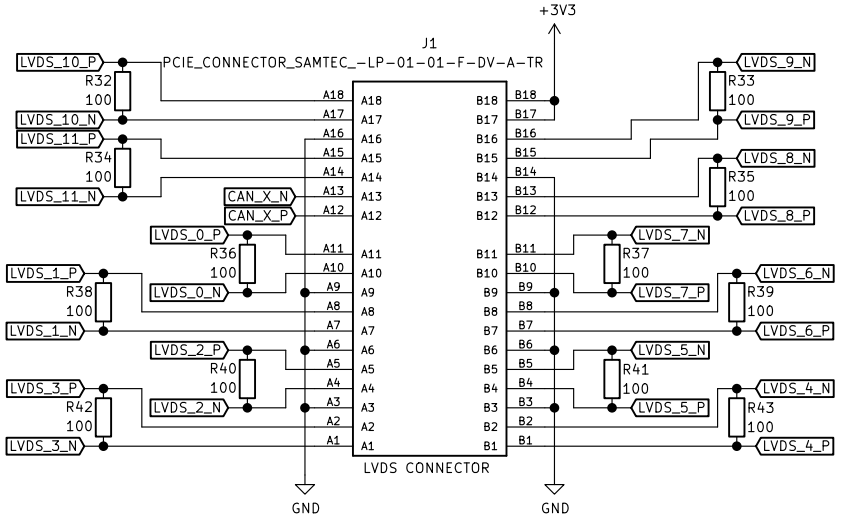
Title: Channel Unit

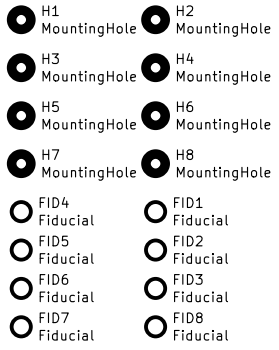
Size: A4	Date: 2020-08-08	**Rev: Version 2.1**
KiCad E.D.A. eeschema (5.1.5)-3		Id: 7/7

C.2. Backplane







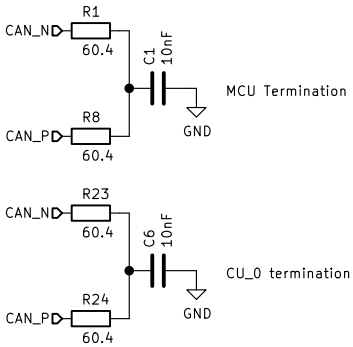


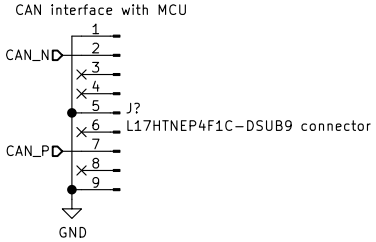
Author: Tijmen van Eijk
Single Quantum

Sheet: /
File: Backplane_v1.sch

Title: Backplane

Size: A4	Date: 2020-08-14	**Rev: 1.1**
KiCad E.D.A. kicad (5.1.4)-1		Id: 1/5



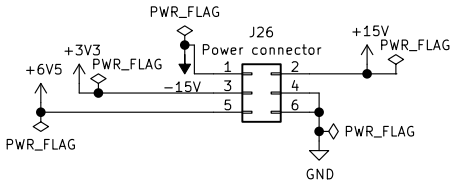


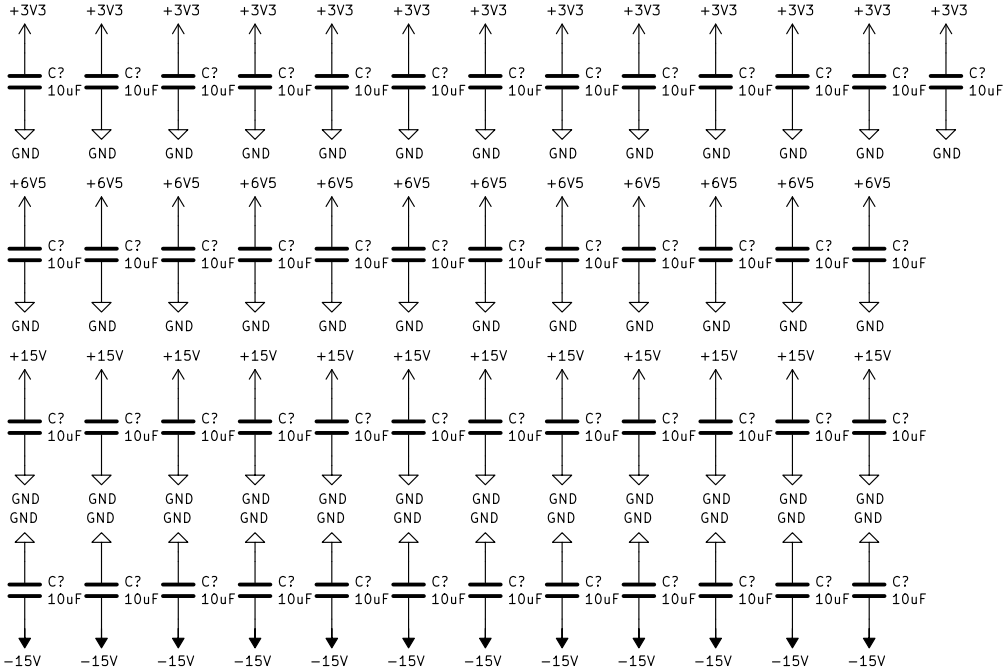
Author: Tijmen van Eijk
Single Quantum

Sheet: /CAN_FD/
File: CAN_FD.sch

Title: Backplane

Size: A4	Date: 2020-08-14	**Rev: 1.1**
KiCad E.D.A. kicad (5.1.4)-1		Id: 2/5



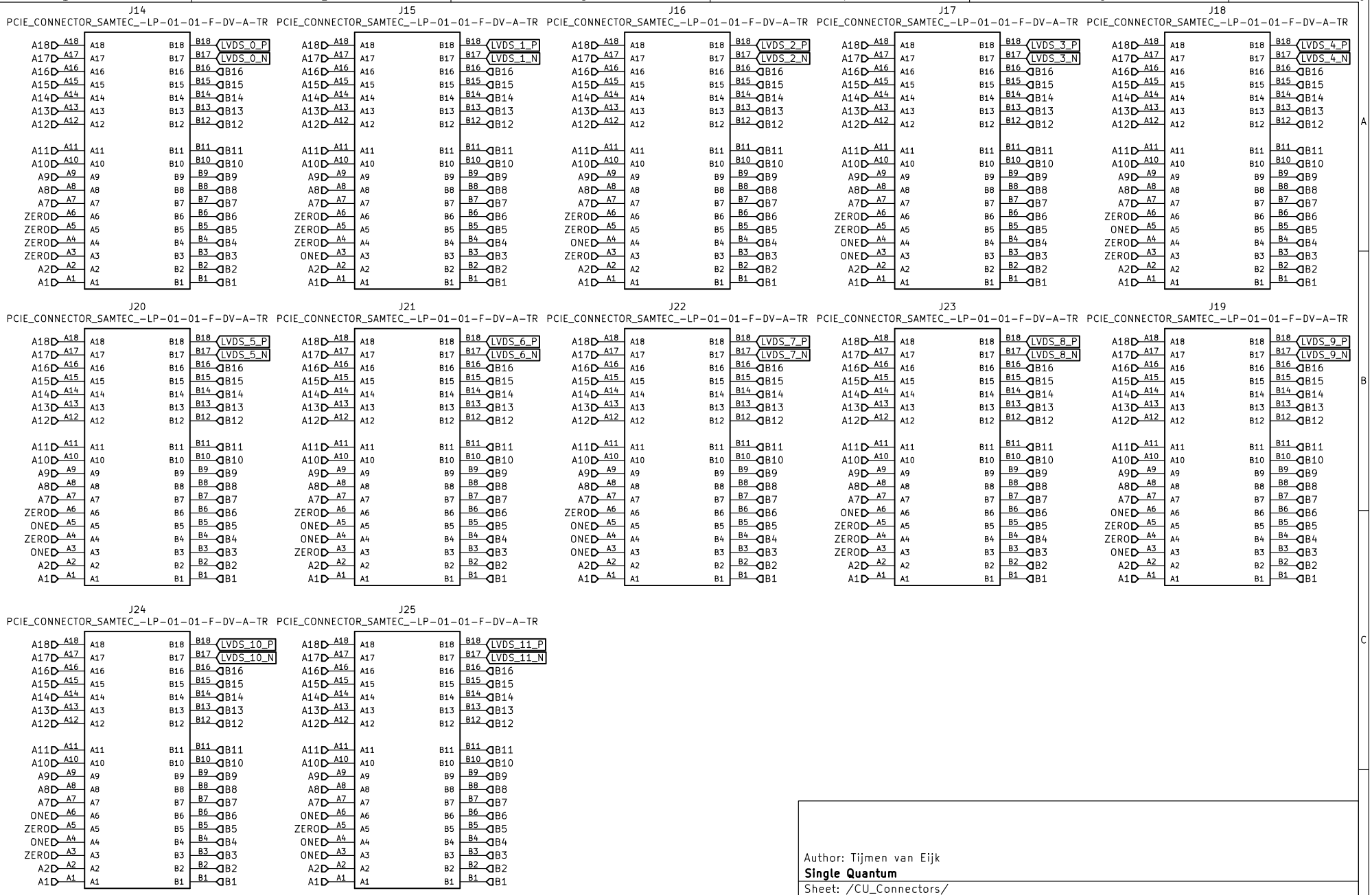


Author: Tijmen van Eijk
Single Quantum

Sheet: /Power_Supply/
File: Power_Supply.sch

Title: Backplane

Size: A4	Date: 2020-08-14	**Rev: 1.1**
KiCad E.D.A. kicad (5.1.4)-1		Id: 3/5



Author: Tijmen van Eijk

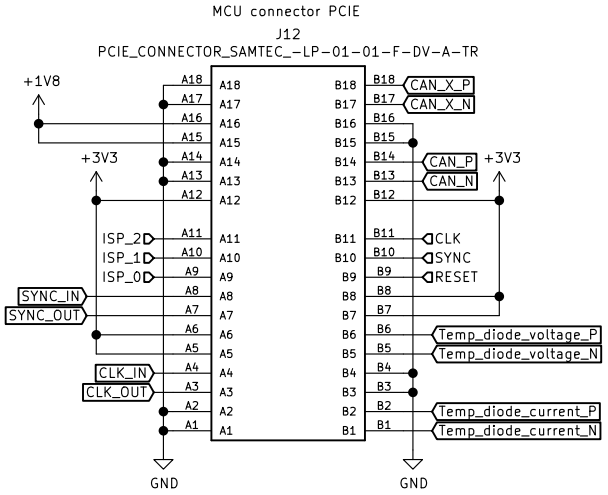
Single Quantum

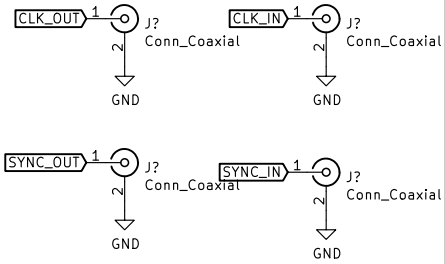
Sheet: /CU_Connectors/

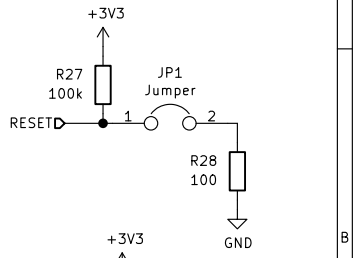
File: CU_Connectors.sch

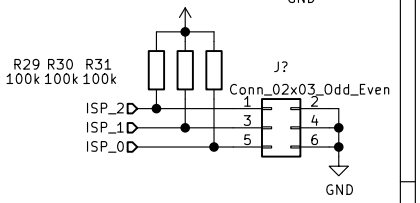
Title: Backplane

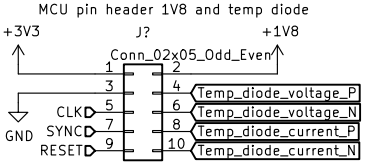
Size: A4	Date: 2020-08-14	**Rev: 1.1**
KiCad E.D.A. kicad (5.1.4)-1		Id: 4/5











Author: Tijmen van Eijk
Single Quantum

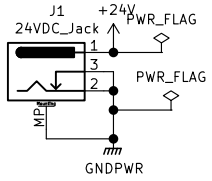
Sheet: /MCU_Connectors/
File: MCU_Connectors.sch

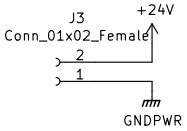
Title: Backplane

Size: A4	Date: 2020-08-14	**Rev: 1.1**
KiCad E.D.A. kicad (5.1.4)-1		Id: 5/5

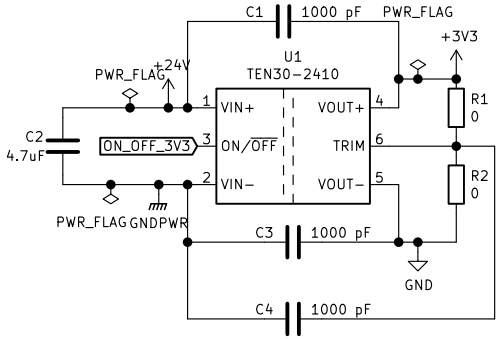
C.3. Power Supply Unit

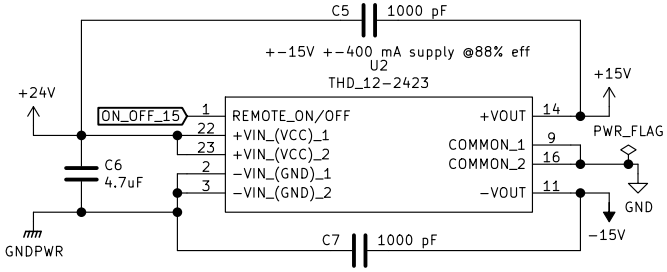
2.5mm inner, 5,5mm outer. 9,25 mm length

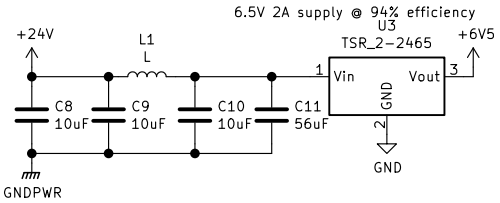




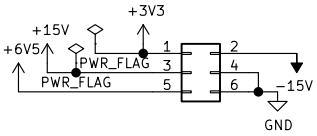
3V3 8A @ 87% efficiency
0 Ohm resistors in place if trimming is needed
(6.8K to VOUT− for +5%)(8.2K to VOUT+ for −5%)

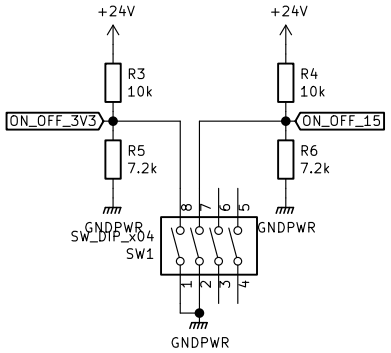




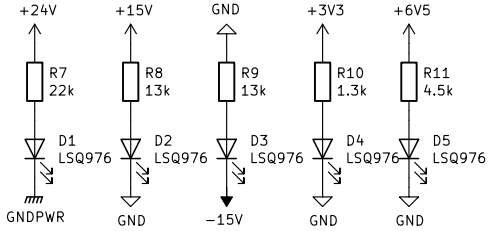


J2
Conn_02x03_Odd_Even





Create 10V when not switched, 0V when switched on



H1 MountingHole
H2 MountingHole
H3 MountingHole
H4 MountingHole

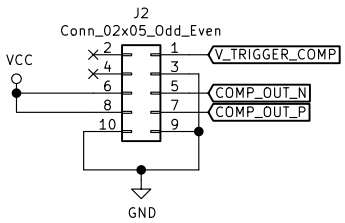
FID1 Fiducial
FID2 Fiducial
FID3 Fiducial
FID4 Fiducial
FID5 Fiducial
FID6 Fiducial

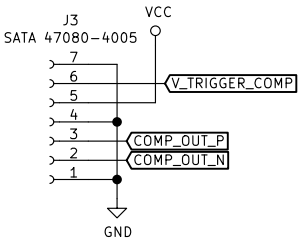
Author: Tijmen van Eijk
Single Quantum
Sheet: /
File: PSU.sch

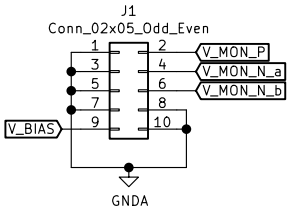
Title: Power Supply Unit (PSU)

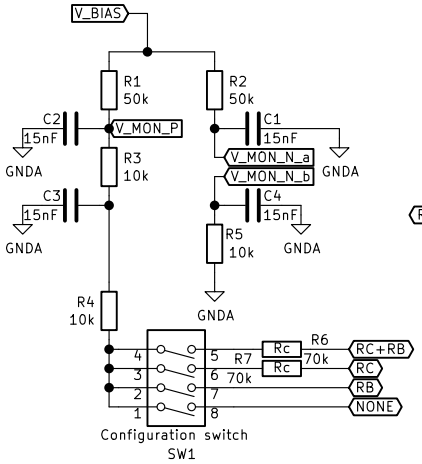
Size: A4	Date: 2020-08-14	**Rev: 1.1**
KiCad E.D.A. kicad (5.1.4)-1		Id: 1/1

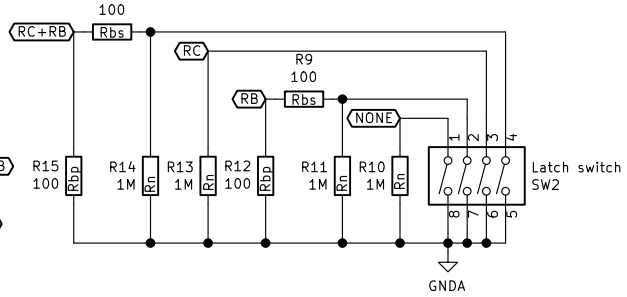
C.4. Testboard for Channel Unit

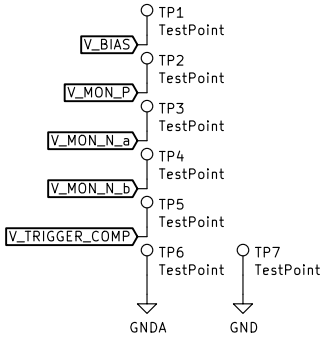












Author: Tijmen van Eijk
Single Quantum

Sheet: /
File: test_board_CU_v2.sch

Title: Test Board for Channel Unit v2

Size: A4	Date: 2020-08-14	**Rev: 1**
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D

PCB design

This appendix will hold all images from the designed PCBs.

D.1. Channel Unit

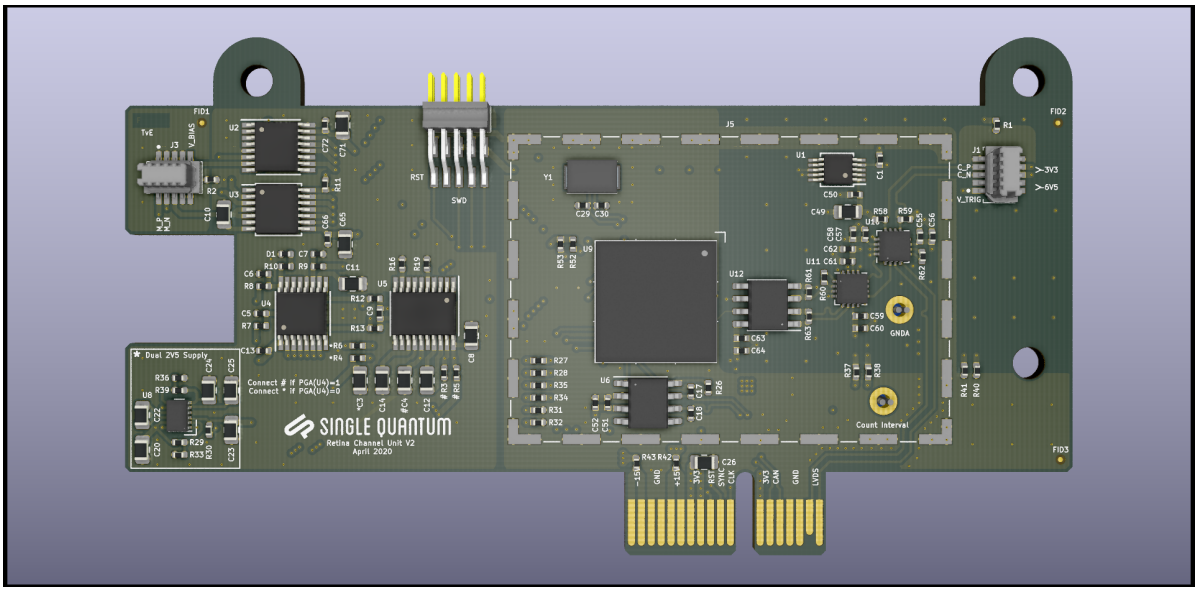

Figure D.1: Channel Unit Front.

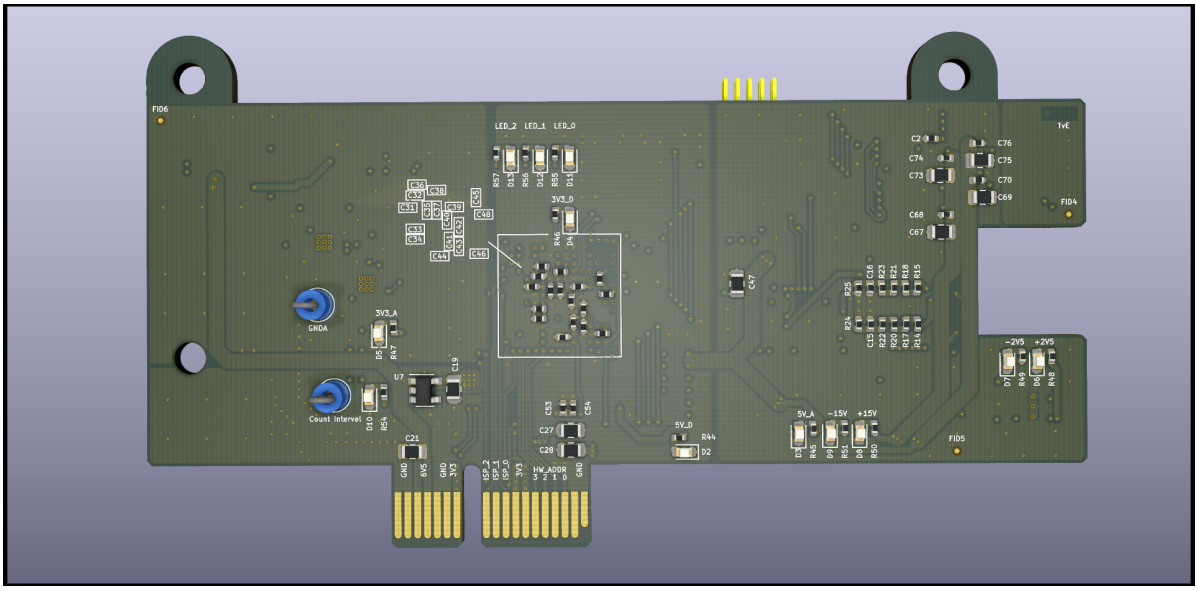

Figure D.2: Channel Unit Back.

D.2. Backplane

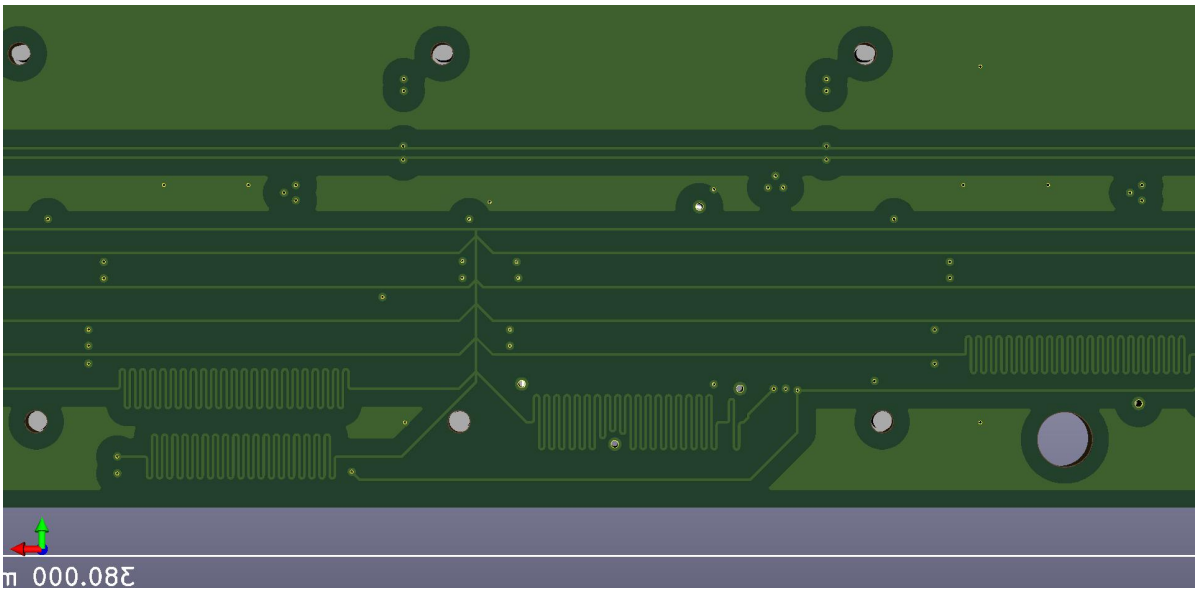

Figure D.3: Signal lines zoomed in

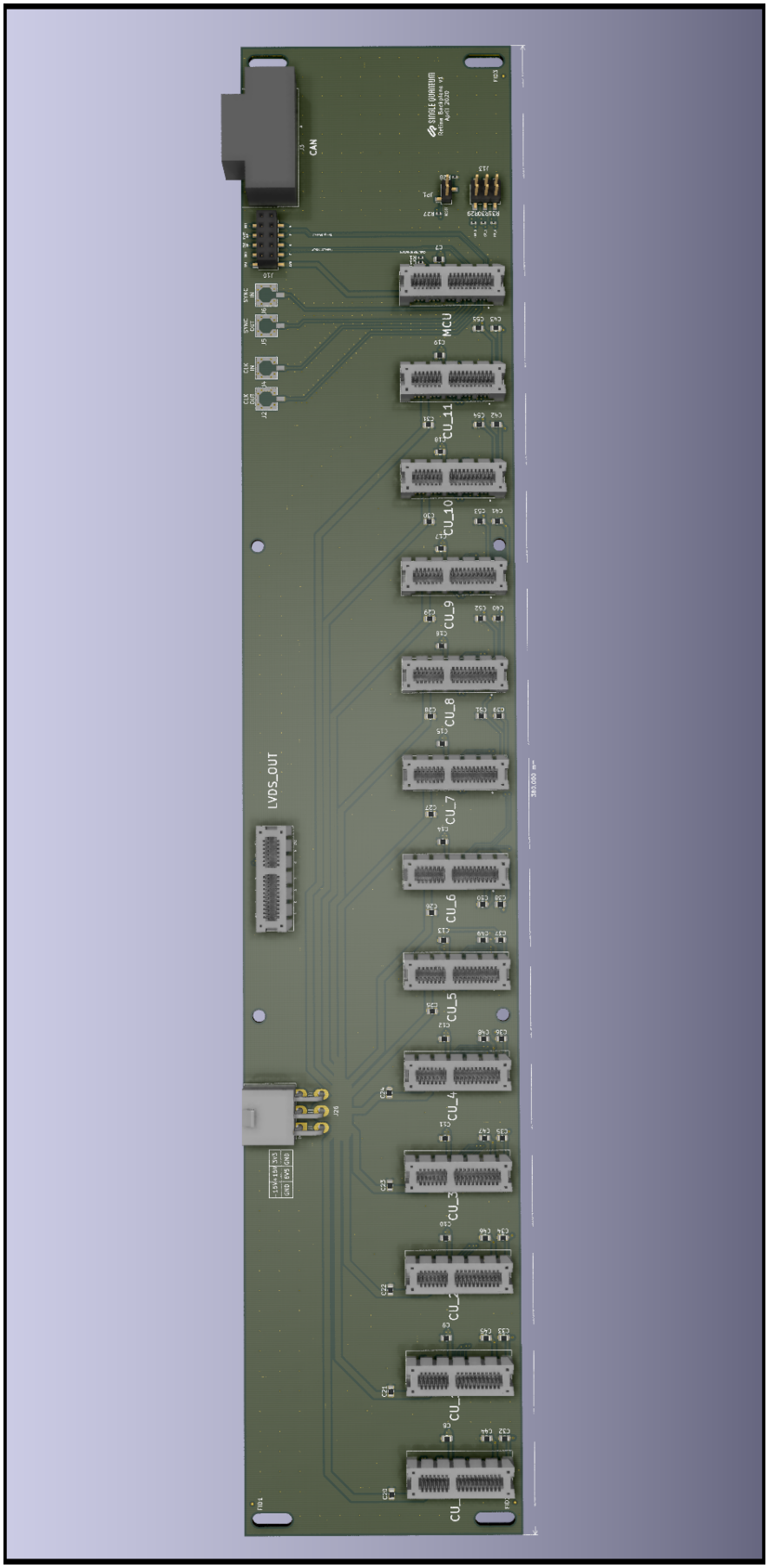

Figure D.4: Backplane front.

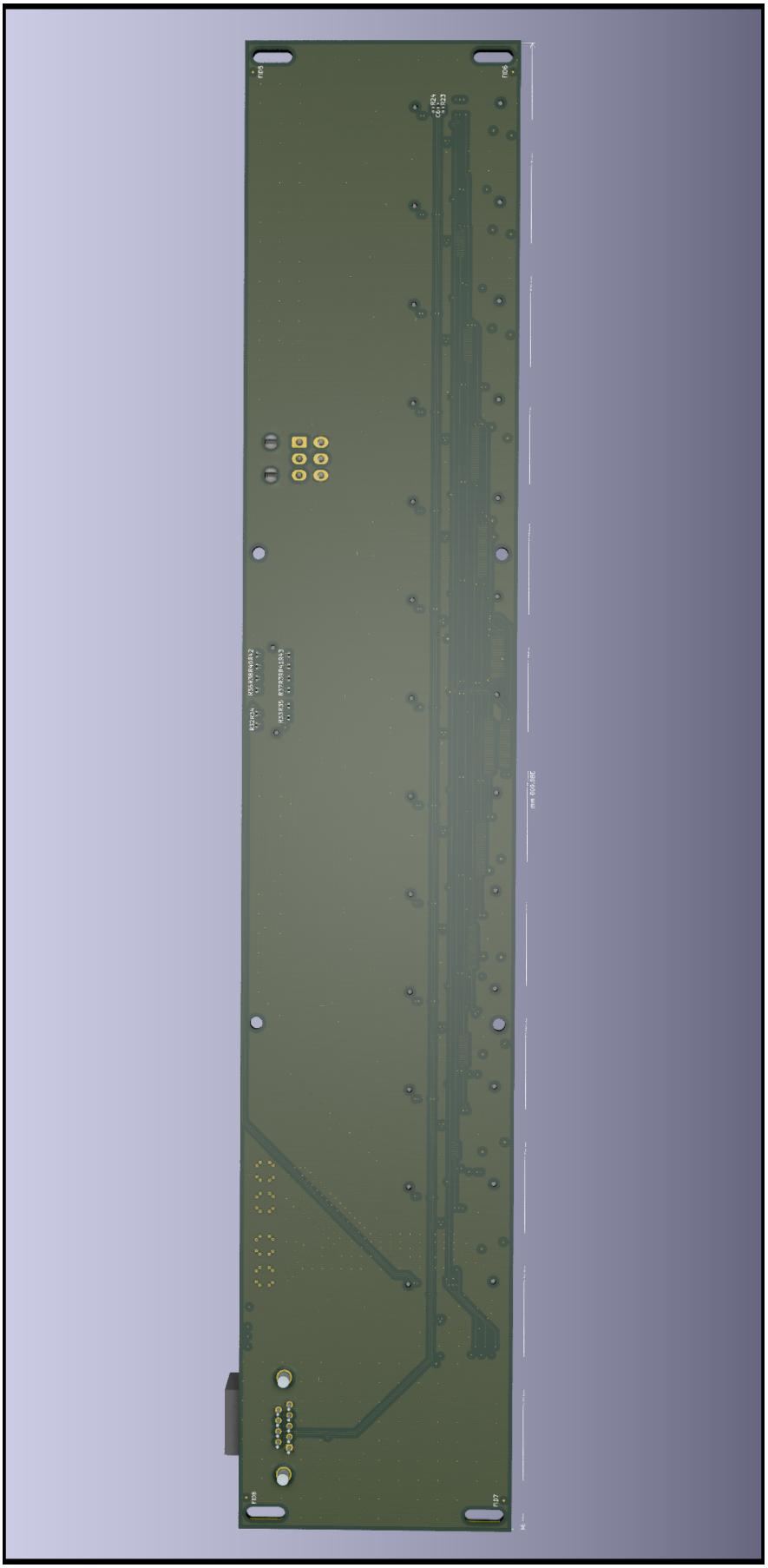

Figure D.5: Backplane bottom.

D.3. Power Supply Unit

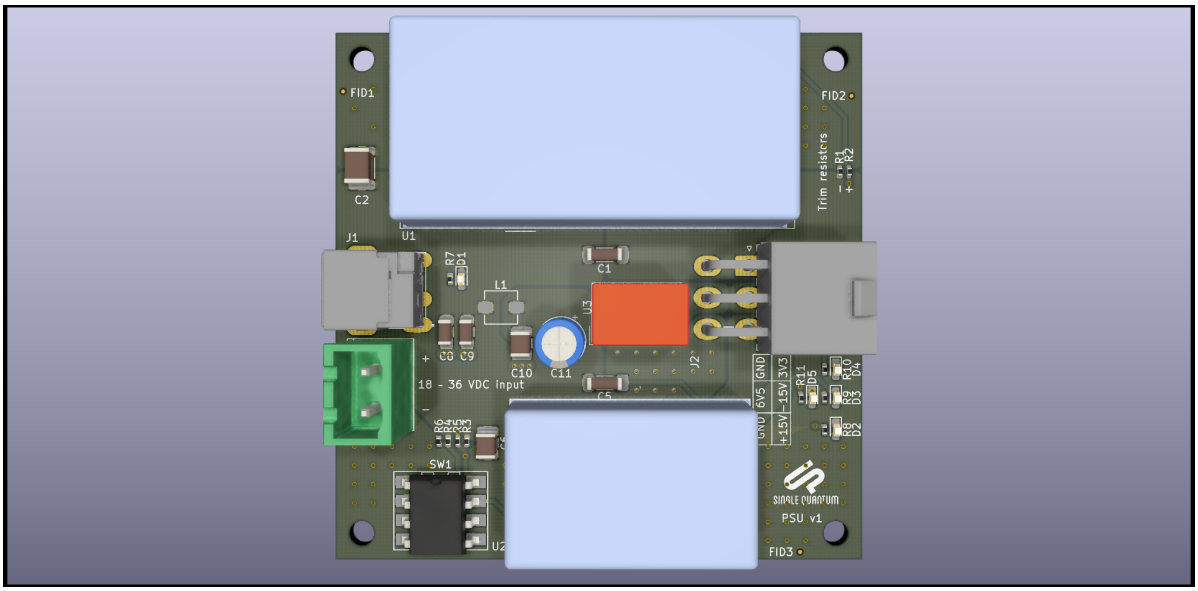

Figure D.6: Power Supply Unit front.

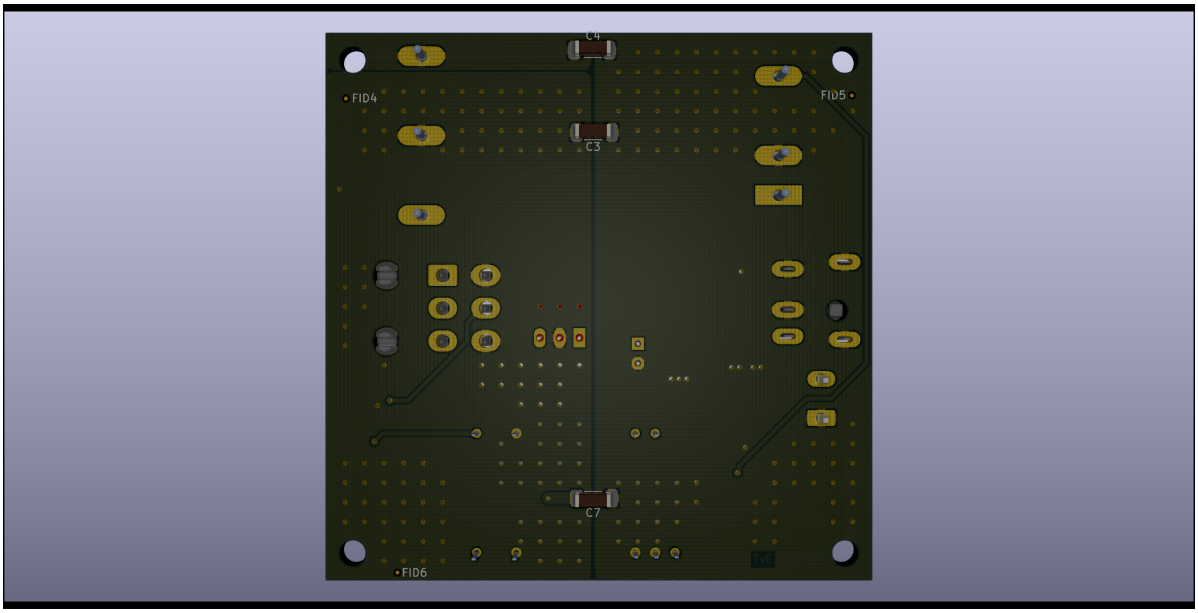

Figure D.7: Power Supply Unit back.

D.4. Test board

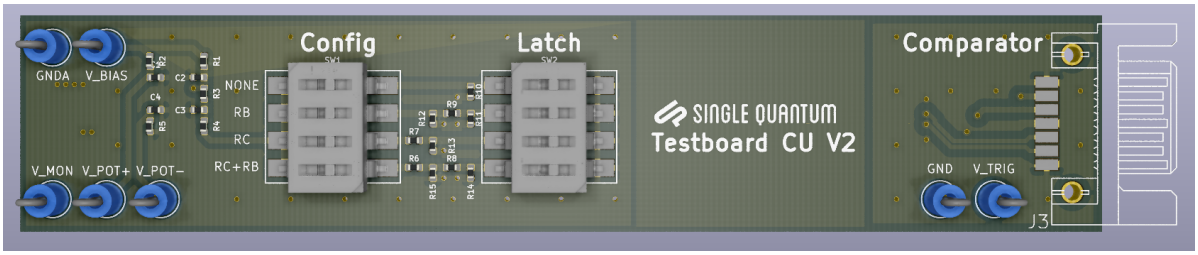

Figure D.8: Testboard Front.

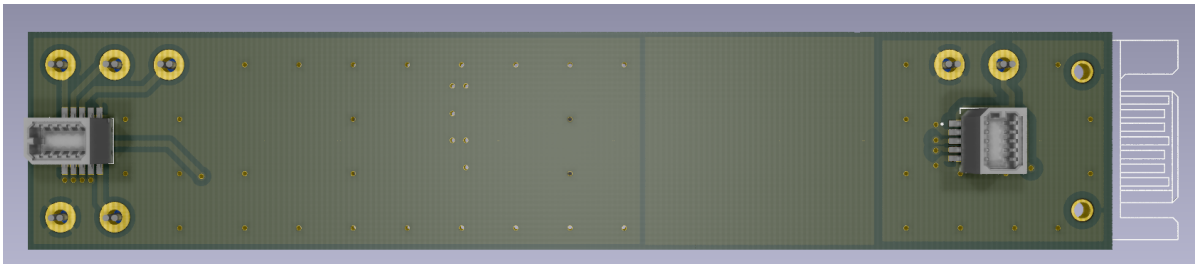

Figure D.9: Testboard Back.

E

Miscellaneous

E.1. Graphical User Interface

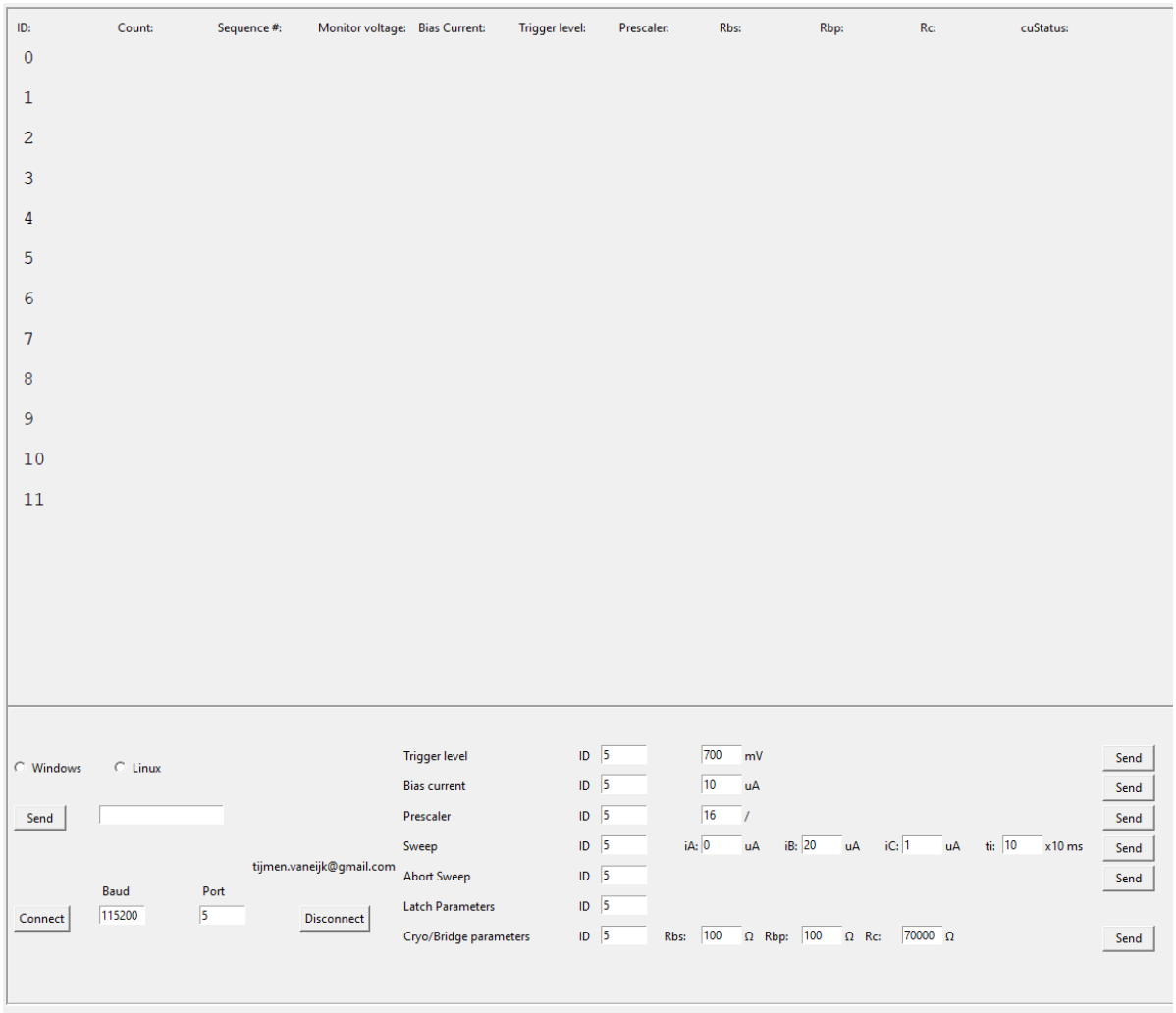

Figure E.1: UART Graphical User Interface.

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